	Case 3:17-cv-06782 Docu	ument 1 Filed 11/26/17 Page 1 of 9
1 2 3 4 5 6 7 8 9	Duncan M. McNeill 1514 Van Dyke Avenue San Francisco, CA 94124 415 752-5063 Telephone 415 752-5063 Facsimile dmcneill1@netzero.com Fed. Bar No. 136416 David Fink (pro hac vice to be filed) Fink & Johnson 7519 Apache Plume Houston, TX 77071 713 729-499a Telephone 713 729-8408 Facsimile	
10	UNITED STATES DISTRICT COURT	
11 12	FOR THE NORTHERN DISTRICT OF CALIFORNIA	
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14	JAMES B. GOODMAN,	Civil Action No.
15	Plaintiff,	COMPLAINT FOR PATENT
16	vs. LENOVO (UNITED STATES) INC.	INFRINGEMENT AND DEMAND FOR JURY TRIAL
17 18	Defendant.	
19	*****	*****
20	NOW COMES Plaintiff, JAMES B. GOODMAN ("Goodman"), through his attorney,	
21	and files this Complaint for Patent Infringe	ment and Demand for Jury Trial against Lenovo
22	United States) Inc ("Lenovo").	
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24	PARTIES	
25	1. Goodman is an individual residing in the State of Texas.	
26	2. Lenovo is a Delaware corpo	ration with its principal place of business at 1009
27	Think Place, Morrisville, NC 27560.	
28	3. Lenovo maintains an office in this Judicial District at 3325 Scott Blvd., Santa	
	Clara, CA 95054.	
		Page 1

3.	On information and belief, Lenovo is a recognized innovative leader in consumer
	electronics products, including laptop computers, mobile devices and desktop
	computers.
4.	On information and belief, products sold by Lenovo are sold under the trademark
	"Lenovo" to indicate that the products are connected to Lenovo.
5.	On information and belief, Lenovo sells its consumer electronics products
	throughout the U.S. in stores and on the internet.
6.	On information and belief, Lenovo sells its consumer electronics products through
	retail stores in this Judicial District.
	JURISDICTION AND VENUE
7.	Lenovo maintains an office in this Judicial District, and is using and selling in this
	Judicial District products infringing U.S. Patent No. 6,243,315 ("315 Patent") in
	violation of 35 U.S.C. § 271.
8.	Litigation to enforce the '315 Patent under 35 U.S.C. § 281 is proper.
9.	This Court has original jurisdiction for this patent infringement case under
	35 U.S.C. § 1338(a) and 35 U.S.C. § 1331.
10.	Venue is proper in this Judicial District under 28 U.S.C. § 1391(d) and 1400(b) in
	view of the presence of Lenovo with permanent offices in this Judicial District,
	and the infringing activities of Lenovo in this Judicial District.
F	BACKGROUND RELATING TO GOODMAN AND HIS PATENT
11.	Goodman is the inventor and patent owner of the '315 Patent. The '315 Patent
	leaped into importance when the manufacturers discovered the enormous
	advantages of incorporating the claimed invention of the '315 Patent to reduce
	power consumption and inhibit errors in devices requiring memories systems.
12.	Many of the mobile phones, and computer related products sold in this Judicial
	District by Lenovo incorporate memory products known in the industry as DDR3,
	and DDR4 memory products. Variations of these memory products such as the
	DDR3 memory product include DDR3-800, DDR3-1066, DDR3-1333, DDR3-
	4. 5. 6. 7. 8. 9. 10. H 11.

		Case 3:17-cv-06782 Document 1 Filed 11/26/17 Page 3 of 9
1		1600, and DDR3-1666 as well as DDR3L-800, DDR3L-1066, DDR3L-1333,
2		DDR3L-1600, and DDR3L-1666. The use of the terms "DDR3", and "DDR4" to
3		include in the designation of a memory product in the industry requires the
4		performance of the memory product to comply with the respective industry
5		standards for performance, and operations.
6	13.	The standards published by the Joint Electron Device Engineering Council Solid
7		State Technology Association ("JEDEC") state for the respective DDR3, and
8		DDR4 memory products and their variation: "No claims to be in conformance
9		with this standard may be made unless all requirements stated in the standard are
10		met."
11	14.	On information and belief, the use of the terms "DDR3", and "DDR4", and
12		variations of each implies that the respective memory products complies with the
13		corresponding JEDEC Standards.
14	15.	Therefore, the DDR3, and DDR4 memory products and their variations must
15		operate in compliance with the respective standards established by the JEDEC
16		Solid State Technology Association, 3103 North 10th Street, Suite 240-S,
17		Arlington, VA 22201.
18	16.	Any memory product identified as being a DDR3 memory product, or a variation
19		thereof including the term "DDR3" must comply with JEDEC Standard
20		JESD79-3F.
21	17.	Any memory product identified as being a DDR4 memory product, or a variation
22		thereof including the term "DDR4" must comply with JEDEC Standard
23		JESD79-4A.
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Case 3:17-cv-06782 Document 1 Filed 11/26/17 Page 4 of 9

18. On information and belief, the JEDEC Standards for DDR3, and DDR4 memory products have several relevant operating capabilities in common when installed in a Lenovo mobile phone, or computer related product, for example: (a) Each memory product has at least two banks of volatile memory, and this is the equivalent of a plurality of volatile solid state memory devices under the doctrine of equivalents; (b) A first external device (supplied by Lenovo mobile phone, and computer related product) connected to the memory product can provide signals for selectively electrically isolating the address and control lines so that signals on the address and control lines do not reach the memory devices; and (c) A second external device (supplied by Lenovo mobile phone, and computer related product) connected to the memory product can determine when the memory system is not being accessed and can initiate a low power for the memory system wherein the first external device isolates the memory devices and places the memory devices in self refresh mode, thereby reducing the electrical energy drawn from the electrical power supply of the Lenovo mobile phone, and computer related product.

- 19. On information and belief, the aforementioned Lenovo computer related products incorporating a DDR3, and DDR4 provide the aforementioned first and second external devices in order to take advantage of the respective operating specification of the memory products, including the low power mode which saves electrical energy while protecting the memory product against potential signals which could damage or corrupt the stored data.
 - 20. The following is a Claim Chart for Claim 1 of the '315 Patent for the DDR3 memory product (and similarly applies to the DDR4 memory product) incorporated into a Lenovo mobile phone, or computer relates systems:

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	Case 3:17-cv-06782 Docu	ment 1 Filed 11/26/17 Page 5 of 9
1 2	CLAIM CHART AND A	ASSOCIATED CONSTRUCTION
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4	U.S. Patent No. 6,243,315	LENOVO MOBILE PHONE, OR COMPUTER RELATED SYSTEM
5		HAVING AN INSTALLED DDR3 MEMORY PRODUCT AND PROVIDING
6		THE AFOREMENTIONED FIRST AND SECOND EXTERNAL DEVICES
7 8	Claim 1. A memory system for use in a computer system, said memory system comprising:	A "memory system" can be construed to be "a system capable of retaining data". The JEDEC Standard JESD79-3F specification at
9	·····	p. 18, Sec. 3.2. "The DDR3 SDRAM is a
10		high-speed dynamic random-access memory ". On the same page, "an interface designed to transfer two data words per clock cycle".
11		The DDR3 memory product retains data.
12		Thus, this memory product is within the preamble description.
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devi elec mer	urality of volatile solid state memory ces that retain information when an trical power source is applied to said nory devices within a predetermined age range and	A "memory device" can be construed to be an "integrated circuit or chip"; and "a plurality of volatile solid state memory devices" can be construed to be "two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while a electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information".
		The JEDEC Standard JESD79-3F at p. 109, Sec. 6.1 states the absolute maximum DC Ratings. P. 111, Sec. 7.1 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages.
		The JEDEC Standard JESD79-3F in at p. 77 refers to the memory module as being a "chip". See Sec. 4.15.
		The JEDEC Standard JESD79-3F at p. 18, Sec. 3.2 states, "The DDR3 SDRAM is a high-speed dynamic random-access internally configured a an eight-bank DRAM." The second paragraph describes how a bank can be selected. See the Command Truth Table at p. 33, Sec. 4.1, and NOTE 3 explains that "BA" is for the selection of a bank being operated upon. Hence, the DDR3 has eight memory banks and the equivalents of a plurality of solid state memory devices.
		On information and belief, a DRAM is volatile memory and that means a voltage in a specific range must be applied to operate acceptably as pointed out above.
mod	able of being placed in a self refresh le; said memory devices having address s and control lines;	The JEDEC Standard JESD79-3F shows that the DDR3 is capable of being refreshed at p. 13, Sec. 2.10 for CKE, (CKE0), (CKE1) "Self-Refresh operations (all banks idle)"; p. 17, Sec. 3.1 on the diagram; p. 31, Sec. 3.4.4.1 entitled "Partial Array Self-Refresh (PASR)"; p. 35, Sec. 4.2 shows an entry for "Self-Refresh"; p. 46, Sec. 4.9.0.1 entitled, "Auto Self-Refresh"; and p. 79, Sec. 4.16 entitled "Self-Refresh Operation".

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2 3 4 5 6 7 8 9 10 11 12 13 14 15	a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	JEDEC Standard JESD79-3F at p. 81, Sec. 4.17.1 entitled "Power-Down Entry and Exit" discloses a power-down operation. The description states, "Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cylce(s) after, this timing period are defined as tCPDED. CKE low will result in deactivation of command and receivers after tCPDED has expired. The text also states, "In power-down mode, CKE low, RESET# high, and stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care." The input signals are address and control signals are related to the CK# input noted at p. 13, Sec. 2.10, where it is stated, "All Address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.		
 15 16 17 18 19 20 21 22 23 24 25 26 27 28 	a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	The power-down is due to an input signal from the second external device as pointed out at P. 13, Sec. 2.10. The device generating the input signal for the power-down functions like the claimed memory access enable control device. JEDEC Standard JESD79-3F, Sec. 4.17.1 states, "Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operations are in progress.		
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Case 3:17-cv-06782 Document 1 Filed 11/26/17 Page 8 of 9

21. The respective DDR3, and DDR4 memory products are typically incorporated into the Lenovo mobile phones and computer related products on what is known in the industry as a "motherboard", and other components on the motherboard provide subsystems to monitor activity in the mounted memory product, initiate the reduced power down mode, to inhibit responses in the memory products on the motherboard, and other requirements of the respective JEDEC standard.

COUNT ONE (DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,243,315)

- 22. Plaintiff Goodman repeats and incorporates herein the allegations contained in paragraphs 1 through 21 above.
- On June 5, 2001, the '315 Patent entitled "COMPUTER MEMORY SYSTEM WITH A LOW POWER MODE", was duly and legally issued to James B. Goodman, as the sole patentee.
- 24. Plaintiff Goodman is the sole owner of the '315 Patent, and has standing to bring this action.
- 25. All of the limitations of Claim 1 of the '315 Patent are present in Lenovo related mobile phones, or computer products incorporating at least one DDR3, or DDR4 memory product offered for sale, and being sold directly or indirectly by Lenovo in this Judicial District.
- 26. Lenovo is infringing claim 1 of the '315 Patent literally, or under the doctrine of equivalents in this Judicial District.

Case 3:17-cv-06782 Document 1 Filed 11/26/17 Page 9 of 9

JURY DEMAND

Pursuant to Fed. R. Civ. P. 38(b), Plaintiff hereby demands a jury trial as to all issues in this lawsuit.

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4		PRAYER FOR RELIEF
5	THER	EFORE, Plaintiff respectfully requests this Court to:
6	a.	enter judgment for Plaintiff on Claim 1 of the '315 Patent for patent infringement,
7		either literally, and/or under the doctrine of equivalents against Lenovo;
8	b.	order that an accounting be had for the damages caused to the Plaintiff by the
9		infringing activities of the Lenovo;
10	с.	enter an injunction to prohibit Lenovo from directly or indirectly from offering for
11		sale, or selling infringing products;
12	d.	award Plaintiff interest and costs from Lenovo; and
13	e.	award Plaintiff such other and further relief as this Court may deem just and
14		equitable.
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18		Respectfully submitted,
19		<u>/s/ Duncan M. McNeill</u> Duncan M. McNeill
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21		1514 Van Dyke Avenue San Francisco, CA 94124 415 752-5063 Telephone 415 752-5063 Facsimile
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