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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

POLARIS INNOVATIONS LTD., an Ireland limited company, Plaintiff, v. ELITE SEMICONDUCTOR MEMORY TECHNOLOGY INC., a Taiwan corporation, Defendant.	No. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

Polaris Innovations Limited ("Polaris") files this Complaint against Elite Semiconductor Memory Technology, Inc. ("ESMT"), for its infringement of United States Patents 6,653,882 B2, 6,728,143 B2, and 7,532,523 B2. Polaris alleges as follows:

PARTIES

1. Polaris is a limited company organized and existing under the laws of the Republic of Ireland, with its principal place of business at 29 Earlsfort Terrace, Dublin 2, Republic of Ireland.

2. ESMT is a corporation organized and existing under the laws of Taiwan, with its principal place of business at No.23, Industry E Rd. IV Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.

JURISDICTION

3. Polaris brings this action under the patent laws of the United States, 35 U.S.C. § 1 *et. seq*. This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

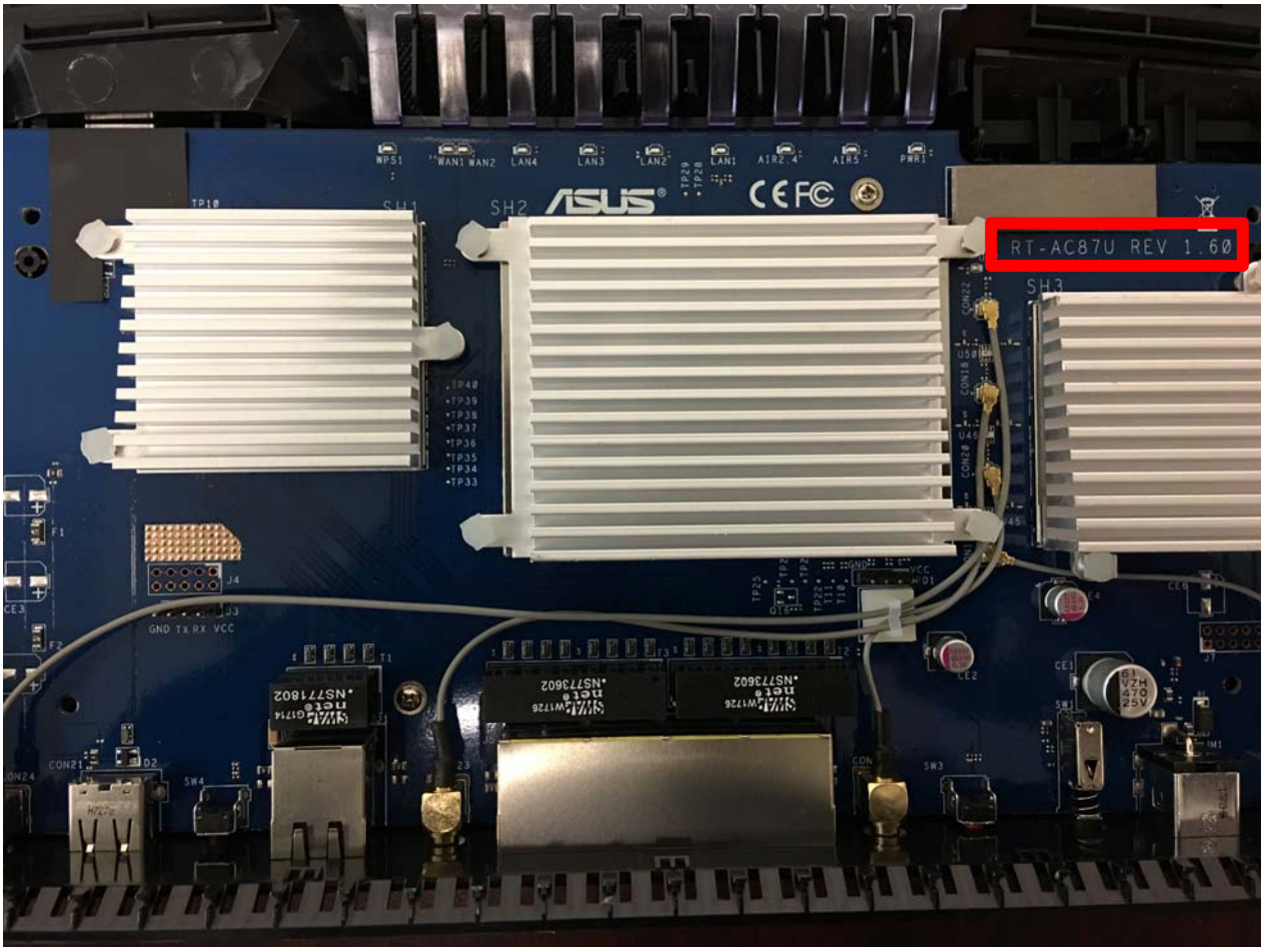
VENUE

4. Venue is proper in this District under 28 U.S.C. §§ 1391and 1400(b).

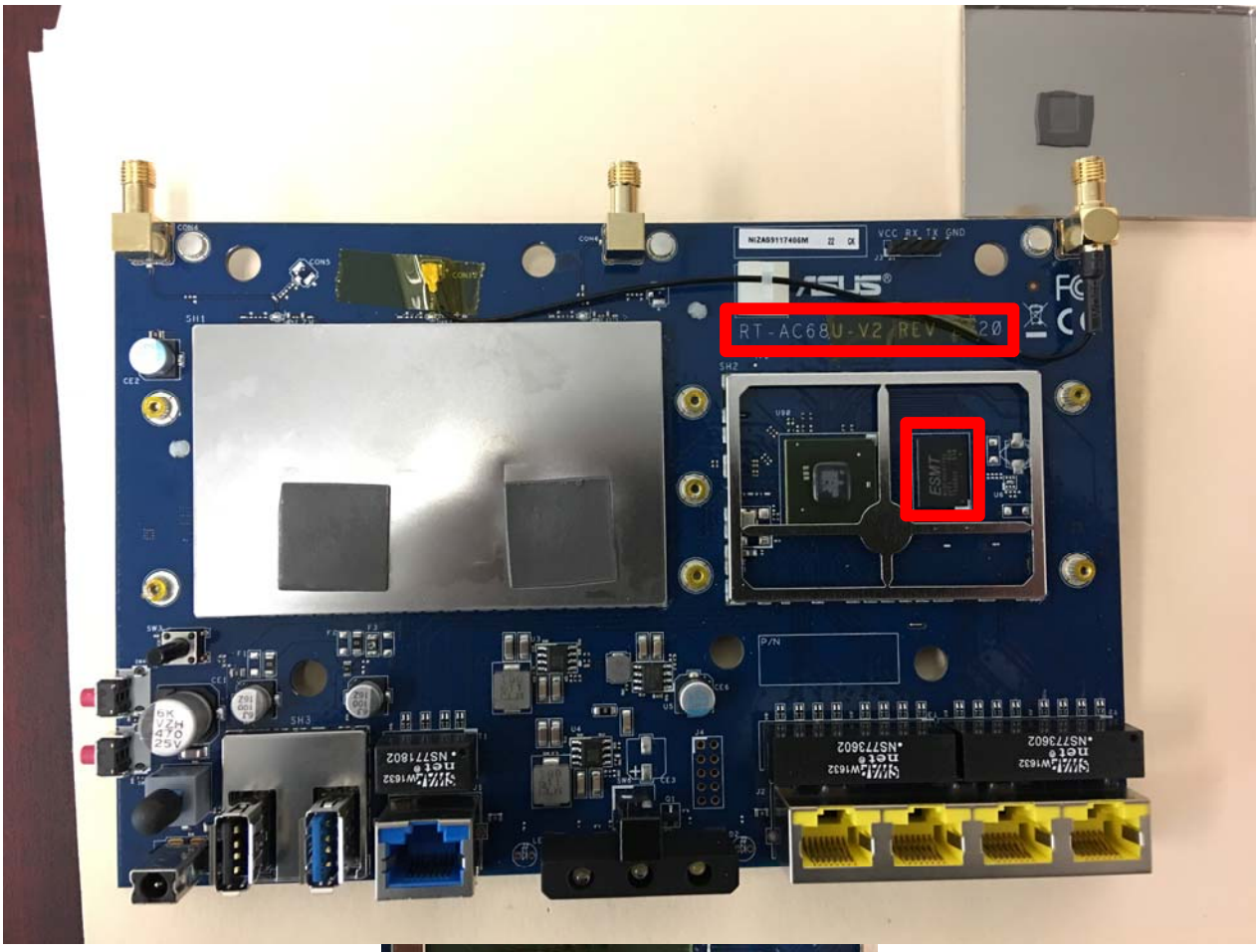
5. ESMT is subject to personal jurisdiction before this Court. ESMT purposefully directed its infringing activities to residents of California by selling its infringing memory chips to electronics manufacturers such as LG Electronics Inc., AsusTek Computer Inc., and D-Link Corporation, knowing that the infringing memory chips are incorporated into LG, Asus, and D-Link-branded products, such as televisions and wireless routers, that are sold through established distribution channels, up to and including electronics retailers in California and in this District.

6. For example, infringing ESMT memory chips are incorporated into Asus routers such as the RT-AC87U, *see e.g.* https://frys.com/product/8242606, and RT-AC68U, *see e.g.*, https://frys.com/product/7879149. The RT-AC87U and RT-AC68U are sold at retail electronics stores in this District, and contain infringing ESMT DDR3 memory chips.

7. The RT-AC87U contains the accused ESMT M15F1G1664A DDR3 memory chip:



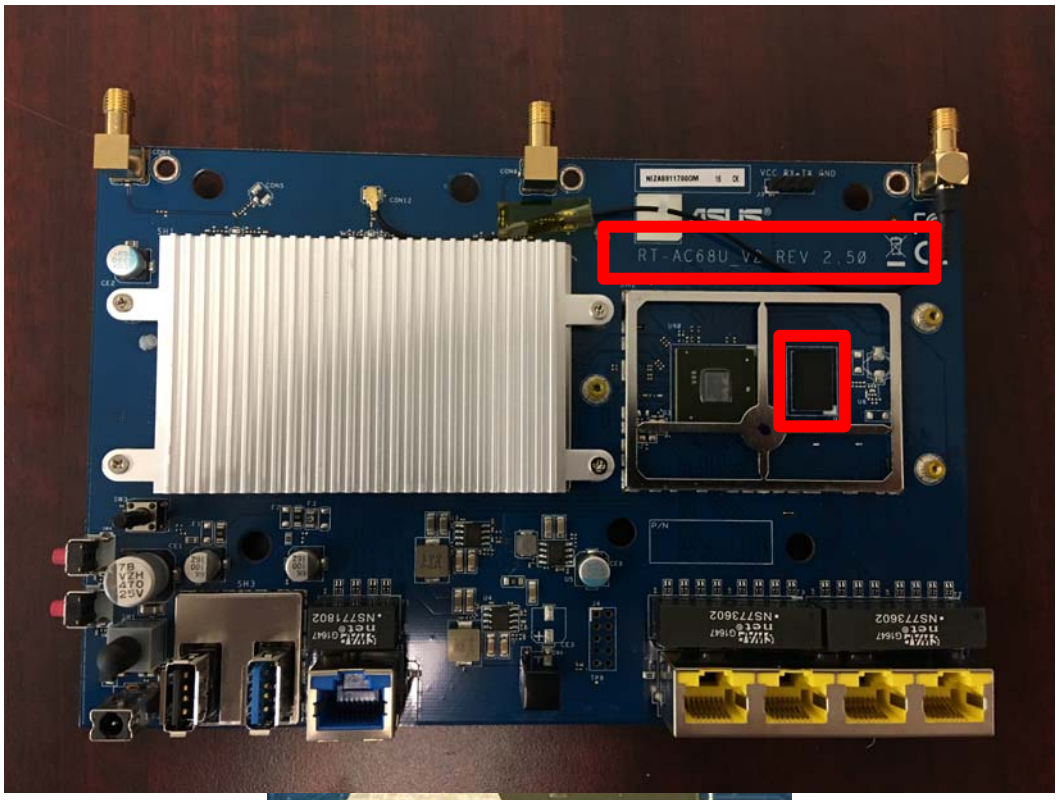
8. The RT-AC68U contains the infringing ESMT M15F2G16128A DDR3 memory chip:

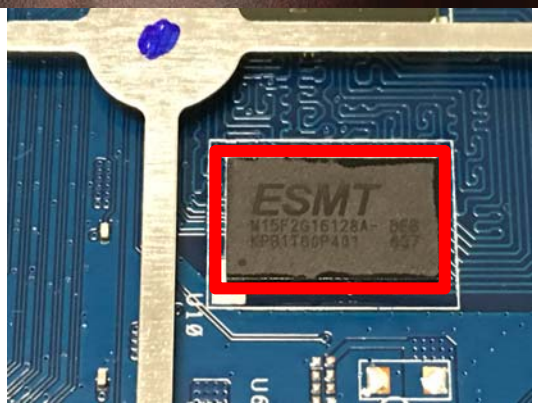

RT-AC68U-V2


ESMT
M15F2G16128A
KPF1 -BDB
T50E603 618

9. ESMT memory chips are also incorporated into Asus routers that are exclusive to US retailers. For example, the Asus RT-AC1900P router is exclusive to Best Buy, and is available at Best Buy stores within this District. *See e.g.*, https://www.bestbuy.com/site/asus-wireless-ac-dual-band-wi-fi-router-black/5091000.p?skuId=5091000.

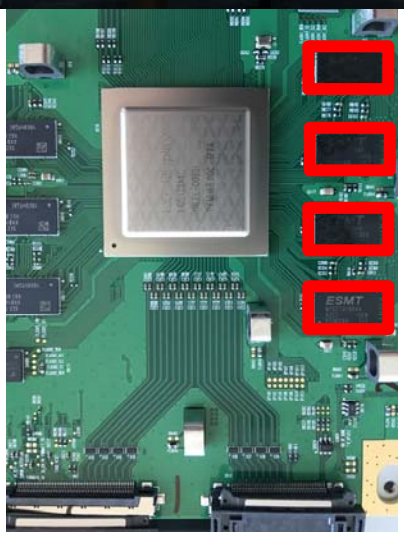
10. The Asus RT-AC1900P contains an infringing ESMT MF15F2G16128A DDR3 memory chip:





11. Infringing ESMT memory chips also are incorporated into televisions manufactured by LG, such as the OLED55C7P 55" OLED 4K Ultra HD TV with HDR. The OLED55C7P 55" OLED 4K Ultra HD TV with HDR is available for retail purchase in California and in this district at electronics retailers such as Best Buy and Frys Electronics. *See e.g.,* https://www.bestbuy.com/site/lg-55-class-54-6-diag--oled-2160p-smart-4k-ultra-hd-tv-with-high-dynamic-range/5763400.p?skuId=5763400; https://frys.com/product/9104898.

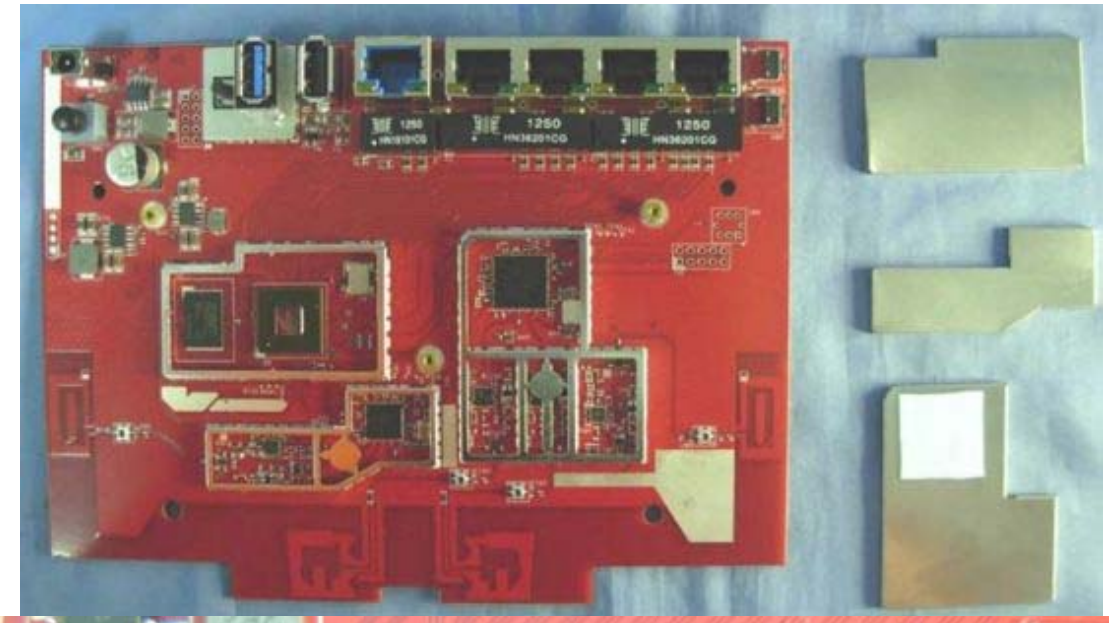
12. The LG OLED55C7P 55" OLED 4K Ultra HD TV with HDR contains at least 4 infringing ESMT M15T1G1664A DDR3 memory chips:

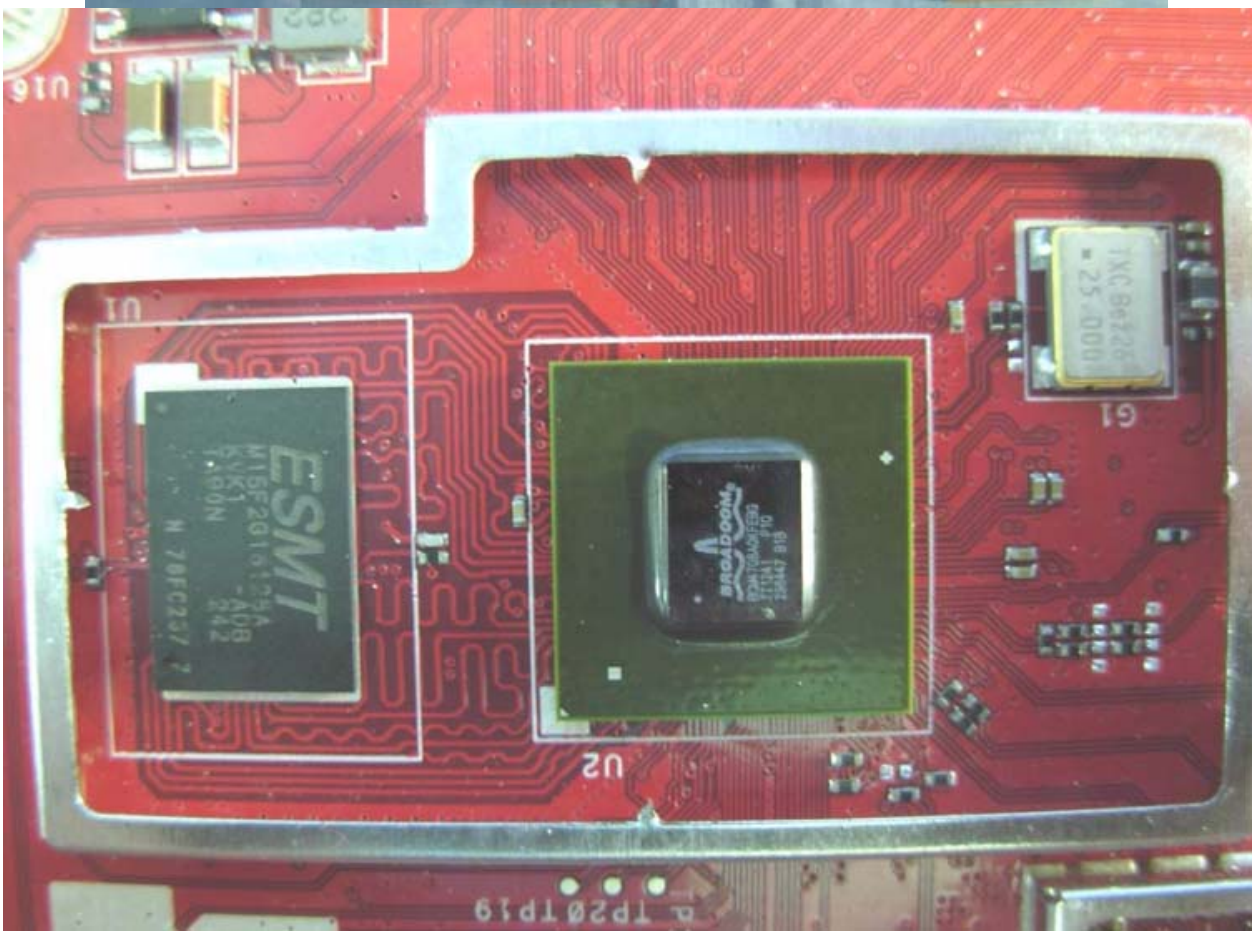


13. Upon information and belief, infringing ESMT DDR3 chips have also been incorporated into the LG OLED55C6P television, sold in this district within the last 6 years.

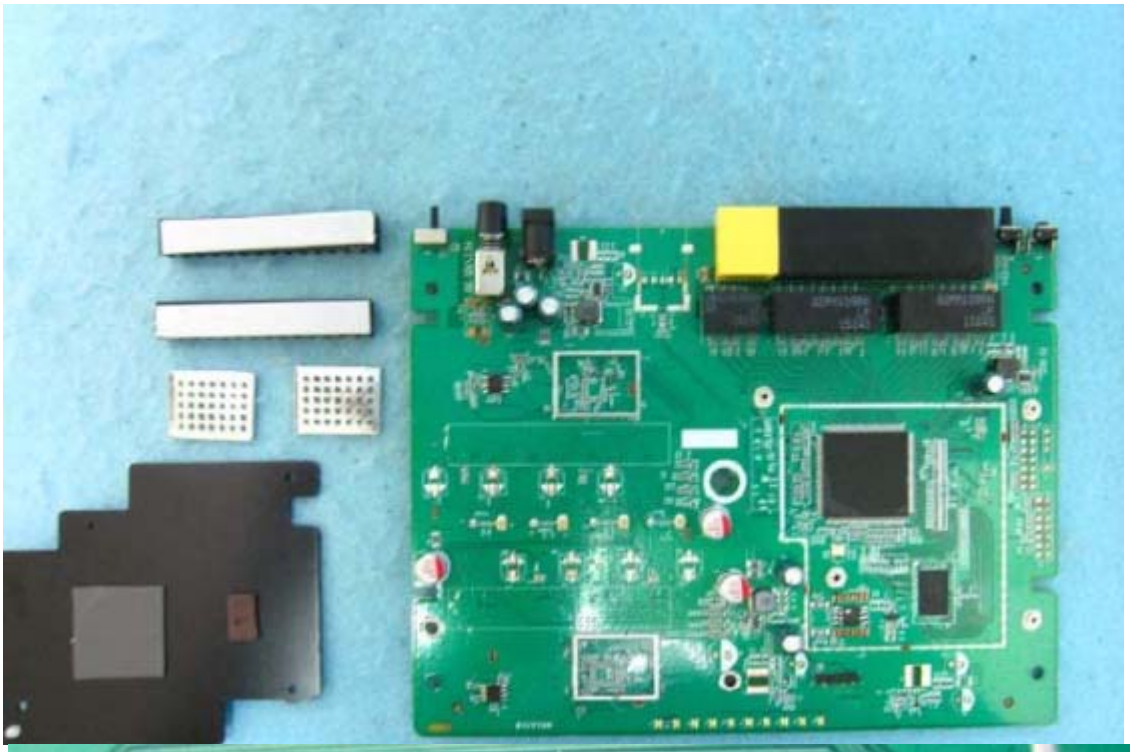
14. Upon information and belief, Asus and D-Link have each represented to the FCC that infringing ESMT DDR3 chips were incorporated into the following products, each sold in this District within the last six years:

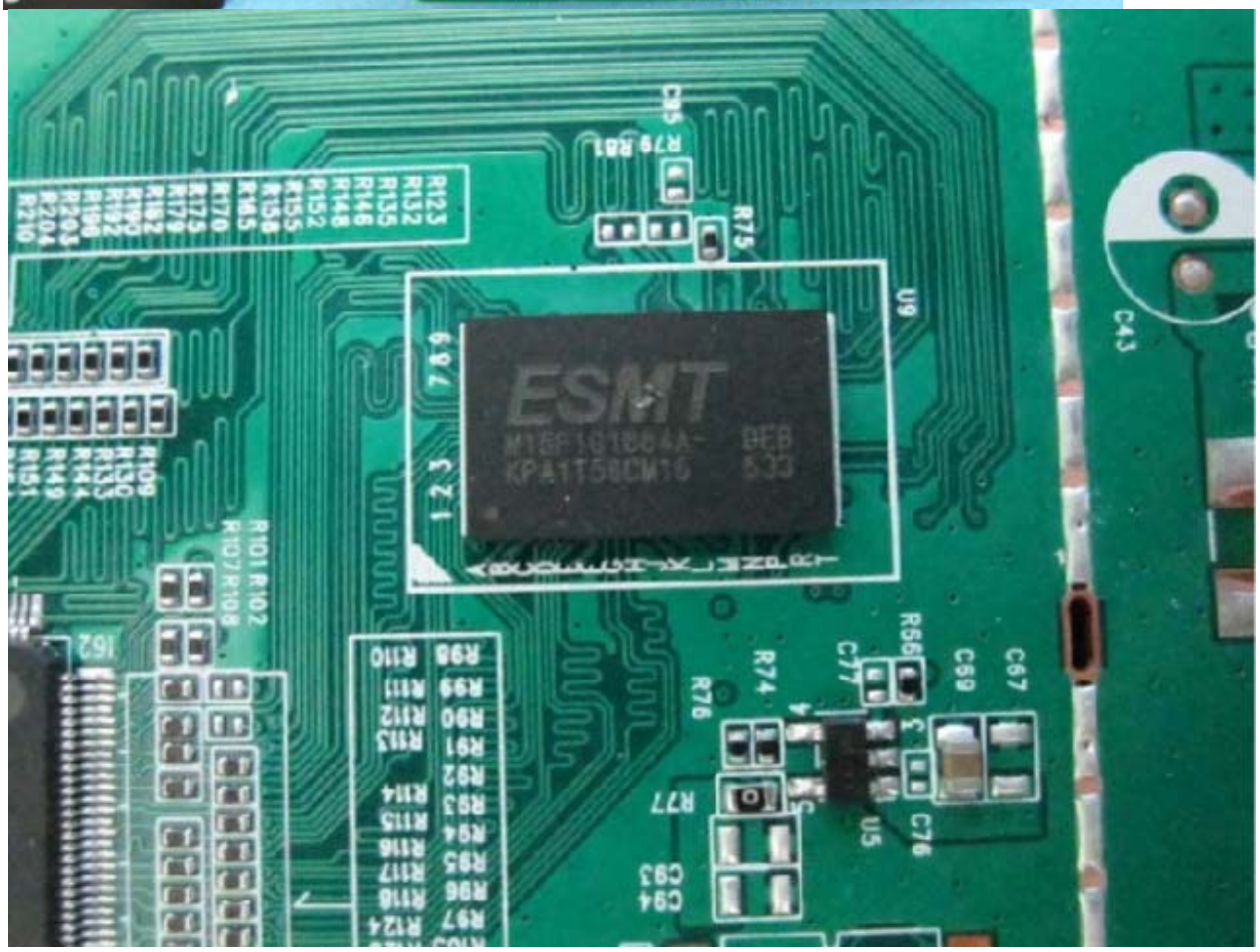
a. Asus RT-AC56U Router



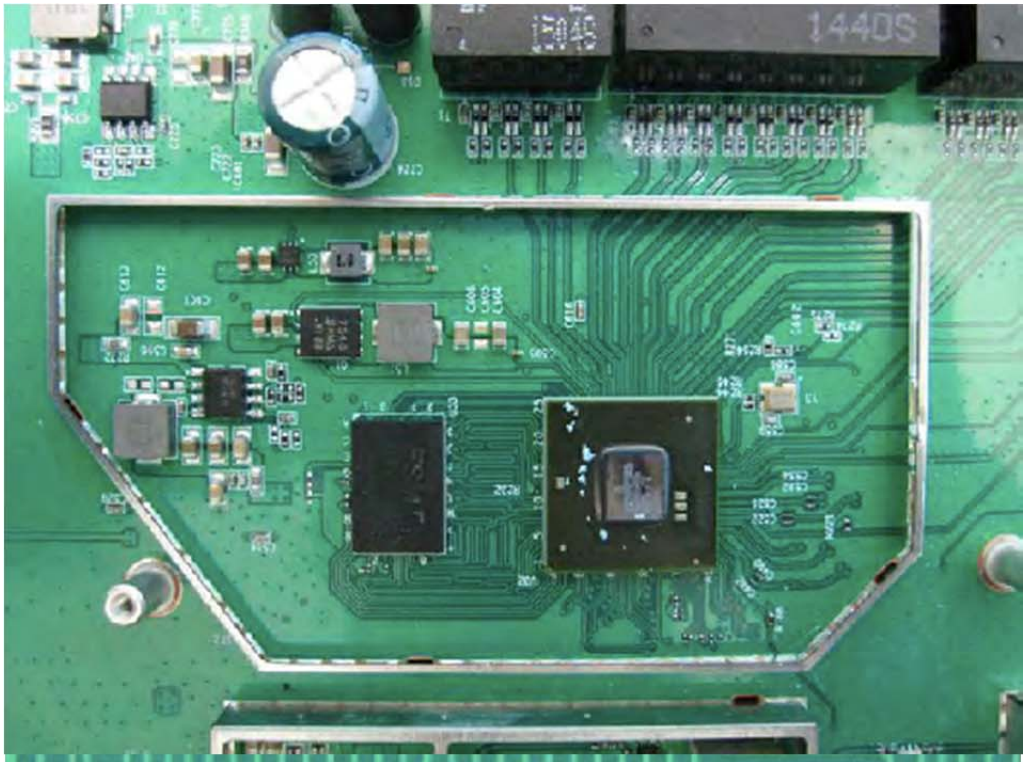


b. D-Link DIR-879 Router





c. D-Link IR895LA1 Router



INTRADSTRICT ASSIGNMENT

15. This is an Intellectual Property Action pursuant to Local Rule 3-2(c).

THE PATENTS IN SUIT

16. On November 25, 2003, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,653,882 B2 ("'882 Patent"), which is entitled "Output Drivers for IC," and identifies Arindam Raychaudhuri as the sole inventor. A true and correct copy of the '882 Patent is attached hereto as Exhibit A. The '882 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '882 Patent, including the right to collect and receive damages for past, present and future infringement of the '882 Patent.

17. On April 27, 2004 the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,728,143 B2 ("the '143 Patent"), which is entitled "Integrated Memory," and identifies Robert Feurle as the sole inventor. A true and correct copy of the '143 Patent is attached hereto as Exhibit B. The'143 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '143 Patent, including the right to collect and receive damages for past, present and future infringement of the '143 Patent.

18. On May 12, 2009 the United States Patent and Trademark Office duly and legally issued United States Patent No. 7,532,523 B2 ("the '523 Patent"), which is entitled "Memory Chip With Settable Termination Resistance Circuit," and identifies Georg Braun, Christian Weis, and Eckehard Plaettner as inventors. A true and correct copy of the '523 Patent is attached hereto as Exhibit C. The '523 Patent has been assigned to Plaintiff Polaris. Polaris holds all right, title, and interest in the '523 Patent, including the right to collect and receive damages for past, present and future infringement of the '523 Patent.

19. The '882 Patent discloses inventions related to integrated circuit devices including, for example, SDRAM devices used in personal computer systems, among other products. The inventions of the '882 Patent generally are directed to a novel output driver circuit that improves data transfer speeds from an integrated circuit to other circuits in a computer system. The '143 Patent discloses inventions related to integrated memory devices such as SDRAM that can be used in personal computer systems and other products. The inventions of the '143 Patent

generally are directed to improving memory access times, and thus the operating speed of a memory device, by employing a novel control circuit for performing memory accesses. The '523 Patent discloses inventions related to integrated memory devices such as SDRAM that can be used in personal computer systems and other products. The inventions of the '523 Patent generally are directed to a novel memory chip that optimally sets terminations at a terminal of the memory chip by variably setting the terminations in accordance with the claims of the '523 Patent.

20. The usefulness and value of the patents in suit has been acknowledged by various companies engaged in the design, manufacture, and sale of SDRAM devices. Polaris has widely licensed the patents in suit to numerous SDRAM manufacturers, among others, some of which compete with ESMT for sales of SDRAM devices.

21. Polaris has offered to license the patents in suit to ESMT, but ESMT has not agreed to license the patents in suit. Polaris has therefore been compelled to file this suit to protect its rights.

FIRST CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,653,882

22. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

23. ESMT has infringed, and continues to infringe, at least claims 1 and 4 of the '882 Patent. ESMT sells, or offers to sell in the United States, products, such as DDR3L SDRAM, including the ESMT M15F1G1664A, MF15F2G16128A , and M15T1G1664A DDR3(L) SDRAM chips (individually and collectively, "ESMT DDR3 SDRAM"), that meet each and every limitation of claim 1.

24. Claim 1 of the '882 Patent is directed to an output driver for an integrated circuit. The output driver comprises:

a. a driver circuit for driving an external circuit, the driver circuit having:

i. a data input connected to the integrated circuit;

ii. a data output connected to a transmission line leading to the external circuit;

iii. and an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data;

b. a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line being electrical replicas of the driver circuit and the transmission line, respectively;

c. and an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means,

i. wherein the impedance control circuit is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit, wherein the dummy driver circuit is a scaled down replica of the driver circuit.

25. The ESMT DDR3 SDRAM meets each and every limitation of claim 1. For example, the ESMT DDR3 SDRAM is an integrated circuit that contains an output driver for driving an external circuit. The output driver of the ESMT DDR3 SDRAM includes a driver circuit, for example, a DQ Buffer, having a data input connected to the integrated circuit and a data output connected to a transmission line leading to the external circuit.

26. The ESMT DDR3 SDRAM is capable of adjusting the output impedance of the driver circuit, and does so through an impedance adjusting means for adjusting the output impedance of the driver circuit according to impedance adjusting data. For example, the ESMT DDR3 SDRAM adjusts the output impedance of the driver circuit using pull-up and pull-down resistors. The ESMT DDR3 SDRAM also contains a dummy circuit comprising a dummy driver circuit and a dummy transmission line, the dummy driver circuit and the dummy transmission line

are electrical replicas of the driver circuit and the transmission line, for example including the ZQ Cal module and the RZQ reference resistor of the ESMT DDR3 SDRAM, respectively.

27. The ESMT DDR3 SDRAM also contains an impedance control circuit for controlling the output impedance of the driver circuit, the impedance control circuit being connected to the dummy circuit and the impedance adjusting means. For example, the ESMT DDR3 SDRAM uses the ZQ Calibration command to calibrate DRAM Ron values, corresponding to the output impedance of the driver circuit. The ESMT DDR3 SDRAM further transfers calibrated values from the calibration engine to DRAM IO.

28. The ESMT DDR3 SDRAM's use of ZQ Calibration indicates that the impedance control circuit of the ESMT DDR3 SDRAM is configured to control the impedance of the driver circuit by determining the impedance adjusting data necessary for matching the output impedance of the dummy driver circuit to the impedance of the dummy transmission line and outputting the determined impedance adjusting data to the impedance adjusting means of the driver circuit. For example, the ESMT DDR3 SDRAM uses the ZQ Calibration command to calibrate DRAM Ron values, corresponding to the output impedance of the driver circuit. The ESMT DDR3 SDRAM further transfers calibrated values from the calibration engine to DRAM IO. The dummy driver circuit is a scaled down replica of the driver circuit.

29. Claim 4 of the '882 patent depends on claim 1, and claims "The output driver according to claim 1, wherein the driver circuit is a push-pull on-chip current driver." The driver circuit of the ESMT DDR3 SDRAM is a push-pull on-chip current driver.

30. Upon information and belief, other ESMT products similarly infringe one or more claims of the '882 Patent. The specific part numbers of all ESMT products that practice one or more claims of the '882 Patent are not presently known to Polaris. Polaris accuses of infringement all ESMT products that contain features and functions similar to those described above that practice one or more claims of the '882 Patent.

31. ESMT has had notice of the '882 Patent and of its infringement of the '882 Patent since at least September 20, 2017. Before initiating this litigation, Polaris attempted to engage ESMT in discussions about Polaris's belief that ESMT requires a license to the '882 Patent. On

the assumption that ESMT would participate in good faith licensing discussions, Polaris transmitted to ESMT information demonstrating ESMT's use of the inventions claimed in the '882 Patent. Polaris invited ESMT to discuss Polaris's concerns and to seek mutually agreeable resolution. However, ESMT did not respond to that correspondence and, to date, has not communicated with Polaris. Nevertheless, and despite its knowledge that it infringes one or more claims of the '882 Patent, ESMT continues to infringe the '882 Patent. ESMT's infringement of the '882 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

SECOND CLAIM FOR RELIEF

Infringement of U.S. Patent No. 6,728,143

32. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

33. ESMT has infringed, and continues to infringe, at least claims 1 and 2 of the '143 patent. ESMT sells or offers to sell in the United States, products, such as ESMT DDR3 SDRAM that meet each and every limitation of claim 1.

34. Claim 1 of the '143 Patent is directed to an integrated memory. The integrated memory comprises:

a. a memory cell array having memory cells;

b. a control circuit for controlling a memory access selected from the group consisting of a read memory access for reading out a data signal from one of said memory cells and a write memory access for writing a data signal into one of said memory cells;

c. for performing the memory access, said control circuit designed for receiving an access command selected from the group consisting of an activation command, a read command, and a write command;

d. for performing the memory access, said control circuit designed for receiving a configuration value in a combined manner with the access command; and

e. the configuration value being selected from the group consisting of a CAS latency value and a value for specifying a burst access.

35. ESMT DDR3 SDRAM contains a memory cell array having memory cells. The ESMT DDR3 SDRAM contains a control circuit for controlling read and write memory accesses, for example the command decoder, column counter, mode register, and control signal generator modules of the ESMT DDR3 SDRAM. The control circuit of the ESMT DDR3 SDRAM is designed to receive access commands in the form of activation commands, read commands (e.g., BC4, BL8), and write commands (e.g., BC4, BL8). The control circuit is further designed to receive a configuration value in a combined manner with the access command, *e.g.*, BC# values. The BC# configuration value received by the ESMT DDR3 SDRAM is, for example, a value for specifying a burst access.

36. Claim 2 of the ’143 Patent is dependent upon Claim 1, and claims “The integrated memory according to claim 1, wherein: said control circuit is designed to receive a multi-bit signal that includes the access command and the configuration value.”

37. The control circuit of the ESMT DDR3 SDRAM is designed to receive a multi-bit signal that includes the access command and the configuration value, including bits for CS#, RAS#, CAS#, WE#, A12/BC#.

38. Upon information and belief, other ESMT products similarly infringe one or more claims of the ’143 Patent. The specific part numbers of all ESMT products that practice one or more claims of the ’143 Patent are not presently known to Polaris. Polaris accuses of infringement all ESMT products that contain features and functions similar to those described above that practice one or more claims of the ’143 Patent.

39. ESMT has had notice of the ’143 Patent and of its infringement of the ’143 Patent since at least September 20, 2017. Before initiating this litigation, Polaris attempted to engage ESMT in discussions about Polaris’s belief that ESMT requires a license to the ’143 Patent. On the assumption that ESMT would participate in good faith licensing discussions, Polaris transmitted to ESMT information demonstrating ESMT’s use of the inventions claimed in the ’143 Patent. Polaris invited ESMT to discuss Polaris’s concerns and to seek mutually agreeable

resolution. However, ESMT did not respond to that correspondence and, to date, has not communicated with Polaris. Nevertheless, and despite its knowledge that it infringes one or more claims of the '143 Patent, ESMT continues to infringe the '143 Patent. ESMT's infringement of the '143 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

THIRD CLAIM FOR RELIEF

Infringement of U.S. Patent No. 7,532,523

40. Polaris realleges and incorporates by reference the allegations of paragraphs 1-14, inclusive, as if set forth in full herein.

41. ESMT has infringed, and continues to infringe, at least claims 1 and 2 of the '523 patent. ESMT sells or offers to sell in the United States, products, such as ESMT DDR3 SDRAM that meet each and every limitation of claim 1.

42. Claim 1 of the '523 Patent is directed to memory chip. The memory chip comprises

a. a terminal;

b. a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value;

c. a control command port for receiving a control command signal for affecting accessibility of the memory chip;

d. a control circuit connected to the termination circuit and configured to set the resistance value as a function of the received control command signal; and

e. a termination port to receive a termination signal, wherein the control circuit is configured to selectively terminate the terminal with the set resistance value in response to the termination signal,

f. wherein the control circuit, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value after a first time delay; and (ii) does not terminate the

terminal in accordance with a second time delay, the first time delay being sufficiently long to set the resistance value.

43. ESMT DDR3 SDRAM contains a terminal, for example, the DQ (DQL/DQU) pin of the bi-directional data bus. The ESMT DDR3 SDRAM contains a termination circuit coupled to the terminal and configured to terminate the terminal according to a settable resistance value. The ESMT DDR3 SDRAM's On-Die Termination feature "allows the DRAM to turn on/off termination resistance … vis the ODT control pin." The resistance values can be set, for example, to RZQ/4 or RZQ/2. The ESMT DDR3 SDRAM contains a control command port, for example the CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ pins, for receiving a control command signal for affecting accessibility of the memory chip, for example, the Mode Register Set signals. The ESMT DDR3 SDRAM contains a control circuit. The control circuit is configured to set the resistance value as a function of the received control command signal, for example, resistance values such as RZQ/4 or RZQ/2. The ESMT DDR3 SDRAM further contains a termination port, such as an ODT pin, to receive a termination signal. The control circuit is configured to selectively terminate the terminal with the set resistance value, e.g., RTT_WR, in response to the termination signal. Furthermore, the control circuit of the ESMT DDR3 SDRAM, as a function of the termination signal, selectively performs one of: (i) terminates the terminal with the set resistance value (e.g., RTT_WR) after a first time delay (e.g., ODTLon); and (ii) does not terminate the terminal in accordance with a second time delay (ODTLoff), the first time delay being sufficiently long to set the resistance value.

44. Claim 2 of the '523 Patent is dependent upon Claim 1, and claims "The memory chip of claim 1, wherein the control circuit is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value after a first predetermined switchover time and is set to a second resistance value after a second predetermined switchover time."

45. The ESMT DDR3 SDRAM is configured such that, as a function of the received control command signal, the resistance value is set to a first resistance value (e.g., RTT_WR) after a first predetermined switchover time (e.g., ODTLon) and is set to a second resistance value

(e.g., RTT_NOM) after a second predetermined switchover time (e.g., ODTLoff).

46. Upon information and belief, other ESMT products similarly infringe one or more claims of the ’523 Patent. The specific part numbers of all ESMT products that practice one or more claims of the ’523 Patent are not presently known to Polaris. Polaris accuses of infringement all ESMT products that contain features and functions similar to those described above that practice one or more claims of the ’523 Patent.

47. ESMT has had notice of the ’523 Patent and of its infringement of the ’523 Patent since at least September 20, 2017. Before initiating this litigation, Polaris attempted to engage ESMT in discussions about Polaris’s belief that ESMT requires a license to the ’523 Patent. On the assumption that ESMT would participate in good faith licensing discussions, Polaris transmitted to ESMT information demonstrating ESMT’s use of the inventions claimed in the ’523 Patent. Polaris invited ESMT to discuss Polaris’s concerns and to seek mutually agreeable resolution. However, ESMT did not respond to that correspondence and, to date, has not communicated with Polaris. Nevertheless, and despite its knowledge that it infringes one or more claims of the ’523 Patent, ESMT continues to infringe the ’523 Patent. ESMT’s infringement of the ’523 Patent has therefore been, and continues to be, willful, deliberate, and egregious, and has caused and continues to cause substantial damage to Polaris.

WHEREFORE, Polaris prays that judgment be entered in its favor and against ESMT as follows:

a. For damages in an amount according to proof, but no less than a reasonable royalty for infringement of the patents in suit;

d. For enhanced damages pursuant to 35 U.S.C. § 284;

e. For prejudgment and post-judgment interest as provided by law;

e. For costs of suit and reasonable attorneys’ fees incurred herein; and

f. For such other relief as the Court deems proper.

Dated: December 15, 2017

ROBERT E. FREITAS
JASON S. ANGELL
JING H. CHERNG
FREITAS ANGELL & WEINBERG LLP

/s/Jason S. Angell
Jason S. Angell
Attorneys for Plaintiff
Polaris Innovations Ltd.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Polaris demands a trial by jury on all issues so triable.

Dated: December 15, 2017

ROBERT E. FREITAS
JASON S. ANGELL
JING H. CHERNG
FREITAS ANGELL & WEINBERG LLP

/s/Jason S. Angell
Jason S. Angell
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