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UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

JAMES B. GOODMAN, **Plaintiff,** **vs.** **ACER AMERICAN CORPORATION,** **Defendant.**	**Civil Action No.** **COMPLAINT FOR PATENT INFRINGEMENT AND** **DEMAND FOR JURY TRIAL**

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NOW COMES Plaintiff, JAMES B. GOODMAN ("Goodman"), through his attorney, and files this Complaint for Patent Infringement and Demand for Jury Trial against Acer America Corporation ("Acer").

PARTIES

1. Goodman is an individual residing in the State of Texas.

2. Acer is a California corporation and maintains an office at 333 West San Carlos Street, Suite 1500, San Jose, CA 95110

BACKGROUND RELATING TO ACER

3. On information and belief, Acer is a recognized innovative leader in consumer electronics products, including laptop computers, and desktop computers.

4. On information and belief, products sold by Acer are sold under the trademark "Acer" to indicate that the products are connected to Acer.

5. On information and belief, Acer sells its consumer electronics products throughout the U.S. through national resellers, including CDW, CDW-G, PCM, D & H, SYNNEX, and others; and online stores including Acer, Best Buy, Fry's Electronics, Office Depot, Sam's Club, Amazon.com, and others.

6. On information and belief, Aces sells its consumer electronics products through retail stores such as Staples, Target, and Walmart in this Judicial District.

JURISDICTION AND VENUE

7. Acer maintains an office in this Judicial District, and is using and selling in this Judicial District products infringing U.S. Patent No. 6,243,315 ("315 Patent") in violation of 35 U.S.C. § 271.

8. Litigation to enforce the '315 Patent under 35 U.S.C. § 281 is proper.

9. This Court has original jurisdiction for this patent infringement case under 35 U.S.C. § 1338(a) and 35 U.S.C. § 1331.

10. Venue is proper in this Judicial District under 28 U.S.C. § 1391(d) and 1400(b) in view of the presence of Aces with permanent offices in this Judicial District, and the infringing activities of Aces in this Judicial District.

BACKGROUND RELATING TO GOODMAN AND HIS PATENT

11. Goodman is the inventor and patent owner of the ‘315 Patent. The ‘315 Patent leaped into importance when the manufacturers discovered the enormous advantages of incorporating the claimed invention of the ‘315 Patent to reduce power consumption and to inhibit errors in devices requiring memories systems.

12. Many of the computer related products sold in this Judicial District by Acer incorporate at least one of the memory products known in the industry as DDR3, and DDR4 memory products. Variations of these memory products such as the DDR3 memory product include DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600, and DDR3-1666 as well as DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1666. The use of the terms “DDR3", and “DDR4" to include in the designation of a memory product in the industry requires the performance of the memory product to comply with the respective industry standards for performance, and operations.

13. The standards published by the Joint Electron Device Engineering Council Solid State Technology Association (“JEDEC”) state for the respective DDR3, and DDR4 memory products and their variation: "No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."

14. On information and belief, the use of the terms “DDR3", and “DDR4", and variations of each implies that the respective memory products comply with the corresponding JEDEC Standards.

15. Therefore, the DDR3, and DDR4 memory products and their variations must operate in compliance with the respective standards established by the JEDEC Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201.

16. Any memory product identified as being a DDR3 memory product, or a variation thereof including the term “DDR3" must comply with JEDEC Standard JESD79-3F.

17. Any memory product identified as being a DDR4 memory product, or a variation thereof including the term “DDR4" must comply with JEDEC Standard JESD79-4A.

18. On information and belief, the JEDEC Standards for DDR3, and DDR4 memory products have several relevant operating capabilities in common when installed in a Aces computer related product, for example: (a) Each memory product has at least two banks of volatile memory, and this is the equivalent of a plurality of volatile solid state memory devices under the doctrine of equivalents; (b) A first external device (supplied by Aces computer related product) connected to the memory product can provide signals for selectively electrically isolating the address and control lines so that signals on the address and control lines do not reach the memory devices; and (c) A second external device (supplied by Aces computer related product) connected to the memory product can determine when the memory system is not being accessed and can initiate a low power for the memory system wherein the first external device isolates the memory devices and places the memory devices in self refresh mode, thereby reducing the electrical

energy drawn from the electrical power supply of the Aces computer related product.

19. On information and belief, the aforementioned Aces computer related products incorporating a DDR3, and DDR4 provide the aforementioned first and second external devices in order to take advantage of the respective operating specification of the memory products, including the low power mode which saves electrical energy while protecting the memory product against potential signals which could damage or corrupt the stored data.

20. The following is a Claim Chart for Claim 1 of the ‘315 Patent for the DDR3 memory product (and similarly applies to the DDR4 memory product in computer systems using the appropriate JEDEC Standard JESD79-4A.

CLAIM CHART AND ASSOCIATED CONSTRUCTION

U.S. Patent No. 6,243,315	**ACES COMPUTER RELATED SYSTEM HAVING AN INSTALLED DDR3 MEMORY PRODUCT AND PROVIDING THE AFOREMENTIONED FIRST AND SECOND EXTERNAL DEVICES**
Claim 1. A memory system for use in a computer system, said memory system comprising:	A "memory system" can be construed to be "**a system capable of retaining data**". The JEDEC Standard JESD79-3F specification at p. 18, Sec. 3.2, "The DDR3 SDRAM is a high-speed dynamic random-access memory ...". On the same page, "an interface designed to transfer two data words per clock cycle". The DDR3 memory product retains data. Thus, this memory product is within the preamble description.
a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and	A "memory device" can be construed to be an "**integrated circuit or chip**"; and "a plurality of volatile solid state memory devices" can be construed to be "**two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while an electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information**".

	The JEDEC Standard JESD79-3F at p. 109, Sec. 6.1 states the absolute maximum DC Ratings. P. 111, Sec. 7.1 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages. The JEDEC Standard JESD79-3F in at p. 77 refers to the memory module as being a "chip". See Sec. 4.15. The JEDEC Standard JESD79-3F at p. 18, Sec. 3.2 states, "The DDR3 SDRAM is a high-speed dynamic random-access internally configured an eight-bank DRAM." The second paragraph describes how a bank can be selected. See the Command Truth Table at p. 33, Sec. 4.1, and NOTE 3 explains that "BA" is for the selection of a bank being operated upon. Hence, the DDR3 has eight memory banks and the equivalents of a plurality of solid state memory devices. On information and belief, a DRAM is volatile memory and that means a voltage in a specific range must be applied to operate acceptably as pointed out above.
capable of being placed in a self refresh mode; said memory devices having address lines and control lines;	The JEDEC Standard JESD79-3F shows that the DDR3 is capable of being refreshed at p. 13, Sec. 2.10 for CKE, (CKE0), (CKE1) "Self-Refresh operations (all banks idle)"; p. 17, Sec. 3.1 on the diagram; p. 31, Sec. 3.4.4.1 entitled "Partial Array Self-Refresh (PASR)"; p. 35, Sec. 4.2 shows an entry for "Self-Refresh"; p. 46, Sec. 4.9.0.1 entitled, "Auto Self-Refresh"; and p. 79, Sec. 4.16 entitled "Self-Refresh Operation".

a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	JEDEC Standard JESD79-3F at p. 81, Sec. 4.17.1 entitled "Power-Down Entry and Exit" discloses a power-down operation. The description states, "Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and receivers after tCPDED has expired. The text also states, "In power-down mode, CKE low, RESET# high, and stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care." The input signals are address and control signals are related to the CK# input noted at p. 13, Sec. 2.10, where it is stated, "All Address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	The power-down is due to an input signal from the second external device as pointed out at P. 13, Sec. 2.10. The device generating the input signal for the power-down functions like the claimed memory access enable control device. JEDEC Standard JESD79-3F, Sec. 4.17.1 states, "Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read/write operations are in progress.

21. The respective DDR3, and DDR4 memory products are typically incorporated into the Aces computer related products on what is known in the industry as a "motherboard", and other components on the motherboard provide subsystems to monitor activity in the mounted memory product, initiate the reduced power down mode, to inhibit responses in the memory products on the motherboard, and other requirements of the respective JEDEC standard.

COUNT ONE
(DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,243,315)

22. Plaintiff Goodman repeats and incorporates herein the allegations contained in paragraphs 1 through 21 above.

23. On June 5, 2001, the ‘315 Patent entitled "COMPUTER MEMORY SYSTEM WITH A LOW POWER MODE", was duly and legally issued to James B. Goodman, as the sole patentee.

24. Plaintiff Goodman is the sole owner of the ‘315 Patent, and has standing to bring this action.

25. All of the limitations of Claim 1 of the ‘315 Patent are present in Aces related computer products incorporating at least one DDR3, or DDR4 memory product offered for sale, and being sold directly or indirectly by Aces in this Judicial District.

26. Aces is infringing claim 1 of the ‘315 Patent literally, or under the doctrine of equivalents in this Judicial District.

JURY DEMAND

Pursuant to Fed. R. Civ. P. 38(b), Plaintiff hereby demands a jury trial as to all issues in this lawsuit.

PRAYER FOR RELIEF

THEREFORE, Plaintiff respectfully requests this Court to:

a. enter judgment for Plaintiff on Claim 1 of the '315 Patent for patent infringement, either literally, and/or under the doctrine of equivalents against Aces;

b. order that an accounting be had for the damages caused to the Plaintiff by the infringing activities of the Aces;

c. Order an injunction to prohibit Aces from directly or indirectly from offering for sale, or selling infringing products;

d. award Plaintiff interest and costs from Aces; and

e. award Plaintiff such other and further relief as this Court may deem just and equitable.

Respectfully submitted,

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