IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

NORTH STAR INNOVATIONS, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 17-cv-506-LPS-CJB
	)	
MICRON TECHNOLOGY, INC.,	)	**JURY TRIAL DEMANDED**
	)	
Defendant.	)	

SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

North Star Innovations, Inc. ("North Star"), by and through its attorneys, files this Second Amended Complaint for Patent Infringement against Defendant, Micron Technology, Inc. ("Micron"), and avers as follows:

PARTIES

1. North Star is a corporation organized and existing under the laws of Delaware, with its principal place of business located at 600 Anton Blvd., Suite 1350, Costa Mesa, CA 92626. North Star has a registered agent, Corporation Service Company, located at 251 Little Falls Drive, Wilmington, Delaware 19808. North Star is the owner, through assignment, of the entire right, title and interest in the following patents: U.S. Patent No. 7,171,526, entitled "MEMORY CONTROLLER USEABLE IN A DATA PROCESSING SYSTEM" ("the '526 Patent"); U.S. Patent No. 6,465,743, entitled "MULTI-STRAND SUBSTRATE FOR BALL-GRID ARRAY ASSEMBLIES AND METHOD" ("the '743 Patent"); U.S. Patent No. 6,127,875, entitled "COMPLIMENTARY DOUBLE PUMPING VOLTAGE BOOST CONVERTER" ("the '875 Patent"); and U.S. Patent No. 5,943,274, entitled "METHOD AND APPARATUS FOR

AMPLIFYING A SIGNAL TO PRODUCE A LATCHED DIGITAL SIGNAL" ("the '274 Patent") (collectively referred to herein as the "Patents-in-Suit").

2. Micron is a corporation incorporated under the laws of Delaware, having its principal place of business at 8000 South Federal Way, Boise, ID 83707. Micron's registered agent for service of process is also Corporation Service Company, 251 Little Falls Drive, Wilmington DE 19808.

3. At all times relevant to this action, Micron has been engaged in the business of manufacturing, using, offering for sale and selling in the United States, and importing into the United States, memory devices that infringe the Patents-in-Suit.

JURISDICTION AND VENUE

4. This action arises under the patent laws of the United States, 35 U.S.C. §§ 1 et seq. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and § 1338(a).

5. This Court has personal jurisdiction over Defendant in this district, in that Defendant, directly or through its agents, is a resident of this district in that it is incorporated in Delaware, and further has regularly conducted business activities in this district; has committed infringing activities in this district by manufacturing, using, marketing, offering for sale, selling and importing products and systems that infringe the Patents-in-Suit; and has placed products that infringe the Patents-in-Suit in the stream of commerce with the knowledge and intent that they would be used, offered for sale and sold by others in this district.

6. Venue is proper pursuant to 28 U.S.C. §§ 1391(b) and 1400(b), in that Defendant resides in this district.

THE PATENTS-IN-SUIT - GENERAL ALLEGATIONS

7. The '526 Patent was duly and legally issued by the United States Patent and Trademark Office ("USPTO") on January 30, 2007, naming Arnaldo R. Cruz as inventor, and Freescale Semiconductor, Inc., as assignee. The '526 Patent relates to a memory controller useable in a data processing system. A true and correct copy of the '526 Patent is attached as Exhibit "A" hereto.

8. The '743 Patent was duly and legally issued by the USPTO on October 15, 2002, naming Norman Lee Owens as inventor, and Motorola, Inc., as assignee. The '743 Patent relates to a method for manufacturing BGA package integrated circuit devices. A true and correct copy of the '743 Patent is attached as Exhibit "B" hereto.

9. The '875 Patent was duly and legally issued by the USPTO on October 3, 2000, naming Steven Peter Allen, Ahmad H. Artiss, Gerald Lee Walcott and Walter C. Seelbach as inventors, and Motorola, Inc., as assignee. The '875 Patent relates to a voltage boosting circuit that provides an output voltage greater than the supplied input voltage. A true and correct copy of the '875 Patent is attached as Exhibit "C" hereto.

10. The '274 Patent was duly and legally issued by the USPTO on August 24, 1999, naming Alan S. Roth and Scott G. Nogle as inventors, and Motorola, Inc., as assignee. The '274 Patent relates to an apparatus and method for amplifying a signal to produce a latched digital signal in a memory integrated circuit. A true and correct copy of the '274 Patent is attached as Exhibit "D" hereto.

11. The Patents-in-Suit were all ultimately assigned to North Star, and North Star is the exclusive and current owner of all rights, title and interest in the Patents-in-Suit, and is

entitled to enforce the Patents-in-Suit against infringers, including by commencing the present action.

12. As set forth more fully below, Micron has engaged and continues to engage in acts of infringement under 35 U.S.C. § 271, *inter alia,* by using, offering for sale and selling in the United States, and importing into the United States, various memory devices that infringe at least one claim of one or more of the Patents-in-Suit, either literally or under the doctrine of equivalents.

13. Micron does not have a license or other authorization to practice the claims set forth in the Patents-in-Suit.

COUNT I- CLAIM FOR PATENT INFRINGEMENT OF U.S. PATENT NO. 7,171,526

14. North Star incorporates by reference and in their entirety the averments set forth in paragraphs 1 through 13, inclusive, of this Second Amended Complaint.

15. On information and belief, Micron has engaged and continues to engage in acts of infringement under 35 U.S.C. § 271, *inter alia,* by using, offering for sale and selling in the United States, and importing into the United States, data processing systems, including, without limitation, solid state storage devices ("SSDs"), that embody each element of at least claim 15 of the '526 Patent.

16. By way of example only, one of the infringing products that Micron has specifically used, offered for sale and sold in the United States, and imported into the United States for sale, and continues to use, offer for sale and sell in the United States, and import into the United States for sale, is the Micron 9100 PRO PCIe NVMe SSD, that includes the PMC-Sierra 89HF16P04CG3 memory controller. The Micron 9100 PRO PCIe NVMe SSD is a system that stores and processes data. Accordingly, to the extent, if any, that the preamble of claim 15 is

deemed to be limiting, the Micron 9100 PRO PCIe NVMe SSD, that includes the PMC-Sierra 89HF16P04CG3 memory controller, meets the language of the preamble of claim 15.

17. Further, the Micron 9100 PRO PCIe NVMe SSD includes a multiple lanes PCIe bus, i.e., a "system bus," used to transfer data or other information. Accordingly, the Micron 9100 PRO PCIe NVMe SSD meets the claim limitations of the first element of claim 15 that recites "a system bus."

18. The PMC-Sierra 89HF16P04CG3 memory controller that is included within the Micron 9100 PRO PCIe NVMe SSD includes a PCIe controller portion, i.e., "system bus master," that is coupled to the system bus, and that controls the transfer of data or other information via the system bus. Accordingly, the PMC-Sierra 89HF16P04CG3 memory controller meets the claim limitations of the second element of claim 15 that recites "a system bus master, coupled to the system bus".

19. The PMC-Sierra 89HF16P04CG3 memory controller that is included within the Micron 9100 PRO PCIe NVMe SSD further includes a NAND flash memory controller, i.e., "first memory controller," that is coupled to the system bus, and that controls the operations of the NAND flash memory devices that are included in the Micron 9100 PRO PCIe NVMe SSD, including the reading, writing and erasing operations of those NAND flash memory devices. Accordingly, the PMC-Sierra 89HF16P04CG3 memory controller meets the claim limitations of the third element of claim 15, which recites "a first memory controller, coupled to the system bus, for controlling a first memory".

20. The PMC-Sierra 89HF16P04CG3 memory controller that is included within the Micron 9100 PRO PCIe NVMe SSD further includes a DRAM controller, i.e., "second memory controller," that is coupled to the system bus, and that controls the operations of the DRAM

devices that are included within the Micron 9100 PRO PCIe NVMe SSD, including the reading, writing and erasing operations of those DRAM devices. Accordingly, the PMC-Sierra 89HF16P04CG3 memory controller meets the claim limitations of the fourth element of claim 15, which recites "a second memory controller, coupled to the system bus, for controlling a second memory".

21. The PMC-Sierra 89HF16P04CG3 memory controller that is included within the Micron 9100 PRO PCIe NVMe SSD further includes a buffer manager that is connected to the DRAM controller and that includes arbitration logic for arbitrating between the PCIe controller portion of the PMC-Sierra 89HF16P04CG3 memory controller and the NAND flash memory controller for access to data buffered in the DRAM devices. Accordingly, the PMC-Sierra 89HF16P04CG3 memory controller meets the claim limitations of the fifth element of claim 15, which recites "arbitration logic, coupled to the second memory controller, said arbitration logic arbitrating between the system bus master and the first memory controller for access to the second memory".

22. The PMC-Sierra 89HF16P04CG3 memory controller further includes an internal data path, i.e., "memory controller bus", that operates independently of the multiple lanes PCIe bus, and that is coupled to both the NAND flash memory controller and the DRAM controller, and that further controls the transfer of data between the NAND flash memory controller and the DRAM controller. Accordingly, the PMC-Sierra 89HF16P04CG3 memory controller meets the claim limitations of the sixth element of claim 15, which recites "a memory controller bus operating independent of the system bus, said memory controller bus being coupled to the first memory controller and to the second memory controller, said memory controller bus transferring data between the first memory controller and the second memory controller."

23. Accordingly, the Micron 9100 PRO PCIe NVMe SSD, including the PMC-Sierra 89HF16P04CG3 memory controller, embodies all of the elements of, and therefore infringes, at least Claim 15 of the '526 Patent.

COUNT II- CLAIM FOR PATENT INFRINGEMENT OF U.S. PATENT NO. 6,465,743

24. North Star incorporates by reference and in their entirety the averments set forth in paragraphs 1 through 13, inclusive, of this Second Amended Complaint.

25. On information and belief, Micron has engaged and continues to engage in acts of infringement under 35 U.S.C. § 271, *inter alia,* by using, offering for sale and selling in the United States, and importing into the United States, memory devices that consist of, or include, BGA package integrated circuit devices that are made according to a method that embodies each element of at least claim 1 of the '743 Patent.

26. By way of example only, one of the infringing products that Micron has specifically used, offered for sale and sold in the United States, and imported into the United States for sale, and continues to use, offer for sale and sell in the United States, and import into the United States for sale, is the Micron 1Tb TLC 3D NAND Flash device, that is included, for example, in the Micron Crucial® MX300 525GB SSD.

27. The Micron 1Tb TLC 3D NAND Flash device consists of a BGA package integrated circuit device that is assembled by a method that provides multiple BGA substrates arranged in an N by M array within a printed circuit board, wherein N and M are each equal to or greater than two. Further, each of the BGA substrates includes bond posts on one side of the substrate and contact pads on the other side of the substrate. Accordingly, the method for manufacturing the Micron 1Tb TLC 3D NAND Flash device meets the language of the preamble of claim 1 to the extent, if any, that the preamble is deemed to be limiting, and further meets the

claim limitations of the first step of claim 1 that recites "providing a plurality of BGA substrates arranged in an N by M array within a printed circuit board having a thickness, wherein N and M are greater than or equal to 2, each of the plurality of BGA substrates having a plurality of bond posts on one side and a plurality of contact pads on an opposite side".

28. The method by which the Micron 1Tb TLC 3D NAND Flash device is assembled further includes attaching a silicon die to each of the BGA substrates included in the N by M array, with each silicon die including multiple bond pads. Accordingly, the method for manufacturing the Micron 1Tb TLC 3D NAND Flash device meets the claim limitations of the second step of claim 1 that recites "attaching a semiconductor die to each of the plurality of BGA substrates, the semiconductor die having a plurality of bond pads".

29. The method by which the Micron 1Tb TLC 3D NAND Flash device is assembled further includes encapsulating each silicon die with an encapsulating material that is cured to form a solid material to protect the silicon die. Conductive solder balls are attached to each of the contact pads on the one side of each substrate. Accordingly, the method for manufacturing the Micron 1Tb TLC 3D NAND Flash device meets the claim limitations of the third, fourth and fifth steps of claim 1 that recite "encapsulating the semiconductor die with an encapsulant", "curing the encapsulant" and "attaching conductive solder balls to each of the plurality of contact pads".

30. The method by which the Micron 1Tb TLC 3D NAND Flash device is assembled further includes dividing the array into separate substantially planar BGA packages, wherein each BGA package includes a BGA substrate with corresponding silicon die, encapsulating material and solder balls. Accordingly, the method for manufacturing the Micron 1Tb TLC 3D NAND Flash device meets the claim limitations of the sixth step of claim 1 that recites "dividing

the N by M array into separate BGA packages, and wherein each of the separate BGA packages is substantially planar."

31. Accordingly, the Micron 1Tb TLC 3D NAND Flash device, and the Crucial® MX300 525GB SSD that includes the Micron 1Tb TLC 3D NAND Flash device, are assembled according to a method that embodies all of the elements of, and therefore infringe, at least Claim 1 of the '743 Patent.

COUNT III- CLAIM FOR PATENT INFRINGEMENT OF U.S. PATENT NO. 6,127,875

32. North Star incorporates by reference and in their entirety the averments set forth in paragraphs 1 through 13, inclusive, of this Second Amended Complaint.

33. On information and belief, Micron has engaged and continues to engage in acts of infringement under 35 U.S.C. § 271, *inter alia,* by using, offering for sale and selling in the United States, and importing into the United States, memory devices, including, without limitation, NAND Flash memory devices and SDRAM devices, that embody each element of at least claim 1 of the '875 Patent.

34. By way of example only, one of the infringing products that Micron has specifically used, offered for sale and sold in the United States, and imported into the United States for sale, and continues to use, offer for sale and sell in the United States, and import into the United States for sale, is the Micron 96 GB TLC 3D NAND Flash device, that is included, for example, in the Micron Crucial® MX300 750GB SSD.

35. The Micron 96 GB TLC 3D NAND Flash device includes a high voltage generation system, that further includes a clock generation circuit and a two-sided charge pump circuit. The clock generation circuit and the charge pump circuit are shown in the schematic

attached as Exhibit "E" hereto, which is derived from an inspection and analysis of the Micron 96 GB TLC 3D NAND Flash device.

36. The clock generation circuit provides four non-overlapping clock signals to two complimentary sides (Side A and Side B) of the charge pump circuit. These non-overlapping clock signals consist of BS1, which is a non-inverted form of a "boost signal;" BS2, which is an inverted form of the boost signal; Θ1, which is a "phase signal" that is an inverted form of the boost signal; and Θ2, which is a phase signal that is a non-inverted form of the boost signal. BS1 and BS2 are used for driving pumping capacitors that form a part of the charge pump circuit, and Θ1 and Θ2 are used for turning on and turning off transistors that are included on each side of the charge pump circuit. During the operation of the charge pump circuit, a supply voltage is provided to an input terminal of the charge pump circuit, and the turning on and turning off of the transistors, together with the driving of the pumping capacitors, causes an increased (or "boosted") voltage to be output on the output terminal of the charge pump circuit.

37. Accordingly, to the extent, if any, that the preamble of claim 1 is deemed to be limiting, the combination of the clock generation circuit and the charge pump circuit in the Micron 96 GB TLC 3D NAND Flash device, as described, is a "boost circuit having an input terminal and an output terminal," and thus satisfies the language of the preamble of claim 1.

38. The schematic attached as Exhibit "F" hereto, which is also derived from an inspection and analysis of the Micron 96 GB TLC 3D NAND Flash device, shows the charge pump circuit in further detail.

39. As shown in Exhibit "F", the charge pump circuit further includes, as part of Charge Pump Side A, a "first switch" in the form of a transistor. As further shown, that transistor is coupled between the input terminal of the charge pump circuit and the output

terminal of the charge pump circuit, and is turned on and turned off by Θ1, i.e., "a first phase signal." Accordingly, the Micron 96 GB TLC 3D NAND Flash device meets the claim limitations of the first element of claim 1 that recites "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal."

40. As further shown in Exhibit "F", the charge pump circuit further includes, as part of Charge Pump Side B, a "second switch" in the form of another transistor, that is coupled between the input terminal of the charge pump circuit and the output terminal of the charge pump circuit, and that is turned on and turned off by Θ2, i.e., "a second phase signal."

41. The schematic attached as Exhibit "G" hereto, which is also derived from an inspection and analysis of the Micron 96 GB TLC 3D NAND Flash device, shows the clock generation circuit in further detail. As shown, Θ1 and Θ2 have opposite phases, i.e., when Θ1 is in a state "0," Θ2 is in a state "1," and when Θ1 is in a state "1," Θ2 is in a state "0."

42. Accordingly, the Micron 96 GB TLC 3D NAND Flash device meets the claim limitations of the second element of claim 1 that recites "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal".

43. As shown in Exhibit "F", the charge pump circuit further includes a first capacitor that is included as part of Charge Pump Side A. As shown further in Exhibit "F," the capacitor has one of its terminals coupled to the output terminal of the charge pump circuit, and as further shown in Exhibit "G," its other terminal is coupled to receive the boost signal through an inverting buffer. Accordingly, the Micron 96 GB TLC 3D NAND Flash device meets the claim limitations of the third element of claim 1 that recites "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal".

44. As further shown in Exhibit "F", the charge pump circuit further includes a second capacitor that is included as part of Charge Pump Side B. As shown further in Exhibit "F," the second capacitor has one of its terminals coupled to the output terminal of the charge pump circuit, and as further shown in Exhibit "G," its other terminal is coupled to receive the boost signal through a non-inverting buffer. Accordingly, the Micron 96 GB TLC 3D NAND Flash device meets the claim limitations of the fourth element of claim 1 that recites "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.

45. Accordingly, the Micron 96 GB TLC 3D NAND Flash device, and the Crucial® MX300 750 GB SSD that includes the Micron 96 GB TLC 3D NAND Flash device, embody all of the elements of, and therefore infringe, at least Claim 1 of the '875 Patent.

46. By way of further example, another one of the infringing products that Micron has specifically used, offered for sale and sold in the United States, and imported into the United States for sale, and continues to use, offer for sale and sell in the United States, and import into the United States for sale, is the Micron 4 Gb DDR4 SDRAM device, that is included, for example, in the Micron Crucial 4GB DDR4-2133 SODIMM.

47. The Micron 4 Gb DDR4 SDRAM device includes a voltage boosting circuit, which further includes a clock generation circuit and a charge pump circuit, the charge pump circuit having two complimentary sides. This voltage boosting circuit is shown in the schematic attached as Exhibit "H" hereto, which is derived from inspection and analysis of the Micron 4 Gb DDR4 SDRAM device.

48. As shown in Exhibit H, the clock generation circuit provides two non-overlapping clock signals to two complimentary sides of the charge pump circuit. These two non-

overlapping clock signals constitute both inverted and non-inverted forms of a "boost signal" used for driving pumping capacitors that form a part of the charge pump circuit. The two non-overlapping clock signals are further used as "phase signals" for turning on and turning off transistors that are included on each side of the charge pump circuit. During the operation of the charge pump circuit, a supply voltage (VS) is provided to an input terminal of the charge pump circuit, and the turning on and turning off of the transistors, together with the driving of the pumping capacitors, causes an increased, or "boosted," voltage (VPP) to be output on the output terminal of the charge pump circuit.

49. Accordingly, to the extent, if any, that the preamble of claim 1 is deemed to be limiting, the combination of the clock generation circuit and the charge pump circuit in the Micron 4 Gb DDR4 SDRAM device, as described, is a "boost circuit having an input terminal and an output terminal," and thus satisfies the language of the preamble of claim 1.

50. The schematic attached as Exhibit "I" hereto, which is also derived from an inspection and analysis of the Micron 4 Gb DDR4 SDRAM device, shows the charge pump circuit in further detail.

51. As shown in Exhibit "I," the charge pump circuit further includes, as part of one side of the charge pump circuit, a "first switch" in the form of a PMOS transistor. As further shown, that PMOS transistor is coupled at its source to the input terminal of the charge pump circuit via an NMOS transistor as shown in Exhibit "H," and is coupled at its drain to the output terminal of the charge pump circuit via another NMOS transistor. The PMOS transistor is turned on and off by one of the two clock signals (shown in Exhibit "I" in logic state 1), i.e., "a first phase signal."

52. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the first element of claim 1 that recites "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal."

53. As further shown in Exhibit "I," the charge pump circuit further includes, as part of the other side of the charge pump circuit, a "second switch" in the form of another PMOS transistor that is coupled at its source to the input terminal of the charge pump circuit via the same NMOS transistor shown in Exhibit "H" that connects the first PMOS transistor to the input terminal. As further shown in Exhibit "I," that second PMOS transistor is coupled at its drain to the output terminal of the charge pump circuit via another NMOS transistor. That second PMOS transistor is turned on and off by the other of the two clock signals (shown in Exhibit "I" in logic state 0), i.e., "a second phase signal." Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the second element of claim 1 that recites "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal."

54. The schematic attached as Exhibit "J" hereto, which is also derived from an inspection and analysis of the Micron 4 Gb DDR4 SDRAM device, further shows the clock generation circuit and the two clock signals generated by that circuit. As shown, the two clock signals have opposite phases, i.e., when one of them is in a logic state "0," the other is in a logic state "1," and when one of them is in logic state "1," the other is in logic state "0."

55. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the second element of claim 1 that recites "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal".

56. As shown in Exhibit "I", the charge pump circuit further includes a first capacitor that is included as part of one side of the charge pump circuit. As shown in Exhibit "I," this first capacitor has one of its terminals coupled to the output terminal of the charge pump circuit via an NMOS transistor, and its other terminal coupled to receive the boost signal through an inverting buffer as shown in Exhibits "H" and "J."

57. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the third element of claim 1 that recites "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal".

58. As shown in Exhibit "I", the charge pump circuit further includes a second capacitor that is included as part of the other side of the charge pump circuit. As shown in Exhibit "I," this second capacitor has one of its terminals coupled to the output terminal of the charge pump circuit via another NMOS transistor, and its other terminal coupled to receive the boost signal through a non-inverting buffer as shown in Exhibits "H" and "J."

59. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the fourth element of claim 1 that recites "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal."

60. Accordingly, the Micron 4 Gb DDR4 SDRAM device, and the Micron Crucial 4GB DDR4-2133 SODIMM that includes the Micron 4 Gb DDR4 SDRAM device, embody all of the elements of, and therefore infringe, at least Claim 1 of the '875 Patent.

COUNT IV- CLAIM FOR PATENT INFRINGEMENT OF U.S. PATENT NO. 5,943,274

61. North Star incorporates by reference and in their entirety the averments set forth in paragraphs 1 through 13, inclusive, of this Second Amended Complaint.

62. On information and belief, Micron has engaged and continues to engage in acts of infringement under 35 U.S.C. § 271, *inter alia,* by using, offering for sale and selling in the United States, and importing into the United States, memory devices, including, without limitation, SDRAM devices, that embody each element of at least claim 1 of the '274 Patent.

63. By way of example only, one of the infringing products that Micron has specifically used, offered for sale and sold in the United States, and imported into the United States for sale, and continues to use, offer for sale and sell in the United States, and import into the United States for sale, is the Micron 4 Gb DDR4 SDRAM device, that is included, for example, in the Micron Crucial 4GB DDR4-2133 SODIMM.

64. The Micron 4 Gb DDR4 SDRAM device is a DRAM memory device that includes a memory array for storing data, and an output stage coupled to the memory array, the output stage structured to generate appropriate logic level output signals, based on data stored in the memory array, that can be output on the data output circuitry of the DRAM memory device.

65. Accordingly, to the extent, if any, that the preamble of claim 1 is deemed to be limiting, the Micron 4 Gb DDR4 SDRAM device meets the language of the preamble of claim 1.

66. The output stage that is part of the read data path of the Micron 4 Gb DDR4 SDRAM device is shown in detail in the schematic attached as Exhibit "K" hereto, which is derived from an inspection and analysis of the Micron 4 Gb DDR4 SDRAM device.

67. As shown in Exhibit "K," the output stage includes a timing circuit, a differential amplifier, an impedance control circuit, a level converter and a clock-free latch.

68. The timing circuit generates certain timing signals for controlling the operation of the output stage. Specifically, as shown in Exhibit "K," the timing circuit consists of a two-input NAND gate that receives control signals labeled PRECHG and ENN. It further consists of an

inverter that receives the control signal ENN. The timing signals control when the impedance control circuit, differential amplifier and data lines providing data to the differential amplifier are activated.

69. Accordingly, the Micron 4 Gb DDR4 SDRAM device "meets the claim limitations of the first element of claim 1 that recites "a timing circuit".

70. As further shown in Exhibit "K, the differential amplifier is coupled to the timing circuit. As shown, data from the memory array is transferred to the differential amplifier via two PMOS data access transistors and their respective data lines. The differential amplifier senses data on the data lines. The differential amplifier consists of two cross-coupled PMOS transistors, two cross-coupled NMOS transistors, and a third NMOS transistor. The sources of the PMOS transistors are connected to a power supply (VS), and the drains of the PMOS transistors are connected to the drains of two cross-coupled NMOS transistors. The sources of the two cross-coupled NMOS transistors are connected to the drain of the third NMOS transistor. The source of that third NMOS transistor is connected to ground, and its gate is connected to the output of the inverter of the timing circuit. The differential amplifier is turned on and off by the timing signals generated by the timing circuit. As such, the timing circuit controls the operation of the differential amplifier.

71. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the second element of claim 1 that recites "a differential amplifier responsive to the timing circuit."

72. The impedance control circuit precharges and equalizes the data lines before the data from the memory array is transferred to the differential amplifier. As further shown in Exhibit "K," the impedance control circuit consists of three PMOS transistors, with the sources

of two of those transistors connected to a power supply (VS), and the drain of each of the two transistors connected to a respective data line by which data from the memory array is transferred to the differential amplifier. The third PMOS transistor of the impedance control circuit is connected to the other two PMOS transistors at their drains. The gates of all three PMOS transistors are connected together and further connected to the output of the NAND gate of the timing circuit.

73. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the third element of claim 1 that recites "an impedance control circuit."

74. The level converter converts the signal levels sensed by the differential amplifier into full logic level signals that are ultimately output on the data output circuitry of the DRAM memory device via the clock-free latch. As further shown in Exhibit "K," the level converter includes a PMOS transistor, an NMOS transistor and an inverter. The source of the PMOS transistor is connected to a power supply (VS), the gate of the PMOS transistor is connected to a control signal labeled ENP, and the drain of the PMOS transistor is connected to the drain of the NMOS transistor. The source of the NMOS transistor is connected to ground, and the gate of the NMOS transistor is connected to the output of the inverter. The input of the inverter is connected to the output of the differential amplifier, as well as the output of the impedance control circuit. The differential amplifier senses data from the memory array, and the level converter converts the signal levels received from the differential amplifier in response to the impedance control circuit precharging and equalizing the data lines prior to the differential amplifier sensing the data.

75. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the fourth element of claim 1 that recites "a level converter responsive to the differential

amplifier and the impedance control circuit."

76. As further shown in Exhibit "K," the clock-free latch consists of two cross-coupled inverters. The clock-free latch is coupled to the level converter, which outputs the full logic level signals to the clock-free latch. In response to receiving the full logic level signals from the level converter, the clock-free latch stores those signals, and ultimately outputs them on the data output circuitry of the DRAM memory device.

77. Accordingly, the Micron 4 Gb DDR4 SDRAM device meets the claim limitations of the fifth element of claim 1 that recites "a clock-free latch responsive to the level converter."

78. Accordingly, the Micron 4 Gb DDR4 SDRAM device, and the Micron Crucial 4GB DDR4-2133 SODIMM that includes the Micron 4 Gb DDR4 SDRAM device, embody all of the elements of, and therefore infringe, at least Claim 1 of the '274 Patent.

DAMAGES

79. North Star incorporates by reference and in their entirety the averments set forth in paragraphs 1 through 78, inclusive, of this Second Amended Complaint.

80. Micron has caused and will continue to cause North Star substantial damage by virtue of its infringing activities.

81. North Star is entitled to recover from Micron the damages it has sustained as a result of Micron's infringing activities.

DEMAND FOR JURY TRIAL

82. North Star hereby demands a trial by jury of all issues triable of right before a jury.

PRAYER FOR RELIEF

WHEREFORE, North Star respectfully requests the following relief:

a) That this Court enter judgment in favor of North Star and against Micron that Micron has infringed the Patents-in-Suit;

b) That this Court award North Star all damages adequate to compensate North Star for the harm it has suffered as a result of Micron's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with pre- and post-judgment interest and costs as fixed by the Court, all pursuant to 35 U.S.C. § 284;

c) In the event that evidence is adduced through discovery or at trial that Micron's infringement was willful and deliberate, that this Court award North Star enhanced damages pursuant to 35 U.S.C. § 284;

d) In the event that circumstances warrant a declaration that this case be declared to be exceptional, that this Court award North Star its reasonable attorneys' fees pursuant to 35 U.S.C. § 285; and

e) That this Court award to North Star such other and further relief as this Court deems to be just and proper.

Dated: January 5, 2018

Respectfully submitted,

FARNAN LLP

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