UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

ANZA TECHNOLOGY, INC.	§	
	§	
PLAINTIFF	§	**CAUSE NO. A-17-CV-01193-LY**
	§	
v.	§	**SECOND AMENDED COMPLAINT**
	§	**FOR PATENT INFRINGEMENT**
AVANT TECHNOLOGY, INC.	§	
D/B/A/ MUSHKIN ENHANCED MFG	§	
	§	
DEFENDANT	§	
	§	

Plaintiff Anza Technology, Inc. ("Anza" or "Plaintiff") complains and alleges against Defendant Avant Technology, Inc. d/b/a Mushkin Enhanced Mfg. ("Defendant") as follows:

NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the laws of the United States relating to patents, 35 U.S.C. § 101 *et seq*. The statutory provisions at issue in the civil action include, without limitation, 35 U.S.C. §§ 271 and 281. Plaintiff Anza seeks monetary damages for patent infringement.

JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a). This court further has subject matter jurisdiction over this case for patent infringement pursuant to the patent laws of the United States of America, 35 U.S.C. § 101, *et seq.*

3. Venue properly lies within the Western District of Texas. Venue is properly vested with the Western District of Texas pursuant to the provisions of 28 U.S.C. §§ 1391(b), (c), and 1400(b). Defendant is a Nevada corporation that maintains its principal place of business in Pflugerville, Texas. Defendant maintains a physical production facility in Pflugerville, Texas. Pflugerville, Texas, is located within the jurisdictional limits of the Western District of Texas. Defendant has admitted that the Western District of Texas is the appropriate venue for this action.

4. This Court has personal jurisdiction over Defendant because Defendant transacts continuous and systematic business within the Western District of Texas. Examples of continuous and systematic business include the operation of its principal place of business from within the Western District of Texas. Defendant's principal place of business is responsible for, at the least, North American and Worldwide Sales as is reflected by the portion of Defendant's website reproduced here:

Examples of continuous and systematic business further include the operation of its physical production facility within the Western District of Texas, specifically Pflugerville, Texas. This facility assembles and aggregates performance computer products, including hard drives and

memory cards.

5. This Court further has personal jurisdiction over the Defendant because the activities that Plaintiff contends infringe one or more claims of the patents-in-suit occur within or are caused to occur within the Western District of Texas. This includes, but is not limited to, Defendant having made, used, sold, imported, exported, and/or offered for sale products manufactured utilizing an infringed system, method, or apparatus otherwise claimed by one of the aforementioned patents-in-suit. This further includes Defendant having placed, or caused to be placed, products manufactured utilizing an infringing system, method, or apparatus claimed by one of the aforementioned patents-in-suit in the stream of interstate commerce.

PARTIES

6. Plaintiff Anza Technology, Inc. is a corporation organized and existing under the laws of the State of California. Plaintiff Anza maintains an office and principal place of business at 4121 Citrus Avenue, Suite 4, Rocklin, California 95677. Anza is a designer, manufacturer, and seller of products directed to the manufacture and assembly of electronics including the bonding of electrostatic-sensitive devices.

7. Defendant Avant Technology, Inc. is a corporation organized and existing under the laws of the State of Nevada. Defendant maintains its principal place of business in the State of Texas at 828 New Meister Ln, Suite 300, Pflugerville, Texas 78660. Defendant assembles and aggregates performance computer products including hard drives and memory cards.

8. Defendant acquired the entirety of an electronic memory component business from Mushkin, Inc. This acquisition includes the Mushkin brand name. This acquisition includes all rights to do business under the Mushkin brand name. This acquisition also includes

all assets related to Mushkin, Inc.'s electronic memory module and board sales business. Defendant declares itself to be the sole aggregator and assembler of all Mushkin brand products. Defendant's declaration is inclusive of all Mushkin brand computer memory board and module components. Defendant declares that it assembles and sells Mushkin brand memory boards and memory modules products under the trade name Mushkin Enhanced MFG.

9. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant is involved in product development services. These product development services include JEDEC (f/k/a the Joint Electron Device Engineering Council, but now known as the JEDEC Solid State Technology Association) compliant product designs for dynamic random access memory (DRAM). In addition to assembling and aggregating performance computer products including hard drives and memory cards, the engineering team of the Defendant produces memory products. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant is an active member of JEDEC with influence in key committees and contributes to industry standards for memory modules. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant produces custom high-density memory solutions.

10. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant produces DDR 3, DDR 2, DDR, and legacy modules, as well as flash memory products. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant offers contract manufacturing as well as custom, high-volume, and turn-key memory services. In addition to assembling and aggregating performance computer products including hard drives

and memory cards, Defendant produces custom high-density memory and storage solutions. In addition to assembling and aggregating performance computer products including hard drives and memory cards, Defendant utilizes more than a dozen surface mount technology lines incorporating industry recognized equipment from the likes of Panasonic, Phillips, Fuji, MPM, and Omni. Defendant utilizes these surface mount technology lines to produce, manufacture, and assemble memory modules, including but not limited to the accused products identified below.

BACKGROUND

11. Electrostatic discharge (ESD) is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. ESD can cause a range of harmful effects of importance in the electronics industry, specifically with respect to integrated circuits. Integrated circuits can suffer permanent damage when subjected to ESD as can memory modules like the accused products identified herein.

12. The assembly process of various surface mount technologies take an integrated circuit or other computing component—such as a memory module—and affix or 'bond' that component to a printed circuit board. The integrated circuit or memory module comes in contact with one or more tools that not only place the circuit or module on the board but in some instances aid in effectuating the bonding of the same by way of wires, leads, or pads. Subject to a particular bonding technique, heat may be applied to a bonding medium or material (such as a metallic solder ball) by way of a tool tip or an oven. Application of heat causes the medium to melt and electrically 'bond' the integrated circuit or memory module to the surface of the circuit board.

13. For the purpose of context, reproduced below are FIGURES 1 and 2 of U.S. patent number 6,354,479. U.S. patent number 6,354,479 is one of the patents-in-suit in the present action. FIGURE 1 (as reproduced below) "illustrates a typical capillary bonding tool 10. Such bonding tools are usually about one-half inch (12-13 mm) long and about one-sixteenth inch (1.6 mm) in diameter. The bonding tool tip 12 itself is usually from 3 to 10 mils (0.08 to 0.25 mm) long." '479:3:3-7. FIGURE 2—to continue the example and for the purposes of context—is "a highly enlarged, cross-sectional view of the capillary bonding tool 10 as shown and described in FIG. 1." '479:3:10-11. "[T]he chamfer surface 16 is provided to allow for smoother looping of the [bonding] wire as the bonding tool 10 is moved from the bonding pad on an integrated circuit to the bonding pad (not shown) on a lead frame of an integrated circuit assembly." '479:3:20-24.

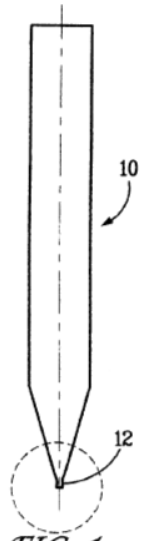


FIG. 1

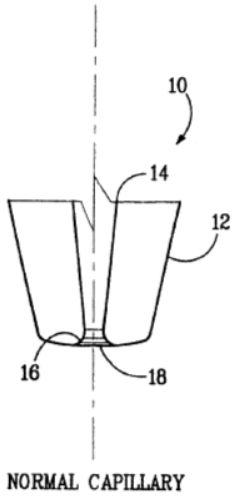


FIG. 2

14. Another manufacturing technique is known as flip chip. The term flip chip describes the method of electrically connecting a die or module to a substrate. Flip chip microelectronic assembly is the direct electrical connection of face-down (or flipped) integrated

circuit chips onto substrates using conductive bumps on the chip bond pads. The interconnection between the die and carrier in flip chip packaging occurs when using a conductive bump placed directly on the die surface. The bumped die is then flipped and placed face down so that the bumps connect directly to the substrate.

15. Naturally occurring electrostatic charges of varying degrees build up when bonding tools come in contact with the die and the bonding medium. Electrostatic charges can even build up when a die is removed from storage or a transport vessel and placed on the circuit board before any bonding takes place. Without strict safeguards, electrostatic charges can be built up from almost any contact and through almost any activity. If enough static is generated, discharge can occur and damage to an electronic component may result.

16. Notwithstanding the different methodology involved in flip chip bonding, the possibility of ESD remains. For example, the direct electrical connection of face-down (or flipped) integrated circuit chips onto substrates using conductive bumps on the chip bond pads can result in static build-up. There remains a need, therefore, to dissipate and/or block such a build up to avoid damage to the electrical componentry being bonded.

17. Electronics manufacturers therefore establish electrostatic protective areas free of static using measures to prevent charging, including the use of bonding tools, apparatus, and techniques that obviate a buildup of ESD or otherwise dissipate the same. ESD damage, being a well-known phenomenon in the electronics industry, has resulted in now broadly accepted standards developed by industry-recognized standards setting organizations such as the American National Standards Institute (ANSI), JEDEC, the International Electro-technical Commission (IEC), and the Electrostatic Discharge Association (ESDA) (cumulatively referred to as "ESD Standards"). ESD Standards minimize the risk of damage to ESD sensitive devices

during assembly and manufacture.

18. For example, ESDA and JEDEC have—since October 2008—had a joint memorandum of understanding concerning the development of standards and publications in the field of ESD. The ESDA and JEDEC entered into such an agreement in the best interest of their organizations, their membership, and the electronics industry. Notwithstanding the foregoing joint relationship, JEDEC has—since December 1999—through at least JEDEC Standard No. 625-A ("Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices") indicated that JEDEC members should "incorporate these minimal requirements into their ESD control program to provide a consistent protection level for their products."

19. JEDEC Standard No. 625-A, for example, "establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD)." JEDEC Standard No. 625-A continues in noting that "[t]he passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part." Table 1 of Section 6.1 of JEDEC Standard No. 625-A, for example, requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

20. Like JEDEC Standard No. 625-A, subsequent and ancillary ESD Standards require, in part, the use of tools made of dissipative materials having approximately the same resistance values in connection with handling integrated circuits that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent the discharge of a charge to an ESD sensitive device such as a memory module, including the accused products as discussed

further herein. These ranges are also high enough to avoid current flows that may damage a device such as a memory module, including the accused products as discussed further herein. Panasonic, Phillips, Fuji, MPM, and Omni—all manufacturers of equipment utilized by Defendant—are believed to comply with one or more of the aforementioned ESD Standards, including but not limited to those concerning electrical dissipation and electrostatic discharge.

21. DDR DRAM stands for Double Data Rate (DDR) Dynamic Random Access Memory (DRAM). DDR DRAM is a class of memory integrated circuits used in computers. DDR DRAM involves a random access semiconductor memory that stores each bit of data in a capacitor on an integrated circuit. A memory refresh circuit periodically re-writes data in the capacitors to prevent a phenomenon known as data 'leakage' that would otherwise result in data being lost. Because of the re-writing of data by the refresh circuit, this type of memory is known as dynamic random access memory (the aforementioned DRAM).

22. Generations of DRAM are referenced with a prefix (*e.g.*, DDR4, SDR, EDR, and EDO). This abbreviation is reflective of a buffer size as it relates to datawords per memory access. For example, DDR 4 SDRAM is an abbreviation for double data rate fourth-generation synchronous dynamic random-access memory, which is a type of synchronous dynamic random-access memory (SDRAM) with a high bandwidth ("double data rate") interface. DDR4 is a successor to DDR3 technologies, which is a successor to DDR2, and so on.

23. DRAM is typically used in digital electronics where low-cost and high-capacity is a concern. One of the largest applications for DRAM is the main memory of a computer or a graphics card. DRAM is also used in portable devices and video game consoles. An advantage of DRAM is the structural simplicity of its memory cells usually involving one transistor and a capacitor. Because of this structural simplicity, DRAM can be implemented in extremely high

densities allowing it to be 'cheaper per bit' versus other memory technologies such as static random access memory (SRAM). As electronic parts like computer central processing units become packed more densely with transistors, the transistors shrink and become more vulnerable to ESD.

24. The low-cost nature of DRAM makes ESD of particular concern. Damage suffered as a result of ESD during the manufacture or assembly process will drive up the cost of the finished product. In order for products utilizing DRAM technology to remain cost-feasible, it is important for DRAM products to remain ESD-free during the manufacture and assembly process. Defendant's acquisition, assembly, aggregation, development, design, production, and manufacture of memory solutions, specifically including DRAM solutions, utilizing surface mount technology lines invokes concerns as to ESD and ESD sensitive devices.

25. Acquisition, assembly, aggregation, development, design, production, and manufacture of memory solutions, specifically including ESD-sensitive DRAM solutions, requires the use of certain techniques and methods to guard against ESD events that can have catastrophic consequences for ESD-sensitive DRAM solutions. As a result, Plaintiff alleges that Defendant uses specific design, engineering, assembly, and manufacturing practices in making the accused products to minimize the costs resulting from damaging ESD events. Further, Plaintiff alleges that Defendant specifies and/or directs other parties involved in the design, engineering, assembly, and manufacturing process that require the accused products (specifically including but not limited to the DRAM Modules discussed herein) to be designed, engineered, assembled, or manufactured in ways that meet or exceed ESD-Standards for reducing the risk of damage to ESD sensitive devices. Certain techniques and methods utilized by Defendant or at the direction of the Defendant with respect to the design, engineering, assembly, and

manufacture of memory modules, including but not limited to DRAM products, including the accused products identified below, infringe the patents-in suit as is further detailed herein.

ACCUSED PRODUCTS

26. Defendant contends that it "offers a comprehensive range of [memory] modules from SDR to the latest DDR3 modules." Defendant makes such a declaration on its website at the address of http://www.avanttechnology.com/index.php/products. A true and correct copy of the website located at the aforementioned address is attached hereto as Exhibit A. Defendant further contends that "[w]hether you are looking to upgrade a few computers or your entire server infrastructure, AVANT has the right solution to maximize your business hardware." Defendant makes such a declaration on its website at the address of http://www.avanttechnology.com/index.php/products/memory. A true and correct copy of the website located at the aforementioned address is attached hereto as Exhibit B. Defendant also provides a listing of the following memory modules at said website address, including: DDR4 DRAM Modules, DDR3 DRAM Modules, DDR2 DRAM Modules, DDR DRAM Modules, SDR DRAM Modules, and EDO DRAM Modules. The accused products include the aforementioned DDR4 DRAM Modules, DDR3 DRAM Modules, DDR2 DRAM Modules, DDR DRAM Modules, SDR DRAM Modules, and EDO DRAM Modules (hereinafter referring to as the "Avant Accused Products").

27. A sample of the DDR4 DRAM Modules made available by Defendant and initially disclosed above is further referenced here:

DDR4 DRAM Modules

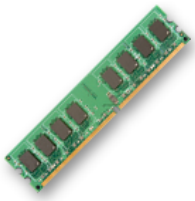
DDR4 is the next-generation, high-performance solution for CPU systems—it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR4 supports data rates of 2133 to 2400 Mb/s, with clock frequencies of 1067 to 1200 MHz, respectively.

28. A sample of the DDR3 DRAM Modules made available by Defendant and initially disclosed above is further referenced here:

DDR3 DRAM Modules

DDR3 doubles the data rate transfers of its predecessor, DDR2, while also using 30% less power. We have a variety of modules to fit your product needs- whether you are looking to improve the performance of your personal computing experience or designing new hardware to take advantage of DDR3's long product life cycle. DDR3 supports data rates of 1067 to 2133 Mb/s, with clock frequencies of 533 to 1067 MHz, respectively.

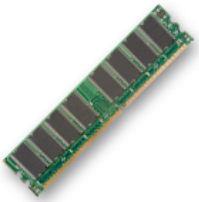
29. A sample of the DDR2 DRAM Modules made available by Defendant and initially disclosed above is further referenced here:



DDR2 DRAM Modules

A wide array of capabilities makes our DDR2 an excellent memory choice for the diverse needs of many applications—from automotive and industrial to server, consumer, networking, and computing. In fact, we've designed both the long-term road map and the product features of our DDR2 memory with those needs in mind.

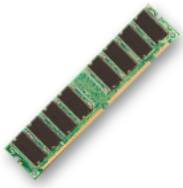
30. A sample of the DDR DRAM Modules made available by Defendant and initially disclosed above is further referenced here:



DDR DRAM Modules

We know that many of our customers will continue to use DDR solutions in their designs well into the future. We're committed to leveraging our proven technology, premier quality, and industry-leading manufacturing efficiency to provide DDR for many years to come.

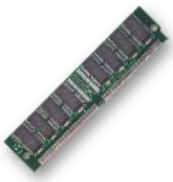
31. A sample of the SDR DRAM Modules made available by Defendant and initially disclosed above is further referenced here:



SDR DRAM Modules

Why complicate your design? If a simple, cost-effective SDRAM solution will do, plug it in and go. You already know it's a reliable part. You know it's got all the features you're looking for. Plus it's a solid long-term solution. We have plans to support it for years to come so it's still a good fit for products with long life cycles.

32. A sample of the Legacy Modules made available by Defendant and initially disclosed above is further referenced here:



Legacy Modules

EDO, sometimes referred to as Hyper Page Mode enabled DRAM, is similar to **FPM** Fast Page Mode DRAM with the additional feature that a new access cycle can be started while keeping the data output of the previous cycle active. This allows a certain amount of overlap in operation (pipe lining), allowing somewhat improved performance

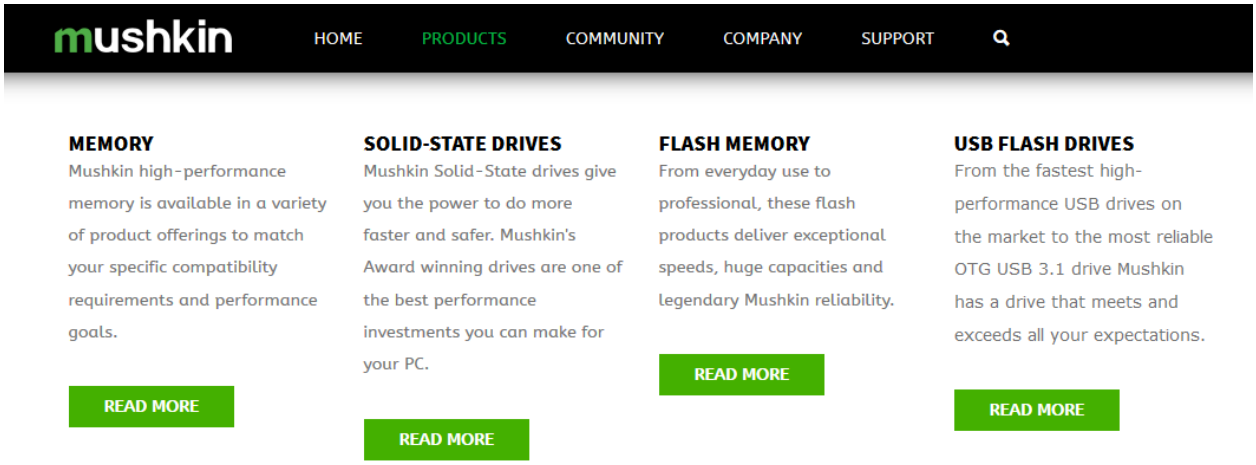
33. Defendant previously declared that it is the sole aggregator and assembler of all Mushkin brand products. Defendant previously declared that said aggregation and assembly includes all Mushkin brand computer memory board and module components. Defendant previously declared that is assembles and sells Mushkin brand memory boards and memory modules products under the trade name Mushkin Enhanced MFG.

34. A website may be located on the Internet at the address http://www.poweredbymushkin.com. A true and correct copy of a portion of that website at the address http://www.poweredbymushkin.com/Home/index.php/company/about-us is attached hereto as Exhibit C. The aforementioned website declares that "Mushkin Enhanced MFG has since become one of the nation's most recognized Manufacturers of performance computer products." The aforementioned website further includes the following branding bearing the

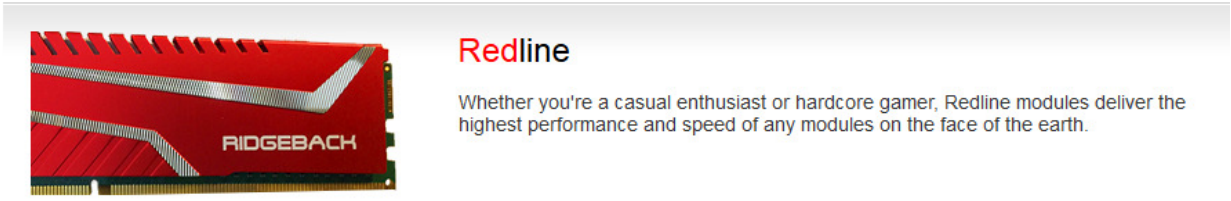
name 'Mushkin':

35. In light of the previous declarations of the Defendant that it is the sole aggregator and assembler of all Mushkin brand products and that the Defendant assembles and sells Mushkin brand memory boards and memory modules products under the trade name Mushkin Enhanced MFG, the fact that the http://www.poweredbymushkin.com site bears the Mushkin brand name, and the fact that the http://www.poweredbymushkin.com site bears the trade name Mushkin Enhanced MFG, Plaintiff is informed and believes and thereon alleges that certain products that infringe the patents-in-suit are also offered for sale by way of the http://www.poweredbymushkin.com site.

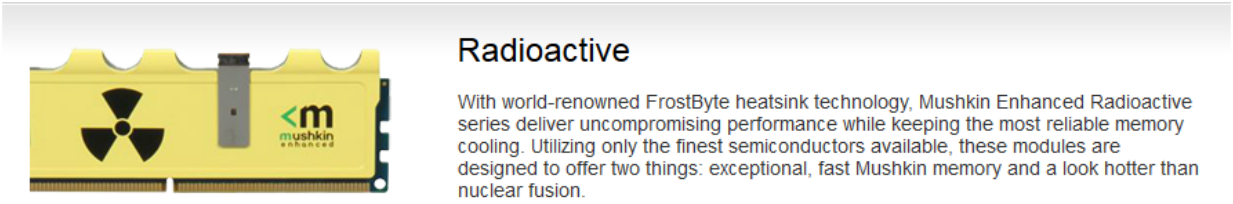
36. These products include "high-performance memory" "available in a variety of product offerings to match your specific compatibility requirements and performance goals" as declared at the address: http://www.poweredbymushkin.com/Home/index.php/catalog. A portion of that website is reproduced here:



37. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Redline product line. The Redline product line is available in a DDR 4 and a DDR 3 DRAM offering. A portion of the Mushkin Memory Product Line Catalog concerning the Redline product line is reproduced below:



38. The high-performance memory product offering made available under the Defendant controlled Mushkin brand includes the Radioactive product line. The Radioactive product line is available in a DDR 3 DRAM offering. A portion of the Mushkin Memory Product Line Catalog concerning the Radioactive product line is reproduced below:



39. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Blackline product line. The Blackline product line is available in a DDR 4 and a DDR 3 DRAM offering. A portion of the Mushkin Memory Product Catalog concerning the Blackline product line is reproduced below:

Blackline

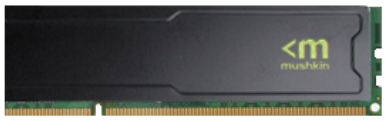
Whether you're breaking your own records or you're building a dream gaming rig, you can count on the performance and reliability of Mushkin's Blackline memory modules.

40. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the ECO^2 product line. The ECO^2 product line is available in a DDR 3 offering. A portion of the Mushkin Memory Product Catalog concerning the ECO^2 product line is reproduced below:

ECO^2

Combining Mushkin's award winning performance with an ECOnomical design, the Mushkin ECO2 Series memory delivers unprecedented value. The sleek, low-profile heatsink design and legendary Mushkin reliability make this memory the perfect fit for any system.

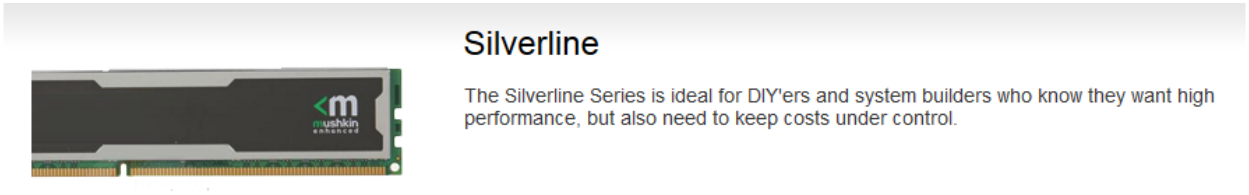
41. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Stealth product line. The Stealth product line is available in a DDR 3 offering. A portion of the Mushkin Memory Product Catalog concerning the Stealth product line is reproduced below:



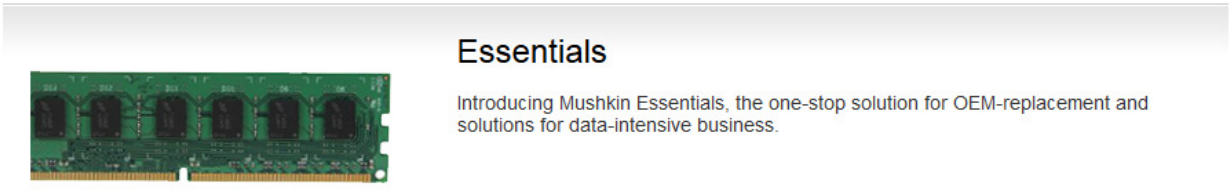
Stealth

The new Stealth family of modules, in its new black limited edition design, includes high-performance specifications for professionals and tech enthusiasts who want the best possible computing experience at prices that make sense.

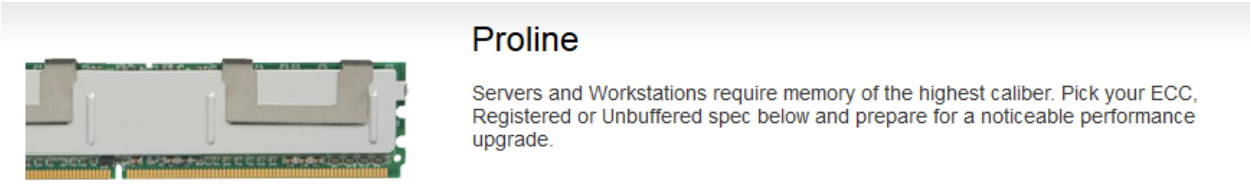
42. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Silverline product line. The Silverline product line is available in a DDR 4, DDR 3, and DDR 2 offering. A portion of the Mushkin Memory Product Catalog concerning the Silverline product line is reproduced below:



43. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Essentials product line. The Essentials product line is available in a DDR 4, DDR 3, DDR 2, DDR, and SDR offering. A portion of the Mushkin Memory Product Catalog concerning the Essentials product line is reproduced below:



44. The high-performance memory product offerings made available under the Defendant controlled Mushkin brand include the Proline product line. The Proline product line is available in a DDR4, DDR3, DDR2, DDR, and SDR offering. A portion of the Mushkin Memory Product Catalog concerning the Proline product line is reproduced below:



45. The accused products further include the aforementioned Redline, Radioactive, Blackline, ECO^2, Stealth, Silverline, Essentials, and Proline product lines, and more specifically the inclusion by one or more of the aforementioned product lines of DDR4 DRAM Modules, DDR3 DRAM Modules, DDR2 DRAM Modules, DDR DRAM Modules, and SDR DRAM

Modules (hereinafter referred to as the "Mushkin Brand Accused Products"). The Avant Accused Products and the Mushkin Brand Accused Products are collectively referred to as the "Accused Products."

THE PATENTS-IN-SUIT

46. On March 12, 2002, the United States Patent and Trademark Office ("USPTO") duly and legally issued U.S. patent number 6,354,479 entitled 'Dissipative Ceramic Bonding Tip,' (the "'479 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '479 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '479 Patent is attached hereto as Exhibit D.

47. On November 25, 2003, the USPTO duly and legally issued U.S. patent number 6,651,864 entitled 'Dissipative Ceramic Bonding Tool Tip,' (the "'864 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '864 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '864 Patent is attached hereto as Exhibit E.

48. On October 24, 2006, the USPTO duly and legally issued U.S. patent number 7,124,927 entitled "Flip Chip Bonding Tool and Ball Placement Capillary," (the "'927 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in and to the '927 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '927 Patent is attached hereto as Exhibit F.

49. The foregoing patents are collectively referred to as the "Patents-in-Suit" and are incorporated into this Second Amended Complaint as if fully set forth herein.

COUNT ONE

INFRINGEMENT OF THE '479 PATENT

50. Plaintiff re-alleges each of the foregoing paragraphs 1-49 as if fully set forth herein.

51. Defendant has been aware of the '479 Patent since the filing of the original complaint in this action, which set forth claims of infringement as they pertain to the '927 Patent. The '927 Patent is a child of the '479 Patent. The relationship between the '927 Patent and the '479 Patent is identified on the face of the '927 Patent. Defendant was also made aware of the '479 Patent by way of correspondence dated January 4, 2018, in which Plaintiff indicated its intent to add one or more claims from the '479 Patent to the present action.

52. Defendant infringes (at least) claim 1 of the '479 Patent at its Texas fabrication and assembly facility. Claim 1 of the '479 Patent recites as follows:

> A tip having a dissipative material for use in wire bonding machines for connecting leads on integrated circuit bonding pads, wherein said dissipative material has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded.

'479:6:24-29.

53. Defendant—through the personal knowledge of its President, Tim Peddecord—admitted to placing wire bonded chips on printed circuit boards at this fabrication and assembly facility. Bonding a chip or memory module—like the Accused Products—to a printed circuit board utilizing surface mounting technology requires the use of one or more bonding tools. These one or more bonding tools include a tip.

54. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, Defendant contends that it is compliant with

JEDEC standards. Plaintiff is informed and believes that Defendant does comply with JEDEC standards. Such contentions and compliance would comport with Defendant's contention that it is an active member of JEDEC with influence in key committees and contributes to industry standards for memory modules.

55. JEDEC standards include requirements and ranges for the use of bonding tools to avoid ESD incidents. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance low enough to prevent a discharge of a charge to a device being bonded. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance high enough to avoid current flow large enough to damage a device being bonded. An example of a device being bonded in the context of claim 1 of the '479 Patent is an Accused Product memory module to a printed circuit board.

56. Defendant also infringes (at least) claim 2 of the '479 Patent at its Texas fabrication and assembly facility. Claim 2 of the '479 Patent recites: "[a] tip as in claim 1, having a resistance in the range of 10^5 to 10^{12} ohms." '479:6:30-31. JEDEC Standard No. 625-A, with which Defendant is presumably compliant, purports to be compliant, and otherwise has influence as a member of JEDEC requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and $1x10^{11}$ ohms."

57. Defendant also infringes (at least) claim 46 of the '479 Patent at its Texas fabrication and assembly facility. Claim 46 of the '479 Patent recites as follows:

> A device comprising:
>
> a bonding tip having a dissipative material that is positioned to come in contact with a device being bonded during bonding,
>
> in which a current is allowed to flow that is produced by static charge generated during bonding, and
>
> that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough so that the current flow is not large enough to damage said device being bonded.

'479:9:24-33.

58. Claim 1—the infringement of which was evidenced above—includes a 'tip having a dissipative material . . . for connecting leads on integrated circuit bonding pads.' The basis for infringement of the foregoing claim element of claim 1 would similarly correspond to the 'bonding tip . . . positioned to come in contact with a device being bonded' element of claim 46.

59. The production of a current that correlates to a static charge generated during bonding is all but inherent in light of the fact that—as noted above—'electrostatic charges can be built up from almost any contact and through almost any activity.' Further, 'if enough static is generated, discharge can occur and damage to an electronic component may result.'

60. Claim 1—the infringement of which was evidenced above—includes the claim element of said dissipative material having a resistance 'low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded.' That claim element of claim 46 reciting 'a resistance low enough to prevent a discharge of charge to a device being bonded and high enough so that the current flow is not large enough to damage said device being bonded' would be met for at least the same reasons as that similar claim element in independent claim 1.

61. A tip with the properties recited by claim 46 would, in turn, be used in the likes of one of Defendant's more than a dozen surface mount technology lines incorporating industry recognized equipment from the likes of Panasonic, Phillips, Fuji, MPM, and Omni. Defendant

utilizes these surface mount technology lines to produce, manufacture, and assemble memory modules, including but not limited to the Accused Products.

62. In light of the foregoing, Defendant infringes the '479 Patent under at least 35 U.S.C. § 271(a). Defendant—without authority—uses the patented invention embodied in (at least) claims 1, 2, and 46 of the '479 Patent. Defendant would also infringe at least claims 1, 2, and 46 of the '479 Patent to the extent that it makes or imports into the United States the tip having a dissipative material recited in (at least) claims 1 and 2 of the '479 Patent or a device having such a tool tip as recited in (at least) claim 46.

63. Defendant also infringes (at least) claim 19 of the '479 Patent under 35 U.S.C. § 271(g) to the extent that Defendant manufactures or sees to the manufacture of a dissipative bonding tip like that recited in claims 1 and 46 of the '479 Patent. Any such tip manufactured or caused to be manufactured outside of the United States and then brought into the United States for use without the authority of the Plaintiff constitutes import, for later use, of "a product which is made by a process patented in the United States."

64. On information and belief, Plaintiff alleges that it is not aware of any material change to any dissipative bonding tip manufactured by any such process abroad after being imported into the United States. On information and belief, Plaintiff contends that any dissipative bonding tip manufactured by any such process abroad is not immaterial or otherwise non-essential in that it forms a fundamental and necessary component of the tip of claim 1 and a device using such a tip as in claim 46.

COUNT TWO

INFRINGEMENT OF THE '864 PATENT

65. Plaintiff re-alleges each of the foregoing paragraphs 1-49 and 50-64 as if fully set forth herein.

66. Defendant has been aware of the '864 Patent since the filing of the original complaint in this action, which set forth claims of infringement as they pertain to the '927 Patent. The '927 Patent is a child of the '864 Patent. The relationship between the '927 Patent and the '864 Patent is identified on the face of the '927 Patent. Defendant was also made aware of the '864 Patent by way of correspondence dated January 4, 2018, in which Plaintiff indicated its intent to add one or more claims from the '864 Patent to the present action.

67. Defendant infringes (at least) claim 1 of the '864 Patent at its Texas fabrication and assembly facility. Claim 1 of the '864 Patent recites as follows:

> A device comprising:
> a tip having a dissipative material for use in wire bonding machines for connecting leads to integrated circuit bonding pads, wherein said dissipative material has a resistance in the range of 5×10^{5} to 10^{12} ohms.

'864:12:50-54.

68. Defendant—through the personal knowledge of its President, Tim Peddecord—admitted to placing wire bonded chips on printed circuit boards at this fabrication and assembly facility. Bonding a chip or memory module—like the Accused Products—to a printed circuit board utilizing surface mounting technology requires the use of one or more bonding tools. These one or more bonding tools include a tip.

69. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, Defendant contends that it is compliant with

JEDEC standards. Plaintiff is informed and believes that Defendant does comply with JEDEC standards. Such contentions and compliance would comport with Defendant's contention that it is an active member of JEDEC with influence in key committees and contributes to industry standards for memory modules.

70. JEDEC standards include requirements and ranges for the use of bonding tools to avoid ESD incidents. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance low enough to prevent a discharge of a charge to a device being bonded. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance high enough to avoid current flow large enough to damage a device being bonded. An example of a device being bonded in the context of claim 1 of the '864 Patent is an Accused Product memory module to a printed circuit board.

71. JEDEC Standard No. 625-A, with which Defendant is presumably compliant, purports to be compliant, and otherwise has influence as a member of JEDEC requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

72. In light of the foregoing, Defendant infringes the '864 Patent under at least 35 U.S.C. § 271(a). Defendant—without authority—uses the patented invention embodied in (at least) claim 1 of the '864 Patent. Defendant would also infringe at least claim 1 of the '864 Patent to the extent that it makes or imports into the United States a device having a tip having a dissipative material recited in (at least) claim 1 of the '864 Patent.

73. Defendant is also believed to infringe (at least) claim 28 of the '864 Patent, which recites:

> A method of using an electrically dissipative bonding tool tip, having a resistance in the range of 10^5 to 10^{12} ohms, comprising:
>
> providing the electrically dissipative bonding tool tip;
>
> bonding a material to a device;
>
> allowing an essentially smooth current to dissipate to the device, the current being low enough so as not to damage said device being bonded and high enough to avoid a build up of charge that could discharge to the device being bonded and damage the device being bonded.

'864:14:27-38.

74. Claim 28—similar to claim 1—recites an electrically dissipative bonding tool tip, specifically the use thereof. Claim 28 would, therefore, be infringed by placing a bonding tip like that infringing claim 1 in a device positioned to come in contact with a device being bonded. As noted above, an example of a device being bonded in the context of claim 1 of the '864 Patent is an Accused Product memory module to a printed circuit board. Such a device might include one or more of Defendant's surface mount technology lines incorporating industry recognized equipment from the likes of Panasonic, Phillips, Fuji, MPM, and Omni.

75. JEDEC standards include requirements and ranges for the use of bonding tools to avoid ESD incidents. JEDEC and other ESD Standards include the use of dissipative materials that allow for current to dissipate to the device low enough so as not to damage the device but high enough as to avoid a build-up of a charge that could discharge to the device and damages the same. JEDEC Standard No. 625-A, with which Defendant is presumably compliant, purports to be compliant, and otherwise has influence as a member of JEDEC, requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

76. Defendant may also infringe (at least) claim 28 of the '864 Patent under at least 35 U.S.C. § 271(g) to the extent that it imports Accused Product manufactured or assembled

utilizing the methodology of claim 28 if the manufacture or assembly occurred outside of the United States. Plaintiff is informed and believes such manufacture and import in violation of claim 28 may, in fact, occur in light of Defendant's declaration that in some instances it assembles and aggregates pre-packaged memory components (manufactured and designed by others) onto larger memory boards and memory modules.

77. Plaintiff is not aware of any material change to any such pre-packaged memory components manufactured and designed by others. Plaintiff similarly contends that the methodology for assembly as recited in claim 28 is not immaterial or otherwise non-essential in that failure to utilize an ESD-compliant manufacturing method may result in damage or destruction of a bonded component such as the Accused Product memory modules identified above.

COUNT THREE

INFRINGEMENT OF THE '927 PATENT BY DEFENDANT

78. Plaintiff re-alleges each of the foregoing paragraphs 1-49, 50-64, and 65-77 as if fully set forth herein.

79. Defendant has been aware of the '927 Patent since the filing of the original complaint in this action.

80. Defendant is believed to infringe (at least) claims 1 and 14 of the '927 Patent at its Texas fabrication and assembly facility. Such infringement is believed to occur utilizing one or more flip chip bonding manufacturing practices. Panasonic, Phillips, and Fuji—all providers of equipment utilized by Defendant—manufacture and provide flip chip bonders for surface mounted technology utilization.

81. Claims 1 and 14 of the '927 Patent recite a flip chip bonding tool and ball placement capillary system and ESD preventative device, respectively. The system of claim 1 and device of claim 14 are both used for bonding of componentry to circuit boards such as the Accused Products. On information and belief, Plaintiff contends that such a system may encompass a flip chip bonding tool and placement system.

82. In both claims 1 and 14, there is the recitation of the use of dissipative material having a resistance low enough to prevent a discharge of a charge to a device being bonded and high enough to stop current flop large enough to damage the device being bonded. To combat ESD, Defendant contends that it is compliant with JEDEC standards. Plaintiff is informed and believes that Defendant does comply with JEDEC standards. Such contentions and compliance would comport with Defendant's contention that it is an active member of JEDEC with influence in key committees and contributes to industry standards for memory modules such as the Accused Products.

83. JEDEC standards include requirements and ranges for the use of bonding tools to avoid ESD incidents. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance low enough to prevent a discharge of a charge to a device being bonded. JEDEC and other ESD Standards include the use of dissipative materials that have a resistance high enough to avoid current flow large enough to damage a device being bonded. An example of a device being bonded is an Accused Product memory module.

84. JEDEC Standard No. 625-A, with which Defendant is presumably compliant, purports to be compliant, and otherwise has influence as a member of JEDEC, requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material

having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

85. In light of the foregoing, Defendant is believed to infringe the '927 Patent under at least 35 U.S.C. § 271(a). Defendant is believed—without authority—to use the patented invention embodied in at least claims 1 and 14. Defendant would also infringe at least claim 1 and 14 of the '927 Patent to the extent that it makes or imports into the United States the system or device of claims 1 and 14.

86. Defendant would also infringe (at least) claim 16 of the '927 Patent under at least 35 U.S.C. § 271(g) to the extent that it imports Accused Product manufactured or assembled utilizing a methodology incorporating a flip chip bonding methodology (like that of claim 16) and that would otherwise occur in the context of a system or device like that recited in claims 1 and 14 if the manufacture or assembly occurred outside of the United States. As noted in the context of the assertion of infringement of claim 1 and 14, the bonding material is alleged to have a resistance low enough to prevent a discharge of a charge to a device being bonded and high enough to stop all current flow to the device being bonded.

87. Defendant may import previously manufactured or assembled Accused Product into the United States without authority as it contends that in some instances it assembles and aggregates pre-packaged memory components (manufactured and designed by others) onto larger memory boards and memory modules. Section 271(g) prohibits such import into the United States, for later use, "a product which is made by a process patented in the United States . . . if the importation . . . or use of the product occurs during the term of such process patent."

88. Plaintiff is not aware of any material change to any such pre-packaged memory components manufactured and designed by others outside of the United States. Plaintiff contends that the methodology utilized in the manufacturing and for assembly process is not

immaterial or otherwise non-essential. Failure to utilize an ESD-compliant manufacturing method would result in damage or destruction of the bonded component.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for relief and judgment as follows:

1. That Defendant has infringed the Patents-in-Suit;

2. Compensation for all damages caused by Defendant's infringement of the Patents-in-Suit to be determined at trial;

3. A finding that this case is exceptional and an award of reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

4. Granting Plaintiff pre-and post-judgment interest on its damages, together with all costs and expenses; and,

5. Awarding such other relief as this Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all claims.

February 27, 2018

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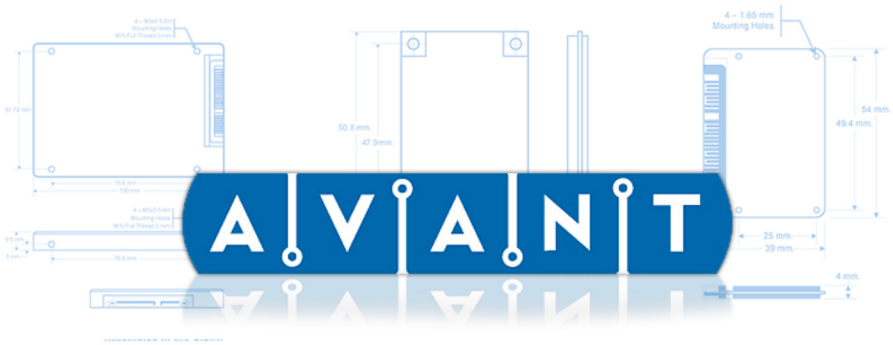
EXHIBIT A

Avant Products

What if? Two simple words. But when combined, the possibilities are endless. At Avant Technology we've stopped simply asking what if the impossible was possible and started manufacturing it.



Solid State Drives

Solid State Drives (SSDs) are a breakthrough in modern computing. SSDs are faster, lighter, more durable, and more reliable than traditional hard drives.

LEARN MORE

Memory Modules

From product development to manufacturing, testing and customized logistics, Avant Technology offers a comprehensive range of modules from SDR to the latest DDR3 modules.

LEARN MORE

Legacy Modules

EDO, sometimes referred to as Hyper Page Mode enabled DRAM, is similar to FPM Fast Page Mode DRAM with the additional feature that a new access cycle can be started while keeping the data output of the previous cycle active.

LEARN MORE

Solid State Drives	DDR3 Modules	DDR2 Modules	DDR Modules	SDR Modules	Legacy Modules
No moving parts	ECC RDIMM	FBDIMM	UDIMM	UDIMM	EDO
Energy efficient	SODIMM	ECC RDIMM	SODIMM	SODIMM	FPM
Reliable	VLP RDIMM	Mini RDIMM	ECC UDIMM	ECC UDIMM	
Vibration free	VLP Mini UDIMM	SODIMM	ECC RDIMM	ECC RDIMM	

EXHIBIT B

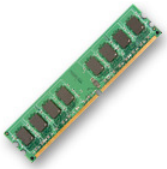
Whether you are looking to upgrade a few computers or your entire server infrastructure, AVANT has the right solution to maximize your business hardware.

DDR4 DRAM Modules

DDR4 is the next-generation, high-performance solution for CPU systems—it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR4 supports data rates of 2133 to 2400 Mb/s, with clock frequencies of 1067 to 1200 MHz, respectively.

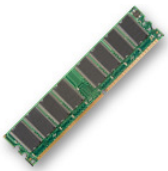
DDR3 DRAM Modules

DDR3 doubles the data rate transfers of its predecessor, DDR2, while also using 30% less power. We have a variety of modules to fit your product needs- whether you are looking to improve the performance of your personal computing experience or designing new hardware to take advantage of DDR3's long product life cycle. DDR3 supports data rates of 1067 to 2133 Mb/s, with clock frequencies of 533 to 1067 MHz, respectively.



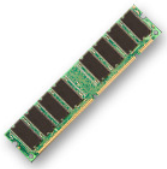
DDR2 DRAM Modules

A wide array of capabilities makes our DDR2 an excellent memory choice for the diverse needs of many applications—from automotive and industrial to server, consumer, networking, and computing. In fact, we've designed both the long-term road map and the product features of our DDR2 memory with those needs in mind.



DDR DRAM Modules

We know that many of our customers will continue to use DDR solutions in their designs well into the future. We're committed to leveraging our proven technology, premier quality, and industry-leading manufacturing efficiency to provide DDR for many years to come.



SDR DRAM Modules

Why complicate your design? If a simple, cost-effective SDRAM solution will do, plug it in and go. You already know it's a reliable part. You know it's got all the features you're looking for. Plus it's a solid long-term solution. We have plans to support it for years to come so it's still a good fit for products with long life cycles.

Legacy Modules

EDO, sometimes referred to as Hyper Page Mode enabled DRAM, is similar to **FPM** Fast Page Mode DRAM with the additional feature that a new access cycle can be started while keeping the data output of the previous cycle active. This allows a certain amount of overlap in operation (pipe lining), allowing somewhat improved performance

EXHIBIT C

ABOUT US

Founded in Denver, Colorado in 1994, Mushkin Enhanced MFG has since become one of the nation's most recognized Manufacturers of performance computer products worldwide and has well established relationships with all of the top computer component companies in the world including Intel, AMD, NVIDIA, LSI, as well as top retail channels globally. Exceptional quality, enhanced performance and unparalleled customer support are what make our products the best in the industry.

With a strong team of over 25 years experience, we have focused around cutting edge technology including digital storage devices and a complete selection of memory upgrades for desktops, servers and notebooks – we offer something for everyone; from business user to gamer.

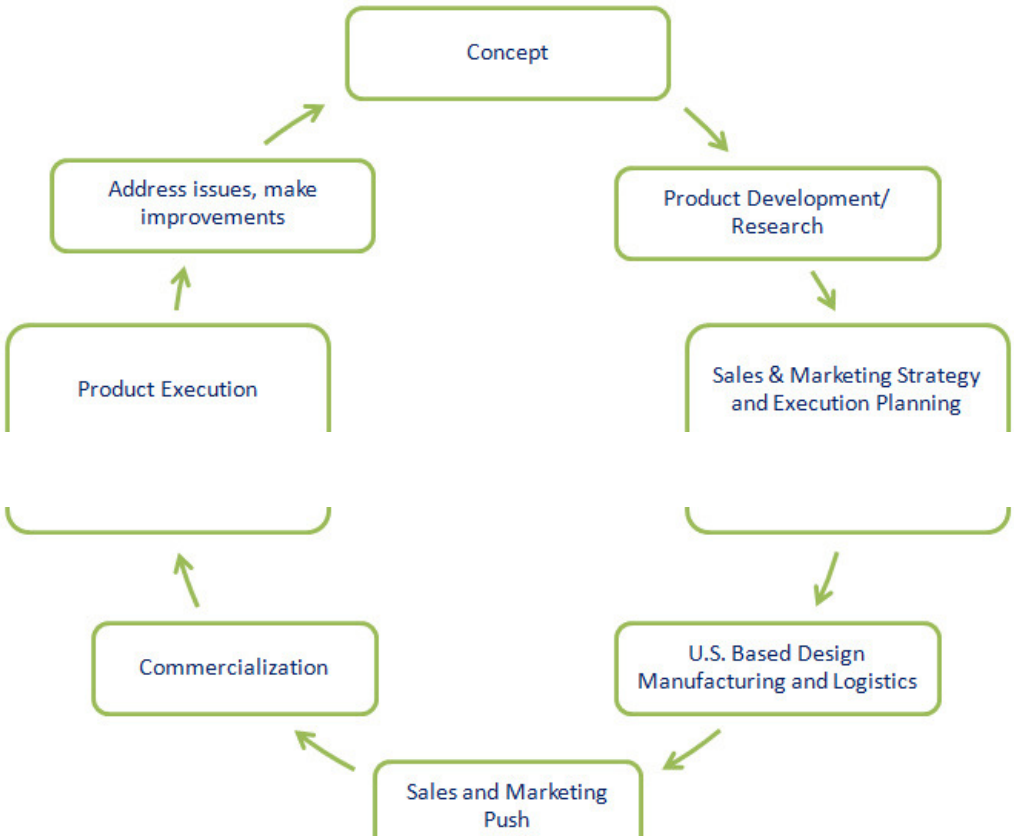
Company Philosophy

As we grow as a company, it has become more and more important to explicitly define the core values from which we develop our culture, our brand, and our business strategies. These are the eight core values that we live by:

- Deliver WOW Through Quality Products and Service

- Embrace and Drive Change

- Drive Innovation through Fun, Exciting new channels



- Build Open
and Honest Relationships with Communication

- Build a Positive Team and Family Spirit

- Do More With Less

- Be Passionate and Determined

- Most Importantly, Be Humble

All of us Mushkin live the "work hard, play hard" mentality! We believe in operational excellence and realize that there is always room for improvement in everything we do. This means that our work is never done. In order to stay ahead of the competition (or would-be competition), we need to continuously innovate as well as make incremental improvements to our operations, always striving to make ourselves more efficient, always trying to figure out how to do something better. On the right you will see our Product Launch cycle, showing how we don't only launch a product, but develop and consistently improve them. It's called the Mushkin difference.

EXHIBIT D

US006354479B1

(12) **United States Patent**
Reiber et al.

(10) **Patent No.: US 6,354,479 B1**
(45) **Date of Patent: Mar. 12, 2002**

(54) **DISSIPATIVE CERAMIC BONDING TIP**

(75) Inventors: **Steven Frederick Reiber**, Sunnyvale; **Mary Louise Reiber**, Los Altos, both of CA (US)

(73) Assignee: **SJM Technologies**, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/514,454**

(22) Filed: **Feb. 25, 2000**

Related U.S. Application Data

(60) Provisional application No. 60/121,694, filed on Feb. 25, 1999.

(51) **Int. Cl.**[7] **B23K 37/00**; B23K 1/00; B23K 5/00

(52) **U.S. Cl.** **228/4.5**; 228/180.5; 228/6.1; 228/6.2; 219/56.21

(58) **Field of Search** 228/4.5, 180.5, 228/6.1, 6.2; 219/56.21

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,892,924 A		6/1959	Wood	219/118
3,538,205 A	*	11/1970	Gates, Jr. et al.	264/61
3,660,050 A	*	5/1972	Iler et al.	29/182.8
3,986,653 A	*	10/1976	Gilding	228/44.1 A
4,020,543 A	*	5/1977	Pennings	29/423
4,171,477 A	*	10/1979	Funari	219/56.21
4,182,947 A		1/1980	Brower	219/70
4,315,128 A	*	2/1982	Matcovich et al.	219/85
4,331,048 A	*	5/1982	Dworak et al.	82/1
4,387,283 A		6/1983	Peterson et al.	219/56.21

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0435423 A2	*	7/1991	228/4.5
GB	2287897 A	*	10/1995	228/4.5
JP	54037114	*	3/1979	228/4.5
JP	63164228	*	7/1988	228/4.5

OTHER PUBLICATIONS

Newburg, Carl E., "Test Report", Anza Technolgy, Incorporated Static Dissipative Ceramic Rods for Wire Bonding Applications, Report 190 :2000–92, River's Edge Technical Service, Nov. 29, 2000, pp. 1–5.*

James R. Huntsman and Donald M. Yenni, Jr., "Test Methods for Static Control Products," Electrical Overstress/Electrostatic Discharge Symposium Proceedings, Sep. 21, 1982, pp. 94–109, vol. 4, IIT Research Institute, Chicago, IL.

Carl E. Newberg, "Test Report," Anza Technology, Incorporated Static Dissipative Ceramic Rods for Wire Bonding Applications, Tested for Electrical Properties Discharge Current Resistance and Decay Time, Report #: 2000–92, River's Edge Technical Service, Nov. 29, 2000, pp. 1–5.

Stan Weitz, "Trends in ESD Test Methods, " Materials Testing Section of the ETS Testing Laboratory, Electrotech Systems, http://www.electrotechsystems.com, the website has a copyright of 1998, pp. 1–7.

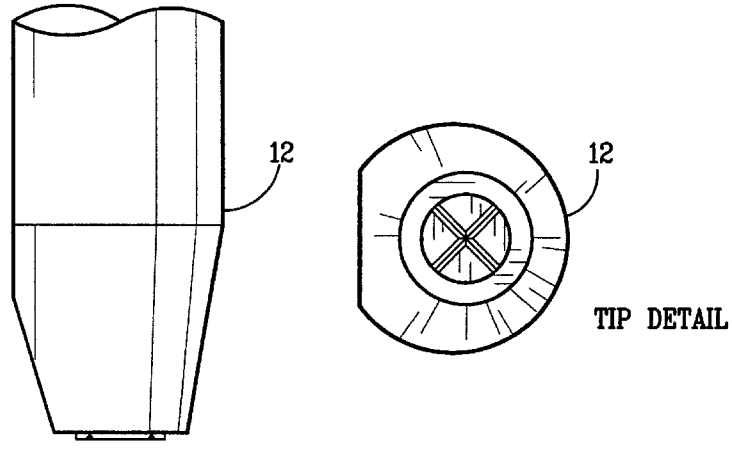
(List continued on next page.)

Primary Examiner—Tom Dunn
Assistant Examiner—L. Edmondson
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP; John S. Ferrell; Davis Lewis

(57) **ABSTRACT**

Dissipative ceramic bonding tips for wire bonding electrical connections to bonding pads on integrated circuits chips and packages are disclosed. In accordance with the principles of the present invention, to avoid damaging delicate electronic devices by any electrostatic discharge, an ultrasonic bonding wedge tool tip must conduct electricity at a rate sufficient to prevent charge buildup, but not at so high a rate as to overload the device being bonded. For best results, a resistance in the tip assembly itself should range from 10^5 to 10^{12} ohms. In addition, the wedges must also have specific mechanical properties to function satisfactorily.

51 Claims, 4 Drawing Sheets



U.S. PATENT DOCUMENTS

4,390,771	A		6/1983	Kurtz et al.	219/56.22
4,502,983	A	*	3/1985	Omori et al.	252/516
4,513,190	A	*	4/1985	Ellet et al.	219/56.21
4,691,854	A	*	9/1987	Haefling et al.	228/4.5
4,705,204	A		11/1987	Hirota et al.	228/179
4,897,710	A	*	1/1990	Suzuki et al.	357/71
4,909,427	A	*	3/1990	Plaisted et al.	228/4.5
4,998,002	A		3/1991	Okikawa et al.	219/56.22
5,178,742	A		1/1993	Lemke et al.	204/129.55
5,180,093	A	*	1/1993	Stansbury et al.	228/1.1
5,214,259	A		5/1993	Terakado et al.	219/56.22
5,217,154	A	*	6/1993	Elwood et al.	228/4.5
5,280,979	A	*	1/1994	Poli et al.	294/64.1
5,290,507	A	*	3/1994	Runkle	419/14
5,367,956	A	*	11/1994	Fogle, Jr.	102/202.2
5,463,197	A		10/1995	Miyazaki	219/56.22
5,463,896	A		11/1995	Abbate et al.	
5,491,605	A		2/1996	Hughbanks et al.	
5,527,441	A		6/1996	Offer	204/280
5,544,804	A	*	8/1996	Test et al.	228/180.5
5,601,740	A		2/1997	Eldridge et al.	219/130.4
5,616,257	A		4/1997	Harada et al.	219/56.21
5,649,355	A		7/1997	Offer	29/825
5,651,901	A		7/1997	Mohri et al.	219/69.17
5,676,856	A		10/1997	Haji et al.	219/56.21
5,797,388	A		8/1998	Nakamura et al.	228/180.5
5,816,472	A	*	10/1998	Linn	228/1.1
5,827,470	A	*	10/1998	Chatterjee et al.	264/604
5,931,368	A	*	8/1999	Hadar et al.	228/4.5
6,030,472	A	*	2/2000	Hajaligol et al.	148/651
6,073,827	A	*	6/2000	Razon et al.	228/4.5

OTHER PUBLICATIONS

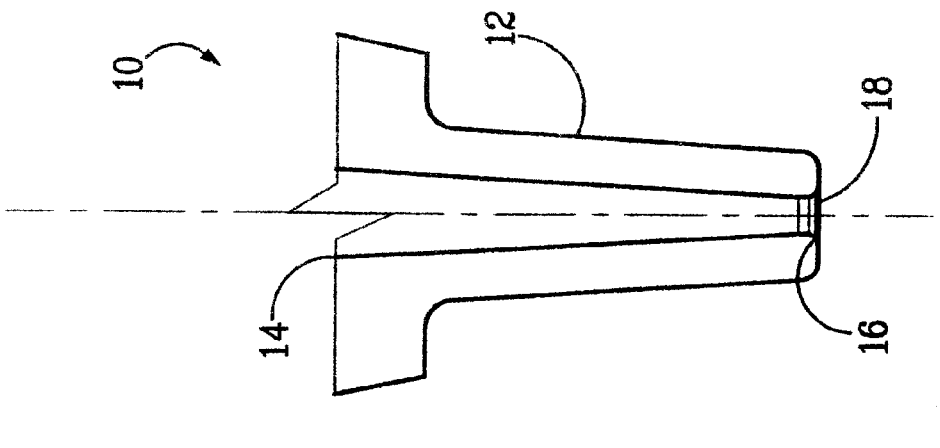
Instrument FAQs, Drivers, Libraries and Examples, Keithley Instruments Model 6517/6517A, http://208.240.90.52/techsupport/instruments/kth6517a.html, Keithley Instruments, Inc., 1999, pp. 1–2.

Keithley Instruments Model 6517A Electometer/High Resistance Meter, http://208.240.90.52/products/prod__pages . . . K13_pages/summary_pgs/6517A_Summary.html, Keithley Instruments, Inc., This or an equivalent was in use for testing the Applicants' invention, earlier than Feb. 25, 1999, pp. 1–9.

"Low–Current /High–Resistance Meters," Keithley Instruments Model 6517A Electrometer/High Resistance Meter, www.keithley.com, Keithley Instruments, Inc., This or an equivalent was in use for testing the Applicants' invention earlier than Feb. 25, 1999, pp. 112–115.

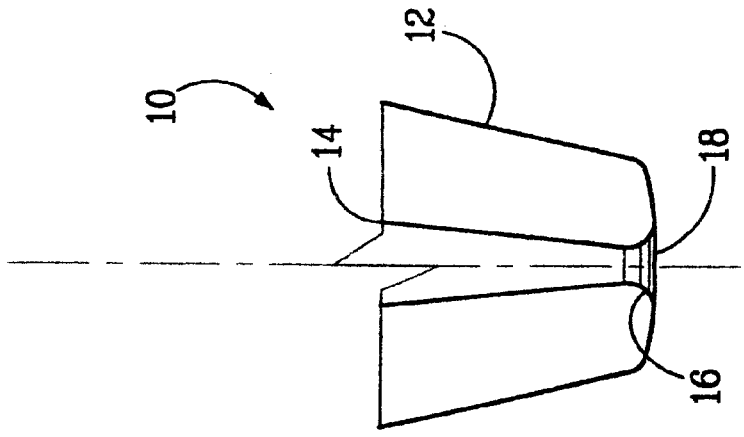
Keytech 200 XV–2 ESD Simulator, http://www.kandus-.com/Configurations/KEYTECH16842.html, K & Us Equipment, p. 1.

* cited by examiner



BOTTLE-NECK CAPILLARY

FIG. 3



NORMAL CAPILLARY

FIG. 2

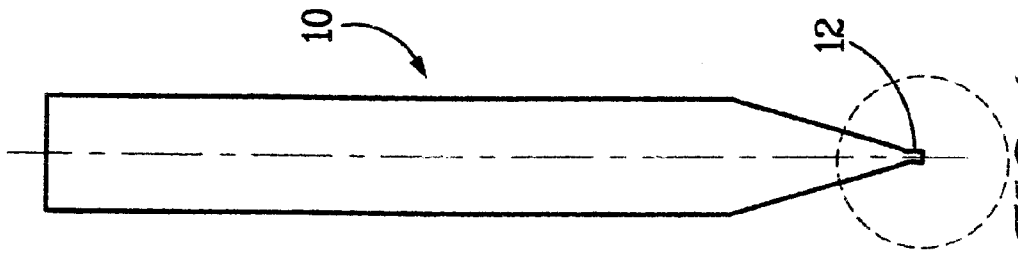


FIG. 1

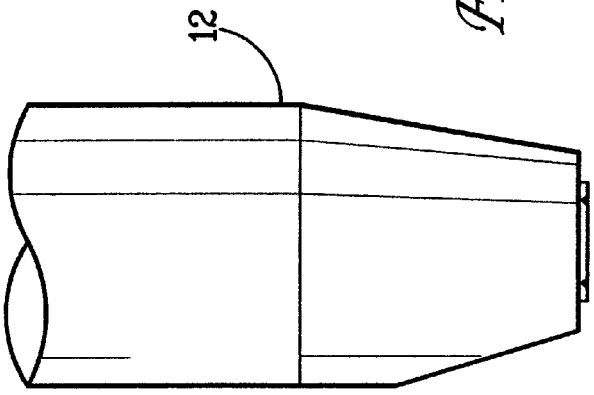


FIG. 5a

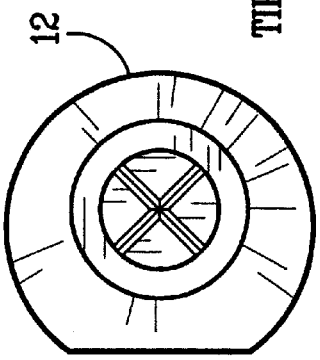


FIG. 5b

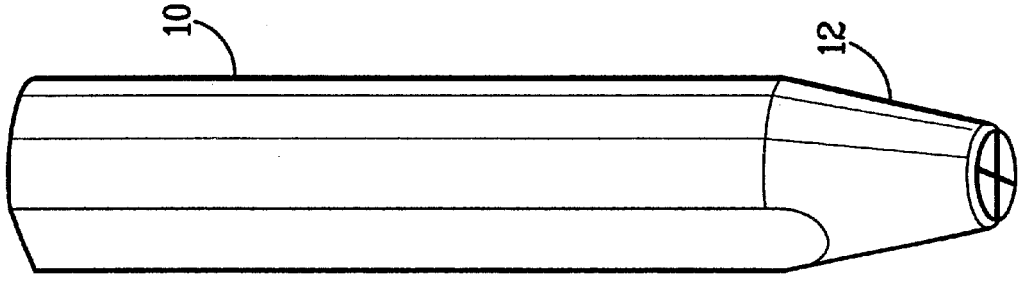


FIG. 4

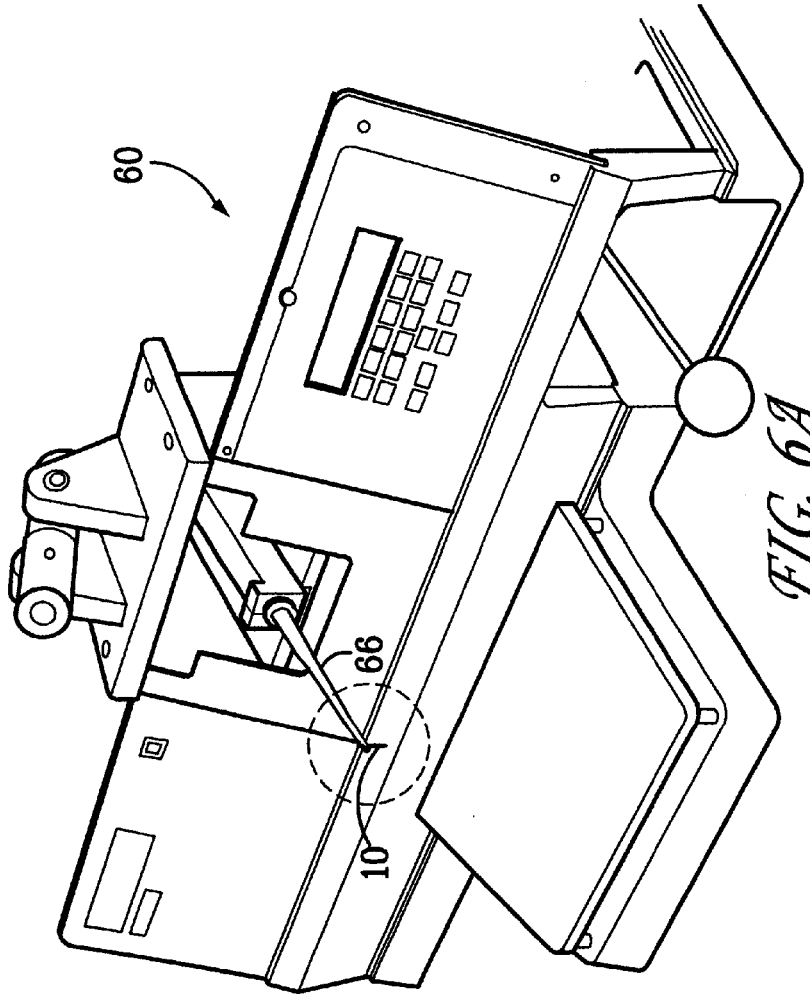
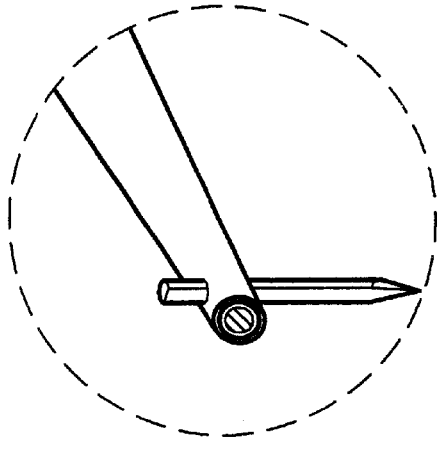
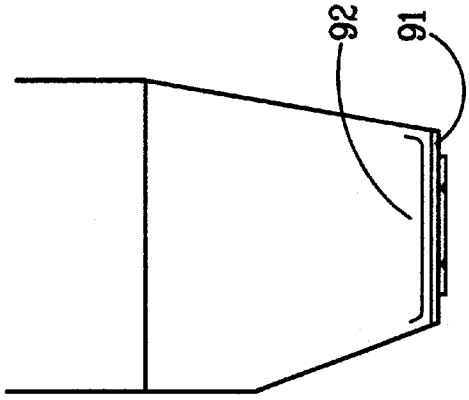


FIG. 6A



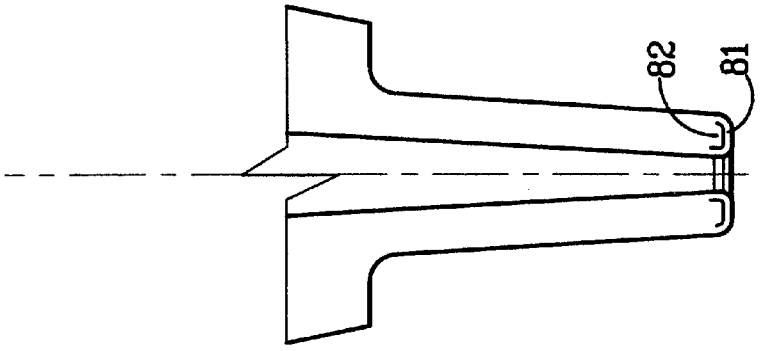
Transducer Horn Tip and Wedge Detail

FIG. 6B



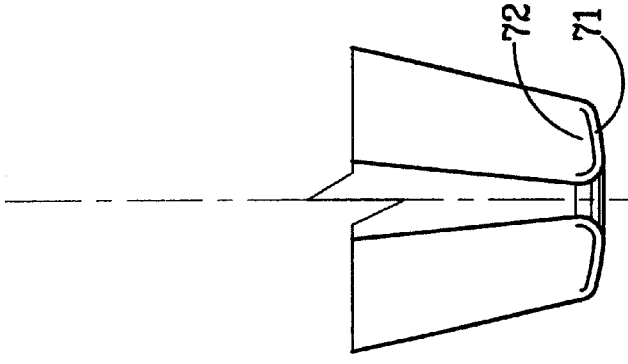
TIP DETAIL

FIG. 9



BOTTLE-NECK CAPILLARY

FIG. 8



NORMAL CAPILLARY

FIG. 7

DISSIPATIVE CERAMIC BONDING TIP

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefits of Provisional Application Ser. No. 60/121,694, filed Feb. 25, 1999, entitled Dissipative Ceramic Bonding Tip.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to bonding tool tips and more particularly to dissipative ceramic bonding tips for bonding electrical connections.

Description of the Prior Art

Integrated circuits are typically attached to a lead frame, and individual leads are connected to individual bond pads on the integrated circuit with wire. The wire is fed through a tubular bonding tool tip having a bonding pad at the output end. These tips are called capillary tips. An electrical discharge at the bonding tool tip supplied by a separate EFO (electronic flame off) device melts a bit of the wire, forming a bonding ball. Other bonding tools do not have the center tube, but have a feed hole or other feature for feeding the wire along, as needed. Some bonding tips have no such wire arrangement, as the wire is supplied, as in magnetic disk recording devices, where the wire is insulated and bonded to a magnetic head and then to a flexible wire circuit.

When the bonding tip is on the integrated circuit die side of the wire connection, the wire will have a ball formed on the end of the wire, as above, before reaching the next die bonding pad. The ball then makes intimate contact with the film formed on the die pad on the integrated circuit. The bonding tip is then moved from the integrated circuit die pad, with gold wire being fed out as the tool is moved, onto the bond pad on the lead frame, and then scrubbed laterally by an ultrasonic transducer. Pressure from the bonding tool tip and the transducer, and capillary action, 'flows' the wire onto the bonding pad where molecular bonds produce a reliable electrical and mechanical connection.

Bonding tool tips must be sufficiently hard to prevent deformation under pressure, and mechanically durable so that many bonds can be made before replacement. Prior art bonding tool tips were made of aluminum oxide, which is an insulator, but provides the wearability to form thousands of bonding connections. Bonding tool tips must also be electrically designed to produce a reliable electrical contact, yet prevent electrostatic discharge damage to the part being bonded. Certain prior art devices have a one or more volt emission when the tip makes bonding contact. This could present a problem, as a one volt static discharge could generate a 20 milliamp current to flow, which, in certain instances, could cause the integrated circuit to fail due to this unwanted current.

U.S. Pat. No. 5,816,472 to Linn describes a durable alumina bonding tool "without electrically conductive metallic binders." U.S. Pat. No. 5,616,257 to Harada describes covering the bonding tool electrode with an insulating cap or covering "made of a ceramic material" to produce a large electrostatic discharge that creates bonding balls of stable diameter. U.S. Pat. No. 5,280,979 to Poli describes a vacuum wafer-handling tool having a ceramic coating "made with a controlled conductivity" to prevent a large electrostatic discharge.

SUMMARY OF THE INVENTION

Electrically, dissipative ceramic bonding tips for bonding electrical connections to bonding pads on electrical devices

are disclosed. In accordance with the principles of the present invention, to avoid damaging delicate electronic devices by any electrostatic discharge, a bonding tool tip must conduct electricity at a rate sufficient to prevent charge buildup, but not at so high a rate as to overload the device being bonded. In other words, it is desirable for the bonding tip to discharge slowly. The tip needs to discharge to avoid a sudden surge of current that could damage the part being bonded. For best results, a resistance in the tip assembly itself should range from 10^5 to 10^{12} ohms. The tools must also have specific mechanical properties to function satisfactorily. The high stiffness and high abrasion resistance requirements have limited the possible material to ceramics (electrical non-conductors) or metals, such as tungsten carbide (electrical conductor).

In the present invention, bonding tool tips with the desired electrical conduction can be made with three different configurations.

First, the tools can be made from a uniform extrinsic semiconducting material which has dopant atoms in the appropriate concentration and valence states to produce sufficient mobile charge carrier densities (unbound electrons or holes) which will result in electrical conduction in the desired range. For example, polycrystalline silicon carbide uniformly doped with boron.

Second, the tools can be made by forming a thin layer of a highly doped semiconductor on an insulating core. In this case the core provides the mechanical stiffness and the semiconductor surface layer provides abrasion resistance and provides a charge carrier path from the tip to mount which will permit dissipation of electrostatic charge at an acceptable rate. For example, a diamond tip wedge that is ion implanted with boron.

Third, the tools can be made by forming a lightly doped semiconductor layer on a conducting core. The conducting core provides the mechanical stiffness and the semiconductor layer provides abrasion resistance and provides a charge carrier path from the tip to conducting core, which is electrically connected to the mount. The doping level is chosen to produce conductivity through the layer which will permit dissipation of electrostatic charge at an acceptable rate. For example, cobalt bonded tungsten carbide coated with titanium nitride carbide.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view vastly enlarged of a capillary bonding tool tip;

FIG. **2** is a cross-sectional view, vastly enlarged, of a capillary-type construction of the operating end or tip of a bonding tool;

FIG. **3** is a cross-sectional view of a bottle-neck capillary bonding tool tip;

FIG. **4** is an isometric view of a wedge bonding tool tip;

FIGS. **5***a* and **5***b* are top and front views, respectively, of the wedge design bonding tool tip as shown in conjunction with FIG. **4**; and

FIG. **6** is an isometric view of a typical commercial apparatus utilized in the wire bonding of a semiconductor integrated circuit chip or other apparatus.

FIG. **7** a cross section of embodiments of FIG. **2** having two layers.

FIG. **8** a cross section of embodiments of FIG. **3** having two layers.

FIG. **9** a cross section of embodiments of FIG. **5** having two layers.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** illustrates a typical capillary bonding tool **10**. Such bonding tools are usually about one-half inch (12–13 mm) long and about one-sixteenth inch (1.6 mm) in diameter. The bonding tool tip **12** itself is usually from 3 to 10 mils (0.08 to 0.25 mm) long. Running the length of the tool itself, but not viewable in FIG. **1**, is a tube hole which would accommodate a continuous fed length of gold wire (not shown).

FIG. **2** is a highly enlarged, cross-sectional view of the capillary bonding tool **10** as shown and described in FIG. **1**. Only that portion of the bonding tool **10** shown within the dotted circle in FIG. **1** is shown in FIG. **2**. Tool tip **12** has the hole tube **14** which may run the entire length of bonding tool **10**. The exit hole **18** is where the wire (not shown) would exit the tool tip **12**. If a ball is formed on the wire, the ball would be seen immediately adjacent the exit hole **18**. The chamfer **16** at the exit hole **18** is there for at least two reasons. First, to accommodate a ball that has been formed at the end of the gold wire. Also, the chamfer surface **16** is provided to allow for smoother looping of the wire as the bonding tool **10** is moved from the bonding pad on an integrated circuit to the bonding pad (not shown) on a lead frame of an integrated circuit assembly. The wedge tool for disk drive bonding is used to capture the insulated wire, lay it on the head and ultrasonically bond it there.

FIG. **3** is an alternative embodiment of a bonding tool **10** showing similar features, as the hole tube **14**, chamfer surface **16**, and exit hole **18**. This bonding tool tip, named a bottle-neck capillary tip, is provided for narrower bond situations where the bonding pitch (distance between the centers of the bonding pads) is smaller and smaller as the dimensions of an integrated circuit get smaller, or the number of circuits on a chip get larger, but the die area remains more or less constant.

FIG. **4** shows still another type of bonding tool **10**. This bonding tool is typically used with an integrated circuit die mounted on a lead frame (not shown). This is the case where the wires from the integrated circuit are not connected from the die to connections directly in an integrated circuit package, but from the integrated circuit die to a lead frame, which technology is well known to skilled practitioners in the art. The composition of the lead frame being different than the composition of an integrated circuit package, the tip **12** of the bonding tool **10** must be different to accommodate the different physical attributes of the integrated circuit lead frame, as seen in FIGS. **5** *a* and **5***b*.

FIG. **6***a* illustrates a typical wire bonding machine **60** for use in bonding wire leads in magnetic disk drive units. Shown within the dotted circle is the bonding tool **10**. The bonding tool **10** is mounted to arm **66** which is moved in the desired directions by the apparatus of wire bonding machine **60**. Such a machine is available as Model 7400 from the West Bond Company in Anaheim, Calif.

Typical bonding tips available on the market today are made of an insulator of alumina (Al_2O_3), sometimes termed aluminum oxide. This is a very hard compound which has been used on commercial machines with success as it provides a reasonably long life in use as a wire bonding tool. To insure that it is an insulator no conductive binders are used in these bonding tips. However, as stated previously, the problem has existed that an electrostatic discharge from the bonding tool making contact with the bonding pad of the desired circuit can damage the very circuit it is wiring up.

However, in accordance with the principles of the present invention, to avoid damaging delicate electronic devices by this electrostatic discharge, a bonding tool tip must conduct electricity at a rate sufficient to prevent charge buildup, but not at so high a rate as to overload the device being bonded. It has been determined that the tool must have electrical conduction greater than one ten-billionth of a mho (i.e. >1×10 raised to the minus 12th power reciprocal ohms) but its electrical conductivity must be less than one one-hundred thousandth of a mho (i.e. <1×10 raised to the minus fifth power reciprocal ohms). The resistance should be low enough so that the material is not an insulator, not allowing for any dissipation of charge and high enough so that it is not a conductor, allowing a current flow. For best results, a resistance in the tip assembly itself should range from 10^5–10^{12} ohms. For example, for today's magnetic recording heads 5 milliamps of current will damage them. Preferably, for today's magnetic recording heads, no more than 2 to 3 milliamps of current should be allowed to pass through the tip to the head.

The tools must also have specific mechanical properties to function satisfactorily. The high stiffness and high abrasion resistance requirements have limited the possible material to ceramics (electrical non-conductors) or metal, such as tungsten carbide (electrical conductor). The tip should have a Rockwell hardness of about 25 or above, preferably of about 32 or above. The tip needs to be able to last for at least two bondings.

In the present invention, bonding tool tips with the desired electrical conduction can be made with three different configurations.

First, the tools can be made from a uniform extrinsic semiconducting material which has dopant atoms in the appropriate concentration and valence states to produce sufficient mobile charge carrier densities (unbound electrons or holes) which will result in electrical conduction in the desired range. For example, polycrystalline silicon carbide uniformly doped with boron.

Second, the tools can be made by forming a thin layer of a highly doped semiconductor on an insulating core. In this case the core provides the mechanical stiffness and the semiconductor surface layer provides abrasion resistance and provides a charge carrier path from the tip to the mount, which will permit dissipation of electrostatic charge at an acceptable rate. For example, a diamond tip wedge that has a surface that is ion implanted with boron or a doped ceramic.

Third, the tools can be made by forming a lightly doped semiconductor layer on a conducting core. The conducting core provides the mechanical stiffness and the semiconductor layer provides abrasion resistance and provides a charge carrier path from the tip to conducting core, which is electrically connected to the mount. The doping level is chosen to produce conductivity through the layer which will permit dissipation of electrostatic charge at an acceptable rate. For example, cobalt bonded tungsten carbide coated with titanium nitride carbide.

FIGS. **7**, **8** and **9** illustrate the two-layered structure of the last two configurations. This structure is not intended to be specific to the type of tool tip. Rather, it could be used for any bonding tool tip. In the second and third configurations, the outer layers are labeled **71**, **81** and **91** and the cores are labeled **72**, **82** and **92**. In the second configuration, mentioned above, layers **71**, **81** and **91** are highly doped semiconductor and the cores **72**, **82** and **92** are insulators. In the third configuration, mentioned above, layers **71**, **81** and **91** are lightly doped semiconductor and the cores **72**, **82** and **92** are conductors. No significance should be attached to the

relative thickness or scale of the portions of the layer **71**. Layer **71** may or may not have a uniform thickness.

Dissipative tools can be manufactured by any of the following methods.

1. Mixing, molding and sintering reactive powders. Fine particles of the desired composition are mixed with organic and inorganic solvents, dispersants, binders, and sintering aids are then molded into oversize wedges. The pieces are carefully dried, and heated slowly to remove the binders and dispersants and then heated to a high enough temperature so that the individual particles sinter together into a solid structure with low porosity. The heat-treating atmosphere is chosen to facilitate the removal of the binder at a low temperature and to control the valence of the dopant atoms at the higher temperature and while cooling. After cooling, the pieces may be machined to achieve the required tolerances. The pieces may then be treated to produce the desired surface layer by ion implementation, vapor deposition, chemical vapor deposition, physical deposition, electro-plating deposition, neutron bombardment, or combinations of the above. The pieces may be subsequently heat treated in a controlled atmosphere to produce the desired layer properties through diffusion, recrystalization, dopant activation, or valence changes of metallic ions.
2. Hot pressing reactive powders. Fine particles of the desired composition are mixed with binders and sintering aids and then pressed in a mold at a high enough temperature to cause consolidation and binding of the individual particles into a solid structure with low porosity. The hot pressing atmosphere is chosen to control the valence of the dopant atoms. After cooling and removal from the hot press, the pieces may be machined to achieve the required tolerances. The pieces may then be treated to produce the desired surface layer by ion implantation, vapor deposition, chemical vapor deposition, physical deposition, electo-plating deposition, neutron bombardment or combinations of the above. The pieces may subsequently be heat treated in a controlled atmosphere to produce the desired layer properties through diffusion, recrystalization, dopant activation, or valence changes of metallic ions.
3. Fusion casting. Metals of the desired composition are melted in a non-reactive crucible then cast into an ingot. The ingot is then rolled, extruded, drawn, pressed, heat treated in a suitable atmosphere and chemically treated. The pieces are then machined to achieve the required tolerances. The metallic pieces are then heat treated to produce the desired surface layer by vapor deposition, chemical vapor deposition, physical deposition, electo-plating deposition, or combinations of the above. The pieces may be subsequently heat treated in a controlled atmosphere to produce the desired layer properties through diffusion, recrystalization, dopant activation, or valence changes of metallic ions.

The invention further includes that the layer used in the bonding process could be the following composition of matter. More specifically, a formula for dissipated ceramic comprising alumina (aluminum oxide Al_2O_3) and zirconia (zirconium oxide ZrO_2) and other elements. This mixture is both somewhat electrically conductive and mechanically durable. The tip of a bonding tool will be coated with this material or it could be made completely out of this material The shape of the tip may be wedge or circular shaped as shown and described in the earlier FIGS. **1** to **5**.

One actual sample was constructed with the following elements:

ELEMENT
Iron
Oxygen
Sodium
Carbon
Zirconium
Silicon
Aluminum
Yttrium

While the range of alumina could extend from 15% to 85% and the range of zirconia from 15% to 85%, another sample included alumina at 40% and zirconia at 60%.

The bonding tip of the present invention could be used for any number of different types of bonding. Two examples are ultrasonic and thermal bonding.

While the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the true spirit and scope of the invention. In addition, modifications may be made without departing from the essential teachings of the invention.

What is claimed is:

1. A tip having a dissipative material for use in wire bonding machines for connecting leads on integrated circuit bonding pads, wherein said dissipative material has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded.

2. A tip as in claim **1**, having a resistance in the range of 10^5 to 10^{12} ohms.

3. A tip as in claim **1**, having a high enough stiffness to resist bending when hot and a high enough abrasiveness so as to function for at least two uses.

4. A tip as in claim **1**, wherein said material is an extrinsic semiconducting material which has dopant atoms in the appropriate concentration and valence states to produce said resistance.

5. A tip as in claim **4** wherein said material comprises a polycrystalline silicon carbide uniformly doped with boron.

6. A tip as in claim **1** wherein said dissipative material comprises a doped semiconductor formed on an insulating core.

7. A tip as in claim **6**, wherein said insulating core is diamond and said doped semiconductor is an outer surface of said diamond that is ion implanted with boron.

8. A tip as in claim **1** wherein said material is a doped semiconductor formed on a conducting core.

9. A tip having

a dissipative material for use in wire bonding machines for connecting leads on integrated circuit bonding pads, wherein

said dissipative material is a doped semiconductor which is titanium nitride carbide, has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded, and is formed on a conducting core of cobalt bonded tungsten carbide.

10. A dissipative ceramic for use in capillary wedge-type wire bonding machines for connecting leads on integrated circuit bonding pads, wherein said dissipative ceramic is electrically dissipative.

11. The dissipative ceramic of claim **10**, wherein said electrically dissipative ceramic comprises alumina (Al_2O_3).

12. The dissipative ceramic of claim **10**, comprising zirconia (ZrO_2).

13. The dissipative ceramic of claim 10, comprising alumina (Al_2O_3) and zirconia (ZrO_2).

14. The dissipative ceramic of claim 13, wherein the range of alumina is from 15% to 85% and the range of zirconia is from 15% to 85%.

15. The dissipative ceramic of claim 13, having 40 percent alumina and 60 percent zirconia with other additives.

16. A dissipative ceramic comprising aluminum oxide (A_2O_3) zirconium oxide (ZrO_2).

17. The dissipative ceramic of claim 16, wherein the range aluminum oxide is from 15% to 85% and the range of zirconium oxide is from 15% to 85%.

18. The dissipative ceramic of claim 16, having of about 40 percent aluminum oxide and about 60 percent zirconium with other additives.

19. A method of manufacturing a dissipative bonding tip comprising:

forming a dissipative material as a bonding tip that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded.

20. The method of claim 19 wherein the step of forming includes mixing, molding and sintering reactive powders.

21. The method of claim 19 wherein the step of forming includes hot pressing reactive powders.

22. The method of claim 19 wherein the step of forming includes fusion casting.

23. The method of claim 19, wherein said dissipative material has a resistance in the range of 10^5 to 10^{12} ohms.

24. The method of claim 19, wherein said dissipative material has a high enough stiffness to resist bending when hot, and has a high enough abrasiveness to function for at least two uses.

25. The method of claim 19, wherein said dissipative material is an extrinsic semiconducting material which has dopant atoms in the appropriate concentration and valence states to produce said resistance.

26. The method of claim 19, wherein said dissipative material comprises a polycrystalline silicon carbide uniformly doped with boron.

27. The method of claim 19, wherein said dissipative material comprises a doped semiconductor, and said step of forming includes forming said doped semiconductor on an insulating core.

28. The method of claim 27, wherein said insulating core is diamond and said doped semiconductor is an outer surface of said diamond that is ion implanted with boron.

29. The method of claim 19, wherein said dissipative material comprises a doped semiconductor, and said step of forming includes forming said doped semiconductor on a conducting core.

30. A method of manufacturing a dissipative bonding tip comprising:

forming a dissipative material having at least a doped semiconductor that is titanium nitride carbide, as a bonding tip that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough to avoid current flow large enough to damage said device being bonded,

wherein said step of forming includes forming said doped semiconductor on a conducting core of cobalt bonded tungsten carbide.

31. The method of claim 19 wherein the step of forming comprises:

mixing fine particles of a composition appropriate for forming said dissipative material with a solvent, a dispersant, a binder, and a sintering aid to form a mixture;

molding the mixture into at least one wedge;

drying the at least one wedge;

providing a heat-treating atmosphere that facilitates removal of the binder at a low temperature and that controls the valence of the dopant atoms;

heating the at least one wedge at a temperature appropriate to remove the binder and the dispersant;

heating the at least one wedge to a high enough temperature to sinter the particles together into a solid structure having low porosity; and

cooling the solid structure.

32. The method of claim 19 wherein the step of forming comprises:

forming a solid structure; and

machining the solid structure to achieve a required size and shape within a required tolerance.

33. The method of claim 19 wherein the step of forming comprises:

forming a solid structure; and

treating the solid structure by ion implantation, vapor deposition, chemical vapor deposition, physical deposition, electro-plating deposition, or neutron bombardment to produce a surface layer.

34. The method of claim 33 wherein the step of forming further comprises:

producing the desired layer properties within said surface layer by heating the solid structure in a controlled atmosphere to induce diffusion, recrystalization, dopant activation, or valence changes of metallic ions.

35. The method of claim 19 wherein the step of forming comprises:

mixing fine particles of a composition appropriate for forming said dissipative material with binders and sintering aids into a mixture;

choosing a hot pressing atmosphere to control a valence of dopant atoms;

pressing the mixture in a mold at a temperature high enough to cause consolidation and binding of the particles into a solid structure having low porosity; and

cooling and removing the solid structure from the mold.

36. The method of claim 19 wherein the step of forming comprises:

melting metals of a composition appropriate for forming said dissipative material in a non-reactive crucible;

casting the melted metals into an ingot;

rolling the ingot into a rolled ingot;

extruding the rolled ingot into an extruded material;

drawing the extruded material into a drawn material;

pressing the drawn material in a pressed material; and

heating the pressed material.

37. A method of using a bonding tip, comprising:

bonding a device using a bonding tip made with a dissipative material that has a resistance low enough to prevent a discharge of charge to said device and high enough to avoid current flow large enough to damage said device.

38. The method of claim 37, wherein said dissipative material has a resistance in the range of 10^5 to 10^{12} ohms.

39. The method of claim 37, wherein said dissipative material has a high enough stiffness to resist bending when hot and has a high enough abrasiveness to function for at least two uses.

40. The method of claim 37, wherein said dissipative material is an extrinsic semiconducting material which has

dopant atoms in appropriate concentration and valence states to produce said resistance.

41. The method of claim **37** wherein said dissipative material comprises a polycrystalline silicon carbide uniformly doped with boron.

42. The method of claim **37**, wherein said dissipative material comprises a doped semiconductor formed on an insulating core.

43. The method of claim **42**, wherein said insulating core is diamond and said doped semiconductor is an outer surface of said diamond that is ion implanted with boron.

44. The method of claim **37** wherein said dissipative material is a doped semiconductor formed on a conducting core.

45. A method of using a bonding tip, comprising:

bonding a device using a bonding tip made with a dissipative material that is a doped semiconductor of titanium nitride carbide and has a resistance low enough to prevent a discharge of charge to said device and high enough to avoid current flow large enough to damage said device, wherein said dissipative material is formed on a conducting core of cobalt bonded tungsten carbide.

46. A device comprising:

a bonding tip having a dissipative material

that is positioned to come in contact with a device being bonded during bonding,

in which a current is allowed to flow that is produced by static charge generated during bonding, and

that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough so that the current flow is not large enough to damage said device being bonded.

47. The device of claim **46** wherein the current flow allowed is no more than 3 milliamps.

48. A method of manufacturing a dissipative bonding tip comprising:

forming a bonding tip having a dissipative material

that is positioned to come in contact with a device being bonded during bonding,

in which a current is allowed to flow that is produced by static charge generated during bonding, and

that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough so that the current flow is not large enough to damage said device being bonded.

49. The method of claim **46** wherein the current flow allowed is no more than 3 milliamps.

50. A method of bonding using a dissipative bonding tip comprising:

providing a bonding tip having a dissipative material that has a resistance low enough to prevent a discharge of charge to a device being bonded and high enough so that the current flow is not large enough to damage a device being bonded,

positioning the bonding tip so that the dissipative material electrically couples with the device being bonded during bonding,

forming a bond on the device being bonded, and

allowing a current flow that is produced by static charge generated by the bonding.

51. The method of claim **46** wherein the current flow allowed is no more than 3 milliamps.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,354,479 B1
DATED : March 12, 2002
INVENTOR(S) : Steven Frederick Reiber and Mary Louise Reiber

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Delete [73] Assignee: **SJM Technologies**, Mountain View, CA (US)."

Signed and Sealed this

Twenty-seventh Day of May, 2003

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,354,479 B1
APPLICATION NO. : 09/514454
DATED : March 12, 2002
INVENTOR(S) : Reiber et al.

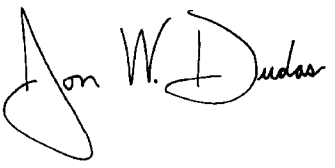
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim 49 at Column 10, Line 14, that portion of the claim reading "The method of claim 46" should read -- The method of clam 48 --

In Claim 51 at Column 10, Line 29, that portion of the claim reading "The method of claim 46" should read -- The method of claim 50 --

Signed and Sealed this

Twenty-ninth Day of January, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

Disclaimer

6,354,479—Steven Frederick Reiber, Sunnyvale; Mary Louise Reiber, Los Altos, both of CA (US). DISSIPATIVE CERAMIC BONDING TIP. Patent Dated March 12, 2002. Disclaimer filed December 7, 2009 by Co-Inventor and Co-Owner, Steven Frederick Reiber.

Hereby enters this disclaimer to claims 20-22, 25-31, 33-36, 40-45 of said patent.

(*Official Gazette, June 15, 2010*)

EXHIBIT E

US006651864B2

(12) **United States Patent**
Reiber et al.

(10) **Patent No.: US 6,651,864 B2**
(45) **Date of Patent: Nov. 25, 2003**

(54) **DISSIPATIVE CERAMIC BONDING TOOL TIP**

(76) Inventors: **Steven Frederick Reiber**, 4409 Vivien Way, Rocklin, CA (US) 95677; **Mary Louise Reiber**, 867 Mossy Ridge, Linclon, CA (US) 95648

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/036,579**

(22) Filed: **Dec. 31, 2001**

(65) **Prior Publication Data**

US 2002/0096551 A1 Jul. 25, 2002

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/514,454, filed on Feb. 25, 2000, now Pat. No. 6,354,479.
(60) Provisional application No. 60/288,203, filed on May 1, 2001, and provisional application No. 60/121,694, filed on Feb. 25, 1999.

(51) **Int. Cl.**[7] **B23K 37/00**; B23K 31/00; B23K 1/00; B23K 5/00

(52) **U.S. Cl.** **228/4.5**; 228/180.5; 228/6.1; 228/6.2; 219/56.4; 219/56.22

(58) **Field of Search** 228/4.5, 180.5, 228/6.1, 6.2; 219/56.21, 56.22

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,892,924	A		6/1959	Wood
3,538,205	A		11/1970	Gates, Jr. et al.
3,660,050	A		5/1972	Iler et al.
3,986,653	A		10/1976	Gilding
4,020,543	A		5/1977	Pennings
4,171,477	A	*	10/1979	Funari 219/56.21
4,182,947	A		1/1980	Brower

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0435423		7/1991
GB	2287897		10/1995
JP	54037114		3/1979
JP	63164228		7/1988
JP	02-67741 A	*	3/1990
JP	04-149065 A	*	5/1992

OTHER PUBLICATIONS

James R. Huntsman et a., "Test Methods for Static Control Products," Electrical Overstress/Electrostatic Discharge Symposium Proceedings, Sep. 21, 1982, pp. 94–109, vol. 4, IIT Research Institute, Chicago, IL.

Newburg, Carl E., "Test Report," Anza Technology, Inc., Static Dissipative Ceramic Rods for Wire Bonding Applications, Tested for Electrical Properties Discharge Current Resistance and Decay Time, Report 2000–92, River's Edge Technical Service, Nov. 29, 2000, pp. 1–5.

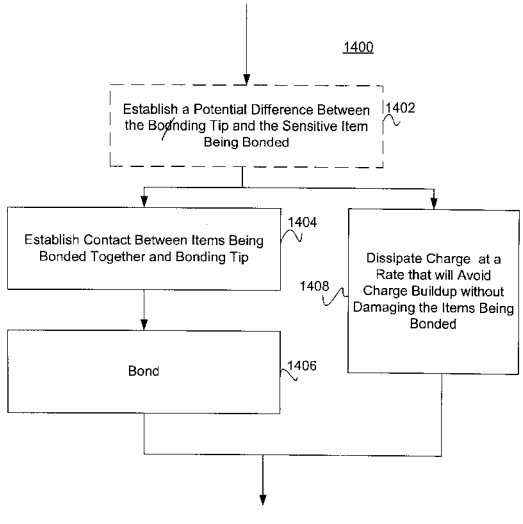
(List continued on next page.)

Primary Examiner—Tom Dunn
Assistant Examiner—Lynne Edmondson
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

Methods for making and using dissipative ceramic bonding tool tips for wire bonding electrical connections to bonding pads on integrated circuit chips and packages. The method of using the dissipative ceramic bonding tool tip includes dissipating charge while bonding to avoid damaging delicate electronic devices by a sudden surge of accumulated charge. The method of making the tool tip includes affecting its conductivity so that it conducts electricity at a rate sufficient to prevent charge buildup, but not sufficient to overload the device being bonded. For best results, a resistance in the tip assembly itself should range from 5×10^4 or 10^5 to 10^{12} ohms. In addition, the tips must also have specific mechanical properties to function satisfactorily.

78 Claims, 15 Drawing Sheets



U.S. PATENT DOCUMENTS

4,315,128	A		2/1982	Matcovich et al.	
4,331,048	A		5/1982	Dworak et al.	
4,387,283	A		6/1983	Peterson et al.	
4,390,771	A		6/1983	Kurtz et al.	
4,502,983	A		3/1985	Omori et al.	
4,513,190	A	*	4/1985	Ellett et al.	219/56.21
4,555,052	A	*	11/1985	Kurtz et al.	228/104
4,691,854	A		9/1987	Haefling et al.	
4,705,204	A		11/1987	Hirota et al.	
4,772,498	A	*	9/1988	Bertin et al.	428/34.4
4,821,944	A	*	4/1989	Tsumura	228/110.1
4,897,710	A		1/1990	Suzuki et al.	
4,909,427	A		3/1990	Plaisted et al.	
4,998,002	A		3/1991	Okikawa et al.	
5,123,935	A	*	6/1992	Kanamaru et al.	51/309
5,178,742	A		1/1993	Lemke et al.	
5,180,093	A		1/1993	Stansbury et al.	
5,214,259	A		5/1993	Terakado et al.	
5,217,154	A	*	6/1993	Elwood et al.	228/4.5
5,280,979	A		1/1994	Poli et al.	
5,290,507	A		3/1994	Runkle	
5,367,956	A		11/1994	Fogle, Jr.	
5,463,197	A		10/1995	Miyazaki	
5,463,896	A		11/1995	Abbate et al.	
5,491,605	A		2/1996	Hughbanks et al.	
5,527,441	A		6/1996	Offer	
5,544,804	A		8/1996	Test et al.	
5,601,740	A		2/1997	Eldridge et al.	
5,616,257	A		4/1997	Harada et al.	
5,649,355	A		7/1997	Offer	
5,651,901	A		7/1997	Mohri et al.	
5,676,856	A		10/1997	Haji et al.	
5,797,388	A		8/1998	Nakamura et al.	
5,816,472	A	*	10/1998	Linn	228/1.1
5,827,470	A		10/1998	Chatterjee et al.	
5,931,368	A		8/1999	Hadar et al.	
6,030,472	A		2/2000	Hajaligol et al.	
6,073,827	A		6/2000	Razon et al.	
6,354,479	B1	*	3/2002	Reiber et al.	228/4.5

OTHER PUBLICATIONS

Stan Weitz, "Tends in ESD Test Methods," Materials Testing Section of the ETS Testing Laboratory, Electrotech Systems, http://www.electrotechsystems.com, 1998, pp.1–7.

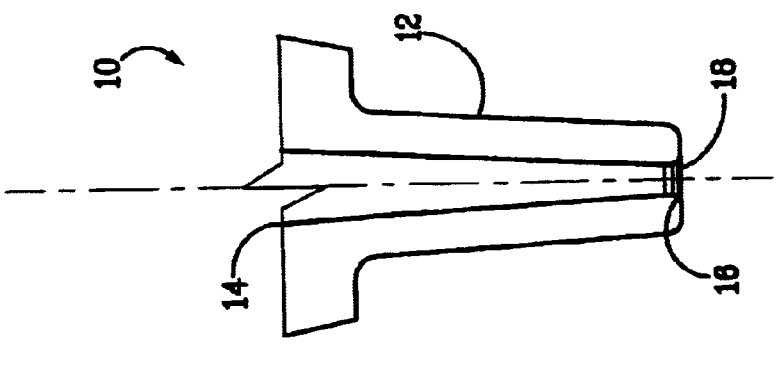
Instrument FAQs, Drivers, Libraries and Examples, Keithley Instruments Model 6517/6517A, http://208.240.90.52/techsupport/instruments/kth6517a.html, Keithley Instruments, Inc., 1999, pp. 1–2.

Keithley Instrumets Model 6517A Electrometer/High Resistance Meter, http://208.240.90.52/products/prod_pages . . . K13_pages/summary_pgs/6517A_Summary.html, Keithley Instruments, Inc., pp.1–9 no date avail.

"Low–Current/High–Resistance Meters," Keithley Instruments Model 6517A Electrometer/High Resistance Meter, www.keithley.com, Keithley Instruments, Inc., pp. 112–115 no date avail.

Keytech 200 XV–2 ESD Simulator, http://www.kandus.com/configurations/keytech16842.html, K & Us Equipment, p.1 no date avail.

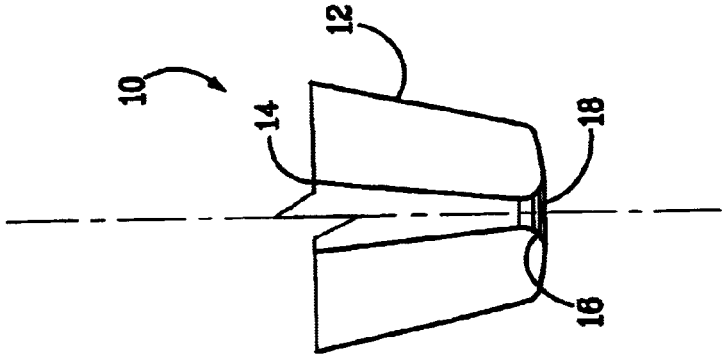
* cited by examiner



BOTTLE-NECK CAPILLARY

FIG. 3

PRIOR ART



NORMAL CAPILLARY

FIG. 2

PRIOR ART

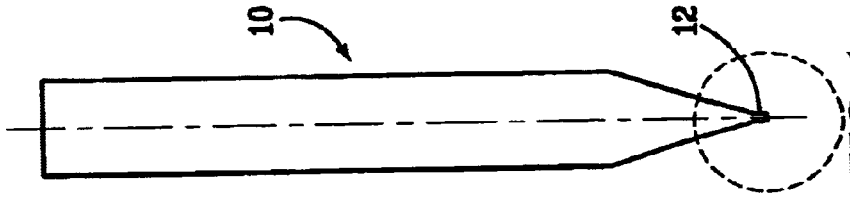


FIG. 1

PRIOR ART

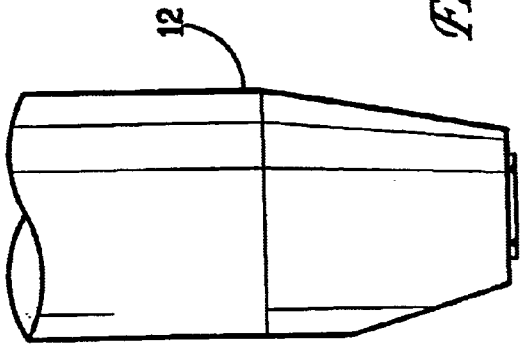


FIG. 5A
PRIOR ART

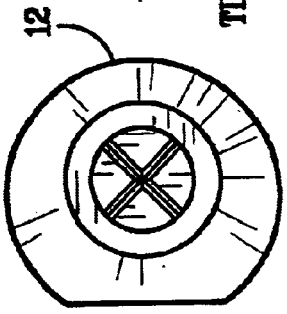


FIG. 5B
TIP DETAIL
PRIOR ART

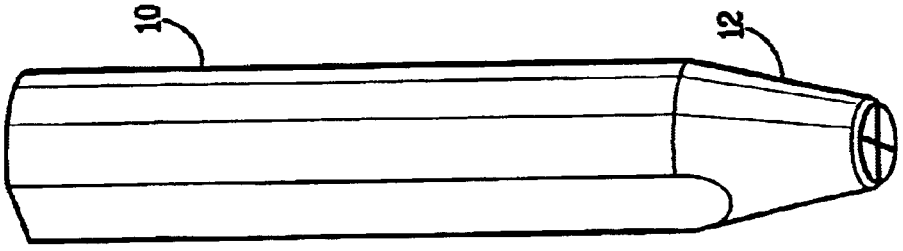


FIG. 4
PRIOR ART

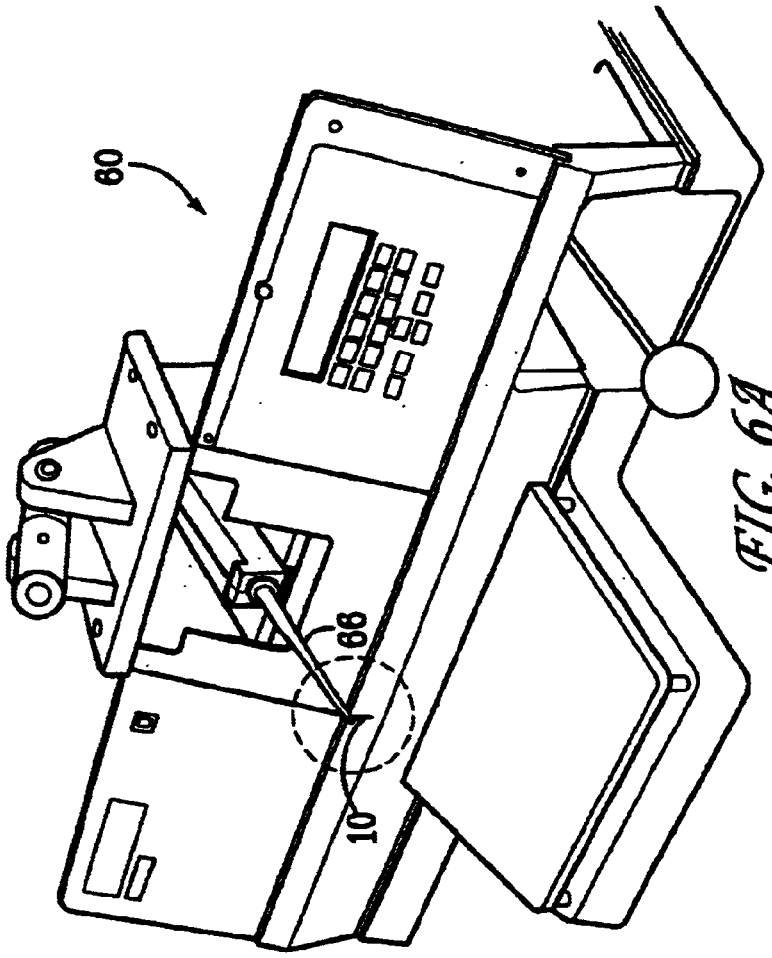
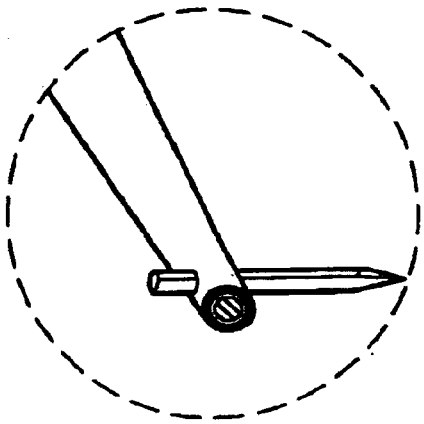
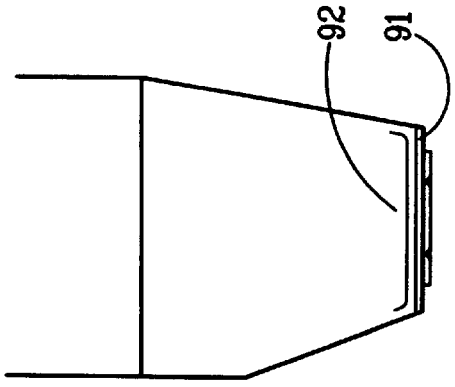


FIG. 6A
PRIOR ART



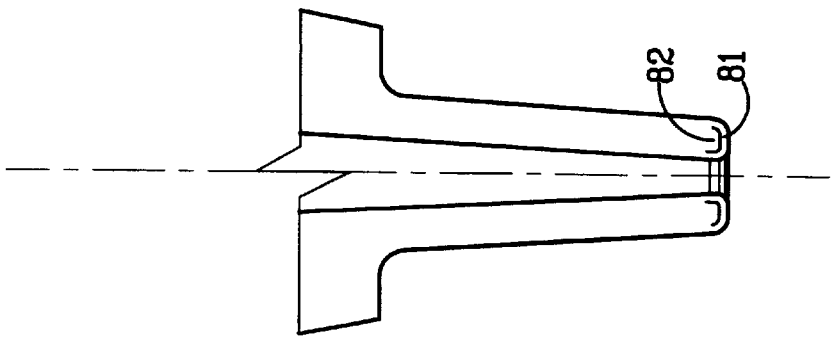
Transducer Horn Tip and Wedge Detail

FIG. 6B
PRIOR ART



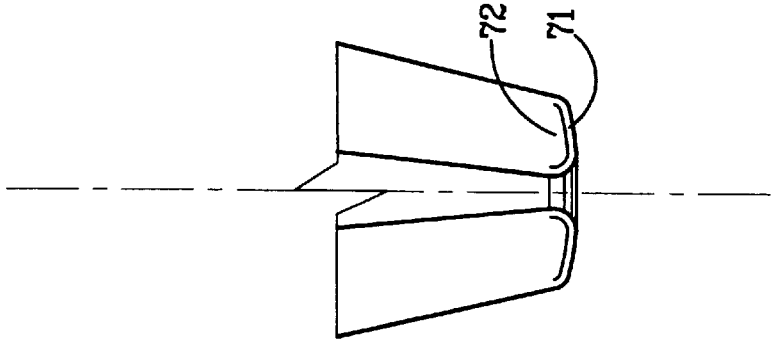
TIP DETAIL

FIG. 9



BOTTLE-NECK CAPILLARY

FIG. 8



NORMAL CAPILLARY

FIG. 7

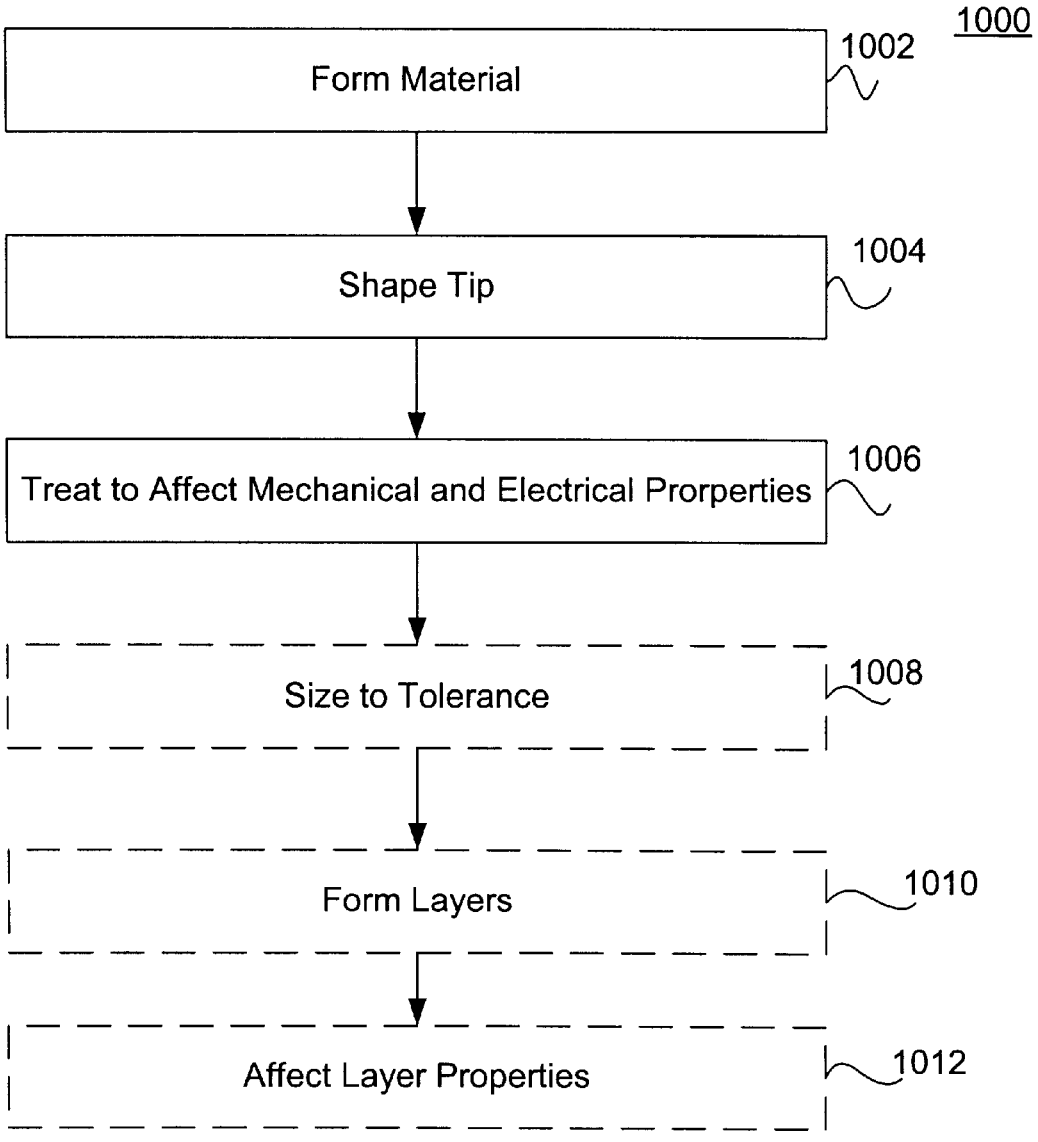

1000
Form Material
1002
Shape Tip
1004
Treat to Affect Mechanical and Electrical Prorperties
1006
Size to Tolerance
1008
Form Layers
1010
Affect Layer Properties
1012

FIG. 10

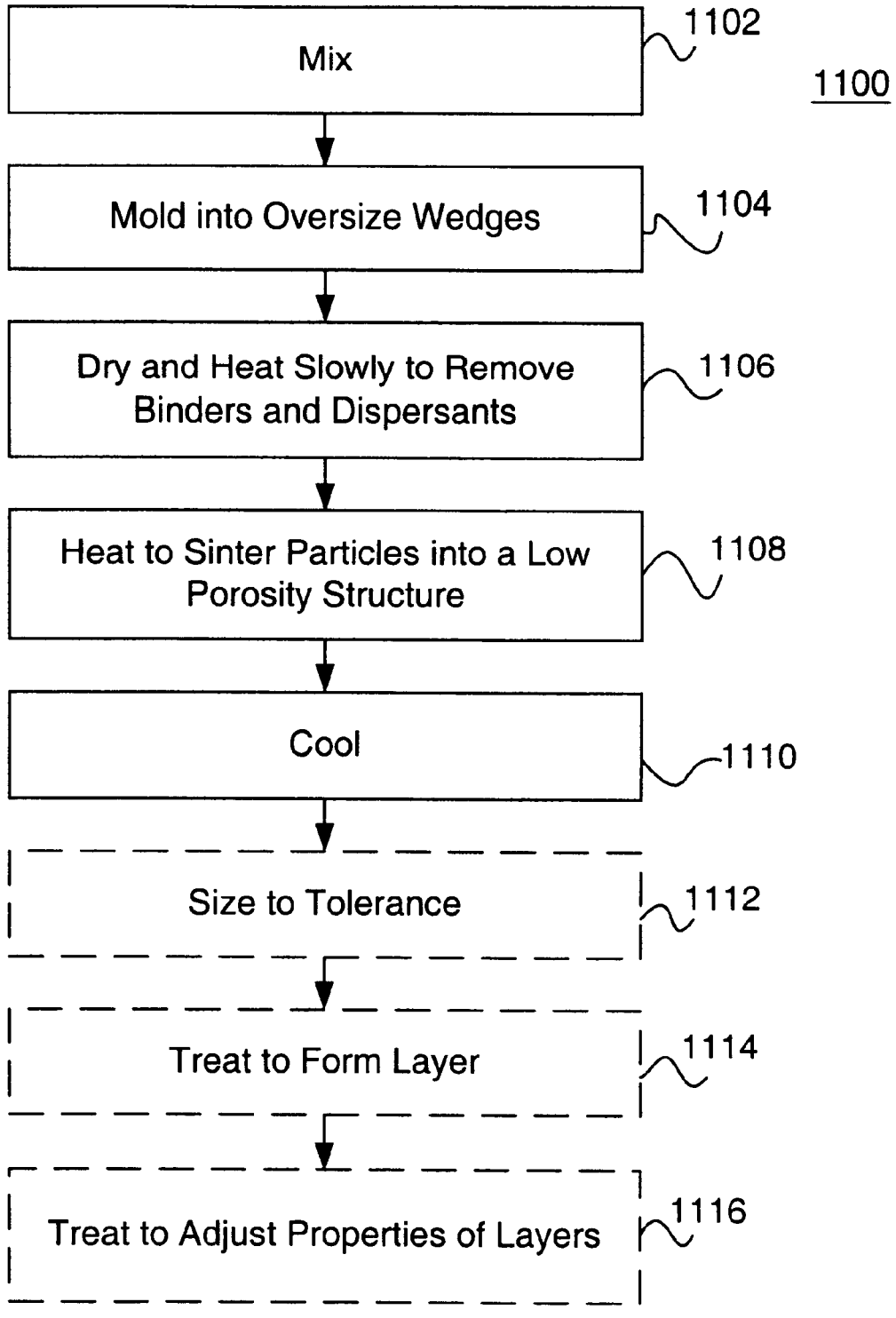

Mix
1102
1100
Mold into Oversize Wedges
1104
Dry and Heat Slowly to Remove Binders and Dispersants
1106
Heat to Sinter Particles into a Low Porosity Structure
1108
Cool
1110
Size to Tolerance
1112
Treat to Form Layer
1114
Treat to Adjust Properties of Layers
1116

FIG. 11

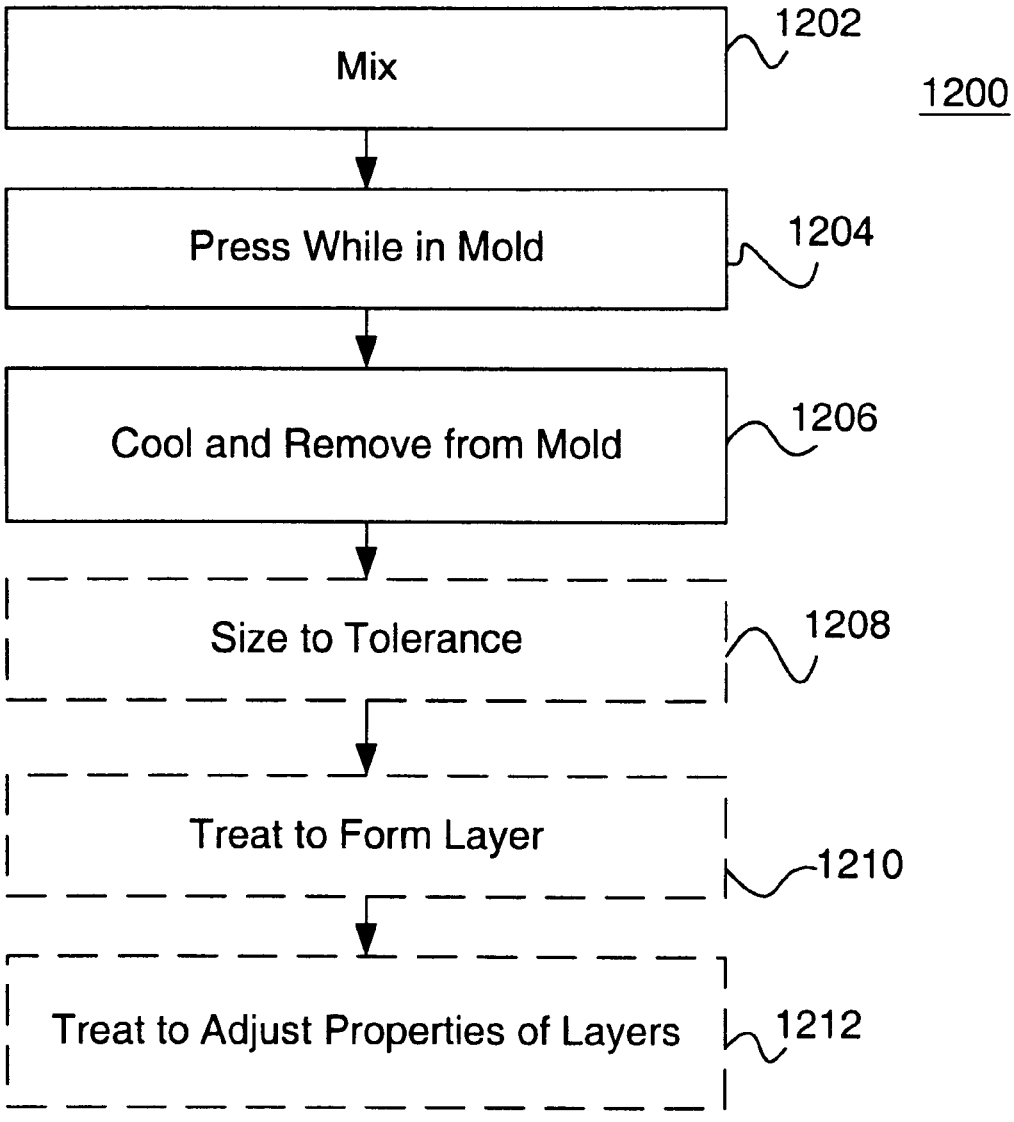

Mix
1202
1200
Press While in Mold
1204
Cool and Remove from Mold
1206
Size to Tolerance
1208
Treat to Form Layer
1210
Treat to Adjust Properties of Layers
1212

FIG. 12

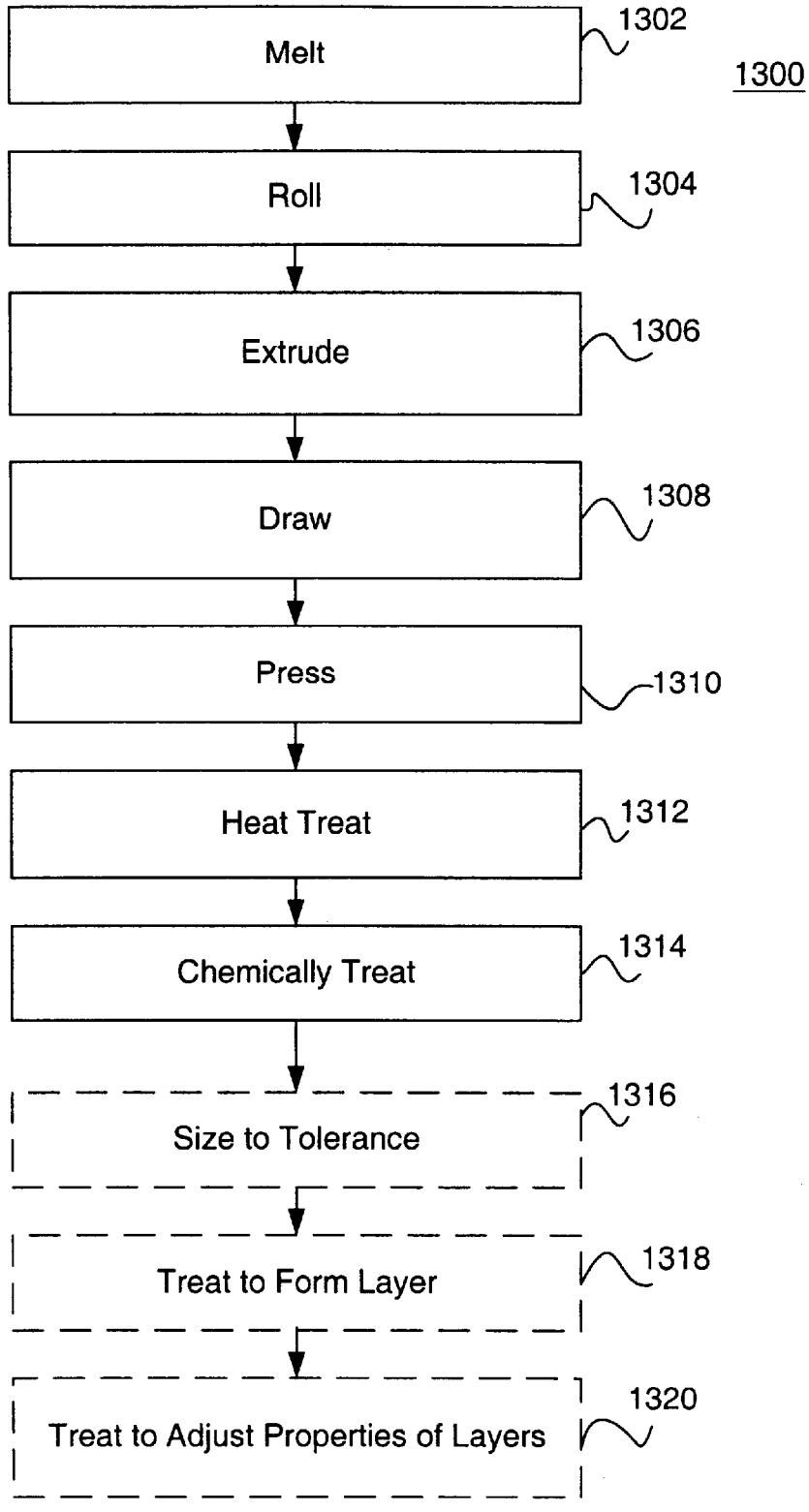

Melt
1302
1300
Roll
1304
Extrude
1306
Draw
1308
Press
1310
Heat Treat
1312
Chemically Treat
1314
Size to Tolerance
1316
Treat to Form Layer
1318
Treat to Adjust Properties of Layers
1320

FIG. 13

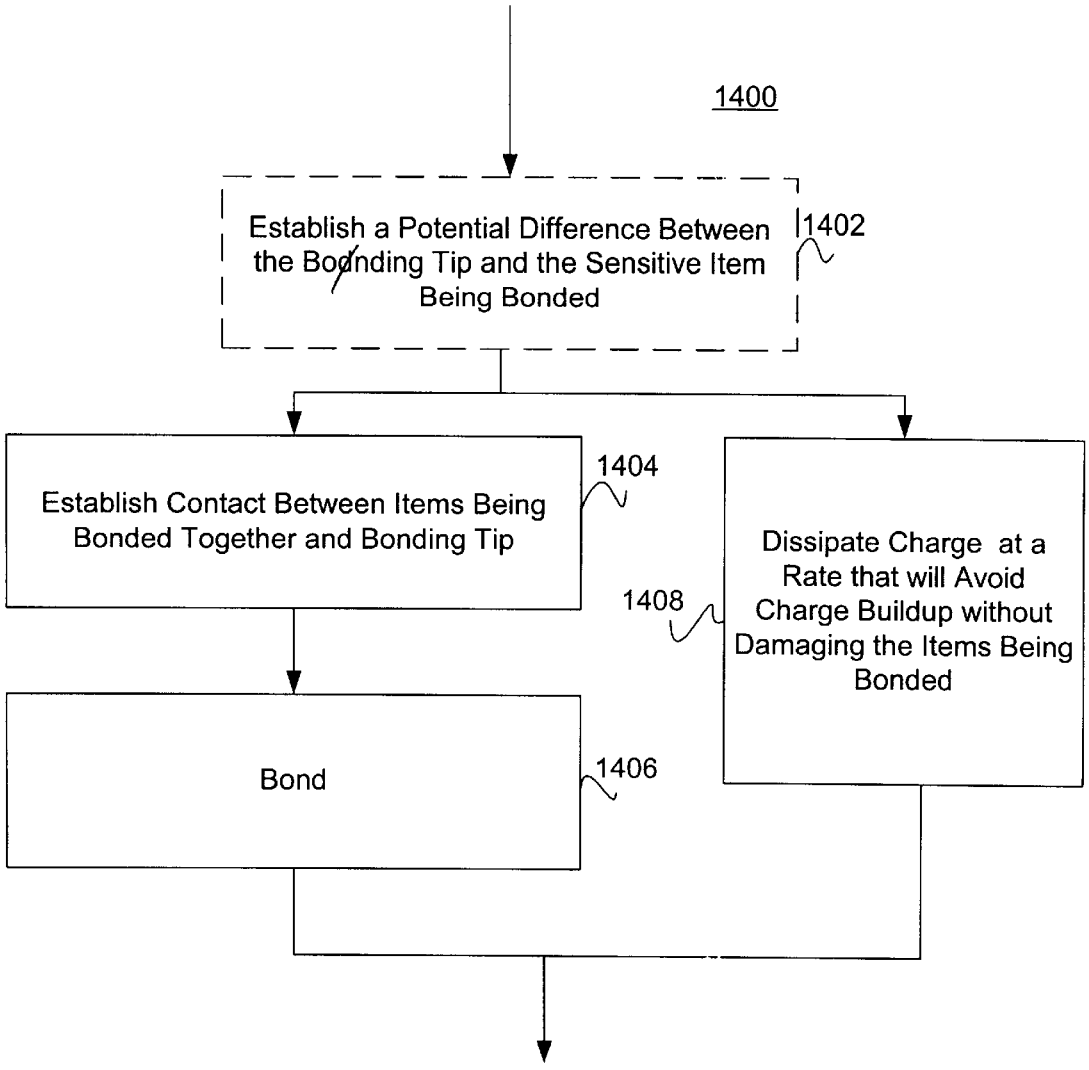

1400
Establish a Potential Difference Between the Bonding Tip and the Sensitive Item Being Bonded
1402
Establish Contact Between Items Being Bonded Together and Bonding Tip
1404
Dissipate Charge at a Rate that will Avoid Charge Buildup without Damaging the Items Being Bonded
1408
Bond
1406

FIG. 14

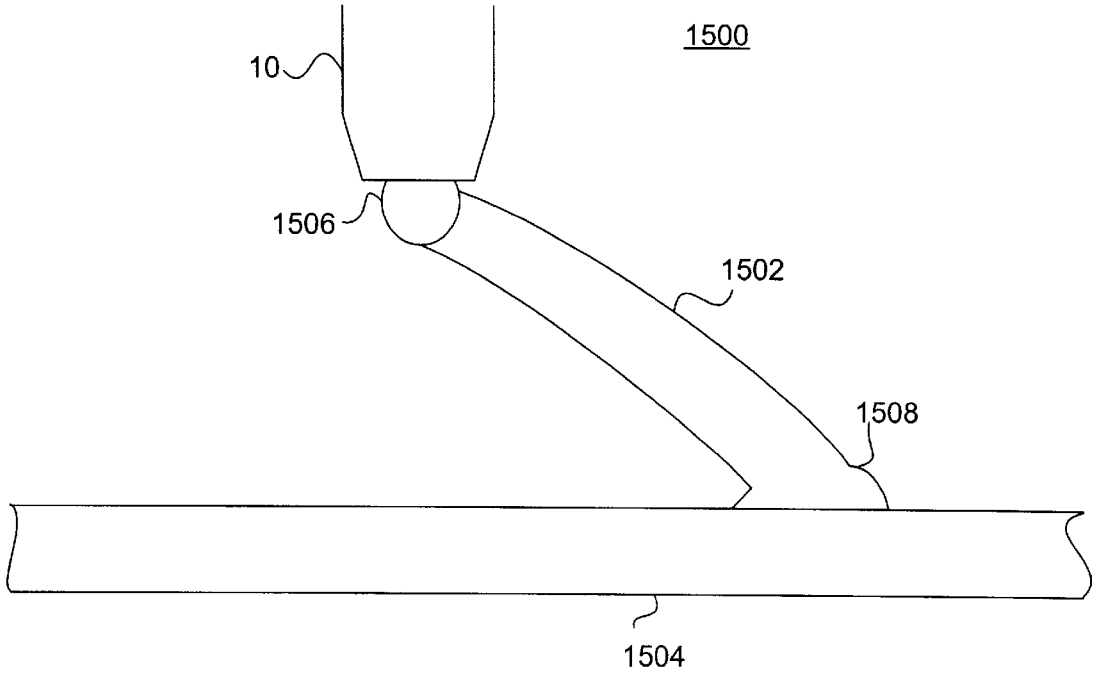


FIG. 15

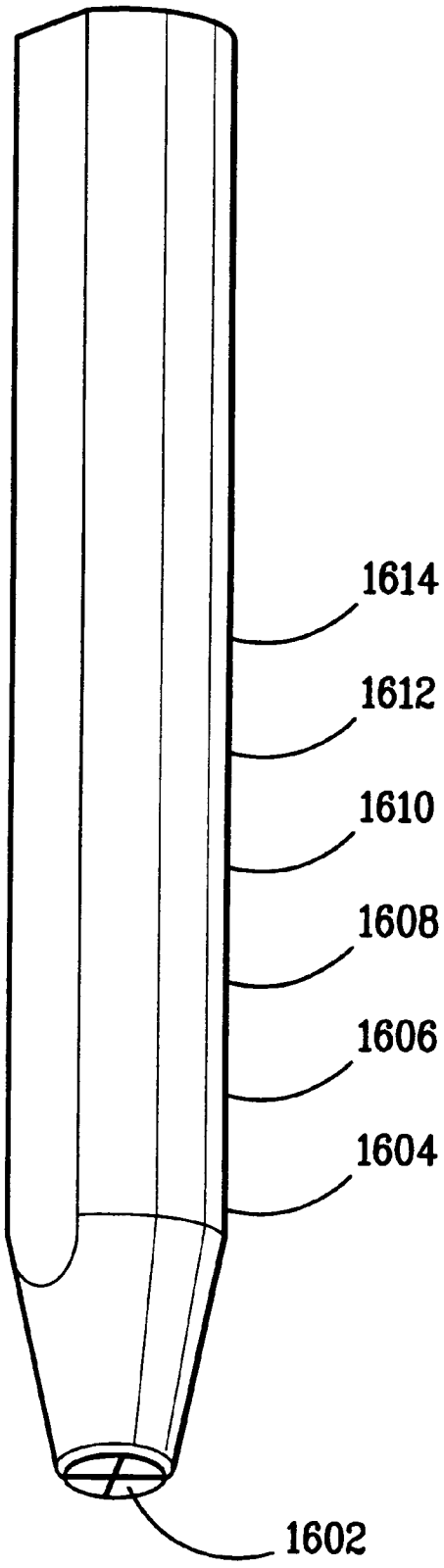
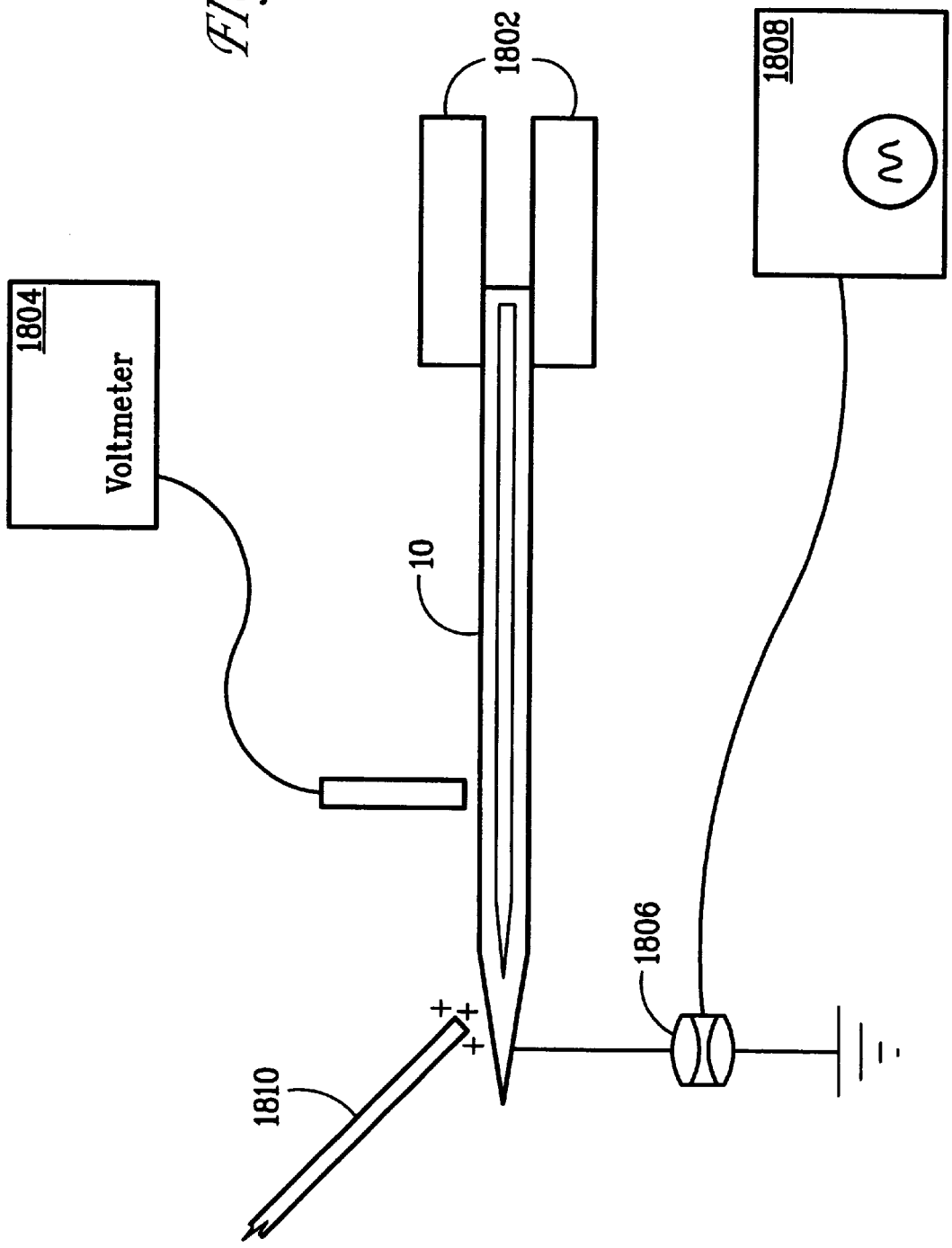


FIG. 16

Reading @	Rod #1		Rod #2	
	10V	100V	10V	100V
1"	$2.11 \times 10^8\Omega$	$1.80 \times 10^8\Omega$	$2.38 \times 10^8\Omega$	$1.89 \times 10^9\Omega$
2"	$2.78 \times 10^8\Omega$	$2.42 \times 10^8\Omega$	$4.13 \times 10^8\Omega$	$3.63 \times 10^8\Omega$
3"	$3.34 \times 10^8\Omega$	$3.03 \times 10^8\Omega$	$5.49 \times 10^8\Omega$	$5.17 \times 10^8\Omega$
4"	$4.35 \times 10^8\Omega$	$4.09 \times 10^8\Omega$	$8.52 \times 10^8\Omega$	$8.25 \times 10^8\Omega$
5"	$5.67 \times 10^8\Omega$	$5.46 \times 10^8\Omega$	$1.27 \times 10^9\Omega$	$1.22 \times 10^9\Omega$
6"	$7.05 \times 10^8\Omega$	$6.93 \times 10^8\Omega$	$1.26 \times 10^9\Omega$	$1.23 \times 10^9\Omega$
Average	$4.22 \times 10^8\Omega$	$3.96 \times 10^8\Omega$	$7.64 \times 10^8\Omega$	$1.01 \times 10^9\Omega$
Minimum	$2.11 \times 10^8\Omega$	$1.80 \times 10^8\Omega$	$2.38 \times 10^8\Omega$	$3.63 \times 10^8\Omega$
Maximum	$7.05 \times 10^8\Omega$	$6.93 \times 10^8\Omega$	$1.27 \times 10^9\Omega$	$1.89 \times 10^9\Omega$

FIG. 17

FIG. 18



Reading #	Small Diameter Rod #1	Small Diameter Rod #2
1	0.16 sec.	0.48 sec.
2	0.16 sec.	0.21 sec.
3	0.20 sec.	0.12 sec.
4	0.21 sec.	0.22 sec.
5	0.21 sec.	0.23 sec.
6	0.15 sec.	0.22 sec.
Average	0.18 sec.	0.25 sec.
Minimum	0.15 sec.	0.12 sec.
Maximum	0.21 sec.	0.48 sec.

FIG. 19

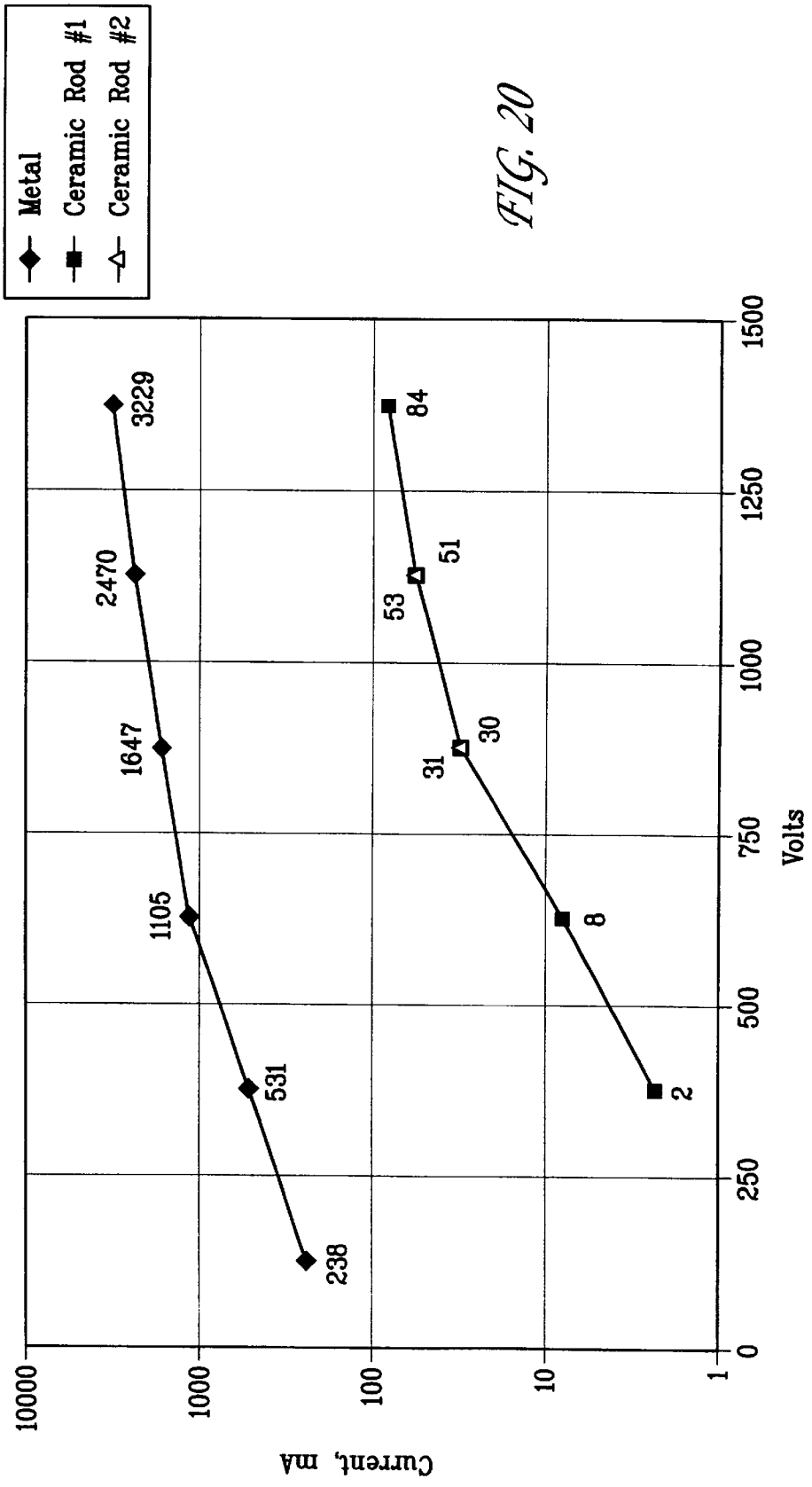

Metal
Ceramic Rod #1
Ceramic Rod #2
10000
1000
100
10
1
Current, mA
0
250
500
750
1000
1250
1500
Volts
3229
2470
1647
1105
531
238
84
53
51
31
30
8
2

FIG. 20

DISSIPATIVE CERAMIC BONDING TOOL TIP

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. patent application Ser. No. 09/514,454, filed Feb. 25, 2000, now U.S. Pat. No. 6,354,479 entitled, "Dissipative Ceramic Bonding Tool Tip," which claims benefits of Provisional Patent Application Ser. No. 60/121,694, filed Feb. 25, 1999, also entitled, "Dissipative Ceramic Bonding Tool Tip." This application also claims benefit of Provisional Application 60/288,203 filed May 1, 2001. The contents of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to bonding tool tips in general and more particularly to ceramic tool tips for bonding electrical connections.

2. Description of the Prior Art

Integrated circuits are typically attached to a lead frame, and individual leads are connected with wire to individual bond pads on the integrated circuit. The wire is fed through a tubular bonding tool tip having a bonding pad at the output end. These tips are called capillary tips. An electrical discharge at the bonding tool tip supplied by a separate Electronic Flame Off (EFO) device melts a bit of the wire, forming a bonding ball. Other bonding tools do not have the center tube, but have a feed hole or other feature for feeding the wire along, as needed. Some bonding tool tips have no such arrangement for feeding wire, such as bonding tool tips for magnetic disk recording devices, where the wire is insulated and bonded to a magnetic head and then to a flexible wire circuit.

When the bonding tool tip is on the integrated circuit die side of the wire connection, the wire will have a ball formed on the end of the wire, as above, before reaching the next die bonding pad. The ball then contacts the film formed on the die pad on the integrated circuit. The bonding tool tip is then moved from the integrated circuit die pad, feeding out gold wire as the tool is moved, onto the bond pad on the lead frame, and then scrubbed laterally by an ultrasonic transducer. Pressure from the bonding tool tip and the transducer, and capillary action, causes the wire to "flow" onto the bonding pad where molecular bonds produce a reliable electrical and mechanical connection.

Bonding tool tips must be sufficiently hard to prevent deformation under pressure, and mechanically durable so that many bonds can be made before replacement. Prior art bonding tool tips were made of aluminum oxide, which is an insulator that is durable enough to form thousands of bonding connections. Bonding tool tips must also be designed to produce a reliable electrical contact, yet prevent electrostatic discharge damage to the part being bonded. Certain prior art devices emit one or more volts when the tip makes bonding contact. This could present a problem, as a one volt static discharge could cause a 20 milliamp current to flow, which, in certain instances, could damage the integrated circuit or magnetic recording head.

U.S. Pat. No. 5,816,472 to Linn describes a durable alumina bonding tool "without electrically conductive metallic binders" that is therefore an insulator. U.S. Pat. No. 5,616,257 to Harada describes covering a bonding tool electrode with an insulating cap or covering "made of a ceramic material" to produce a large electrostatic discharge that creates bonding balls of stable diameter. U.S. Pat. No. 5,280,979 to Poli describes a vacuum wafer-handling tool having a ceramic coating "made with a controlled conductivity" to prevent a large electrostatic discharge.

SUMMARY OF THE INVENTION

The present invention may provide electrically dissipative ceramic bonding tool tips for bonding electrical connections to bonding pads on electrical devices. In accordance with principles of the present invention, the method of using the invention involves an added step of dissipating electrical charge at a rate sufficiently high to prevent charge buildup, but not high enough to overload the device being bonded. This added step is at least partially counter-intuitive because ordinarily charge dissipation is avoided so as not to overload the circuit. Consequently, to avoid damaging delicate electronic devices by any electrostatic discharge, the bonding tool tip is made to conduct electricity at a rate sufficiently high to prevent charge buildup, but not high enough to overload the device being bonded. In other words, it is desirable for the bonding tool tip to discharge slowly. The tip needs to discharge to avoid a sudden surge of current that could damage the part being bonded. For best results, a resistance in the tip assembly itself should range from about 5×10^4 or 10^5 to 10^{12} ohms. This range of resistances is adequate no matter the method of characterizing the resistance. The tools may also have a high stiffness and high abrasion resistance so that the tools have a long lifetime. However, bonding tool tips having a low stiffness and low abrasion resistance may also be made, except that they would have a short lifetime. Possible materials that can be used for the bonding tool tips that have a high abrasion resistance and high stiffness include ceramics (electrical non-conductors) or metals, such as tungsten carbide (an electrical conductor).

In the present invention, bonding tool tips with the desired electrical conduction can be made in at least three different configurations.

First, the tools can be made from a uniform extrinsic semiconducting material that has dopant atoms in the appropriate concentration and valence states to produce sufficient mobile charge carrier densities (unbound electrons or holes) that will result in electrical conduction in the desired range. For example, the tools can be made from polycrystalline silicon carbide uniformly doped with boron.

Second, the tools can be made with a thin layer of a highly doped semiconductor on an insulating core. In this case, the core provides the mechanical stiffness and the semiconductor surface layer provides abrasion resistance and provides a charge carrier path from the tip to the mount that will permit dissipation of electrostatic charge at an acceptable rate. For example, the tools can be made from a diamond tip wedge that has a surface that is ion implanted with boron.

Third, the tools can be made with a lightly doped semiconductor layer on a conducting core. The conducting core provides the mechanical stiffness and the semiconductor layer provides abrasion resistance and provides a charge carrier path from the tip to the conducting core, which is electrically connected to the mount. The doping level is chosen to produce a conductance through the layer that will permit dissipation of electrostatic charge at an acceptable rate. For example, the tools can be made from a cobalt-bonded tungsten carbide coated with titanium nitride carbide.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a vastly enlarged cross-sectional view of a capillary bonding tool tip;

FIG. **2** is a vastly enlarged cross-sectional view of a capillary-type construction of the operating end or tip of a bonding tool;

FIG. **3** is a cross-sectional view of a bottle-neck capillary bonding tool tip;

FIG. **4** is an isometric view of a wedge bonding tool tip;

FIGS. **5***a* and **5***b* are side and end views, respectively, of the wedge design bonding tool tip shown in FIG. **4**;

FIGS. **6***a* and **6***b* are an isometric view and a detailed close-up, respectively, of an apparatus utilized in the wire bonding of a semiconductor integrated circuit chip or other apparatus;

FIG. **7** is a cross-section of an embodiment of FIG. **2** having two layers;

FIG. **8** is a cross-section of an embodiment of FIG. **3** having two layers;

FIG. **9** is a cross-section of an embodiment of FIG. **5** having two layers;

FIG. **10** is a flowchart of a generic method for making a dissipative tool;

FIG. **11** is a flowchart of a first exemplary embodiment of the method of FIG. **10**;

FIG. **12** is a flowchart of a second exemplary embodiment of the method of FIG. **10**;

FIG. **13** is a flowchart of a third exemplary embodiment of the method of FIG. **10**;

FIG. **14** is a flowchart for a method of using the bonding tool tip according to the invention;

FIG. **15** is an illustration showing the method of use of a capillary bonding tool tip according to the invention;

FIG. **16** shows sections of the bonding tool whose resistances were measured;

FIG. **17** is a table of resistances for two ceramic bonding tools measured at the points shown in FIG. **16**;

FIG. **18** is a schematic representation of the experimental setup used for measuring the static discharge;

FIG. **19** is a table showing the static decay times measured using the experimental setup of FIG. **18**; and

FIG. **20** is a plot comparing the discharge current at various voltages of the ceramic bonding tools to a metal rod.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** illustrates a typical capillary bonding tool **10** according to the invention. Such bonding tools **10** can be about one-half inch (12–13 mm) long and about one-sixteenth inch (1.6 mm) in diameter. The bonding tool tip **12** can be from 1 to 8 mils, 2 to 6 mils, or 3 to 10 mils (0.08 to 0.25 mm) long. Running the length of the tool itself, but not viewable in FIG. **1**, is a tool hole that accommodates a continuously fed length of gold wire (not shown).

FIG. **2** is a highly enlarged, cross-sectional view of the capillary bonding tool **10** **10** shown in FIG. **1**. Only the portion of the bonding tool **10** that is shown within the dotted circle in FIG. **1** is shown in FIG. **2**. Tool tip **12** has a tool hole **14** which may run the entire length of bonding tool **10**. The wire (not shown) exits the tool tip **12** through an exit hole **18**. If a ball is formed on the wire, the ball is seen immediately adjacent the exit hole **18**. The wire may be gold, for example, but could be made from other conductive metals or mixtures of conductive metals. The chamfer **16** at the exit hole **18** has at least two purposes. First, the chamfer **16** accommodates a ball that has been formed at the end of the wire. Second, the chamfer surface **16** allows a smoother looping of the wire as the bonding tool **10** is moved from the bonding pad on an integrated circuit (not shown) to a bonding pad (not shown) on a lead frame (not shown) of an integrated circuit assembly (not shown). The inner diameter of the bonding tool tip **10** may be about 1.5 times the width of the wire being fed through it. For example the inner diameter may be 1.3 or 1.4 to 1.6 microns.

Although the size of the bonding tool **10** may change according to the size of the component being manufactured, the diameter of the tool tip **12** may remain essentially the same.

FIG. **3** shows an alternative embodiment of a bonding tool **10** having similar features, such as the tool hole **14**, chamfer surface **16**, and exit hole **18**. This bonding tool tip, named a bottle-neck capillary tip, is provided for narrower bond situations where the bonding pitch (distance between the centers of the bonding pads) is small. Bonding tool tips and the bonding pitch tend to get smaller as the dimensions of integrated circuits get smaller, or as the number of circuits on a chip gets larger, while the die area remains more or less constant.

FIG. **4** shows still another type of bonding tool **10**, called a wedge tool, having end **14**, raised portion **16**, and grooves **18**. The FIG. **4** embodiment of bonding tool **10** can be used for disk drive bonding where it is used to capture the insulated wire, lay it on the head of bonding tip **12** and ultrasonically bond it to a part of the disk drive system, for example, or other device being bonded. Bonding tool **10** may also be used with an integrated circuit die mounted on a lead frame (not shown). When bonding a magnetic recording head or integrated circuit dies the wires from the magnetic recording head or integrated circuit die may not be connected from the die directly to connections in an integrated circuit package, but from the magnetic recording head or integrated circuit die to a lead frame, as is well-known to skilled practitioners in the art. The composition of the lead frame may be different than the composition of the integrated circuit package. The tip **12** of the bonding tool **10** of FIGS. **5***a* and **5***b* accommodates the different physical attributes of different integrated circuit lead frames. The grooves **18** in FIGS. **4**, **5***a* and **5***b* frictionally hold the pad being bonded in place during ultrasonic bonding. The grooves **18** are typically "v" shaped but other shapes such as cylindrical also work. The size of the grooves **18** and/or die area may be kept essentially constant despite differences in size of the component being worked on. The width of the grooves **18** may be approximately the same or slightly smaller than the diameter of the wire being bonded. In an embodiment, the grooves **18** are 1 to 30 microns wide and 1 to 30 microns deep. The grooves **18** may cut through the entire depth of the raised portion **16**, which may also be 1 to 30 microns deep. In an embodiment, raised portion **16** is 6 to 7 microns deep, grooves **18** are 2.5 to 4.5 microns deep, raised portion **16** is 100 to 150 microns wide. Raised portion **16** and end **14** may be 8 to 35 or 40 microns wide. Although FIGS. **4**, **5***a*, and **5***b* show two grooves **18** forming a cross the bonding tool tip **12** may have just one groove or a mesh of intersecting and/or parallel groves. Although the grooves **18** are illustrated as being perpendicular they may be at any angle with respect to one another.

FIG. **6***a* illustrates a typical wire bonding machine **60** for use in bonding wire leads in magnetic disk drive units. Shown within the dotted circle is the bonding tool **10**. The bonding tool **10** is mounted to an arm **66** that can be moved in the desired directions by the apparatus of wire bonding machine **60**. Such a machine is available as Model 7400 from the West Bond Company in Anaheim, Calif.

Typical bonding tool tips available on the market today are made of an insulator of alumina (Al_2O_3), sometimes termed aluminum oxide, ruby, or sapphire, which are very hard compounds that have been used successfully on commercial machines. Wire bonding tool tips made of alumina, ruby, or sapphire have a reasonably long lifetime. In the prior art, to ensure that the tool tip is an insulator, no conductive binders are used in these bonding tool tips. However, as stated previously, a problem has existed that an electrostatic discharge from the bonding tool making contact with the bonding pad of the circuit can damage the very circuit it is wiring.

In accordance with principles of the present invention, to avoid damaging delicate electronic devices by this electrostatic discharge, bonding tool tip **12** should conduct electricity at a rate sufficiently high to prevent charge buildup, but not high enough to overload the device being bonded. It has been determined that the bonding tool **10** may have an electrical conductance greater than one ten-billionth of a mho (i.e. $>1\times10^{-12}$ reciprocal ohms (Ω^{-1}) of power) and its electrical conductivity may be less than one one-hundred thousandth of a mho (i.e. $<1\times10^{-5}$ Ω^{-1}). The resistance should be low enough that the material is not an insulator that does not allow charge dissipation, and high enough that it is not a conductor allowing a current flow that is damaging to the device being bonded. For best results, a resistance in the tip assembly itself should range from 5×10^4 or 10^5 to 10^{12} ohms. For example, today's magnetic recording heads are damaged by 5 milliamps of current. In an embodiment that may be used with magnetic recording heads, no more than 2 to 3 milliamps of current should be allowed to pass through the bonding tool tip **12** to the head.

In an embodiment, to achieve high stiffness and high abrasion resistance, ceramics (electrical non-conductors) or metals, such as tungsten carbide (an electrical conductor) are used. The bonding tool tip of this embodiment may have a Rockwell hardness of about 25 or above, preferably of about 32 or above. The tip needs to be able to last for at least two bondings.

In the present invention, bonding tool tips with the desired electrical conduction can be made in at least three different configurations.

First, the tools can be made from a uniform extrinsic semiconducting material that has dopant atoms in the appropriate concentration and valence states to produce sufficient mobile charge carrier densities (unbound electrons or holes) that will result in electrical conduction in the desired range. For example, polycrystalline silicon carbide uniformly doped with boron can give the desired range of conductivity. Preferably the amount of boron used is 5–7% by weight of the polycrystalline silicon carbide.

Second, the tools can be made by forming a thin layer of a highly doped semiconductor on an insulating core. For example, a diamond tip wedge may have a surface that is ion implanted with boron or have a surface that is a doped ceramic. In this case the core provides the mechanical stiffness and the semiconductor surface layer provides abrasion resistance and provides a charge carrier path from the tool tip **12** to the mount (not shown), which will permit dissipation of electrostatic charge at an acceptable rate. The conductance of the semiconductor surface layer should be about 10^{8-109} Ω^{-1}.

Third, the tools can be made by forming a lightly doped semiconductor layer on a conducting core, for example, a cobalt bonded tungsten carbide core coated with titanium nitride carbide. The conducting core provides the mechanical stiffness and the semiconductor layer provides abrasion resistance and provides a charge carrier path from the device being bonded to the conducting core, which is electrically connected to the mount. The doping level is chosen to produce a conductance through the layer that will permit dissipation of electrostatic charge at an acceptable rate. The conductivity of the semiconductor surface layer should be about $10^{7-108}\Omega^{-1}$.

FIGS. **7**, **8** and **9** illustrate the two-layered structure of the last two configurations. This structure is not intended to be specific to the type of tool tip. Rather, it could be used for any bonding tool tip. Layers **71**, **81**, and **91** could be 100–1000 Angstroms thick, for example. In the second and third configurations, the outer layers are labeled **71**, **81**, and **91** and the cores are labeled **72**, **82**, and **92**. In the second configuration, mentioned above, layers **71**, **81**, and **91** are highly doped semiconductor and the cores **72**, **82**, and **92** are insulators. In the third configuration, mentioned above, layers **71**, **81**, and **91** are lightly doped semiconductor and the cores **72**, **82**, and **92** are conductors. No significance should be attached to the relative thickness or scale of the portions of the layer **71**, **81**, and **91**, which may or may not have a uniform thickness.

Dissipative tools can be manufactured by any of several methods.

FIG. **10** illustrates a generic method **1000** for manufacturing dissipative tools. The process of creating a ceramic part may start with a powder having the same or a similar composition as desired in the ceramic part to be created. The quality of the ceramic component may be influenced by the quality of the ceramic powder used. To ensure quality, the ceramic powder may be tested and processed multiple times. The purity, concentration of agglomerations, and particle size of the ceramic powder may be monitored. The powder may be milled (e.g., attrition milled, balled milled, or turbo milled). The milling operation refines the particle size of the ceramic powder before process **1000** begins. In step **1002** a material, which may initially be a powder, is formed having the desired composition. The material is next shaped and sized in step **1004** into a form appropriate for the tool. The material may be further treated in step **1006** to affect or impart desired mechanical, chemical and/or electrical properties. Depending upon the embodiment, steps **1002**, **1004**, and **1006** may be performed simultaneously as part of one process. Since the properties of the material depend upon the process of making and the materials used for making the composition, parts or all of step **1006** may be performed before step **1004**. In optional step **1008** the material is sized to tolerance. In optional step **1010** the layering is formed. In optional step **1012** the material is further treated to impart desired properties to the layers or affect the desired properties of the layers.

FIGS. **11–13** show three examples of the method of FIG. **10**.

FIG. **11** shows method **1100**, which includes mixing, molding and sintering reactive powders of, for example, alumina (Al_2O_3), zirconia (Zr_2O_3), iron oxide (FeO_2), or titanium oxide (Ti_2O_3).

In general, sintering may involve the densification of powder compacts at a temperature below the melting point of the powder. The shrinkage occurs as the pores between the particles decrease in size until they are eliminated. The driving force of the sintering process is the reduction of surface energy. During the sintering of two spherical particles, for example, the inter-particle contact areas will increase as the growth into a neck between the particles

increases. There are three basic stages involved with the sintering process. In the first stage, the material between the particles moves outward by viscous flow, plastic flow or volume diffusion and is deposited on the neck area. The distance between the particle centers decreases and shrinkage occurs. If the material is transported from the circumference into the neck by evaporation-condensation or surface diffusion then there is no shrinkage. In the second stage, the growing necks merge, the original particle structures disappear and are replaced by polycrystalline bodies with an inter-granular pore network along grain boundary edges. The grain growth can occur by the movement of grain boundaries towards their centers of curvature. In the third stage the grain growth continues; pores become closed at grain comers and further densification occurs as the pores shrink. If the grain boundaries are sufficiently curved, they can move over the pores leaving them isolated in the grains. The process of further shrinkage may be slow once the pores are within the grains.

In step **1102** fine particles (e.g., a half of a micron in size) of the desired composition are mixed with organic and inorganic solvents, dispersants, binders, and sintering aids. The solvents could be Yttrium or H_2O, for example. The binder and/or the sintering aids could be any of, any combination of, or all of ceria, magnesia, yttria, boron, carbon colloidal silica, alumina solvents, ethyl silicate, any phosphate, any rare earth metal oxide, or yttrium, for example. In step **1104** the mix is molded into oversize wedges. The pieces are carefully dried, and heated slowly in step **1106** to remove the binders and dispersants and then heated in step **1108** to a high enough temperature so that the individual particles sinter together into a solid structure with low porosity. The slow heating can be done over three to eight hours at a rate of 50° C. to 200° C. every 15 minutes, for example, in an atmosphere of 500° C. or 1000° C. to 2500° C. for 3 to 24 hours, so as to obtain low porosity, and to obtain homogeneity. The sintering can occur at 4000° C., for example. The heat-treating atmosphere is chosen to facilitate the removal of the binder at a low temperature and to control the valence of the dopant atoms at the higher temperature and while cooling. The low porosity can be ensured by keeping the grain size less than about half a micron. Next, in step **1110**, the solid structures are allowed to cool preferably over a period of one to two hours. After cooling, in optional step **1112**, the pieces may be machined or otherwise sized to achieve the required tolerances. In optional step **1114** the pieces may then be treated to produce the desired surface layer by ion implementation, vapor deposition, chemical vapor deposition, physical deposition, electro-plating deposition, neutron bombardment, or combinations of the above. The pieces may be subsequently heat treated in optional step **1116** in a controlled atmosphere to produce desired layer properties (e.g., the desired hardness and resistivity) through diffusion, recrystallization, dopant activation, or valence changes of metallic ions.

In an example, in step **1104** silicon nitride or zirconia ceramic materials could be fabricated by firing a powder compact at a suitable temperature until agglomeration of the particles occurs with a decrease in the surface area and porosity of the compact. This process may involve chemical reactions, crystal growth and/or the formation of liquid phases and solid state diffusion. An untreated silicon nitride ceramic powder is typically in the alpha phase. The sintering process of step **1106** involves heating the ceramic powder to +2000° C. to convert the powder to the preferred beta-Si_3N_4 state. The beta-Si_3N_4 state has the high thermo-mechanical properties suitable for high temperature applications such as resistive heating. Silicon nitride is very difficult to sinter because it has very strong directional covalent bonds. Although silicon nitride may be at least partially sintered without adding sintering aids, the ceramic powder may not completely turn from the alpha phase to the beta-Si_3N_4 phase during the heating process without the sintering aids. Sintering aids of rare earth oxides and other oxides may act as nucleating agents for the Si_3N_4 powders to nucleate the formation of grains. Yttria (Y_2O_3) and Aluminum Oxide (Al_2O_3) may be used as the sintering aids although other sintering aids will also work.

In another example, silicon carbide, zirconia, or silicon nitride could be used for the bonding tip **12**. Although silicon nitride does not need much preparation before it enters the sintering stage of step **1106**, silicon carbide and zirconia have two phases that can exist that may affect the quality of the finished product. Silicon nitride has two phases, alpha and beta-Si_3N_4, a hexagonal structure, and can be used to make a polycrystalline ceramic. Similarly, zirconia exists as a monoclinic crystal at room temperature and inverts to a tetragonal phase above 1200° C. In other words, zirconia has a low temperature monoclinic state and a high temperature tetragonal state. The silicon nitride beta phase and the tetragonal zirconia crystal have the higher strength properties of their two respective phases but some stabilizers should be added in step **1102** in order to induce silicon nitride and zirconia to remain in their beta phase and tetragonal phase, respectively, during the cooling step **1110**. For example, a stabilizer such as magnesium oxide may be added in step **1102** to prevent the transformation upon cooling in step **1110**. The addition of yttria in step **1102** yields an extremely fine grained (less than 1 micron) microstructure known as tetragonal zirconia polycrystal (TZP).

The process of mixing in the additives during step **1102** to achieve the higher strength phase is called forming the green body.

There are several other types of sintering processes that can be used to manufacture the bonding tool tip. In reaction bonding sintering, in step **1106** the green body is placed in a chamber where it is heated and infiltrated with a reacting gas to form a compound. The process of reaction bonding silicon nitride to form a silicon nitride bonding tool tip involves taking a silicon green body between steps **1106** and **1108** and reacting the body to a gas of hydrogen and nitrogen to form Si_3N_4. Exposing the green body to the hydrogen and nitrogen gas is commonly known as nitriding. The body is nitrided in the gas starting at 1150° C. and slowly increasing the temperature to 1420° C. The resulting product is a mixture of alpha and beta silicon nitrides with 18 to 25% porosity. The original dimensions of the silicon compact remain virtually unchanged during the nitriding. The bonding tool tip can be machined after partial nitriding in step **1112**. Reaction bonding can be relatively cheap.

When using hot press sintering to form a bonding tool tip, a ceramic powder is placed in a die and then it is compressed at a high pressure while the powder is heated in step **1104**. When working with silicon nitride powers, the powder is hot pressed with a suitable oxide additive in a graphite die and it may be heated by induction, for example, to 1700° C. to 1800° C. to give a fully dense high strength beta-silicon nitride. Diamond machining follows the hot pressing.

When using Hot Isostatic Pressing (HIP) to form the bonding tool tip, in step **1104** the powder is placed in an evacuated pressure vessel. The vessel will simultaneously heat and isostatically press the material with an inert gas with pressures as high as 310 MPa (45,000 psi) and tem-

peratures up to 2000° C. The powder is simultaneously heated and isostatically pressed by inert gas pressure until densified.

FIG. **12** illustrates method **1200** of hot pressing reactive powders. Fine particles (e.g., a half of a micron in size) of the desired composition are mixed in step **1202** with binders and sintering aids and then pressed in a mold in step **1204** at a high enough temperature to cause consolidation and binding of the individual particles into a solid structure (e.g., 1000° C. to 4000° C., preferably 2000° C.) with low porosity (e.g., having grain size of less than half a micron in size). The hot pressing atmosphere is chosen to control the valence of the dopant atoms. After cooling and removal from the hot press in step **1206**, the pieces may be machined or otherwise sized to achieve the required tolerances in step **1208**. The pieces may then be treated in optional step **1210** to produce the desired surface layer (e.g., 100 to 1000 Angstroms thick) by ion implantation, vapor deposition, chemical vapor deposition, physical deposition, electro-plating deposition, neutron bombardment or combinations of the above. In optional step **1212** the pieces may subsequently be heat treated (e.g., 2000° C. to 2500° C. for 3 to 5 minutes) in a controlled atmosphere to produce the desired layer properties through diffusion, recrystallization, dopant activation, and/or valence changes of metallic ions.

FIG. **13** illustrates method **1300** of fusion casting. Metals of the desired composition are melted in step **1302** in a non-reactive crucible then cast into an ingot. The ingot is then rolled in step **1304**, extruded in step **1306**, drawn in step **1308**, pressed in step **1310**, heat treated (e.g., at 1000° C. or 500° C. to 2500° C. for one to two hours) in step **1312** in a suitable atmosphere, and chemically treated in step **1314**. The rolling **1304**, extruding **1306**, drawing **1308** and pressing **1310** steps shape the tip and the heat treatment **1312** and chemical treatment **1314** steps are for affecting or imparting the mechanical and electrical properties such as the hardness and resistivity. The pieces are then optionally machined or otherwise sized to achieve the required tolerances in step **1316**. The metallic pieces are then optionally heat treated to produce the desired surface layer by vapor deposition, chemical vapor deposition, physical deposition, electroplating deposition, or combinations of the above in step **1318**. The pieces may be subsequently heat treated (e.g., at 4000° C. for three to four hours) in a controlled atmosphere to produce the desired layer properties through diffusion, recrystallization, dopant activation, or valence changes of metallic ions in step **1320**.

Although steps **1008**, **1112**, **1208**, and **1316**; **1010**, **1114**, **1210**, and **1318**; and **1012**, **1116**, **1212** and **1320** share similar descriptions they are given different labels because the details of how to best carry out these steps may be partly dependent upon the details of the preceding steps.

In the three methods above the heat-treating, hot pressing, and controlled atmospheres are preferably primarily an inert gas such as nitrogen using a nitrogen-based furnace.

The green body for the bonding tool tip can be formed by using a variety of other methods of casting high temperature ceramics such as injecting molding, cold isostatic, extrusion, slip casting, Hot Isostatic Pressing (HIP), and gelcasting

Injection molding can be used with all types of ceramics. The features basic to injection molding are that the powder is placed in a thermosetting polymeric binder, is injected into a mold where it hardens with time, and then is ejected from the mold. A concern with injection molding is that the de-waxing or removing the resin should be done without degrading the surface of the green body.

When using slip casting, a slip may be made of water and the ceramic powder. The slip is cast into an absorbent mold. The casting rate is dependant on the pressure applied to the slip cast and the cast thickness. The geometry of the casting surface may also affect the casting time.

In extrusion, a feedrod for coextrusion is formed from the compounded material, which may have of a silicon nitride-filled core with a cladding of boron nitride-filled material. The feedrod is then extruded through a heated die to form fine filaments.

In dipcoating a single component filament (such as a silicon nitride-filled polymer) is pulled through a slurry of boron nitride which dries to form the cell boundary material. Gelcasting is a ceramic-forming process for making high-quality, complex-shaped ceramic parts. Gelcasting can be used for making bonding tool tips **12** with any of the ceramic powders mentioned in this specification. Gelcasting involves mixing ceramic powders in a polymerizable aqueous monomer solution that is then gelled in a mold. The cast body will be both homogeneous in its chemistry and have a certain density, resulting in the material properties (e.g., hardness and resistivity) being constant throughout the body and the drying and sintering processes having uniform volume changes. Using Gelcasting, the casting time from design to final fired part can be one week.

Layers **71**, **81**, and **91** of bonding tool tip **12** may be made from several compositions of matter. A formula for dissipated ceramic may include alumina and zirconia and/or other elements. This mixture is both somewhat electrically conductive and mechanically durable. The tip of a bonding tool is coated with this material or can be made completely out of this material. The tip may be wedge-shaped or circular-shaped as shown and described in the earlier FIGS. **1** to **5**, for example.

One actual sample was constructed with the following elements:

ELEMENT

Iron
Oxygen
Sodium
Carbon
Zirconium
Silicon
Aluminum
Yttrium

While the range of alumina could extend from 15% to 85% and the range of zirconia from 15% to 85%, in one embodiment the sample included alumina at 40% and zirconia at 60%.

FIG. **14** is a flowchart for a method of using the invention. In optional step **1402** an initial potential is established between the bonding tool tip and the item being bonded that is sensitive to electrical discharge. Although not necessary, establishing a potential may give the user some additional control over how the tip discharges. Establishing a potential may involve establishing an electrical connection or grounding the lead frame, individual leads on the integrated circuit and/or the individual bond pads on the integrated circuit. In step **1404** the bonding tool tip is placed in contact with the items being bonded together to hold them in place. In step **1406** the bond is formed. Steps **1404** and **1406** may be performed simultaneously as part of the same step. In step **1408** the charge is dissipated. This step may be performed simultaneously with steps **1404** and **1406**. It is important that

this step be performed whenever the tip and the electrostatic discharge sensitive component are in contact to prevent a discharge.

For example, in the case of a capillary tip the wire is fed through the tubular bonding tool tip prior to placing it in contact with the items being bonded. Then an electrical discharge at the bonding tool tip is supplied by a separate EFO device to melt a bit of the wire, forming a bonding ball. The ball then makes intimate contact with the film formed on the die pad on the integrated circuit, initiating the dissipation of charge. The bonding tool tip is then moved from the integrated circuit die pad, with gold wire being fed out as the tool is moved, onto the bond pad on the lead frame, and then scrubbed laterally by an ultrasonic transducer. Pressure from the bonding tool tip and the transducer, and capillary action, 'flows' the wire onto the bonding pad where molecular bonds produce a reliable electrical and mechanical connection while still dissipating charge. In this example the bonding, the contact between the bonding tool tip and the electrostatic discharge sensitive integrated circuit, and the dissipation all occur essentially simultaneously.

FIG. **15** shows a capillary bonding tool **10** being used to bond wire **1502** to pad **1504**. Ball **1506** will be used to bond wire **1502** to the next point. The bonding joint **1508** was formed with a ball similar to **1506**. The difference between this method of use and the prior art is primarily in the dissipation of charge from the bonding tool **10**.

The bonding tool tip **12** of the present invention could be used for any number of different types of bonding. Two examples are ultrasonic and thermal bonding.

FIG. **16** shows sections of the bonding tool **10** having end **1602** and points **1604–1614**. Point **1604** is 1 inch from end **1602** whose resistances were measured. Points **1604–1614** are each one inch apart.

Two ceramic rods **#1** and **#2** (not shown), were used as the base material for ceramic wire bonding tool tips **12** to form bonding tools **10** according to the invention. The two rods each had a diameter of approximately 0.07 inches. The point-to-point resistances along both of the rods were measured from the end of the bonding tool tip to various points along the tool tip at 10 and 100 volts. The resistance at each voltage was measured six times, each time from end **1602** to a different one of points **1604–1614** to obtain measurements of a 1, 2, 3, 4, 5, and 6 inch section, respectively, that starts at end **1602**.

FIG. **17** is a table of resistances for two ceramic bonding tools measured at the points shown in FIG. **16**. As shown in the table and as discussed in the preceding paragraph, the resistances were measured at 1, 2, 3, 4, 5, and 6 inches at 10V and 100V. The two bonding tools had point-to-point resistances that varied between 1.8×10^{8} Ω and 1.9×10^{9} Ω. After measuring the resistances according to FIG. **16** the static discharge was measured.

FIG. **18** is a schematic representation of the experimental setup used for measuring the static discharge having bonding tool **10**, clamp **1802**, voltmeter **1804**, current probe **1806**, oscilloscope **1808**, and ElectroStatic Discharge (ESD) simulator **1810**.

The static discharge was measured by charging bonding tool **10** and measuring the time required for the charge to dissipate. The charge was assumed to have dissipated once the current from the bonding tool **10** to ground dropped off significantly from its initial value (e.g., the current was less than 10% of its initial value). The current was measured from the bonding tool **10** when it was charged and grounded. The bonding tool **10** was held in insulative clamp **1802** on a ring stand (not shown), charged to a known voltage with ESD simulator **1810**. The voltage was verified using voltmeter **1804**, and then the bonding tool **10** was grounded. The current moving through the ground wire was measured with current probe **1806** connected to oscilloscope **1808**. Ten measurements were made at each voltage level on the bonding tool **10**. Using the setup of FIG. **18** the bonding tool **10** can be charged and discharged successively. The rise and fall of the current is plotted by the trace on oscilloscope **1808** which allows the discharge time of several successive cycles of discharging to be viewed and measured graphically.

The voltmeter **1804** could be, but is not limited to, a TREK model **341** non-contact voltmeter. The current probe **1806** could be, but is not limited to, a CT-1 current probe. Oscilloscope **1808** could be, but is not limited to, a Tektronics TDS 520A Digital Oscilloscope. The ESD simulator **1810** could be, but is not limited to, a KeyTech MZ-15.

FIG. **19** is a table showing the static decay times measured using the experimental setup of FIG. **18**. The static decay from **1000** volts to **10** volts was also measured on both rods, **#1** and **#2**. The static decay times varied between 0.1 and 0.5 seconds, or more precisely between 0.12 and 0.48 seconds, indicating how quickly the charge dissipate. The decay time is the product of the resistance times the capacitance. Using the data of the tables of FIGS. **17** and **19** an estimate of the capacitance as a function of position associated with the bonding tool **10** can be made, indicating how much charge may build up in bonding tool **10**.

FIG. **20** is a plot comparing the discharge current at various voltages of the ceramic bonding tools to a metal rod. The averages of the current at each voltage level are plotted in FIG. **20**. One of the bonding tools (**#1**) was measured at five different voltages, and the other bonding tool (**#2**) was measured at two voltage levels to verify the discharge currents. The data points representing the two bonding tool tips are marked using squares for one tool tip and triangles for the other. The data points representing the metal rod are marked with diamonds. The resistance associated with this measurement is around 1×10^{5} Ω or more precisely between about 7.5×10^{4} Ω and 2.8×10^{5} Ω. The current represents the discharge rate. Clearly the bonding tools discharge at a slower rate than the metal rod.

While the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the true spirit and scope of the invention. In addition, modifications may be made without departing from the essential teachings of the invention.

What is claimed is:

1. A device comprising:

a tip having a dissipative material for use in wire bonding machines for connecting leads to integrated circuit bonding pads, wherein said dissipative material has a resistance in the range of 5×10^{4} to 10^{12} ohms.

2. The device of claim **1**, wherein the tip has a tube for feeding wire.

3. The device of claim **1**, wherein the tip has grooves.

4. A device comprising:

a tip having a dissipative material for use in wire bonding machines for connecting leads to integrated circuit bonding pads, wherein said dissipative material has a resistance low enough to conduct an essentially constant current and high enough to prevent a current equal to or more than 20 milliamps from discharging to a device being bonded.

5. The device of claim **4**, wherein the resistance is high enough to prevent a current less than or equal to 5 milliamps.

6. The device of claim 4, wherein the resistance is high enough to prevent a current less than or equal to 3 milliamps.

7. The device of claim 4, wherein the resistance is high enough so that the current dissipated from the tip is less than or equal to 2 milliamps.

8. A method of making a dissipative ceramic bonding tool tip having a resistance in the range of 10^5 to 10^{12} ohms, comprising:

sintering fine particles to form said dissipative ceramic bonding tool tip.

9. The method of claim 8, wherein sintering fine particles comprises:

mixing fine particles of a composition appropriate for forming said dissipative material with a solvent, a dispersant, a binder, and a sintering aid to form a mixture;

molding the mixture into at least one wedge;

drying the at least one wedge;

providing a heat-treating atmosphere that facilitates removal of the binder at a low temperature and that controls the valence of the dopant atoms;

heating the at least one wedge in the atmosphere at a temperature appropriate to remove the binder and the dispersant;

heating the at least one wedge to a high enough temperature in the atmosphere to sinter the particles together into a solid structure having low porosity; and

cooling the solid structure.

10. The method of claim 8, wherein the fine particles are heated to a 500–2500 degrees Celsius to remove binders.

11. The method of claim 8, wherein the fine particles are sintered to a 4000 degrees Celsius to remove binders.

12. The method of claim 8, wherein the fine particles are mixed with solvents, dispersants, binders, and sintering aids.

13. The method of claim 8, wherein the fine particles are mixed with a solvent including H_2O.

14. The method of claim 8, wherein the fine particles are mixed with a binder including ceria.

15. The method of claim 8, wherein the fine particles are mixed with a solvent including ceria.

16. The method of claim 8, wherein the dissipative ceramic bonding tool tip has a grain size of less than half a micron.

17. A method of making a dissipative ceramic bonding tool tip having a resistance in the range of 10^5 to 10^{12} ohms, comprising:

hot pressing reactive fine particles to form the dissipative ceramic bonding tool tip.

18. The method of claim 17, wherein the step of hot pressing comprises:

mixing fine particles of a composition appropriate for forming a dissipative material with binders and sintering aids into a mixture;

choosing a hot pressing atmosphere to control a valence of dopant atoms;

pressing the mixture in a mold at a temperature high enough to cause consolidation and binding of the particles into a solid structure having low porosity; and

cooling and removing the solid structure from the mold.

19. The method of claim 17, wherein the fine particles are mixed with binders and sintering aids.

20. The method of claim 17, wherein hot pressing is performed at a temperature that is between 1000 and 2500 degrees Celsius.

21. The method of claim 17, wherein the fine particles are mixed with a solvent including H_2O.

22. The method of claim 17, wherein the fine particles are mixed with a binder including ceria.

23. The method of claim 17, wherein the fine particles are mixed with a solvent including ceria.

24. The method of claim 17, wherein the dissipative ceramic bonding tool tip has a grain size of less than half a micron.

25. A method of making a dissipative ceramic bonding tool tip having a resistance in the range of 10^5 to 10^{12} ohms, comprising:

fusion casting fine particles to form said dissipative ceramic bonding tool tip.

26. The method of claim 25, wherein the fusion casting comprises:

melting metals of a composition appropriate for forming a dissipative material in a non-reactive crucible;

casting the melted metals into an ingot;

rolling the ingot into a rolled ingot;

extruding the rolled ingot into an extruded material;

drawing the extruded material into a drawn material;

pressing the drawn material into a pressed material; and

heating the pressed material.

27. The method of claim 25, wherein the dissipative ceramic bonding tool tip as a grain size of less than half a micron.

28. A method of using an electrically dissipative bonding tool tip, having a resistance in the range of 10^5 to 10^{12} ohms, comprising:

providing the electrically dissipative bonding tool tip;

bonding a material to a device;

allowing an essentially smooth current to dissipate to the device, the current being low enough so as not to damage said device being bonded and high enough to avoid a build up of charge that could discharge to the device being bonded and damage the device being bonded.

29. The method of claim 28, wherein the bonding comprises:

heating the electrically dissipative bonding tool tip using electrical resistive heating; and

using the electrically dissipative bonding tool tip to melt a bonding material.

30. The method of claim 28, wherein the bonding comprises scrubbing the material laterally to cause the material to flow.

31. The method of claim 28, further comprising establishing a potential between the electrically dissipative bonding tool tip and the device being bonded.

32. The method of claim 31, wherein the establishing further comprises grounding leads on the device being bonded.

33. The method of claim 28 further comprising placing the electrically dissipative bonding tool tip in electrical contact with the device being bonded.

34. The method of claim 33 further comprising feeding wire through a tubular channel in the electrically dissipative bonding tool tip prior to placing it in contact with the device being bonded.

35. The method of claim 28 further comprising:

providing an electrical discharge at the electrically dissipative bonding tool tip to melt a bit of wire, and forming the bit of wire into a bonding ball.

36. The method of claim 35 further comprising causing the ball to make intimate contact with the device, thereby initiating dissipation of charge.

37. The method of comprising moving the electrically dissipative ceramic bonding tool tip from the device, with wire being fed as the electrically dissipative bonding tool tip is moved, onto a different point of the device.

38. The device of claim **1**, wherein the range of 5×10^4 *to* 10^{12} Ohms of the resistance is limited to 10^5 to 10^{12} Ohms.

39. The method of claim **8**, wherein the fine particles are mixed with dispersants.

40. The method of claim **8**, wherein the fine particles are mixed with binders.

41. The method of claim **8**, wherein the fine particles are mixed with sintering aids.

42. The method of claim **8**, wherein the fine particles are mixed with solvents.

43. The method of claim **8**, wherein the fine particles are mixed with a binder including magnesia.

44. The method of claim **8**, wherein the fine particles are mixed with a binder including yttria.

45. The method of claim **8**, wherein the fine particles are mixed with a binder including boron.

46. The method of claim **8**, the fine particles are mixed with a binder including a carbon colloidal silica.

47. The method of claim **8**, wherein the fine particles are mixed with a binder including an alumina solvent.

48. The method of claim **8**, wherein the fine particles are mixed with a binder including ethyl silicate.

49. The method of claim **8**, wherein the fine particles are mixed with a binder including a phosphate.

50. The method of claim **8**, wherein the fine particles are mixed with a binder including a rare earth metal oxide.

51. The method of claim **8**, wherein the fine particles are mixed with a binder including yttrium.

52. The method of claim **8**, wherein the fine particles are mixed with a solvent including magnesia.

53. The method of claim **8**, wherein the fine particles are mixed with a solvent including yttria.

54. The method of claim **8**, wherein the fine particles are mixed with a solvent including boron.

55. The method of claim **8**, wherein the fine particles are mixed with a solvent including a carbon colloidal silica.

56. The method of claim **8**, wherein the fine particles are mixed with a solvent including an alumina solvent.

57. The method of claim **8**, wherein the fine particles are mixed with a solvent including ethyl silicate.

58. The method of claim **8**, wherein the fine particles are mixed with a solvent including a phosphate.

59. The method of claim **8**, wherein the fine particles are mixed with a solvent including a rare earth metal oxide.

60. The method of claim **8**, wherein the fine particles are mixed with a solvent including yttrium.

61. The method of claim **17**, wherein the fine particles are mixed with a binder including magnesia.

62. The method of claim **17**, wherein the fine particles are mixed with a binder including yttria.

63. The method of claim **17**, wherein the fine particles are mixed with a binder including boron.

64. The method of claim **17**, wherein the fine particles are mixed with a binder including a carbon colloidal silica.

65. The method of claim **17**, wherein the fine particles are mixed with a binder including alumina solvents.

66. The method of claim **17**, wherein the fine particles are mixed with a binder including ethyl silicate.

67. The method of claim **17**, wherein the fine particles are mixed with a binder including a phosphate.

68. The method of claim **17**, wherein the fine particles are mixed with a binder including a rare earth metal oxide.

69. The method of claim **17**, wherein the fine particles are mixed with a binder including yttrium.

70. The method of claim **17**, wherein the fine particles are mixed with a solvent including magnesia.

71. The method of claim **17**, wherein the fine particles are mixed with a solvent including yttria.

72. The method of claim **17**, wherein the fine particles are mixed with a solvent including boron.

73. The method of claim **17**, wherein the fine particles are mixed with a solvent including a carbon colloidal silica.

74. The method of claim **17**, wherein the fine particles are mixed with a solvent including alumina solvents.

75. The method of claim **17**, wherein the fine particles are mixed with a solvent including ethyl silicate.

76. The method of claim **17**, wherein the fine particles are mixed with a solvent including a phosphate.

77. The method of claim **17**, wherein the fine particles are mixed with a solvent including a rare earth metal oxide.

78. The method of claim **17**, wherein the fine particles are mixed with a solvent including yttrium.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,651,864 B2
DATED : November 25, 2003
INVENTOR(S) : Reiber et al.

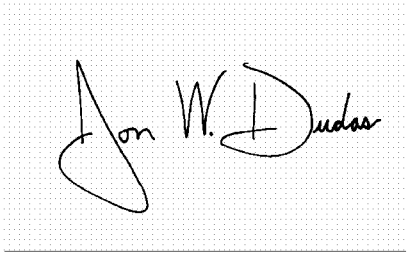
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,
Line 54, "5×10^{4}" should read -- 5×10^{5} --

Column 15,
Line 5, "5×10^{4to}" should read -- $5 \times 10^{5}$to --

Signed and Sealed this

Fourth Day of May, 2004



JON W. DUDAS
Acting Director of the United States Patent and Trademark Office

Disclaimer

6,651,864—Steven Frederick Reiber, 4409 Vivien Way, Rocklin, CA (US); Mary Louise Reiber, 867 Mossy Ridge, Linclon, CA (US). DISSIPATIVE CERAMIC BONDING TOOL TIP. Patent Dated Nov. 24, 2003. Disclaimer filed December 7, 2009 by Co-Inventor and Co-Owner, Mary Louise Reiber.

Hereby enters this disclaimer to claims 8, 9, 10-27, 39-78 of said patent.

(*Official Gazette, June 15, 2010*)

EXHIBIT F

US007124927B2

(12) **United States Patent**
Reiber

(10) **Patent No.: US 7,124,927 B2**
(45) **Date of Patent: *Oct. 24, 2006**

(54) **FLIP CHIP BONDING TOOL AND BALL PLACEMENT CAPILLARY**

(76) Inventor: **Steven F. Reiber**, 4409 Vivien Way, Rocklin, CA (US) 95677

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **11/107,308**

(22) Filed: **Apr. 15, 2005**

(65) **Prior Publication Data**

US 2005/0242155 A1 Nov. 3, 2005

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/942,311, filed on Sep. 15, 2004, and a continuation-in-part of application No. 10/943,151, filed on Sep. 15, 2004, which is a continuation-in-part of application No. 10/650,169, filed on Aug. 27, 2003, now Pat. No. 6,935,548, which is a continuation of application No. 10/036,579, filed on Dec. 31, 2001, now Pat. No. 6,651,864, and a continuation-in-part of application No. 09/514,454, filed on Feb. 25, 2000, now Pat. No. 6,354,479.

(60) Provisional application No. 60/503,267, filed on Sep. 15, 2003, provisional application No. 60/288,203, filed on May 1, 2001, provisional application No. 60/121,694, filed on Feb. 25, 1999.

(51) **Int. Cl.**
B23K 37/00 (2006.01)

(52) **U.S. Cl.** **228/4.5**; 228/6.1; 228/180.5

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2,892,924	A	6/1959	Wood
3,538,205	A	11/1970	Gates, Jr. et al.
3,563,443	A	2/1971	Perdotti et al.
3,660,050	A	5/1972	Iler et al.
3,917,148	A	11/1975	Runyon
3,938,722	A	2/1976	Kelly et al.
3,971,499	A	7/1976	Goodrich, Jr. et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0435423	7/1991

(Continued)

OTHER PUBLICATIONS

Stan Weitz, "Trends in ESD Test Methods," Materials Testing Section of the ETS Testing Laboratory, Electrotech Systems, 1998, pp. 1-7.

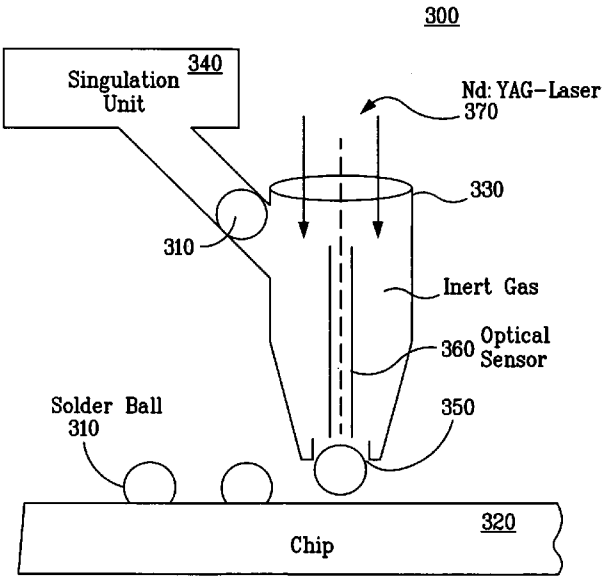
(Continued)

Primary Examiner—Lynne R. Edmondson
(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

A flip chip bonding tool and ball placement capillary system comprising a dissipative material with a resistance low enough to prevent a discharge of a charge to a device being bonded and high enough to avoid current flow to the device being bonded is disclosed.

17 Claims, 6 Drawing Sheets



U.S. PATENT DOCUMENTS

3,986,255	A	10/1976	Mandal	
3,986,653	A	10/1976	Gilding	
4,020,543	A	5/1977	Pennings	
4,050,762	A	9/1977	Hines et al.	
4,157,932	A	6/1979	Hirata	
4,171,477	A	10/1979	Funari	
4,182,947	A	1/1980	Brower	
4,315,128	A	2/1982	Matcovich et al.	
4,331,048	A	5/1982	Dworak et al.	
4,387,283	A	6/1983	Peterson et al.	
4,390,771	A	6/1983	Kurtz et al.	
4,405,074	A	9/1983	Levintov et al.	
4,502,983	A	3/1985	Omori et al.	
4,513,190	A	4/1985	Ellett et al.	
4,554,033	A	11/1985	Dery et al.	
4,555,052	A	11/1985	Kurtz et al.	
4,686,465	A	8/1987	Kruger	
4,691,854	A	9/1987	Haefling et al.	
4,705,204	A	11/1987	Hirota et al.	
4,772,498	A	9/1988	Bertin et al.	
4,821,944	A	4/1989	Tsumura	
4,842,662	A	6/1989	Jacobi	
4,897,710	A	1/1990	Suzuki et al.	
4,899,921	A	2/1990	Bendat et al.	
4,909,427	A	3/1990	Plaisted et al.	
4,974,767	A	12/1990	Alfaro et al.	
4,998,002	A	3/1991	Okikawa et al.	
5,123,935	A	6/1992	Kanamaru et al.	
5,144,747	A	9/1992	Eichelberger	
5,178,742	A	1/1993	Lemke et al.	
5,180,093	A	1/1993	Stansbury et al.	
5,214,259	A	5/1993	Terakado et al.	
5,217,154	A	6/1993	Elwood et al.	
5,250,843	A	10/1993	Eichelberger	
5,280,979	A	1/1994	Poli et al.	
5,290,507	A	3/1994	Runkle	
5,341,979	A	8/1994	Gupta	
5,347,086	A	9/1994	Potter et al.	
5,367,956	A	11/1994	Fogle, Jr.	
5,421,503	A	6/1995	Perlberg et al.	
5,427,301	A	6/1995	Pham et al.	
5,437,405	A	8/1995	Asanasavest	
5,463,197	A	10/1995	Miyazaki	
5,491,605	A	2/1996	Hughbanks et al.	
5,527,441	A	6/1996	Offer	
5,544,804	A	8/1996	Test et al.	
5,558,270	A	9/1996	Nachon et al.	
5,601,740	A	2/1997	Eldridge et al.	
5,616,257	A	4/1997	Harada et al.	
5,649,355	A	7/1997	Offer	
5,651,901	A	7/1997	Mohri et al.	
5,662,261	A	9/1997	Fogal	
5,669,545	A	9/1997	Pham et al.	
5,676,856	A	10/1997	Haji et al.	
5,797,388	A	8/1998	Nakamura et al.	
5,816,472	A	10/1998	Linn	
5,827,470	A	10/1998	Chatterjee et al.	
5,871,141	A	2/1999	Hadar et al.	
5,931,368	A	8/1999	Hadar et al.	
5,984,162	A	11/1999	Hortaleza et al.	
6,030,472	A	2/2000	Hajaligol et al.	
6,041,995	A	3/2000	Takahashi et al.	
6,053,777	A	4/2000	Boyle	
6,073,827	A	6/2000	Razon et al.	
6,219,911	B1	4/2001	Estes et al.	
6,325,269	B1	12/2001	Suzuki et al.	
6,337,522	B1	1/2002	Kang et al.	
6,354,479	B1 *	3/2002	Reiber et al.	228/4.5
6,646,355	B1	11/2003	Kang et al.	
6,651,864	B1 *	11/2003	Reiber et al.	228/4.5
6,759,642	B1	7/2004	Hoshino	
6,905,350	B1	6/2005	Wallash et al.	
6,935,548	B1	8/2005	Reiber	
2005/0109814	A1	5/2005	Reiber	
2005/0109817	A1	5/2005	Reiber	

FOREIGN PATENT DOCUMENTS

GB	2287897	10/1995
JP	54037114	3/1979
JP	63164228	7/1988
JP	63-239959	10/1988
JP	02-67741	3/1990
JP	04-149065	5/1992
JP	04-149605	5/1992
JP	06-45389	2/1994
JP	09-162223	6/1997
JP	11-186315	7/1999
JP	11-251357	9/1999
JP	2001-201515	7/2001
JP	2001-351934	12/2001

OTHER PUBLICATIONS

Instrument FAQs, Drivers, Libraries and Examples, Keithley Instrument Model 6517/6517A, Keithley Instruments, Inc., 1999, pp. 1-2.
Keithley Instruments Model 6517A Electrometer/High Resistance Meter, Keithley Instruments, Inc., pp. 1-9, date unknown.
"Low-Current/High-Resistance Meters," Keithley Instruments Model 6517A, Keithley Instruments, Inc. pp. 112-115, date unknown.
Keytech 200 XV-2 ESD Simulator, Kandus Equipment, p. 1, date unknown.
Newburg, Carl E., "Test Report", Anza Technology, Incorporated Static Dissipative Ceramic Rods . . . , Report 190:2000-92, River's Edge Technical Service, Nov. 29, 2000, pp. 1-5.
Huntsman, James et al., "Test Methods for Static Control Products," Electrical Overstress/Electrostatic Discharge Sym., Sep. 21, 1982, pp. 94-109, vl.4, IIT Rsrch Inst.
Mayer, Michael et al., "Active Test Chips for In Situ Wire Bonding Process Characterization," Semicon Singapore 2001, May 2001.
National Semiconductor, "Semiconductor Packaging Assembly Technology," Aug. 1999.
Suman et al., "Wire Bond Temperature Sensor," IMAPS International Symposium on Microelectronics, Baltimore, MD, Oct. 9-11, 2001.
Klossner, et al., "An Integrated Approach to Solving sub-45um Wire Bond Process Challenges," SEMICON Singapore, 2001.
Wilson, et al. "Holographic Interferometry Applied to Motion Studies of Ultrasonic Bonders," IEEE Transactions on Sonics and Ultrasonics, vol. 19, No. 4, Oct. 1972.
Olney et al., "A New ESD Model: The Charged Strip Model," EOS/ESD Symposium Proceedings, 2002.
Andres et al., "Bumping Wafers via Ultrasonically Enhanced Stencil Printing," SEMICON West 2003.
Jittinorasett, Suwanna, "UBM Formation on Single Die/Dice for Flip Chip Applications," Aug. 1999.
Zakel, et al., "Laser Solder Attach for Optoelectronic Packages," Proceedings of the PhoPack Conference (Stanford University, California), Jul. 2002.
PacTech Packaging Technologies, "Laser Solder Ball Jet System," www.pactech-usa.com, date unknown.

* cited by examiner

FIG. 1

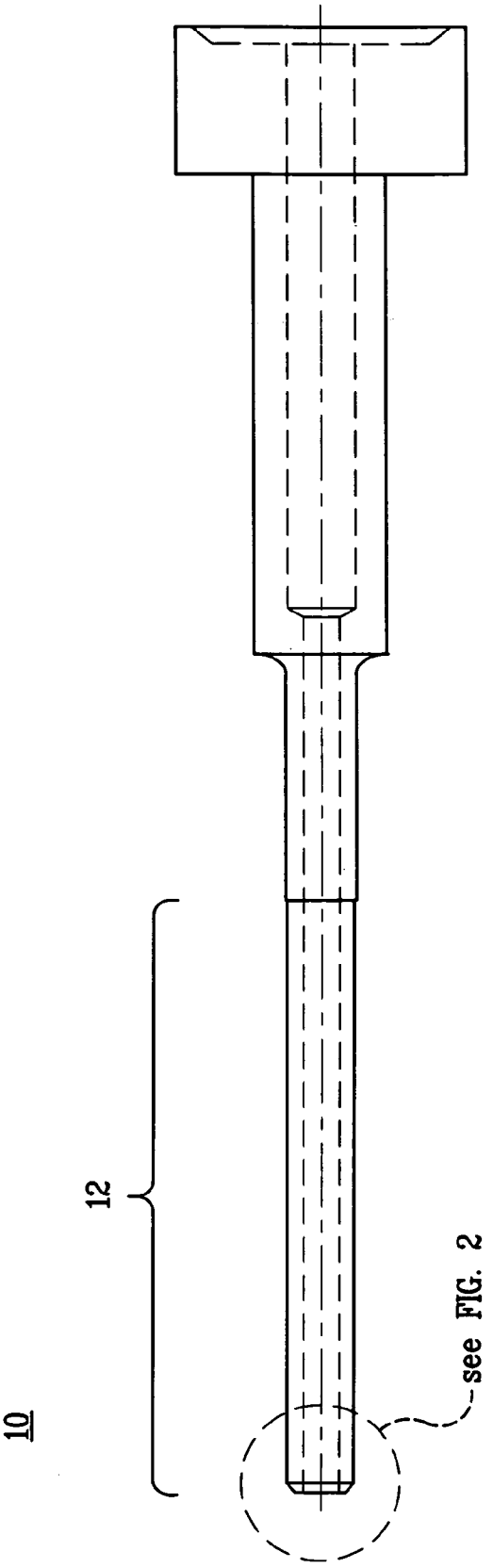


FIG. 2

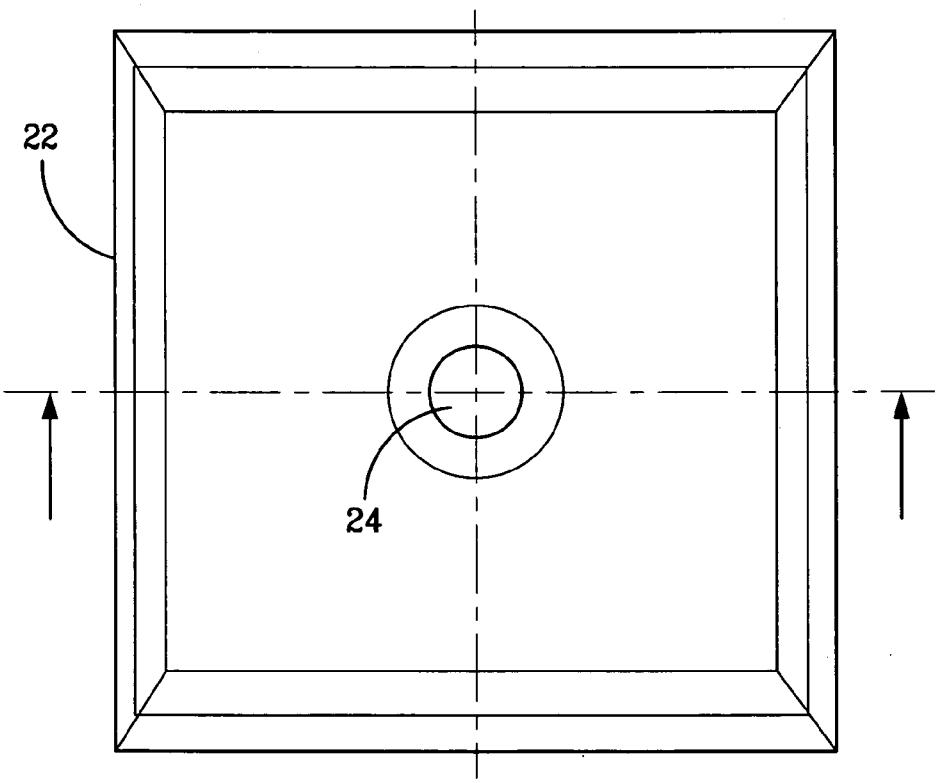
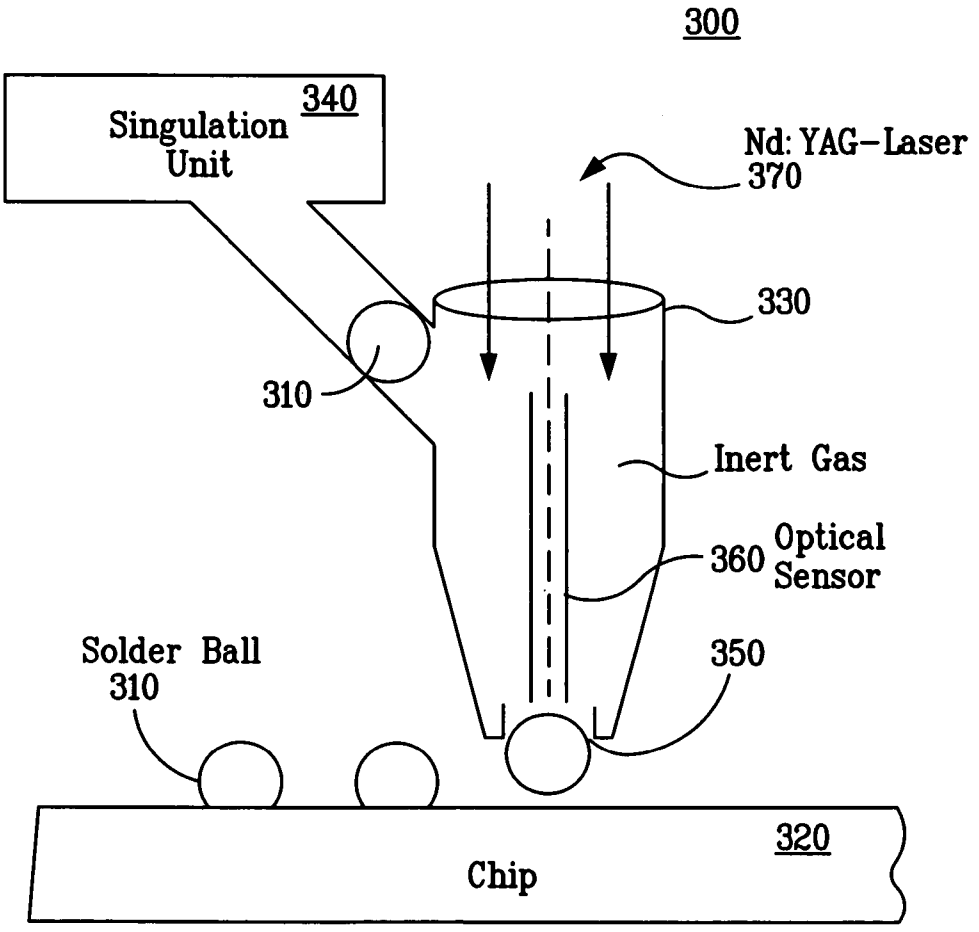


FIG. 3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340
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370
330
310
Inert Gas
360
Optical Sensor
Solder Ball
310
350
320
Chip

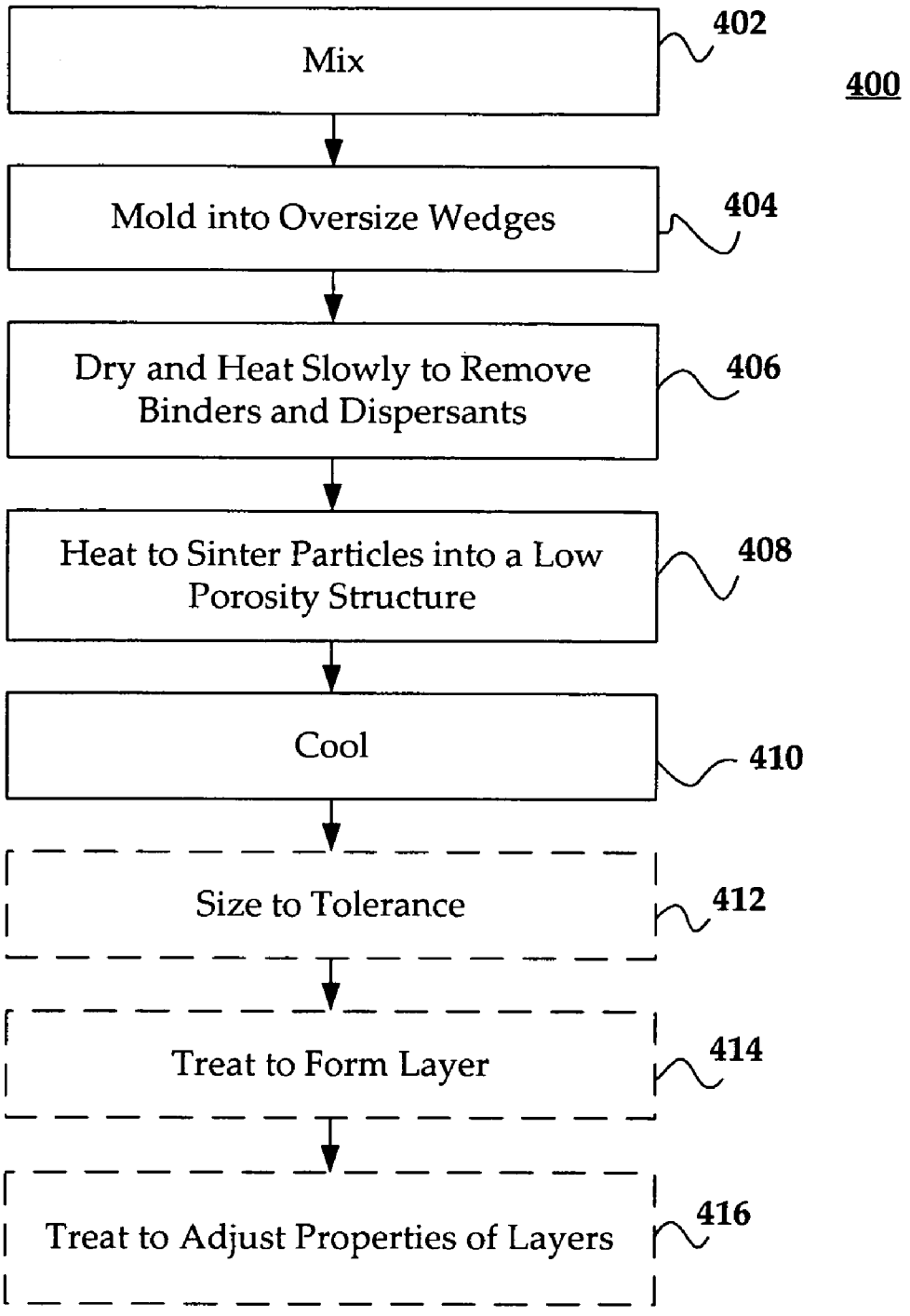
Mix
402
400
Mold into Oversize Wedges
404
Dry and Heat Slowly to Remove Binders and Dispersants
406
Heat to Sinter Particles into a Low Porosity Structure
408
Cool
410
Size to Tolerance
412
Treat to Form Layer
414
Treat to Adjust Properties of Layers
416

FIGURE 4

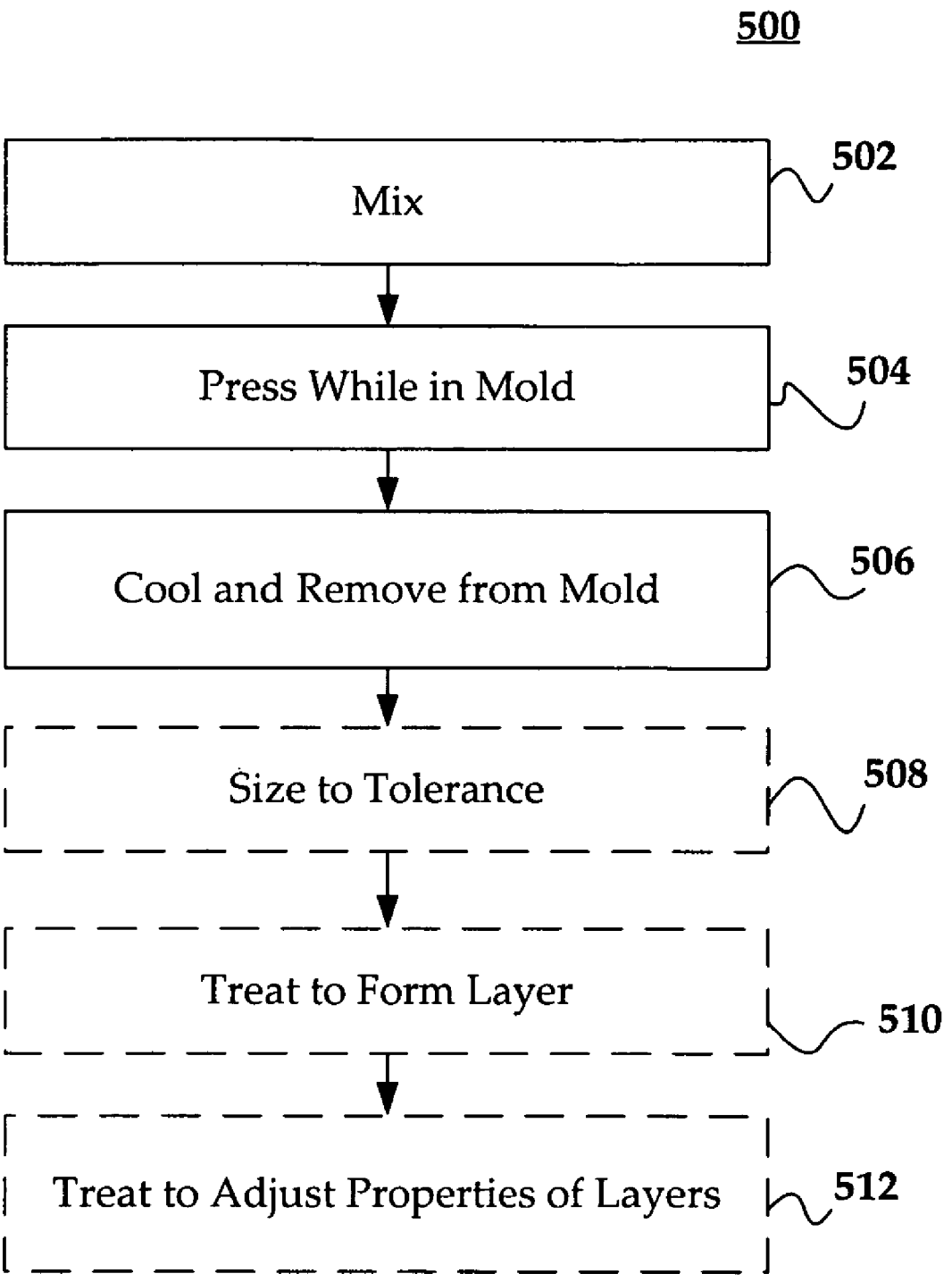
500
Mix
502
Press While in Mold
504
Cool and Remove from Mold
506
Size to Tolerance
508
Treat to Form Layer
510
Treat to Adjust Properties of Layers
512

FIGURE 5

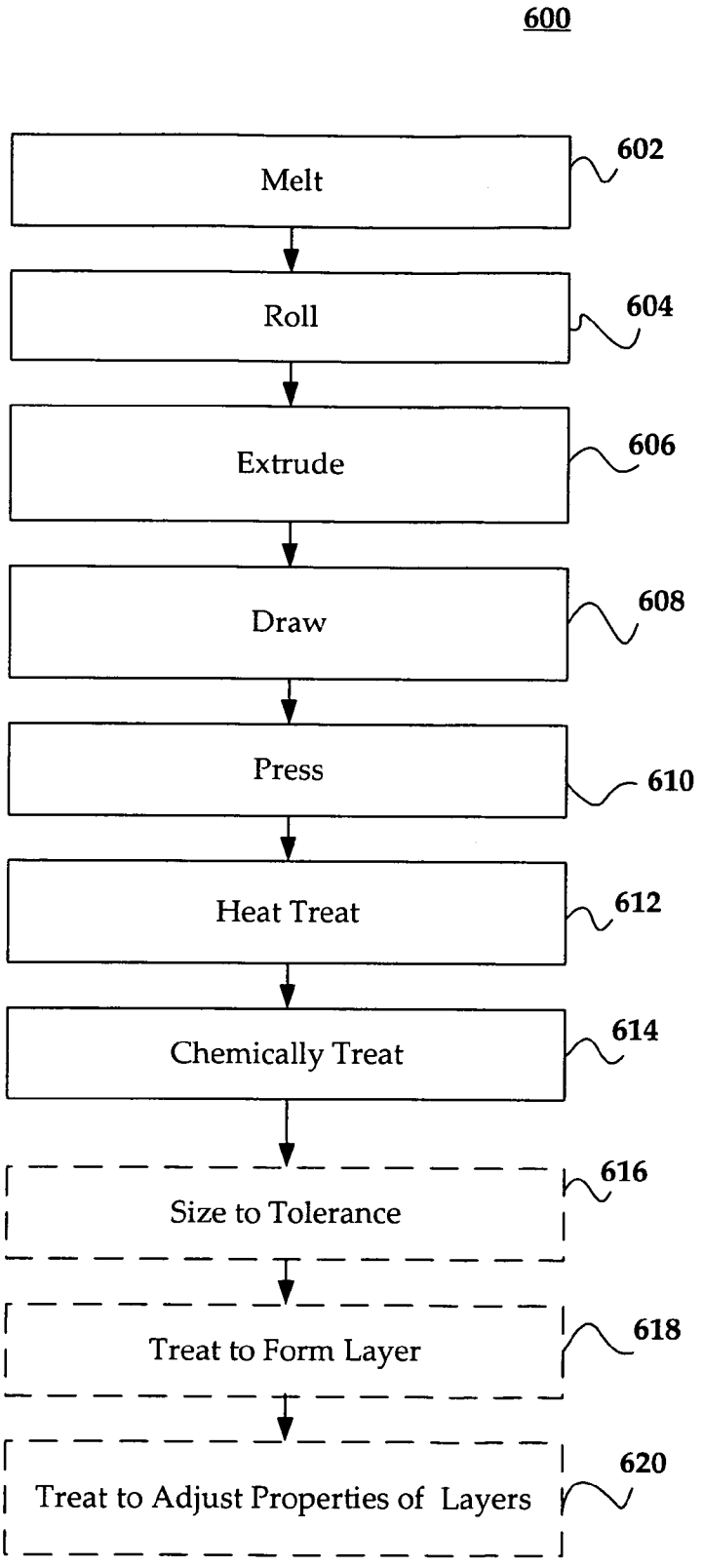
600
Melt
602
Roll
604
Extrude
606
Draw
608
Press
610
Heat Treat
612
Chemically Treat
614
Size to Tolerance
616
Treat to Form Layer
618
Treat to Adjust Properties of Layers
620

FIGURE 6

FLIP CHIP BONDING TOOL AND BALL PLACEMENT CAPILLARY

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part and claims the priority benefit of U.S. patent application Ser. No. 10/942,311 filed Sep. 15, 2004 entitled "Flip Chip Bonding Tool Tip"; this application is also a continuation-in-part and claims the priority benefit of U.S. patent application Ser. No. 10/943,151 filed Sep. 15, 2004 and entitled "Bonding Tool with Resistance"; U.S. patent application Ser. No. 10/942,311 and U.S. patent application Ser. No. 10/943,151 are a continuation-in-part and claim the priority benefit of U.S. patent application Ser. No. 10/650,169 filed Aug. 27, 2003 entitled "Dissipative Ceramic Bonding Tool Tip" now U.S. Pat. No. 6,935,548 which is a continuation of U.S. patent application Ser. No. 10/036,579 filed Dec. 31, 2001, now U.S. Pat. No. 6,651,864, entitled "Dissipative Ceramic Bonding Tool Tip" which claims the priority benefit of U.S. provisional patent application No. 60/288,203 filed May 1, 2001 and is also a continuation-in-part of U.S. patent application Ser. No. 09/514,454 filed Feb. 25, 2000, now U.S. Pat. No. 6,354,479 and entitled "Dissipative Ceramic Bonding Tool Tip" which claims the priority benefit of provisional patent application No. 60/121,694 filed Feb. 25, 1999; U.S. patent application Ser. No. 10/942,311 and U.S. patent application Ser. No. 10/943,151 also claim the priority benefit of U.S. provisional patent application No. 60/503,267 filed Sep. 15, 2003 and entitled "Bonding Tool." The contents of all of these applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to flip chip bonding tool tips. More particularly, the present invention relates to dissipative and insulative ceramic flip chip bonding tools and capillaries for ball placement for bonding electrical connections.

2. Description of the Prior Art

Integrated circuits have different methods of attachment to a lead frame. One method is an ultrasonic wire bond whereby individual leads are connected to individual bond pads on the integrated circuit with wire. Ball bonding—a type of wire bonding—involves a process whereby a metal sphere is melted on a length of wire. Wedge bonding is similar to ball bonding except that the process generally utilizes aluminum wire; no 'ball' is formed and the process can be performed at room temperature. Gold ball bonding, on the other hand, typically occurs at temperatures in excess of 150° Celsius. Gold ball bonding is most often used in high volume applications as it is a faster process whereas aluminum wire bonding is used in situations when packages or a printed circuit board cannot be heated. Gold ball bonding, too, has pitch limits of approximately 60 micron. Aluminum wedge bonding can be performed as pitches finer than 60 micron.

Wire bonding techniques use "face-up" chips with a wire connection to each pad. Bump or "flip chip" microelectronic assembly, on the other hand, is a direct electrical connection of face-down—"flipped"—electronic components onto substrates, circuit boards, or carriers by means of conductive bumps on a chip bond pad.

Flip chip components are predominantly semiconductor devices. Components such as passive filters, detector arrays, and MEMs devices are also used in flip chip form. Flip chip is sometimes referred to as Direct Chip Attach (DCA) as the chip is attached directly to the substrate, board, or carrier by the conductive bumps. Automotive electronics, electronic watches, and a growing percentage of cellular phones, pagers, and high speed microprocessors are assembled with flip chips.

The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of a die to the substrate. The bump also provides a spacer, preventing electrical contact between the chip and substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

Stud bumps are placed on die bond pads through a modification of the "ball bonding" process used in conventional wire bonding or by the use of a ball placement machine where small balls are forced down a small capillary onto a pad and then laser reflowed. In the ball bonding referenced above, a tip of a bond wire is melted to form a sphere. A wire bonding tool presses this sphere against an aluminum bond pad, applying mechanical force, heat, and ultrasonic energy to create a metallic connection.

For stud bumping, the first ball bond is made as described but the wire is then broken close above the ball. The resulting ball, or "stud bump" remaining on the bond pad provides a permanent and reliable connection through the aluminum oxide to the underlying metal. After placing the stud bumps on a chip, the stud bumps may be flattened—"coined"—by mechanical pressure to provide a flatter top surface and more uniform bump heights while pressing any remaining wire tail into the ball. Each bump may be coined by a tool immediately after forming or all bumps on the die may be simultaneously coined by pressure against a flat surface in a separate operation following bumping.

Bonding tool tips must be sufficiently hard to prevent deformation under pressure, and mechanically durable so that many bonds can be made before replacement. Typical flip chip bonding tips available on the market today are made of a tungsten carbide or titanium carbide. These conducting tools are very hard compounds that have been successfully used on commercial machines as these compounds provide a reasonably long life in use as a flip chip bonding tool and ball placement capillary.

The problem, however, is that an electrostatic discharge (ESD) from the bonding tool or transient currents from the machine can damage the very circuit the tool is bonding. Flip chip bonding and ball placement capillaries tools must be electrically designed to produce a reliable electrical contact, yet prevent electrostatic discharge damage to the part being bonded. Certain prior art devices have a one-or-more volt emission when the tip makes bonding contact. This could present a problem as a one-volt static discharge can generate a 20 milliamp current to flow, which, in certain instances, can cause the integrated circuit to fail due to this unwanted current.

SUMMARY OF THE INVENTION

Dissipative flip chip bonding tools and ball placement capillaries for bonding electrical connections to bonding pads on electrical devices are disclosed. In accordance with the principles of the present invention, to avoid damaging delicate electronic devices by any electrostatic discharge, a flip chip bonding tool tip conducts electricity at a rate

sufficient to prevent charge buildup but not at so high a rate as to overload the device being bonded. In other words, it is desirable for the bonding tip to discharge slowly to avoid a sudden surge of current that can damage the part being bonded.

In one embodiment, a resistance in the tip assembly itself may range from 10^2 to 10^{19} ohms. The tools in such an embodiment also have specific mechanical properties to function satisfactorily. High stiffness and high abrasion resistance requirements may result in the utilization of ceramics (e.g., electrical non-conductors) or metals like tungsten carbide (e.g., electrical conductors).

In an embodiment of the present invention, flip chip bonding tool and ball placement capillaries with the desired electrical conduction can be made with three different configurations. Tools can be made from a uniform extrinsic semi-conducting material on an insulator. Tools can also be made by forming a thin layer of a highly doped semi-conductor on an insulator on a core. Finally, tools can be made by forming a lightly doped semi-conductor layer on a conducting core.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a flip chip bonding tool tip;

FIG. **2** is an enlarged, cross-sectional view of the flip chip bonding tool of FIG. **1**;

FIG. **3** is an exemplary ball placement capillary;

FIG. **4** is an exemplary method for manufacturing a dissipative flip chip bonding tool through the use of mixing, molding, and sintering reactive powders;

FIG. **5** is an exemplary method for manufacturing a dissipative flip chip bonding tool tip through the use of hot pressing reactive powders; and

FIG. **6** is an exemplary method for manufacturing a dissipative flip chip bonding tool tip through fusion casting.

DETAILED DESCRIPTION OF AN EMBODIMENT

FIG. **1** illustrates an embodiment of a flip chip bonding tool **10**. In one embodiment, the bonding tool is about two inches (30 to 80 mm) long and about 0.124 inch (3.0 mm) in diameter. An exemplary bonding tool tip **12**, itself, is from 3 to 100 mils (0.8 to 2.54 mm) long. Running a length of the tool, but not viewable in FIG. **1**, is a tube hole, which will accommodate a vacuum to, for example, pick up a tool.

FIG. **2** is an enlarged, cross-sectional view of the flip chip bonding tool **10** of FIG. **1**. Only that portion of the bonding tool **10** shown within the dotted circle in FIG. **1** is shown in FIG. **2**. As shown, tool tip **22** has a tube hole **24**, which may run an entire length of the bonding tool **10**.

In accordance with principles of the present invention, to avoid damaging delicate electronic devices by an electrostatic discharge, a bonding tool tip conducts electricity at a rate sufficient to prevent charge buildup but not at so high a rate as to overload a device being bonded. It has been determined that the tool should have electrical conduction greater than one ten-billionth of a mho (i.e., $>1\times10^{-19}$ reciprocal ohms), but the tool's electrical conductivity should be less than one one-hundred thousandth of a mho (i.e., $<1\times10^{-2}$ reciprocal ohms). Further, the tool's resistance should be low enough that the material is not an insulator and does not allow for any dissipation of charge, but high enough that the material is not a conductor and allows a current flow. In one embodiment of the present invention, a resistance in the tip assembly ranges from 10^2 to 10^{19} ohms. Five (5) milliamps of current will, generally, damage present-day magnetic recording heads. Preferably, for today's magnetic recording heads, no more than 2 to 3 milliamps of current should be allowed to pass through the tip to a head.

The tools should also have specific mechanical properties to function satisfactorily. Due to high stiffness and high abrasion resistance requirements, ceramics (e.g., electrical non-conductors) or metals, such as tungsten carbide (e.g., electrical conductor) have emerged as preferred materials. In one embodiment, the tip comprises a Rockwell hardness of about 55 or above. More preferably, in an embodiment, the Rockwell hardness is about 85 or above. In an embodiment of the present invention, the tip lasts for approximately fifteen thousand bondings.

In the present invention, flip chip bonding tool and ball placement capillaries with the desired electrical conduction can be made with three different configurations.

First, the tools may be made from a uniform extrinsic semi-conducting material or insulator, which has dopant atoms in appropriate concentrations and valence states to produce sufficient mobile charge carrier densities—unbound electrons or holes. Sufficient mobile charge carrier densities result in electrical conduction in a desired range. Silicon carbide uniformly doped with boron is an example of such a uniform extrinsic semi-conducting material. Silicon nitride is a further example of a uniform non-conducting material. Polycrystalline silicon carbide uniformly doped with boron is yet another example of such a uniform extrinsic semi-conducting material.

Second, the tools may be made by forming a thin layer of a highly doped semi-conductor on an insulating core. In this instance, the core provides mechanical stiffness, and the semi-conductor surface layer provides abrasion resistance and a charge carrier path from tip to a mount. This resistance and carrier path will permit dissipation of electrostatic charge at an acceptable rate. A diamond tip wedge that is ion implanted with boron is an example of such a thin layered tool.

Third, the tools may be made by forming a lightly doped semi-conductor layer on a conducting core. The conducting core provides mechanical stiffness and the semi-conductor layer provides abrasion resistance and a charge carrier path from tip to conducting core, which is electrically connected to the mount. The doping level is chosen to produce conductivity through the layer which will permit dissipation of electrostatic charge or stop all transient current at an acceptable rate. A cobalt-bonded tungsten carbide coated with titanium nitride carbide is an example of such a lightly doped tool.

FIG. **3** is an exemplary ball placement capillary system **300**. The ball placement capillary system **300** sequentially solders a ball to a variety of different microelectronic substrates. An embodiment of the invention may singulate, position, and reflow solder balls **310** on a chip **320** with a diameter between 100 μm and 760 μm.

Capillary system **300** comprises a bondhead **330** coupled to a singulation unit **340**, a capillary **350** for ball positioning, an optional optical sensor **360**, and a laser system **370**. Some embodiments of the capillary system **300** may further comprise a pressure sensor (not shown) and various vacuum capabilities (not shown), for example, a vacuum ejector. Bondhead **330** is further coupled to a solder ball loading station (not shown). The bondhead **330** is the mechanical apparatus generally responsible for physical delivery of solder balls to various locales on a chip or substrate.

Bondheads **330** are usually configured to deliver a particular size of solder ball typically ranging in size from 100 μm to 760 μm. The bondhead **330** is generally configured, in exemplary embodiments, to travel on an X-, Y-, and Z-axis. The exemplary bondhead **330** is typically controlled by a general computing device coupled to a keyboard or joystick to allow for directional control by a user or operator of the capillary system **300**.

Singulation unit **340** operates to queue and subsequently deliver individual solder balls **310** to the capillary **350** for physical delivery and placement on the chip **320**. Singulation unit **340** may operate in conjunction solder ball loading station (not shown). Capillary **350** serves to provide a physical channel for ejection of a solder ball onto chip **320** or other substrate surface. Optical sensor **360** operates to optimize placement of the solder ball **310** on the chip **320**.

Laser system **370** utilizes a pointing laser as a target light for precise location of the reflowed solder ball **310** on the chip **320** and may operate in conjunction with optical sensor **360** to further optimize precise solder ball **310** placement. One embodiment of laser system **370** comprises a solid state, pulsed neodymium:yttrium-aluminum-garnet (Nd:YAG) laser. In a Nd:YAG laser, a cylindrical rod of yttrium-aluminum-garnet doped with neodymium is the active medium. Such a laser may comprise a wavelength of approximately 1064 nm, laser energy of 4J and a pulse frequency and width of up to 10 Hz and 1 ms to 20 ms, respectively. The laser system **370** also is operative to melt the solder ball **310** thereby wetting the chip **320** to provide a sufficient interface.

Dissipative tools can be manufactured through the use of mixing, molding, and sintering reactive powders as shown in the flowchart of FIG. **4**; the use of hot pressing reactive powders as shown in the flowchart of FIG. **5**; and through fusion casting as shown in the flowchart of FIG. **6**.

Through the use of mixing, molding, and sintering reactive powders (flowchart **400** of FIG. **4**), fine particles of a desired composition are mixed **402** with organic and inorganic solvents, dispersants, binders, and sintering aids and then molded **404** into oversized wedges. The wedges are carefully dried and slowly heated to a temperature between 500–2500 degrees Celsius **406** to remove the binders and dispersants. The wedges are then heated to a high enough temperature so that individual particles sinter together **408** into a solid structure with low porosity. The heat-treating atmosphere is chosen to facilitate the removal of the binder at a low temperature and to control valence of dopant atoms at a higher temperature and while cooling. After cooling **410**, the wedges may be optionally machined, or otherwise sized, **412** to achieve required tolerances.

The wedges may then be optionally treated **414** to produce a desired surface layer by ion implementation, vapor deposition, chemical vapor deposition, physical deposition, electroplating deposition, neutron bombardment, or combinations of the above. The pieces may optionally be subsequently heat treated **416** in a controlled atmosphere (e.g., 2000 to 2500 degrees Celsius for 3 to 5 minutes) to produce the desired layer properties through diffusion, re-crystallization, dopant activation, or valence changes of metallic ions.

Through the use of hot pressing reactive powders (flowchart **500** of FIG. **5**), fine particles of a desired composition are mixed **502** with binders and sintering aids and then pressed **504** in a mold at a high enough temperature (e.g., 1000 to 4000 degrees Celsius) to cause consolidation and binding of the individual particles into a solid structure with low porosity. The hot pressing atmosphere is chosen to control valence of dopant atoms. After cooling and removal **506** from the hot press mold, the pieces may optionally be machined, or otherwise sized, **508** to achieve required tolerances. The pieces may then be optionally treated **510** to produce a desired surface layer by ion implantation, vapor deposition, chemical vapor deposition, physical deposition, electo-plating deposition, neutron bombardment, or combinations of the above. The pieces may optionally be subsequently heat treated **512** in a controlled atmosphere to produce desired layer properties through diffusion, re-crystallization, dopant activation, or valence changes of metallic ions.

Through fusion casting (flowchart **600** of FIG. **6**), metals of a desired composition are melted **602** in a non-reactive crucible then cast into an ingot. The ingot is then rolled **604**, extruded **606**, drawn **608**, pressed **610**, heat-treated **612** in a suitable atmosphere, and chemically treated **614**. The pieces may then optionally be machined, or otherwise sized, **616** to achieve required tolerances. The metallic pieces may also be optionally heat-treated to produce a desired surface layer **618** by vapor deposition, chemical vapor deposition, physical deposition, electroplating deposition, or combinations of the above. The pieces may optionally be subsequently heat-treated in a controlled atmosphere to produce desired layer properties **620** through diffusion, re-crystallization, dopant activation, or valence changes of metallic ions.

In an embodiment of the invention, the layer used in the bonding process could be a formula for dissipated or insulative ceramic comprising alumina (aluminum oxide Al_2O_3) and zirconia (zirconium oxide ZrO_2) and other elements or a silicon carbide with boron. This mixture is both somewhat electrically conductive and mechanically durable. The tip of a bonding tool can be coated with this material or the tip can be made completely out of this material. The shape of the tip may be wedge- or circular-shaped.

The bonding tip of the present invention may be used for any number of different types of bonding including ultrasonic and thermal flip chip bonding.

While the present invention has been described with reference to an exemplary embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the true spirit and scope of the present invention. In addition, modifications may be made without departing from the essential teachings of the present invention.

What is claimed is:

1. A flip chip bonding tool and ball placement capillary system for connecting leads on integrated circuit bonding pads, comprising a dissipative material having a resistance low enough to prevent a discharge of a charge to a device being bonded and high enough to stop current flow large enough to damage the device being bonded.

2. The system of claim **1**, wherein the dissipative material comprises a resistance in the range of 10^2 to 10^{19} ohms.

3. The system of claim **1**, wherein the bonding tool comprises a vacuum tube.

4. The system of claim **1**, wherein the dissipative material comprises a semi-conducting material.

5. The system of claim **4**, wherein the semi-conducting material comprises dopant atoms in appropriate concentration and valence states to produce resistance.

6. The system of claim **4**, wherein the semi-conductive material comprises silicon carbide.

7. The system of claim **6**, wherein the silicon carbide is uniformly doped with boron.

8. The system of claim **1**, wherein the dissipative material comprises a doped semi-conductor formed on an insulating core.

9. The system of claim **8**, wherein the insulating core comprises a diamond.

10. The system of claim **8**, wherein the doped semi-conductor further comprises an outer surface of the insulating core implanted with boron.

11. The system of claim **1**, wherein the dissipative material comprises a doped semi-conductor formed on a conducting core.

12. The system of claim **11**, wherein the conducting core comprises a cobalt-bonded tungsten carbide.

13. The system of claim **11**, wherein the conducting core is coated with titanium nitride carbide.

14. An ESD-preventive device comprising:

a flip chip bonding tool and ball placement capillary, comprising a dissipative material and configured to come in contact with a device being bonded, wherein a current produced by static charge generated during bonding is allowed to flow; wherein the dissipative material has a resistance low enough to prevent a discharge of charge to the device being bonded and high enough to stop all current flow to the device being bonded.

15. The ESD-preventive device of claim **14**, wherein the current flow allowed is no more than 3 milliamps.

16. A method of utilizing a flip chip bonding tool and ball placement capillary in a microelectronic assembly, comprising:

providing a bonding machine capable of being equipped with a flip chip bonding tool and ball placement capillary having a tip comprised of a dissipative material, the dissipative material having a resistance low enough to prevent a discharge of a charge to a device being bonded and high enough to stop all current flow to the device being bonded;

equipping the bonding machine with the flip chip bonding tool and ball placement capillary;

providing a bonding material that is thermally and electrically conductive;

melting the bonding material so that the bonding material becomes substantially spherical in shape; and

electrically connecting at least one component to a substrate by means of pressing the substantially spherical-shaped bonding material, the substantially spherical bonding material being pressed to form a conductive bump.

17. The method of claim **16**, further comprising coining the conductive bump.

* * * * *

Disclaimer

7,124,927—Steven F. Reiber, Rocklin, CA (US). FLIP CHIP BONDING TOOL AND BALL PLACEMENT CAPILLARY. Patent dated December 7, 2009 by Inventor and Owner, Steven F. Reiber.

Hereby enters this disclaimer to claims 5-13 of said patent.

(Official Gazette, April 13, 2010)