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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ANZA TECHNOLOGY, INC., a California corporation,

Plaintiff,

v.

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., a California corporation, and TOSHIBA MEMORY AMERICA, INC., a California corporation.

Defendants.

Case No. 5:17-cv-07289-LHK

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Anza Technology, Inc., by and through its undersigned counsel complains and alleges against Defendants Toshiba America Electronic Components, Inc. ("TAEC") and Toshiba Memory America, Inc. ("TMA") as follows:

NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the laws of the United States relating to patents, 35 U.S.C. § 101 *et seq*. The statutory provisions at issue in the civil action include, without limitation, 35 U.S.C. §§ 271 and 281. Plaintiff Anza Technology, Inc. seeks monetary damages for patent infringement.

JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a). This court further has subject matter jurisdiction over this case for patent infringement pursuant to the patent laws of the United States of America, 35 U.S.C. § 101, *et seq*.

3. Venue properly lies within the Northern District of California. Venue is properly vested with the Northern District of California pursuant to the provisions of 28 U.S.C. §§ 1391(b), (c), and 1400(b). Defendant TAEC previously sought transfer of this action from the United States District Court for the Eastern District of California. Defendant TAEC did not contest transfer of this action to the Northern District of California.

4. Defendant TAEC is a California corporation. TAEC—by its own admission—maintains its principal place of business at 5231 California Avenue, Irvine, California. TAEC—by its own admission—employs 248 people, 131 of which are located in San Jose, California. TAEC—by its own admission—employs individuals that may be able to provide corporate testimony regarding TAEC's sales and marketing of its past and future products in the United States. Those persons, according to TAEC, are located in or near San Jose, California. San Jose, California, is located within the jurisdictional limits of the Northern District of California. San Jose, California, is located within the San Jose division of the Northern District of California.

5. Defendant TMA is a California corporation. As of October 1, 2017—according to declarations made by TAEC—TAEC's business related to at least flash memory products was "spun off" to TMA. TMA—according to the California Secretary of State—maintains an office

at 2610 Orchard Parkway, San Jose, California. San Jose, California, is located within the jurisdictional limits of the Northern District of California. San Jose, California, is located within the San Jose division of the Northern District of California.

6. This Court has personal jurisdiction over TAEC because TAEC is incorporated under the laws of the State of California. This Court has personal jurisdiction over TAEC because TAEC's business is conducted mainly in San Jose and Irvine, California. This Court has personal jurisdiction over TAEC because TAEC has transacted continuous and systematic business within the State of California. Such continuous and systematic business includes but is not limited to certain of the infringing activities complained of herein. Those infringing activities have caused harm to Plaintiff Anza Technology, Inc. in the State of California.

7. This Court has personal jurisdiction over TMA because TMA is incorporated under the laws of the State of California. This Court has personal jurisdiction over TMA because TMA's business is believed to be conducted in and around San Jose, California. This Court has personal jurisdiction over TMA because TMA has transacted continuous and systematic business within the State of California. Such continuous and systematic business includes but is not limited to certain of the infringing activities complained of herein. Those infringing activities have caused harm to Plaintiff Anza Technology, Inc. in the State of California.

PARTIES

8. Plaintiff Anza Technology, Inc. ("Anza") is a corporation organized and existing under the laws of the State of California. Plaintiff Anza maintains an office and principal place of business at 4121 Citrus Avenue, Suite 4, Rocklin, California. Anza is a designer, manufacturer, and seller of products directed to the manufacture and assembly of electronics including the bonding of electrostatic-sensitive devices.

9. TAEC is a California corporation. TAEC maintains its principal place of business at 5231 California Avenue, Irvine, California. TAEC maintains operations in San Jose, California. TAEC is the North America electronic components business of Toshiba Corporation. TAEC offers high-end microcontrollers, application specific integrated circuits, and application specific standard products for automotive, multimedia, industrial, telecoms and networking applications. TAEC also offers power semiconductor solutions and storage products including hard disk drives.

10. TMA is a California corporation. As of October 1, 2017, TMA operates *inter alia* the solid state drive and flash memory product business previously controlled by TAEC. TMA maintains an office at 2610 Orchard Parkway, San Jose, California. TMA is the United States-based subsidiary of Toshiba Memory Corporation. Toshiba Memory Corporation is part of the electronic devices business domain of Toshiba Corporation.

BACKGROUND

11. JEDEC was formerly known as the Joint Electron Device Engineering Council. JEDEC is now known as the JEDEC Solid State Technology Association. JEDEC develops open standards for the microelectronics industry. JEDEC's mission is to create standards to meet the diverse technical and developmental needs of the industry. JEDEC brings manufacturers and suppliers together to participate in various committees and subcommittees. JEDEC's collaborative efforts ensure product interoperability thereby benefitting the industry by decreasing time-to-market and reducing product development costs. The creation of standards

by way of collaboration through committees and subcommittees is sometimes referred to as 'Standard Setting.' JEDEC is sometimes referred to as a Standards Setting Organization ("SSO").

12. Among the standards developed by JEDEC are those for addressing the phenomenon known as electrostatic discharge (ESD). ESD is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. ESD can cause a range of harmful effects of importance in the electronics industry, specifically with regard to integrated circuits. Integrated circuits like memory and semiconductor devices can suffer permanent damage when subjected to ESD as discussed herein.

13. A packaged integrated circuit includes one or more semiconductor dies. Semiconductor dies are generally mounted on a substrate and encapsulated in a mold as illustrated below in FIGURE 1. The substrate is the solid substance onto which another object—the semiconductor die—is etched, deposited, or otherwise fabricated. Mold compounds are the plastics used to encapsulate electronic packages such as a semiconductor die. A die coupled to a substrate and encapsulated in a mold is illustrated in FIGURE 1.

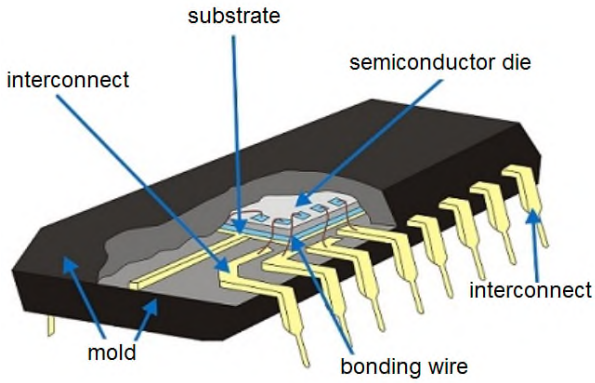


FIGURE 1

The packaged integrated circuit illustrated in FIGURE 1 includes interconnects (e.g., leads or pads). Interconnects are electrically coupled to the corresponding inputs and outputs of the semiconductor die to allow signals to pass between the die and other electronic componentry.

Coupling of interconnects to the semiconductor die is referred to as bonding. In FIGURE 1, the die is bonded to the interconnects using bonding wire.

14. Bonding also encompasses coupling interconnects to a printed circuit board (PCB). A PCB mechanically supports and electrically connects the die package to other electrical components that might be found on the PCB using conductive tracks, pads, or other features. A Toshiba Memory America single-cell (SLC) NAND flash memory device (model number TC58NVG0S3HTA00) is shown below as FIGURE 2. The flash memory device shown in FIGURE 2 includes a digital integrated circuit encompassed in a mold (*i.e.*, a package) in which the semiconductor die is internally bonded to a series of interconnects. Those interconnects are then externally bonded to a PCB, which is electronically coupled to other componentry. As a result of the internal bonding of the die within the package and the subsequent bonding of the package to the PCB, the device of FIGURE 2 is able to perform storage functions.

FIGURE 2

15. Interconnects are not limited to pins or wires. Other bonding techniques may be used. For example, a ball grid array (BGA) assembly technique may be implemented in the bonding process. A BGA assembly technique involves an array of conductive balls arranged on the face of the chip rather than the pins located along the sides as shown in FIGURE 1. An illustration of a ball grid array is shown in FIGURE 3 below.

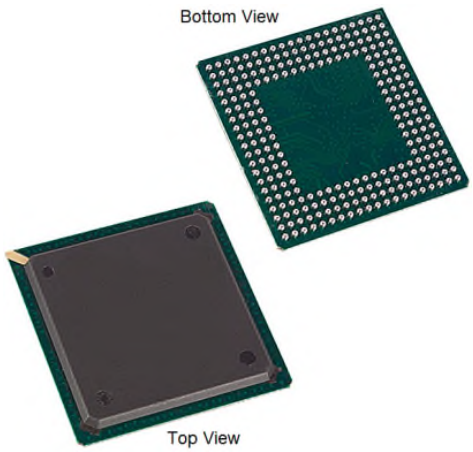


FIGURE 3

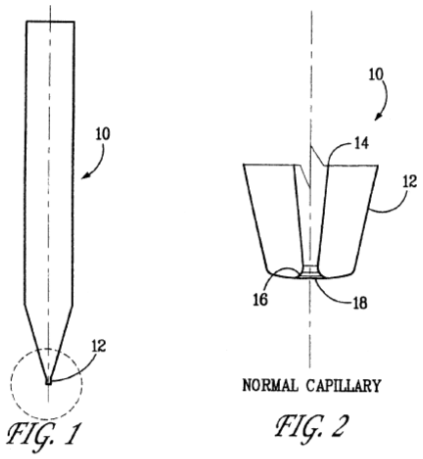
A ball grid array may be utilized both inside and outside a semiconductor package.

16. Bonding an integrated circuit or other computing component to a substrate or a PCB involves the use of one or more bonding tools. The integrated circuit comes in contact with such a tool, which places or connects the package on the substrate or the PCB as is appropriate. These tools may aid in effectuating the bonding of the circuit or component by way of wires, leads, bumps, or pads. Subject to a particular bonding technique, heat (thermal energy) may be applied to a bonding medium or material such as a metallic solder ball. This thermal energy may be applied by way of a bonding tool tip or an oven. Application of heat causes the medium to melt and electrically 'bond' the integrated circuit or module to the surface of the substrate or PCB.

17. One bonding technique is wire bonding. Wire bonding is the method of making interconnections with the integrated circuit and other components using, for example, gold or copper wire and the application of ultra-sonics or heat. The wire is attached at both ends using a combination of downward pressure, ultrasonic energy, and/or heat to make a weld.

18. Reproduced below are FIGURES 1 and 2 of U.S. patent number 6,354,479. U.S. patent number 6,354,479 is one of the patents-in-suit in the present action. FIGURE 1 of the '479 Patent "illustrates a typical capillary bonding tool 10. Such bonding tools are usually about one-half inch (12-13 mm) long and about one-sixteenth inch (1.6 mm) in diameter. The bonding tool tip 12 itself is usually from 3 to 10 mils (0.08 to 0.25 mm) long." '479:3:3-7. FIGURE 2 of the '479 Patent—to continue the example and for the purposes of context—is "a highly enlarged,

cross-sectional view of the capillary bonding tool 10 as shown and described in FIG. 1 [of the '479 Patent]." '479:3:10-11. "[T]he chamfer surface 16 is provided to allow for smoother looping of the [bonding] wire as the bonding tool 10 is moved from the bonding pad on an integrated circuit to the bonding pad (not shown) on a lead frame of an integrated circuit assembly." '479:3:20-24.



(FIGURE 1 and 2 of the '479 Patent)

19. Another type of bonding is known as 'flip chip' bonding. Like wire bonding, flip chip bonding is a method for interconnecting an integrated circuit with other electrical components. Unlike wire bonding, interconnects are established utilizing solder bumps deposited on a substrate or package. Flip chip microelectronic assembly is the direct electrical connection of face-down (or flipped) integrated circuit chips onto substrates or semiconductor packages onto PCBs using conductive bumps. The bumped die or package is flipped and placed face down so that the bumps directly connect to the substrate or PCB. This technique is in contrast to wire bonding where the die or package is mounted upright and wires establish interconnects.

20. Naturally occurring electrostatic charges of varying degrees can build up when bonding tools come in contact with the die, package, or bonding medium. Electrostatic charges can even build up when a die or package is removed from storage or a transport vessel and placed on the wafer or PCB before any bonding takes place. Without strict safeguards,

electrostatic charges can be built up from almost any contact and through almost any activity. If enough static is generated, discharge can occur and damage to an electronic component may result. The threat of ESD is present in microelectronics assembly utilizing both wire and flip chip bonding techniques. There is a need to dissipate and/or block such a static build up as to avoid damage to the electrical componentry being bonded.

21. Electronics manufacturers establish electrostatic protective areas free of static using measures to prevent (dis)charging. This includes the use of bonding tools, apparatus, and techniques that obviate a buildup of ESD or otherwise dissipate the same. JEDEC has taken a leadership role in developing standards for ESD since the early 1980s. This includes developing standards for device handling related to ESD. JEDEC is accredited by the American National Standards Institute (ANSI). ANSI oversees the creation, promulgation, and use of norms and guidelines for various industries. ANSI is actively engaged in accreditation to assess the competence of organizations determining conformance to standards. The Electrostatic Discharge Association (ESDA), too, is a professional association dedicated to advancing the theory and practice of ESD avoidance. The foregoing groups are cumulatively referred to as "ESD Standards Organizations" and develop, collectively or on their own, "ESD Standards."

22. For example, ESDA and JEDEC have—since October 2008—had a joint memorandum of understanding concerning the development of ESD Standards and publications in the field of ESD. The ESDA and JEDEC entered into such an agreement in the best interest of their organizations, their membership, and the electronics industry. Notwithstanding the foregoing joint relationship, JEDEC has—since December 1999—through at least JEDEC Standard No. 625-A ("Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices") indicated that JEDEC members should "incorporate these minimal requirements into their ESD control program to provide a consistent protection level for their products." JEDEC Standard No. 625-A is attached hereto as Exhibit A.

23. JEDEC Standard No. 625-A, for example, "establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic

devices that are susceptible to damage or degradation from electrostatic discharge (ESD)." JEDEC Standard No. 625-A continues in noting that "[t]he passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part." Table 1 of Section 6.1 of JEDEC Standard No. 625-A, for example, requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

24. Like JEDEC Standard No. 625-A, subsequent and ancillary ESD Standards implemented by various ESD Standards Organizations require, in part, the use of tools made of dissipative materials having approximately the same resistance values in connection with handling integrated circuits that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent the discharge of a charge to an ESD sensitive device such as flash memory, including the Accused Products as further discussed herein. These ranges are also high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package.

25. For example, JEDEC Standard 625-B ("Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices"), which is attached hereto as Exhibit B, "replaces JESD625-A and JEDEC Standard No. 42." In a manner similar to its predecessor JEDEC 625-A, the JEDEC 625-B Standard was "prepared to standardize the requirements for a comprehensive Electrostatic Discharge (ESD) control program for handling ESD-Sensitive (ESDS) devices." JEDEC 625-B "establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD)." JEDEC 625-B states that "[t]he device types for which these requirements are applicable include, but are not limited to, ESD-sensitive discrete and integrated circuit semiconductors, multi-chip modules, optoelectronic devices, and thin film passive devices." JEDEC 625-B, too, incorporates a series of other ESD Standards, including but not limited to ANSI/ESD S20.20.

26. JEDEC 625-B discusses the use of static dissipative material as "[a] material having a surface resistance between 1 x 10^4 ohms and 1 x 10^{11} ohms." JEDEC 625-B also discusses the applicable use of the standard to include both semiconductor manufacture and semiconductor processing and testing. JEDEC 625-B characterizes manufacture as "from wafer electrical probe through shipment of finished devices," JEDEC 625-B characterizes processing and testing as "from receipt through shipment of finished devices." JEDEC 625-B also incorporates a series of other ESD Standards as set forth in Section 2 of the standard and entitled "Technical References."

27. JEDEC has also published a series of other ESD-related standards including but not limited to:

* Joint JEDEC / ESDA Human Body Model (JS-001-2017);
* Joint JEDEC / ESDA Charged Device Model (JS-002-2014);
* Understanding Electrical Overstress (JEP174);
* Discontinuing Use of the Machine Model for Device ESD Qualification (JEP172A);
* HBM Target Levels (JEP155);
* CDM Target Levels (JEP157);
* System Level Part 1 Overview (JEP161); and
* System Level Part 2 Design Methods (JEP162).

28. Each of the foregoing standards seek to avoid inadvertent electrostatic static discharge by implementing manufacturing and quality controls that include the use of bonding tools with resistance high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package. This includes implementing ESD controls related to resisting current flow in ranges between 10^5 and 10^{12} ohms. This further includes maintaining current flows low enough to prevent a discharge.

29. Toshiba Memory Corporation is a member of JEDEC. Toshiba Memory Corporation and its affiliated entities, including but not limited to TAEC and TMA, are believed

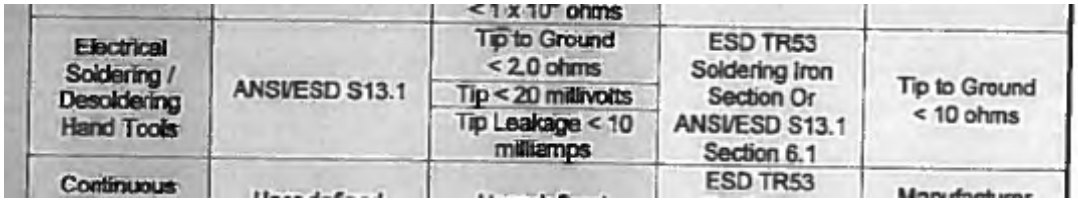
to comply with the ESD Standards published by JEDEC as well as other ESD Standards Organizations. Toshiba Memory Corporation and employees of its affiliated entities, including but not limited to TAEC and TMA, are active in JEDEC activities. For example, Douglas Wong—a Senior Engineer in the Memory Business Unit at TAEC—is involved with JEDEC. Douglas Wong has given presentations on behalf of TAEC in conjunction with JEDEC. Such presentations include but are not limited to discussing the development of JEDEC standards and contributing to the same. Douglas Wong is currently believed to be a Senior Engineer in the Memory Business Unit with TMA.

30. Toshiba Memory Corporation and its affiliated entities, including but not limited to TAEC and TMA, are also believed to comply with certain ESD standards published by ANSI, including but not limited to ANSI ESD 20.20, which is attached hereto as Exhibit C. ANSI ESD 20.20 seeks to provide "technical requirements for establishing, implementing and maintaining an ESD Control Program." Such a program includes utilization of proper "Grounding / Equipotential Bonding Systems" that "shall be used to ensure that ESDS items, personnel and any other conductors that come into contracts with ESDS items (e.g., mobile equipment) are at the same electrical potential." ANSI ESD 20.20 includes Table 3, which sets forth various ESD Control Items, which further includes work surfaces:

ESD Control Item	Product Qualification[b]		Compliance Verification	
	Test Method	Required Limit(s)[c]	Test Method	Required Limit(s)
Worksurface[9,10] (Qualification can be done by either Test Method)	ANSI/ESD S4.1	Point to Point $< 1 \times 10^9$ ohms	ESD TR53 Worksurface Section	Point to Ground $< 1 \times 10^9$ ohms
		Point to Groundable Point $< 1 \times 10^9$ ohms		
	ANSI/ESD STM4.2	< 200 volts		

Table 3 of ANSI ESD 20.20

and specifically tools used at those work surfaces:



		< 1 x 10⁹ ohms		
Electrical Soldering / Desoldering Hand Tools	ANSI/ESD S13.1	Tip to Ground < 2.0 ohms Tip < 20 millivolts Tip Leakage < 10 milliamps	ESD TR53 Soldering Iron Section Or ANSI/ESD S13.1 Section 6.1	Tip to Ground < 10 ohms
Continuous			ESD TR53	

Table 3 of ANSI ESD 20.20 (continued)

31. ANSI requires the use of "dissipative materials" and tools made of such dissipative materials. These materials, and tools made from such materials, should have approximately the same resistance values in connection with handling integrated circuits that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent the discharge of a charge to an ESD sensitive device such as a memory module, including the Accused Products as further discussed herein. These ranges are also high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package. Compliance with the dissipative materials dictated by ANSI includes implementing ESD controls related to resisting current flow in ranges between 10^5 and 10^{12} ohms.

ACCUSED PRODUCTS

32. TAEC's business includes the sale and marketing of products manufactured and assembled outside of the United States. The products manufactured and assembled outside of the United States are imported in the United States for sale and marketing. These products include, prior to October 1, 2017, flash memory products. As of October 1, 2017, the sale and marketing of flash memory products in the United States is believed to have been "spun off" to TMA. The aforementioned flash memory products include, but are not limited to, NAND Flash Memory (the "Accused Products").

33. An example of NAND Flash Memory includes manufacturer part number TC58BYG2S0HBAI6. This example of NAND Flash Memory is a non-volatile integrated circuit that encompasses electrically erasable programmable read-only memory (EEPROM). This particular example of NAND Flash Memory is manufactured utilizing surface mount technology. This particular example of NAND Flash Memory is believed to be manufactured in accordance with JEDEC standards for managing ESD. Certain JEDEC standards incorporate by reference other ESD Standards, including but not limited to ANSI. Publically available information related to NAND Flash Memory, manufacturer part number TC58BYG2S0HBAI6 is illustrated below as a part of FIGURE 4:

Product Overview	
Digi-Key Part Number	TC58BYG2S0HBAI6-ND
Quantity Available	201 Can ship immediately
Manufacturer	Toshiba Memory America, Inc.
Manufacturer Part Number	TC58BYG2S0HBAI6
Description	IC EEPROM 4GBIT 25NS 67VFBGA
Lead Free Status / RoHS Status	Lead free / RoHS Compliant
Moisture Sensitivity Level (MSL)	3 (168 Hours)
Detailed Description	FLASH - NAND (SLC) Memory IC 4Gb (512M x 8) Parallel 25ns 67-VFBGA (6.5x8)

FIGURE 4 (Continued Below)

Product Attributes		Select All
Categories	Integrated Circuits (ICs) Memory	
Manufacturer	Toshiba Memory America, Inc.	
Series	Benand™	
Packaging	Tray	
Part Status	Active	
Memory Type	Non-Volatile	
Memory Format	FLASH	
Technology	FLASH - NAND (SLC)	
Memory Size	4Gb (512M x 8)	
Write Cycle Time - Word, Page	25ns	
Access Time	25ns	
Memory Interface	Parallel	
Voltage - Supply	1.7 V ~ 1.95 V	
Operating Temperature	-40°C ~ 85°C (TA)	
Mounting Type	Surface Mount	
Package / Case	67-VFBGA	
Supplier Device Package	67-VFBGA (6.5x8)	

FIGURE 4 (Continued from Above)

34. This particular example of NAND Flash Memory is believed to have been sold and marketed by TAEC from at least July 2013 up to October 1, 2017. This particular example of NAND Flash Memory is believed to be sold and marketed by TMA since October 1, 2017.

35. An illustration of this particular example of NAND Flash Memory is reproduced below as FIGURE 5.

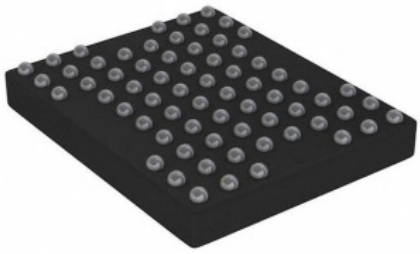


FIGURE 5

A data sheet for this particular example of NAND Flash Memory is attached hereto as Exhibit D. As can be seen from the above illustration and data sheet attached hereto as Exhibit D, this particular example of NAND Flash Memory is manufactured using a BGA manufacturing technique.

36. TAEC did import, sell, and market and TMA continues to import, sell, and market the Accused Products, including NAND Flash Memory, including but not limited to manufacturer part number TC58BYG2S0HBAI6, in compliance with ESD Standards including those promulgated by JEDEC, ANSI, and other ESD Standards Organizations. By implementing these and other ESD Standards during the manufacturing process, TAEC was able to import, market, and sell and TMA is able to continue importing, marketing, and selling products that avoid inadvertent electrostatic static discharge during bonding. This avoidance occurs through implementing manufacturing and quality controls that involve the use of tools with resistance high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package. This includes implementing ESD controls related to resisting current flow in ranges between 10^5 and 10^{12} ohms. This further includes maintaining current flows low enough to prevent a discharge.

37. TAEC and/or TMA may have imported, sold, and marketed or may continue to import, sell, and market additional products, including but not limited to other NAND Flash Memory products, that similarly adopt and implement ESD Standards and quality controls in their manufacturing processes prior to import (like those described above) to avoid inadvertent static discharge that might otherwise damage and electronic component. TAEC and/or TMA may have effectuated such import of Accused Products and additional products implementing ESD Standards in conjunction with certain Toshiba manufacturing facilities or Toshiba authorized manufacturing facilities in Japan or otherwise outside the United States.

THE PATENTS-IN-SUIT

38. On March 12, 2002, the United States Patent and Trademark Office ("USPTO") duly and legally issued U.S. patent number 6,354,479 entitled 'Dissipative Ceramic Bonding Tip,' (the "'479 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '479 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '479 Patent is attached hereto as Exhibit E.

39. On November 25, 2003, the USPTO duly and legally issued U.S. patent number 6,651,864 entitled 'Dissipative Ceramic Bonding Tool Tip,' (the "'864 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '864 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '864 Patent is attached hereto as Exhibit F.

40. The foregoing patents are collectively referred to as the "Patents-in-Suit" and are incorporated into this First Amended Complaint as if fully set forth herein.

41. Defendants TAEC and TMA are successors in interest of an entity formerly known as Toshiba American Information Systems, Inc. of Irvine, California. Toshiba American Information Systems, Inc. of Irvine, California, was previously involved in an investigation before the United States International Trade Commission. That investigation was captioned *In the Matter of Certain Hard Disks Drives, Components Thereof, and Products Containing the Same* (Inv. No. 337-TA-616). The complaint for Investigation number 337-TA-616 was filed on September 10, 2007. Investigation number 337-TA-616 commenced on October 15, 2007. Investigation number 337-TA-616 involved both of the Patents-in-Suit. TAEC and TMA have, therefore, been aware of the claims of the Patents-in-Suit by virtue of their predecessor-in-interest since at least October 15, 2007.

COUNT ONE

INFRINGEMENT OF THE '479 PATENT BY DEFENDANTS

42. Plaintiff re-alleges each of the foregoing paragraphs 1-41 as if fully set forth herein.

43. Defendants infringe (at least) claim 39 of the '479 Patent under 35 U.S.C. § 271(g). Claim 39 of the '479 Patent recites as follows:

> 39. The method of claim 37, wherein said dissipative material has a high enough stiffness to resist bending when hot and has a high enough abrasiveness to function for at least two uses.

44. Claim 37 of the '479 Patent—from which claim 39 depends—recites as follows:

> 37. A method of using a bonding tip, comprising bonding a device using a bonding tip made with a dissipative material that has a resistance low enough to prevent a discharge of charge to said device and high enough to avoid current flow large enough to damage said device.

45. Section 271(g) of Title 35 allows for a claim of infringement whenever a party—without authority—imports into the United States or offers to sell, sells, or uses within the United States a product that is made by a process patented in the United States if said infringement occurs during the term of said patent. The '479 Patent—and claim 39 thereof—is currently in force. Anza has not granted authority to TAEC or TMA to import into the United States any product—including the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6)—covered by claim 39 of the '479 Patent.

46. TAEC and TMA have admitted that the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) are manufactured outside of the United States. TAEC and TMA admit that their involvement with the Accused Products (specifically including but not limited to

NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) is the sale and marketing of the same. TAEC and TMA have not alleged that they undertake any change to the design or manufacture of the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) upon its arrival in the United States or prior thereto.

47. Plaintiff Anza is not aware of any material change to the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) upon its entry or prior to said entry into the United States. Anza therefore alleges that NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6 and that has been sold and marketed in the United States by TAEC and that continues to be marketed and sold in the United States by TMA has not been significantly altered or subjected to any real difference from the time of manufacture using Anza's patented methodologies to the time of import and subsequent marketing and sale in the United States. Anza further contends that it is not aware of any commercially viable non-infringing processes that might have resulted in the manufacture of the Accused Products that are imported into the United States for later marketing and sale

48. The Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) are sold as individual components and therefore cannot be said to be trivial and nonessential products in that they are, in fact, the product being sold and marketed.

49. Further, and with respect to claim 37, Defendant TAEC admits that the Accused Products that it sells and markets include electronic componentry bonded to a substrate. Defendant TMA has, since October 1, 2017, taken on the sale and marketing of these Accused Products that include electronic componentry that are bonded to a substrate. The Accused

Products are manufactured and assembled—including the bonding of componentry to a substrate—outside of the United States. TAEC further admitted that these bonding processes include, at least, wire bonding as described above.

50. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, TAEC has imported (or has caused to be imported) and TMA does now import (or does cause to be imported) the Accused Product, which is manufactured in accordance and compliance with JEDEC standards as confirmed below in FIGURE 6, which comes from publically available literature concerning, at the least, manufacturer part number TC58BYG2S0HBAI6, which is believed to be representative of other types of NAND Flash Memory and Accused Product:

> Tray usually refers to a JEDEC standard matrix tray measuring 12.7x5.35 inches and either 0.25 or 0.40 inches tall. Trays are usually constructed from plastic, but aluminum is permissible. JEDEC trays contain slots to allow air to pass vertically and are rated for at least 140°C to allow drying of parts in industrial ovens. Trays are stackable and feature a chamfered corner indicating the orientation of pin one of the parts. Trays are packaged according to the ESD (ElectroStatic Discharge) and MSL (Moisture Sensitivity Level) protection requirements determined by the manufacturer.

FIGURE 6

51. Defendants TAEC and TMA are also affiliated with members of certain ESD Standard Organizations. Defendants TAEC and TMA further employ individuals—including senior engineers—that are involved with and promote ESD Standard Organizations and ESD Standards promulgated by these organizations.

52. In light of the foregoing, it is believed that the foregoing bonding processes are undertaken in accordance with one or more ESD Standards, including but not limited to JEDEC 625-A and/or JEDEC 625-B. The aforementioned bonding processes are further believed to be undertaken in accordance with one or more ESD Standards, including but not limited to ANSI

ESD 20.20. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require the use of dissipative tools to minimize electrostatic discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 require a resistance low enough to prevent a discharge to a device being bonded. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 require a resistance high enough to avoid current flow large enough to damages a device being bonded.

53. With respect to claim 39—which depends from claim 37 and that Anza alleges is infringed under 35 U.S.C. § 271(g)—TAEC has sold and marketed and TMA does now sell and market an imported product that is manufactured using JEDEC and ANSI compliant standards and—further—that utilizes dissipative bonding tools that can be used more than once. It would defy commercial manufacturing principles for any manufacturer to replace a bonding tool with each and every bond. For example—referring to the die package in FIGURES 1 and 2—multiple bond points are illustrated. As such, and accepting for the sake of argument TAEC's contention that the Accused Products are wire bonded, a bonding tool would be required to facilitate each of those wire bonds if the tool were not used more than once.

54. As such, TAEC and TMA infringe—prior to October 1, 2017 and after October 1, 2017, respectively—claim 39 of the '479 Patent under 35 U.S.C. § 271(g). TAEC and TMA—by virtue of their predecessor in interest—have both been aware of the '479 Patent since at least October 15, 2007 as a result of International Trade Commission investigation number 337-TA-616. Notwithstanding their respective knowledge of the '479 Patent since at least October 15, 2007, TAEC and TMA have both elected to engage in activity that constitutes an infringement of the '479 Patent under 35 U.S.C. § 271(g). Notwithstanding their respective knowledge of the '479 Patent since at least October 15, 2007, TAEC and TMA have both elected not to undertake any efforts to avoid engaging in activity that constitutes an infringement of the '479 Patent under

35 U.S.C. § 271(g). Anza alleges that such activity (or conscious lack thereof) is willful in light of knowledge of the '479 Patent, especially since said knowledge is a result of the predecessor in interest to TAEC and TMA having been engaged in litigation involving the '479 Patent. Anza therefore alleges that TAEC and TMA's infringement of the '479 Patent was and remains willful.

COUNT TWO

INFRINGEMENT OF THE '864 PATENT BY DEFENDANTS

55. Plaintiff re-alleges paragraphs 1-41 and 42-55 as if fully set forth herein.

56. Defendants infringe (at least) claim 28 of the '864 Patent, which recites:

> A method of using an electrically dissipative bonding tool tip, having a resistance in the range of 10^5 to 10^{12} ohms, comprising:
> providing the electrically dissipative bonding tool tip;
> bonding a material to a device;
> allowing an essentially smooth current to dissipate to the device, the current being low enough so as not to damage said device being bonded and high enough to avoid a build up of charge that could discharge to the device being bonded and damage the device being bonded.

57. Claim 28 recites an electrically dissipative bonding tool tip, specifically the use thereof. Claim 28 would, therefore, be infringed (in part) by placing a bonding tip in a device positioned to come in contact with a device being bonded. TAEC and TMA admit, with respect to the Accused Product, including NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6, that said Accused Product is manufactured outside of the United States. TAEC and TMA admit that the manufacture of said Accused Product involves bonding a device to a substrate. The aforementioned bonding activity requires the use of one or more bonding tools—either wire or flip chip bonding, the former of which is admitted to by TAEC and TMA.

58. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, TAEC has imported and TMA does continue to import the Accused Product, which is manufactured in accordance and compliance with JEDEC standards as confirmed below in reproduced FIGURE 6, which comes from publically available literature concerning, at the least, manufacturer part number TC58BYG2S0HBAI6, which is believed to be representative of other types of NAND Flash Memory and Accused Product:

> Tray usually refers to a JEDEC standard matrix tray measuring 12.7x5.35 inches and either 0.25 or 0.40 inches tall. Trays are usually constructed from plastic, but aluminum is permissible. JEDEC trays contain slots to allow air to pass vertically and are rated for at least 140°C to allow drying of parts in industrial ovens. Trays are stackable and feature a chamfered corner indicating the orientation of pin one of the parts. Trays are packaged according to the ESD (ElectroStatic Discharge) and MSL (Moisture Sensitivity Level) protection requirements determined by the manufacturer.

FIGURE 6 (reproduced)

59. Defendants TAEC and TMA are also affiliated with members of certain ESD Standard Organizations. Defendants TAEC and TMA further employ individuals—including senior engineers—that are involved with a promote ESD Standard Organizations and ESD Standards promulgated by these organizations.

60. In light of the foregoing, it is believed that the foregoing bonding processes are undertaken in accordance with one or more ESD Standards, including but not limited to JEDEC 625-A. and/or JEDEC625-B. The aforementioned bonding processes are further believed to be undertaken in accordance with one or more ESD Standards, including but not limited to ANSI ESD 20.20. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require the use of dissipative tools to minimize electrostatic discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require a resistance low enough to not damage a

device being bonded by way of electro-static discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require a resistance high enough to avoid a build-up of a charge large enough to damage a device being bonded as might otherwise occur through ESD discharge. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all seek to avoid inadvertent discharges thus JEDEC 625-A, JEDEC-625-B, and ANSI ESD 20.20 all seek to implement an essentially smooth current flow. Further—and as is evidenced by the requirements of JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20—the resistance range for various dissipative bonding tools and related tool tips is within 10^5 to 10^{12} ohms as is set forth in the asserted claim.

61. Anza has not granted authority to TAEC or TMA to import into the United States any product—including the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6)—covered by claim 28 of the '864 Patent. TAEC and TMA have admitted that the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) are manufactured outside of the United States. TAEC and TMA admit that their involvement with the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) is the sale and marketing of the same. TAEC and TMA have not alleged that they undertake any change to the design or manufacture of the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) upon its arrival in the United States or prior thereto.

62. Plaintiff Anza is not aware of any material change to the Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in

manufacturer part number TC58BYG2S0HBAI6) upon its entry into the United States. Anza therefore alleges that NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6 and that has been sold and marketed in the United States by TAEC and that continues to be marketed and sold in the United States by TMA has not been significantly altered or subjected to any real difference from the time of manufacture using Anza's patented methodologies to the time of import and subsequent marketing and sale in the United States. Anza further contends that it is not aware of any commercially viable non-infringing processes that might have resulted in the manufacture of the Accused Products that are imported into the United States for later marketing and sale.

63. The Accused Products (specifically including but not limited to NAND Flash Memory like that embodied in manufacturer part number TC58BYG2S0HBAI6) are sold as individual components and therefore cannot be said to be trivial and nonessential products in that they are, in fact, the product being sold and marketed.

64. As such, TAEC and TMA infringe—prior to October 1, 2017 and after October 1, 2017, respectively—claim 28 of the '864 Patent under 35 U.S.C. § 271(g). TAEC and TMA—by virtue of their predecessor in interest—have both been aware of the '864 Patent since at least October 15, 2007 as a result of International Trade Commission investigation number 37-TA-616. Notwithstanding their respective knowledge of the '864 Patent since at least October 15, 2007, TAEC and TMA have both elected to engage in activity that constitutes an infringement of the '864 Patent under 35 U.S.C. § 271(g). Notwithstanding their respective knowledge of the '864 Patent since at least October 15, 2007, TAEC and TMA have both elected not to undertake any efforts to avoid engaging in activity that constitutes an infringement of the '864 Patent under 35 U.S.C. § 271(g). Anza alleges that such activity (or conscious lack thereof) is willful in light of knowledge of the '864 Patent, especially since said knowledge is a result of the predecessor in

interest to TAEC and TMA having been engaged in litigation involving the '864 Patent. Anza therefore alleges that TAEC and TMA's infringement of the '864 Patent was and remains willful.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for relief and judgment as follows:

1. That Defendants have infringed the Patents-in-Suit;

2. That Defendants infringement of the Patents-in-Suit has been willful;

3. Compensation for all damages caused by Defendants' infringement of the Patents-in-Suit to be determined at trial, including a trebling of the same in light of Defendants' infringement having been willful;

4. A finding that this case is exceptional and an award of reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

5. Granting Plaintiff pre-and post-judgment interest on its damages, together with all costs and expenses; and,

6. Awarding such other relief as this Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all claims.

April 18, 2018

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