IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLORADO

Civil Action No. 17-cv-03135-WJM-MEH

ANZA TECHNOLOGY, INC., a California Corporation,

Plaintiff,

v.

MUSHKIN, INC., a Colorado Corporation,
d/b/a ENHANCED NETWORK SYSTEMS

Defendant.

SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

In accordance with Federal Rule of Civil Procedure 15(a)(1)(B), Plaintiff Anza Technology, Inc. ("Anza" or "Plaintiff"), by and through its undersigned counsel, complains and alleges against Defendant Mushkin, Inc. d/b/a Enhanced Network Systems, Inc. ("Defendant" or "Mushkin") as follows through this Second Amended Complaint for Patent Infringement of U.S. Patents 6,354,479 and 6,651,864 (the "Patents-in-Suit"):

NATURE OF THE ACTION

1. This is a civil action for patent infringement arising under the laws of the United States relating to patents, 35 U.S.C. § 101, *et seq*. The statutory provisions at issue in the civil action include, without limitation, 35 U.S.C. §§ 271 and 281. Plaintiff Anza Technology, Inc. seeks monetary damages for patent infringement.

JURISDICTION AND VENUE

2. This court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a). This court further has subject matter jurisdiction over this

case for patent infringement pursuant to the patent laws of the United States of America, 35 U.S.C. § 101, *et seq.*

3. Venue properly lies within the District of Colorado. Venue is properly vested with the District of Colorado pursuant to the provisions of 28 U.S.C. §§ 1391(b), (c), and (d) and 1400(b). Defendant is a Colorado corporation that maintains its principal place of business in Englewood, Colorado. Englewood, Colorado is located within the jurisdictional limits of the District of Colorado. Defendant has admitted that the District of Colorado is the appropriate venue for this action.

4. This Court has personal jurisdiction over Defendant because Defendant is incorporated under the laws of the State of Colorado. This Court further has personal jurisdiction over Defendant because Defendant transacts continuous and systematic business within the District of Colorado. Defendant's Corporate Headquarters are located within the District of Colorado. A portion of Defendant's website reproduced here identifies the Englewood, Colorado address as Defendant's Corporate Headquarters:

Corporate Headquaters
14 Inverness Drive East, Suite F-100
Englewood, CO 80112
720.383.2142 (Direct)
303.534.0827 (Fax)

5. This Court further has personal jurisdiction over the Defendant because the activities that Plaintiff contends infringe one or more claims of the Patents-in-Suit occur within or are caused to occur within the District of Colorado. This includes, but is not limited to, Defendant having sold and/or offered for sale products manufactured utilizing an infringing system, method, or apparatus otherwise claimed by one of the Patents-in-Suit. This further

includes Defendant having placed, or caused to be placed, products manufactured utilizing an infringing system, method, or apparatus claimed by one of the aforementioned Patents-in-Suit in the stream of interstate commerce.

PARTIES

6. Plaintiff Anza Technology, Inc. ("Anza") is a corporation organized and existing under the laws of the State of California. Plaintiff Anza maintains an office and principal place of business at 4121 Citrus Avenue, Suite 4, Rocklin, California. Anza is a designer, manufacturer, and seller of products directed to the manufacture and assembly of electronics including the bonding of electrostatic-sensitive devices.

7. Defendant Mushkin, Inc. ("Mushkin") is a corporation organized and existing under the laws of the State of Colorado. Mushkin maintains a regular and established place of business at 14 Inverness Drive East, Suite F-100, Englewood, Colorado. Mushkin operates under its trade name Enhanced Network Systems, Inc.

8. Up to and including parts of 2012, Mushkin was involved in and has admitted to being involved in the acquisition and sale of computer memory products, including those at issue with respect to the Patents-in-Suit as is further alleged below. Said admissions, and admissions similar thereto, come in the form of multiple Declarations of George Stathakis—President of Mushkin, Inc.—and which are attached to this Second Amended Complaint as Exhibits E and F, and otherwise incorporated herein.

9. In accordance with an asset purchase agreement dated April 1, 2012, by and between Defendant Mushkin and Avant Technology, Inc. ("Avant"), Avant became the sole aggregator of Mushkin-brand products by virtue of Avant having acquired certain assets of Defendant Mushkin. That asset purchase agreement included but was not limited to rights to sell under the Mushkin-brand name, marks, patents, and to retain certain employees that previously worked in Defendant Mushkin's memory component sales business. That purchase agreement likewise included the sale of the entirety of Defendant Mushkin's electronic memory component

sales business, which is alleged to have engaged in certain activities that constitute an infringement of the Patents-in-Suit. There is no indication in said asset purchase agreement of Avant having acquired any of the liabilities related to that business. Mushkin therefore retains liability for the same.

BACKGROUND

10. Defendant Mushkin acquired, assembled, imported, and/or sold products with Integrated Circuit ("IC") chips. The IC chips are electrostatic discharge ("ESD") sensitive devices. Manufacture and design of products with these ESD sensitive IC chips requires certain techniques and methods to guard against ESD events that have catastrophic consequences on IC chips. These certain techniques and methods infringe the Patents-in-Suit, described in further detail below.

11. JEDEC was formerly known as the Joint Electron Device Engineering Council. JEDEC is now known as the JEDEC Solid State Technology Association. JEDEC develops open standards for the microelectronics industry. JEDEC's mission is to create standards to meet the diverse technical and developmental needs of the industry. JEDEC brings manufacturers and suppliers together to participate in various committees and subcommittees. JEDEC's collaborative efforts ensure product interoperability thereby benefitting the industry by decreasing time-to-market and reducing product development costs. The creation of standards by way of collaboration through committees and subcommittees is sometimes referred to as 'Standard Setting.' JEDEC is sometimes referred to as a Standards Setting Organization ("SSO").

12. Among the standards developed by JEDEC are those for addressing the phenomenon known as electrostatic discharge (ESD). ESD is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. ESD can cause a range of harmful effects of importance in the electronics industry, specifically with regard to integrated circuits. Integrated circuits like memory and

semiconductor devices can suffer permanent damage when subjected to ESD as discussed herein.

13. A packaged integrated circuit includes one or more semiconductor dies. Semiconductor dies are generally mounted on a substrate and encapsulated in a mold as illustrated below in FIGURE 1. The substrate is the solid substance onto which another object—the semiconductor die—is etched, deposited, or otherwise fabricated. Mold compounds are the plastics used to encapsulate electronic packages such as a semiconductor die. A die coupled to a substrate and encapsulated in a mold is illustrated in FIGURE 1.

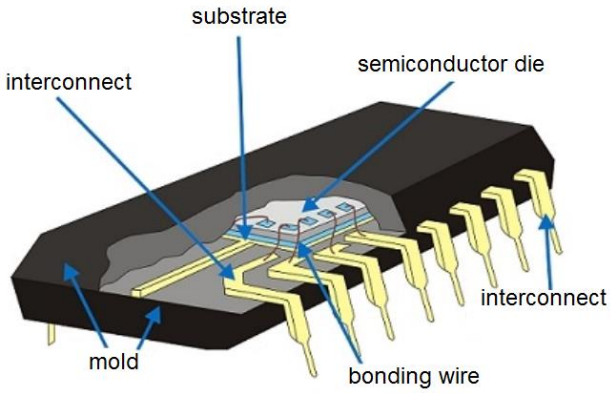

FIGURE 1

The packaged integrated circuit illustrated in FIGURE 1 includes interconnects (e.g., leads or pads). Interconnects are electrically coupled to the corresponding inputs and outputs of the semiconductor die to allow signals to pass between the die and other electronic componentry. Coupling of interconnects to the semiconductor die is referred to as bonding. In FIGURE 1, the die is bonded to the interconnects using bonding wire.

14. Bonding also encompasses coupling interconnects to a printed circuit board (PCB). A PCB mechanically supports and electrically connects the die package to other electrical components that might be found on the PCB using conductive tracks, pads, or other features. A Mushkin Redline memory kit from Mushkin's website prior to the April 1, 2012 asset sale is shown below as FIGURE 2. The memory kit shown in FIGURE 2 includes a digital integrated circuit encompassed in a mold (*i.e.*, a package) in which the semiconductor die is internally bonded to a series of interconnects. Those interconnects are then externally bonded to

a PCB, which is electronically coupled to other componentry. As a result of the internal bonding of the die within the package and the subsequent bonding of the package to the PCB, the device of FIGURE 2 is able to perform storage functions.

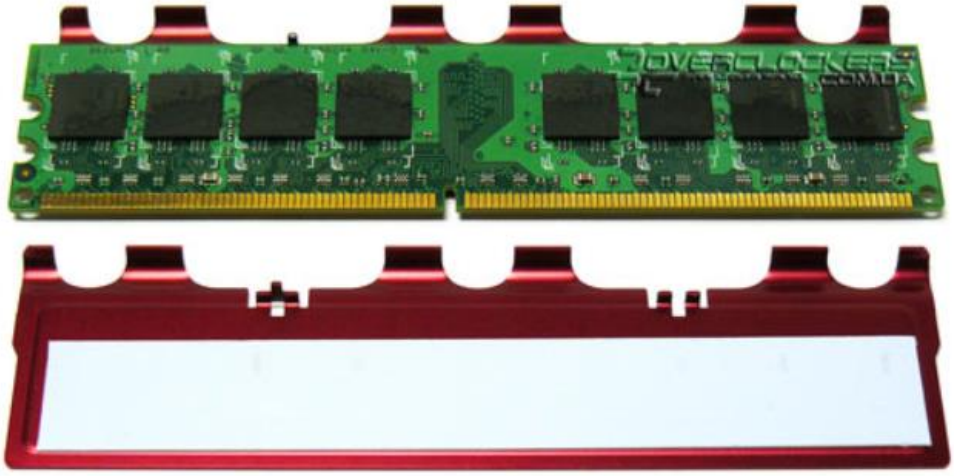

FIGURE 2

15. Interconnects are not limited to pins or wires. Other bonding techniques may be used. For example, a ball grid array (BGA) assembly technique may be implemented in the bonding process. A BGA assembly technique involves an array of conductive balls arranged on the face of the chip rather than the pins located along the sides as shown in FIGURE 1. An illustration of a ball grid array is shown in FIGURE 3 below.

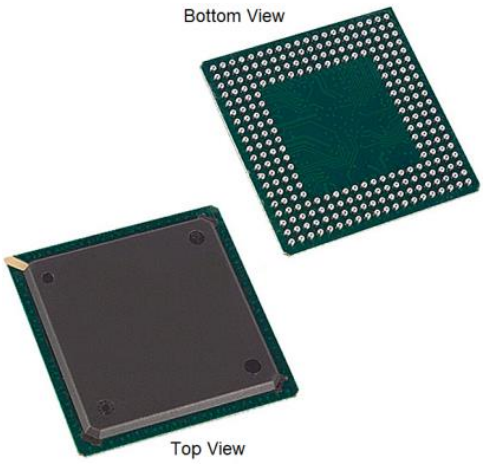

FIGURE 3

A ball grid array may be utilized both inside and outside a semiconductor package.

16. Bonding an integrated circuit or other computing component to a substrate or a PCB involves the use of one or more bonding tools. The integrated circuit comes in contact with such a tool, which places or connects the package on the substrate or the PCB as is appropriate. These tools may aid in effectuating the bonding of the circuit or component by way of wires, leads, bumps, or pads. Subject to a particular bonding technique, heat (thermal energy) may be applied to a bonding medium or material such as a metallic solder ball. This thermal energy may be applied by way of a bonding tool tip or an oven. Application of heat causes the medium to melt and electrically 'bond' the integrated circuit or module to the surface of the substrate or PCB.

17. One bonding technique is wire bonding. Wire bonding is the method of making interconnections with the integrated circuit and other components using, for example, gold or copper wire and the application of ultra-sonics or heat. The wire is attached at both ends using a combination of downward pressure, ultrasonic energy, and/or heat to make a weld.

18. Reproduced below are FIGURES 1 and 2 of U.S. patent number 6,354,479. U.S. patent number 6,354,479 is one of the Patents-in-Suit in the present action. FIGURE 1 of the '479 Patent "illustrates a typical capillary bonding tool 10. Such bonding tools are usually about one-half inch (12-13 mm) long and about one-sixteenth inch (1.6 mm) in diameter. The bonding tool tip 12 itself is usually from 3 to 10 mils (0.08 to 0.25 mm) long." '479:3:3-7. FIGURE 2 of the '479 Patent—to continue the example and for the purposes of context—is "a highly enlarged, cross-sectional view of the capillary bonding tool 10 as shown and described in FIG. 1 [of the '479 Patent]." '479:3:10-11. "[T]he chamfer surface 16 is provided to allow for smoother looping of the [bonding] wire as the bonding tool 10 is moved from the bonding pad on an integrated circuit to the bonding pad (not shown) on a lead frame of an integrated circuit assembly." '479:3:20-24.

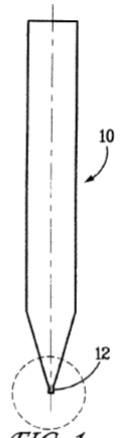

FIG. 1

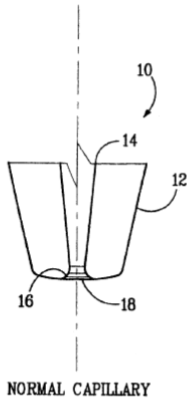

FIG. 2

(FIGURE 1 and 2 of the '479 Patent)

19. Another type of bonding is known as 'flip chip' bonding. Like wire bonding, flip chip bonding is a method for interconnecting an integrated circuit with other electrical components. Unlike wire bonding, interconnects are established utilizing solder bumps deposited on a substrate or package. Flip chip microelectronic assembly is the direct electrical connection of face-down (or flipped) integrated circuit chips onto substrates or semiconductor packages onto PCBs using conductive bumps. The bumped die or package is flipped and placed face down so that the bumps directly connect to the substrate or PCB. This technique is in contrast to wire bonding where the die or package is mounted upright and wires establish interconnects.

20. Naturally occurring electrostatic charges of varying degrees can build up when bonding tools come in contact with the die, package, or bonding medium. Electrostatic charges can even build up when a die or package is removed from storage or a transport vessel and placed on the wafer or PCB before any bonding takes place. Without strict safeguards, electrostatic charges can be built up from almost any contact and through almost any activity. If enough static is generated, discharge can occur and damage to an electronic component may result. The threat of ESD is present in microelectronics assembly utilizing both wire and flip chip bonding techniques. There is a need to dissipate and/or block such a static build up as to avoid damage to the electrical componentry being bonded.

21. Electronics manufacturers establish electrostatic protective areas free of static using measures to prevent (dis)charging. This includes the use of bonding tools, apparatus, and

techniques that obviate a buildup of ESD or otherwise dissipate the same. JEDEC has taken a leadership role in developing standards for ESD since the early 1980s. This includes developing standards for device handling related to ESD. JEDEC is accredited by the American National Standards Institute (ANSI). ANSI oversees the creation, promulgation, and use of norms and guidelines for various industries. ANSI is actively engaged in accreditation to assess the competence of organizations determining conformance to standards. The Electrostatic Discharge Association (ESDA), too, is a professional association dedicated to advancing the theory and practice of ESD avoidance. The foregoing groups are cumulatively referred to as "ESD Standards Organizations" and develop, collectively or on their own, "ESD Standards."

22. For example, ESDA and JEDEC have—since October 2008—had a joint memorandum of understanding concerning the development of ESD Standards and publications in the field of ESD. The ESDA and JEDEC entered into such an agreement in the best interest of their organizations, their membership, and the electronics industry. Notwithstanding the foregoing joint relationship, JEDEC has—since December 1999—through at least JEDEC Standard No. 625-A ("Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices") indicated that JEDEC members should "incorporate these minimal requirements into their ESD control program to provide a consistent protection level for their products." JEDEC Standard No. 625-A is attached hereto as Exhibit A.

23. JEDEC Standard No. 625-A, for example, "establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD)." JEDEC Standard No. 625-A continues in noting that "[t]he passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part." Table 1 of Section 6.1 of JEDEC Standard No. 625-A, for example, requires the use of an ESD protected area, workstations, and tools having a resistance to ground of less than 10^9 ohms. JEDEC Standard No. 625-A also references static dissipative material as "[a] material having a surface resistance between 1 x 10^5 ohms and 1x10^{11} ohms."

24. Like JEDEC Standard No. 625-A, subsequent and ancillary ESD Standards implemented by various ESD Standards Organizations require, in part, the use of tools made of dissipative materials having approximately the same resistance values in connection with handling integrated circuits that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent the discharge of a charge to an ESD sensitive device such as flash memory, including the Accused Products as further discussed herein. These ranges are also high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package.

25. For example, JEDEC Standard 625-B ("Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices"), which is attached hereto as Exhibit B, "replaces JESD625-A and JEDEC Standard No. 42." In a manner similar to its predecessor JEDEC 625-A, the JEDEC 625-B Standard was "prepared to standardize the requirements for a comprehensive Electrostatic Discharge (ESD) control program for handling ESD-Sensitive (ESDS) devices." JEDEC 625-B "establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD)." JEDEC 625-B states that "[t]he device types for which these requirements are applicable include, but are not limited to, ESD-sensitive discrete and integrated circuit semiconductors, multi-chip modules, optoelectronic devices, and thin film passive devices." JEDEC 625-B, too, incorporates a series of other ESD Standards, including but not limited to ANSI/ESD S20.20.

26. JEDEC 625-B discusses the use of static dissipative material as "[a] material having a surface resistance between 1×10^4 ohms and 1×10^{11} ohms." JEDEC 625-B also discusses the applicable use of the standard to include both semiconductor manufacture and semiconductor processing and testing. JEDEC 625-B characterizes manufacture as "from wafer electrical probe through shipment of finished devices," JEDEC 625-B characterizes processing and testing as "from receipt through shipment of finished devices." JEDEC 625-B also incorporates a series of other ESD Standards as set forth in Section 2 of the standard and entitled

"Technical References."

27. JEDEC has also published a series of other ESD-related standards including but not limited to:

* Joint JEDEC / ESDA Human Body Model (JS-001-2017);

* Joint JEDEC / ESDA Charged Device Model (JS-002-2014);

* Understanding Electrical Overstress (JEP174);

* Discontinuing Use of the Machine Model for Device ESD Qualification (JEP172A);

* HBM Target Levels (JEP155);

* CDM Target Levels (JEP157);

* System Level Part 1 Overview (JEP161); and

* System Level Part 2 Design Methods (JEP162).

28. Each of the foregoing standards seek to avoid inadvertent electrostatic static discharge by implementing manufacturing and quality controls that include the use of bonding tools with resistance high enough to avoid current flows that may damage a device such as an integrated circuit die and/or package. This includes implementing ESD controls related to resisting current flow in ranges between 10^5 and 10^{12} ohms. This further includes maintaining current flows low enough to prevent a discharge.

29. Like JEDEC Standard No. 625-A, subsequent and ancillary ESD Standards require, in part, the use of tools made of dissipative materials having approximately the same resistance values in connection with handling integrated circuits that are particularly sensitive to ESD events. These resistance ranges are low enough to prevent the discharge of a charge to an ESD sensitive device such as a memory module, including the accused products as discussed further herein. These ranges are also high enough to avoid current flows that may damage a device such as a memory module, including the accused products as discussed further herein.

30. DDR DRAM stands for Double Data Rate (DDR) Dynamic Random Access Memory (DRAM). DDR DRAM is a class of memory integrated circuits used in computers.

DDR DRAM involves a random access semiconductor memory that stores each bit of data in a capacitor on an integrated circuit. A memory refresh circuit periodically re-writes data in the capacitors to prevent a phenomenon known as data 'leakage' that would otherwise result in data being lost. Because of the re-writing of data by the refresh circuit, this type of memory is known as dynamic random access memory (the aforementioned DRAM).

31. Generations of DRAM are referenced with a prefix (e.g., DDR4, SDR, EDR, and EDO). This abbreviation is reflective of a buffer size as it relates to datawords per memory access. For example, DDR 4 SDRAM is an abbreviation for double data rate fourth-generation synchronous dynamic random-access memory, which is a type of synchronous dynamic random-access memory (SDRAM) with a high bandwidth ("double data rate") interface. DDR4 is a successor to DDR3 technologies, which is a successor to DDR2, and so on.

32. DRAM is typically used in digital electronics where low-cost and high-capacity is a concern. One of the largest applications for DRAM is the main memory of a computer or a graphics card. DRAM is also used in portable devices and video game consoles. An advantage of DRAM is the structural simplicity of its memory cells usually involving one transistor and a capacitor. Because of this structural simplicity, DRAM can be implemented in extremely high densities allowing it to be 'cheaper per bit' versus other memory technologies such as static random access memory (SRAM). As electronic parts like computer central processing units become packed more densely with transistors, the transistors shrink and become more vulnerable to ESD.

33. The low-cost nature of DRAM makes ESD of particular concern. Damage suffered as a result of ESD during the manufacture or assembly process will drive up the cost of the finished product. In order for products utilizing DRAM technology to remain cost-feasible, it is important for DRAM products to remain ESD-free during the manufacture and assembly process. Defendant's acquisition, assembly, aggregation, development, design, production, and manufacture of memory solutions, specifically including DRAM solutions, utilizing surface mount technology lines invokes concerns as to ESD and ESD sensitive devices.

34. Acquisition, assembly, aggregation, development, design, production, and manufacture of memory solutions, specifically including ESD-sensitive DRAM solutions, requires the use of certain techniques and methods to guard against ESD events that can have catastrophic consequences for ESD-sensitive DRAM solutions.

35. As a result, Plaintiff alleges that Defendant acquired, assembled, imported, and/or sold products that utilized certain manufacturing practices to minimize the costs resulting from damaging ESD events, which includes but is not limited to complying with or otherwise observing the aforementioned JEDEC, ANSI, and ESDA standards as well as other ESD Standards observed in the manufacture of ESD sensitive electronics devices like those at issue in the present litigation and otherwise accused of infringement.

36. Defendant intentionally acquired, assembled, imported, and/or sold products that were designed, engineered, assembled, or manufactured in ways that meet or exceed ESD-Standards for reducing the risk of damage to ESD sensitive devices. This includes but is not limited to certain DRAM products, including the accused products identified below, which are therefore alleged to infringe the Patents-in-Suit as is further detailed herein.

ACCUSED PRODUCTS

37. The Accused Products with respect to Defendant Mushkin, for purposes of the Patents-In-Suit, include but are not limited to BGA packaged ICs and PCBs to which the BGA packaged ICs are mounted. The Accused Products also include packaged ICs and PCBs involving non-BGA related bonding techniques. The Accused Products specifically include but are not limited to: REDLINE, BLACKLINE, RIDGEBACK, RADIOACTIVE, SILVERLINE, PROLINE, ESSENTIALS, and APPLE (the "Accused Products").

38. The Accused Products have at one time or another, prior to April 1, 2012—and within the relevant statute of limitations time period—been made, used, sold, manufactured, imported, or offered for sale by Defendant Mushkin as shown in Figure 4, below, which is a screenshot from Mushkin's archived website.

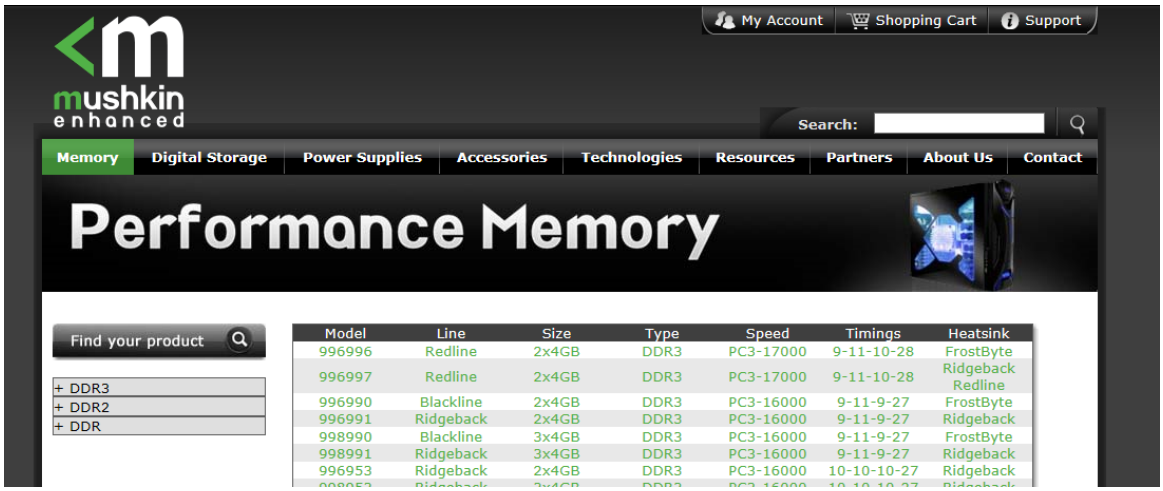

Figure 4.

39. The Accused Products utilize various ICs including but not limited to memory modules that are bonded to PCBs or other electronic componentry. As explained above, in order to minimize the risk of an ESD event, ICs are manufactured using processes and methods that infringe at least claim 39 of the '479 patent, and claim 28 of the '864 patent. Therefore, Plaintiff alleges that Defendant acquired, imported, marketed, and/or sold the Accused Products that were manufactured using processes and methods that infringe at least claim 39 of the '479 patent, and claim 28 of the '864 patent. Plaintiff further alleges that the Accused Products are manufactured or have been manufactured on assembly lines that utilize processes and methods recited by claim 39 of the '479 patent and claim 28 of the '864 patent to reduce the risk of damage from ESD events.

40. Defendant Mushkin acquired, assembled, imported, marketed, and/or sold products, including the Accused Products, made in compliance with ESD Standards including those promulgated by JEDEC, ANSI, and other ESD Standards Organizations. Defendant Mushkin acquired, assembled, imported, marketed, and/or sold products, including the Accused Products, that avoided inadvertent electrostatic static discharge during bonding. This avoidance occurs through implementing manufacturing and quality controls that involve the use of tools with resistance high enough to avoid current flows that may damage a device such as an

integrated circuit die and/or package. This includes implementing ESD controls related to resisting current flow in ranges between 10^5 and 10^{12} ohms. This further includes maintaining current flows low enough to prevent a discharge.

41. Defendant Mushkin may have acquired, assembled, imported, marketed, and/or sold additional products that similarly adopt and implement ESD Standards and quality controls in their manufacturing processes prior to acquisition, assembly, importation, marketing, and/or sale (like those described above) to avoid inadvertent static discharge that might otherwise damage and electronic component.

THE PATENTS-IN-SUIT

42. On March 12, 2002, the United States Patent and Trademark Office ("USPTO") duly and legally issued U.S. patent number 6,354,479 entitled 'Dissipative Ceramic Bonding Tip,' (the "'479 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '479 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '479 Patent is attached hereto as Exhibit C.

43. On November 25, 2003, the USPTO duly and legally issued U.S. patent number 6,651,864 entitled 'Dissipative Ceramic Bonding Tool Tip,' (the "'864 Patent"). Plaintiff Anza is, by way of assignment, owner of the entire right, title, and interest in the '864 Patent and vested with the right to bring this suit for damages. A true and correct copy of the '864 Patent is attached hereto as Exhibit D.

44. The foregoing patents are collectively referred to as the "Patents-in-Suit" and are incorporated into this Second Amended Complaint as if fully set forth herein.

COUNT ONE

INFRINGEMENT OF THE '479 PATENT

45. Plaintiff re-alleges each of the foregoing paragraphs 1-44 as if fully set forth herein.

46. Defendant infringed (at least) claim 39 of the '479 Patent under 35 U.S.C. § 271(g). Claim 39 of the '479 Patent recites as follows:

> 39. The method of claim 37, wherein said dissipative material has a high enough stiffness to resist bending when hot and has a high enough abrasiveness to function for at least two uses.

Claim 37 of the '479 Patent—from which claim 39 depends—recites as follows:

> 37. A method of using a bonding tip, comprising bonding a device using a bonding tip made with a dissipative material that has a resistance low enough to prevent a discharge of charge to said device and high enough to avoid current flow large enough to damage said device.

47. Section 271(g) of Title 35 allows for a claim of infringement whenever a party—without authority—imports into the United States or offers to sell, sells, or uses within the United States a product that is made by a process patented in the United States if said infringement occurs during the term of said patent. The '479 Patent—and claim 39 thereof—is currently in force. Plaintiff Anza has not granted authority to Defendant Mushkin to market, sell, or offer for sale in the United States any product—including the Accused Products covered by claim 39 of the '479 Patent. Defendant Mushkin has admitted to its having acquired, assembled, imported, marketed, and/or sold products, including the Accused Products, by way of the Stathakis Declarations, which are attached hereto as Exhibits E and F, respectively.

48. Plaintiff Anza is not aware of any material change to the Accused Products upon its entry or prior to said entry into the United States. Nor is Plaintiff Anza aware of any material change to the Accused Products after Defendant Mushkin having acquired, assembled, imported, marketed, and/or sold the same, including as set forth in in the Stathakis Declarations. Anza therefore alleges that the REDLINE, BLACKLINE, RIDGEBACK, RADIOACTIVE, SILVERLINE, PROLINE, ESSENTIALS, and APPLE product lines have been acquired, assembled, imported, marketed, and/or sold in the United States by Defendant Mushkin without having been significantly altered or subjected to any real difference from the time of manufacture

using Anza's patented methodologies to the time of acquisition, assembly, importation, marketing, and/or sale in the United States. Anza further contends that it is not aware of any commercially viable non-infringing processes that might have resulted in the manufacture of the Accused Products.

49. The Accused Products are sold as individual components and therefore cannot be said to be trivial and nonessential products in that they were, in fact, the product being acquired, assembled, imported marketed, and/or sold.

50. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, Defendant Mushkin acquired, assembled, imported marketed, and/or sold the Accused Products, which are manufactured in accordance and compliance with JEDEC standards.

51. In light of the foregoing, it is believed that the foregoing bonding processes are undertaken in accordance with one or more ESD Standards, including but not limited to JEDEC 625-A and/or JEDEC 625-B. The aforementioned bonding processes are further believed to be undertaken in accordance with one or more ESD Standards, including but not limited to ANSI ESD 20.20. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require the use of dissipative tools to minimize electrostatic discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 require a resistance low enough to prevent a discharge to a device being bonded. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 require a resistance high enough to avoid current flow large enough to damages a device being bonded.

52. With respect to claim 39—which depends from claim 37 and that Anza alleges is infringed under 35 U.S.C. § 271(g)—Defendant Mushkin is believed to have acquired, assembled, imported marketed, and/or sold product that is manufactured using JEDEC and ANSI compliant standards and—further—that utilized dissipative bonding tools that could be used more than once. It would defy commercial manufacturing principles for any manufacturer to

replace a bonding tool with each and every bond. For example—referring to the die package in FIGURES 1, 2, and 3 —multiple bond points are illustrated. As such, a bonding tool would be required to facilitate each of those wire bonds if the tool were not used more than once.

53. As such, Defendant Mushkin infringed—prior to April 1, 2012—claim 39 of the '479 Patent under 35 U.S.C. § 271(g).

COUNT TWO

INFRINGEMENT OF THE '864 PATENT

54. Plaintiff re-alleges paragraphs 1-53 as if fully set forth herein.

55. Defendant infringed (at least) claim 28 of the '864 Patent, which recites:

> 28. A method of using an electrically dissipative bonding tool tip, having a resistance in the range of 10^5 to 10^{12} ohms, comprising:
> providing the electrically dissipative bonding tool tip;
> bonding a material to a device;
> allowing an essentially smooth current to dissipate to the device, the current being low enough so as not to damage said device being bonded and high enough to avoid a build up of charge that could discharge to the device being bonded and damage the device being bonded.

56. Claim 28 recites an electrically dissipative bonding tool tip, specifically the use thereof. Claim 28 would, therefore, be infringed (in part) by placing a bonding tip in a device positioned to come in contact with a device being bonded. Defendant Mushkin admits by way of the Stathakis Declarations, which have been incorporated into this Second Amended Complaint by reference, that it would purchase standard 'off the shelf' memory products and memory modules from suppliers. Defendant Mushkin further admits that the encapsulated IC chips were "already placed and bonded on a module board or printed circuit board. Defendant Mushkin admits that the supplier to Mushkin or the IC chip manufacturer would have bonded the IC chips on printed circuit boards or memory module boards prior to delivery to Mushkin. The aforementioned bonding activity requires the use of one or more bonding tools—either wire or flip chip bonding. Such bonding requires the use of a bonding tool tip as recited in claim 28.

57. Surface mounted technology inherently leads to the creation of electrostatic conditions that may result in ESD. To combat ESD, Defendant Mushkin has acquired, assembled, imported, marketed, and/or sold the Accused Products, which are manufactured in accordance and compliance with JEDEC standards.

58. In light of the foregoing, it is believed that the foregoing bonding processes are undertaken in accordance with one or more ESD Standards, including but not limited to JEDEC 625-A. and/or JEDEC625-B. The aforementioned bonding processes are further believed to be undertaken in accordance with one or more ESD Standards, including but not limited to ANSI ESD 20.20. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require the use of dissipative tools to minimize electrostatic discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require a resistance low enough to not damage a device being bonded by way of electro-static discharge. The resistance ranges set forth in JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all require a resistance high enough to avoid a build-up of a charge large enough to damage a device being bonded as might otherwise occur through ESD discharge. JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20 all seek to avoid inadvertent discharges thus JEDEC 625-A, JEDEC-625-B, and ANSI ESD 20.20 all seek to implement an essentially smooth current flow. Further—and as is evidenced by the requirements of JEDEC 625-A, JEDEC 625-B, and ANSI ESD 20.20—the resistance range for various dissipative bonding tools and related tool tips is within 10^5 to 10^{12} ohms as is set forth in the asserted claim.

59. Anza has not granted authority to Defendant Mushkin to acquire, assemble, import, market, and/or sell in the United States any product—including the Accused Products—made by the method covered by claim 28 of the ’864 Patent. Defendant Mushkin admits that its involvement with the Accused Products is the acquisition, marketing, and sale of the same, up through April 1, 2012. Defendant Mushkin has not alleged by way of the Stathakis Declarations that it undertook any change to the design or manufacture of the Accused Products, except for

the relabeling of the Accused Products, and the addition of a "heatsink" to memory module boards.

60. Plaintiff Anza is not aware of any material change to the Accused Products by subsequent processes. Anza therefore alleges that the Accused Products that were acquired, assembled, imported, marketed, and/or sold in the United States by Defendant Mushkin had not been significantly altered or subjected to any real difference from the time of manufacture using Anza's patented methodologies to the time of acquisition, assembly, importation, marketing, and/or sale in the United States. Anza further contends that it is not aware of any commercially viable non-infringing processes that might have resulted in the manufacture of the Accused Products that are imported into the United States for later of acquisition, assembly, importation, marketing, and/or sale.

61. The Accused Products are sold as individual components and therefore cannot be said to be trivial and nonessential products in that they were, in fact, the product being acquired, assembled, imported, marketed, and/or sold.

62. As such, Defendant Mushkin infringed—prior to April 1, 2012—claim 28 of the '864 Patent under 35 U.S.C. § 271(g).

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for relief and judgment as follows:

1. That Defendant infringed the Patents-in-Suit up to an including April 1, 2012;

2. Compensation for all damages caused by Defendant's infringement of the Patents-in-Suit to be determined at trial;

3. Granting Plaintiff pre-and post-judgment interest on its damages, together with all costs and expenses; and,

4. Awarding such other relief as this Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a trial by jury on all claims.

Date: June 8, 2018

/s/*Colby B. Springer*

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CERTIFICATE OF SERVICE

I hereby certify that the following documents were served on the date below to counsel of record by electronic transmission using the Court's CM/ECF system. The CM/ECF system will send out notification of this filing to all counsel of record.

- **SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT**
- **EXHIBITS A-F**

June 8, 2018

/s/*Hannah T. Yang*
Hannah T. Yang