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Complex Memory LLC

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

COMPLEX MEMORY LLC,

Plaintiff

v.

RENESAS ELECTRONICS CORPORATION and RENESAS ELECTRONICS AMERICA INC.,

Defendants

Case No.: 3:18-cv-4103

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Complex Memory LLC ("Complex Memory"), for its Complaint against Defendants Renesas Electronics Corporation ("Renesas-Japan") and Renesas Electronics America Inc. ("Renesas-America") (collectively, "Renesas" or "Renesas Defendants"), hereby alleges as follows:

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 17330 Preston Road, Suite 200D, Dallas, Texas 75252.

2. On information and belief, Defendant Renesas-Japan is a Japanese corporation with a principal place of business at Toyosu Foresia, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan.

3. On information and belief, Defendant Renesas-America is a California corporation with a principal place of business at 1001 Murphy Ranch Road, Milpitas, CA 95035.

JURISDICTION AND VENUE

4. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Renesas of claims of U.S. Patent Nos. 5,890,195; 5,896,550; 5,963,481; 6,393,590; 6,658,576; 6,968,469; and 7,730,330 ("the Patents-in-Suit").

5. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. Renesas-Japan is subject to the personal jurisdiction of this Court because, among other things, Renesas-Japan has committed and continues to commit acts of patent infringement in the State of California, directly, through its subsidiaries, and/or through authorized distributors, including by making, using, offering to sell, and/or selling, Accused Products and services in California, and/or importing the Accused Products into California. In addition, or in

the alternative, this Court has personal jurisdiction over Renesas-Japan pursuant to Fed. R. Civ. P. 4(k)(2).

7. Venue is proper as to Renesas-Japan in this district under 28 U.S.C. § 1391(c) because, *inter alia*, Renesas-Japan is a foreign corporation.

8. Renesas-America is subject to personal jurisdiction of this Court because, inter alia, on information and belief, (i) Renesas-America is headquartered in the State of California, (ii) Renesas-America maintains office locations in the State of California; (iii) Renesas-America is registered to transact business in the State of California; and (iv) Renesas-California has committed and continues to commit acts of patent infringement in the State of California, including by making, using, offering to sell, and/or selling accused products and services in California, and/or importing the Accused Products into California.

9. Venue is proper as to Renesas-America in this district because, inter alia, on information and belief, Renesas-America is headquartered in, and maintains a regular and established place of business, in this judicial district, and Renesas-America has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district, and/or importing accused products and services into this district.

BACKGROUND

10. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM".

11. G.R. Mohan Rao invented the technology claimed in the '195 Patent.

12. On April 20, 1999, the United States Patent and Trademark Office duly and

lawfully issued U.S. Patent No. 5,896,550 ("the '550 Patent"), entitled "Direct Memory Access Controller With Full Read/Write Capability."

13. Omer Lem Wehunt and Jeffrey M. Lavin invented the technology claimed in the '550 Patent.

14. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 ("the '481 Patent"), entitled "Embedded Enhanced DRAM, And Associated Method."

15. Michael Alwais and Michael Peters invented the technology claimed in the '481 Patent.

16. On May 21, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,393,590 ("the '590 Patent"), entitled "Method and Apparatus for Ensuring Proper Functionality of a Shared Memory, Multiprocessor System."

17. Barry Everett Wood and Brian Baker invented the technology of the '590 Patent.

18. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 ("the '576 Patent"), entitled "Energy-Conserving Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction."

19. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

20. On November 22, 2005, the United States Patent and Trademark Office duly and lawfully issued U.S . Patent No. 6,968,469 ("the '469 Patent"), entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored."

21. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '469 Patent.

22. On June 1, 2010, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,730,330 ("the '330 Patent"), entitled "System and Method For Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set."

23. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '330 Patent.

24. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

25. By letter dated May 4, 2018, Complex Memory notified Renesas-Japan of the existence of the Patents-in-Suit, and of infringement thereof by Renesas and its customers. Complex Memory's letter identified exemplary infringing Renesas products and an exemplary infringed claim for each of the Patents-in-Suit.

26. By letter dated May 4, 2018, Complex Memory notified Renesas-America of the existence of the Patents-in-Suit, and of infringement thereof by Renesas and its customers. Complex Memory's letter identified exemplary infringing Renesas products and an exemplary infringed claim for each of the Patents-in-Suit.

27. In addition, while prosecuting U.S. Patent Application No. 10/869,760, Renesas, through U.S. counsel, notified the U.S. Patent and Trademark Office of the existence of the '550 Patent.

28. As of the date of this Complaint, Complex Memory has not received any response from Renesas.

29. Accordingly, Renesas has received notice of the Patents-in-Suit and of

infringement thereof by Renesas and its customers.

COUNT I: INFRINGEMENT OF THE '195 PATENT

30. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

31. Upon information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A15, A57, A53, and other ARM Cortex-A architectures, including the products identified in Exhibit A ("Accused Renesas Products").

32. For example, on information and belief, Renesas has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. The Accused Renesas Products include the R-Car H3 platform. On information and belief, the R-Car H3 platform includes ARM Cortex-A57 and A53 Cores, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, R-Car H3 Block Diagram. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. In performing the method of claim 6, processors in the Accused Renesas Products receive an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller) or an address channel of a bus. Accused Renesas Products compare the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When [the cache controller] receives a request from the core, it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." Ex. 3, ARM

Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller. When a match between the received address and a matching address stored in one of the latches occurred, the Accused Renesas Products perform the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match, known as a hit, and the line is marked valid, then the read or write occurs the cache memory." *Id*. When a match between the received address and an address stored in one of the latches does not occur, the Accused Renesas Products perform the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "If the address is not found in the L1 cache but is in the L2 cache, then the cache line is loaded into the L1 cache from the L2 cache and the data is returned to the core. . . . If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 cache from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3. Inclusive and exclusive caches. When the match does not occur, the Accused Renesas Products further store the received address in one of the latches corresponding to the selected register. For example, the Accused Renesas Products store the received address, such as the tag, corresponding to the register being accessed, in the cache memory system latches, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches. *See*, *e.g.*, Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. The Accused Renesas Products further modify the received address to generate a modified address. For example, the hardware autoprefetcher in the Accused Renesas Products prefetches data or instructions stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 6.6.2 Data prefetching and monitoring ("When a pattern is detected, the automatic

prefetcher starts linefills in the background"). *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher. "[P]refetch address = current address + (stride x programmed distance)." On information and belief, the Accused Renesas Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused Renesas Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 caches from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3 Inclusive and exclusive caches. The Accused Renesas Products then stored the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way register latches.

33. On information and belief, Renesas has committed the foregoing infringing activities without a license.

34. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

COUNT II: INFRINGEMENT OF THE '550 PATENT

35. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

36. Upon information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed the '550 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the

United States or importing into the United States products incorporating DMA controllers with secure modes, including products identified in Exhibit A ("Accused Renesas Products").

37. For example, on information and belief, Renesas has infringed at least claim 14 of the '550 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Renesas RZ/G Series MPUs, which comprise a DMA controller that controls direct memory access transfers to and from main memory. *See* Ex. 7, RZ/G Series for Rich Graphics Applications, User's Manual: Hardware, Chapter 16. Direct Memory Access Controller for System (SYS-DMAC), 16-1 ("The SYS-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules."). Renesas' DMA Controllers include a register set for providing control and status of the direct memory access transfers to and from the main memory. *See id.*, Chapter 16.3 Register Descriptions, 16-3 ("Table 16.1 lists the registers of the SYS-DMAC. Table 16.2 shows the register states of the SYS-DMAC in each operating mode.") Renesas' DMA Controller provides limited access to registers within the register set, for example, when operating in Secure Mode. *See id.*, Chapter 16.3.3 DMA Secure Control Register for Lower-Numbered Channels (DMASEC_L), at 16-23 ("Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode. DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE"). Renesas DMA Controllers include a configuration register having a first control field, wherein access provided to registers within the register set changes based on a value placed in the first control field. For example, configuration register DMASEC_L includes a first control field, such as the "Secure" vs. "Non-secure" Mode Settings for DMA channels. When a control field in the DMASEC_L

register is set to "Secure," limited access is provided to registers described above. *Id.*

38. On information and belief, Renesas has induced, and continues to induce, infringement of the '550 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

39. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

40. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

41. On information and belief, Renesas knew the '550 Patent existed, knew of its claims, and knew of Renesas' infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '550 Patent.

COUNT III: INFRINGEMENT OF THE '481 PATENT

42. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

43. On information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed, and continue to infringe the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States devices that interface with DDRxL and/or LPDDRx memories, including the Accused Renesas Products identified in Exhibit A.

44. For example, on information and belief, the Renesas Defendants infringe at least claim 16 of the '481 Patent by performing a method of accessing data. Specifically, on information and belief, the Accused Renesas Products access LPDDR memory. See, e.g., Ex. 8, R-Car H3 and M3 Starter Kit Product Specifications ("memory controller for LPDDR4 4 GB in 2 channels, each 64-bit wide"). LPDDR4 memory accessed by Renesas products is a memory system comprising multiple banks with multiple rows. *See, e.g.*, Ex. 9, LPDDR4 Standard, JEDEC JSD209-4B at p. 18 ("LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured with either 1 or 2 channels. Each channel is comprised of 8-banks with from 2 Gb to 16 Gb per channel density."). The Accused Renesas Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id*. ("Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access."). On information and belief, in LPDDR4 memory accessed by Renesas products, the memory locations of the first memory row are disposed upon a substrate. The Accused Renesas Products access the data stored at the memory locations identified in the first access request. *Id*. While the data stored at the memory locations identified by the first access request is being accessed, the Accused Renesas Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a seamless burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See id.* at

p. 135, Table 38 NOTE 3 ("After READ w/AP, seamless read operations to different banks are supported") and at p. 124 ("The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued."). In LPDDR4 memory access by the Accused Renesas Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. The Accused Renesas Products also access the data stored at the memory locations identified in the second access request. *Id*. at p. 18.

45. On information and belief, Renesas has induced, and continues to induce, infringement of the '481 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

46. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

47. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

48. On information and belief, Renesas knew the '481 Patent existed, knew of an exemplary infringed claim of the '481 Patent, and knew of exemplary infringing Renesas products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '481 Patent.

COUNT IV: INFRINGEMENT OF THE '590 PATENT

49. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

50. Upon information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed, and continue to infringe, the '590 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States Microcontroller units and kits, including the Accused Renesas Products identified in Exhibit A.

51. For example, on information and belief, the Renesas Defendants have infringed at least claim 1 of the '590 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Renesas RX71M MCU, which includes a processing element for use in a multiprocessor computing system. *See, e.g.,* Ex. 10, RX71M Group, RENESAS 32-Bit MCU, RX Family/RX700 Series, User's Manual: Hardware, Dec. 2017, p. 2048, Chapter 40.4 Multi-Processor Communications Function ("[u]sing the multi-processor communication functions enables to transmit and receive data by sharing a communication line between multiple processors by using asynchronous serial communication in which the multi-processor bit is added.") Accused Renesas Products include a processing block, such as the RX CPU. *Id.* at p. 87. Accused Renesas Products include an input port for receiving instruction elements for execution by said processor block. *Id.* Accused Renesas Products include a watchdog timer in operative relationship with said processor block, said watchdog timer capable to cause said processor block to reset after a first predetermined time interval has elapsed from setting the watchdog timer in a first initial condition. *See id.* at 87 ("The watchdog timer (WDT) is a 14-bit down-counter. It can be used to reset this MCU when the counter underflows because its value cannot be refreshed due to the system being out of control."). *See also id.* at 1499 ("The WDT has two start modes: auto-start mode, in which counting automatically starts after release

from the reset state, and register start mode, in which counting is started by refreshing (writing to the register)."). Accused Renesas Products include a sanity timer in operative relationship with said processor block, such as an Independent Watchdog Timer, which is capable to cause said processor block to reset after a second predetermined time interval has elapsed from setting the sanity timer in a second initial condition. *See id.* at 1506 ("The independent watchdog timer (IWDT) can be used to detect programs being out of control. The user can detect when a program runs out of control if an underflow occurs, by creating a program that refreshes the IWDT counter before it underflows.") In the Accused Renesas Products, the processor block is responsive to the presence of at least one predetermined executable instruction element to cause said watchdog timer to acquire the first initial condition. For example, in the Renesas RX71M, the CPU responds to a predetermined executable instruction element, such as an instruction to set the WDT into "Register Start Mode," to cause the watchdog timer to acquire the initial condition. In the Accused Renesas Products, the processing element is responsive to an external signal to cause said sanity timer to acquire the second initial condition. For example, the MCU is responsive to an external signal, such as the IWDT start mode selection signal that sets register OFS0. *See id.* at p. 258 ("The option-setting memory determines the state of this MCU after a reset. Option-setting memory is allocated to the configuration setting area and user boot area of the flash memory, and the available methods of setting are different for the two areas.").

52. On information and belief, Renesas has induced, and continues to induce, infringement of the '590 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set

up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

53. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

54. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

55. On information and belief, Renesas knew the '590 Patent existed, knew of an exemplary infringed claim of the '590 Patent, and knew of exemplary infringing Renesas products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '590 Patent.

COUNT V: INFRINGEMENT OF THE '576 PATENT

56. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

57. Upon information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed, and continue to infringe, the '576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including the Accused Renesas Products identified in Exhibit A.

58. For example, on information and belief, the Renesas Defendants have infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. For example, on information and belief, the Renesas R-Car M3 platform includes an SoC based on ARM Cortex-A53 and A-57 architecture. *See* Ex. 11, R-Car M3 Overview and Block Diagram ("• Dynamic Power Shutdown • AVS(Adaptive Voltage Scaling), DVFS(Dynamic Voltage and Frequency Scaling), DDR-SDRAM power supply backup mode"). "Power

management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." Ex. 12, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 15 Power Management. The Accused Renesas Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, Renesas devices activate a set of keep-alive instructions, in separate processing cores, such as low powered processing cores. The instructions provide an energy-conserving operation that utilizes keep-alive microprocessor circuitry, such as the LITTLE cores. *See* Ex. 13, Renesas Presentation, Automotive Linux Summit 2017, Power management for in-vehicle infotainment systems, slide 11. If detecting a power-up signal, the Accused Renesas Products power up to provide a main operation that utilizes main microprocessor circuitry, such as the Cortex-A57 MPCore, and a set of main operating instructions. *Id.* The Accused Renesas Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, if the Accused Renesas Products detect a power-down signal, such as a software instruction, they power down main Cortex-A57 processing cores (main microprocessor circuitry) while one of the low power Cortex-A53 cores (or a power manager or other low power core) remains alive. *Id.* In the Accused Renesas Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

59. On information and belief, Renesas has induced, and continues to induce, infringement of the '576 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly

inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

60. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

61. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

62. On information and belief, Renesas knew the '576 Patent existed, knew of an exemplary infringed claim of the '576 Patent, and knew of exemplary infringing Renesas products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '576 Patent.

COUNT VI: INFRINGEMENT OF THE '469 PATENT

63. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

64. On information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed, and continue to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States devices incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including the Accused Renesas Products identified in Exhibit A.

65. For example, on information and belief, the Renesas Defendants infringe at least Claim 14 of the '469 Patent by making, using, selling, or offering to sell in the United States, or

importing into the United States the Accused Renesas Products, such as the R-Car M3 SoC, SiP, and R-Car Starter Kits, which are computer systems. On information and belief, the Accused Renesas Products include a processor, such as the Cortex-A53/A57 MPCore processor or MPCore that boots the device. *See* Ex. 11, R-Car M3 Overview and Block Diagram. The Accused Renesas Products include a first memory accessible by said processor, such as the main system memory or LPDDR. *See id.* ("The R-Car M3 is available as a standalone chip and also as a system-in-package (SiP) module already mounted with DDR memory. The difficulty of designing a connection is increasing due to faster connection speeds between an SoC and DDR memory, or an increasing number of connection signals. The R-Car M3 SiP module offered by Renesas helps alleviate this design burden"). On information and belief, the Accused Renesas Products also include a second memory accessible only to said processor, wherein said second memory is internal to said processor. For example, Cortex-based processors include L2 cache which is internal to the Cortex MPCore processor, and accessible only to said processor. *See, e.g.*, Ex. 14, ARM Cortex-A53 MPCore Technical Reference Manual, Chapter 2.1 About the Cortex-A53 processor functions (illustrating L2 cache internal to the Cortex-A53 processor). On information and belief, in the Accused Renesas Products, power to said second memory is controlled separately from power to said processor and to said first memory. For example, on information and belief, the power domain for a Cortex-A53 processor is separated into a PDCPU<n> power domain for each core, a PLD2 power domain, and an overall PDCORTEXA53 power domain. *See* Ex. 15, ARM Cortex-A53 MPCore Technical Reference Manual, Chapter 2.4.1 Power domains. The power domain for the L2 cache, PDL2, is controlled separately from the PDCORTEXA53 power domain and separately from the individual PDCPU<n> core power domains. *Id. See also* Ex. 16, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 2.4.2 Power modes. Further, the PDL2 power domain is

controlled separately from power for the main system memory. *Id*. In the Accused Renesas Products, power is maintained to the second memory when power is removed from said processor. See, e.g., Ex. *Id.*, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 2.4.2 Power modes. In the Accused Renesas Products, the second memory maintains internal context of the processor when power is removed from said processor. For example, in "dormant" mode, where power is removed from the PDCORTEXA53 and PDCPU<n> power domains, the L2 cache RAMs are powered up and retain state. On information and belief, the Accused Renesas Products also include a third memory external to the processor and accessible only to the processor. For example, the Accused Renesas Products include a flash memory or ROM including boot code, which is external to the processor, and accessible only to the processor. Id. On information and belief, in the Accused Renesas Products, the power to the flash memory or ROM is controlled separately from power to the processor, and to the main system memory and to the L2 cache memory. *See id*. In another example, the Accused Renesas Products include a portion of a flash memory, the access to which is limited by, for example, TrustZone functionality, only to the A53/A57 MPCore processor. On information and belief, power to that flash memory, and the portion accessible only by the A53/A57 MPCore processor, is provided separately from the processor, the first memory (the main system memory or LPDDR), and the second memory (the corresponding L2 cache).

66. On information and belief, Renesas has induced, and continues to induce, infringement of the '469 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set

up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

67. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

68. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

69. On information and belief, Renesas knew the '469 Patent existed, knew of an exemplary infringed claim of the '469 Patent, and knew of exemplary infringing Renesas products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '469 Patent.

COUNT VII: INFRINGEMENT OF THE '330 PATENT

70. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

71. On information and belief, the Renesas Defendants have, individually, and jointly under control of Renesas-Japan, infringed, and continue to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States devices ARM Cortex-R and/or ARM Cortex-A architectures, including the Accused Renesas Products identified in Exhibit A.

72. For example, on information and belief, the Renesas Defendants infringe at least Claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused Renesas Products include a central processing unit, such as the Cortex-R4 CPU. *See* Ex. 17, RZ/T1 Microcontroller. On information and belief, CPUs in the Accused

Renesas Products execute several instruction sets, including ARM and Thumb instruction sets. *See* Ex. 18, RZ/T1 Important Notes for the Thumb Instruction Set. *See also* Ex. 19, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 1.2.1 ARM architecture (describing the "A32 instruction set," the "T32 instruction set," and the "A64 instruction set."). On information and belief, the Accused Renesas Products include one or more registers holding a state, such as the system and control registers. *See, e.g.*, Ex. 16. On information and belief, in the Accused Renesas Products, the CPU is adapted, upon executing a first instruction from the first instruction set (such as an instruction from a program in an ARM or Thumb instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save the state in a memory without executing any additional instructions from the first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs, such as ARM) (see, e.g., Ex. 16 at p. 7 ("Before entering Dormant mode the architectural state of the cluster, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")) and Ex. 18 ("The Cortex-R4 architecture is supposed to set the CPU operation mode to ARM instruction mode when an interrupt occurs after coming from a reset. Therefore, it's not possible to make a program using only the Thumb instruction set – even if you want to. In other words, you must make a program using both the ARM instruction set and the Thumb instruction set."), and (ii) to initiate an action that may cause the state of the registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which may result in registers having UNKNOWN values). *See, e.g.*, ARM Cortex-A53 MPCore Technical Reference Manual, Chapters 4.4-4.5. On information and belief, in the Accused Renesas Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from the first

instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is Thumb, instructions from ARM are executed upon exiting the dormant mode). *See* Ex. 18 ("The Cortex-R4 architecture is supposed to set the CPU operation mode to ARM instruction mode when an interrupt occurs after coming from a reset. Therefore, it's not possible to make a program using only the Thumb instruction set – even if you want to. In other words, you must make a program using both the ARM instruction set and the Thumb instruction set."). See *also*, Ex. 16 at p. 7 ("As part of the exit from Dormant mode to Normal state, the SoC must perform a Cold reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the cluster exits the Cold reset sequence, and the architectural state must be restored.").

73. On information and belief, Renesas has induced, and continues to induce, infringement of the '330 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Renesas website.

74. Upon information and belief, Renesas has committed the foregoing infringing activities without a license.

75. On information and belief, Renesas' infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

76. On information and belief, Renesas knew the '330 Patent existed, knew of an exemplary infringed claim of the '330 Patent, and knew of exemplary infringing Renesas products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '330 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Complex Memory prays for the judgment in its favor against the Renesas Defendants, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against the Renesas Defendants on all counts;

B. Entry of judgment that the Renesas Defendants have infringed the Patents-in-Suit;

C. Entry of judgment that the Renesas Defendants' infringement of the Patents-in-Suit has been willful;

D. Award of compensatory damages adequate to compensate Complex Memory for the Renesas Defendants' infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Declaration and finding that the Renesas Defendants' conduct in this case is exceptional under 35 U.S.C. § 285;

F. Award of reasonable attorneys' fees and expenses against the Renesas Defendants pursuant to 35 U.S.C. § 285;

G. Award of Complex Memory's costs;

H. Pre-judgment and post-judgment interest on Complex Memory's award; and

I. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff Complex Memory hereby demands trial by jury in this action of all claims so triable.

Dated: July 10, 2018

Respectfully submitted,

/s/ Dmitry Kheyfits

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