IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

COMPLEX MEMORY, LLC, Plaintiff v. MOTOROLA MOBILITY LLC Defendant	Civil Action No.: 1:18-cv-6255 **PATENT CASE** **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Complex Memory, LLC ("Complex Memory"), by way of this Complaint against Defendant Motorola Mobility LLC ("Motorola" or "Defendant"), alleges as follows:

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 17330 Preston Road, Suite 200D, Dallas, Texas 75252.

2. On information and belief, Defendant Motorola is a Delaware limited liability company headquartered at 222 W. Merchandise Mart Plaza, Chicago, IL 60654.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq.*, for infringement by Motorola of claims of U.S. Patent Nos. 5,890,195; 5,963,481; 6,658,576; 6,968,469; and 7,730,330 ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. Motorola is subject to personal jurisdiction of this Court because, *inter alia*, on

information and belief, (i) Motorola is registered to transact business in the State of Illinois; (ii) Motorola conducts business in the State of Illinois and maintains a facility and employees within the State of Illinois; and (iii) Motorola has committed and continues to commit acts of patent infringement in the State of Illinois, including by making, using, offering to sell, and/or selling accused products and services in the State of Illinois, and/or importing accused products and services into the State of Illinois.

6. Venue is proper as to Motorola in this district under 28 U.S.C. § 1400(b) because, *inter alia*, on information and belief, Motorola has a regular and established place of business in this district and has committed and continues to commit acts of patent infringement in the State of Illinois, including by making, using, offering to sell, and/or selling accused products and services into the State of Illinois, and/or importing accused products and services into the State of Illinois.

BACKGROUND

7. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM." A copy of the '195 Patent is attached as Exhibit A.

8. G.R. Mohan Rao invented the technology claimed in the '195 Patent.

9. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 ("the '481 Patent"), entitled "Embedded Enhanced DRAM, And Associated Method." A copy of the '481 Patent is attached as Exhibit B.

10. Michael Alwais and Michael Peters invented the technology claimed in the '481 Patent.

11. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 ("the '576 Patent"), entitled "Energy-Conserving

Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction." A copy of the '576 Patent is attached as Exhibit C.

12. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

13. On November 22, 2005, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,968,469 ("the '469 Patent"), entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored." A copy of the '469 Patent is attached as Exhibit D.

14. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '469 Patent.

15. On June 1, 2010, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,730,330 ("the '330 Patent"), entitled "System and Method For Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set." A copy of the '330 Patent is attached as Exhibit E.

16. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '330 Patent.

17. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

18. By letter dated May 18, 2018, Complex Memory notified Motorola of the existence of the Patents-in-Suit, and of infringement thereof by Motorola and its customers. Complex Memory's

letter identified exemplary infringing Motorola products and an exemplary infringed claim for each of the Patents-in-Suit.

19. By email dated June 13, 2018, Motorola acknowledged receipt of Complex Memory's May 18, 2018 letter.

20. Accordingly, Motorola has received notice of the Patents-in-Suit and of infringement thereof by Motorola and its customers.

COUNT I: INFRINGEMENT OF THE '195 PATENT

21. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

22. Upon information and belief, Motorola has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States mobile devices, such as smart phones, incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including Qualcomm Snapdragon, Kryo and Krait devices, including the devices identified in Attachment A ("Accused Motorola Products").

23. For example, on information and belief, Motorola has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. For example, on information and belief, the Motorola G5 Plus smartphone includes a Qualcomm Snapdragon 625 System-on-Chip ("SoC"), based on ARM Cortex-A53 architecture, which includes L1 and L2 cache memories having a plurality of registers and a memory array. *See* Ex. 1, Moto G5 Plus (retrieved from www.motorola.com/us/products/moto-g-plus) and Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. In performing the method of claim 6, processors in the Accused

Motorola Products receive an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller) or an address channel of a bus. Accused Motorola Products compare the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When [the cache controller] receives a request from the core, it must check to see whether the requested address is to be found in the cache. This is known as a *cache look-up*. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." Ex. 3, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller. When a match between the received address and a matching address stored in one of the latches occurs, the Accused Motorola Products perform the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match, known as a hit, and the line is marked valid, then the read or write occurs the cache memory." *Id.* When a match between the received address and an address stored in one of the latches does not occur, the Accused Motorola Products perform the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "If the address is not found in the L1 cache but is in the L2 cache, then the cache line is loaded into the L1 cache from the L2 cache and the data is returned to the core. . . . If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 cache from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3. Inclusive and exclusive caches. When the match does not occur, the Accused Motorola Products further store the received address in one of the latches corresponding to the selected register. For example, the Accused Motorola Products store the received address, such as the

tag, corresponding to the register being accessed, in the cache memory system latches, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches. *See, e.g.*, Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. The Accused Motorola Products further modify the received address to generate a modified address. For example, the hardware autoprefetcher in the Accused Motorola Products prefetches data or instructions stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 6.6.2 Data prefetching and monitoring ("When a pattern is detected, the automatic prefetcher starts linefills in the background"). *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher. "[P]refetch address = current address + (stride x programmed distance)." On information and belief, the Accused Motorola Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused Motorola Products further exchange data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 caches from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3 Inclusive and exclusive caches. The Accused Motorola Products then store the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stores the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current

TAG, set, index, and way register latches.

24. On information and belief, Motorola has committed the foregoing infringing activities without a license.

25. On information and belief, Motorola's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

COUNT II: INFRINGEMENT OF THE '576 PATENT

26. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

27. Upon information and belief, Motorola has infringed, and continues to infringe, the '576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States mobile devices, such as smart phones, incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including Qualcomm Snapdragon, Kryo and Krait devices, including the Accused Motorola Products identified in Attachment A.

28. For example, on information and belief, Motorola has infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. For example, on information and belief, the Moto G5 Plus smartphone includes a Qualcomm Snapdragon 625 System-on-Chip ("SoC"), based on ARM Cortex-A53 architecture. *See* Ex. 1, Moto G5 Plus (retrieved from www.motorola.com/us/products/moto-g-plus) and Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet. "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." Ex. 7, ARM

Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 15 Power Management. The Accused Motorola Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, the Accused Motorola Products activate a set of interrupt-handling instructions for the generic interrupt controller in connection with handling an interrupt in a standby mode, caused by, among others, the issuance of the WFI (wait for interrupt) instruction executed by a core. *See, e.g.*, Ex. 8, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 10.6 The Generic Interrupt Controller. If detecting a power-up signal, the Accused Motorola Products power up to provide a main operation that utilizes main microprocessor circuitry and a set of main operating instructions. For example, when the main microprocessor circuitry, such as a core, is in the WFI low power state, an interrupt is detected by the generic interrupt controller, followed by powering up, such as enabling various clocks, to provide the main operation that utilizes that core and a set of main operating instructions, such as the instructions of the executed code following the WFI instruction. "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the PSTATE I-bit is set. • An FIQ interrupt, even if the PSTATE F-bit is set. • An asynchronous abort. In the event of the core being woken by an interrupt when the relevant PSTATE interrupt flag is disabled, the core implements the next instruction after WFI." Ex. 9, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 15.3 Assembly language power instructions. The Accused Motorola Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, in the regular operating state, a WFI instruction detected by a core is a power-down signal. "Software indicates that the core can enter the WFI low-power

state by executing the WFI instruction." Ex. 10, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Section 2.4.2 Power modes. If the WFI command is detected, the operating system places the system in the low-power WFI mode. "Wait for Interrupt is a feature of the ARMv8-A architecture that puts the core in a low-power state by disabling most of the clocks in the core while keeping the core powered up. Apart from a small dynamic power overhead on the logic to enable the core to wake up from WFI low-power state, this reduces the power drawn to static leakage current only." *Id.* In the Accused Motorola Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

29. On information and belief, Motorola has induced, and continues to induce, infringement of the '576 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Motorola Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as user manuals, "how to" instructions, and other technical documentation available on the Motorola website.

30. On information and belief, Motorola has committed and continues to commit the foregoing infringing activities without a license.

31. On information and belief, Motorola's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

32. On information and belief, Motorola knew the '576 Patent existed, knew of its claims, and knew of Motorola's infringing products while committing the foregoing infringing acts,

thereby willfully, wantonly, and deliberately infringing the '576 Patent.

COUNT III: INFRINGEMENT OF THE '481 PATENT

33. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

34. On information and belief, Motorola has infringed the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States mobile devices, such as smart phones, incorporating DDRxL and/or LPDDRx memories, including the Accused Motorola Products identified in Attachment A.

35. For example, on information and belief, Motorola has infringed at least claim 16 of the '481 Patent by performing a method of accessing data. Specifically, on information and belief, the Accused Motorola Products include LPDDR memory. *See, e.g.*, Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet ("Memory + LPDDR3"). For example, LPDDR3 memory included in Motorola products is a memory system comprising multiple banks with multiple rows. *See, e.g.*, Ex. 11, *LPDDR3 Standard, JEDEC JSD209-3C* at p. 16 ("LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory."). The Accused Motorola Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id.* ("Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access."). In Motorola's LPDDR3

memory, the memory locations of the first memory row are disposed upon a substrate. *Id.* ("LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory."). *See also* Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet ("The First 14nm 600-tier Snapdragon Processor). The Accused Motorola Products access the data stored at the memory locations identified in the first access request. *Id.* While the data stored at the memory locations identified by the first access request is being accessed, the Accused Motorola Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a seamless burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See, e.g., id.* at p. 49 ("After READ with AP, seamless read operations to different banks are supported.") (Ex. 12). *See also id.* at p. 45 ("The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.") (Ex. 13). In the Accused Motorola Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet ("The First 14nm 600-tier Snapdragon Processor). The Accused Motorola Products also access the data stored at the memory locations identified in the second access request. *Id.*

36. On information and belief, Motorola has induced, and continues to induce, infringement of the '481 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Motorola Products by, among other things,

providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as user manuals, "how to" instructions, and other technical documentation available on the Motorola website.

37. On information and belief, Motorola has committed and continues to commit the foregoing infringing activities without a license.

38. On information and belief, Motorola's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

39. On information and belief, Motorola knew the '481 Patent existed, knew of its claims, and knew of Motorola's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '481 Patent.

COUNT IV: INFRINGEMENT OF THE '469 PATENT

40. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

41. On information and belief, Motorola has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States mobile devices, such as smart phones, incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including Qualcomm Snapdragon, Kryo and Krait devices, including the Accused Motorola Products identified in Attachment A.

42. For example, on information and belief, Motorola infringes at least Claim 14 of the '469 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused Motorola Products, which are computer systems. On information and belief, the Accused Motorola Products include a processor, such as the Qualcomm Snapdragon 625 processor in the Moto G5 Plus smartphone. *See* Ex. 1, Moto G5 Plus (retrieved from

www.motorola.com/us/products/moto-g-plus). On information and belief, the Snapdragon 625 processor includes Cortex-A53 cores, and additional cores based on ARM Cortex architecture. *See, e.g.,* Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet. The Accused Motorola Products include a first memory accessible by said processor, such as the main system memory or LPDDR. *Id.* On information and belief, the Accused Motorola Products also include a second memory accessible only to said processor, wherein said second memory is internal to said processor. For example, Cortex-based processors include L2 cache which is internal to the Cortex processor, and accessible only to said processor. *See, e.g.,* Ex. 15, ARM Cortex-A53 MPCore Technical Reference Manual, Chapter 2.1 About the Cortex-A53 processor functions (illustrating L2 cache internal to the Cortex-A53 processor). *See also* Ex. 16, ARM Cortex-A53 MPCore Technical Reference Manual, Chapter 7.3.3 Snoop channel properties ("The SCU can accept and process a maximum of eight snoop requests from the system"). On information and belief, in the Accused Motorola Products, power to said second memory is controlled separately from power to said processor and to said first memory. For example, on information and belief, the power domain for a Cortex-A53 processor is separated into a PDCPU<n> power domain for each core, a PLD2 power domain, and an overall PDCORTEXA53 power domain. *See* Ex. 17, ARM Cortex-A53 MPCore Technical Reference Manual, Chapter 2.4.1 Power domains. The power domain for the L2 cache, PDL2, is controlled separately from the PDCORTEXA53 power domain and separately from the individual PDCPU<n> core power domains. *Id. See also* Ex. 19, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 2.4.2 Power modes. Further, the PDL2 power domain is controlled separately from power for the main system memory. *Id.* In the Accused Motorola Products, power is maintained to the second memory when power is removed from said processor. *See, e.g.,* Ex. 19, ARM Cortex-A53

MPCore Processor Technical Reference Manual, Chapter 2.4.2 Power modes. In the Accused Motorola Products, the second memory maintains internal context of the processor when power is removed from said processor. For example, in "dormant" mode, where power is removed from the PDCORTEXA53 and PDCPU<n> power domains, the L2 cache RAMs are powered up and retain state. On information and belief, the Accused Motorola Products also include a third memory external to the processor and accessible only to the processor. For example, the Accused Motorola Products include a flash memory or ROM including boot code, which is external to the processor, and accessible only to the processor. *Id.* On information and belief, in the Accused Motorola Products, the power to the flash memory or ROM is controlled separately from power to the processor, and to the main system memory and to the L2 cache memory. *See id.* In another example, the Accused Motorola Products include a portion of a flash memory, the access to which is limited by, for example, TrustZone functionality, only to the A53 MPCore processor. On information and belief, power to that flash memory, and the portion accessible only by the A53 MPCore processor, is provided separately from the processor, the first memory (the main system memory or LPDDR), and the second memory (the corresponding L2 cache).

43. On information and belief, Motorola has induced, and continues to induce, infringement of the '469 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Motorola Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as user manuals, "how to" instructions, and other technical documentation available on the Motorola website.

44. On information and belief, Motorola has committed and continues to commit the foregoing infringing activities without a license.

45. On information and belief, Motorola's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

46. On information and belief, Motorola knew the '469 Patent existed, knew of its claims, and knew of Motorola's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '469 Patent.

COUNT V: INFRINGEMENT OF THE '330 PATENT

47. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

48. On information and belief, Motorola has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States mobile devices, such as smart phones, incorporating ARM Cortex-A53 and other ARM Cortex-A architectures, including Qualcomm Snapdragon, Kryo and Krait devices, including the Accused Motorola Products identified in Attachment A.

49. For example, on information and belief, Motorola infringes at least Claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused Motorola Products include a central processing unit, such as the Qualcomm Snapdragon 625 CPU in the Moto G5 Plus smartphone. *See* Ex. 1, Moto G5 Plus (retrieved from www.motorola.com/us/products/moto-g-plus). On information and belief, the Snapdragon 625 processor includes Cortex-A53 cores, and additional cores based on ARM Cortex architecture.

See, e.g., Ex. 14, Qualcomm Snapdragon 625 Processor Datasheet. On information and belief, CPUs in the Accused Motorola Products execute the "A32 instruction set," the "T32 instruction set," and the "A64 instruction set." Ex. 18, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 1.2.1 ARM architecture. On information and belief, the Accused Motorola Products include one or more registers holding a state, such as the system and control registers. *See, e.g.*, Ex. 19, ARM Cortex-A53 MPCore Processor Technical Reference Manual, Chapter 2.4.2 Power modes. On information and belief, in the Accused Motorola Products, the CPU is adapted, upon executing a first instruction from the first instruction set (such as an instruction from a program in an A32, T32, or A64 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save the state in a memory without executing any additional instructions from the first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs, such as A64) (*see, e.g.*, Ex. 19 at p. 7 ("Before entering Dormant mode the architectural state of the cluster, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")), and (ii) to initiate an action that may cause the state of the registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which may result in registers having UNKNOWN values). *See, e.g.*, ARM Cortex-A53 MPCore Technical Reference Manual, Chapters 4.4-4.5. On information and belief, in the Accused Motorola Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from the first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example,

by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). *See, e.g.*, Ex. 19 at p. 7 ("As part of the exit from Dormant mode to Normal state, the SoC must perform a Cold reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the cluster exits the Cold reset sequence, and the architectural state must be restored."). In further addition, the Snapdragon SoC is similarly adapted when removing power from the GPU cores.

50. On information and belief, Motorola has induced, and continues to induce, infringement of the '330 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Motorola Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as user manuals, "how to" instructions, and other technical documentation available on the Motorola website.

51. On information and belief, Motorola has committed and continues to commit the foregoing infringing activities without a license.

52. On information and belief, Motorola's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

53. On information and belief, Motorola knew the '330 Patent existed, knew of its claims, and knew of Motorola's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '330 Patent.

PRAYER FOR RELIEF

WHEREFORE, Complex Memory prays for the judgment in its favor against Motorola, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against Motorola on all counts;

B. Entry of judgment that Motorola has infringed the Patents-in-Suit;

C. Entry of judgment that Motorola's infringement of the Patents-in-Suit has been willful;

D. Award of compensatory damages adequate to compensate Complex Memory for Motorola's infringement of the Patents-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Complex Memory's costs;

F. Pre-judgment and post-judgment interest on Complex Memory's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. Proc., Plaintiff hereby demands trial by jury in this action of all claims so triable.

Dated: September 13, 2018

Respectfully submitted,

/s/ David R. Bennett

David R. Bennett
Direction IP Law
P.O. Box 14184
Chicago, IL 60614-0184
Telephone: (312) 291-1667
e-mail: dbennett@directionip.com

Attorneys for Plaintiff Complex Memory, LLC

Of Counsel
Dmitry Kheyfits
(*Pro Hac Vice* motion to be filed)
California State Bar No. 321326
dkheyfits@kblit.com
KHEYFITS BELENKY LLP

4 Embarcadero Center, Suite 1400
San Francisco, CA 94111
Tel: 415-429-1739
Fax: 415-429-6347

Andrey Belenky
(*Pro Hac Vice* motion to be filed)
New York State Bar No. 4524898
abelenky@kheyfits.com
Hanna G. Cohen
(*Pro Hac Vice* motion to be filed)
hgcohen@kheyfits.com
New York State Bar No. 4471421
KHEYFITS BELENKY LLP
1140 Avenue of the Americas
9th Floor
New York, New York 10036
Tel. (212) 203-5399
Fax. (212) 203-6445