IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHEN DISTRICT OF TEXAS
DALLAS DIVISION

SUPER INTERCONNECT TECHNOLOGIES LLC,	§ § § § §	
		JURY TRIAL DEMANDED
Plaintiff,		
v.	§ § §	**CIVIL ACTION NO. _____**
ZTE CORPORATION AND ZTE USA, INC.,	§ § §	
Defendants.	§ § §	

PLAINTIFF'S ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Super Interconnect Technologies LLC ("Super Interconnect") files this Original Complaint against ZTE Corporation and ZTE USA, Inc. (collectively, "ZTE") for infringement of U.S. Patent No. 7,627,044 ("the '044 patent"), U.S. Patent No. 6,463,092 ("the '092 patent"), and U.S. Patent No. 7,158,593 ("the '593 patent").

THE PARTIES

1.   Super Interconnect Technologies LLC is a Texas limited liability company, located at 1701 Directors Blvd., Suite 300, Austin, Texas 78744.

2.   On information and belief, ZTE Corporation is a corporation existing under the laws of China with its principal place of business at ZTE Plaza, Keji Road South, Hi-tech Industrial Park Nanshan, Shenzhen, Guangdong, 518057, China.

3.   On information and belief, ZTE USA, Inc. is a corporation organized under the laws of New Jersey with its principal place of business located at 2425 North Central Expressway, Suite 800, Richardson, TX 75080. ZTE USA, Inc. may be served through its registered agent, Incorp

Services, Inc., 815 Brazos, Suite 500, Richardson, TX 78701. On information and belief, ZTE

USA, Inc. is a wholly-subsidiary of ZTE Corporation.

JURISDICTION AND VENUE

4.   This action arises under the patent laws of the United States, namely 35 U.S.C. §§

271, 281, and 284-285, among others.

5.   This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6.   Venue is proper in this judicial district as to ZTE Corporation because it is a foreign

entity that may be sued in any judicial district under 28 U.S.C. § 1391(c).

7.   Venue is proper in this judicial district as to ZTE USA, Inc. under 28 U.S.C. §

1400(b) because ZTE USA, Inc. has committed acts of infringement in this District and has a

regular and established place of business in this District, located at 2425 North Central

Expressway, Suite 800, Richardson, TX 75080.

8.   ZTE is subject to personal jurisdiction pursuant to due process due at least to its

substantial business in this State, including: (A) at least part of its infringing activities alleged

herein; and (B) regularly doing or soliciting business, engaging in other persistent conduct, and/or

deriving substantial revenue from goods sold and services provided to Texas residents. ZTE has

conducted and regularly conducts business within the United States and this District. ZTE has

purposefully availed itself of the privileges of conducting business in the United States, and more

specifically in Texas and this District. ZTE has sought protection and benefit from the laws of the

State of Texas by placing infringing products into the stream of commerce through an established

distribution channel with the awareness and/or intent that they will be purchased by consumers in

this District.

9.   On information and belief, ZTE has significant ties to, and presence in, this District, making venue in this judicial district both proper and convenient for this action.

COUNT I
(INFRINGEMENT OF U.S. PATENT NO. 7,627,044)

10.   Super Interconnect incorporates paragraphs 1 through 9 herein by reference.

11.   Super Interconnect is the assignee of the '044 patent, entitled "Clock-Edge Modulated Serial Link with DC-Balance Control," with ownership of all substantial rights in the '044 patent, including the right to exclude others and to enforce, sue, and recover damages for past and future infringement. A true and correct copy of the '044 patent is attached as Exhibit A.

12.   The '044 patent is valid, enforceable, and was duly issued in full compliance with Title 35 of the United States Code. The '044 patent issued from U.S. Patent Application No. 11/264,303.

13.   To the extent any marking or notice was required by 35 U.S.C. § 287, Super Interconnect and all predecessors-in-interest to the '044 patent have complied with the requirements of that statute by providing actual or constructive notice to ZTE of its alleged infringement.

14.   ZTE has and continues to directly and/or indirectly infringe (by inducing infringement and/or contributing to infringement) one or more claims of the '044 patent in this judicial district and elsewhere in the United States, including at least claims 1, 2, 8, 9, 10, 11, 12, 13, 14, 15 and 19, by, among other things, making, having made, using, offering for sale, selling, and/or importing electronic devices with Universal Flash Storage (UFS) that incorporate the fundamental technologies covered by the '044 patent. These products are referred to as the "'044 Accused Products." Examples of the '044 Accused Products include, but are not limited to, the Axon 7 smartphone.

15.   For example, the ZTE Axon 7 directly infringes claim 1 of the '044 patent, as shown in the below paragraphs.

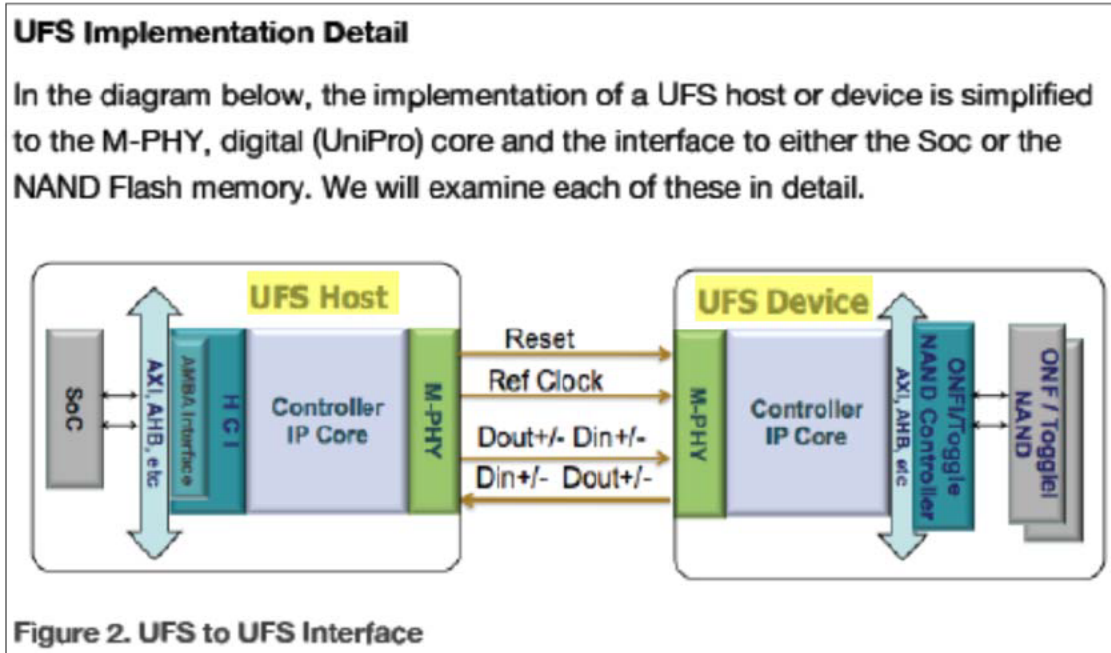16.   An example of the ZTE Axon 7 is shown in the image below.

17.   ZTE incorporates UFS 2.0 storage in the Axon 7, as shown in the image below.

http://newst8.com/specifications/zte-axon-7-full-specification-and-features-8520852025

18.   The citations below show that the ZTE Axon 7's UFS storage uses the MIPI M-PHY protocol for physical layer communication between the UFS host and the UFS device.

UFS Implementation Detail

In the diagram below, the implementation of a UFS host or device is simplified to the M-PHY, digital (UniPro) core and the interface to either the Soc or the NAND Flash memory. We will examine each of these in detail.

Figure 2. UFS to UFS Interface

Arasan Chip Systems Inc. White Paper, "Universal Flash Storage: Mobilize Your Data" at 6 (Oct. 2012).

M-PHY I/O

MIPI defines two types of M-PHY, type 1 and type 2. The UFS specification calls out type 1. M-PHY Type 1 uses NRZ signaling for HS and PWM signaling for LS, while type 2 uses NRZ signaling for both HS and LS.

UFS utilizes two speed modes, high-speed and low-speed. Low speed mode In Gear 1 is used upon power up or reset, then a transition occurs to high-speed gears for data transmission. The low speed gears and high-speed gears are listed here for your reference. UFS v1.1 has been ratified and supports HS Gear 2 running approximately @ 3Gbps per lane. The UFS spec also supports up to 4 lanes for higher throughput.

Id.

19.   UFS hosts and devices, which are included in the '044 Accused Products, contain signal transmitters. These signal transmitters drive a DC-balanced differential signal for a communications channel. This signal is comprised of a pair of data signals: a positive (true) data signal and a negative (complement) data signal. These transmitters multiplex a pulse-width modulated clock signal, a data signal, and control signals to apply them to the communications channel.

20.   The '044 Accused Products thus include each and every limitation of claim 1 of the '044 patent; accordingly, they literally infringe this claim. ZTE directly infringes the '044 patent by making, using, offering to sell, selling, and/or importing the '044 Accused Products. ZTE is thereby liable for direct infringement.

21.   During discovery and development of its infringement contentions, Plaintiff may provide additional theories under which ZTE infringes the '044 patent besides the example provided above, including for the same product and using the same components identified above, and nothing in the example above is meant to limit the infringement allegations of Plaintiff or limit the interpretations of the claims or their terms.

22.   At a minimum, ZTE has known that the '044 Accused Products infringe the '044 patent at least as early as the service date of this Original Complaint.

23.   Upon information and belief, since at least the above-mentioned date when ZTE was on notice of its infringement, ZTE has actively induced, under U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers that purchase or sell the '044 Accused Products that include all of the limitations of one or more claims of the '044 patent to directly infringe one or more claims of the '044 patent by making, having made, using, offering for sale, selling, and/or importing the '044 Accused Products. Since at least the notice provided on the above-mentioned date, ZTE does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the '044 patent. Upon information and belief, ZTE intends to cause, and has taken affirmative steps to induce, infringement by these third-party manufacturers, distributors, importers, and/or consumers by, inter alia, creating advertisements that promote the infringing use of the '044 Accused Products, creating established distribution channels for the '044 Accused Products into and within the United States, manufacturing the '044

Accused Products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States. For example, ZTE advertises, provides support for, and publishes a user manual for the Axon 7 on its own website at the following web address: https://www.zteusa.com/axon-7.

24.   Super Interconnect has been damaged as a result of ZTE's infringing conduct described in this Count. ZTE is, thus, liable to Super Interconnect in an amount that adequately compensates Super Interconnect for ZTE's infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II
(INFRINGEMENT OF U.S. PATENT NO. 6,463,092)

25.   Super Interconnect incorporates paragraphs 1 through 24 herein by reference.

26.   Super Interconnect is the assignee of the '092 patent, entitled "System and Method for Sending and Receiving Data Signals Over A Clock Signal Line," with ownership of all substantial rights in the '092 patent, including the right to exclude others and to enforce, sue, and recover damages for past and future infringement. A true and correct copy of the '092 patent is attached as Exhibit B.

27.   The '092 patent is valid, enforceable, and was duly issued in full compliance with Title 35 of the United States Code. The '092 patent issued from U.S. Patent Application No. 09/393,235.

28.   To the extent any marking or notice was required by 35 U.S.C. § 287, Super Interconnect and all predecessors-in-interest to the '092 patent have complied with the requirements of that statute by providing actual or constructive notice to ZTE of its alleged infringement.

29.   ZTE has and continues to directly and/or indirectly infringe (by inducing infringement and/or contributing to infringement) one or more claims of the '092 patent in this judicial district and elsewhere in the United States, including at least claims 1, 2, 5, 10, and 11 by, among other things, making, having made, using, offering for sale, selling, and/or importing electronic devices with Universal Flash Storage (UFS) that incorporate the fundamental technologies covered by the '092 patent. These products are referred to as the "'092 Accused Products." Examples of the '092 Accused Products include, but are not limited to, the ZTE Axon 7 smartphone.

30.   For example, the ZTE Axon 7 directly infringes claim 1 of the '092 patent, as shown in the below paragraphs.

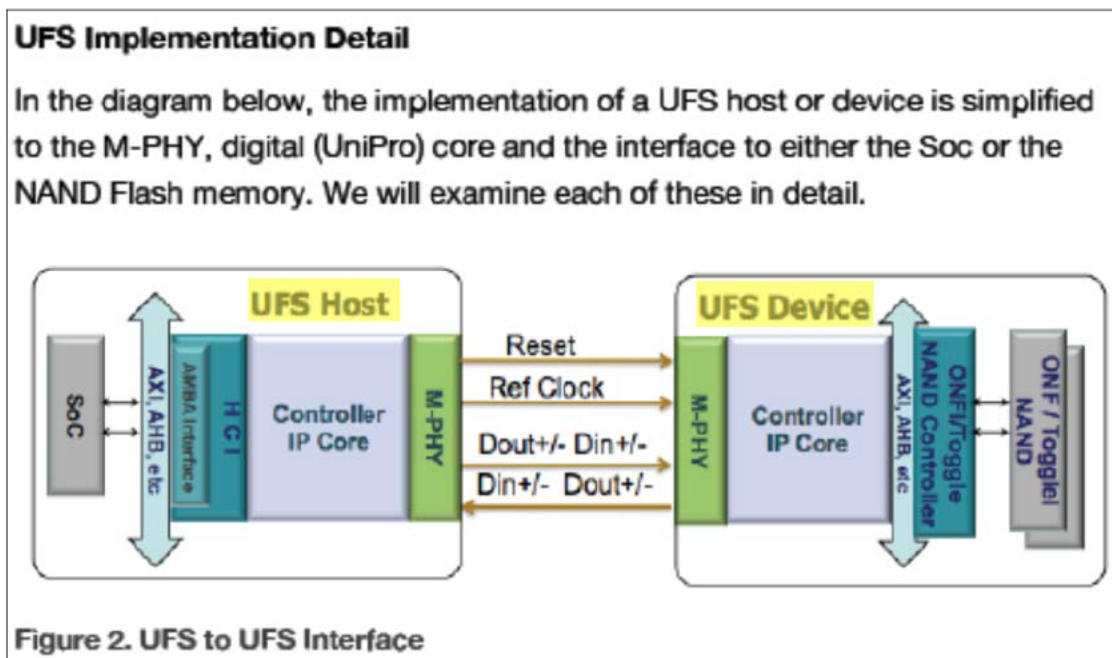31.   An example of the ZTE Axon 7 is shown in the image below.

32.   ZTE incorporates UFS 2.0 storage in the Axon 7, as shown in the image below.

Memory	
Internal Memory (ROM)	− 64 GB (4 GB RAM) − 128 GB (6 GB RAM)
Internal Storage Type	UFS 2.0 (Universal Flash Storage)

http://newst8.com/specifications/zte-axon-7-full-specification-and-features-8520852025

33. The images below show that the ZTE Axon 7's UFS storage uses the MIPI M-PHY protocol for physical layer communication between the UFS host and the UFS device.

UFS Implementation Detail

In the diagram below, the implementation of a UFS host or device is simplified to the M-PHY, digital (UniPro) core and the interface to either the Soc or the NAND Flash memory. We will examine each of these in detail.

Figure 2. UFS to UFS Interface

Arasan Chip Systems Inc. White Paper, "Universal Flash Storage: Mobilize Your Data" at 6 (Oct. 2012).

M-PHY I/O

MIPI defines two types of M-PHY, type 1 and type 2. The UFS specification calls out type 1. M-PHY Type 1 uses NRZ signaling for HS and PWM signaling for LS, while type 2 uses NRZ signaling for both HS and LS.

UFS utilizes two speed modes, high-speed and low-speed. Low speed mode In Gear 1 is used upon power up or reset, then a transition occurs to high-speed gears for data transmission. The low speed gears and high-speed gears are listed here for your reference. UFS v1.1 has been ratified and supports HS Gear 2 running approximately @ 3Gbps per lane. The UFS spec also supports up to 4 lanes for higher throughput.

Id.

34. UFS hosts and devices, which are included in the '092 Accused Products, multiplex clock and data signals for transmission over a single communications channel. This clock signal is modulated based on the data to be transmitted before being combined with the output data stream.

35.   The '092 Accused Products thus include each and every limitation of claim 1 of the '092 patent; accordingly, they literally infringe this claim. ZTE directly infringes the '092 patent by making, using, offering to sell, selling, and/or importing the '092 Accused Products. ZTE is thereby liable for direct infringement.

36.   During discovery and development of its infringement contentions, Plaintiff may provide additional theories under which ZTE infringes the '092 patent besides the example provided above, including for the same product and using the same components identified above, and nothing in the example above is meant to limit the infringement allegations of Plaintiff or limit the interpretations of the claims or their terms.

37.   At a minimum, ZTE has known that the '092 Accused Products infringe the '092 patent at least as early as the service date of this Original Complaint.

38.   Upon information and belief, since at least the above-mentioned date when ZTE was on notice of its infringement, ZTE has actively induced, under U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers that purchase or sell the '092 Accused Products that include all of the limitations of one or more claims of the '092 patent to directly infringe one or more claims of the '092 patent by making, having made, using, offering for sale, selling, and/or importing the '092 Accused Products. Since at least the notice provided on the above-mentioned date, ZTE does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the '092 patent. Upon information and belief, ZTE intends to cause, and has taken affirmative steps to induce, infringement by these third-party manufacturers, distributors, importers, and/or consumers by, inter alia, creating advertisements that promote the infringing use of the '092 Accused Products, creating established distribution channels for the '092 Accused Products into and within the United States, manufacturing the '092

Accused Products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States. For example, ZTE advertises, provides support for, and publishes a user manual for the Axon 7 on its own website at the following web address: https://www.zteusa.com/axon-7.

39. Super Interconnect has been damaged as a result of ZTE's infringing conduct described in this Count. ZTE is, thus, liable to Super Interconnect in an amount that adequately compensates Super Interconnect for ZTE's infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III
(INFRINGEMENT OF U.S. PATENT NO. 7,158,593)

40. Super Interconnect incorporates paragraphs 1 through 39 herein by reference.

41. Super Interconnect is the assignee of the '593 patent, entitled "Combining a Clock Signal and a Data Signal," with ownership of all substantial rights in the '593 patent, including the right to exclude others and to enforce, sue, and recover damages for past and future infringement. A true and correct copy of the '593 patent is attached as Exhibit C.

42. The '593 patent is valid, enforceable, and was duly issued in full compliance with Title 35 of the United States Code. The '593 patent issued from U.S. Patent Application No. 10/099,533.

43. To the extent any marking or notice was required by 35 U.S.C. § 287, Super Interconnect and all predecessors-in-interest to the '593 patent have complied with the requirements of that statute by providing actual or constructive notice to ZTE of its alleged infringement.

44. ZTE has and continues to directly and/or indirectly infringe (by inducing infringement and/or contributing to infringement) one or more claims of the '593 patent in this judicial district and elsewhere in the United States, including at least claims 34 and 35, by, among other things, making, having made, using, offering for sale, selling, and/or importing electronic devices with Universal Flash Storage (UFS) that incorporate the fundamental technologies covered by the '593 patent. These products are referred to as the "'593 Accused Products." Examples of the '593 Accused Products include, but are not limited to, the ZTE Axon 7 smartphone.

45. The ZTE Axon 7 directly infringes claim 34 of the '593 patent, as shown in the below paragraphs.

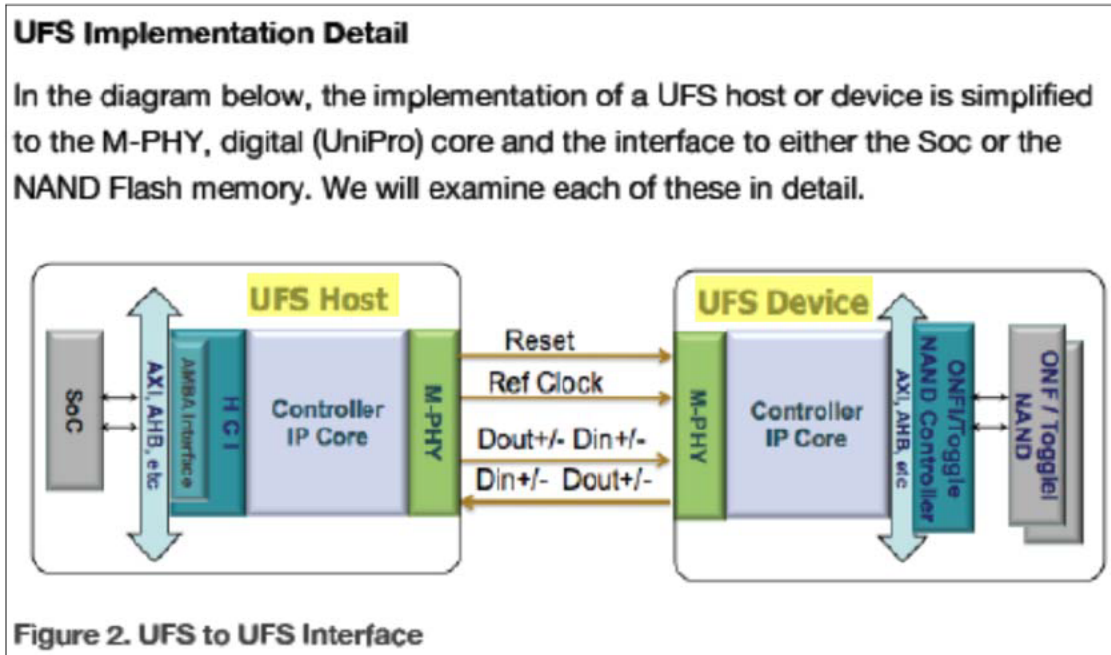46. An example of the ZTE Axon 7 is shown in the image below.

47. ZTE incorporates UFS 2.0 storage in the Axon 7, as shown in the image below.

Memory	
Internal Memory (ROM)	— 64 GB (4 GB RAM) — 128 GB (6 GB RAM)
Internal Storage Type	UFS 2.0 (Universal Flash Storage)

http://newst8.com/specifications/zte-axon-7-full-specification-and-features-8520852025

48.   The images below show that the ZTE Axon 7's UFS storage uses the MIPI M-PHY protocol for physical layer communication between the UFS host and the UFS device.

UFS Implementation Detail

In the diagram below, the implementation of a UFS host or device is simplified to the M-PHY, digital (UniPro) core and the interface to either the Soc or the NAND Flash memory. We will examine each of these in detail.

Figure 2. UFS to UFS Interface

Arasan Chip Systems Inc. White Paper, "Universal Flash Storage: Mobilize Your Data" at 6 (Oct. 2012).

M-PHY I/O

MIPI defines two types of M-PHY, type 1 and type 2. The UFS specification calls out type 1. M-PHY Type 1 uses NRZ signaling for HS and PWM signaling for LS, while type 2 uses NRZ signaling for both HS and LS.

UFS utilizes two speed modes, high-speed and low-speed. Low speed mode In Gear 1 is used upon power up or reset, then a transition occurs to high-speed gears for data transmission. The low speed gears and high-speed gears are listed here for your reference. UFS v1.1 has been ratified and supports HS Gear 2 running approximately @ 3Gbps per lane. The UFS spec also supports up to 4 lanes for higher throughput.

Id.

49.   UFS hosts and devices, which are included in the '593 Accused Products, contain signal transmitters. These transmitters encode the data to be transmitted and further multiplex a pulse-width modulated clock signal, an encoded data signal, and control signals to apply them to

the communications channel. This encoding scheme shifts an energy spectrum of the combined clock and encoded data signal away from an effective loop bandwidth of a clock recovery block.

50.   The '593 Accused Products thus include each and every limitation of claim 34 of the '593 patent; accordingly, they literally infringe this claim. ZTE directly infringes the '593 patent by making, using, offering to sell, selling, and/or importing the '593 Accused Products. ZTE is thereby liable for direct infringement.

51.   During discovery and development of its infringement contentions, Plaintiff may provide additional theories under which ZTE infringes the '593 patent besides the example provided above, including for the same product and using the same components identified above, and nothing in the example above is meant to limit the infringement allegations of Plaintiff or limit the interpretations of the claims or their terms.

52.   At a minimum, ZTE has known that the '593 Accused Products infringe the '593 patent at least as early as the service date of this Original Complaint.

53.   Upon information and belief, since at least the above-mentioned date when ZTE was on notice of its infringement, ZTE has actively induced, under U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers that purchase or sell the '593 Accused Products that include all of the limitations of one or more claims of the '593 patent to directly infringe one or more claims of the '593 patent by making, having made, using, offering for sale, selling, and/or importing the '593 Accused Products. Since at least the notice provided on the above-mentioned date, ZTE does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the '593 patent. Upon information and belief, ZTE intends to cause, and has taken affirmative steps to induce, infringement by these third-party manufacturers, distributors, importers, and/or consumers by, *inter alia*, creating advertisements

that promote the infringing use of the '593 Accused Products, creating established distribution channels for the '593 Accused Products into and within the United States, manufacturing the '593 Accused Products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States. For example, ZTE advertises, provides support for, and publishes a user manual for the Axon 7 on its own website at the following web address: https://www.zteusa.com/axon-7.

54.   Super Interconnect has been damaged as a result of ZTE's infringing conduct described in this Count. ZTE is, thus, liable to Super Interconnect in an amount that adequately compensates Super Interconnect for ZTE's infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Super Interconnect hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

Super Interconnect requests that the Court find in its favor and against ZTE, and that the Court grant ZTE the following relief:

a.   Judgment that one or more claims of the '044, '092, and '593 patents have been infringed, either literally and/or under the doctrine of equivalents, by ZTE and/or by others whose infringement has been induced by ZTE;

b.   Judgment that ZTE account for and pay to Super Interconnect all damages to and costs incurred by Super Interconnect because of ZTE's infringing activities and other conduct complained of herein;

c.   Judgment that ZTE account for and pay to Super Interconnect a reasonable, ongoing, post-judgment royalty because of ZTE's infringing activities and other conduct complained of herein;

d.   Judgment that ZTE's conduct warrants that the Court award treble damages pursuant to 35 U.S.C. § 284;

e.   Judgement that Super Interconnect be granted pre-judgment and post-judgment interest on the damages caused by ZTE's infringing activities and other conduct complained of herein;

f.   Judgment and an order finding this to be an exceptional case and requiring ZTE to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. § 285; and

g.   That Super Interconnect be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: November 2, 2018   Respectfully submitted,

                                                          /s/Jeffrey R. Bragalone
                                                          Jeffrey R. Bragalone
                                                          Texas Bar No. 02855775
                                                          T. William Kennedy Jr.
                                                          Texas Bar No. 24055771
                                                          Brian P. Herrmann
                                                          Texas Bar No. 24083174

                                                          Bragalone Conroy PC
                                                          2200 Ross Avenue
                                                          Suite 4500W
                                                          Dallas, TX 75201
                                                          Tel: (214) 785-6670
                                                          Fax: (214) 785-6680
                                                          jbragalone@bcpc-law.com
                                                          bkennedy@bcpc-law.com
                                                          bherrmann@bcpc-law.com

EXHIBIT A

US007627044B2

(12) **United States Patent**
Kim et al.

(10) **Patent No.:** **US 7,627,044 B2**
(45) **Date of Patent:** **Dec. 1, 2009**

(54) **CLOCK-EDGE MODULATED SERIAL LINK WITH DC-BALANCE CONTROL**

(75) Inventors: **Gyudong Kim**, Sunnyvale, CA (US);
Won Jun Choe, Seoul (KR);
Deog-Kyoon Jeong, Seoul (KR); **Jaeha Kim**, Mountain View, CA (US);
Bong-Joon Lee, Seoul (KR); **Min-Kyu Kim**, Sunnyvale, CA (US)

(73) Assignee: **Silicon Image, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 605 days.

(21) Appl. No.: **11/264,303**

(22) Filed: **Oct. 31, 2005**

(65) **Prior Publication Data**

US 2007/0098112 A1 May 3, 2007

(51) **Int. Cl.**
 H04B 3/00 (2006.01)
(52) **U.S. Cl.** **375/257**
(58) **Field of Classification Search** 375/257,
 375/259, 260, 295, 316, 319; 324/98; 455/453,
 455/284, 305; 718/105; 370/284, 301
 See application file for complete search history.

(56) **References Cited**

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OTHER PUBLICATIONS

Kyeongho Lee, et al., "1.04 GBd Low EMI Digital Video Interface System Using Small Serial Link Technique," *IEEE Journal of Solid-State Circuits*, vol. 33, No. 5, May 1998, pp. 816-823.
Wei-Hung Chen, et al., "A CMOS 400-Mb/s Serial Link for AS-Memory Systems Using a PWM Scheme," *IEEE Journal of Solid-State Circuits*, vol. 36, No. 10, Oct. 2001, pp. 1498-1505.

* cited by examiner

Primary Examiner—Sam K Ahn
(74) *Attorney, Agent, or Firm*—Blakely Sokoloff Taylor & Zafman

(57) **ABSTRACT**

A battery powered computing device has a channel configured as a single direct current balanced differential channel. A signal transmitter is connected to the channel. The signal transmitter is configured to apply clock edge modulated signals to the channel, where the clock edge modulated signals include direct current balancing control signals. A signal receiver is connected to the channel. The signal receiver is configured to recover the direct current balancing control signals.
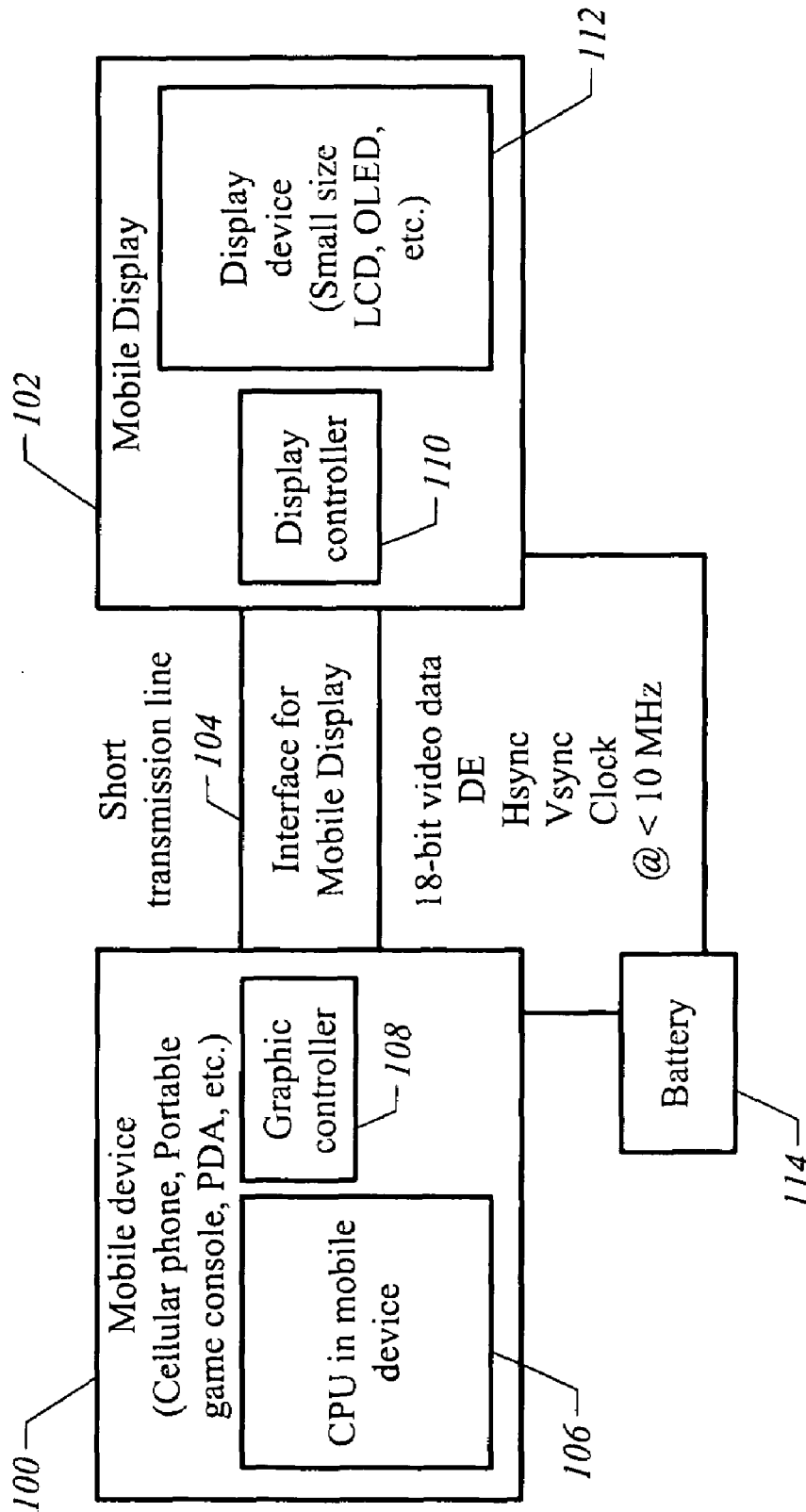
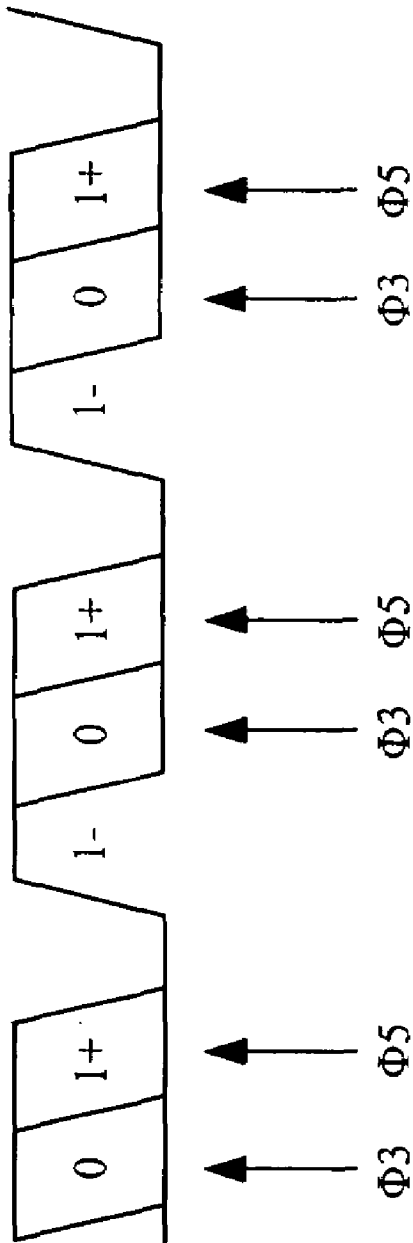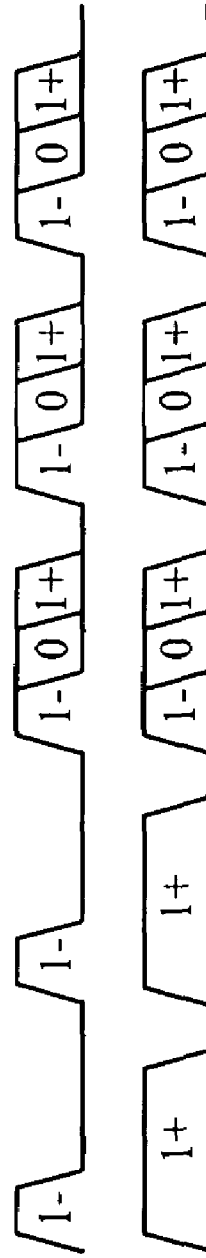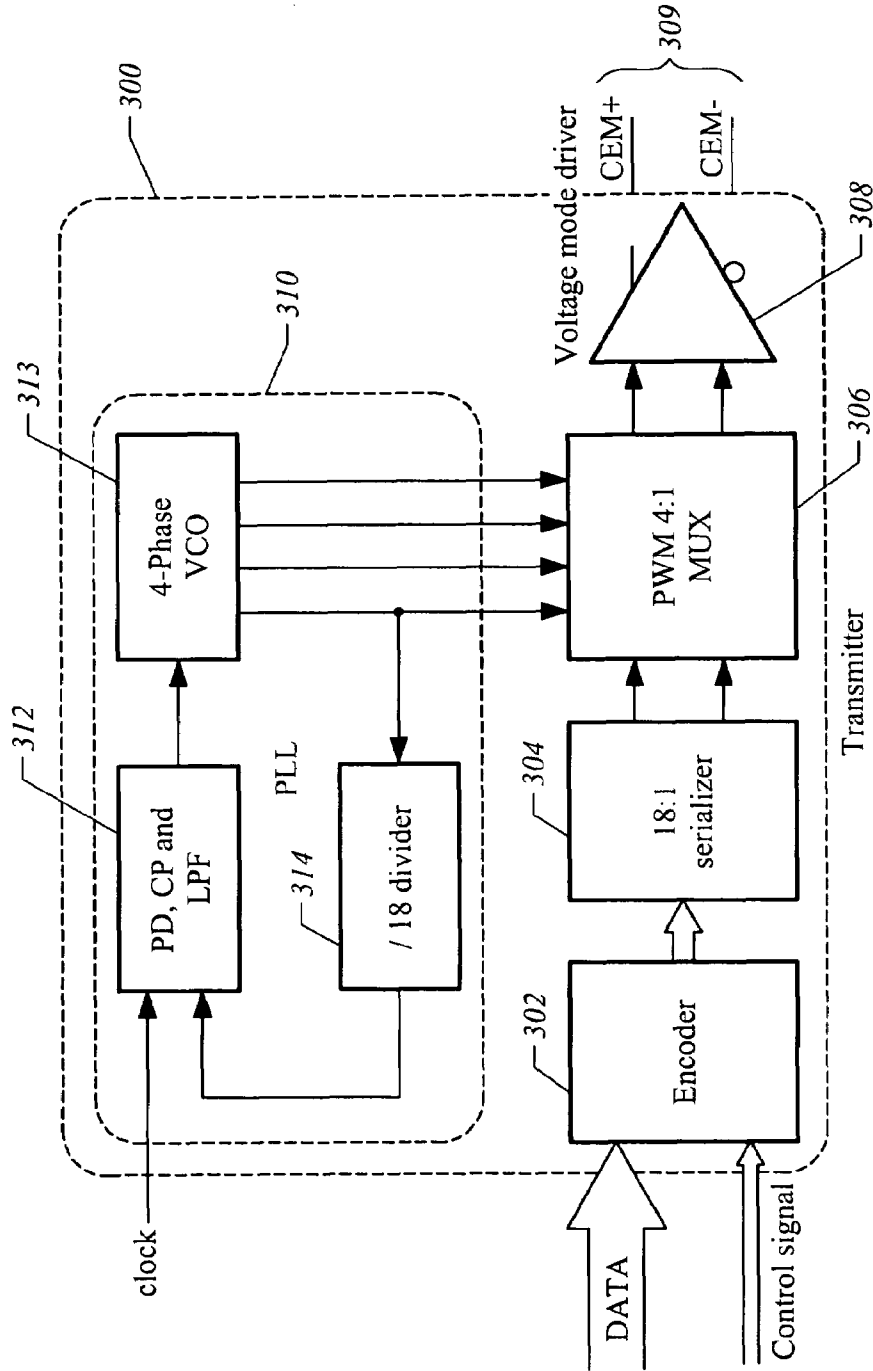**19 Claims, 8 Drawing Sheets**
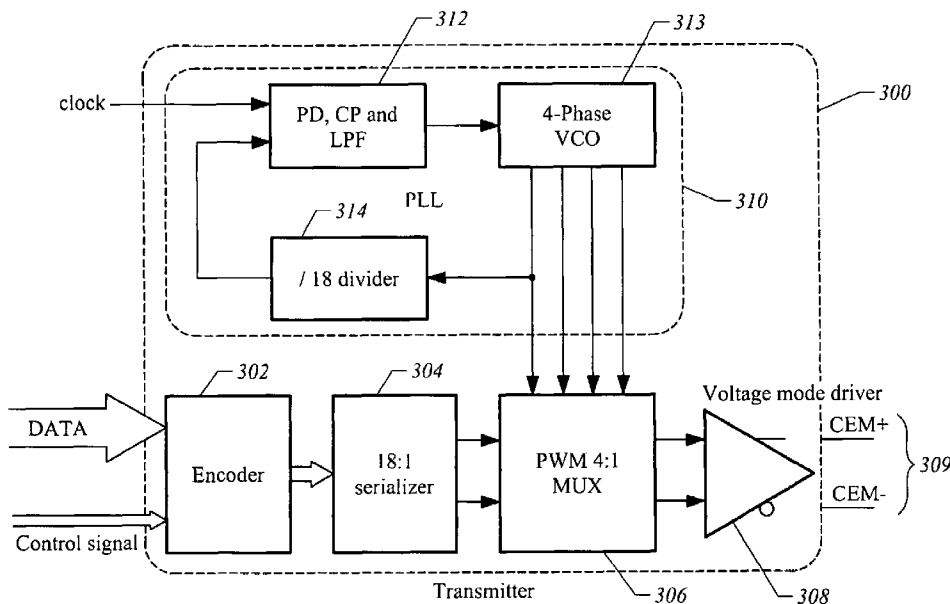
FIG. 1

FIG. 2A

FIG. 2B

FIG. 3

FIG. 4

FIG. 5

clock

DATA

Control Signal

606

Sampler &
PWM decoder

$\Phi_1\Phi_2\Phi_3\Phi_4\Phi_5\Phi_6\Phi_7\Phi_8$

8-Phase VCDL

604

600

DLL

PD,
CP

Φ_0

608

602

CEM+

CEM-

Limiting Amplifier

603

Receiver

FIG. 6

FIG. 7

FIG. 8A

$\Phi 0$

$\Phi 1$

| PC works | Coarse up assertion |

FIG. 8B

$\Phi 0$

$\Phi 4$ $t_{VCDL,MIN}$

$\Phi 8$

UP

DN

PD_reset
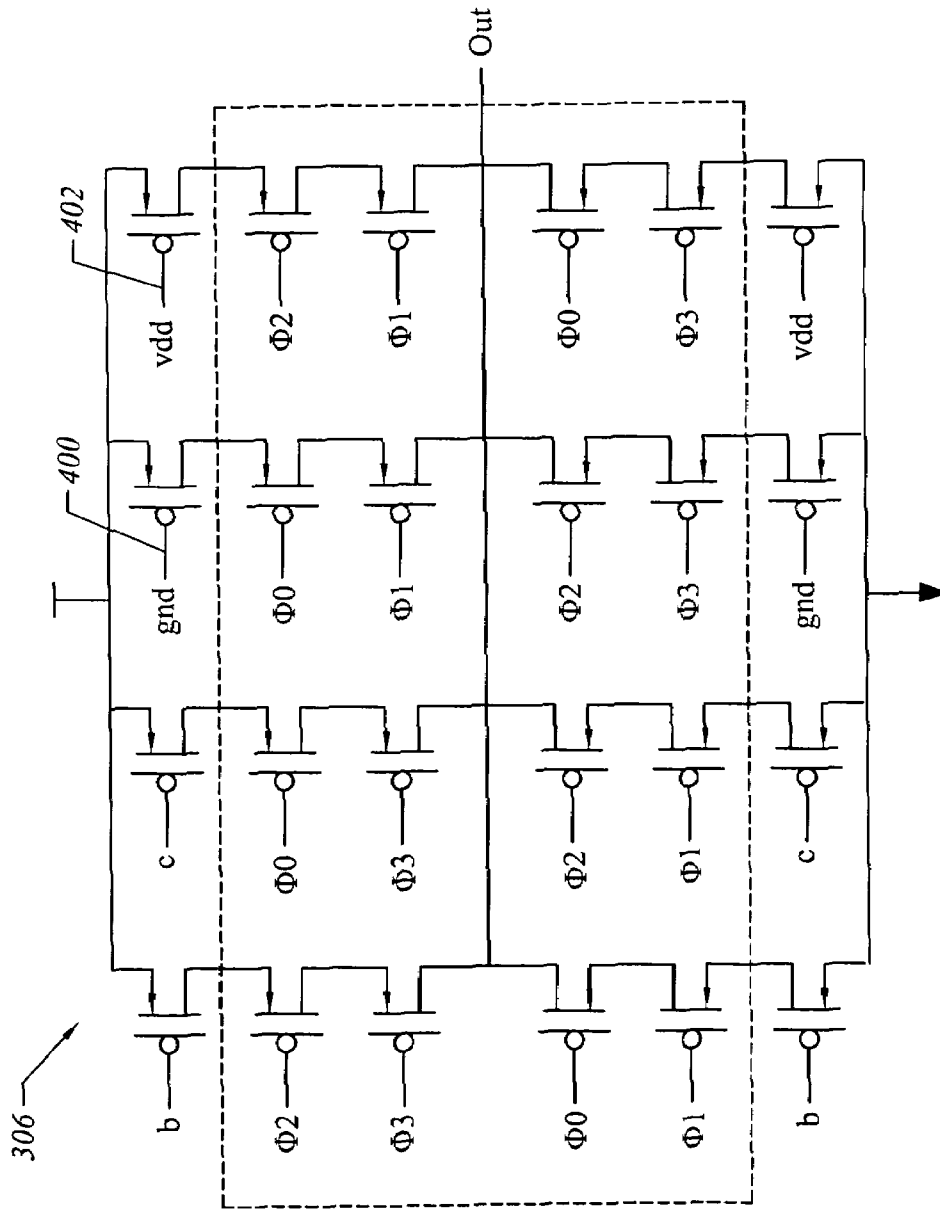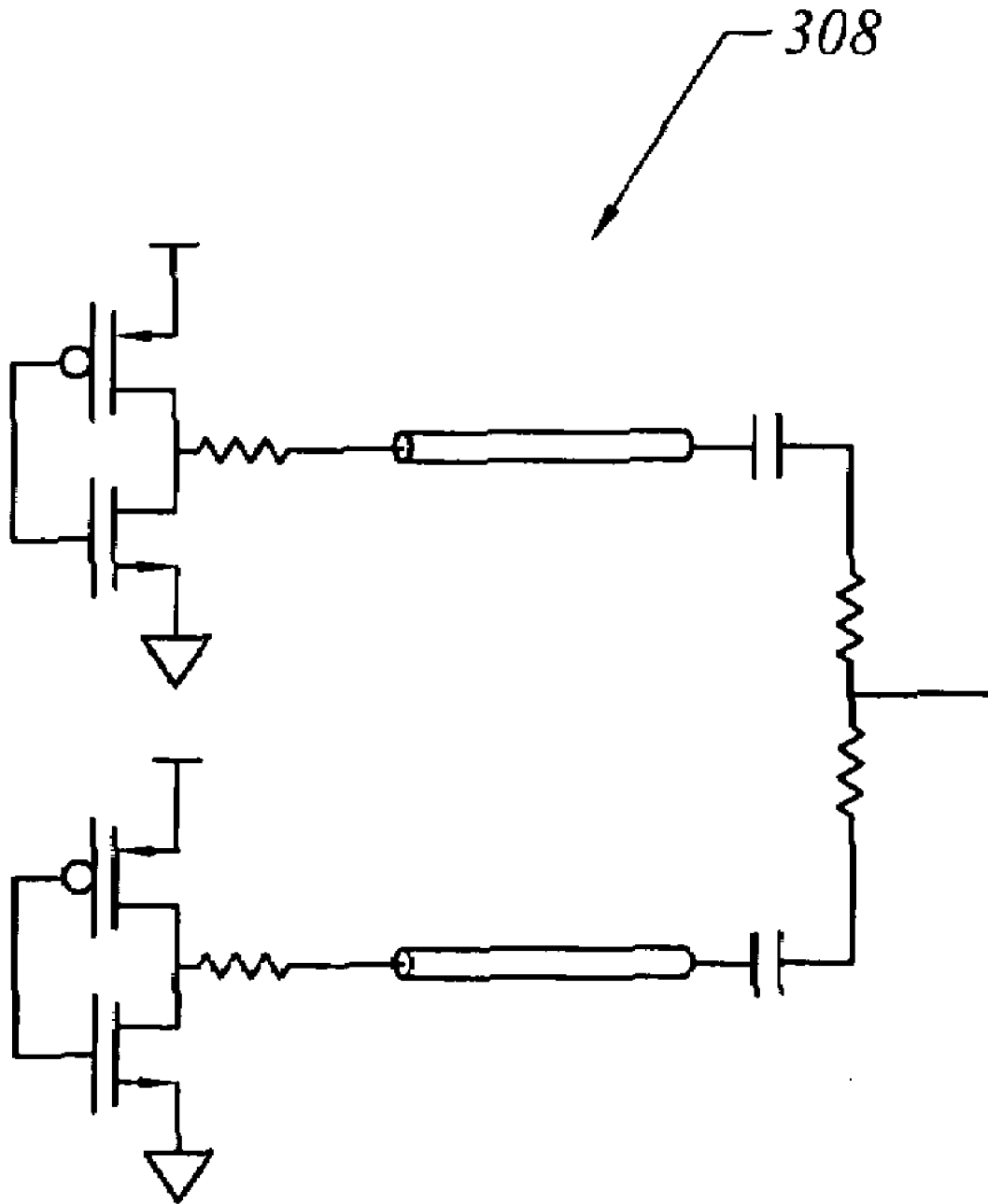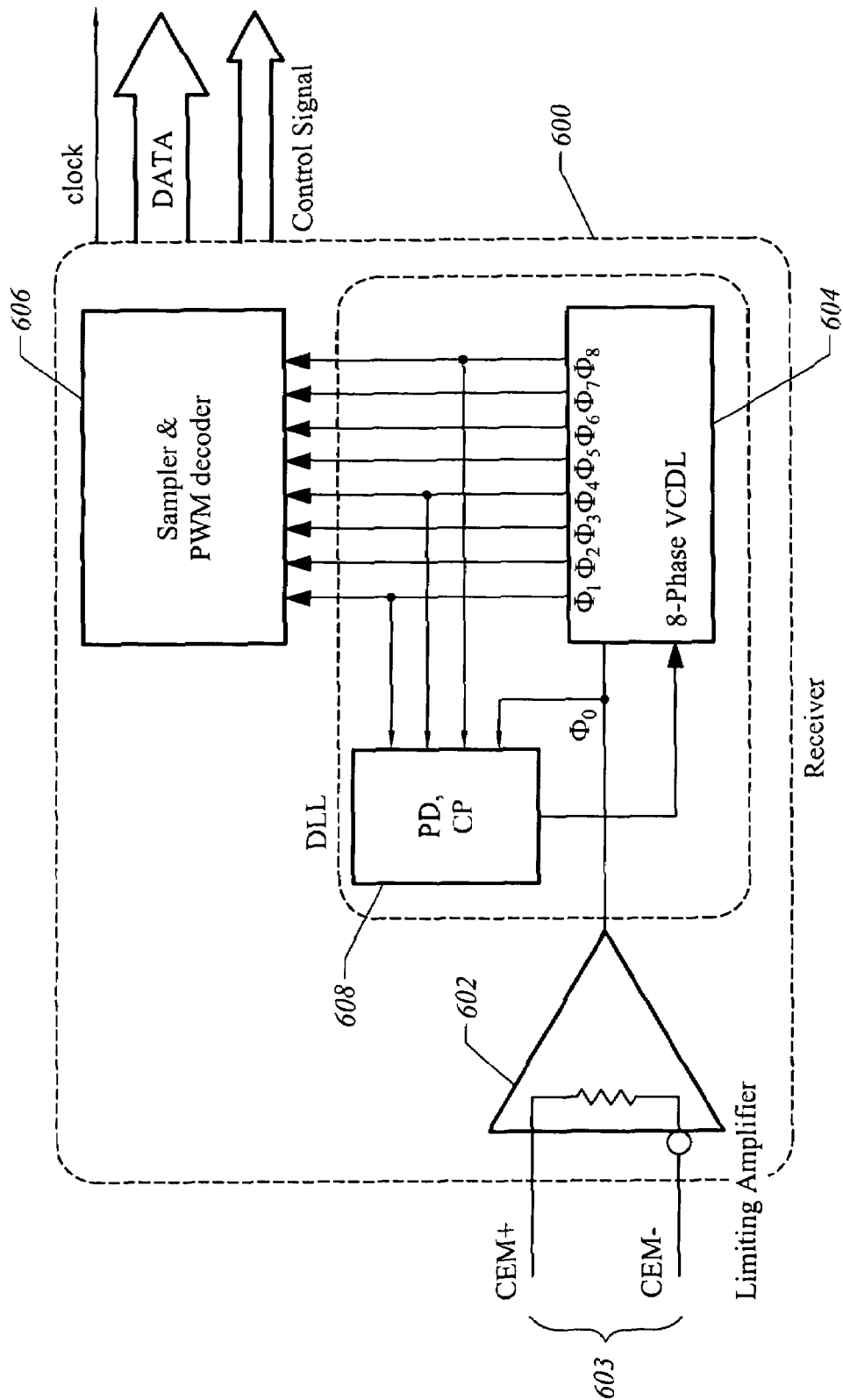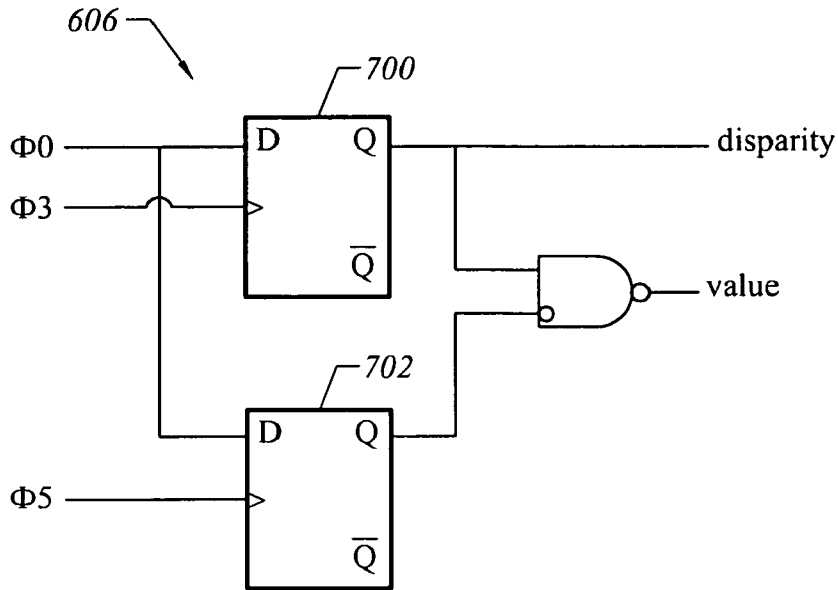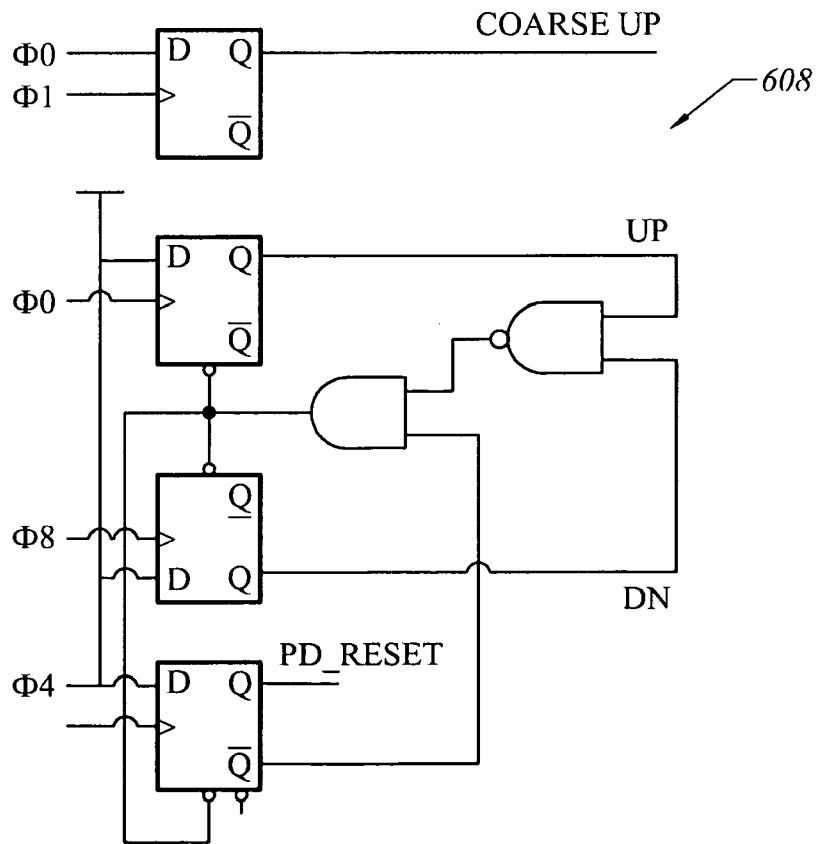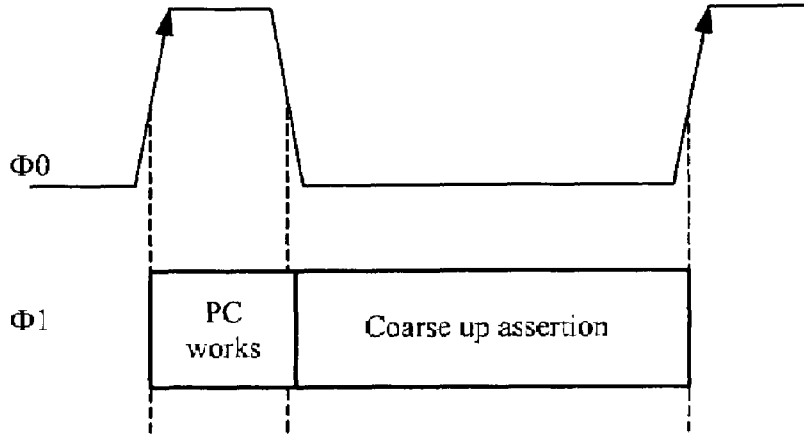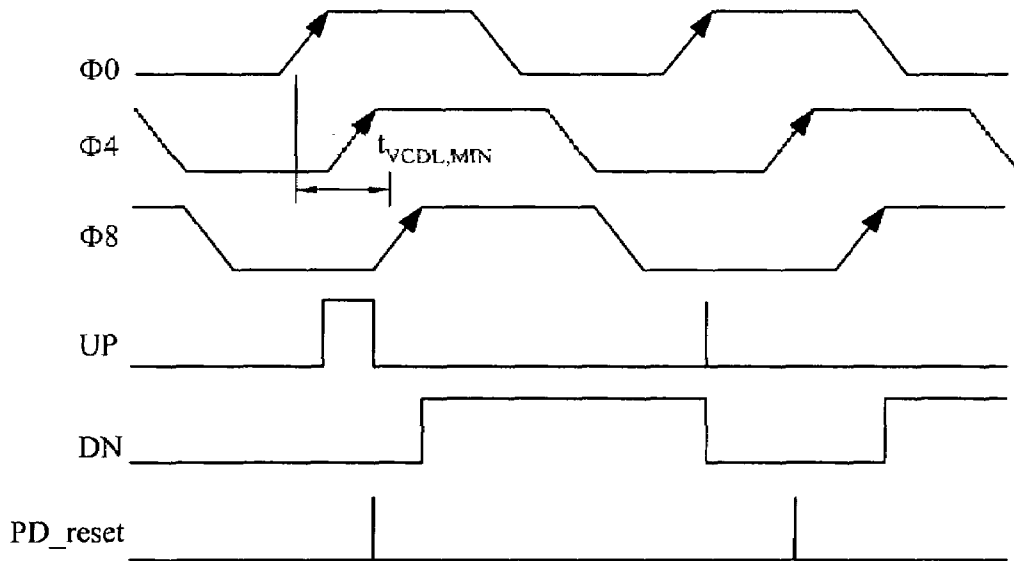
FIG. 8C

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CLOCK-EDGE MODULATED SERIAL LINK WITH DC-BALANCE CONTROL

BRIEF DESCRIPTION OF THE INVENTION

This invention relates generally to the transmission of serial signals, such as in a transition minimized differential signaling system. More particularly, this invention relates to a clock-edge modulated serial link incorporating direct current (DC) balancing control signals.

BACKGROUND OF THE INVENTION

Mobile devices, such as cellular phones, Personal Digital Assistants (PDAs) and portable game consoles continue to grow in popularity. FIG. 1 illustrates an example of such a mobile device. In particular, FIG. 1 illustrates a mobile device 100 connected to a mobile display 102 via an interface 104. The mobile device 100 includes a central processing unit 106 and a graphic controller 108. The mobile display 102 includes a display controller 110 and a display 112, such as a liquid crystal display. A battery 114 powers the mobile device 100 and the mobile display 102. Low power design is critical in mobile applications of this type.

A conventional mobile device interface 104 uses parallel channels with single-ended full-swing signaling. The channels are composed of many lines, for example, 22 lines with 18-bit video pixel data lines and control signal lines, such as dot-clock, data enable (DE), horizontal sync (HSYNC), vertical sync (VSYNC), and other display-specific configuration settings. These signal lines consume power and space. In addition, they produce excessive electromagnetic radiation. To reduce the number of lines, a serial link with low-voltage swing differential signaling may be used. As known in the art, this type of signaling amplifies difference signals, while rejecting common-mode signals.

Popular display interfaces, such as Low Voltage Differential Signaling (LVDS) and Digital Visual Interface (DVI) use 3 channels of serialized differential signals for 18-bit or 24-bit pixel color data. In addition, a separate channel is used for clock transmission. In such an application, the voltage swing is reduced to about 400 mV.

In certain applications, such as a mobile display, relatively low video resolution is acceptable. In such a case, it is possible to use a single data channel. However, in this situation, the prior art has relied upon a separate clock channel. Since the dedicated channel solely for clock transmission increases hardware costs and power, it would be desirable to remove the dedicated clock channel and use only a single channel for transmitting the clock, data and control signals. However, if conventional network protocols, such as 802.3z Gigabit Ethernet are employed, a number of problems arise. For example, a local reference clock must be used at the receiver. This increases hardware costs and reduces flexibility in transmission bandwidth.

In view of the foregoing, it would be desirable to provide a low-power mobile device with a serial channel that supports clock, data and control signals, such as DC balancing control signals.

SUMMARY OF THE INVENTION

The invention includes a battery powered computing device with a channel configured as a single direct current balanced differential channel. A signal transmitter is connected to the channel. The signal transmitter is configured to apply clock edge modulated signals to the channel, where the

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clock edge modulated signals include direct current balancing control signals. A signal receiver is connected to the channel. The signal receiver is configured to recover the direct current balancing control signals.

The invention includes a signal transmitter. The signal transmitter has a channel node to interface with a single direct current balanced differential channel. Circuitry is connected to the channel node, the circuitry being configured to multiplex clock, data and control signals and apply them to the channel node. The clock signal is pulse width modulated to incorporate direct current balancing control signals.

The invention also includes a signal receiver. A channel node interfaces with a channel configured as a single direct current balanced differential channel. Circuitry is connected to the channel node. The circuitry is configured to de-multiplex clock, data and control signals from the channel node. The circuitry identifies direct current balancing control signals within a pulse width modulate clock signal.

The invention allows many parallel channels to be reduced to a single serial channel, which reduces power consumption. To further reduce power dissipation, the invention may be implemented with voltage-mode drivers. Still additional power reduction can be achieved by removing the source transmission channel termination and relying solely upon receiver side source transmission channel termination. The invention includes a delay-locked loop (DLL) data-recovery circuit that operates robustly in a high jitter environment.

BRIEF DESCRIPTION OF THE FIGURES

The invention is more fully appreciated in connection with the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a mobile device and a mobile display that may be configured in accordance with an embodiment of the invention.

FIG. 2A illustrates DC-balanced clock-edge modulation in accordance with an embodiment of the invention.

FIG. 2B illustrates special character embedded clock-edge modulation utilized in accordance with an embodiment of the invention.

FIG. 3 illustrates a clock-edge modulated transmitter configured in accordance with an embodiment of the invention.

FIG. 4 illustrates a multiplexer that may be used in the clock-edge modulated transmitter of FIG. 3.

FIG. 5 illustrates a voltage mode driver utilized in accordance with an embodiment of the invention.

FIG. 6 illustrates a clock-edge modulated receiver configured in accordance with an embodiment of the invention.

FIG. 7 illustrates clock-edge modulated decoder that may be used in accordance with an embodiment of the invention.

FIG. 8A illustrates a phase detector circuit configured in accordance with an embodiment of the invention.

FIG. 8B illustrates the use of a coarse-up signal in accordance with an embodiment of the invention.

FIG. 8C illustrates various signals processed in accordance with an embodiment of the invention.

Like reference numerals refer to corresponding parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

The invention includes a single-channel serial link using clock edge modulation (CEM). This scheme, also known as pulse-width modulation (PWM), encodes data information onto a periodic clock by varying the position of a selected edge (i.e., the rising edge or falling edge); thus, the pulse-

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width of the clock is altered or modulated. The invention provides techniques to transfer a clock signal, data and control signals over a single channel.

By way of example, the invention may be implemented by varying the falling edge of the clock signal. As shown in FIG. 2A, data are encoded as a variation of the clock falling edge position, while the position of the rising edge is fixed. The periodic occurrence of the rising edges enables easy extraction of the clock signal, from which the receiver can generate the "dot-clock" simply by dividing down the incoming signal (e.g., by 18) with no further clock recovery mechanism. The modulation of the falling edge position or the clock pulse width allows one to embed data and control signals in the clock, therefore reducing the pin count.

U.S. Pat. No. 6,463,092 (the '092 patent) utilizes a pulse width modulation technique of this type. The '092 patent, which is assigned to the assignee of the current invention, is hereby incorporated by reference. The current invention builds upon the disclosed scheme of the '092 patent to achieve DC-balancing. In one embodiment, DC-balancing is achieved by inserting DC-balancing control signals into the serial link. The DC-balancing control signals may include signals to maintain DC-balance, increase DC-balance, and decrease DC-balance. Standard techniques are used to generate and process the DC-balance control signals. An aspect of the invention is directed toward incorporating the DC-balance control signals into a single serial link along with clock and data signals.

In one embodiment of the invention, the bit "0" is coded as a 50% duty cycle clock, indicating that no changes are necessary to keep balance. On the other hand, the bit "1" is coded as either a 25% or a 75% duty cycle clock, denoted as "1−" and "1+", respectively, in FIG. 2(a). Whether to use a 25% or a 75% duty cycle is determined by the DC value of the bits transmitted so far. If the DC value is lower than nominal, the bit "1" is coded as 75%, and vice versa. With this encoding, the maximum disparity counted in unit pulse length (i.e., 25% pulse width) is only 2 and good DC-balance is achieved.

The serial link may also be used to transmit control signals, such as HSYNC and VSYNC. In one embodiment, these control signals are transmitted when DE is unasserted. Leveraging this fact, the state of DE being 0 is coded as two consecutive "1+"'s or "1−"'s, as shown in FIG. 2(b), which is an impossible sequence while the normal pixel data are being sent (i.e., DE is 1). This special sequence indicates that the following 16 pulse-width modulated symbols represent control characters. In this way, the control signals can be transmitted without requiring any additional channels. That is, the invention leverages the DE 0 state (when data is not being sent) to send DC-balance and other control information on a single channel.

FIG. 3 illustrates a transmitter 300 configured in accordance with an embodiment of the invention. The transmitter 300 includes an encoder 302 that receives data and control signals. For example, the data may be 6 bits of red pixel data, 6 bits of green pixel data, and 6 bits of blue pixel data. The control signals may include HSYNC, VSYNC, and DE signals. The output of the encoder 302 is applied to a serializer circuit 304, which serializes the data and control information for the serial link. The encoder 302 or the serializer circuit 304 may be used to generate a DC-balance control signal.

The serialized data is then applied to a multiplexer, which receives control inputs form a phase-locked loop 310. The output of the multiplexer 306 is applied to a channel driver 308, in this case a voltage mode driver, which produces differential clock-edge modulated signals. In particular, the

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channel driver 308 applies a positive CEM signal (CEM+) and a negative CEM signal (CEM−) to a channel node 309.

In one embodiment, the phase detector 312 of the phase-locked loop 310 multiplies the reference clock by 18 and operates with a voltage controlled oscillator 313 to generate 4 clock phases: 0(ϕ0), 90(ϕ1), 180(ϕ2), and 270(ϕ3). A divider 314 divides the multiplied clock signal and provides a feedback input to the phase detector 312. The transmitter operates as if it is sending 4 Non-Return to Zero (NRZ) bits per symbol using these clock phases. The phase signals are processed by the multiplexer 306.

FIG. 4 illustrates a pulse width modulated 4-to-1 multiplexer configured in accordance with an embodiment of the invention. Note that the first bit 400 and the last bit 402 are fixed at 1 and 0, respectively. Only the middle two bits (b and c in FIG. 4) need to vary to express the three different falling edge positions. The encoder 302 and serializer 304 may be used to generate these two bits from the parallel pixel data and control signals.

Since power consumption is a significant concern in a mobile device, an embodiment of the invention uses a voltage mode driver 308 for off-chip signaling in the CEM transmitter. FIG. 5 illustrates a known voltage mode driver that may be used in accordance with an embodiment of the invention. Unlike other prior art drivers, the voltage mode driver does not have a current source stack, hence it is capable of low voltage operation. To reduce the power consumption, the voltage mode driver is designed to operate at 1.2V supply and the voltage swing is also reduced to 80 mV. Since the link span of the mobile display is short (less than several inches) and the CEM signal is relatively immune to inter-symbol interference, an 80 mV swing is enough to guarantee proper operation of the receiver. Using the voltage mode driver with reduced swing, the CEM transmitter has been implemented to consume less than 1 mW when operating at 270 Mbps.

For the proposed CEM link, the data is delivered on the clock signal, making the receiver architecture much simpler. That is, the receiver does not require an NRZ phase detector nor a local frequency reference, as is the case in many serial link receivers. In one embodiment, the invention uses a delay locked loop (DLL) for data recovery, as shown in FIG. 6.

The receiver 600 has a front-end limiting amplifier 602 which receives differential input signals CEM+ and CEM− at channel node 603. The amplifier 602 facilitates an adequate signal level for the DLL input. A voltage-controlled delay line (VCDL) 604 generates 8-phase delayed clocks to sample and decode the CEM data. FIG. 2(a) shows a timing relationship between sampling clocks and input CEM data. In one embodiment, the sampler 606 examines the CEM data at two different phases (ϕ3 and ϕ5, as shown in FIG. 2A) to identify the location of the clock falling edge.

FIG. 7 illustrates a sampler and pulse-width modulated decoder 606 implemented with two flip-flops 700 and 702. Each flip-flop receives the ϕ0 signal, while flip flop 700 receives the ϕ3 signal and flip flop 702 receives the ϕ5 signal. Using the sampled results, the CEM decoder extracts the data and disparity information. From the disparity information, the receiver can detect the pixel boundary and special sequences indicating DE, HSYNC, and VSYNC.

As shown in FIG. 6, the input CEM data is sampled by its own delayed version. So, the DLL can recover data even if the input clock has a large amount of jitter. To ensure enough lock range of the DLL, a phase detector 608 with false-lock detection may be used. FIG. 8A illustrates a phase detector 608 configured in accordance with an embodiment of the invention. If the initial delay of VCDL is larger than $2 \times T_{CLK}$, i.e., the rising edge of the ϕ1 clock is located in the shaded area of

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FIG. 8(b), the coarse_up signal is asserted to prevent harmonic lock. On the other hand, when the initial delay is so small that the VCDL delay would be stuck to its minimum value, the PD_reset signal is asserted to deactivate the false up signal. This is accomplished by comparing rising edges of $\phi0$ and $\phi4$, as shown in FIG. 8(c). If the rising edge of $\phi4$ is found between $\phi0$ and $\phi8$, the phase detector no longer generates an up signal, but makes the VCDL slow down.

The clock-edge modulated serial link of the invention has been fabricated in a standard 0.18 μm CMOS technology. The fabricated chip consumes 3.12 mW at 1.2 V supply voltage when operating at 270 Mb/s.

Those skilled in the art will appreciate that the invention may be implemented with various modifications. For example, the serial link may be augmented with multiple links to increase throughput. In addition, the invention can be utilized in a bidirectional (full-duplex) mode. Also, since differential mode signals are used, there is a common mode signal that may be used for other purposes. For example, the common mode signal may be used to exchange configuration data. The configuration data may specify such parameters as data format, data destination (when multiple transmitters/receivers are connected on the bus), data directionality, and the like.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that specific details are not required in order to practice the invention. Thus, the foregoing descriptions of specific embodiments of the invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed; obviously, many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, they thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the following claims and their equivalents define the scope of the invention.

The invention claimed is:

1. A signal transmitter, comprising:
a channel node to interface with a single direct current balanced differential channel; and
circuitry connected to the channel node, the circuitry being configured to multiplex clock, data and control signals and apply them to the channel node, wherein the clock signal is pulse width modulated to incorporate direct current balancing control signals.

2. The signal transmitter of claim 1 wherein the circuitry is configured to specify a low direct current value at a first duty cycle position.

3. The signal transmitter of claim 2 wherein the circuitry is configured to specify a high direct current value at a second duty cycle position.

4. The signal transmitter of claim 3 wherein the circuitry is configured to specify a no change direct current value at a third duty cycle position.

5. The signal transmitter of claim 1 wherein the circuitry generates multiple phase signals.

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6. The signal transmitter of claim 5 wherein the circuitry includes a multiplexer to process the multiple phase signals and serialized data.

7. The signal transmitter of claim 6 wherein the circuitry includes a voltage mode driver to process the output of the multiplexer.

8. A signal receiver, comprising:
a channel node to interface with a channel configured as a single direct current balanced differential channel; and
circuitry connected to the channel node, the circuitry configured to de-multiplex clock, data and control signals from the channel node, wherein the circuitry identifies direct current balancing control signals within a pulse width modulated clock signal.

9. The signal receiver of claim 8 wherein the circuitry includes an amplifier to process signals from the channel.

10. The signal receiver of claim 9 wherein the circuitry includes a delay-locked loop to process output from the amplifier.

11. The signal receiver of claim 10 wherein the delay-locked loop generates multiple phase signals for application to a pulse width modulated decoder.

12. The signal receiver of claim 11 wherein the delay-locked loop generates multiple phase signals for application to a phase detector.

13. A battery powered computing device, comprising:
a channel configured as a single direct current balanced differential channel;
a signal transmitter connected to the channel, the signal transmitter being configured to multiplex clock, data, and control signals, wherein the clock signal is pulse width modulated to incorporate direct current balancing control signals, the signal transmitter configured to apply the multiplexed signals to the channel; and
a signal receiver connected to the channel, the signal receiver configured to de-multiplex the clock, data and control signals from the channel node, the signal receiver configured to identify and recover the direct current balancing control signals from the pulse width modulated clock signal.

14. The battery powered computing device of claim 13 wherein the signal transmitter includes a voltage-mode driver.

15. The battery powered computing device of claim 13 wherein the channel is terminated only at the signal receiver.

16. The battery powered computing device of claim 13 further comprising a graphics controller connected to the signal transmitter.

17. The battery powered computing device of claim 13 further comprising a display controller connected to the signal receiver.

18. The battery powered computing device of claim 13 wherein the signal transmitter and the signal receiver are configured to exchange configuration information using a common mode signal on the channel.

19. The battery powered computing device of claim 13 wherein the signal transmitter and the signal receiver are configured for bidirectional data transfers over the channel.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.   : 7,627,044 B2   Page 1 of 1
APPLICATION NO. : 11/264303
DATED   : December 1, 2009
INVENTOR(S)   : Kim et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page:
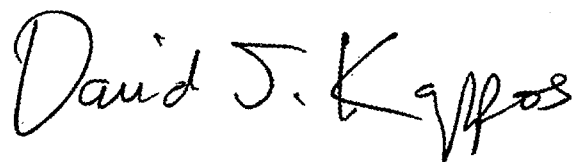
The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1001 days.

Signed and Sealed this

Second Day of November, 2010

David J. Kappos
Director of the United States Patent and Trademark Office

EXHIBIT B

(12) **United States Patent**
     Kim et al.

(10) **Patent No.:**   **US 6,463,092 B1**
(45) **Date of Patent:**   **Oct. 8, 2002**

(54) **SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE**

(75) Inventors: **Gyudong Kim**, Sunnyvale, CA (US); **Min-Kyu Kim**, Cupertino, CA (US); **Seung Ho Hwang**, Palo Alto, CA (US)

(73) Assignee: **Silicon Image, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/393,235**

(22) Filed: **Sep. 9, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/099,770, filed on Sep. 10, 1998.

(51) **Int. Cl.^{7}** **H04B 1/38**
(52) **U.S. Cl.** **375/219**; 375/220; 375/244; 375/257; 375/293; 375/354; 375/355; 375/360; 370/284; 370/301
(58) **Field of Search** 375/219, 220, 375/244, 257, 288, 293, 354, 355, 359, 360, 377; 370/284, 301, 307

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Loinaz, Marc J., Wooley, Bruce A., "A BiCMOS Time Interval Digitizer for High–Energy Physics Instrumentation", Center for Integrated Systems, Stanford University, IEEE 1993 Custom Integrated Circuits Conference, pp. 28.6.1–28.6.4.

Primary Examiner—Chi Pham
Assistant Examiner—Khanh Cong Tran
(74) *Attorney, Agent, or Firm*—Perkins Coie LLP; Paul Hickman; Steve S. Kelley

(57) **ABSTRACT**

The system preferably includes a unique transmitter that sends both clock and data signals over the same transmission line. The receiver uses the same transmission line to send data signals back to the transmitter. The transmitter comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data from the clock signal. The receiver comprises a clock re-generator, a data decoder and a return channel encoder. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The return channel encoder generates signals and asserts them on the transmission line. The signal is asserted or superimposed over the clock & data signal provided by the transmitter.
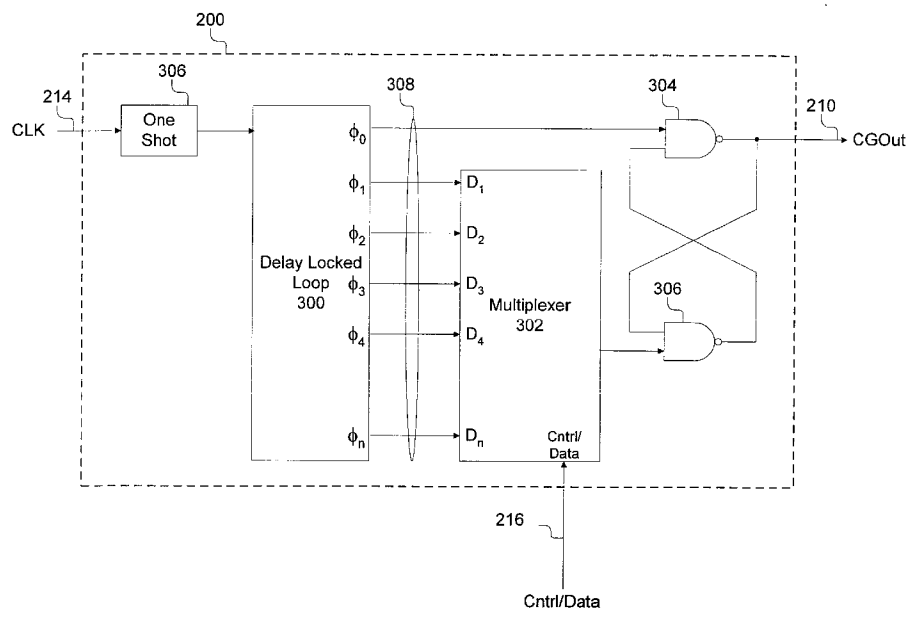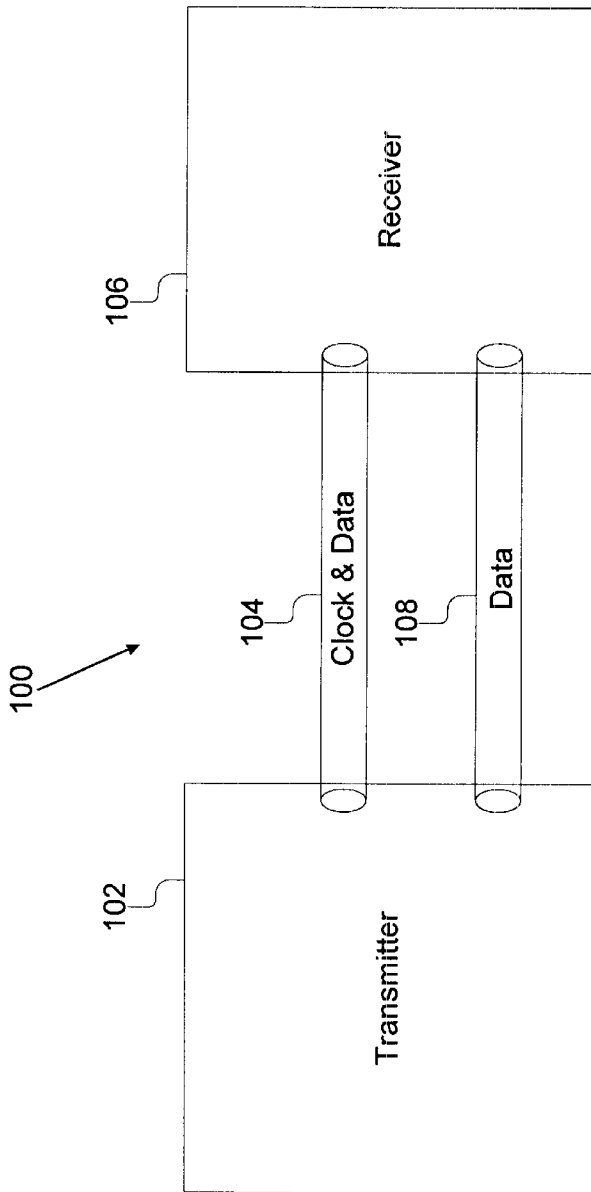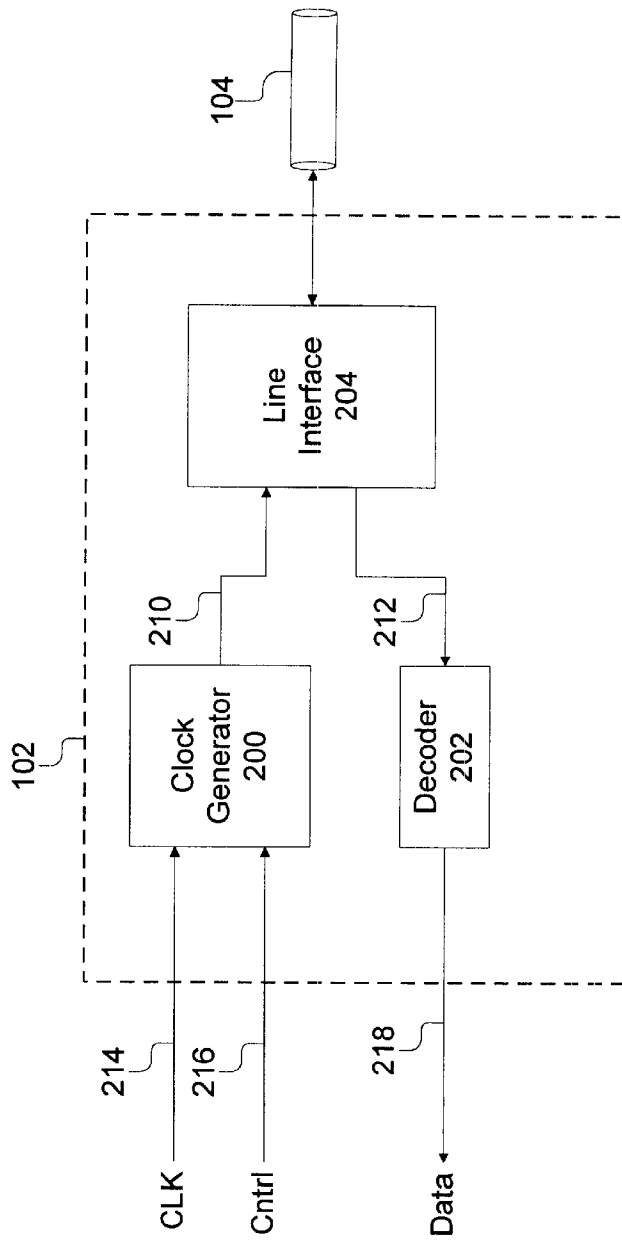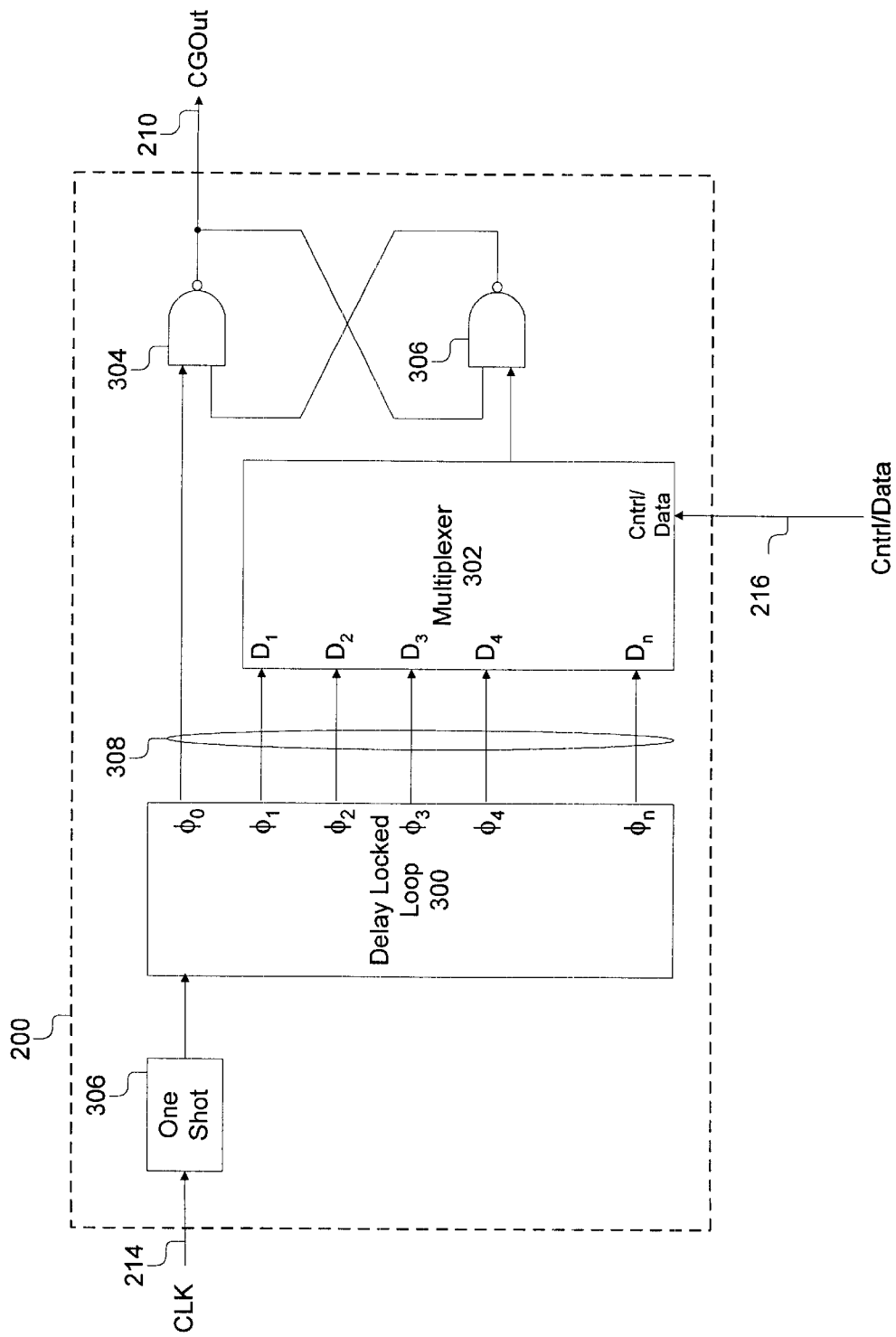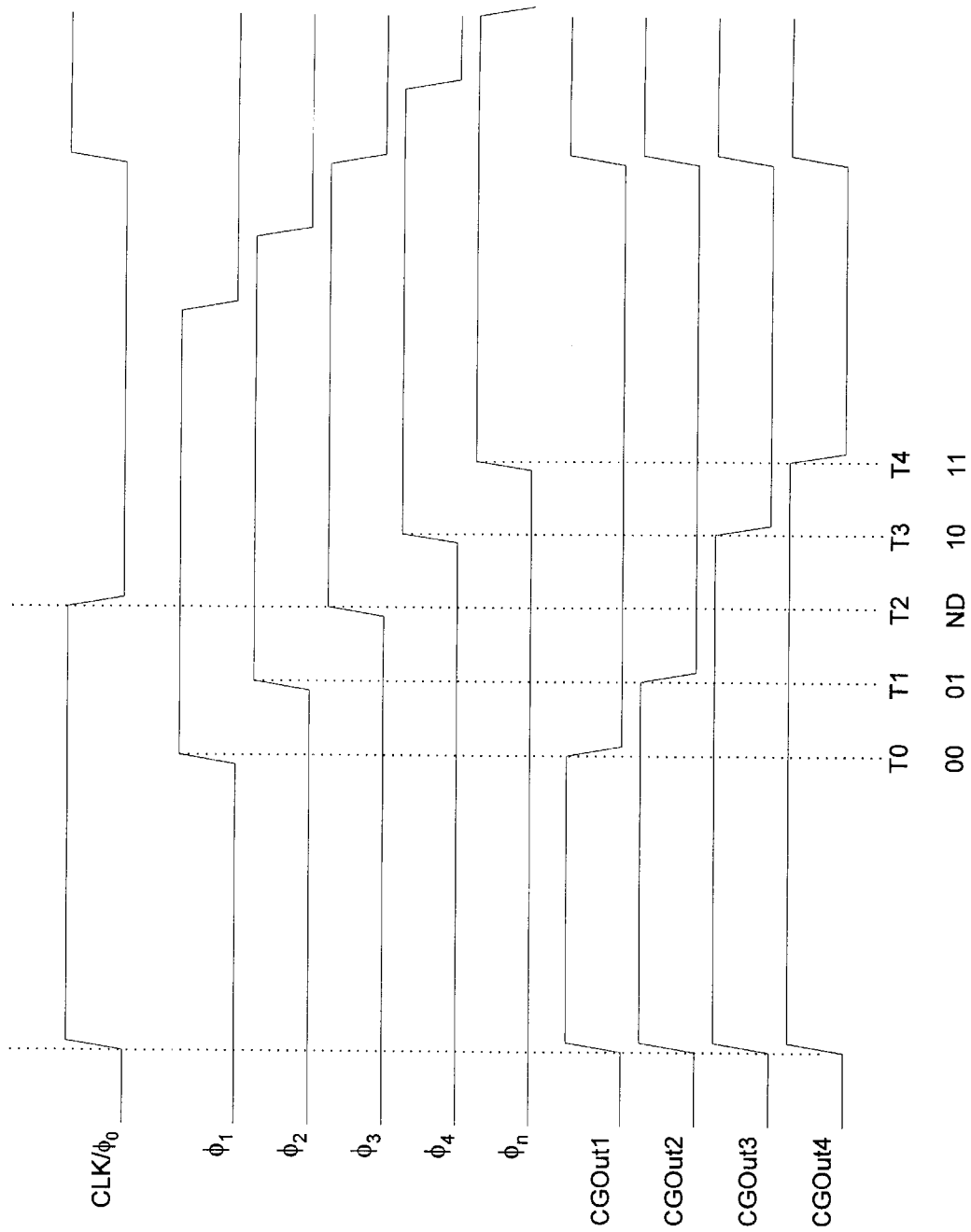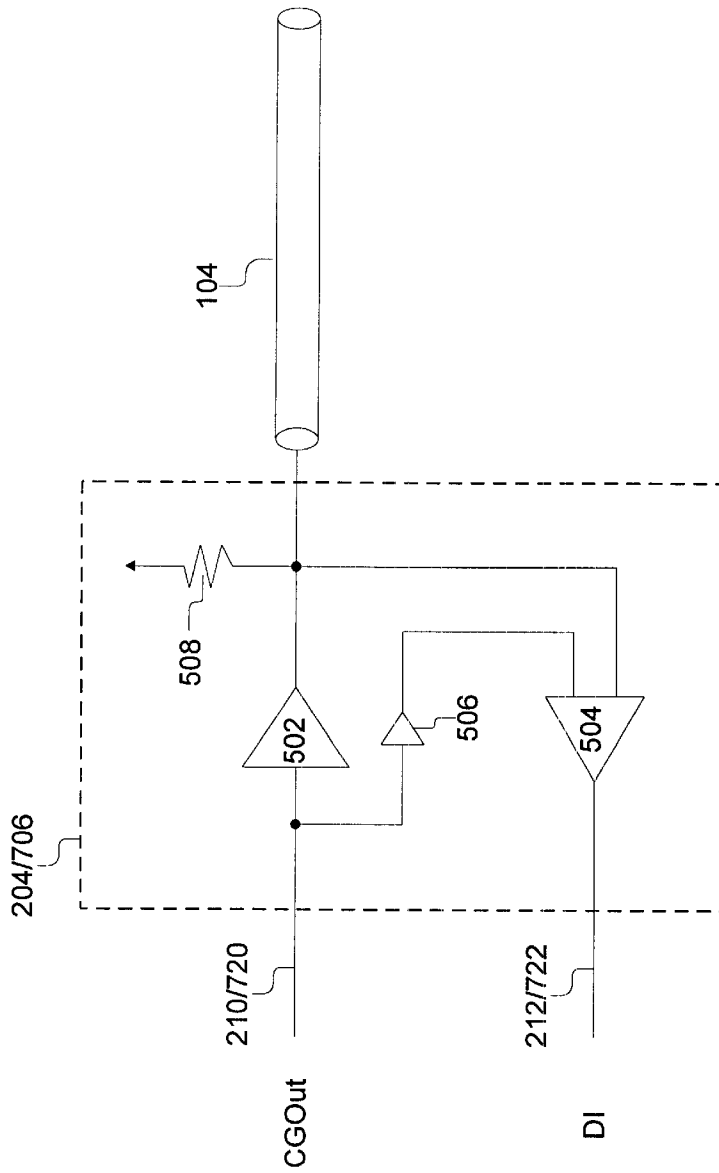
26 Claims, 17 Drawing Sheets
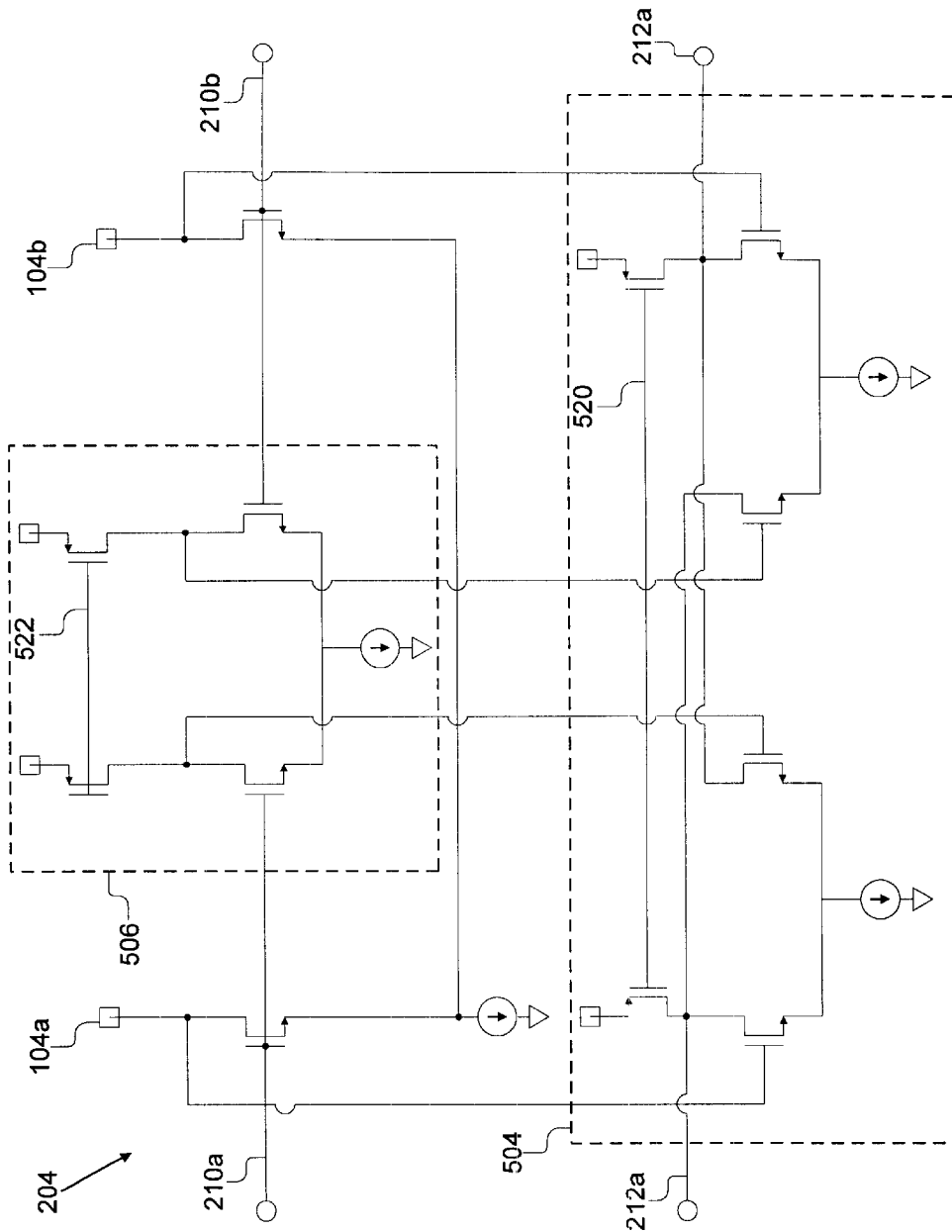
Figure 1

Figure 2

Figure 3

Figure 4

Figure 5A

Figure 5B

Figure 6A
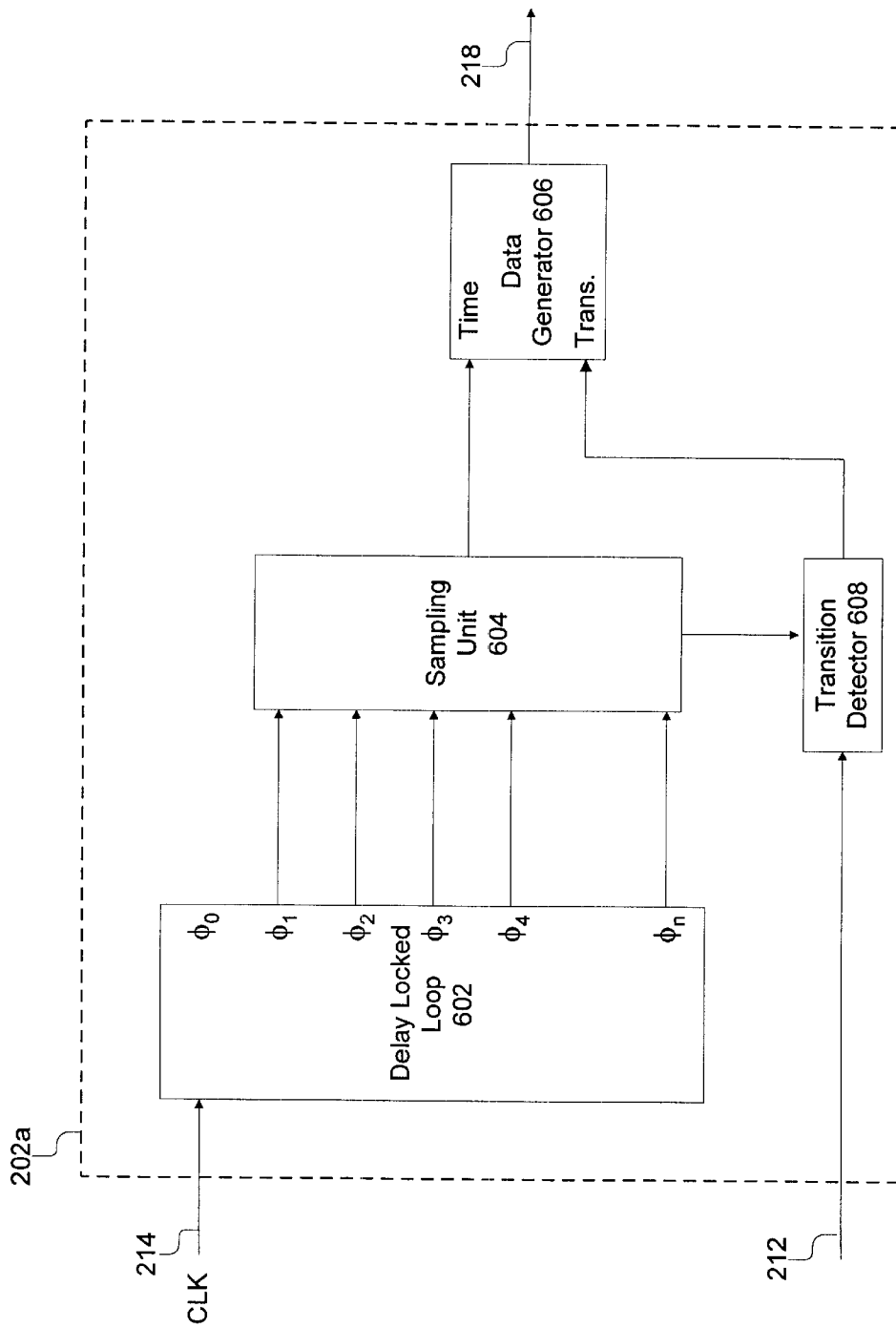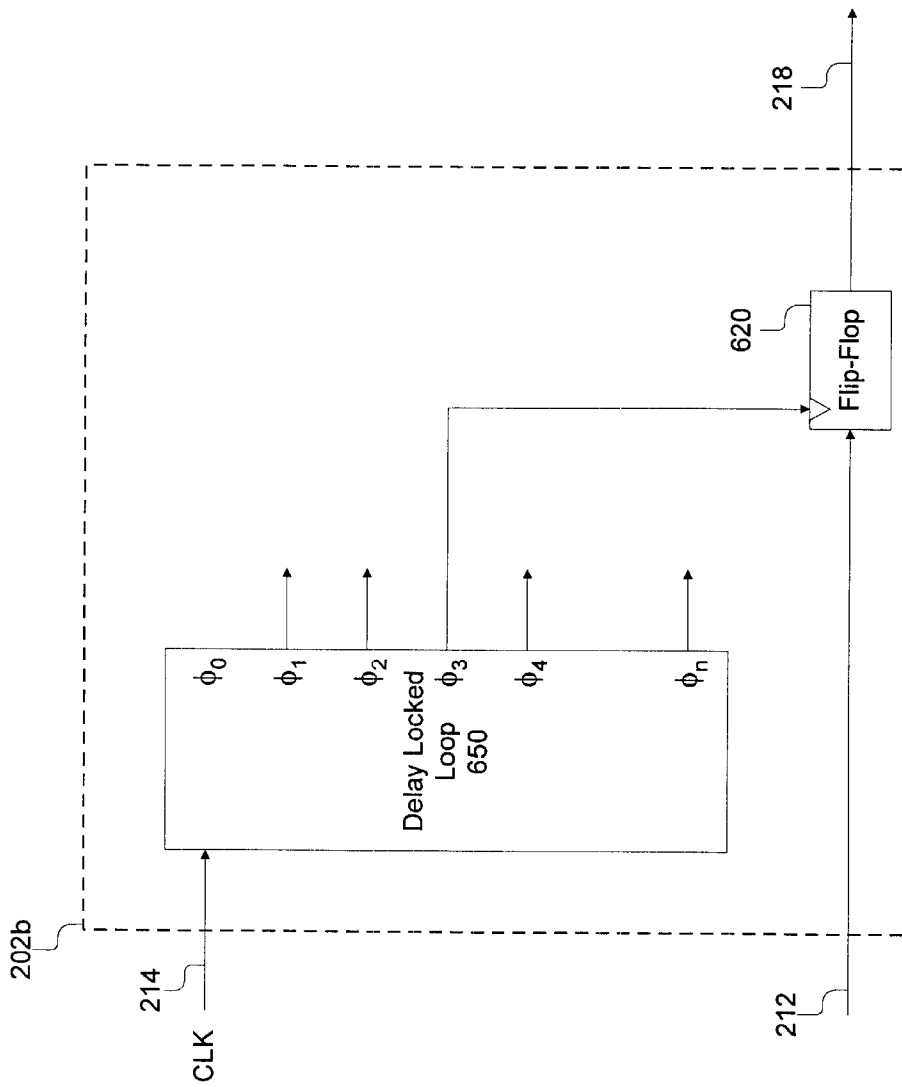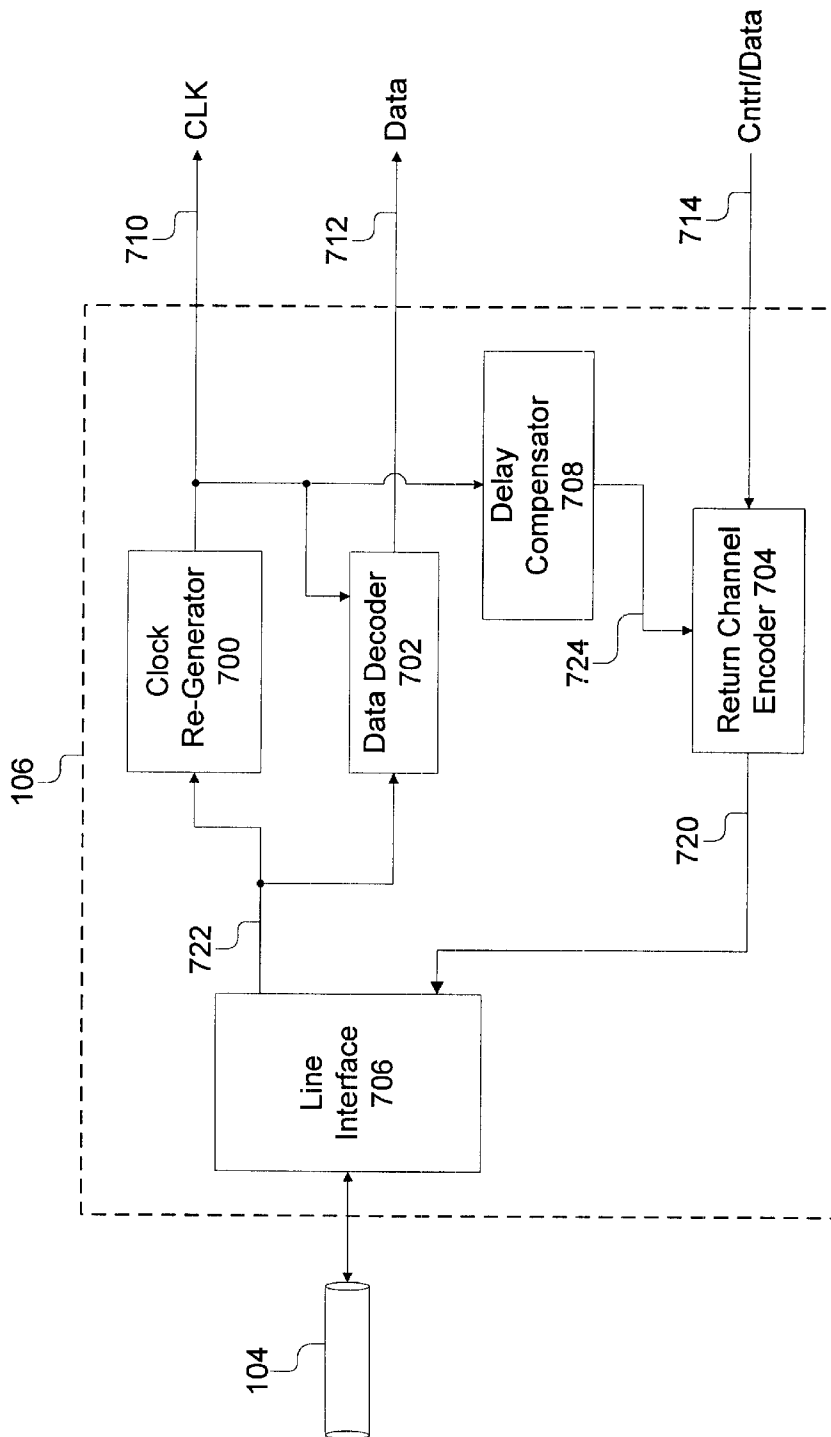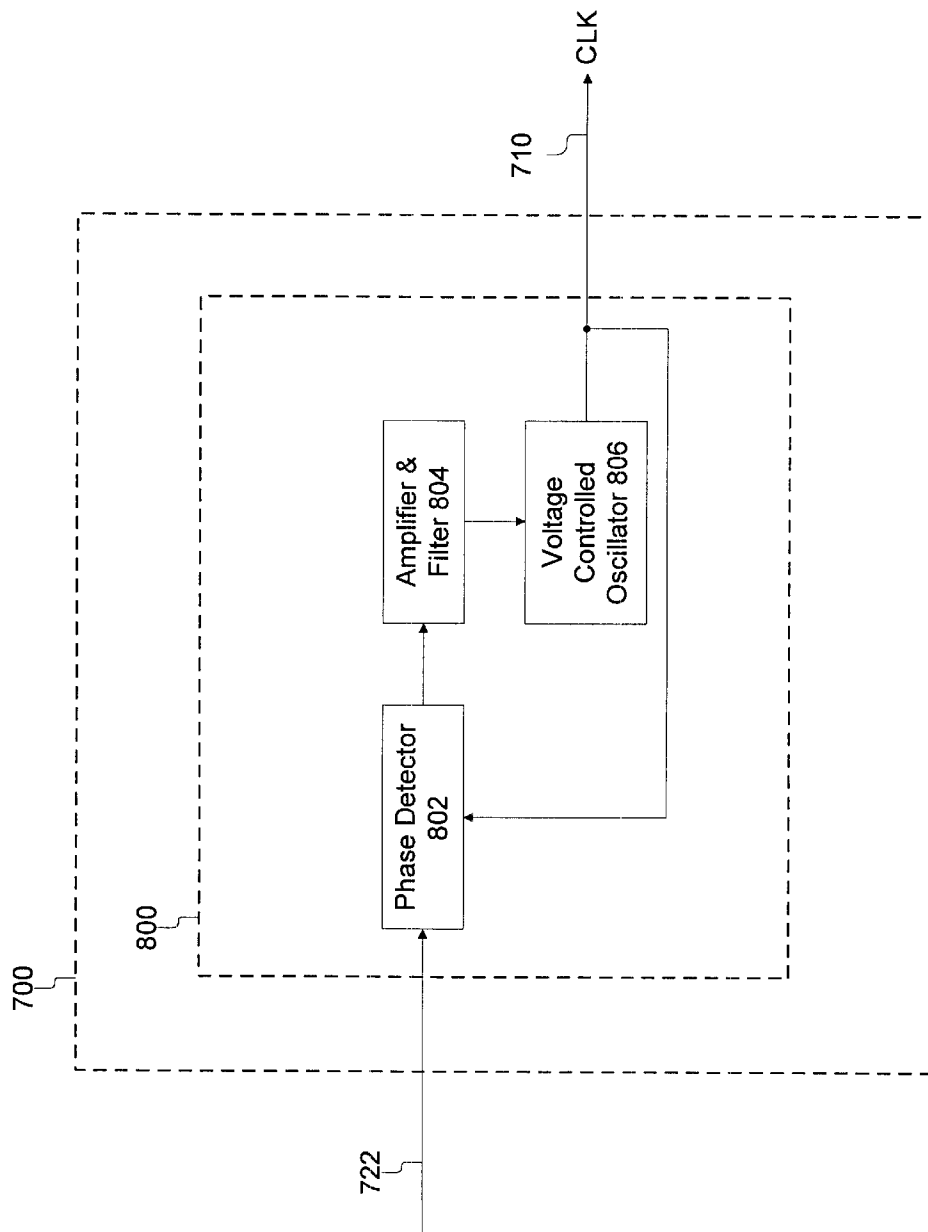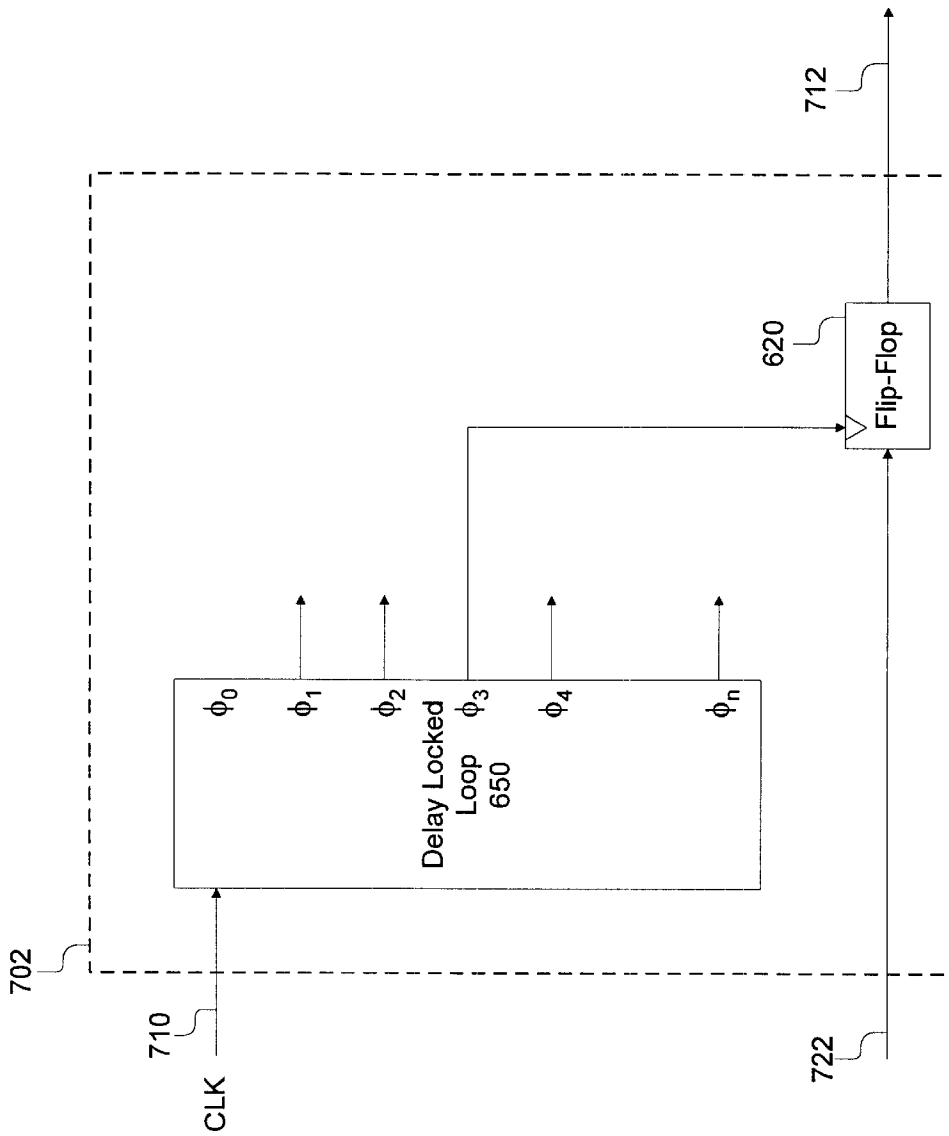
Figure 6B

Figure 7

Figure 8

Figure 9

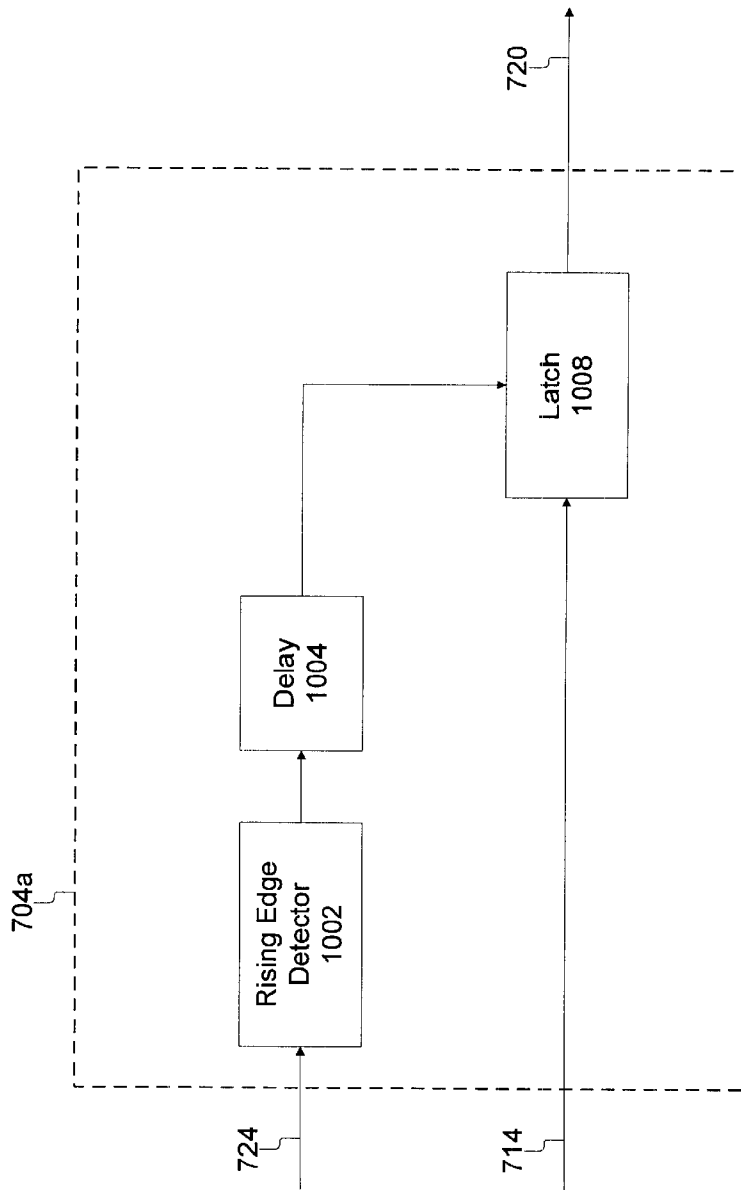Figure 10A

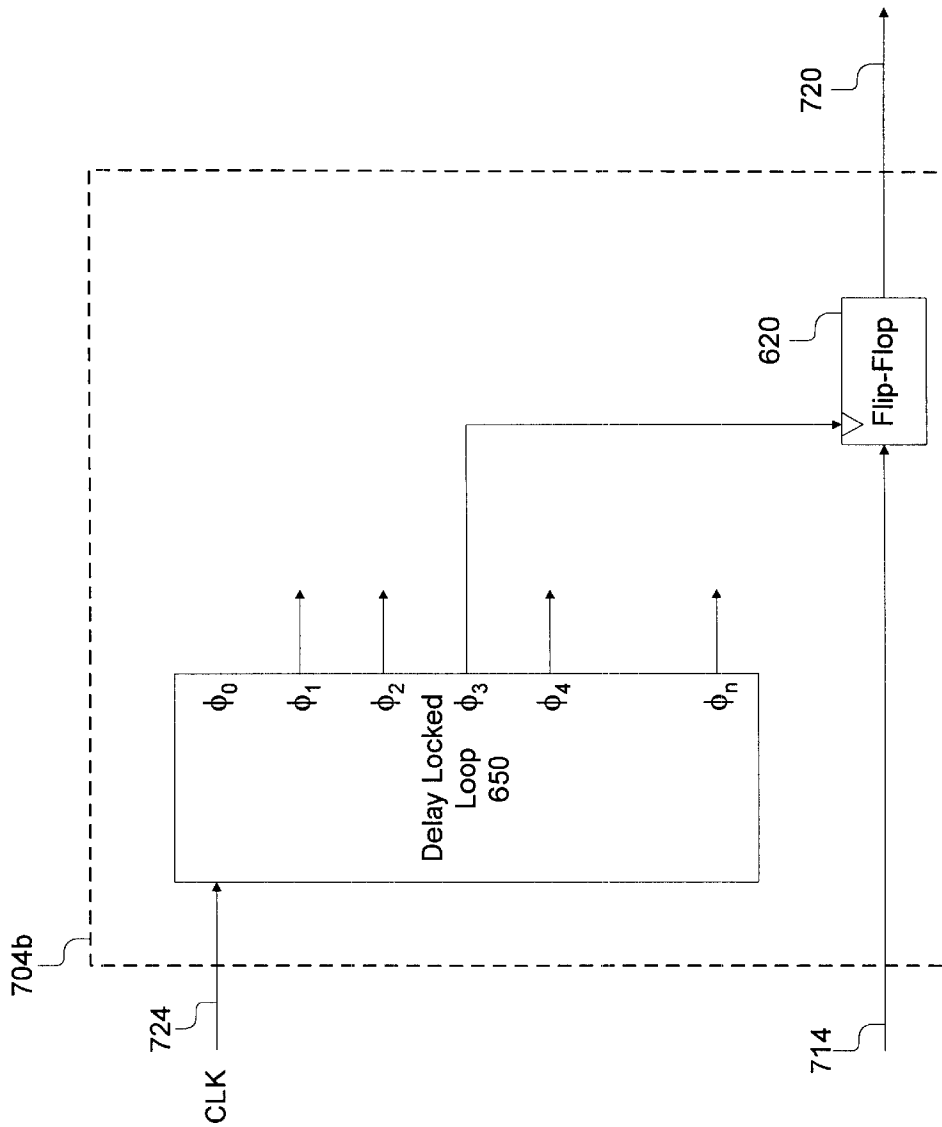Figure 10B
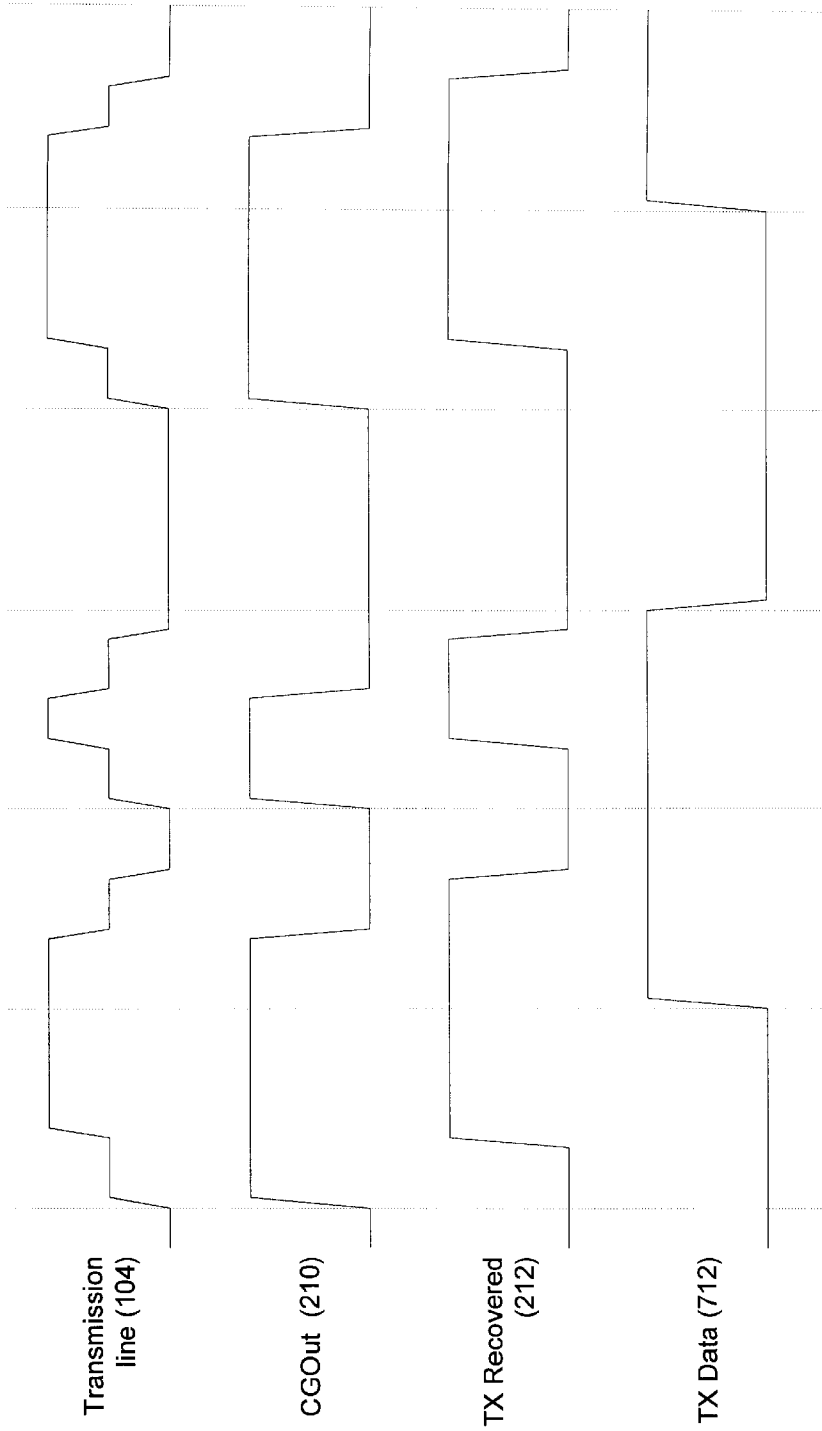
Transmission line (104)

CGOut (210)

TX Recovered (212)

TX Data (712)

Figure 11A

Transmission line (104)

RX Out (720)

RX CLK (710)

RX Data (712)

Figure 11B

Transmission line (104)

CGOut (210)

TX Recovered (212)

TX Data (712)

Figure 12A

Figure 12B

Transmission line (104)

RX Out (720)

RX CLK (710)

RX Data (712)
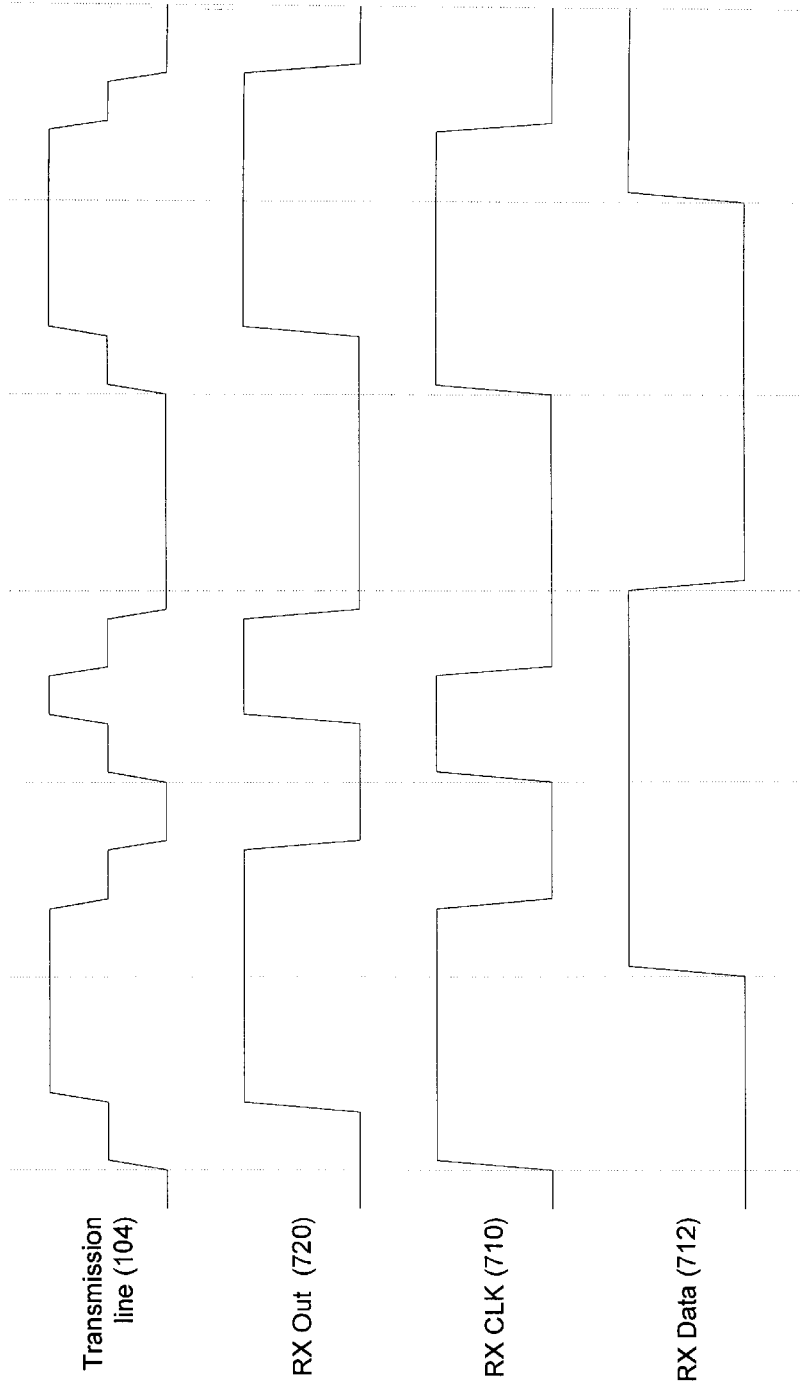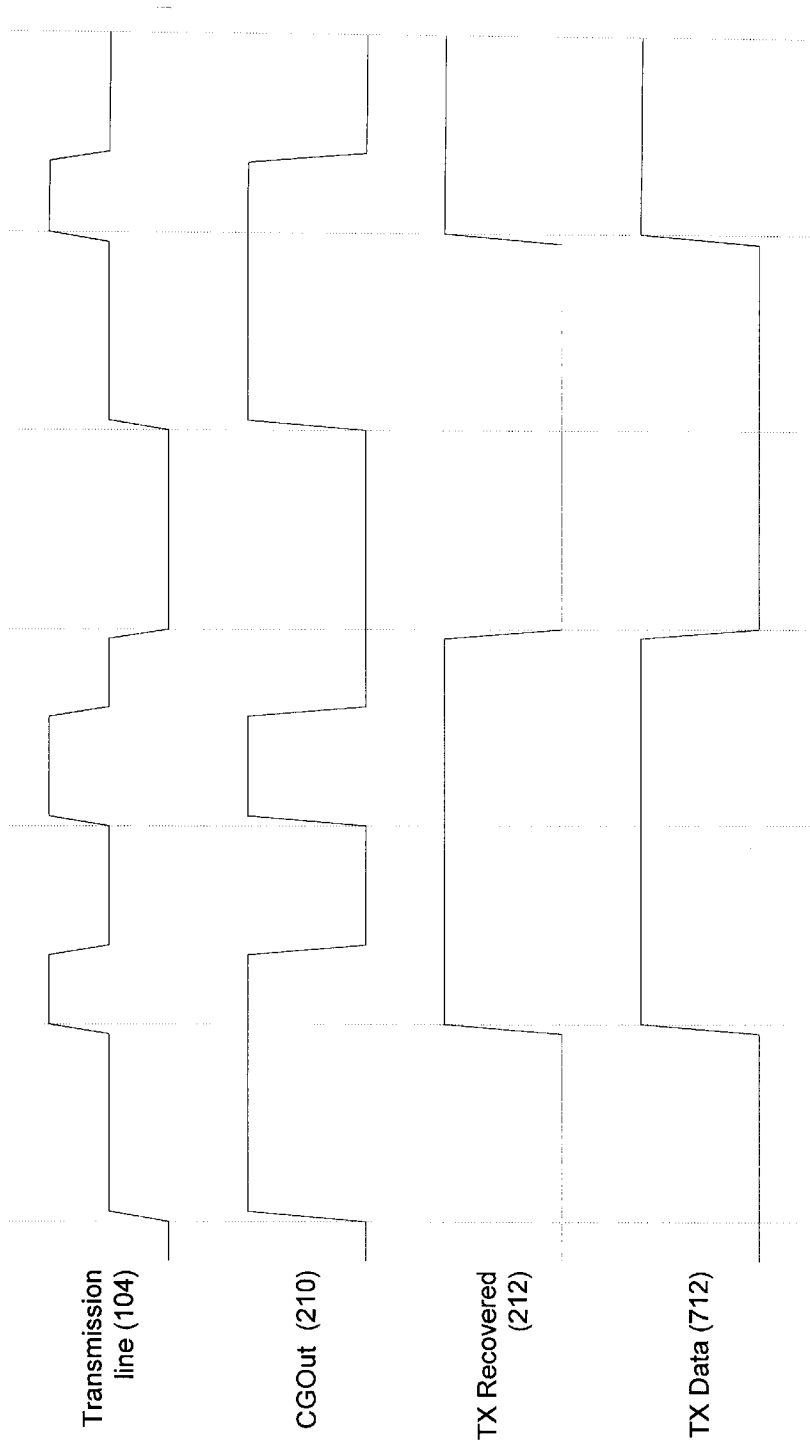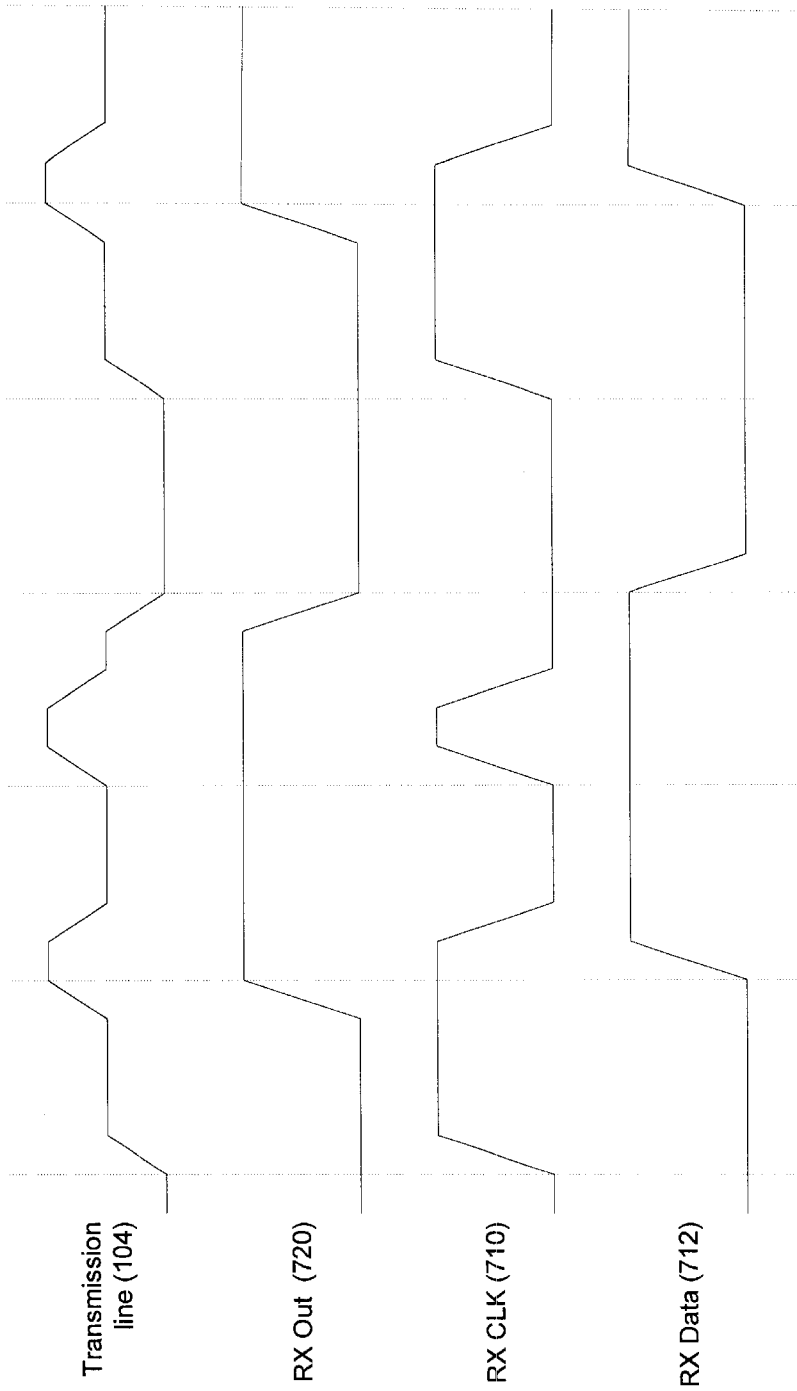
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SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA SIGNALS OVER A CLOCK SIGNAL LINE

This application claims benefit of provisional No. 60/099,770 filed Sep. 10, 1998.

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a utility conversion of U.S. Pat. No. 60/099,770, entitled "Embedded Back Channel For TMDS" by Gyudong Kim, filed Sep. 10, 1998.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of data communications, and more particularly, to the transmission of clock and data signals. Still more particularly, the present invention relates to the transmission of clock signals and data signals on the same transmission line in transition minimized differential signaling (TMDS) system.

2. Description of the Background Art

There are a variety of prior art systems and method for transmitting data between a transmitter and a receiver. Various serial links and other methods for transmitting data and clock signals are well known. However, most such schemes provide a single line or channel dedicated for the transmission of the clock signals and other signal lines or channels dedicated for the transmission of data. Once such system is described by Kyeongho Lee, Sungjoon Kim, Gijung Ahn, and Deog-kyoon Jeong in "A CMOS Serial Link For Fully Duplexed Data Communication," IEEE Journal of Solid State Circuits, Vol. 30, No. pp. 353–364, April 1995.

The present invention will be discussed in the context of transition minimized differential signaling (TMDS), however, those skilled in the art will recognize that the present invention is applicable in various other data communication contexts. In TMDS, four signal lines are provided, and each signal line is preferably a differential pair. One signal line is a for a low speed clock signal and the three other signal lines are for high-speed data transmission.

One important aspect of all data communication systems is to maximize the bandwidth provided by the data. channels. However, most systems include a variety of control signals that must be sent between the transmitter and the receiver to ensure proper operation, and maintain synchronization between the transmitter and the receiver. For example, it is not uncommon for as much as 20% of the bandwidth to be used for framing and synchronization in serial communication. One problem is that the bandwidth available for data is typically reduced because the data signal lines must be used to transmit these control signals between the transmitter and receiver. Yet another problem is latency in transmitting the control signals to the recipient. Especially in video data communication, much of the data must be transmitted in blocks during which control signals cannot be sent. For example, when transmitting data from a controller to a flat panel, the data is transmitted, and then there is a data enable period corresponding to the blanking period in CRT display that is used to send control and synchronization signal. Only during that data enable period can the control signals be sent under most protocols. Therefore, there is latency imposed on transmitting control signals to the receiver. Thus, there is need for a system that

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can provide for control signaling between the transmitter and the receiver without decreasing the available bandwidth for data transfer, and while reducing the latency in sending control signals.

Yet another problem in the prior art is that most systems do not provide a mechanism to get signals from the receiver back to the transmitter. In other words, there is not a return channel for communication. Some systems have provided additional signal lines, however, their addition and interface add significant complication, require re-wiring and create other problems that make the addition of a physical line unworkable. Another approach is to add a second transmitter, second receiver and signal lines. However, this essentially doubles the hardware requirements making such a solution too expensive. Furthermore, such duplication is overkill for the amount of data that needs to be sent between the transmitter and the receiver, especially when the application is one of sending video data from a transmitter to a receiver such as communication between a graphic controller and a video display device.

Therefore, there is a need for a system and method for that uses the clock signal line also for transmitting data signals between the transmitter and the receiver and vice-versa.

SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies and limitations of the prior art with a unique data communication system. The system preferably includes a unique transmitter and receiver coupled by a transmission line. The transmitter sends both a clock signal and data signals over the transmission line to the receiver. The receiver uses the same transmission line to send data signals back to the transmitter.

The transmitter preferably comprises a clock generator, a decoder and a line interface. The clock generator produces a clock signal that includes a variable position falling edge. The falling edge position is decoded by the receiver to extract data in addition to the clock signal. The line interface couples the output of the clock generator to the transmission line. The line interface also couples the transmission line to the decoder and in doing so removes the signals from the clock generator. The decoder receives the signals from the line interface and decodes the signal to determine the data being sent from the receiver to the transmitter on the same line used to send the clock and data from the transmitter to the receiver.

The receiver preferably comprises a line interface, a clock re-generator, a data decoder and a return channel encoder. The clock re-generator, the data decoder and the return channel encoder are coupled to the transmission line by the line interface. The clock re-generator monitors the transmission line, receives signals, filters them and generates a clock signal at the receiver from the signal on the transmission line. The data decoder similarly is coupled to receive the signals on the transmission line, and filters and decodes the signals to produce data signals. This is preferably done by determining the position of the falling edge of the clock signal and translating the falling edge position into bit values. In contrast, the return channel encoder generates signals and asserts them on the transmission line. These signals are asserted or superimposed over the clock & data signals provided by the transmitter.

These and other features and advantages of the present invention may be better understood by considering the following detailed description of a preferred embodiment of the invention. In the course of this description, reference will frequently be made to the attached drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of system including the combined clock and data signal line of the present invention.

FIG. 2 is a block diagram of a portion of the transmitter showing a clock generator, decoder and a line interface.

FIG. 3 is a block diagram of a preferred embodiment of the clock generator constructed in accordance with the present invention.

FIG. 4 is a timing diagram illustrating various clock signals that the clock generator of the present invention produces.

FIG. 5A is a block diagram of a preferred embodiment of the line interface constructed in accordance with the present invention.

FIG. 5B is a circuit diagram of the preferred embodiment of the line interface constructed in accordance with the present invention.

FIG. 6A is a block diagram of a first embodiment of the decoder at the transmitter constructed in accordance with the present invention.

FIG. 6B is a block diagram of a second embodiment of the decoder at the transmitter constructed in accordance with the present invention.

FIG. 7 is a block diagram of a first embodiment of portions of the receiver relating to the present invention.

FIG. 8 is a block diagram of a first embodiment of a clock re-generator of the receiver.

FIG. 9 is a block diagram of a preferred embodiment of a data decoder of the receiver.

FIG. 10A is a block diagram of a first embodiment of a return channel encoder of. the receiver.

FIG. 10B is a block diagram of a second and alternate embodiment of a return channel encoder of the receiver.

FIG. 11A is a timing diagram illustrating signals on the transmission line, and the clock and data signals generated by the transmitter for return to zero signaling.

FIG. 11B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the clock and data signals recovered by the receiver for return to zero signaling.

FIG. 12A is a timing diagram illustrating signals on the transmission line, and the clock and data signals generated by the transmitter for non-return to zero signaling.

FIG. 12B is a timing diagram illustrating signals on the transmission line, the data signal sent by the receiver, and the clock and data signals recovered by the receiver for non-return to zero signaling.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, a block diagram of system 100 including the combined clock and data signal line of the present invention is shown. The system 100 preferably includes a transmitter 102, a clock transmission line 104, a receiver 106 and one or more data transmission lines 108. The transmitter 102 preferably provides a clock signal as well as data signals to the receiver 106 via the clock transmission line 104. These data signals are in addition to those provided to the receiver 106 via the high speed data transmission lines 108. The receiver 106 receives the signals on the transmission line 104 and from them, generates the clock and data signals at the receiver 106. These data signals on the clock line 104 are again in addition to the data signals

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that the receiver 106 recovers from the data transmission line 108. The transmitter 102 and the receiver 106 include logic for sending and receiving the data from data transmission line 108. This logic preferably includes transition control, DC balancing, and encoding/decoding in a conventional manner. For example, in addition to the components of the present invention for receiving and sending data and clock signals on the clock transmission line 104 that will be described below, the transmitter 102 and the receiver 106 respectively include conventional data transmission logic for TMDS such as that provided in PanelLink by Silicon Image of Cupertino, Calif. For ease of understanding that logic and the data transmission line 108 are omitted from the discussion below and the remaining figures. Those skilled in the art will also realize that while shown as a single line, the clock transmission line 104 and the data transmission line 108 are preferably each a differential pair of signal lines, and the signal is carried on the differential pair of lines. Furthermore, those skilled in the art will understand the preferred embodiment for the data transmission line 108 is three pairs of data lines.

Transmitter

Referring now to FIG. 2, a preferred embodiment of the transmitter 102 is shown in more detail. The transmitter 102 preferably comprises a clock generator 200, a line interface 204, and a decoder 202.

The clock generator 200 has a first input, a second input and an output. The clock generator 200 produces a clock signal that is encoded with data. The data is encoded into the clock signal by varying the modulation of the falling edge of the clock signal. In other words, the position of the falling edge of the clock relative to the rising edge indicates different data values. This is particularly advantageous because it preserves the rising edge of the clock for clock recovery. All the activity for a bi-directional data link on the clock transmission line 104 is centered around the falling edge of the clock from the transmitter 102. While most of the present invention will be described in the context of the falling edge of the clock having two different positions, FIG. 3 and will also be described in the context of the falling edge of the clock having five different positions. Each of the four positions representing two bit values and one position representing no data. The first input of the clock generator 200 is coupled to line 214 to receive a clock signal either from another portion of the transmitter 102 or from a oscillator or other conventional clock source. The second input of the clock generator 200 is coupled to line 216 to receive control/data signals. These control/data signals dictate the data or no data that is transmitted as part of the clock signal. These control/data signals may be from another portion of the transmitter 102 or from off chip control logic. The output of the clock generator 200 is provided on line 210 that is coupled to an input of the line interface 204. The output of the clock generator 200 provides a CGOut signal.

While the present invention is described throughout this application as preserving the rising edge for the clock signal and centering all the bi-directional data transmission about the falling edge, those skilled in the art will realize that an inverse scheme where the falling edge is preserved for recovering the clock and changes in position of the rising edge is used for encoding data is within the spirit and scope of the present invention.

The line interface 204 has an input, an output and a bi-directional port. The line interface 204 couples the clock generator 200 and the decoder 202 to the clock transmission line 104. The input of the line interface 204 preferably couples line 210 to the clock transmission line 104 so that

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the CGOut signal may be asserted over the clock transmission line **104**. The output of the line interface **204** is coupled to the input of the decoder **202** by line **212**. The line interface **204** advantageously receives the signal on the clock transmission line **104**, removes the CGOut signal as will be described below with reference to FIGS. **5A** and **5B**, and sends the filtered signal as the input to the decoder **202**. The bi-directional port of the line interface **204** is coupled to the clock transmission line **104**..

The decoder **202** receives the filtered signals from the transmission line **104** and decodes the signals to generate the data sent by the receiver **106**. The decoder **202** preferably performs an inverse function to the encoder **704** (See FIG. **7**) of the receiver **106** as will be described below.

Referring now to FIGS. **3** and **4**, the preferred embodiment for the clock generator **200** will be described. While the clock generator **200** will now be described as providing a clock signal having a falling edge in five possible locations to send two bits of data or no data in addition to the clock signal, those skilled in the art will recognize that this is only by way of example. The clock generator **200** could be configured to send from 1 to n bits of data per clock cycle depending on the clock frequency and the number of possible locations for the falling edge of the clock signal. In general, n locations of the falling edge will allow up to $\log_2 n$ bits of data to be transferred per clock cycle. The number of locations for the falling edge is limited only in that the first location must be such that the pulse width is greater than the logic-threshold crossing time of the rising edge, which may be viewed to be jitter by the phase-locked loop at the receiver **106**. In other words, the thresholds for set up and hold time in the logic must be sufficient to recognize a rising edge as the beginning of the clock cycle.

The clock generator **200** preferably generates a clock signal at the dot clock frequency, or the frequency used by device (not shown) connected to the receiver **106** for the display of the data. The maximum symbol rate provided by data transfer as part of the clock signal matches the dot clock frequency. For example, if the dot clock is 100 MHz, the symbol rate is 100 Msymbols/s. The actual data rate will depend on the modulation methods and the number of bits per clock or symbol that can be sent. If simple binary modulation is used, then the bit rate is the same and the clock rate with would provide an additional 100 Mb/s for control signals.

The clock generator **200** preferably comprises a monostable multivibrator **306**, a delay-locked loop **300**, a multiplexer **302**, a first NAND gate **304** and a second NAND gate **306**. The clock generator **200** preferably uses only return to zero signaling for sending the clock and data signals. Non-return to zero signaling cannot be used for sending from the transmitter **102**. The clock signal is received on line **214** and provided as input to the input of the one shot or monostable multivibrator **306**. The monostable multivibrator **306** is provided to generate a signal with a narrower pulse width than the clock signal. This is advantageous for use in other portions of the clock generator **200**. In an alternative embodiment, the one shot **306**, may be replaced by a plurality of monostable multivibrators each respectively coupled in series with an output signal line **308** of the delay locked loop **300**. Such an alternate embodiment provides more flexibility in the design of the delay locked loop **300** at the cost of additional monostable multivibrators will be understood by those skilled in the art. The output of the monostable multivibrator **306** is coupled to the input of the delay-locked loop **300**. The delay-locked loop **300** is of a conventional type and in response to a signal at its input,

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provides a plurality of outputs, each output being the same as the input only shifted in phase. The falling edge is modulated using a delay-locked loop **300**. The falling edge is chosen from one of the phases provided by the delay-locked loop **300**. It is preferable that the selected phases from the delay-locked loop **300** be the ones close to a 50% duty cycle. The delay-locked loop **300** preferably provides five output signals: φ0, φ1, φ2, φ3, φ4, and φn. The φ0 signal is the clock signal unchanged. The φ1, φ2, φ3, φ4, and φn are each phase shifted more with respect to the previous φ signal. The φ0 is coupled to a first input of the first NAND gate **304**. The output of the first NAND gate **304** is provided on line **210** and provides the CGOut signal. The first NAND gate **304** is cross coupled with the second NAND gate **306** to form a set-reset latch. A rising edge on the φ0 causes the output of first NAND gate **304** to be set high or asserted until reset to low by the second NAND gate **306**. The remaining signals from the delay-locked loop **300**, φ1, φ2, φ3, φ4, and φn are coupled to respective data inputs of the multiplexer **302**. The control input of the multiplexer **302** is coupled to line **216** to receive control/data signals. In response to the control/data signals on line **216**, the multiplexer **302** will couple one of the signals from the delay-locked loop **300**, φ1, φ2, φ3, φ4, and φn, to the input of the second NAND gate **306**. Thus, the rising edge on the selected signal from the delay-locked loop **300**, φ1, φ2, φ3, φ4, and φn, will cause the latch to be reset and create a falling edge on the output of the first NAND gate **304**, and thus, line **210**. Thus, it is apparent that using the control/data signals to select one of the signals, the position of the falling edge can be selected. For example control signals such as shown in Table I may be used to control the position of the falling edge.

TABLE I

Control/data Signal (216)	NAND-gate 306 input	Falling edge Position	Data Sent
000	φ1	T0	00
001	φ2	T1	01
100	φ3	T2	00
010	φ4	T3	10
011	φn	T4	11

Those skilled in the art will recognize how the clock generator **200** could be modified to create any number of different falling edge positions for the CGOut signal. Referring also to FIG. **4**, a timing diagram of the clock/φ0, φ1, φ2, φ3, φ4, and φn and the possible CGOut signals are shown. There are five possible CGOut signals. First, the clock/φ0 signal is unchanged which is just the input signal with falling edge at time T2 and sending no data. The remaining CGOut1–CGOut4 signals are have a falling edge with an adjusted position to times T0, T1, T3, T4 respectively each representing a different two bit value. Thus, the preferred embodiment is able to transfer two bits per clock from the transmitter **102** to the receiver **106** in addition to the clock signal. Since the receiver **106** uses only the rising edge to detect and define clock cycles, the present invention uses this to achieve the data transfer without any performance disadvantages. For the receiver **106** embodiments described below where only one bit of data per clock is sent, the clock generator **200** would output falling edges at times T1 and T3.

The ability of the present invention to use the clock transmission line **104** to send data from the transmitter **102** to the receiver **104** is particularly advantageous because it eliminates signal latency present in the prior art. With the present invention as applied to TMDS, the transmitter **102** does not need to wait for the next available data enable (DE)

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low period to send the signals. This greatly decreases the maximum transfer latency. Moreover, the present invention can be used in other serial links that require very short latency. For example, if a fixed bit location is assigned for each link (a fixed bandwidth per fixed dot clock) the synchronization overhead for those channels can be minimized. In this way, the latency of such links can be reduced to 1 frame cycle and the cable flight time. The other bits of the payload can be used with variable bandwidth but the synchronization latency or delay could be longer.

Yet another advantage of the forward channel for sending data from the transmitter 102 to the receiver 106 is that it is fully backward compatible with prior TMDS designs and protocols. Thus, whether the receiver 106 is able to receive data from the transmitter 102 or not, the clock signal is unaffected by the addition of data to the signal. Moreover, a receiver 106 will not have a problem recovering the clock even if data (for either the transmitter 102 or the receiver 106) is added in accordance with the present invention to the signal on the transmission line 104. Therefore, the transmitter 102 of the present invention can still be used even if the receiver does not have the capability to receive the data signal.

Referring now to FIGS. 5A and 5B, the preferred embodiment for the line interface 204 is shown. The line interface preferably comprises a first amplifier 502, a second amplifier 506, a differential amplifier 504 and a line terminator or pull-up resistor 508. The line interface 204 is essentially a bi-directional bridge that allows transmission of data while receiving data from the receiver 106. The input of the first amplifier 502 is coupled to line 210 to receive the CGOut signal. The input of the second amplifier 506 is similarly coupled. The output of the first amplifier 502 is coupled to apply an amplified version of the CGOut signal to clock transmission line 104. The clock transmission line 104 is also coupled by the pull-up resistor 508 to high voltage to form a line terminator. The pull-up resistor 508 could instead be coupled to ground or half V_{DD} as will be understood to those skilled in the art for alternate embodiments of the line terminator. The clock transmission line 104 is also coupled an input of the differential amplifier 504. The other input of the differential amplifier 504 is coupled to the output of the second amplifier 506. The second amplifier 506 also receives the CGOut signal and amplifies the signal, but to the same or lesser extent than the first amplifier 502. The differential amplifier 504 subtracts the CGOut signal from the signal received from the clock transmission line 104. Thus, the output of the differential amplifier 504 that is provided on line 212 includes predominately the signals asserted by the receiver 106 on the clock transmission line 104 and not the CGOut signal. It should be noted that an identical circuit with inputs and output coupled differently may also be used in the receiver 106 as will be described below with reference to FIG. 7.

Referring also now to FIG. 5B, a circuit diagram for one exemplary embodiment for the line interface 204 is shown. The connections to the signal lines 210 and 104 are shown with reference numerals for clarity and ease of understanding. The signals preferably use differential pairs are indicated by reference numerals "a" and "b" as will be understood to those skilled in the art. The transistors and other components forming the second amplifier 506 and the differential amplifier 504 are shown grouped within dashed boxes as will be understood to those skilled in the art. The remaining transistors and other components from the first amplifier (not labeled in FIG. 5B). It should be noted that some of the transistors in the second amplifier 506 are for

impedance matching, and have their gates coupled to signal line 522 to be biased for impedance matching in a conventional manner. Some of the transistors in the differential amplifier 504 are also coupled to line 520 for biasing. In alternate embodiments, the outputs of the differential amplifier 504 could be coupled to line 520 and thereby provide a single output signal as will be realized by those skilled in the art. Those skilled in the art will further recognize that in alternative embodiments, various other conventional bi-directional buffers could be used in place of the circuits shown in FIGS. 5A and 5B.

Referring now to FIGS. 6A and 6B, two alternate embodiments for the decoder 202 are shown. The embodiment for the decoder 202 is dependent on the type of signaling being used by the corresponding encoder 704 (See FIG. 7 and below) in the receiver 106. FIG. 6A shows. a block diagram of the first embodiment of the decoder 202a at the transmitter 106 for use when the receiver 106 sends the data in a non-return to zero (NRZ) signaling. As shown in FIG. 6A, when the receiver 106 sends data in NRZ (non-return to zero) manner and toggles data at the fictitious falling edge (since the clock toggles its falling edge randomly in accordance with the present invention), since the delay is a function of cable delay, at the transmitter side, it is not predictable where the relative location of the data transition will be, even though it may have been obvious at the receiver side. Because of this ambiguous delay, the decoder 202a oversamples the data provided from the clock transmission line 104/212. Since the incoming data rate is the same as outgoing data rate, the present invention generates multiple phases of clocks from the clock signal on line 214. Using these clocks, the signal line 212 is sampled multiple times per data period to locate a data transition. Once the transition is detected, it is used as the data boundary.

As shown in FIG. 6A, the first embodiment of the decoder 202a preferably comprises a delay-locked loop 602, a sampling unit 604, a data generator and a transition detector 608. The delay-locked loop 602 has an input coupled to receive the clock signal on line 214. The same delay-locked loop could be used in both the clock generator 200 and the decoder 202. The delay-locked loop 602 is of a conventional type and provides a plurality of phase shift clock signals. Outputs of the delay-locked loop 602 are coupled to respective inputs of the, sampling unit 604. The sampling unit 604 includes control logic for generating a signal on a first output that controls when the transition detector 608 samples and latches the signal on line 212. For example, the sampling unit 604 can generate this control signal for every rising edge seen at the input from the delay-locked loop 602. The first output is coupled to an input of the transition detector 608. The sampling unit 604 also provides a time signal on a second output indicating the signals from the delay-locked loop 602 that have transitioned, and thus, the time within the clock cycle. The second output of the sampling detector 604 is coupled to an input of the data generator 606. The transition detector 608 has an input coupled to line 212 to receive the signal from the receiver 106. The transition detector 608 detects transitions in the signals on the line 212. When a transition is present the transition detector 608 asserts its output. The data generator 606 is coupled to the sampling unit 604 to receive a signal indicating the time within the clock cycle and the transition detector 608 to identify when the transition occurs. Using this information, the data generator 606 outputs the bit values corresponding to when the transitions occur. For example if the transition is before the time for a falling edge of the clock if it had a 50% duty cycle then the data generator 606 may output a 1

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if after the data generator **606** could output a 0 if the data rate were one bit per clock cycle. Those skilled in the art will recognize how the data generator **606** could be modified according to the number of bits per clock cycle transmitted by the receiver **106**. The output of the data generator **606** is provided on line **218** for use by the transmitter **102**.

FIG. 6B shows an alternate embodiment for the decoder **202**a. When receiver **106** sends data in return to zero (RZ) manner, the rising edge of the incoming clock is preferably used as the data reference point, and a phase in the middle of those consecutive rising edges is generated and used to sample the incoming data at that point. Thus, the decoder **202**a comprises merely a delay-locked loop **650** and a flip-flop **620**. The delay-locked loop **650** preferably provides a signal that has a rising edge in about the middle of the clock cycle such as φ**3**. This signal is coupled to the clock input of the flip-flop **620** to cause the flip-flop **620** to latch near the middle of the clock cycle. The data input of the flip-flop **620** is coupled to line **212** to receive the data signal sent by the receiver **106** and the D output of the flip-flop **620** provides the data output and is coupled to line **218**.

Those skilled in the art will recognize that the decoder **202** may alternatively be formed as an integrator type receiver where the period of the clock is subdivided and the integrator integrates over the subdivided time periods and compares the integration results. The signal is effectively integrated and dumped for comparison to determine the data values.

Receiver

FIG. **7** shows a preferred embodiment for the receiver **106** constructed in accordance with the present invention. The receiver **106** preferably comprises a line interface **706**, a clock re-generator **700**, a data decoder **702**, a delay compensator **708** and a return channel encoder **704**.

The line interface **706** is preferably identical to that described above with reference to FIGS. **5A** and **5B**. However, for the receiver **106**, the line interface **706** is completely optional and the receiver **106** can operate without it. The line interface **706** buffers the signals and filters them for better use in recovery. The line interface **706** has an input, an output and a bi-directional port. The bi-directional port is coupled to the clock transmission line **104**. The input of the line interface **706** is coupled to line **720** to receive the output of the return channel encoder **704**. The output of the line interface **706** is coupled to line **722** to provide input signals to the clock re-generator **700** and the data decoder **702**. For ease of understanding reference numerals for the line interface **706** have been added to FIG. **5A**.

The clock re-generator **7.00** has an input and an output. The input of the clock re-generator **700** is coupled to receive the signals on the clock transmission line **104** via line **722** from the line interface **706**. The clock re-generator **700** monitors the transmission line **104**, receives signals, filters them and generates a clock signal at the receiver **106**. The output of the clock re-generator **700** is coupled to line **710** and provides the clock signal for the receiver **106** to use in recovering data from the data channels **108**. The clock re-generator **700** advantageously only uses the rising edges of the signals on the transmission line **104** to regenerate the clock signal at the receiver **106**. This allows the falling edge position and voltage level to be used for other data transfer. The preferred embodiment for the clock re-generator **700** is simply an amplifier that can provide an amplified version of the signal to other digital logic receiving the clock. Referring now also to FIG. **8**, another embodiment for the clock re-generator **700** is shown. In FIG. **8**, the clock re-generator **700** is a phase-locked loop **800** that has an input that is coupled to the transmission line **104** and an output that

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provides the clock as a square wave. The phase-locked loop **800** is a conventional type and includes a phase detector **802**, an amplifier and filter **804** and a voltage controlled oscillator **806**. These components **802, 804, 806** are coupled in a conventional manner with the input of the phase detector **802** coupled to line **104** and the output of the voltage controlled oscillator providing the clock signal and being feed back to the phase detector **802**. Those skilled in the art will recognize that various other embodiments of phase-locked loops could be used for the clock re-generator **700** since it is only necessary to detect the rising edges on the transmission line **104** and produce a clock signal therefrom. Alternate embodiments for the clock re-generator **700** could also use a delay-locked loop.

The data decoder **702**, like the clock re-generator **700**, has an input coupled to receive the signals on the transmission line **104** via line **722** from the line interface **706**. The data decoder **702** filters and decodes the signals to produce data signals that are output on line **712**. The data decoder **702** also has another input coupled to line **710** to receive the recovered clock signal from the clock re-generator **700**. This is preferably done by determining the position of the falling edge of the clock signal and translating the falling edge position into bit values. The data being sent from the transmitter **102** to the receiver **106** is valid on the falling edge of the clock. Referring also now to FIG. **9**, a preferred embodiment for the data decoder **702** will be discussed. The preferred embodiment of the data decoder **702** is very similar to the second embodiment of the decoder **202**b of the transmitter **102**. The data decoder **702** differs only in its coupling to other components which is shown in FIG. **9**. The data decoder **702** includes a delay-locked loop **650** and a flip-flop **620**. The clock input of the delay-locked loop **650** is coupled to line **710** to receive the regenerated clock signal. The data input to the flip-flop **620** is coupled to line **722** to receive the filter data signals from the transmission line **104**. The output of the flip-flop **620** provides the data output and is coupled to line **712**. The operation is the same as has been described above with reference to FIG. **6B**.

The delay compensator **708** is coupled to line **710** to receive the recovered clock signal. The delay compensator **708** adjusts the recovered clock signal to compensate for propagation delay over the transmission line **104** and propagation delay in recovering the clock such that the signal used to time the sending of data back to the transmitter **102** will have timing that matches the original clock signal on the transmitter side of the clock transmission line **104**. The output of the delay compensator **708** provides an adjusted clock signal and is used by the return channel encoder **704**. In a preferred embodiment, the delay compensator **708** is a phase-locked loop with a delay circuit in the feedback loop between the voltage-controlled oscillator and the phase detector, as will be understood to those skilled in the art. Such a configuration provides negative delay so that the clock signal for return channel signals is moved ahead so that with propagation delay it will matches the timing of the CGOut signal at the transmitter **102**.

The return channel encoder **704** generates signals and asserts them on the transmission line **104** via line **720** and the line interface **706**. The return channel encoder **704** has a data input coupled to line **714** to receive the control and data signals for the data to be sent on the return channel. The return channel encoder **704** also has a clock input coupled by line **724** to the output of the delay compensator **708** to receive a modified clock signal for timing the assertion of data and change in data states. These signals are asserted or superimposed over the clock & data signals provided by the

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transmitter **102**. The return channel encoder **704** advantageously sends data back to the transmitter **106** on the falling edge of the clock thereby preventing the return channel **704** from causing any jitter on the clock signal. More specifically, the return channel encoder **704** minimizes transition activity only around the rising edge of the clock, and minimizes activity by fixing the polarity around the rising edge. This is accomplished by including a delay-locked loop in the return channel encoder **704**. The return channel encoder **704** advantageously places data on the transmission line **104** or clock pair in the form of voltage signal and not edge position, thus reducing any interference and effect on the transmission of the clock and data signals by the transmitter **102**.

Referring now to FIG. **10A**, a first embodiment of the return channel encoder **704***a* is shown. The first embodiment return channel encoder **704***a* provides the minimum functionality for transmission. For example, the return channel encoder **704***a* could be a 1-bit link. This has a low data rate and does not allow DC balancing, however it is advantageous because there is no latency (once the data is at the transmitter there is no latency due to decoding) in getting the data and it is simple to implement. The first embodiment of the return channel encoder **704***a* includes a rising edge detector **1002**, a delay circuit **1004** and a latch **1008**. The rising edge detector **1002** has an input coupled to line **724** to receive a signal for timing the changing of the data output. The rising edge detector **1002** detects the rising edge and then asserts its output upon receiving rising edge. The output of the rising edge detector **1002** is coupled to the input of a delay circuit **1004**. The delay circuit delays the signal output of the rising edge detector **1002**, such as by half the clock period. Thus, the output of the delay circuit **1004** is at a time of an ideal falling edge if the clock were to have a 50% duty cycle. The output of the delay circuit **1004** is used to control or latch the latch **1008**. Thus, the data will only change state on an ideal falling edge of the input timing signal on line **724**. The latch **1008** also has a data input and a data output. The data input is coupled to line **714** to receive the data, and the data output is coupled to line **720** for assertion by the line interface **706**. Those skilled in the art will understand how to construct other return channel encoders such as when more that one bit is send back to the transmitter **102** per clock cycle.

Furthermore, those skilled in the art will realize that the rising edge detector **1002** and the delay circuit **1004** may be replaced by a delay-locked loop or a phase-locked loop as will now be discussed with reference to FIG. **10B**. Referring now to FIG. **10B**, a second embodiment of the return channel encoder **704***b* is shown. The second embodiment of the return channel encoder **704***b* includes a delayed locked loop **650** and a flip-flop **620**. This is identical in operation to FIG. **6B**, and it operation has been described above. The input to the delayed locked loop **650** is coupled to line **724** and the data input of the flip-flop **620** is coupled to line **714**. The data output of the flip-flop **620** provides the data output on line **720**.

It should be understood that the either embodiment of the return channel encoder **704***a,* **704***b* could also include an encoder for providing encoding of the data before transmission over the return channel. The addition of an encoder such as 4 bit/5 bit encoder or a 9 bit/10 bit encoder is advantageous because it increases the amount of data that can be sent per clock cycle. It also provides DC balancing and transition control. However, it makes the transmitter and receiver designs more complicated and adds latency to the availability of the data.

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Referring now to FIGS. **11A**, **11B**, **12A**, and **12B**, timing diagrams for the key signals of the present invention are shown. The timing diagram includes: 1) the CGOut signal on line **210** which is asserted on the clock transmission line **104**; 2) the signal on the clock transmission line **104**; 3) the re-generated clock signal on line **710**; 4) the recovered data signal on line **712**; and 5) the return channel signal asserted by the return channel encoder **704** on the clock transmission line **104**. FIG. **11A** illustrates the signals at the transmitter **102** using a return to zero signaling method. Similarly, FIG. **11B** illustrates signals on the transmission line, and signal in the receiver **106** using a return to zero signaling method. In contrast, FIGS. **12A** and **12B** show the signal relationships for a non-return to zero signaling method. FIG. **12A** shows the signals at the, transmitter **102** and FIG. **12B** shows signals at the receiver **106**.

These timing diagrams demonstrate a number of features of the combined clock and bi-directional data link of the present invention. First, that transition activity and polarity activity by either the transmitter **102** or the receiver **106** is minimized or eliminated close to the rising edge of the CGOut signal. Second, the transmission of data from the transmitter **102** to the receiver **106** is through the position of the falling edge of the clock signal. Third, the transmission of data from the receiver **106** to the transmitter **102** is by current or voltage level adjustment and any changes are not made near the rising edge of the clock signal from the transmitter **102**. Fourth, the effect of assertion of data signals by the receiver **106** does not impact the edges in the signals from the transmitter **102**.

Clock Multiplication

One important advantage of the present invention is that no modification to any portions of the present invention is necessary for the invention to be operable with or without clock multiplication. In some cases, the transmitter **102** and the receiver **106** have the ability to increase the data transmission rate by increasing the clock rate through clock multiplication (sending multiple clock signals within one period of the clock signal). In such a case, the transmitter **102** asks the receiver **106** if it can handle clock multiplication. The receiver **106** indicates to the transmitter **102** what if any levels of clock multiplication can be handled. The transmitter then sends on the highest clock multiplication level possible. In clock multiplication, the transmitter **106** just sends a multiplied clock, however, the receiver **106** has to divide that multiplied clock down to the original pixel clock so that the main data channel can make use of the clock. The phase information on the clock is also important in some data links and it can also be conveyed through the data link provided with the present invention. In the transmitter **102**, a DLL/PLL is used to multiply the clock at the integer multiple of the incoming clock. For some transmission lines, since the jitter information is important, only integer multiple is allowed. However, if this is not that important, rational number multiples can also be used to save the bandwidth.

It is to be understood that the specific mechanisms and techniques that have been described are merely illustrative of one application of the principles of the invention. Numerous additional modifications may be made to the apparatus described above without departing from the true spirit of the invention.

What is claimed is:

1. An apparatus for transmitting a clock signal and data signals over a signal line, the apparatus comprising a clock generator having a first input, a second input and an output, the clock generator modulating a falling edge of an output

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signal to indicate different data values, the first input of the clock generator coupled to receive a clock signal, and the second input of the clock generator coupled to receive a control signal indicating a data value to be transmitted.

2. The apparatus of claim 1, further comprising a data decoder for extracting data signals, the data decoder having an input and an output, the data decoder for extracting data signals, the input of the data decoder coupled to the signal line, the output providing data from the signal line.

3. The apparatus of claim 2, further comprising a line interface for asserting signals on and extracting signals from the signal line, the line interface having an input, an output and a bi-directional port, the bi-directional port coupled to the signal line, the input of the line interface coupled to the output of the clock generator, the output of the line interface coupled to the input of the decoder.

4. The apparatus of claim 3, wherein the line interface further comprises a first amplifier coupling the output of the clock generator to the signal line, a differential amplifier having a first input coupled to the signal line, a second amplifier coupling the clock generator to a second input of the differential amplifier, and the output of the differential amplifier providing the output of the line interface.

5. The apparatus of claim 1, wherein the clock generator further comprises:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a multiplexer having a plurality of inputs and an output for selecting one of the plurality of input signals for output, the plurality of inputs of the multiplexer coupled to respective outputs of the delay-locked loop; and

a latch having a first input and a second input, the first input coupled to an output of the delay-locked loop, and the second input coupled to output of the multiplexer.

6. The apparatus of claim 5, further comprising a monostable multivibrator having an input and an output, the input of the monostable multivibrator adapted to receive the clock signal, the output of the monostable multivibrator coupled to the input of the delay locked loop.

7. The apparatus of claim 5, wherein the latch further comprises a pair of cross-coupled NAND gates.

8. The apparatus of claim 2, wherein the decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a sampling unit having a plurality of inputs, a first output and a second output, the sampling unit for controlling when signals are sampled and for indicating the time at which signals are sampled, the plurality of inputs coupled to respective outputs of the delay-locked loop;

a transition detector for determining when there is a transition in a signal, the transition detector having a data input, a control input and a data output, the data input of the transition detector coupled to the signal line, the control input of the transition detector coupled to the first output of the sampling unit; and

a data generator having a first input, a second input and an output, data generator for producing bit values corresponding to when transitions occur on the signal line, the first input of the data generator coupled to the second output of the sampling unit, the second input of the data generator coupled to the output of the transition detector.

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9. The apparatus of claim 2, wherein the decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to receive the clock signal;

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

10. The apparatus of claim 1, wherein the apparatus is coupled by the signal line to a receiver, and wherein the receiver further comprises:

a clock re-generator having an input and an output for recovering a clock signal from the signal line, the input of the clock re-generator coupled to the signal line;

a second decoder for extracting data signals, the second decoder having a first input, a second input and an output, the second decoder for extracting data signals, the first input of the second decoder coupled to the signal line, the second input of the second decoder coupled to the output of the clock re-generator and the output providing data from the signal line.

11. The apparatus of claim 10, wherein the clock re-generator of the receiver is an amplifier.

12. The apparatus of claim 10, wherein the clock re-generator of the receiver is a phase-locked loop.

13. The apparatus of claim 10, wherein the second decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to output of the clock re-generator;

a sampling unit having a plurality of inputs, a first output and a second output, the sampling unit for controlling when signals are sampled and for indicating the time at which signals are sampled, the plurality of inputs coupled to respective outputs of the delay-locked loop;

a transition detector for determining when there is a transition in a signal, the transition detector having a data input, a control input and a data output, the data input of the transition detector coupled to the signal line, the control input of the transition detector coupled to the first output of the sampling unit; and

a data generator having a first input, a second input and an output, data generator for producing bit values corresponding to when transitions occur on the signal line, the first input of the data generator coupled to the second output of the sampling unit, the second input of the data generator coupled to the output of the transition detector.

14. The apparatus of claim 10, wherein the second decoder further comprises

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to the output of the clock re-generator; and

a flip-flop having a control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

15. The apparatus of claim 10, further comprising a second line interface for asserting signals on and extracting signals from the signal line, the second line interface having an input, an output and a bi-directional port, the

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bi-directional port coupled to the signal line, the output of the line interface coupled to the input of the second decoder and the clock re-generator.

16. The apparatus of claim **10**, further comprising a delay compensator having an input and an output for adjusting a recovered clock signal to compensate. for propagation delay, the input of the delay compensator coupled to the output of the clock re-generator.

17. The apparatus of claim **16**, further comprising a return channel encoder having a first input, a second input and an output, for sending signals on the signal line, the first input of the return channel encoder coupled to receive data for transmission, the second input of the return channel encoder coupled to the output of the delay compensator, and the output of the return channel encoder coupled to the signal line.

18. The apparatus of claim **17**, wherein the return channel encoder further comprises:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to the output of the delay compensator; and

a flip-flop having an control input, a data input and an output, the control input of flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

19. A receiver for coupling to a transmitter through a signal line, wherein the receiver comprises:

a clock re-generator for recovering a clock signal from the signal line, the clock re-generator having an input and an output, the input of the clock re-generator coupled to the signal line; and

a data decoder for extracting data signals from the clock signal, the decoder having a first input, a second input, and an output, the first input of the decoder coupled to the signal line, the second input of the second decoder coupled to the output of the clock re-generator and the output providing data from the signal line, the data decoder comprising:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to the output of the clock re-generator; and

a flip-flop having a control input, a data input, and an output, the control input of the flip-flop coupled to one of the plurality of outputs of the delay-locked loop, the data input of the flip-flop coupled to the signal line, and the output providing data from the signal line.

20. The receiver of claim **19**, further comprising a line interface for asserting signals on and extracting signals from the signal line, the line interface having an input, an output and a bi-directional port, the bi-directional port coupled to the signal line, the output of the line interface coupled to the input of the decoder and the clock re-generator.

21. The receiver of claim **20**, further comprising a delay compensator having an input and an output for adjusting a recovered clock signal to compensate for propagation delay, the input of the delay compensator coupled to the output of the clock re-generator.

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22. The receiver of claim **21**, further comprising a return channel encoder having a first input, a second input and an output, for sending signals on the signal line, the first input of the return channel encoder coupled to receive data for transmission, the second input of the return channel encoder coupled to the output of the delay compensator, and the output of the return channel encoder coupled to the signal line.

23. The receiver of claim **22**, wherein the return channel encoder further comprises:

a rising edge detector having an input and an output, the input coupled to the output of the delay compensator;

a delay circuit having an input and an output, the input coupled to the output of the rising edge detector; and

a latch having a control input, a data input and a data output, the control input coupled to the output of the delay circuit, the data input adapted to receive data, and the data output coupled to the input of the line interface.

24. The receiver of claim **22**, wherein the return channel encoder further comprises:

a delay-locked loop having an input and a plurality of outputs for outputting signals shifted in phase from an input signal, the input of the delay-locked loop coupled to the output of the delay compensator; and

a flip-flop having a control input, a data input and an output, the control input of the flip-flop coupled to one of the plurality of outputs of the delay-locked loop, and the data input of the flip-flop coupled to the signal line.

25. A method for receiving and transmitting signals using a receiver coupled to a signal line, the method comprising:

receiving a signal on an input of a clock re-generator, the clock re-generator having an input and an output, the clock re-generator being adapted for recovering a clock signal from the signal line;

receiving a signal on a data input of a data decoder, the data decoder having a control input, a data input, and a data output, the data decoder adapted for extracting data from the signal on the data input;

passing the clock signal from the output of the clock re-generator to the control input of the data decoder;

passing the clock signal from the output of the clock re-generator to the input of a delay compensator, the delay compensator having an input and an output, the delay compensator adapted for adjusting a clock signal from a clock re-generator to compensate for propagation delay; and

transmitting data from a data output of a return channel encoder over the signal line, the return channel encoder having a control input, a data input, and a data output, the control input coupled to receive the output from the delay compensator and the data input being adapted to receive data.

26. The method of claim **25**, wherein prior to receiving a signal on an input of a clock re-generator, the method further comprises:

receiving a signal on an input of a line interface, the line interface having an input coupled to the signal line and an output.

*   *   *   *   *

EXHIBIT C

US007158593B2

(12) **United States Patent**
Kim et al.

(10) **Patent No.:**   **US 7,158,593 B2**
(45) **Date of Patent:**   **Jan. 2, 2007**

(54) **COMBINING A CLOCK SIGNAL AND A DATA SIGNAL**

(75) Inventors: **Gyudong Kim**, Sunnyvale, CA (US);
Ook Kim, Palo Alto, CA (US);
Min-Kyu Kim, Cupertino, CA (US);
Bruce Kim, Los Altos, CA (US);
Seung Ho Hwang, Palo Alto, CA (US)

(73) Assignee: **Silicon Image, Inc.**, Sunnyvale, CA
(US)

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16, 2001.

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H04L 7/00   (2006.01)
(52) **U.S. Cl.** **375/354**
(58) **Field of Classification Search** 375/238,
375/239, 219–220, 257, 259, 377; 327/35,
327/36, 170, 175, 291, 299; 370/503, 509,
370/510, 512, 535
See application file for complete search history.

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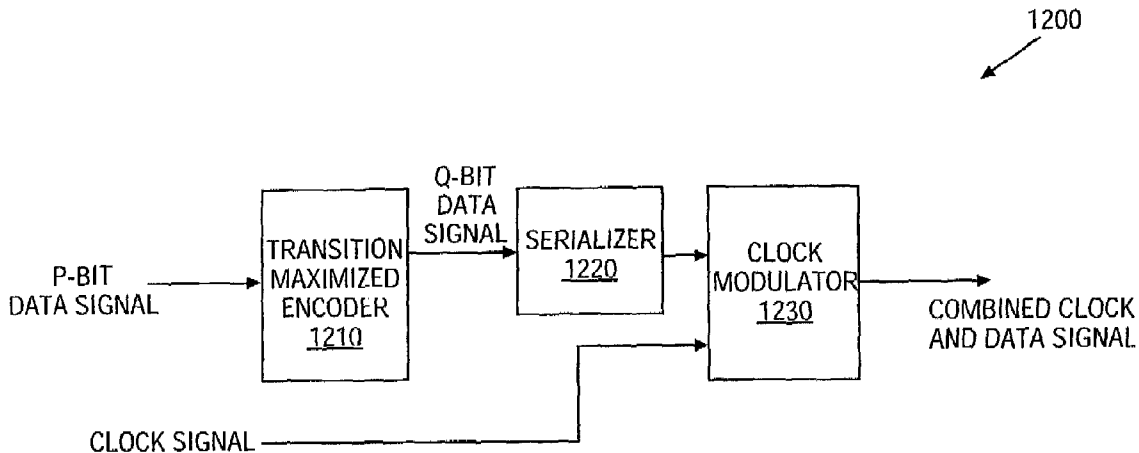| WO	WO 98/14885	4/1998
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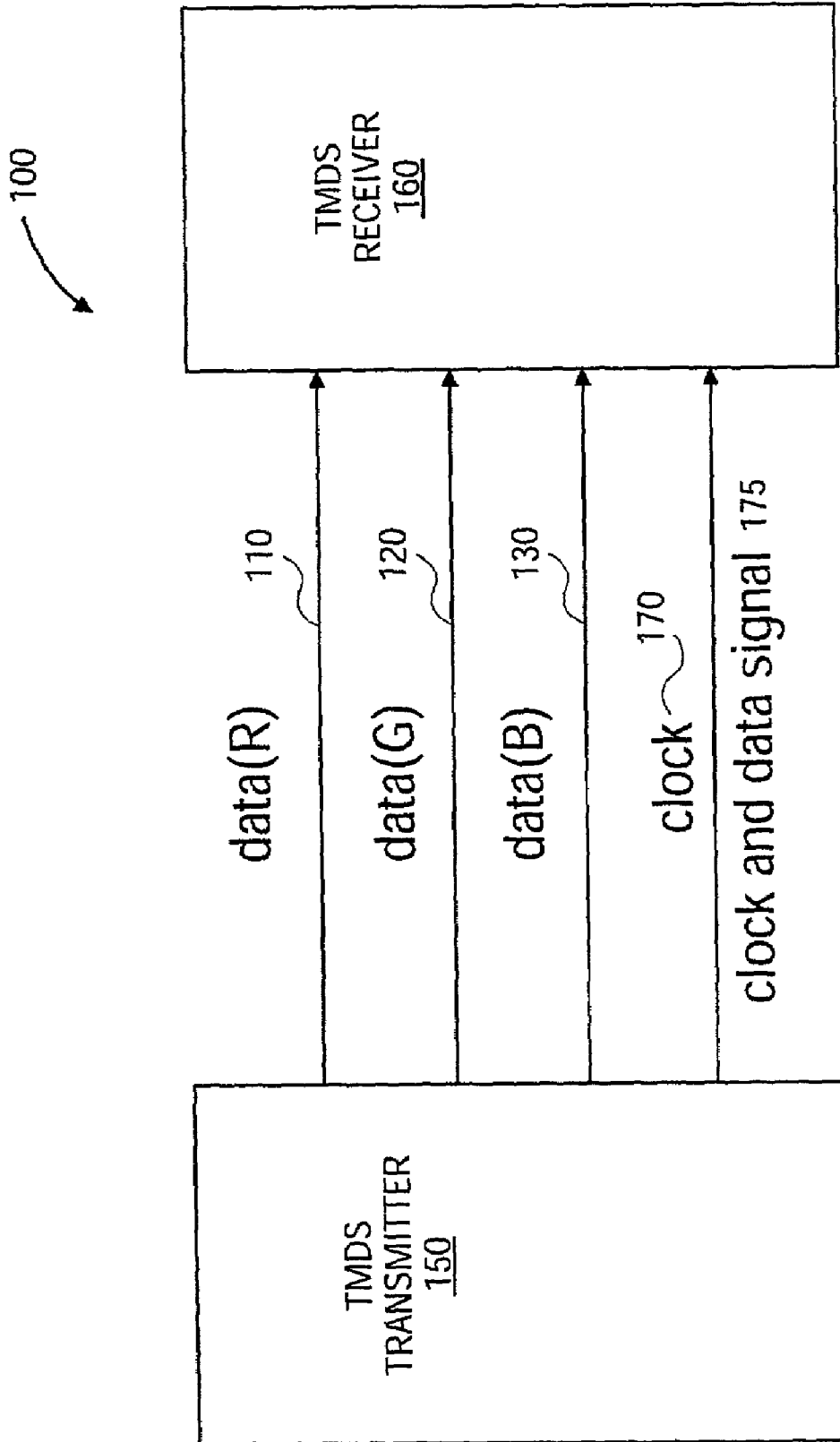
Primary Examiner—Khanh Tran
(74) *Attorney, Agent, or Firm*—Perkins Coie LLP

(57)   **ABSTRACT**

A method of transmitting data in a system including at least one data channel and a separate clock channel is disclosed. The method involves combining a clock signal to be transmitted on the clock channel with a data signal to generate a combined clock and data signal. In one embodiment, the data signal has been generated from data words using an encoding scheme that shifts an energy spectrum of the data signal away from an energy spectrum of the clock signal. In another embodiment, the clock signal has a plurality of pulses each having a front edge and a back edge, and the data signal is modulated onto the clock signal by moving at least one edge (i.e. front or back or both) of the plurality of pulses, thereby to create a combined clock and data signal.

35 Claims, 8 Drawing Sheets

FIG. 1

DATA
SIGNAL 210

CLOCK
SIGNAL 220

FIG. 2

PULSE
315

FALLING
EDGE
310

RISING
EDGE
320

COMBINED
FALLING
EDGE 310

RISING
EDGE
320

CLOCK SIGNAL 301

CLOCK WITH DATA MODULATION 305

FIG. 3

FIG. 4

CLOCK SIGNAL 301

+

DATA SIGNAL 520

FIG. 5

Rx END CLOCK SIGNAL 610

V_{ERROR}

V_{ERROR}

CONTAMINATED SIGNAL

T_{PLL}

Rx END MODULATING PULSE 620

V_{ERROR}

FIG. 6

FREQUENCY [1=DOT CLOCK FREQUENCY]

FIG. 7

PLL JITTER TRANSFER
CURVE (2ND ORDER PLL)

JITTER
GAIN

PASS
BAND

STOP
BAND

FREQ

$$\frac{1}{f^2}$$

FIG. 8

PLL LOOP BW

POWER/Hz

ENERGY AFFECTING PLL JITTER

DOT CLOCK

FREQ

PLL LOOP BW

FIG. 9

POWER/Hz

ENERGY AFFECTING PLL JITTER

DOT CLOCK

FREQ

PLL LOOP BW

FIG. 10

ENCODING A DATA WORD OF A DATA
SIGNAL BY MAPPING THE DATA WORD
FROM A P-BIT DATA WORD INTO A
Q-BIT DATA WORD, WHERE Q IS
GREATER THAN P SO THAT THE NUMBER
OF DATA TRANSITIONS IS INCREASED
TO MOVE THE FREQUENCY OF THE DATA
WORD INTO A HIGHER FREQUENCY
REGION

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COMBINING THE ENCODING DATA WORD
WITH A CLOCK SIGNAL BY MODULATING
ONE OR MORE EDGES OF A CLOCK SIGNAL
PULSE BASED ON THE ENCODED DATA
WORD

1120

TRANSMITTING THE COMBINED CLOCK
AND DATA WORD OVER A SINGLE
TRANSMISSION CHANNEL

1130

FIG. 11

FIG. 12

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COMBINING A CLOCK SIGNAL AND A DATA SIGNAL

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. § 120 from co-pending U.S. application Ser. No. 09/393,235, filed on Sep. 9, 1999 by Gyudong Kim, Minkyu Kim, and Seung Ho Hwang, entitled "A System And Method For Sending And Receiving Data Signals Over A Clock Signal Line," which is fully incorporated into this application by reference; and this application claims priority from and the benefit of U.S. Provisional Patent Application No. 60/276, 672, filed on Mar. 16, 2001, entitled "Encoding Scheme for a Phase Modulated Clock Signal," which is fully incorporated into this application by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to transmitting clock and data signals.

2. Description of the Background Art

The digital visual interface DVI 1.0 Specification, Digital Display Working Group [online], Apr. 2, 1999 [retrieved Mar. 15, 2001], retrieved from the Internet:<URL:http://www.ddwg.org>, which is fully incorporated herein by reference, attempts to address the computer industry's requirements for a digital connectivity specification for high-performance personal computers (PCs) and digital displays.

In synchronous high-speed transmission systems that process digital signals, a clock signal and one or more data signals are transmitted over separate wires. For example, the system transmits data signals over data channels, and transmits a clock signal over a clock channel. These separate channels that transmit only a data signal or only a clock signal permit high performance digital data to be transmitted using a system that has a very simple architecture.

However, because only the clock signal is transmitted over the clock channel, additional signals, such as data signals for example, cannot be transmitted over the clock channel using this system. Therefore, this system does not transmit both a data signal and the clock signal over the clock channel.

SUMMARY OF THE INVENTION

A method and an apparatus to combine a clock signal and a data signal, and to transmit the combined signal over one cable, are disclosed.

According to one aspect of the invention, provided is a method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

combining a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words, to generate a combined clock and data signal, and transmitting the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

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According to another aspect of the invention, the encoding scheme maps the data word from a p-bit data word into a q-bit data word, where q>p.

According to another aspect of the invention, the encoding scheme is direct current (DC) balanced to minimize a DC component of the combined signal.

According to another aspect of the invention, the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the combining step comprises:

modulating the data signal onto the clock signal by moving the front or back edges of the plurality of pulses.

According to a further aspect of the invention, the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the combining step comprises:

modulating the data signal onto the clock signal by moving the front edges of the plurality of pulses.

According to another aspect of the invention, the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a first edge and a second edge, and wherein the combining step comprises:

modulating the data signal onto the clock signal by moving both the front edges and the back edges of the plurality of pulses.

According to a further aspect of the invention, the combining step further comprises:

performing pre-emphasis to the combined signal, so that inter-symbol interference of the combined signal transmitted over a band-limited channel is minimized or reduced.

According to another aspect of the invention, the encoding scheme further comprises:

increasing a number of transitions in each data word. The encoding scheme may also be an encryption scheme.

According to another aspect of the invention, the encoding scheme includes the step of:

encoding an instantaneous data word of said plurality of data words as function of both the instantaneous input word and earlier data words in the data signal.

Further, the encoding scheme may include the step of:

encoding one of the data words of said plurality of data words as a function of one of the following:

future data words; or earlier data words; or future and earlier data words; of said plurality of data words.

According to another aspect of the invention, provided is a method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

providing a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge;

modulating a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal; and

transmitting the combined clock and data signal on the clock channel.
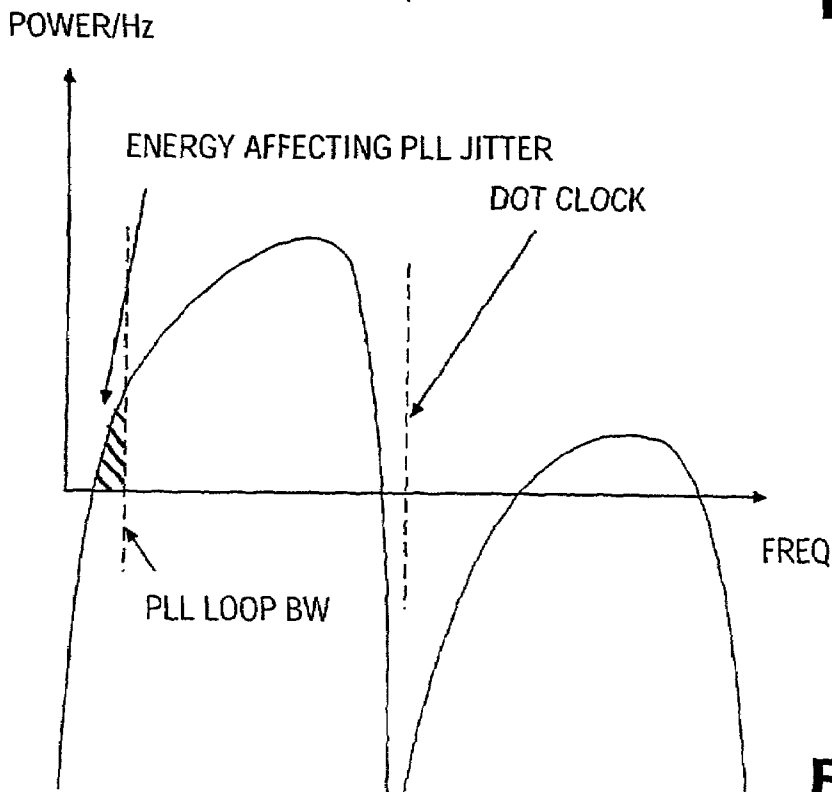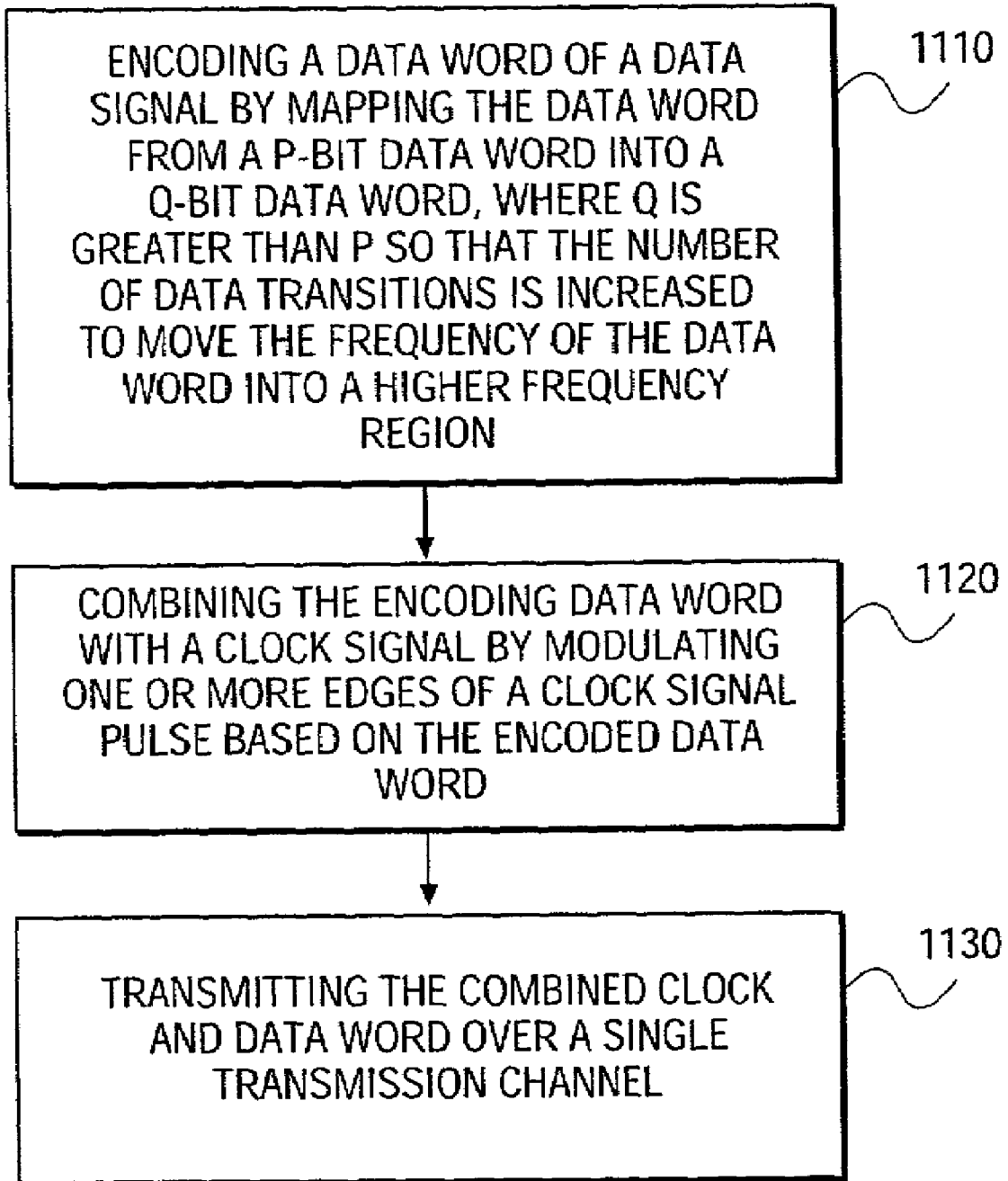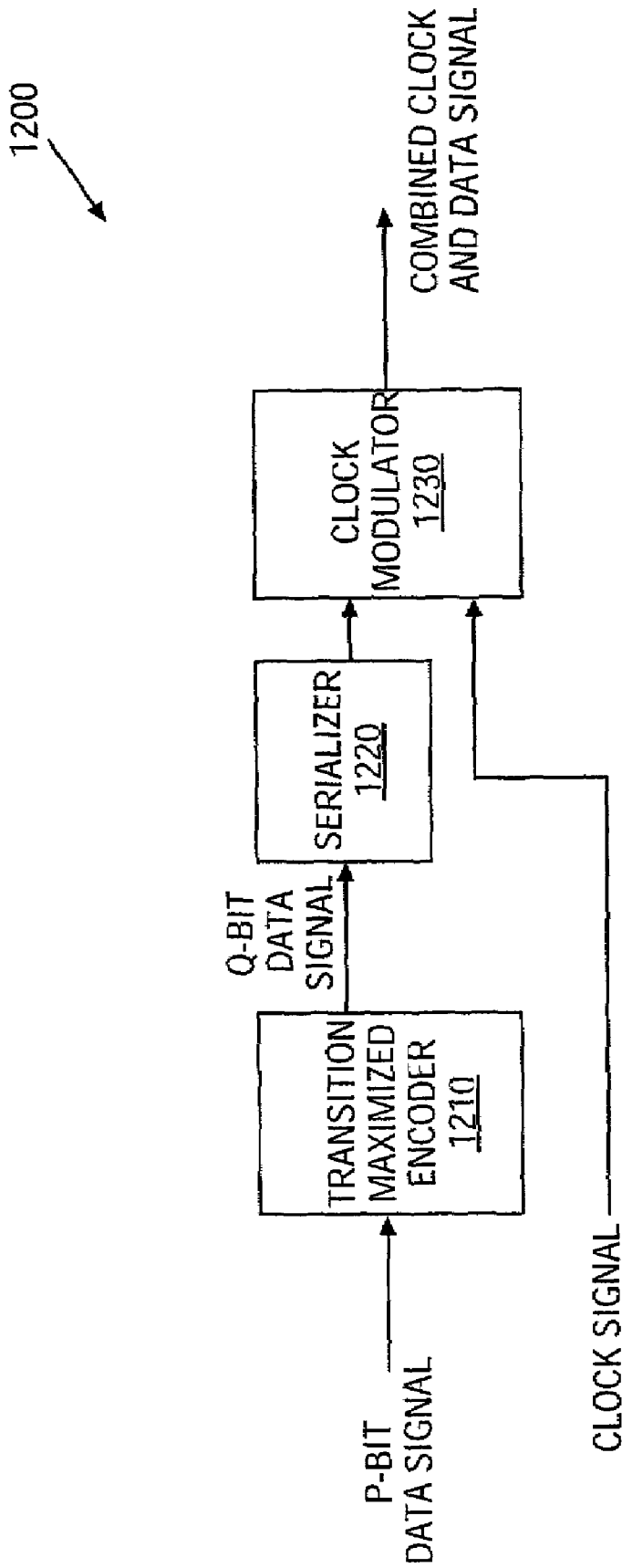
The method may further comprise:

encoding the data words using an encoding scheme that maps the data words from p-bit data words into a q-bit data words, where q>p.

The encoding scheme may be direct current (DC) balanced to minimize a DC component of the combined signal.

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According to another aspect of the invention, the modulating step comprises:

modulating the data signal onto the clock signal by moving both of the front and back edges of the plurality of pulses.

The modulating may step comprise:

modulating the data signal onto the clock signal by moving the front edges of the plurality of pulses.

The modulating step may comprise:

modulating the data signal onto the clock signal by moving the back edges of the plurality of pulses.

The method may further comprise:

performing pre-emphasis to the combined signal, so that inter-symbol interference of the combined signal transmitted over a band-limited channel is minimized or reduced.

The method may further comprise:

encoding the data words using an encoding scheme that increasing a number of transitions in each data word, and the encoding scheme may be an encryption scheme.

Alternatively, the encoding scheme may comprise:

encoding an instantaneous data word of said plurality of data words as function of both the instantaneous input word and earlier data words in the data signal.

Alternatively, the encoding scheme may comprise:

encoding one of the data words of said plurality of data words as a function of one of the following:

future data words; or earlier data words; or future and earlier data words; of said plurality of data words.

According to yet another aspect of the invention, provided is a system for transmitting data, comprising

a transmitter including at least one data channel and a separate clock channel, the clock channel being used by a receiver to decode data transmitted on the at least one data channel, the transmitter being operative to:

combine a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words, to generate a combined clock and data signal, and transmit the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

In the system, the encoding scheme may map the data word from a p-bit data word into a q-bit data word, where q>p.

According to another aspect of the invention, the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the transmitter combines the clock signal with the data signal by:

modulating the data signal onto the clock signal by moving at least one edge of the plurality of pulses.

According to another aspect of the invention, the modulation may be done by moving the front edges of the plurality of pulses.

According to another aspect of the invention, the modulation may be done by moving both the front edges and the back edges of the plurality of pulses.

According to yet another aspect of the invention, provided is a system for transmitting data, comprising

a transmitter including at least one data channel and a separate clock channel, the clock channel being used by a receiver to decode data transmitted on the at least one data channel, the transmitter being operative to:

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provide a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge;

modulate a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal; and

transmit the combined clock and data signal on the clock channel.

The transmitter may further be operative to:

encode the data words using an encoding scheme that maps the data words from p-bit data words into a q-bit data words, where q>p.

The transmitter may further be operative to:

modulate the data signal onto the clock signal by moving both of the front and back edges of the plurality of pulses.

Alternatively, the transmitter may further be operative to:

modulate the data signal onto the clock signal by moving the front edges of the plurality of pulses.

Alternatively, the transmitter may further be operative to:

modulating the data signal onto the clock signal by moving the back edges of the plurality of pulses.

According to a further aspect of the invention, the transmitter uses an encoding scheme for generating the data signal from the data words that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

Other features and embodiments of the present invention will be illustrated by way of example and not by way of limitation in the accompanying abstract, drawings, and detailed description. The abstract, summary of the invention, drawings, and detailed description are, accordingly, to be regarded in an illustrative rather than restrictive sense and the invention measured only in terms of the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

FIG. 1 is a block diagram of a transition-minimized differential signaling (TMDS) system that transmits a clock signal and one or more data signals over the clock channel.

FIG. 2 is a timing diagram for data signals and clock signals that are transmitted over the clock channel.

FIG. 3 illustrates a scheme for mixing a data signal into the clock signal in order to transmit the data and clock signals over the clock channel.

FIG. 4 is a block diagram of a portion of a receiver showing a phase locked loop (PLL) used to recover the clock signal from the combined clock and data signal.

FIG. 5 shows individual clock and data components of a combined clock and data signal.

FIG. 6 illustrates the effects of noise on the recovered clock and data signal at the receiving end.

FIG. 7 shows a non-return-to-zero (NRZ) power spectrum of a data signal that is modulated with the clock signal and transmitted over the clock channel.

FIG. 8 shows PLL jitter transfer characteristics for a 2nd order PLL used to recover the clock signal from the combined clock and data signal

FIG. 9 shows the frequency spectrum of the combined clock and data signal after being transformed by the PLL jitter transfer characteristics.

FIG. 10 shows the frequency spectrum jitter noise components in a combined encoded data and clock signal.

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FIG. **11** shows an example of an encoding method.

FIG. **12** shows a block diagram of an apparatus that generates a combined encoded data and clock signal.

DETAILED DESCRIPTION

A method and system to combine a data signal with a clock signal and to transmit the combined signal are disclosed. The combined clock and data signal are transmitted over a clock channel. This increases the amount of bandwidth that is available in the clock channel. In one embodiment, the data signal is encoded, and the encoded data signal is combined with the clock signal. The encoding of the data signal causes some of the energy components of the encoded data signal to move to higher frequencies, so that a low pass filter can attenuate them. The low pass filter can then recover the clock signal from the combined signal, and output the recovered signal to other devices.

An example of a system that combines the clock signal and the data signal is a transition-minimized differential signaling (TMDS) system, which is described in U.S. application Ser. No. 09/393,235, entitled "A System And Method For Sending And Receiving Data Signals Over A Clock Signal Line," became an U.S. Pat. No. 6,463,092 B1, which is fully incorporated into this application by reference.

FIG. **1** shows a block diagram of the TMDS system that can generate and transmit the combined clock and data signal. The combined signal is generated at the transmitting end **150**, and the data signal and the clock signal are recovered at the receiving end **160**. The combined clock and data signal **175** is transmitted over clock channel **170**. Additional data signals are transmitted over data channels **110**, **120**, and **130**.

FIG. **2** shows an example of a data signal **210** that is typically transmitted separately from a clock signal **220** over one of the data channels **110**, **120**, **130**. The clock signal **220** is used by the TMDS receiver **160** to extract the data from the data signal **210**. In addition to the data signal(s) **210** transmitted over one or more data channels **110**, **120**, **130**, a further data signal may be combined with the clock signal **220** to generate a combined clock and data signal. The transmitting end **150** as shown in FIG. **1** may generate the combined clock and data signal by multiplexing the further digital data signal and the clock signal. The transmitting end then transmits the multiplexed signal over the clock channel.

Multiplexing a data signal with the clock signal may be performed using a modulation method to modulate one signal onto another signal. For example, as shown in FIGS. **3** and **5**, the location of the falling (or trailing) edge **310** of a pulse **315** of the clock signal **301** is modulated, or moved, with respect to the position of the rising edge **320** so that the falling edge **310** of combined clock and data signal **175** is a function of data signal **520**, and the rising edge **320** of combined signal **175** is a function of clock signal **301**. This combined clock and data signal **175** can then be used to transmit the data signal simultaneously with the clock signal. Alternatively, the position of the rising edge **320** is modulated, or moved, with respect to the falling edge **310** so that the position of the rising edge **320** of the combined clock and data signal **175** is a function of the data signal. Alternatively, both the rising and falling edges of the clock signal **301** are modulated, or moved, relative to their normal positions, so that the positions of both the rising and falling edges of the combined clock and data signal **175** is a function of the data signal. Note that the illustrated data signal **520** is the final component that modulates the clock signal **301**. The original data signal, or the data words

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themselves, may typically be more simply represented. That is, the data signal **520** that is shown represents the data signal **520** after any encoding has been done to shift the energy spectrum of the data signal away from the energy spectrum of the clock signal **301**.

The receiving end **160**, as shown in FIG. **1**, may recover the clock signal **301** from the combined signal **175** using a low pass filter, such as phase-locked loop (PLL) that can act as a low pass filter for example. The clock signal component of signal **175** may have a frequency that is well below the bandwidth of the clock transmission channel **170**. Also, the data signal component of the combined signal may have a frequency that is significantly higher than the frequency of the clock signal component, and higher than the low pass filter loop bandwidth. At the receiving end **160**, the combined signal passes through the low pass filter. The high frequency energy of the data signal is attenuated from the combined signal by the low pass filter. Therefore, the low pass filter can remove the data signal from the combined signal, and output a recovered clock signal.

An embodiment of a block diagram of a PLL low pass filter **400** used by the TMDS system **100** to recover the clock signal and send the recovered clock signal to data recovery components is shown in FIG. **4**. Div N block **410** is a divide by N circuit that receives combined clock and data signal **175**, divides signal **175** by N, and outputs a divided by N combined clock and data signal. PFD block **420** is a phase frequency detector that detects the frequency of divided by N combined signal. CP block **430** is a charge pump that increases the voltage level of the signal.

Loop filter (LF) block **440** follows block **430**, and filters the signal in order to recover the data signal **480** and to recover the clock signal **490** from the combined signal **175**. The multi-phase Voltage Controlled Oscillator (VCO) **450** feeds the recovered data signal **480** having a correctly generated frequency to the data extraction circuit **455**. Data extraction circuit **455** is a dual-function circuit in the illustrated embodiment, and serves to extract the data both from recovered data signal **480** and from data signals **485** transmitted separately from the combined clock and data signal **175** over data channels **110**, **120** and **130**, as described above with reference to FIG. **1**. Note that data extraction circuit **455** has been shown schematically as a dual function circuit for purposes of illustrating the invention only, and separate functionality is typically provided in two different modules, one for extracting data from the separate data channels and another for extracting data from the combined clock and data channel. This separate functionality usually results from the fact that the data extracting methods may be very different for the separate data channels as compared to the combined clock and data channel. Also, as will be appreciated by someone of ordinary skill in the art, a clock signal at the frequency of the original clock signal **301** is required to extract the data from the combined clock and data signal **175**. This can be obtained by providing a separate output after the VCO block **450** block including a block that reverses the division conducted by the DIVN block **410**. Alternatively, the data embedded in the combined clock and data signal **175** could be extracted directly by a separate data extraction circuit other than **455**, which has an input of the combined clock and data signal **175**.

VCO **450** also feeds the recovered clock signal to the divide by M (div M) block **470**, where the recovered clock signal is divided by M. Div M block **470** then outputs the recovered clock signal **490** that is at the proper frequency, which is then provided to any device that needs it. For example, the proper frequency of signal **490** may be the

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frequency that is needed by data extraction unit **455** to extract data from the data signals **485** that are received by unit **455**.

Thus, using modulation to combine the clock signal with the data signal allows the system **100** to transmit the combined signal **175** over clock channel **170**. The modulation also allows the system **100** to recover the clock signal from the combined signal by using the low pass filter to attenuate the noise from the data signal component of the combined signal.

An example of the noise generated by combining the clock signal and the data signal is shown in FIG. **3**. Modulating the clock signal **301** to include data signal **520** adds intentional jitter to the falling edge **310** of combined signal **175** in order to allow the transmission of both data and clock information over the same channel, or line. The combined signal **175**, including the jitter in falling edges **310**, is processed at the receiving end **160**. At low frequencies, the jitter may only affect the unused, e.g., falling, edge of the combined signal.

The combined signal gives a minimal penalty in the performance of the system at low frequencies, because the PLL uses the rising edges of the incoming combined signal to compare clock phases. Therefore, a benefit of using modulation to combine signals is maintaining the orthogonal property of both the data signal and the clock signal. Also, because the clock signal is transmitted at a significantly lower frequency than the data signals, as shown in FIG. **2**, the clock signal is not significantly attenuated in the bandwidth-limited clock channel **170**.

However, as the frequency of the combined signal approaches the bandwidth limit of the clock channel, or the length of the clock channel cable increases, the combined signal is attenuated. This attenuation causes errors to the combined signal that is used to recover the clock signal. Therefore, the recovered clock signal that is output from the low pass filter also has errors caused by the attenuation.

Furthermore, at a higher clock frequency, the frequency of the clock signal approaches the frequency of the data signal. As a result, some of the energy components of the data signal are in a frequency region that is below the low pass filter's bandwidth, and are not attenuated by the low pass filter. The data signal's low frequency energy components that are able to pass through the low pass filter cause jitter noise to the combined signal. Therefore, the clock signal recovered by the low pass filter has jitter noise, which causes errors in the recovered clock signal that is output by the PLL. The jitter noise may be caused by inter-symbol interference and signal dispersion, for example.

Inter-symbol interference occurs when the frequency of the signal approaches the frequency of the clock channel bandwidth. At this high frequency, a bit, or symbol, transmitted on the signal is affected by an adjacent bit or symbol. This prevents the symbol from reaching the threshold needed for detection by the receiver.

Signal dispersion also occurs when the frequency of the signal is increased. For example, the digital data bits are represented on the signal as square waves. Each square wave has multiple frequency components. Some frequency components of a square wave travel faster than others, which cause the frequency components to become dispersed at high frequencies. The slower frequency components may affect subsequently transmitted bits, and the faster frequency components may affect previously transmitted bits. For example, the modulated falling edge of the clock signal may affect the rising edge of the clock signal because of this signal dispersion.

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Therefore, the noise from inter-symbol interference and signal dispersion increases the amount of low frequency jitter noise that passes through the low pass filter, such as a PLL for example, along with the clock signal, and results in a noisy recovered clock signal. For example the effects of the noise caused by inter-symbol interference and signal dispersion at higher frequencies is shown with reference to FIGS. **5** and **6**. The combined clock and data signal **175** may be represented as the superposition of clock signal **301** and data signal **520**, as shown in FIG. **5**.

When the combined signal is transmitted over the clock line at a frequency that approaches the limit of the clock channel's bandwidth, noise such as inter-symbol interference and signal dispersion cause the recovered clock and data signals to have errors. For example, FIG. **6** shows the recovered clock signal **610** and the recovered data signal **620** that both have errors produced by the noise that can pass through the low pass filter. Therefore, the recovered clock signal that is output from the PLL has an increased bit error rate (BER).

For example, the rising edge of the recovered clock signal is contaminated by V_{error}. The resulting error impact from the jitter noise can be expressed as:

$$t_{error} = \frac{V_{error}}{\frac{dV_{in}}{dt}}.$$

Because positive and negative pulses have opposite effects on the jitter, they effectively add jitter noise to the signal input to the PFD (Phase Frequency Detector) as shown in FIG. **4**.

The amount of jitter noise in the low frequency region can be graphically shown by power and frequency spectrums. For example, a random data signal produces a power spectrum as illustrated in FIG. **7**. This power spectrum is produced using the following equation:

$$power = k \frac{\sin^2\left(\frac{\pi f}{f_o}\right)}{\left(\frac{\pi f}{f_o}\right)^2},$$

where f_o is the bit rate and f is the frequency.

With respect to the frequency spectrum, if a random data stream is input to a PLL having the transfer curve of FIG. **8**, the noise energy components that are in frequency regions that are below the PLL loop bandwidth are able to pass through the low pass filter of the PLL, as shown in FIG. **9**. Therefore, the PLL reshapes the incoming clock signal based on the unfiltered jitter noise power spectrum, and outputs a recovered clock signal having jitter noise components that are related to the PLL transfer characteristics.

Because the recovered clock signal that is output by the PLL includes the low frequency energy noise of the combined data and clock signal, as shown by the shaded regions of FIG. **9**, this low frequency noise causes the recovered clock signal to have errors, which consequently causes errors in the data signals output by devices that use the clock signal for data recovery.

The amount of jitter noise that passes through the PLL, and is included in the recovered clock signal, can be significantly reduced or eliminated by encoding the data

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signal. The encoding can be used to reduce the amount of low frequency energy introduced onto the recovered clock signal from the jitter noise by moving a major portion of the data signal's data frequency spectrum into a higher frequency region that is above the PLL bandwidth. The PLL low pass filter attenuates the high frequency jitter noise from the combined clock and encoded data signal, and recovers the lower frequency clock signal with a reduced amount of noise.

This movement of some jitter noise energy from lower frequency regions into higher frequency regions by encoding the data signal is apparent by comparing FIGS. **9** and **10**. For example, the spectral energy distribution of a combined clock and unencoded data word is shown in FIG. **9**. When a data signal is encoded, the encoding may include mapping an 8-bit data word onto a 10-bit data word for example. The mapping causes the combined clock and encoded data signal to have the spectral energy distribution as shown in FIG. **10**.

A comparison of the differences between FIGS. **9** and **10** show that encoding a data word into a code space shifts the spectral energy distribution of the data word to higher frequencies, in order to move the energy of some low frequency jitter components of FIG. **9** into the higher frequencies of FIG. **10**. For example, the amount of noise energy from the unencoded data signal that passes unfiltered through the PLL is shown by the energy distribution between the dotted lines of FIG. **9**. This amount of noise energy is greater than the amount of noise energy from the encoded data signal that passes unfiltered through the PLL, which is shown in FIG. **10**.

By shifting the energy spectrum of the combined clock and data signal away from the effective loop bandwidth of the PLL, the dependence on an unchanging front edge of the clock signal is substantially reduced or eliminated, permitting the front edge or both edges of the clock signal to be used for modulation.

The encoding causes the combined clock and encoded data signal to have characteristics that include minimizing or reducing jitter noise, such as inter-symbol interference and signal dispersion for example, in the combined signal that is transmitted over a band-limited channel. Because the PLL can filter the high frequency jitter component from the combined clock and encoded data signal, the encoding allows the PLL to attenuate the high frequency jitter noise energy from the combined signal as shown in FIG. **10**.

As a result of encoding the data signal, therefore, the clock signal that is recovered by the PLL from the combined clock and encoded data signal has a reduced amount of noise energy, as shown by FIGS. **9** and **10**. The recovered clock signal is sent to data recovery devices that use the clock signal to extract data either from a data signal or from the combined clock and encoded data signal. This extracted data has fewer errors because the recovered clock signal used by the data recovery devices has fewer errors, as compared to a clock signal recovered from a combined signal that includes an unencoded data signal.

One benefit of encoding the data is permitting a high frequency clock signal to be combined with encoded data to form a combined signal that is transmitted over a single channel, and permitting the clock signal and the encoded data signal of the transmitted combined signal to be recovered, because some low frequency components of the data signal are pushed to a higher frequency region by the data encoding. The high frequency may be a frequency that approaches the bandwidth of the clock channel, for example.

One method of data encoding uses minimal redundancy to increase the frequency spectrum of the energy introduced to the combined signal from modulating the data signal onto the clock signal, in order to reduce the amount of noise in the recovered clock signal. The minimal redundancy encoding method may include mapping the data signal by increasing the number of bits of data in the data signal before the data signal is mixed with the clock signal. Increasing the number of bits in the data signal allows most of the energy in the data signal to be placed in a frequency region that is high enough to be filtered by the PLL.

The encoding increases, or maximizes, the data transitions, thus moving some or all of the noise energy into a higher frequency spectrum region. For example, an embodiment of encoding data is shown in FIG. **11**. The encoding **1110** includes a data encoder in which an input data word having p-bits is mapped into a data word having q-bits, where q>p. Therefore, the encoding method increases the number of data transitions in order to move some energy from the jitter noise into higher frequency regions.

The method may combine the encoded data word with a clock signal by modulating one or more edges of a clock signal pulse based on the encoded data word, **1120**. For example, modulating the data word onto a clock signal pulse may use a transition maximized encoding scheme to move a rising edge, a falling edge, or both edges of one or more pulses of the clock signal based on the encoded data word. Alternatively, an encoding scheme with less than full transition maximization may be used. In one embodiment, the clock modulation based on the encoded data signal includes pre-emphasis of the combined signal, so that the inter-symbol interference of the combined signal that is transmitted over a band-limited channel is minimized or reduced.

Also, the data may be encoded so that an output data word is a function of both the instantaneous input word and earlier input data words. For example, an output encoded data word may be a function of a finite number of future input data words or a finite number of earlier output data words or both. Furthermore, the encoding method may also include scrambling the encoded data signal in order to encrypt the data while maintaining the data signal's energy shift to higher frequencies. The encrypted data may be decrypted at the receiving end. The encoding method may use a coding that is direct current (DC) balanced to minimize DC component of encoded signal. The type of encoding that is used may vary depending on the frequency used and the amount of jitter reduction effect required by the devices that use the recovered clock signal, such as data recovery devices for example.

The combined clock and encoded data word is then transmitted over a single channel, **1130**. In one embodiment, the data may be transmitted in both directions on the clock line. In another embodiment, the data may be transmitted in the opposite direction from the clock only.

An example of a device **1200** to encode a data signal and to combine the clock signal and the encoded data signal is shown in FIG. **12**. Many different implementations of this device, which may be a transition-maximized (or transition increasing) encoder **1210**, can be used. For example, one embodiment of the encoder **1210** maps an 8-bit input coding space into a 10-bit output coding space. This coding can be extended to map a p-bit into a q-bit by using higher redundancy. For example, instead of using an 8-bit to 10-bit encoding, the encoder may use an 8-bit to 12-bit encoding in order to further remove lower frequency components in the input stream.

If the encoded data signal needs to be serialized, serializer **1220** may be used to serialize the encoded data signal. After the data signal is encoded and serialized, the encoded data

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signal is combined with the clock signal. The combining may be performed by modulator **1230**, which modulates the clock signal based on the encoded data signal to generate a combined clock and encoded data signal.

For example, in one embodiment the modulator may use one or more edges of a first edge, such as a rising or a falling edge for example, of one or more pulses of the clock signal to send precise reference clock information. In this embodiment, the modulator may use one or more edges of a second edge, such as a falling or a rising edge for example, of one or more pulses of the clock signal to send digital data information. Other embodiments of modulation may also be used. For example, both the rising edges and falling edges of the clock signal pulses may be modulated as a function of the encoded data signal, because the impact caused by jitter is greatly reduced by the frequency spectrum characteristics of the combined clock and encoded data signal. The combined signal may be transmitted in one signal cable.

A system and a method to combine a data signal with a clock signal have been discussed. Encoding a data signal before combining the data signal with a high frequency clock signal permits some of the noise components that are moved to higher frequencies by the encoding to be attenuated by the PLL. Because the high frequency noise components are attenuated, the amount of noise in the recovered clock signal is reduced. Therefore, removing some of the noise energy from the combined signal increases the precision in the recovered clock signal that is output by the PLL. This recovered clock signal with a reduced amount of errors allows data recovery devices that use the clock signal to extract data, either from a data signal, or from the combined clock and encoded data signal. This extracted data has fewer errors than data extracted by a data recovery device that uses a noisy clock signal recovered from a combined clock and unencoded data signal.

Thus, combining a clock signal and a data signal increases the bandwidth of the clock channel so that this channel can transmit both clock and data simultaneously. In one embodiment, the data signal may be encoded. Encoding the data signal moves some of the energy components of the data signal to move into higher frequency regions that can be filtered by the PLL, and reduces the amount of noise in the received combined encoded data and clock signal. Therefore, the combined encoded data and clock signal can be transmitted at a frequency that approaches the bandwidth of the clock channel without being significantly affected by noise, such as inter-symbol interference or signal dispersion, for example. Furthermore, the encoding permits the PLL to filter the high frequency energy from the combined signal, and to recover an accurate clock signal that can be used by other devices.

These and other embodiments of the present invention may be realized in accordance with the teachings described herein and it should be evident that various modifications and changes may be made in these teachings without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense and the invention measured only in terms of the claims.

We claim:

1. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

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combining a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words to generate a combined clock and data signal, and

transmitting the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

2. The method of claim **1** wherein the encoding scheme maps the data word from a p-bit data word into a q-bit data word, where q>p.

3. The method of claim **2** wherein said encoding scheme is direct current (DC) balanced to minimize a DC component of the combined signal.

4. The method of claim **2** wherein said encoding scheme further comprises: increasing a number of transitions in each data word.

5. The method of claim **1** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the combining step comprises: modulating the data signal onto the clock signal by moving the front or back edges of the plurality of pulses.

6. The method of claim **1** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the combining step comprises: modulating the data signal onto the clock signal by moving the front edges of the plurality of pulses.

7. The method of claim **1** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a first edge and a second edge, and wherein the combining step comprises: modulating the data signal onto the clock signal by moving both the front edges and the back edges of the plurality of pulses.

8. The method of claim **1** wherein the encoding scheme is an encryption scheme.

9. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

combining a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words to generate a combined clock and data signal,

performing pre-emphasis to the combined signal, so that inter-symbol interference of the combined signal transmitted over a band-limited channel is minimized or reduced, and

transmitting the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

10. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

combining a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words to generate a combined clock and data signal, and

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transmitting the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block,

wherein the encoding scheme includes the step of: encoding an instantaneous data word of said plurality of data words as function of both the instantaneous input word and earlier data words in the data signal.

11. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

combining a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words to generate a combined clock and data signal, and

transmitting the combined clock and data signal on the clock channel;

wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block,

wherein the encoding scheme includes the step of: encoding one of the data words of said plurality of data words as a function of one of the following: future data words; or earlier data words; or future and earlier data words; of said plurality of data words.

12. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

providing a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge;

modulating a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal; and

transmitting the combined clock and data signal on the clock channel.

13. The method of claim 12 further comprising: encoding the data words using an encoding scheme that maps the data words from p-bit data words into a q-bit data words, where q>p.

14. The method of claim 13 wherein the encoding scheme is direct current (DC) balanced to minimize a DC component of the combined signal.

15. The method of claim 12 wherein the modulating step comprises: modulating the data signal onto the clock signal by moving both of the front and back edges of the plurality of pulses.

16. The method of claim 12 wherein the modulating step comprises: modulating the data signal onto the clock signal by moving the front edges of the plurality of pulses.

17. The method of claim 12 wherein the modulating step comprises: modulating the data signal onto the clock signal by moving the back edges of the plurality of pulses.

18. The method of claim 12 further comprising: encoding the data words using an encoding scheme that increasing a number of transitions in each data word.

19. The method of claim 18 wherein the encoding scheme is an encryption scheme.

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20. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

providing a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge,

modulating a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal,

performing pre-emphasis to the combined signal, so that inter-symbol interference of the combined signal transmitted over a band-limited channel is minimized or reduced; and

transmitting the combined clock and data signal on the clock channel.

21. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

providing a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge,

modulating a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal,

encoding an instantaneous data word of said plurality of data words as function of both the instantaneous input word and earlier data words in the data signal; and

transmitting the combined clock and data signal on the clock channel.

22. A method of transmitting data in a system including at least one data channel and a separate clock channel, the clock channel being used to decode data transmitted on the at least one data channel, comprising:

providing a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge,

modulating a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal,

encoding one of the data words of said plurality of data words as a function of one of the following: future data words; or earlier data words; or future and earlier data words; of said plurality of data words; and

transmitting the combined clock and data signal on the clock channel.

23. A system for transmitting data, comprising

a transmitter including at least one data channel and a separate clock channel, the clock channel being used by a receiver to decode data transmitted on the at least one data channel, the transmitter being operative to:

combine a clock signal to be transmitted on the clock channel with a data signal having a plurality of data words, to generate a combined clock and data signal, and

transmit the combined clock and data signal on the clock channel; wherein the data signal has been generated from the data words using an encoding scheme that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

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24. The system of claim **23** wherein the encoding scheme maps the data word from a p-bit data word into a q-bit data word, where q>p.

25. The system of claim **23** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the transmitter combines the clock signal with the data signal by: modulating the data signal onto the clock signal by moving at least one edge of the plurality of pulses.

26. The system of claim **23** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge, and wherein the transmitter combines the clock signal with the data signal by: modulating the data signal onto the clock signal by moving the front edges of the plurality of pulses.

27. The system of claim **23** wherein the clock signal has a plurality of pulses, each pulse of the plurality of pulses having a first edge and a second edge, and wherein the transmitter combines the clock signal with the data signal by: modulating the data signal onto the clock signal by moving both the front edges and the back edges of the plurality of pulses.

28. A system for transmitting data, comprising

a transmitter including at least one data channel and a separate clock channel, the clock channel being used by a receiver to decode data transmitted on the at least one data channel, the transmitter being operative to:

provide a clock signal having a plurality of pulses, each pulse of the plurality of pulses having a front edge and a back edge;

modulate a data signal having a plurality of data words onto the clock signal by moving at least one edge of the plurality of pulses, thereby to create a combined clock and data signal; and

transmit the combined clock and data signal on the clock channel.

29. The system of claim **28** wherein the transmitter is further operative to: encode the data words using an encoding scheme that maps the data words from p-bit data words into a q-bit data words, where q>p.

30. The system of claim **28** wherein the transmitter is further operative to: modulate the data signal onto the clock signal by moving both of the front and back edges of the plurality of pulses.

31. The system of claim **28** wherein the transmitter is further operative to: modulate the data signal onto the clock signal by moving the front edges of the plurality of pulses.

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32. The system of claim **28** wherein the transmitter is further operative to: modulating the data signal onto the clock signal by moving the back edges of the plurality of pulses.

33. The system of claim **28** wherein the transmitter uses an encoding scheme for generating the data signal from the data words that shifts an energy spectrum of the combined clock and data signal away from an effective loop bandwidth of a clock recovery block.

34. A method of transmitting data in a system including at least one data channel and a separate clock channel, the method comprising:

combining a clock signal to be transmitted on the clock channel with an encoded data signal having a plurality of encoded data words to generate a combined clock and encoded data signal;

the clock signal having a plurality of pulses and each pulse having a front edge and a back edge and a pulse width defined by the time difference of the front edge and back edge;

the combining further including encoding an unencoded data to generate an encoded data and modulating the encoded data onto the clock signal based on the encoded data by: (i) moving the front edge only of a particular pulse, (ii) moving the back edge only of a particular pulse, or (iii) moving both the front edge and the back edge of a particular pulse by different amounts or in different directions, wherein the movement in any of the cases causing a change in a change in the width of the particular pulse and the moving of at least one edge is effective to combine the encoded data signal onto the clock signal; and

transmitting the combined clock and encoded data signal on the clock channel;

wherein the encoded data signal is generated from the unencoded data words using an encoding scheme that shifts an energy spectrum of the combined clock and encoded data signal away from an effective loop bandwidth of a clock recovery block.

35. A method as in claim **34**, wherein the modulating of the data signal onto the clock signal is performed after an encoding and a serialization of the data signal.

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