### IN THE UNITED STATES DISTRICT COURT FOR THE WESTERN DISTRICT OF TEXAS WACO DIVISION

### AMERICAN PATENTS LLC,

Plaintiff,

v.

MEDIATEK INC., MEDIATEK USA INC., BROADCOM PTE. LTD., BROADCOM CORPORATION, LENOVO (SHANGHAI) ELECTRONICS TECHNOLOGY CO. LTD., LENOVO GROUP, LTD., NXP SEMICONDUCTORS N.V., NXP B.V., NXP USA, INC., QUALCOMM INCORPORATED and QUALCOMM TECHNOLOGIES, INC., CIVIL ACTION NO. 6:18-CV-339

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

JURY TRIAL DEMANDED

Defendants.

### **ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff American Patents LLC ("American Patents" or "Plaintiff") files this original complaint against Defendants MediaTek Inc., MediaTek USA Inc., Broadcom Pte. Ltd., Broadcom Corporation, Lenovo (Shanghai) Electronics Technology Co. Ltd., Lenovo Group, Ltd., NXP Semiconductors N.V., NXP B.V., NXP USA, Inc., Qualcomm Incorporated, and Qualcomm Technologies, Inc. (collectively "Defendants"), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

### PARTIES

1. American Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas, 75703.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 2 of 109

2. MediaTek Inc. is a company incorporated under the laws of Taiwan, having an address of No. 1, Dusing Road 1, Hsinchu Science Park, Hsinchu City 30078, Taiwan.

3. MediaTek USA Inc. is a company incorporated under the laws of the State of Delaware and having an established place of business at 5914 W. Courtyard Drive, Austin, Texas 78730. MediaTek USA is registered to conduct business in Texas and may be served through its registered agent, CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201-3136.

4. The Defendants identified in paragraphs 2 and 3 above (collectively,"MediaTek") are companies which together comprise one of the world's largest manufacturers of integrated circuits.

5. The MediaTek defendants named above are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and/or using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

6. The MediaTek defendants named above share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

7. Thus, the MediaTek defendants named above operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

8. Broadcom Pte. Ltd. is a corporation organized under the laws of the Republic of Singapore. Broadcom Limited has headquarters at 1 Yishun Avenue 7, Singapore 768923.

9. Broadcom Corporation is a corporation organized under the laws of the state of California. Broadcom Corporation can be served with process by serving its registered agent:

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 3 of 109

Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701.

10. The Defendants identified in paragraphs 8 and 9 above (collectively,"Broadcom") are companies which together comprise one of the world's largest manufacturers of integrated circuits.

11. The Broadcom defendants named above are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and/or using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

12. The Broadcom defendants named above share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

13. Thus, the Broadcom defendants named above operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

Lenovo (Shanghai) Electronics Technology Co. Ltd. is a company organized under the laws of the People's Republic of China. Lenovo (Shanghai) Electronics Technology Co. Ltd. has an office at No. 68 Building, 199 Fenju Rd., China (Shanghai) Pilot Free Trade Zone, Shanghai, China, 200131.

15. Lenovo Group, Ltd. is a company organized under the laws of the People's Republic of China. Lenovo Group, Ltd. has an office at No. 6 Chuang Ye Road, Haidian District, Beijing, China, 100085.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 4 of 109

16. The Defendants identified in paragraphs 14 and 15 above (collectively, "Lenovo") are companies which together comprise one of the world's largest manufacturers of integrated circuits.

17. The Lenovo defendants named above are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and/or using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

18. The Lenovo defendants named above share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

19. Thus, the Lenovo defendants named above operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

20. NXP Semiconductors N.V. is a corporation organized and existing under the laws of the Netherlands, having a place of business at High Tech Campus 60, 5656 AG Eindhoven, the Netherlands.

21. NXP B.V. is a corporation organized and existing under the laws of the Netherlands, having a place of business at High Tech Campus 60, 5656 AG Eindhoven, the Netherlands.

22. NXP USA, Inc. is a corporation organized and existing under the laws of the state of Delaware, having its principal place of business at 6501 William Cannon Drive West, Austin, TX 78735. It can be served via its registered agent: Corporation Service Company d/b/a CSC – Lawyers Inc., 211 E. 7th Street Suite 620, Austin, TX 78701.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 5 of 109

23. The Defendants identified in paragraphs 20-22 above (collectively, "NXP") are companies which together comprise one of the world's largest manufacturers of integrated circuits.

24. The NXP defendants named above are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and/or using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

25. The NXP defendants named above share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

26. Thus, the NXP defendants named above operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

27. Qualcomm Incorporated is a Delaware corporation. Qualcomm Incorporated may be served through its registered agent, Prentice Hall Corp. System, 211 E. 7th Street Suite 620, Austin, Texas 78701.

28. Qualcomm Technologies, Inc. is a Delaware corporation. Qualcomm Technologies, Inc. may be served through its registered agent, Corporation Service Company d/b/a CSC-Lawyers Inc., 211 E. 7th Street Suite 620, Austin, Texas 78701.

29. The Defendants identified in paragraphs 27 and 28 above (collectively,"Qualcomm") are companies which together comprise one of the world's largest manufacturers of integrated circuits.

30. The Qualcomm defendants named above are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and/or using of the

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 6 of 109

accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

31. The Qualcomm defendants named above share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

32. Thus, the Qualcomm defendants named above operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

33. The parties to this action are properly joined under 35 U.S.C. § 299 because the right to relief asserted against Defendants jointly and severally arises out of the same series of transactions or occurrences relating to the making and using of the same products or processes, including products using the processors and related processes based on common ARM architectures. Additionally, questions of fact common to all defendants will arise in this action.

### JURISDICTION AND VENUE

34. This is an action for infringement of United States patents arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

35. This Court has personal jurisdiction over Defendants pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) Defendants have done and continue to do business in Texas and (ii) Defendants have committed and continue to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing a least a portion of any other infringements alleged

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 7 of 109

herein. In addition, or in the alternative, this Court has personal jurisdiction over Defendants pursuant to Fed. R. Civ. P. 4(k)(2).

36. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because (i) MediaTek has done and continues to do business in this district; (ii) MediaTek has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by internet sales and sales via retail and wholesale stores, and/or inducing others to commit acts of patent infringement in this district; (iii) MediaTek Inc. is a foreign entity; and (iv) MediaTek USA Inc. has a regular and established place of business in this district at 5914 W. Courtyard Drive, Austin, Texas 78730, as stated on MediaTek's website:

 $\mathsf{Home} \rightarrow \mathsf{About} \rightarrow \mathsf{Office} \mathsf{Locations} \rightarrow \mathsf{United} \mathsf{States} \mathsf{Offices}$ 

# United States Office Locations

MediaTek USA Inc. (Austin) 5914 W Courtyard Drive Austin, TX 78730 United States Tel: <u>+1-512-687-1900</u> Fax: +1-512-687-1921 View Map

https://www.mediatek.com/about/office-locations/mediatek-usa-offices

37. Venue is proper as to MediaTek Inc., which is organized under the laws of

Taiwan. 28 U.S.C. § 1391(c)(3) provides that "a defendant not resident in the United States may

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 8 of 109

be sued in any judicial district, and the joinder of such a defendant shall be disregarded in determining where the action may be brought with respect to other defendants."

38. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because (i) Broadcom has done and continues to do business in this district; (ii) Broadcom has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by internet sales and sales via retail and wholesale stores, and/or inducing others to commit acts of patent infringement in this district; (iii) Broadcom Pte. Ltd. is a foreign entity; and (iv) Broadcom Corporation has regular and established places of business in this district at 2901 Via Fortuna Drive, Suite 400, Floor 4, Terrace 6, Austin, Texas 78746 and 3801 S. Capital of Texas Highway, Barton Creek Plaza II, Suite 150 and 240, Floor 1 and 2, Austin, Texas 78704 as stated on Broadcom's website:

A https://www.broadcom.com/company/contact/#locations

#### Austin, Texas (Via Fortuna Drive)

2901 Via Fortuna Drive, Suite 400, Floor 4, Terrace 6 Austin, Texas 78746 United States

GET DIRECTIONS O

#### Austin, Texas (S. Capital of Texas Highway)

3801 S. Capital of Texas Highway, Barton Creek Plaza II, Suite 150 and 240, Floor 1 and 2 Austin, Texas 78704 United States

#### GET DIRECTIONS O

### https://www.broadcom.com/company/contact/#locations

39. Venue is proper as to Broadcom Pte. Ltd., which is organized under the laws of the Republic of Singapore. 28 U.S.C. § 1391(c)(3) provides that "a defendant not resident in the United States may be sued in any judicial district, and the joinder of such a defendant shall be disregarded in determining where the action may be brought with respect to other defendants."

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 9 of 109

40. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because (i) Lenovo has done and continues to do business in this district; (ii) Lenovo has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by internet sales and sales via retail and wholesale stores, and/or inducing others to commit acts of patent infringement in this district; and (iii) Lenovo (Shanghai) Electronics Technology Co., Ltd. and Lenovo Group, Ltd. are foreign entities.

41. Venue is proper as to Lenovo (Shanghai) Electronics Technology Co., Ltd. and Lenovo Group, Ltd., which are organized under the laws of the People's Republic of China. 28 U.S.C. § 1391(c)(3) provides that "a defendant not resident in the United States may be sued in any judicial district, and the joinder of such a defendant shall be disregarded in determining where the action may be brought with respect to other defendants."

42. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because (i) NXP has done and continues to do business in this district; (ii) NXP has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by internet sales and sales via retail and wholesale stores, and/or inducing others to commit acts of patent infringement in this district; (iii) NXP Semiconductors N.V. and NXP B.V. are foreign entities; and (iv) NXP USA, Inc. has a regular and established place of business in this district at 6501 William Cannon Dr. West, Austin, TX 78735, as stated on NXP's website:

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 10 of 109

<ul> <li>ATMC-Austin (Ed Bluestein)</li> </ul>	Irvine	▼ OHT-Austin Oak Hill	Washington, D.C.
3501 Ed Bluestein Blvd Austin, TX 78721	Kokomo	Corporate Headquarters 6501 Wm Cannon Dr West Austin,	▶ Woburn, MA
	▹ Novi	TX. 78735	
Chandler		San Diego	
Hoffman Estates		San Jose, CA	

https://www.nxp.com/about/about-nxp/about-nxp/worldwide-locations/nxp-in-the-unitedstates:USA

43. Venue is proper as to NXP Semiconductors N.V. and NXP B.V., which are organized under the laws of the Netherlands. 28 U.S.C. § 1391(c)(3) provides that "a defendant not resident in the United States may be sued in any judicial district, and the joinder of such a defendant shall be disregarded in determining where the action may be brought with respect to other defendants."

44. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b) because (i) Qualcomm has done and continues to do business in this district; (ii) Qualcomm has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by internet sales and sales via retail and wholesale stores, and/or inducing others to commit acts of patent infringement in this district; and (iii) Qualcomm has a regular and established place of business in this district at 9600 N. Mopac, Ste 900, Stonebridge Plaza II, Austin, Texas 78759, as stated on Qualcomm's website:

### 2 Offices in TX, USA

Office Austin - AUS.B 9600 N. Mopac, Ste 900 Stonebridge Plaza II Austin TX 78759 USA

Get directions >

♀<sub>Office</sub> Richardson - RIC.B

2100 Lakeside Blvd. Suite 475 Richardson TX 75082 USA **Get directions** >

### https://www.qualcomm.com/company/facilities/offices?country=USA&region=TX

### **BACKGROUND**

45. The patents-in-suit generally pertain to on-chip service capabilities used in integrated circuits. The technology disclosed by the patents was developed in the 1990s by employees of On-Chip Technologies, Inc. including: Dr. Bulent Dervisoglu, who received his Ph.D. in Computer Science from the University of Edinburgh; Laurence H. Cooke, who received a bachelor's degree in Applied Mathematics from Stanford University; and Vacit Arat, who received a master's degree in Electrical Engineering from the University of Houston.

46. Prior to the patented technology, testing and debugging integrated circuits was largely directed to the chip level of integrated circuits. These approaches led to higher costs (including sometimes doubled circuitry for testing) and longer time-to-market for integrated circuit products.

47. Then, pioneers such as Dr. Dervisoglu and his colleagues solved these problems when they invented their patented on-chip service and testing that uses embedded testing circuitry within an integrated circuit to provide for custom testing with minimal cost addition and

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 12 of 109

improved time-to-market. Their ideas were recognized by *Evaluation Engineering* after Dr. Dervisoglu's presentation at the 1999 International Test Conference, and their solution is widely used throughout the industry.

48. After issuance, the validity of one of the patents-in-suit, the '371 Patent, was tested in an inter partes review. In a Final Written Decision, the PTAB ultimately confirmed the validity of claims 2 and 7-10 of the '371 Patent, imposing estoppel on Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc., and their privies, from further challenging the validity of those claims.

#### <u>COUNT I</u>

### **DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,964,001**

49. On November 8, 2005, United States Patent No. 6,964,001 ("the '001 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "On-Chip Service Processor."

50. American Patents is the owner of the '001 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '001 Patent against infringers, and to collect damages for all relevant times.

51. MediaTek made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its MT6595, Helio X10, and Helio X27 families of products that include advanced on-chip service capabilities ("accused products")<sup>1</sup>:

<sup>&</sup>lt;sup>1</sup> A non-exhaustive list of additional accused products includes the MT6739, MT6750, MT6752, MT6753, Helio P, Helio A22, MT7622, MT7623, MT8x series (including MT8173, MT8176,

# MT6595

## The world's first octa-core 4G LTE smartphone chip with the new ARM Cortex-A17 processor

MediaTek MT6795 is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6595 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6595



CPU Cluster 1: ARM-A17 @ 2.5GHz

CPU Cluster 2: ARM-A7 @ 1.7GHz

Source: https://www.mediatek.com/products/smartphones/mt6595

## MediaTek Helio X10

64-bit true octa-core SoC with LTE and world's first 2K display support

MediaTek Helio X10 (MT6795) is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full. HD Super-Slow Motion videos. MT6795 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

MT8783, MT8785, and MT8163), and Helio X series (including Helio X20, Helio X23, and Helio X25) families of products that include advanced on-chip service capabilities.

Processor

CPU Cluster 1: ARM-A53 @ 2.0GHz

CPU Cluster 2: ARM-A53 @ 2.0GHz

Cores:

Octa (8)

CPU Bit:

64-bit

Heterogeneous Multi-Processing: Yes

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

# MediaTek Helio X27

Premium clocked tri-cluster, deca-core 64-bit WorldMode LTE platform

MediaTek Helio X27 (MT6797X) provides three processor clusters, each designed to more efficiently handle different types of workloads. The premium MediaTek Helio X27 features a maximized clock frequency across all three clusters, with an unequaled maximum of 2.6GHz on the powerful ARM Cortex-A72 cluster.

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

## Processor

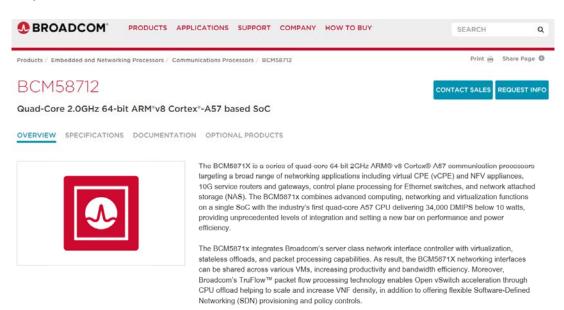
CPU Cluster 1: ARM-A72 @ 2.6GHz

CPU Cluster 2: ARM-A53 @ 2.0GHz

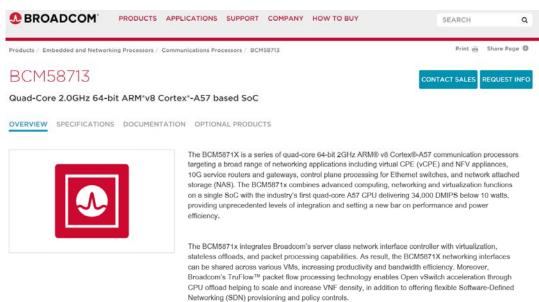
Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

52. Broadcom made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its BCM58712 and BCM58713 families of products that include advanced on-chip service capabilities ("accused products"):



## Source: <u>https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58712/</u>



Source: https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58713/

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 16 of 109

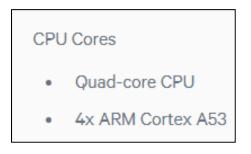
53. Lenovo made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its Lenovo Tab 4 8, Lenovo Tab 4 10, and Lenovo Tab 3 10 families of products that include advanced on-chip service capabilities ("accused products"):

Home > Tablets > Android Tablets > Tab 4 Series > Tab 4 8 Tab 4 8	
A tablet for the whole family Whether it's for homework, online shopping, or a screen- time treat, the Tab 4 8 is ideal for the whole family. Stylish yet rugged, this smooth-performing tablet has a vibrant 8* display, enhanced audio, and long battery life. Everyone can have their own account and there are optional add-ons aimed specifically for the younger ones. Starting at: \$116.99	10:08
VIEW MODELS	

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08

Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> MSM8917 Processor (1.4 GHz)
Operating System	Android <sup>™</sup> Nougat 7.1

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08



Source: https://www.qualcomm.com/products/snapdragon/processors/425

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 17 of 109

Home * Tablets * Android Tablets * Tab 4 Series * Tab 4 10 $Tab 4 \ 10$	
From entertaining the kids to creating key presentations, the Tab 4 10 is ideal for the whole family. This stylish yet robust device offers seamless performance, a 10.1° display, immersive audio, and great battery life. What's more, everyone can have their own account and, with optional add-ons, the Tab 4 10 can be a designated kid's tablet or a more productive 2-in-1. Starting at: \$169.99	
VIEW MODELS ****	

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-X304/p/ZZITZTATB0X</u>

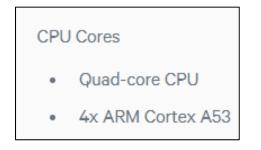
Processo	or	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> APQ8017 Processor	(1.40GHz)
----------	----	---	-----------

٦

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-

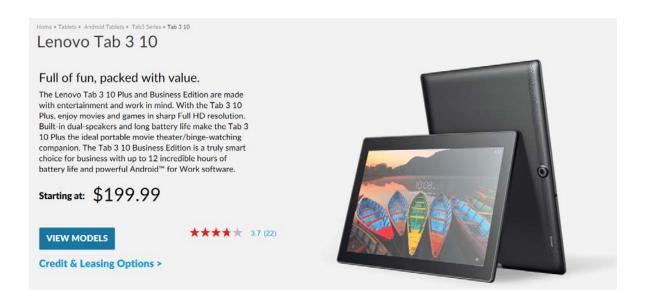
X304/p/ZZITZTATB0X

Г



Source: https://www.qualcomm.com/products/snapdragon/processors/425

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 18 of 109



Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

### Business/p/ZZITZTATB2F

)	)					)	)	)	)	)	3			E	E	E	E	E	E	E	E	E		E															E				E	E	E	E	E	E	E	E	E	E	E	E	1	1	1	1	1	1	1
3	3)	3)	3)	3)	3)	3)	3	3	3	3			E	E	E	E	E	E	E	E	E	E	E	E		E				E								E	E				E	E	E	E	E	E	E	E	E	E	E	E							and the second se
3	3)	3)	3)	3)	3)	3)	3	3	3	3				E	E	E	E	E	E	E	E	E		E															E				E	E	E	E	E	E	E	E	E	E	E	E							
3	3)	3)	3)	3)	3)	3)	3	3	3	3				F	F			F				F		F															F				F	F		F	F	F	F	F	F	F	F	F							
3	3)	3)	3)	3)	3)	3)	3	3	3	3																																																			
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E																F			ł	ł			ł	ł	ł			ł			{																		
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E																F			ł	ł			ł	ł	ł			ł			{																		
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	F																F																																	
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	F	- Name	- Andrew -								- Andrew -	- Name	- Andrew -	E	- Name	E	F	E	- Name			E	E				- Name	- Andrew -		E	E	- Andrew -				- Andrew -						and the second s								1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E	and a second sec	And and a second s	and the second se			and the second se				And and a second s	and a second sec	And and a second s	E	and a second sec	E	F	E	and a second sec	F	F	E	E	F	F	F	and a second sec	And and a second s	F	E	E		and the second se		and the second se	And and a second s		and the second se	and the second se	and the second se	and the second se	and the second se	and the second se	1	1	1	1	1	1	1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	F		- Name	and the second se			and the second se				- Name		- Name	E		E	F	E		F	F	E	E	F	F	F		- Name	F	E	E		and the second se		and the second se	- Name		and the second se	and the second se	and the second se	and the second se		and the second se	1	1	1	1	1	1	1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E		and a second sec								and a second sec		and a second sec	E		E	F	E		F	F	E	E	F	F	F		and a second sec	F	E	E	F				and a second sec								1	1	1	1	1	1	1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E		Name of Street o	and the second se			and the second se				Name of Street o		Name of Street o	E		E	F	E		F	F	E	E	F	F	F		Name of Street o	F	E	E		and the second se		and the second se	Name of Street o		and the second se	and the second se	and the second se	and the second se		and the second se	1	1	1	1	1	1	1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E	E										E		E	E	E	F	E	E	F	F	E	E	F	F	F	E		F	E	E	F												1	1	1	1	1	1	1
B	B)	B)	B)	B)	B)	B)	B	B	B	B	E	E	E										E		E	E	E	F	E	E	F	F	E	E	F	F	F	E		F	E	E	F												1	1	1	1	1	1	1
B	B)	IB)	IB)	IB)	B)	B)	B	B	B	B	IE	IE													E		E	IE	E		IF	IF	E	E	IF	IF	IF			IF	E	E	F												1	1	1	1	1	1	
IB	IB)	IB)	IB)	IB)	IB)	IB)	IB	IB	IB	IB	IE	IE	16										16		IE	16	IE	IE	IE	16	IF	IF	IE	IE	IF	IF	IF	16		IF	IE	IE	IF					1					1		1	1	1	1	1	1	
IB	1B)	1B)	1B)	1B)	1B)	1B)	IB	1B)	IB	IB	16	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	IE	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	/	1					
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	/						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	11	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	11	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	11	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	11	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	11	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	1	16	1	16	1	16	16	16	1	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							/
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	1	1	11	11	1	11	11	1	11	11	11	11	1	11							
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							/
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	11	1	1	11	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	16	11	1	11	11	1	11	11	11	11	1	11	1						
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	16	11	1	1	1	1	1	1	1	11	16	11	16	16	16	16	16	16	16	16	16	16	16	16	16	16	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							/
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	11	11	1	1	1	1	1	1	1	11	11	11	16	11	16	16	16	11	16	16	16	16	16	16	16	11	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							/
1B	1B)	1B)	1B)	1B)	1B)	1B)	1B	1B)	1B	1B	1E	16	1	11	1	1	1	1	1	1	1	11	1	11	16	1	16	16	16	1	16	16	16	16	16	16	16	1	11	16	16	16	11	1	1	1	11	1	1	1	1	1	1	1							/
1B	4B)	4B)	4B)	4B)	4B)	4B)	1B	1B)	1B	1B	1E	16	11	11	1	1	1	1	1	1	1	11	11	11	16	11	16	16	16	11	11	11	16	16	11	11	11	11	11	11	16	16	11	1	1	1	11	1	1	1	1	1	1	1		1	/	/	/	/	/
ИB	4B)	⁄IВ)	⁄IВ)	⁄IВ)	4B)	4B)	ИB	1B	ИB	ИB	ЛE	16	11	11	1	1	1	1	1	1	1	11	11	11	1	11	1	16	1	11	11	11	1	1	11	11	11	11	11	11	1	1	11	1	1	1	11	1	1	1	1	1	1	1							1
ИВ	ИB)	ИB)	ИB)	ИB)	4В)	ИB)	ИB	ИB	ИB	ИB	ИE	16	1	1	1	1	1	1	1	1	1	1	1	1	16	1	16	16	16	1	11	11	16	16	11	11	11	1	1	11	16	16	11	1	1	1	1	1	1	1	1	1	1	1		0					1
ИВ	AB)	ИB)	∕IB)	ИB)	ИB)	AB)	ИB	ИB	ИB	ИВ	ИE	1E	1	1	1	1	1	1	1	1	1	1	1	1	NE	1	NE	1E	NE	1	٩ŀ	٩ŀ	NE	NE	٩ŀ	٩ŀ	٩ŀ	1	1	٩ŀ	NE	NE	1	1	1	1	1	1	1	1	1	1	1	1		0					
ИВ	ØB)	∕IB)	∕IB)	∕IB)	∕IB)	ØB)	ИB	ИB	ИB	ИВ	ИE	ЛE	1	1	1	1	1	1	1	1	1	1	1	1	٩E	1	٩E	٩F	٩E	1	٩ŀ	٩ŀ	٩E	٩E	٩ŀ	٩ŀ	٩ŀ	1	1	٩ŀ	٩E	٩E	ЛI	1	1	1	1	1	1	1	1	1	1	1	U	V					
ИВ	MB)	MB)	MB)	MB)	ИB)	MB)	ИB	ИB	ИB	ИВ	ME	ME	1	1	1	1	1	1	1	1	1	1	1	1	ME	1	ME	ME	ME	1	M	M	ME	ME	M	M	M	1	1	M	ME	ME	M	1	1	1	1	4	1	1	1	1	4	1	0	V	V	V	V	V	V
ИВ	MB)	∕IB)	∕IB)	∕IB)	∕IB)	MB)	ИB	ИB	ИB	ИВ	ME	ME	1	1	1	N	N	1	N	N	N	1	1	1	ME	1	ME	МE	ME	1	٩ŀ	٩ŀ	ME	ME	٩ŀ	٩ŀ	٩ŀ	1	1	٩ŀ	ME	ME	M	1	N	1	1	N	1	1	1	1	4	1	V	V	V	V	V	V	V
ИΒ	MB)	MB)	MB)	MB)	MB)	MB)	MВ	MB	MВ	ИВ	ME	ME	1	1	M	M	M	M	M	M	M	1	1	1	ME	1	ME	ME	ME	1	M	M	ME	ME	M	M	M	1	1	M	ME	ME	M	M	M	M	1	M	M	M	M	M	4	M	V	V	V	V	V	V	V
ИΒ	MB)	MB)	MB)	MB)	MB)	MB)	MВ	MB	MВ	ИВ	ME	ME	1	1	M	M	M	M	M	M	M	1	1	1	ME	1	ME	ME	ME	1	M	M	ME	ME	M	M	M	1	1	M	ME	ME	M	M	M	M	1	M	M	M	M	M	4	M	V	V	V	V	V	V	V
ИΒ	MB)	MB)	MB)	MB)	MB)	MB)	MВ	MB	MВ	ИВ	ME	ME	1	1	M	M	M	M	M	M	M	1	1	1	ME	1	ME	ME	ME	1	M	M	ME	ME	M	M	M	1	1	M	ME	ME	M	M	M	M	1	M	M	M	M	M	4	M	V	V	V	V	V	V	V
ИВ	MB)	MB)	MB)	MB)	ИB)	MB)	ИB	ИB	ИB	ИВ	ME	ME	1	1	1	1	1	1	1	1	1	1	1	1	ME	1	ME	ME	ME	1	M	M	ME	ME	M	M	M	1	1	M	ME	ME	M	1	1	1	1	4	1	1	1	1	4	1	0	V	V	V	V	V	V
ИΒ	MB)	MB)	MB)	MB)	MB)	MB)	MВ	MB	MВ	ИВ	ME	ME	4	M	M	M	M	M	M	M	M	M	4	M	ME	4	ME	ME	ME	4	M	M	ME	ME	M	M	M	4	M	M	ME	ME	M	M	M	M	M	M	M	M	M	M	M	M	V	V	V	V	V	V	V
МВ	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	МВ	ME	ME	M	M	M	M	M	M	M	M	M	M	M	M	ME	M	ME	ME	ME	M	MF	MF	ME	ME	MF	MF	MF	M	M	MF	ME	ME	M	M	M	M	M	M	M	M	M	M	M	M	V	V	V	V	V	V	V
MB	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	MB	ME	ME	M	MI	M	M	M	M	M	M	M	MI	M	MI	M	M	M	ME	M	M	M	M	M	M	M	M	M	M	MI	M	M	M	M	M	M	M	MI	M	M	M	M	M	M	M	V	V	V	V	V	V	V
MB	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	MB	ME	ME	MI	MI	MI	M	M	MI	M	M	M	MI	MI	MI	M	MI	M	ME	M	MI	M	M	M	M	M	M	M	MI	MI	M	M	M	M	MI	M	MI	MI	M	MI	MI	MI	MI	M	MI	N	N	N	N	N	N	V
MB	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	MB	ME	ME	M	M	MI	M	M	MI	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	N
MB	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	MB	ME	ME	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	N	N	N
MB	MB)	MB)	MB)	MB)	MB)	MB)	MB	MB	MB	MB	ME	ME	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	M	M	M	M	M
MB	.MB)	MB)	MB)	MB)	.MB)	.MB)	MB	MB	MB	MB	ME	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	N	N	N	N	N	N	M
IMB	lmb)	lmb)	lmb)	lmb)	lmb)	lmb)	IMB	IMB	IMB	IMB	IME	IME	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IME	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	LM	IM	IM	IM	IM	IM	IM
IMB	lmb)	lmb)	lmb)	lmb)	lmb)	lmb)	IMB	IMB	IMB	IMB	IME	IME	IMI	IM	IM	IM	IM	IM	IM	IM	IM	IM	IMI	IM	IM	IMI	IM	IME	IM	IMI	IM	IM	IM	IM	IM	IM	IM	IMI	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IM	IN	IM	IM	IM	IM	IM	IM
1MB	1MB)	1MB)	1MB)	1MB)	1MB)	1MB)	1MB	1MB	1MB	1MB	1ME	1ME	11	1MI	1M	1M	1M	1M	1M	1M	1M	1MI	11	1MI	11	11	11	111	11	11	1MF	1MF	11	11	1MF	1MF	1MF	11	1MI	1MF	11	11	1M	1M	1M	1M	1MI	1M	1M	1M	1M	1M	1M	1M	11	11	11	11	11	11	11
1MB	1MB)	1MB)	1MB)	1MB)	1MB)	1MB)	1MB	1MB	1MB	1MB	1ME	1ME	1MI	1MI	1MI	1M	1M	1MI	1M	1M	1M	1MI	1MI	1MI	1M	1MI	1M	1MF	1M	1MI	1MF	1MF	1M	1M	1MF	1MF	1MF	1MI	1MI	1MF	1M	1M	1MI	1MI	1M	1MI	1MI	1M	1MI	1MI	1MI	1MI	1M	1MI	1	1	1M	1M	1M	1M	1M

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

### Business/p/ZZITZTATB2F

The MediaTek MT8161 is an ARM based entry-level to mid-range SoC for (Android based) tablets. It offers four ARM Cortex-A53 processor cores (quad-core) that are clocked with up to 1.3 GHz. Furthermore, an ARM Mali-720 graphics card, a LPDDR3 memory controller (e.g., accessing 1 GB in the Lenovo Tab 2 A8-50), Bluetooth 4.0 and dual-band 802.11 b/g/n are integrated in the SoC.

Source: https://www.notebookcheck.net/Mediatek-MT8161-Tablet-SoC.145089.0.html

54. NXP made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its i.MX516, S32V234,

and i.MX 8QuadMax families of products that include advanced on-chip service capabilities

("accused products")<sup>2</sup>:

TS SOLUTI						ALL - Search		
essors and Microcon	ntrollers ~ Arm#-Based Processo	ors and MCUs 👻 i.MX App	lications Processors 👻 i MX Matur	re Processors ~ i.MX516				
			rocessors - Mu y, ARM® Corte	-	Performar	ICE, Folo	∞ ⊠ <	
	OVERVIEW	DOCUMENTATION	SOFTWARE & TOOLS	BUY/PARAMETRICS	PACKAGE/QUALIT	Y TRAINING & SU	JPPORT	
1	/ /		1			1	1	
							ased-processo	ors
<u>mcus/i.</u>	<u>mx-applicati</u>	<u>ions-proce</u>	essors/i.mx-m	nature-proce	<u>ssors/app]</u>	ications-pr	ocessors-	
imadia	high perfor	mance lou	v-power-cont	nactivity or	n cortex c	8 corei M	<b>Y516</b>	
meula	-mgn-perion	mance-iov	v-power-com	licenty-all	II-COILEX-2	10-COTC.1.1VI	<u>AJ10</u>	
							1 A	ccou
0							1 A	ccou
P							1 A	ccou
CTS SOLU	ITIONS SUPPORT	ABOUT				1	L A	ccou
			S32 Automotive Platform ~ S	532V234 Vision and Sensor	Fusion Processor Fam			ccou
			S32 Automotive Platform ~ §	532V234 Vision and Sensor	Fusion Processor Fam			ccou
	controllers ~ Arm*-Based Pr	rocessors and MCUs $\sim$				ily	ALL - Search	
	controllers ~ Arm*-Based Pr S32V234:	occessors and MCUs ~	ocessor for Fr	ont and Suri	ound Viev	ily	ALL - Search	
	controllers ~ Arm*-Based Pr S32V234:	occessors and MCUs ~		ont and Suri	ound Viev	ily	ALL - Search	
	controllers ~ Arm*-Based Pr S32V234:	occessors and MCUs ~	ocessor for Fr nd Sensor Fus	ont and Suri sion Applicat	round Viev ions	<sup>⊪y</sup> v Camera,	ALL - Search Fotow 🛛	<
	S32V234: Machine I	•cessors and MCUs ~ • Vision Pro Learning an	ocessor for Fr nd Sensor Fus	ont and Suri sion Applicat	round Viev ions	ily	ALL - Search	
	S32V234: Machine I	•cessors and MCUs ~ • Vision Pro Learning an	ocessor for Fr nd Sensor Fus	ont and Suri sion Applicat	round Viev ions	<sup>⊪y</sup> v Camera,	ALL - Search Fotow 🛛	<
	S32V234: Machine I	•cessors and MCUs ~ • Vision Pro Learning an	OCCESSOR FOR FR Ind Sensor Fus SOFTWARE & 1	ont and Suri sion Applicat	round View ions	IV V Camera,	ALL - Search Fotow 🛛	<
	Controllers ~ Arm*-Based Pr S32V234: Machine I overview	•cessors and MCUs ~ • Vision Pro Learning an	ocessor for Fr nd Sensor Fus	ont and Suri sion Applicat	round View ions	<sup>⊪y</sup> v Camera,	ALL - Search Fotow 🛛	<
	S32V234: Machine I	•cessors and MCUs ~ • Vision Pro Learning an	OCCESSOR FOR Fr and Sensor Fus SOFTWARE & T Overview	ont and Suri sion Applicat	round View ions	IV V Camera,	ALL - Search Follow 🛛	<
	Controllers ~ Arm*-Based Pr S32V234: Machine I overview	•cessors and MCUs ~ • Vision Pro Learning an	OCCESSOR FOR FR nd Sensor Fus SOFTWARE & 1 OVERVIEW The S32V234 is our 2r family designed to sup	ront and Surr sion Applicat TOOLS BUY/PAS nd generation vision pro	round View tions	IIV V Camera, PACKAGE/QUALITY Itures uad Arm® Cortex®-A55	ALL - Search Fotow I	<
	Arm*-Based Pr S32V234: Machine I overview Jump To Overview & Features Development Boards Target Applications	CONSIGNT AND MCUS Vision Pro Learning an DOCUMENTATI	OCCESSOR FOR Fr nd Sensor Fus SOFTWARE & 1 OVERVIEW The S32V234 is our 2r family designed to sup applications for image	ront and Surr sion Applicat TOOLS BUY/PAF	round View ions AMETRICS Fea cessor ive = C n ISP, P	IIV V Camera, PACKAGE/QUALITY Itures uad Arm® Cortex®-A55 lus M4 core up to 133	ALL - Search Fotow S TRAINING & SUPPORT 3 cores running up to 1GH. MHz	<
	Arm*-Based Pr S32V234: Machine I overview Jump To Overview & Features Development Boards	CONSIGNT AND MCUS Vision Pro Learning an DOCUMENTATI	OVERVIEW The S32V234 is our 2r family designed to sup applications for image powerful 3D GPU, dua security and supports 3	ront and Surr sion Applicat BUY/PAF buy/Paf buy/Paf bu	round View tions AMETRICS Fea cessor ive = C n ISP, = D is suited c	IIV V Camera, PACKAGE/QUALITY Itures uad Arm® Cortex®-A55 lus M4 core up to 133	ALL - Search Fotow S TRAINING & SUPPORT 3 cores running up to 1GH MHz selerator cores enabled by	<
	Arm*-Based Pr S32V234: Machine I overview Jump To Overview & Features Development Boards Target Applications	CONSIGNT AND MCUS Vision Pro Learning an DOCUMENTATI	OVERVIEW The S32V234 is our 2r family designed to sup applications for image powerful 3D GPU, dua security and supports 8 for ADAS, NCAP front recognition, surround v	ront and Surr sion Applicat TOOLS BUY/PAF buy/Paf buy/	round View tions	IIV V Camera, PACKAGE/QUALITY Itures uad Arm® Cortex®-A5: lus M4 core up to 133 ual APEX-2 vision acc penCL <sup>™</sup> , APEX-CV ar	ALL  Search  Follow  TRAINING & SUPPORT  TRAINING & SUPPORT  Gamma Support  ALL  ALL  ALL  ALL  ALL  ALL  ALL  AL	<
	Arm*-Based Pr S32V234: Machine I overview Jump To Overview & Features Development Boards Target Applications	CONSIGNT AND MCUS Vision Pro Learning an DOCUMENTATI	OVERVIEW The S32V234 is our 2r family designed to sup applications for image powerful 3D GPU, dua security and supports 3 for ADAS, NCAP front recognition, surround v fusion applications. S3 automotive-grade relia	ront and Surr sion Applicat TOOLS BUY/PAF buy	round View tions AMETRICS Fea cessor ive = C n ISP, = D is suited n and and sensor r in ISP, = D is suited r is suited r in ISP, = D is suited r is suite su	IV V Camera, PACKAGE/QUALITY Itures uad Arm <sup>®</sup> Cortex <sup>®</sup> -A5' lus M4 core up to 133 ual APEX-2 vision acc penCL <sup>™</sup> , APEX-CV ar upports ISO 26262 fur IC 61508 and DO 178	ALL  Search  Follow  TRAINING & SUPPORT  TRAINING & SUPPORT  Gamma Support  ALL  ALL  ALL  ALL  ALL  ALL  ALL  AL	z,

Source: https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processorsand-mcus/s32-automotive-platform/vision-processor-for-front-and-surround-view-cameramachine-learning-and-sensor-fusion-applications:S32V234

<sup>&</sup>lt;sup>2</sup> A non-exhaustive list of additional accused products includes the i.MX 7 series, i.MX 8 series, i.MX Mature series, QorIQ Layerscape series, i.MX534, i.MX535, i.MX537, i.MX8M, and i.MX 8QuadPlus families of products that include advanced on-chip service capabilities.

Feature	i.MX 8QuadMax	i.MX 8QuadPlus
ARM <sup>®</sup> Core	2 x ARM Cortex®-A72	1 x Cortex-A72
ARM Core	4 x Cortex-A53	4 x Cortex-A53
ARM Core	2 x Cortex-M4F	2 x Cortex-M4F

Source: fact sheet downloaded from https://www.nxp.com/docs/en/fact-sheet/IMX8FAMFS.pdf

55. Qualcomm made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its Snapdragon 410E and

Snapdragon 650 families of products that include advanced on-chip service capabilities

("accused products")<sup>3</sup>:

Designed to meet the demanding requirements of embedded computing applications with its high performance, energy efficiency, multimedia features, integrated connectivity and long-term support, the Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 410E embedded platform is an ideal platform for the Internet of Things.

### Source: https://www.qualcomm.com/products/apq8016e

CPU

CPU Clock Speed: Up to 1.2 GHz CPU Cores: Quad-core CPU, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit, 32-bit

Source: <a href="https://www.qualcomm.com/products/apq8016e">https://www.qualcomm.com/products/apq8016e</a>

<sup>&</sup>lt;sup>3</sup> A non-exhaustive list of additional accused products includes the Snapdragon 400 tier (including Snapdragon 439 (SDM439), Snapdragon 450, Snapdragon 427 (MSM8920), and Snapdragon 435 (MSM8940)), MSM8956, the Snapdragon 600 tier (including Snapdragon 652 (MSM8976), and Snapdragon 653 (MSM8976 Pro)) families of products that include advanced on-chip service capabilities.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 21 of 109



The Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 650 mobile platform supports high-quality, efficient performance, multimedia, gaming and connectivity, thanks to its powerful 64-bit capable hexa-core CPUs, integrated Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> X8 LTE with Cat 7 speeds, Qualcomm<sup>®</sup> Adreno<sup>®</sup> 510 GPU, and support for 4K Ultra HD video.

Source: https://www.qualcomm.com/products/snapdragon/processors/650

CPU

CPU Clock Speed: Up to 1.8 GHz CPU Cores: Hexa-core CPU, 2x ARM Cortex A72, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit

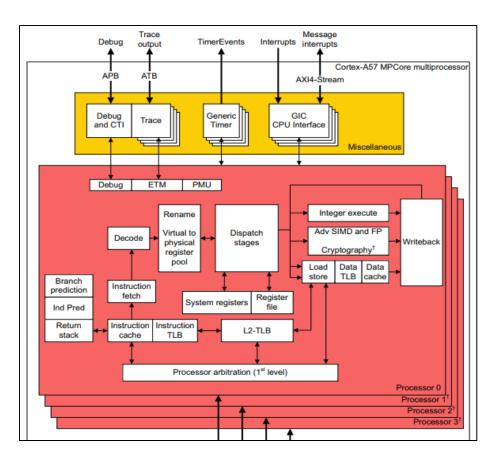
Source: https://www.qualcomm.com/products/snapdragon/processors/650

- 56. By doing so, Defendants have directly infringed (literally and/or under the doctrine of equivalents) at least Claim 5 of the '001 Patent. Defendants' infringement in this regard is ongoing.
  - 57. Defendants have infringed the '001 Patent by making, having made, using,

importing, providing, supplying, distributing, selling or offering for sale integrated circuits

having advanced on-chip service capabilities.

58. The accused products include a multiplicity of logic blocks.

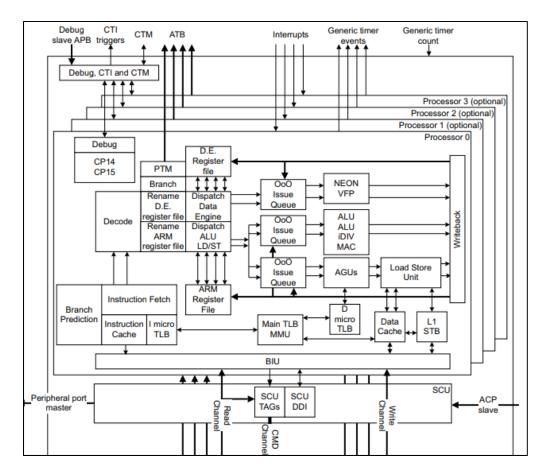


Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

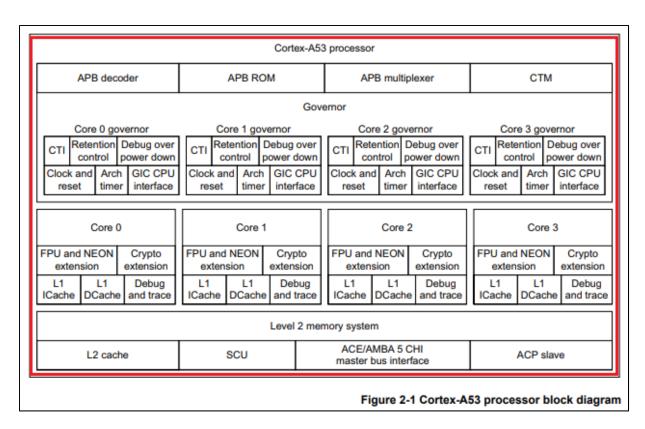
0\_trm.pdf

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 23 of 109



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

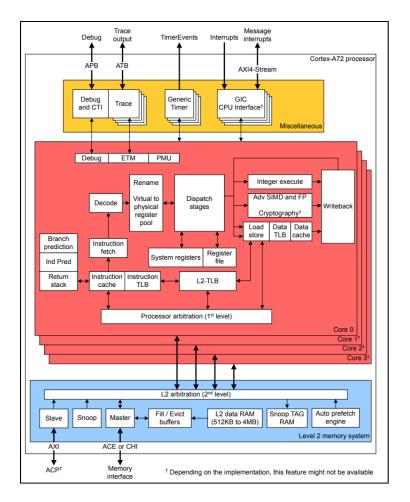
https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf



Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

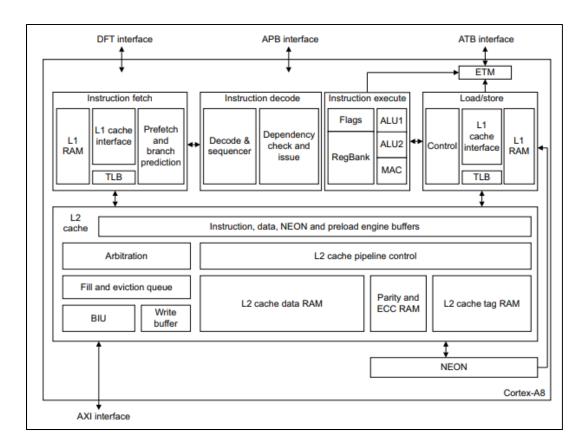
<u>df</u>



Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

<u>100095\_0001\_02\_en.pdf</u>



### Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K cortex a8 r3p2 trm.pdf

59. The accused products include an on-chip logic analyzer with a multiplicity of

input ports.

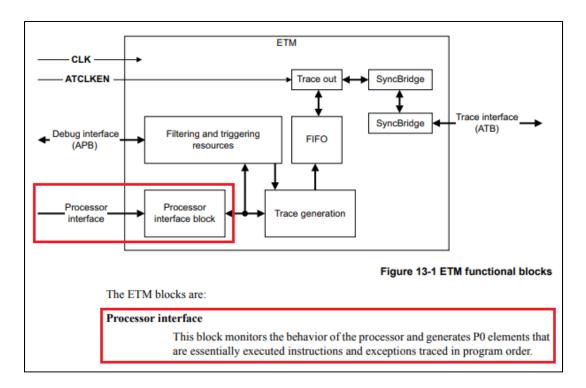
### Embedded Trace Macrocell architecture

The multiprocessor implements the ETMv4 architecture. See the ARM<sup>®</sup> Embedded Trace Macrocell Architecture Specification, ETMv4.

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C\_cortex\_a57\_mpcore\_r1p

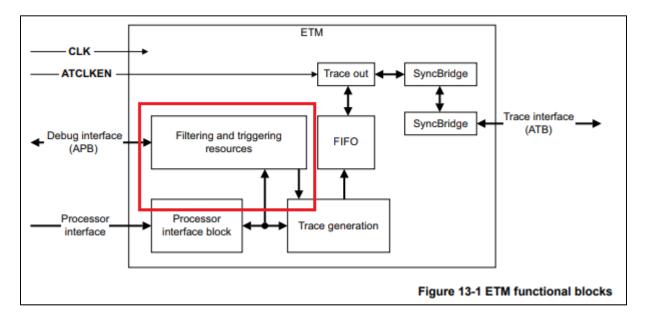
0\_trm.pdf



Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

### 0\_trm.pdf



Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

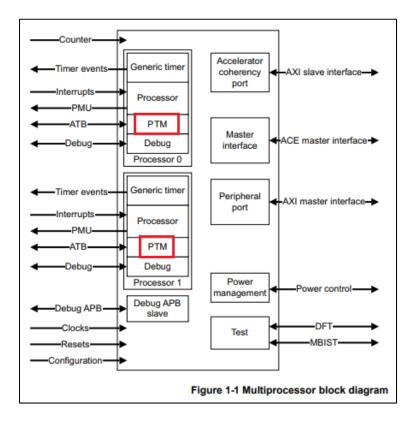
### 0 trm.pdf

Filtering and triggering resources	
	s configuring it to trace only in certain address lyzer style filtering options are also available.
The ETM can also generate a trigge stop capturing trace.	er that is a signal to the trace capture device to

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

0\_trm.pdf



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf

The PTM is a real-time instruction flow trace module that complies with the *Program Flow Trace* (PFTv1.1) architecture. The PTM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5.

For more information see:

- ARM<sup>®</sup> CoreSight<sup>™</sup> Architecture Specification (ARM IHI 0029).
- ARM<sup>®</sup> CoreSight<sup>™</sup> SoC Technical Reference Manual (ARM DDI 0480).

Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf

### Embedded Trace Macrocell architecture

The Cortex-A53 processor implements the ETMv4 architecture. See the ARM<sup>®</sup> ETM<sup>™</sup> Architecture Specification, ETMv4.

Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

### <u>df</u>

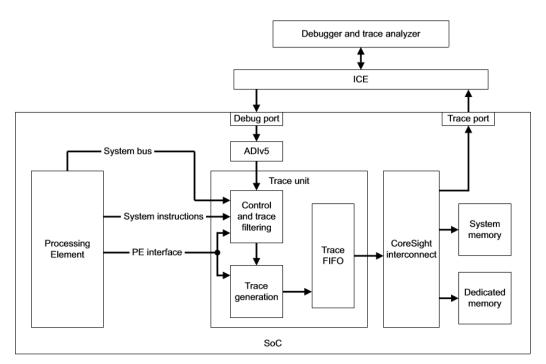


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

### Embedded Trace Macrocell architecture

The processor implements the ETMv4 architecture. See the *ARM*<sup>®</sup> *Embedded Trace Macrocell Architecture Specification*, *ETMv4*.

Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095 0001 02 en/cortex a72 mpcore trm

100095 0001 02 en.pdf

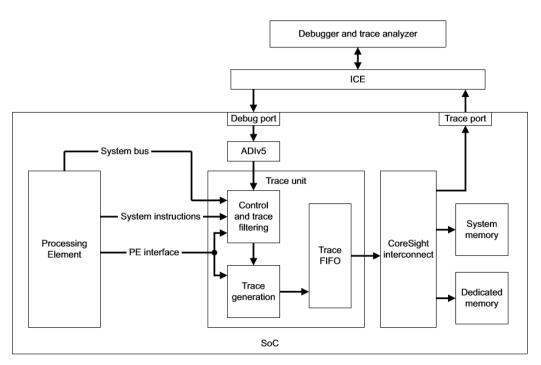


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

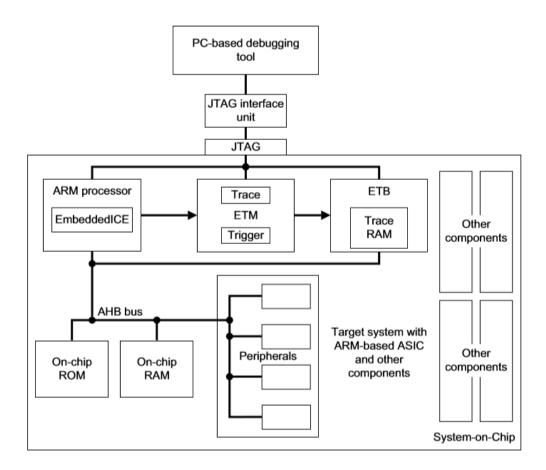
https://static.docs.arm.com/ihi0064/d/IHI0064D etm v4 architecture spec.pdf

### About the ETM

The ETM is a CoreSight<sup>™</sup> component designed for use with the CoreSight Design Kit. CoreSight is the ARM extensible, system-wide debug and trace architecture. The Cortex-A8 processor implements the ETM architecture v3.3.

Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K cortex a8 r3p2 trm.pdf



Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

You control traci	ng in two ways:
Triggering	Triggering controls when the collection of the trace data occurs. Setting a trigger enables you to focus trace collection around your region of interest.
Filtering	Filtering controls the type of trace information that is collected. It is important to optimize usage of the trace port bandwidth, especially when a narrow trace port is used. Filtering the trace serves two purposes:
	<ul> <li>It prevents overflow of the internal FIFO by minimizing the number of data transfers traced. This is especially important when the FIFO is small or the trace port is narrow.</li> </ul>
	<ul> <li>It limits the amount of trace stored by the trace capture device (TCD), for example a TPA or an on-chip trace buffer. This enables more useful information to be stored around the trigger.</li> </ul>
	You can filter the instruction trace or the data trace as follows:
	<ul> <li>Filter the instruction trace by enabling and disabling trace generation. This is the TraceEnable function.</li> </ul>
	<ul> <li>Filter the data trace by indicating the specific data accesses that must be traced. This is the ViewData function.</li> </ul>

### Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

 In this specification:
 An ETM is said to be tracing when TraceEnable is active and no condition exists that prohibits tracing. Conditions that prohibit tracing include:

 The processor is in Debug state.
 The processor is in a Wait For Interrupt (WFI) or Wait For Event (WFE) condition. See Wait For Interrupt and Wait For Event on page 4-251.

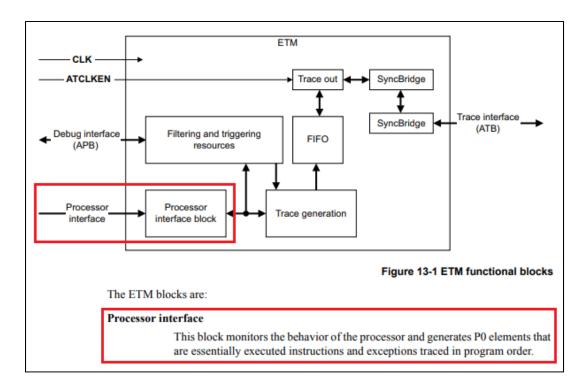
Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

- 60. The accused products include a multiplicity of probe lines.
- 61. The accused products include each of said probe lines being adapted to capture

signals from said logic blocks and to propagate said signals to one of said multiplicity of input

ports of said on-chip logic analyzer.



Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C\_cortex\_a57\_mpcore\_r1p

### 0\_trm.pdf

### Filtering and triggering resources

You can filter the ETM trace such as configuring it to trace only in certain address ranges. More complicated logic analyzer style filtering options are also available.

The ETM can also generate a trigger that is a signal to the trace capture device to stop capturing trace.

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

### 0\_trm.pdf

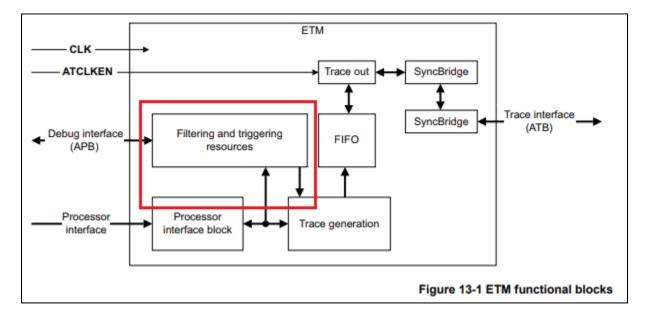
The ETM is a module that performs real-time instruction flow tracing based on the ARM<sup>®</sup> Embedded Trace Macrocell Architecture Specification, ETMv4. The ETM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, RealView. See the CoreSight documentation in Additional reading on page xi for more information.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 34 of 109

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

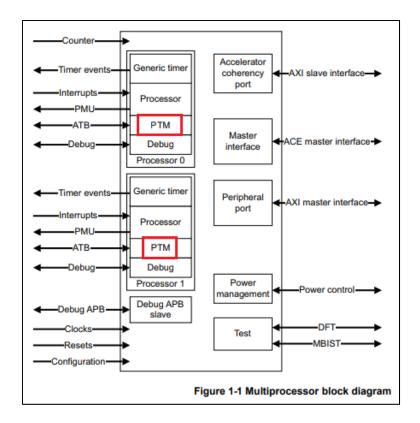
### 0 trm.pdf



Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

0\_trm.pdf



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

The PTM is a real-time instruction flow trace module that complies with the *Program Flow Trace* (PFTv1.1) architecture. The PTM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5.

For more information see:

- ARM<sup>®</sup> CoreSight<sup>™</sup> Architecture Specification (ARM IHI 0029).
- ARM<sup>®</sup> CoreSight<sup>™</sup> SoC Technical Reference Manual (ARM DDI 0480).

Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

### 13.3 ETM trace unit functional description

This section describes the ETM trace unit. It contains the following sections:

- Processor interface.
- Trace generation.
- Filtering and triggering resources.
- FIFO.
- Trace out on page 13-6.
- Syncbridge on page 13-6.

Figure 13-1 shows the main functional blocks of the ETM trace unit.

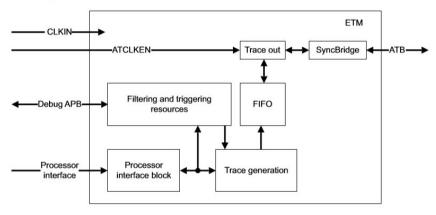


Figure 13-1 ETM functional blocks

Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

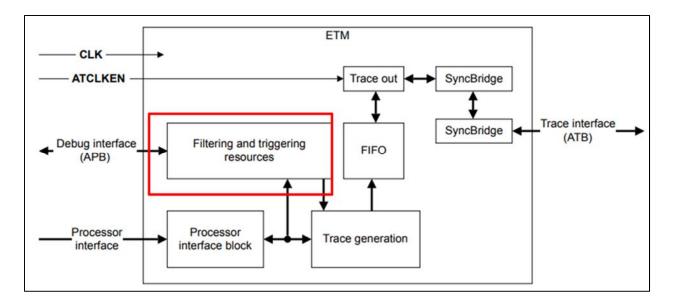
### <u>df</u>

The ETM is a module that performs real-time instruction flow tracing based on the *ARM*<sup>®</sup> *Embedded Trace Macrocell Architecture Specification, ETMv4*. The ETM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, RealView. See the CoreSight SoC-400 documentation for more information.

Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

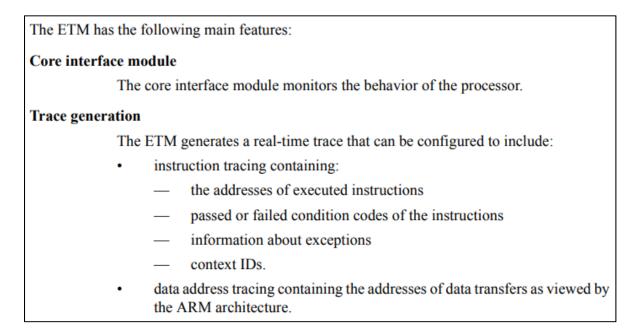
\_100095\_0001\_02\_en.pdf



Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

<u>100095\_0001\_02\_en.pdf</u>



Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K\_cortex\_a8\_r3p2\_trm.pdf

You control traci	ng in two ways:		
Triggering	Triggering controls when the collection of the trace data occurs. Setting a trigger enable you to focus trace collection around your region of interest.		
Filtering	Filtering controls the type of trace information that is collected. It is important to optimize usage of the trace port bandwidth, especially when a narrow trace port is used. Filtering the trace serves two purposes:		
	<ul> <li>It prevents overflow of the internal FIFO by minimizing the number of data transfers traced. This is especially important when the FIFO is small or the trace port is narrow.</li> </ul>		
	<ul> <li>It limits the amount of trace stored by the <i>trace capture device</i> (TCD), for example a TPA or an on-chip trace buffer. This enables more useful information to be stored around the trigger.</li> </ul>		
	You can filter the instruction trace or the data trace as follows:		
	<ul> <li>Filter the instruction trace by enabling and disabling trace generation. This is the TraceEnable function.</li> </ul>		
	<ul> <li>Filter the data trace by indicating the specific data accesses that must be traced. This is the ViewData function.</li> </ul>		

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <u>https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</u>

62. The input ports of the on-chip logic analyzer of the accused products comprises means to capture said signals from said probe lines.

63. The input ports of the on-chip logic analyzer of the accused products comprises means to align said signals propagated through said probe lines to create aligned signals.

64. The input ports of the on-chip logic analyzer of the accused products comprises means to capture said aligned signals.

65. Defendants have had knowledge of the '001 Patent at least as of the date when

they were notified of the filing of this action.

66. On November 23, 2005, the parent of the '001 Patent (U.S. Patent No. 6,687,865) was cited by the Examiner during prosecution of U.S. Patent No. 7,567,892, which is assigned to Broadcom Corp. The Examiner in that prosecution explained that the parent of the '001 Patent was pertinent because "Dervisoglu et al. (U.S. Patent No. 6,687,865) discloses an on-chip service processor for testing and debugging of integrated circuits." Broadcom employees Geoff Barrett,

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 39 of 109

Simon Christopher Dequin Clemow, and Andrew Jon Dawson, who are listed as inventors on U.S. Patent No. 7,567,892, Robert Sokohl, Jeffrey S. Weaver, and others involved in the prosecution of the patent, have had knowledge of the '001 Patent well before this suit was filed.

67. On March 6, 2006, the parent of the '001 Patent (U.S. Patent No. 6,687,865) was cited in an IDS during prosecution of U.S. Patent No. 7,533,315, which is assigned to Mediatek Inc. During that same prosecution, the Examiner also cited the child of the '001 Patent (U.S. Patent No. 7,080,301) on June 18, 2008. MediaTek employees I-Chieh Han and You-Ming Chiu, who are listed as inventors on U.S. Patent No. 7,533,315, Daniel R. McClure, and others involved in the prosecution of the patent, have had knowledge of the '001 Patent well before this suit was filed.

68. American Patents has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants are liable to American Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

69. American Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '001 Patent.

39

## COUNT II

## DIRECT INFRINGEMENT OF U.S. PATENT NO. 7,836,371

70. On November 16, 2010, United States Patent No. 7,836,371 ("the '371 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "On-Chip Service Processor."

71. American Patents is the owner of the '371 Patent, with all substantive rights in

and to that patent, including the sole and exclusive right to prosecute this action and enforce the '371 Patent against infringers, and to collect damages for all relevant times.

72. MediaTek made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its MT6595, Helio X10, and Helio X27 families of products that include advanced on-chip service capabilities ("accused products")<sup>4</sup>:

# MT6595

The world's first octa-core 4G LTE smartphone chip with the new ARM Cortex-A17 processor

MediaTek MT6795 is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6595 embeds a range of MediaTek technologies, including: MediaTek CorePilot<sup>™</sup> heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion<sup>™</sup> technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6595

<sup>&</sup>lt;sup>4</sup> A non-exhaustive list of additional accused products includes the MT6739, MT6750, MT6752, MT6753, Helio P, Helio A22, MT7622, MT7623, MT8x series (including MT8173, MT8176, MT8783, MT8785, and MT8163), and Helio X series (including Helio X20, Helio X23, and Helio X25) families of products that include advanced on-chip service capabilities.

# Processor

CPU Cluster 1: ARM-A17 @ 2.5GHz

CPU Cluster 2:

ARM-A7 @ 1.7GHz

Source: https://www.mediatek.com/products/smartphones/mt6595

## **MediaTek Helio X10**

64-bit true octa-core SoC with LTE and world's first 2K display support

MediaTek Helio XIO (MT6795) is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6795 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

## Processor

CPU Cluster 1: ARM-A53 @ 2.0GHz

CPU Cluster 2: ARM-A53 @ 2.0GHz

Cores:

Octa (8)

CPU Bit:

64-bit

Heterogeneous Multi-Processing: Yes

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

MediaTek Helio X27

Premium clocked tri-cluster, deca-core 64-bit WorldMode LTE platform

MediaTek Helio X27 (MT6797X) provides three processor clusters, each designed to more efficiently handle different types of workloads. The premium MediaTek Helio X27 features a maximized clock frequency across all three clusters, with an unequaled maximum of 2.6GHz on the powerful ARM Cortex-A72 cluster.

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

## Processor

**CPU Cluster 1:** ARM-A72 @ 2.6GHz **CPU Cluster 2:** ARM-A53 @ 2.0GHz

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

73. Broadcom made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its BCM58712 and BCM58713 families of products that include advanced on-chip service capabilities ("accused products"):

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 43 of 109

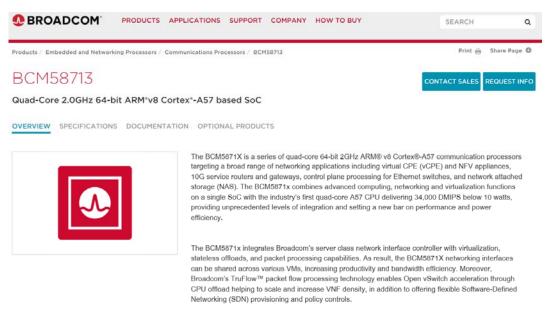




The BCM6871X is a series of quad-core 64-bit 2GH2 ARM® v8 Cortex® A57 communication processors targeting a broad range of networking applications including virtual CPE (vCPE) and NFV appliances, 10G service routers and gateways, control plane processing for Ethernet switches, and network attached storage (NAS). The BCM5871x combines advanced computing, networking and virtualization functions on a single SoC with the industry's first quad-core A57 CPU delivering 34,000 DMIPS below 10 watts, providing unprecedented levels of integration and setting a new bar on performance and power efficiency.

The BCM5871x integrates Broadcom's server class network interface controller with virtualization, stateless offloads, and packet processing capabilities. As result, the BCM5871X networking interfaces can be shared across various VMs, increasing productivity and bandwidth efficiency. Moreover, Broadcom's TruFlow™ packet flow processing technology enables Open vSwitch acceleration through CPU offload helping to scale and increase VNF density, in addition to offering flexible Software-Defined Networking (SDN) provisioning and policy controls.

# Source: https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58712/



Source: <u>https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58713/</u>

74. Lenovo made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its Lenovo Tab 4 8, Lenovo Tab 4 10, and Lenovo Tab 3 10 families of products that include advanced on-chip service capabilities ("accused products"):

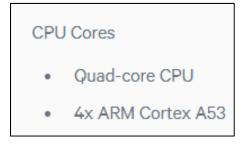
## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 44 of 109

Home > Tablets > Android Tablets > Tab 4 Series > Tab 4 8 Tab 4 8	
A tablet for the whole family Whether it's for homework, online shopping, or a screen- time treat, the Tab 4 8 is ideal for the whole family. Stylish yet rugged, this smooth-performing tablet has a vibrant 8" display, enhanced audio, and long battery life. Everyone can have their own account and there are optional add-ons aimed specifically for the younger ones. Starting at: \$116.99	10:08

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08</u>

Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> MSM8917 Processor (1.4 GHz)
Operating System	Android <sup>™</sup> Nougat 7.1

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08</u>



Source: https://www.qualcomm.com/products/snapdragon/processors/425

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 45 of 109

Home + Tablets + Android Tablets + Tab 4 Series + Tab 4 10 Tab 4 10	
From entertaining the kids to creating key presentations, the Tab 4 10 is ideal for the whole family. This stylish yet robust device offers seamless performance, a 10.1° display, immersive audio, and great battery life. What's more, everyone can have their own account and, with optional add-ons, the Tab 4 10 can be a designated kid's tablet or a more productive 2-in-1. Starting at: \$169.99	
VIEW MODELS ***** Credit & Leasing Options >	

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-X304/p/ZZITZTATB0X</u>

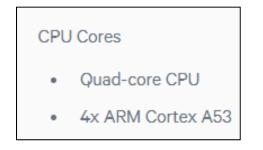
	Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> APQ8017 Processor (1.40GHz)	
--	-----------	---	--

٦

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-

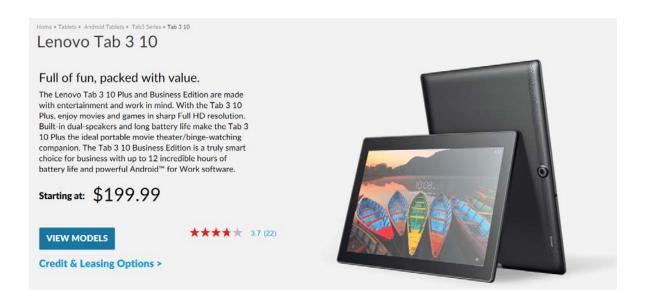
X304/p/ZZITZTATB0X

Г



Source: https://www.qualcomm.com/products/snapdragon/processors/425

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 46 of 109



Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

## Business/p/ZZITZTATB2F

Processor Media
-----------------

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

## Business/p/ZZITZTATB2F

The MediaTek MT8161 is an ARM based entry-level to mid-range SoC for (Android based) tablets. It offers four ARM Cortex-A53 processor cores (quad-core) that are clocked with up to 1.3 GHz. Furthermore, an ARM Mali-720 graphics card, a LPDDR3 memory controller (e.g., accessing 1 GB in the Lenovo Tab 2 A8-50), Bluetooth 4.0 and dual-band 802.11 b/g/n are integrated in the SoC.

Source: https://www.notebookcheck.net/Mediatek-MT8161-Tablet-SoC.145089.0.html

75. NXP made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its i.MX516, S32V234,

and i.MX 8QuadMax families of products that include advanced on-chip service capabilities

("accused products")<sup>5</sup>:

OUCTS SOLUTIO						ALL - Search		
rocessors and Microcontro	ollers ~ Arm#-Based Processo	ors and MCUs ~ I.MX App	olications Processors 👻 i MX Matu	re Processors ~ I.MX516				
	Contraction of the second s		rocessors - Mu y, ARM® Corte	-	Perform	ance, Folo	₩ 8 <	
	OVERVIEW	DOCUMENTATION	SOFTWARE & TOOLS	BUY/PARAMETRICS	PACKAGE/QU	ALITY TRAINING & SU	UPPORT	
roo. http:		n com/nro	ducts/proces	core and mi	arocontr	ollorg/arm b	ased-processo	100
								15
<u>-mcus/1.r</u>	nx-applicati	ions-proce	essors/i.mx-n	nature-proce	<u>ssors/ap</u>	plications-pr	ocessors-	
ltimedia-l	high-perform	mance-lov	v-power-con	nectivity-arr	n-cortex	-a8-core:i.M	X516	
			-1					
P							1 AC	cou
		ABOUT	522 Automatius Bistlerm v	\$321/274 Vision and Sansor	Euclon Processor		1 Ac ALL ~ Search	cou
			S32 Automotive Platform Y	532V234 Vision and Sensor	Fusion Processor		and the second se	cou
	ntrollers ~ Arm*-Based Pro	ocessors and MCUs ~	ocessor for Fr	ont and Surr	ound Vi	Family	and the second se	
	ntrollers ~ Arm*-Based Pro	ocessors and MCUs ~		ont and Surr	ound Vi	Family	ALL - Search	
	ntrollers ~ Arm*-Based Pro	ocessors and MCUs ~	ocessor for Fr nd Sensor Fus	ront and Surr sion Applicat	ound Vi	Family	ALL - Search	
	ntrollers ~ Arm <sup>a</sup> -Based Pro S32V234: Machine L	• Vision Pre Learning an	ocessor for Fr nd Sensor Fus	ront and Surr sion Applicat	ound Vi ions	ew Camera,	ALL - Search Fotow 🛛	
	ntrollers ~ Arm <sup>a</sup> -Based Pro S32V234: Machine L	• Vision Pre Learning an	ocessor for Fr nd Sensor Fus	ront and Surr sion Applicat	ound Vi ions Ametrics	ew Camera,	ALL - Search Fotow 🛛	
	Arme-Based Pro S32V234: Machine L overview Jump To Overview & Features Development Boards	• Vision Pre Learning an	OCCESSOR FOR Fr nd Sensor Fus SOFTWARE & OVERVIEW The S32V234 is our 2 family designed to sup	ront and Surr sion Applicat TOOLS BUY/PAR	round Vi ions Ametrics	ew Camera, PACKAGE/QUALITY Features Quad Arm® Cortex®-A5	ALL - Search Follow II TRAINING & SUPPORT 3 cores running up to 1GHz	<
	Arme-Based Pro S32V234: Machine L OVERVIEW Jump To Overview & Features	CORESSORS and MCUS Vision Pro earning al DOCUMENTATI	OVERVIEW The S32V234 is our 2 family designed to sup applications for image powerful 3D GPU, due security and supports	roont and Surr sion Applicat TOOLS BUY/PAR Ind generation vision pro- sport computation intensi processing and offers and it APEX-2 vision acceler SafeAssure <sup>™</sup> . S32V234	round Vi ions AMETRICS	ew Camera, PACKAGE/QUALITY Ceatures Quad Arm® Cortex®.A5 Plus M4 core up to 133	ALL - Search Follow S TRAINING & SUPPORT 3 cores running up to 1GHz MHz celerator cores enabled by	~
	Arme-Based Pro S32V234: Machine L overview Jump To Overview & Features Development Boards Target Applications	CORESSORS and MCUS Vision Pro earning al DOCUMENTATI	Occessor for Fr           nd Sensor Fus           ION         SOFTWARE &           Overview           The S32V234 is our 2           family designed to sup           applications for image           powerful 3D GPU, due           security and supports           for ADAS, NCAP from           recognition, surround	ront and Surr sion Applicat TOOLS BUY/PAR Ind generation vision prov sport computation intensi processing and offers at al APEX-2 vision acceler. SafeAssure <sup>®</sup> . S32V234 camera, object detection view, machine learning a	round Vi ions AMETRICS	PACKAGE/QUALITY  PACKAGE/QUALITY  Ceatures  Quad Arm® Cortex®.A5  Plus M4 core up to 133 Dual APEX-2 vision acc OpenCL™, APEX-CV ar	ALL V Search Fotow 2 TRAINING & SUPPORT 3 cores running up to 1GHz MHz celerator cores enabled by nd APEX graph tool nctional safety up to ASIL-C	<b>v</b>
	Arme-Based Pro S32V234: Machine L overview Jump To Overview & Features Development Boards Target Applications	CORESSORS and MCUS Vision Pro earning al DOCUMENTATI	OVERVIEW OVERVIEW The S32V234 is our 2 family designed to sup applications for image powerful 30 GPU, due security and supports for ADAS, NCAP fromt recognition, surround fusion applications, S: automotive-grade relia	ront and Surr sion Applicat TOOLS BUY/PAR Ind generation vision pro- sport computation intensi processing and offers and APEX-2 vision acceler SafeAssure <sup>®</sup> . S32V234 camera, object detection	round Vi ions AMETRICS	PACKAGE/QUALITY PACKAGE/QUALITY PACKAGE/QUALITY Ceatures Quad Arm® Cortex®-A5 Plus M4 core up to 133 Dual APEX-2 vision acc OpenCL <sup>™</sup> , APEX-CV ar Supports ISO 26262 fur IEC 61508 and DO 178	ALL V Search Fotow 2 TRAINING & SUPPORT 3 cores running up to 1GHz MHz celerator cores enabled by nd APEX graph tool nctional safety up to ASIL-C	<

Source: https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processorsand-mcus/s32-automotive-platform/vision-processor-for-front-and-surround-view-cameramachine-learning-and-sensor-fusion-applications:S32V234

<sup>&</sup>lt;sup>5</sup> A non-exhaustive list of additional accused products includes the i.MX 7 series, i.MX 8 series, i.MX Mature series, QorIQ Layerscape series, i.MX534, i.MX535, i.MX537, i.MX8M, and i.MX 8QuadPlus families of products that include advanced on-chip service capabilities.

Feature	i.MX 8QuadMax	i.MX 8QuadPlus
ARM <sup>e</sup> Core	2 x ARM Cortex®-A72	1 x Cortex-A72
ARM Core	4 x Cortex-A53	4 x Cortex-A53
ARM Core	2 x Cortex-M4F	2 x Cortex-M4F

Source: fact sheet downloaded from https://www.nxp.com/docs/en/fact-sheet/IMX8FAMFS.pdf

76. Qualcomm made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its Snapdragon 410E and

Snapdragon 650 families of products that include advanced on-chip service capabilities

("accused products")<sup>6</sup>:

Designed to meet the demanding requirements of embedded computing applications with its high performance, energy efficiency, multimedia features, integrated connectivity and long-term support, the Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 410E embedded platform is an ideal platform for the Internet of Things.

## Source: https://www.qualcomm.com/products/apq8016e

CPU

CPU Clock Speed: Up to 1.2 GHz CPU Cores: Quad-core CPU, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit, 32-bit

Source: <a href="https://www.qualcomm.com/products/apq8016e">https://www.qualcomm.com/products/apq8016e</a>

<sup>&</sup>lt;sup>6</sup> A non-exhaustive list of additional accused products includes the Snapdragon 400 tier (including Snapdragon 439 (SDM439), Snapdragon 450, Snapdragon 427 (MSM8920), and Snapdragon 435 (MSM8940)), MSM8956, the Snapdragon 600 tier (including Snapdragon 652 (MSM8976), and Snapdragon 653 (MSM8976 Pro)) families of products that include advanced on-chip service capabilities.

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 49 of 109



The Qualcomm<sup>®</sup> Snapdragon<sup>™</sup> 650 mobile platform supports high-quality, efficient performance, multimedia, gaming and connectivity, thanks to its powerful 64-bit capable hexa-core CPUs, integrated Qualcomm<sup>®</sup> Snapdragon<sup>™</sup> X8 LTE with Cat 7 speeds, Qualcomm<sup>®</sup> Adreno<sup>™</sup> 510 GPU, and support for 4K Ultra HD video.

Source: https://www.qualcomm.com/products/snapdragon/processors/650

CPU

CPU Clock Speed: Up to 1.8 GHz CPU Cores: Hexa-core CPU, 2x ARM Cortex A72, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit

Source: https://www.qualcomm.com/products/snapdragon/processors/650

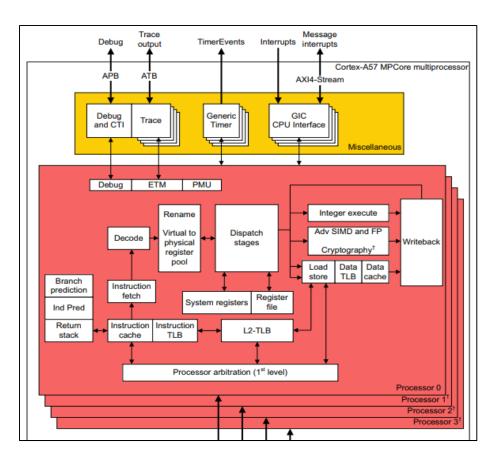
77. By doing so, Defendants have directly infringed (literally and/or under the doctrine of equivalents) at least Claim 7 of the '371 Patent. Defendants' infringement in this regard is ongoing.

78. Defendants have infringed the '371 Patent by making, having made, using,

importing, providing, supplying, distributing, selling or offering for sale integrated circuits

having advanced on-chip service capabilities.

79. The accused products include one or more logic blocks to generate one or more system-operation signals at one or more system-operation clock rates.

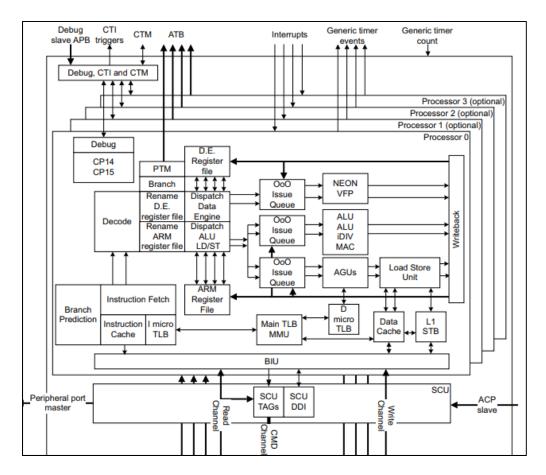


Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

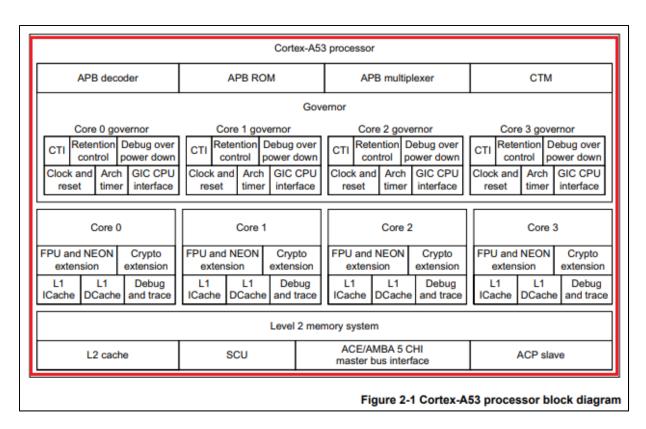
0\_trm.pdf

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 51 of 109



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

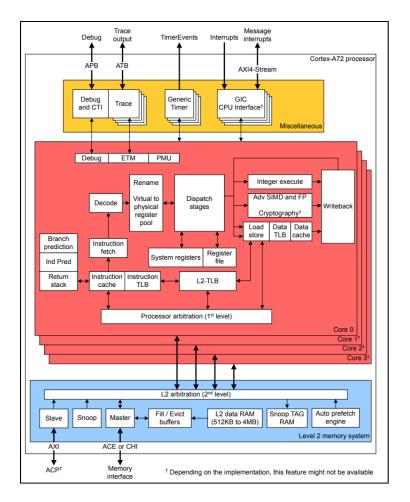
https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf



Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

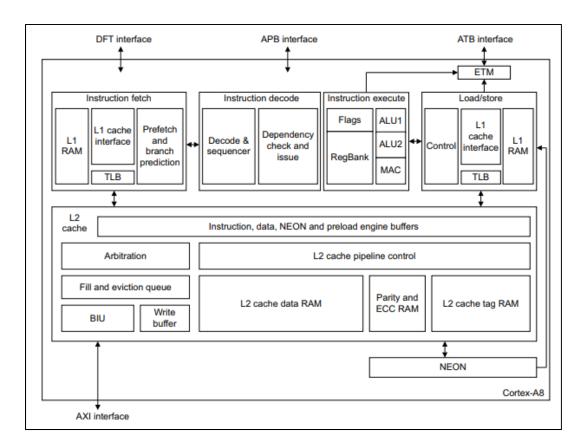
<u>df</u>



Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

<u>100095\_0001\_02\_en.pdf</u>



## Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K\_cortex\_a8\_r3p2\_trm.pdf

- 80. The accused products include a system bus.
- 81. The accused products include a service processor unit comprising a control unit, a

buffer memory, and a system bus interface.

82. The accused products include a service processor unit adapted to perform capture

and analysis of system operation signals on said system bus during normal system operation

through said system bus interface.

## Embedded Trace Macrocell architecture

The multiprocessor implements the ETMv4 architecture. See the ARM<sup>®</sup> Embedded Trace Macrocell Architecture Specification, ETMv4. Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

## 0 trm.pdf

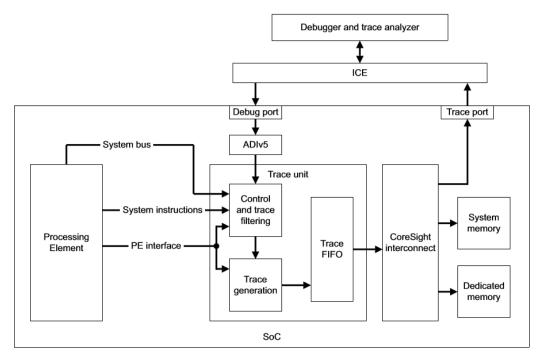
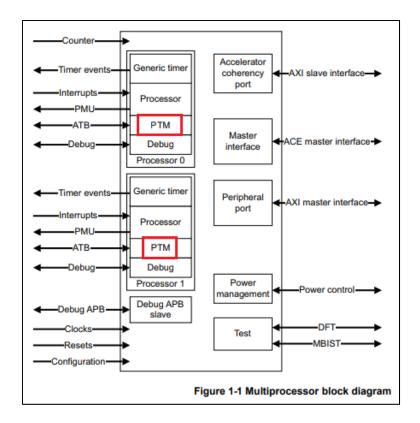


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D etm v4 architecture spec.pdf



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

The PTM is a real-time instruction flow trace module that complies with the *Program Flow Trace* (PFTv1.1) architecture. The PTM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5.

For more information see:

- ARM<sup>®</sup> CoreSight<sup>™</sup> Architecture Specification (ARM IHI 0029).
- ARM<sup>®</sup> CoreSight<sup>™</sup> SoC Technical Reference Manual (ARM DDI 0480).

Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

## Embedded Trace Macrocell architecture

The Cortex-A53 processor implements the ETMv4 architecture. See the ARM<sup>®</sup> ETM<sup>™</sup> Architecture Specification, ETMv4.

Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

## <u>df</u>

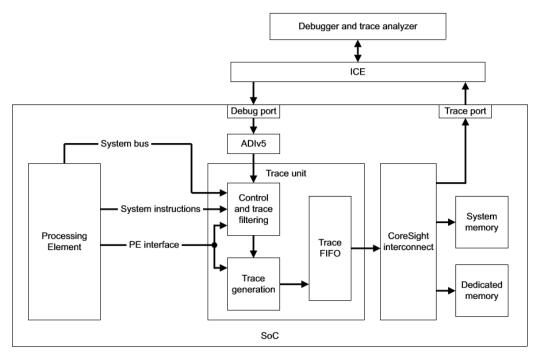


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D etm v4 architecture spec.pdf

### Embedded Trace Macrocell architecture

The processor implements the ETMv4 architecture. See the *ARM*<sup>®</sup> *Embedded Trace Macrocell Architecture Specification, ETMv4.* 

Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095 0001 02 en/cortex a72 mpcore trm

\_100095\_0001\_02\_en.pdf

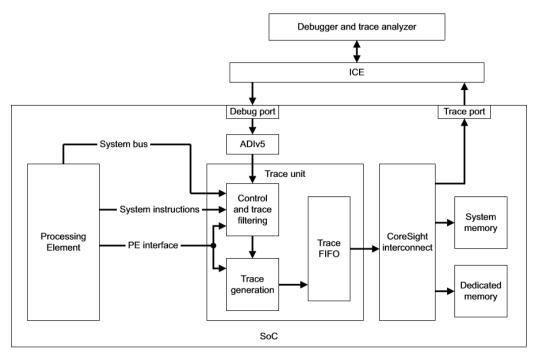


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

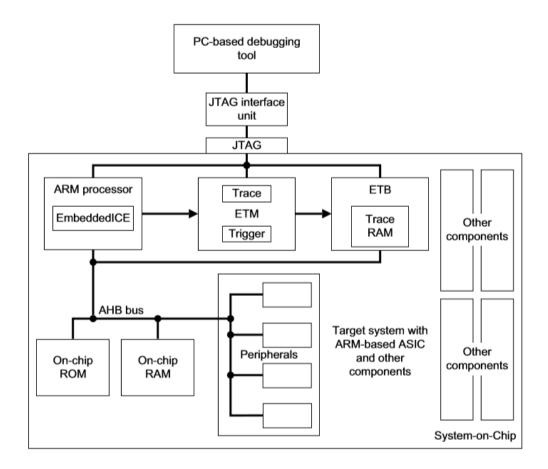
https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

## About the ETM The ETM is a CoreSight<sup>™</sup> component designed for use with the CoreSight Design Kit. CoreSight is the ARM extensible, system-wide debug and trace architecture. The Cortex-A8 processor implements the ETM architecture v3.3.

Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K\_cortex\_a8\_r3p2\_trm.pdf

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 59 of 109



Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

About controlling	tracing	
You control traci	ng in two ways:	
Triggering	Triggering controls when the collection of the trace data occurs. Setting a trigger enabyou to focus trace collection around your region of interest.	
Filtering	Filtering controls the type of trace information that is collected. It is important to optimize usage of the trace port bandwidth, especially when a narrow trace port is used. Filtering the trace serves two purposes:	
	<ul> <li>It prevents overflow of the internal FIFO by minimizing the number of data transfers traced. This is especially important when the FIFO is small or the trace port is narrow.</li> </ul>	
	<ul> <li>It limits the amount of trace stored by the <i>trace capture device</i> (TCD), for example a TPA or an on-chip trace buffer. This enables more useful information to be stored around the trigger.</li> </ul>	
	You can filter the instruction trace or the data trace as follows:	
	<ul> <li>Filter the instruction trace by enabling and disabling trace generation. This is the TraceEnable function.</li> </ul>	
	<ul> <li>Filter the data trace by indicating the specific data accesses that must be traced. This is the ViewData function.</li> </ul>	

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <a href="https://static.docs.arm.com/ihi0014/q/IHI0014.pdf">https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</a>

In this specification:

- An ETM is said to be tracing when **TraceEnable** is active and no condition exists that prohibits tracing. Conditions that prohibit tracing include:
  - The processor is in Debug state.
    - The processor is in a Wait For Interrupt (WFI) or Wait For Event (WFE) condition. See Wait For Interrupt and Wait For Event on page 4-251.

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <u>https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</u>

83. Defendants have had knowledge of the '371 Patent at least as of the date when they were notified of the filing of this action.

84. On November 23, 2005, the great-grandparent of the '371 Patent (U.S. Patent No.

6,687,865) was cited by the Examiner during prosecution of U.S. Patent No. 7,567,892, which is assigned to Broadcom Corp. The Examiner in that prosecution explained that the greatgrandparent of the '371 Patent was pertinent because "Dervisoglu et al. (U.S. Patent No. 6,687,865) discloses an on-chip service processor for testing and debugging of integrated circuits." Broadcom employees Geoff Barrett, Simon Christopher Dequin Clemow, and Andrew Jon Dawson, who are listed as inventors on U.S. Patent No. 7,567,892, Robert Sokohl, Jeffrey S. Weaver, and others involved in the prosecution of the patent, have had knowledge of the '371 Patent well before this suit was filed.

85. On March 6, 2006, the great-grandparent of the '371 Patent (U.S. Patent No. 6,687,865) was cited in an IDS during prosecution of U.S. Patent No. 7,533,315, which is assigned to Mediatek Inc. During that same prosecution, the Examiner also cited the parent of the '371 Patent (U.S. Patent No. 7,080,301) on June 18, 2008. MediaTek employees I-Chieh Han and You-Ming Chiu, who are listed as inventors on U.S. Patent No. 7,533,315, Daniel R.

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 61 of 109

McClure, and others involved in the prosecution of the patent, have had knowledge of the '371 Patent well before this suit was filed.

86. American Patents has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants are liable to American Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

87. American Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '371 Patent.

#### COUNT III

### **DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,239,716**

88. On August 7, 2012, United States Patent No. 8,239,716 ("the '716 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "On-Chip Service Processor."

89. American Patents is the owner of the '716 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '716 Patent against infringers, and to collect damages for all relevant times.

90. MediaTek made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its MT6595, Helio X10, and Helio X27 families of products that include advanced on-chip service capabilities ("accused products")<sup>7</sup>:

<sup>&</sup>lt;sup>7</sup> A non-exhaustive list of additional accused products includes the MT6739, MT6750, MT6752, MT6753, Helio P, Helio A22, MT7622, MT7623, MT8x series (including MT8173, MT8176,

# MT6595

## The world's first octa-core 4G LTE smartphone chip with the new ARM Cortex-A17 processor

MediaTek MT6795 is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6595 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6595



CPU Cluster 1: ARM-A17 @ 2.5GHz

CPU Cluster 2: ARM-A7 @ 1.7GHz

Source: https://www.mediatek.com/products/smartphones/mt6595

## MediaTek Helio X10

64-bit true octa-core SoC with LTE and world's first 2K display support

MediaTek Helio X10 (MT6795) is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full. HD Super-Slow Motion videos. MT6795 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

MT8783, MT8785, and MT8163), and Helio X series (including Helio X20, Helio X23, and Helio X25) families of products that include advanced on-chip service capabilities.

Processor

CPU Cluster 1: ARM-A53 @ 2.0GHz

CPU Cluster 2: ARM-A53 @ 2.0GHz

Cores:

Octa (8)

CPU Bit:

64-bit

Heterogeneous Multi-Processing: Yes

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

# MediaTek Helio X27

Premium clocked tri-cluster, deca-core 64-bit WorldMode LTE platform

MediaTek Helio X27 (MT6797X) provides three processor clusters, each designed to more efficiently handle different types of workloads. The premium MediaTek Helio X27 features a maximized clock frequency across all three clusters, with an unequaled maximum of 2.6GHz on the powerful ARM Cortex-A72 cluster.

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

# Processor

CPU Cluster 1: ARM-A72 @ 2.6GHz

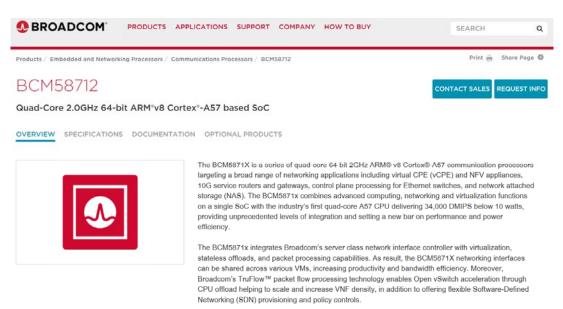
CPU Cluster 2: ARM-A53 @ 2.0GHz

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

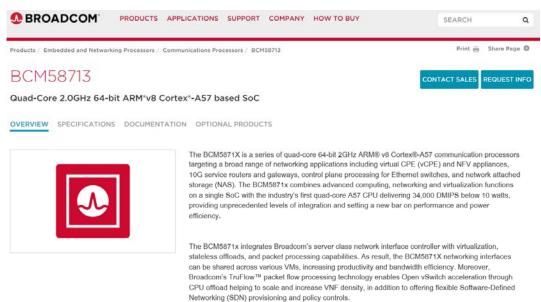
### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 64 of 109

91. Broadcom made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its BCM58712 and BCM58713 families of products that include advanced on-chip service capabilities ("accused products"):



# Source: <u>https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58712/</u>



Source: <u>https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58713/</u>

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 65 of 109

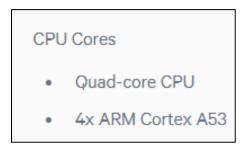
92. Lenovo made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its Lenovo Tab 4 8, Lenovo Tab 4 10, and Lenovo Tab 3 10 families of products that include advanced on-chip service capabilities ("accused products"):

Home > Tablets > Android Tablets > Tab 4 Series > Tab 4 8 Tab 4 8	
A tablet for the whole family Whether it's for homework, online shopping, or a screen- time treat, the Tab 4 8 is ideal for the whole family. Stylish yet rugged, this smooth-performing tablet has a vibrant 8* display, enhanced audio, and long battery life. Everyone can have their own account and there are optional add-ons aimed specifically for the younger ones. Starting at: \$116.99	80.01
VIEW MODELS	

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08

Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> MSM8917 Processor (1.4 GHz)
Operating System	Android <sup>™</sup> Nougat 7.1

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08



Source: https://www.qualcomm.com/products/snapdragon/processors/425

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 66 of 109

Home + Tablets + Android Tablets + Tab 4 Series + Tab 4 10 Tab 4 10	
From entertaining the kids to creating key presentations, the Tab 4 10 is ideal for the whole family. This stylish yet robust device offers seamless performance. a 10.1 <sup>sh</sup> display, immersive audio, and great battery life. What's more, everyone can have their own account and, with optional add-ons, the Tab 4 10 can be a designated kid's tablet or a more productive 2-in-1.	
Starting at: \$169.99	
Credit & Leasing Options >	

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-X304/p/ZZITZTATB0X</u>

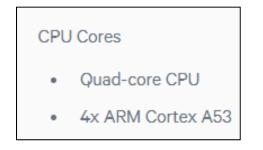
	Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> APQ8017 Processor (1.40GHz)	
--	-----------	---	--

٦

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-

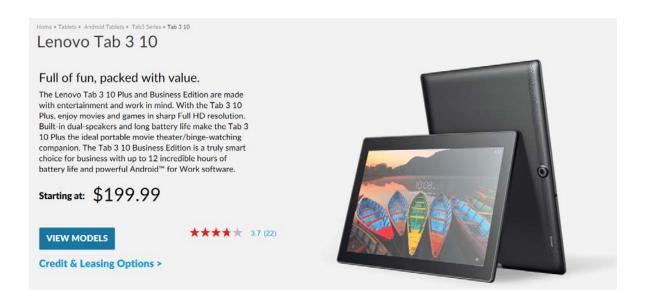
X304/p/ZZITZTATB0X

Г



Source: https://www.qualcomm.com/products/snapdragon/processors/425

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 67 of 109



Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

## Business/p/ZZITZTATB2F

3)	)
----	---

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

## Business/p/ZZITZTATB2F

The MediaTek MT8161 is an ARM based entry-level to mid-range SoC for (Android based) tablets. It offers four ARM Cortex-A53 processor cores (quad-core) that are clocked with up to 1.3 GHz. Furthermore, an ARM Mali-720 graphics card, a LPDDR3 memory controller (e.g., accessing 1 GB in the Lenovo Tab 2 A8-50), Bluetooth 4.0 and dual-band 802.11 b/g/n are integrated in the SoC.

Source: https://www.notebookcheck.net/Mediatek-MT8161-Tablet-SoC.145089.0.html

93. NXP made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its i.MX516, S32V234,

and i.MX 8QuadMax families of products that include advanced on-chip service capabilities

("accused products")<sup>8</sup>:

DUCTS SOLUT						ALL - Search		
Processors and Microci	ontrollers ~ Arm#-Based Processo	rs and MCUs ~ I.MX App	olications Processors 👻 i MX Matu	ure Processors ~ I.MX516				
	Contraction of the second second second		rocessors - Mu y, ARM® Corte	-	Perform	nance,	Follow 🛛 🛠	
	OVERVIEW	DOCUMENTATION	SOFTWARE & TOOLS	BUY/PARAMETRICS	PACKAGE/	QUALITY TRAINING	& SUPPORT	
uraa. htt	ps://www.nxj	n com/nro	ducts/proces	core and mi	arooon	rollors/orm	hasad proces	aaara
	-		_					<u>55015</u>
<u>1-mcus/1</u>	<u>.mx-applicati</u>	lons-proce	essors/1.mx-n	nature-proce	essors/a	pplications-p	processors-	
ltimedia	-high-perform	mance-lov	v-nower-con	nectivity-ar	n-corte	x-a8-core:i.N	MX516	
			-1					
<b>N</b> P								1 ACCOU
	UTIONS SUPPORT	ABOUT	S22 Automotive Distorm v 1	\$32V234 Vielon and Sensol	Eusion Process	e Camily	ALL - Search	1 ACCOU
	UTIONS SUPPORT		S32 Automotive Platform ~	S32V234 Vision and Sensor	Fusion Process	r Family	ALL - Search	1 Accour
	ocontrollers ~ Arm*-Based Pro S32V234:	occessors and MCUs ~	ocessor for Fr	ront and Sur	round V			
	ocontrollers ~ Arm*-Based Pro S32V234:	occessors and MCUs ~		ront and Sur	round V			
	ocontrollers ~ Arm*-Based Pro S32V234:	occessors and MCUs ~	ocessor for Fr nd Sensor Fus	ront and Sur sion Applica	round V			
	S32V234: Machine L	Vision Pre Learning at	ocessor for Fr nd Sensor Fus	ront and Sur sion Applica	round V tions	iew Camera,	Follow	⊠ ≺
	S32V234: Machine L	Vision Pre Learning at	ocessor for Fr nd Sensor Fus	ront and Sur sion Applica	round V tions	iew Camera,	Follow	⊠ ≺
	ocontrollers ~ Arm*-Based Pro S32V234: Machine L overview Jump To Overview & Features Development Boards	Vision Pre Learning at	OCCESSOR FOR Fr nd Sensor Fus SOFTWARE & OVERVIEW The S32V234 is our 2 family designed to sup	ront and Sur sion Applica TOOLS BUY/PA	round V tions RAMETRICS	iew Camera, PACKAGE/QUALITY Features = Quad Arm® Cortex®-	TRAINING & SUPP	D ≺
	ocontrollers ~ Arm*-Based Pro S32V234: Machine L OVERVIEW Jump To Overview & Features	Vision Pro earning al	OCCESSOR FOR Fr           IND SOFTWARE &           OVERVIEW           The S32V234 is our 2 family designed to sup applications for image powerful 3D GPU, due	ront and Sur sion Applica TOOLS BUY/PA	round V tions RAMETRICS REGESSOR ive in 1SP, rators,	iew Camera, PACKAGE/QUALITY Features Plus M4 core up to 1 Dual APEX-2 vision	A53 cores running up to 133 MHz	DORT
	Controllers ~ Arm=Based Pro S32V234: Machine L OVERVIEW Jump To Overview & Features Development Boards Target Applications	Vision Pro earning al	Occessor for Fr           nd Sensor Fus           ION         SOFTWARE &           Overview           The S32V234 is our 2           family designed to sup           applications for image           powerful 3D GPU, due           security and supports           for ADAS, NCAP from           recognition, surround	tod generation vision pro boot computation intension processing and offers a al APEX-2 vision accele SafeAssure <sup>®</sup> . S32V234 t camera, object detectiv view, machine learning	round V tions RAMETRICS REAMETRICS	Features Quad Arm® Cortex® Quad Arm® Cortex® Quad Arm® Cortex® Dual APEX-2 vision OpenCL <sup>™</sup> , APEX-CV Supports ISO 26262	TRAINING & SUPP TRAINING & SUPP A53 cores running up to 4 133 MHz accelerator cores enabled / and APEX graph tool ? functional safety up to A3	PORT 1GHz, id by
	Controllers ~ Arm=Based Pro S32V234: Machine L OVERVIEW Jump To Overview & Features Development Boards Target Applications	Vision Pro earning al	OVERVIEW OVERVIEW The S32V234 is our 2 family designed to sup applications for image powerful 30 GPU, due security and supports for ADAS, NCAP front recognition, surround fusion applications, S: automotive-grade relia	ront and Sur sion Applica TOOLS BUY/PA Ind generation vision pro poort computation intens processing and offers i al APEX-2 vision accele SafeAssure <sup>®</sup> . S32V234 t camera, object detection	round V tions RAMETRICS REGESSOR ive un ISP, rators, is suited on and and sensor or and	Features Quad Arm® Cortex® Quad Arm® Cortex® Quad Arm® Cortex® Dual APEX-2 vision OpenCL <sup>™</sup> , APEX-CV Supports ISO 26262 IEC 61508 and D0 1	A53 cores running up to 4 33 MHz accelerator cores enabler/ 4 and APEX graph tool f.functional safety up to A: 178 applications with OpenCL 1.2 EP 2.0, 6	DORT 1GHz, ed by SSIL-C,

Source: https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processorsand-mcus/s32-automotive-platform/vision-processor-for-front-and-surround-view-cameramachine-learning-and-sensor-fusion-applications:S32V234

<sup>&</sup>lt;sup>8</sup> A non-exhaustive list of additional accused products includes the i.MX 7 series, i.MX 8 series, i.MX Mature series, QorIQ Layerscape series, i.MX534, i.MX535, i.MX537, i.MX8M, and i.MX 8QuadPlus families of products that include advanced on-chip service capabilities.

Feature	i.MX 8QuadMax	i.MX 8QuadPlus		
ARM <sup>e</sup> Core	2 x ARM Cortex®-A72	1 x Cortex-A72		
ARM Core	4 x Cortex-A53	4 x Cortex-A53		
ARM Core	2 x Cortex-M4F	2 x Cortex-M4F		

Source: fact sheet downloaded from https://www.nxp.com/docs/en/fact-sheet/IMX8FAMFS.pdf

94. Qualcomm made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its Snapdragon 410E and

Snapdragon 650 families of products that include advanced on-chip service capabilities

("accused products")<sup>9</sup>:

Designed to meet the demanding requirements of embedded computing applications with its high performance, energy efficiency, multimedia features, integrated connectivity and long-term support, the Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 410E embedded platform is an ideal platform for the Internet of Things.

## Source: https://www.qualcomm.com/products/apq8016e

CPU

CPU Clock Speed: Up to 1.2 GHz CPU Cores: Quad-core CPU, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit, 32-bit

Source: <a href="https://www.qualcomm.com/products/apq8016e">https://www.qualcomm.com/products/apq8016e</a>

<sup>&</sup>lt;sup>9</sup> A non-exhaustive list of additional accused products includes the Snapdragon 400 tier (including Snapdragon 439 (SDM439), Snapdragon 450, Snapdragon 427 (MSM8920), and Snapdragon 435 (MSM8940)), MSM8956, the Snapdragon 600 tier (including Snapdragon 652 (MSM8976), and Snapdragon 653 (MSM8976 Pro)) families of products that include advanced on-chip service capabilities.

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 70 of 109



The Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 650 mobile platform supports high-quality, efficient performance, multimedia, gaming and connectivity, thanks to its powerful 64-bit capable hexa-core CPUs, integrated Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> X8 LTE with Cat 7 speeds, Qualcomm<sup>®</sup> Adreno<sup>®</sup> 510 GPU, and support for 4K Ultra HD video.

Source: https://www.qualcomm.com/products/snapdragon/processors/650

CPU

CPU Clock Speed: Up to 1.8 GHz CPU Cores: Hexa-core CPU, 2x ARM Cortex A72, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit

Source: https://www.qualcomm.com/products/snapdragon/processors/650

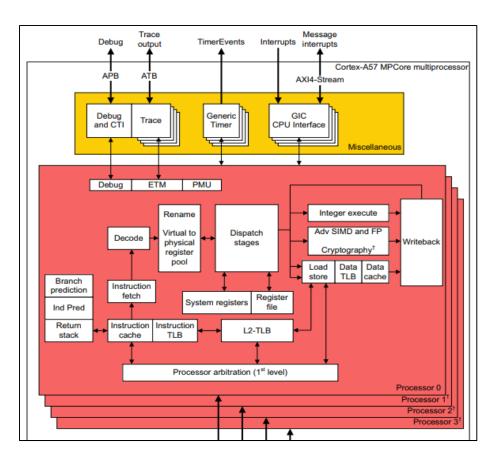
95. By doing so, Defendants have directly infringed (literally and/or under the doctrine of equivalents) at least Claim 1 of the '716 Patent. Defendants' infringement in this regard is ongoing.

96. Defendants have infringed the '716 Patent by making, having made, using,

importing, providing, supplying, distributing, selling or offering for sale integrated circuits

having advanced on-chip service capabilities.

97. The accused products include one or more logic blocks to generate one or more system operation signals at one or more system operation clock rates.

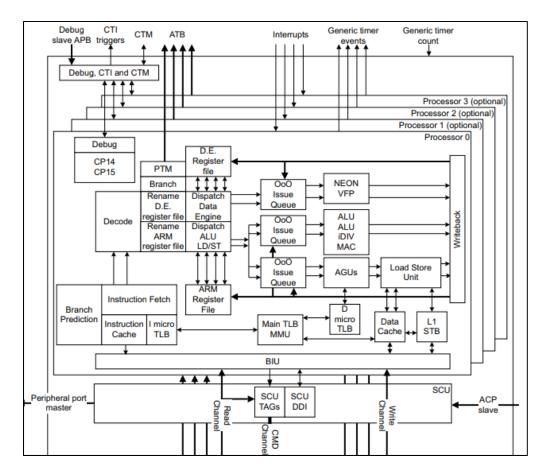


Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

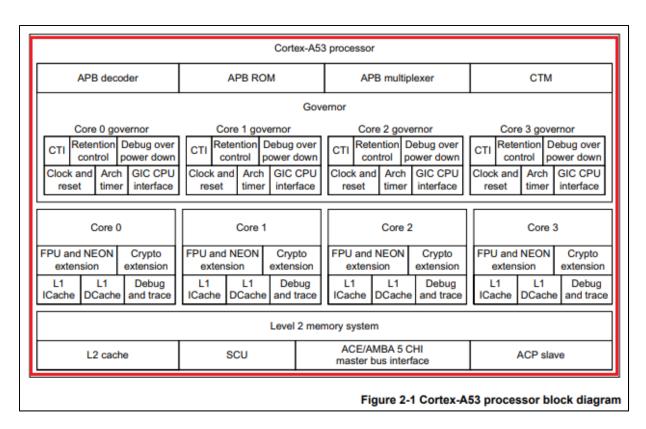
0\_trm.pdf

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 72 of 109



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

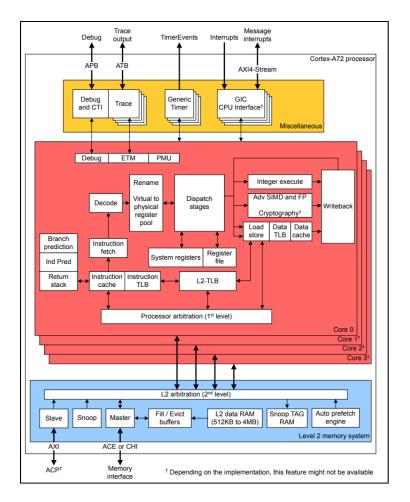
https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf



Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

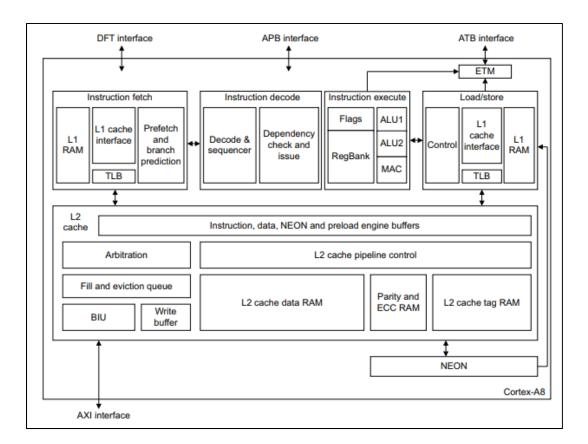
<u>df</u>



Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

<u>100095\_0001\_02\_en.pdf</u>



#### Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K cortex a8 r3p2 trm.pdf

98. The accused products include a service processor unit configured to perform one

or more debug operations on one or more of said logic blocks.

#### Embedded Trace Macrocell architecture

The multiprocessor implements the ETMv4 architecture. See the ARM<sup>®</sup> Embedded Trace Macrocell Architecture Specification, ETMv4.

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C\_cortex\_a57\_mpcore\_r1p

0\_trm.pdf

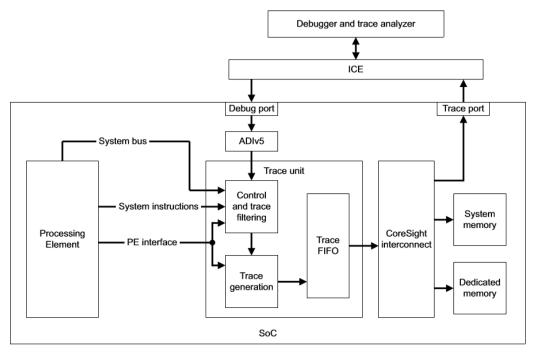
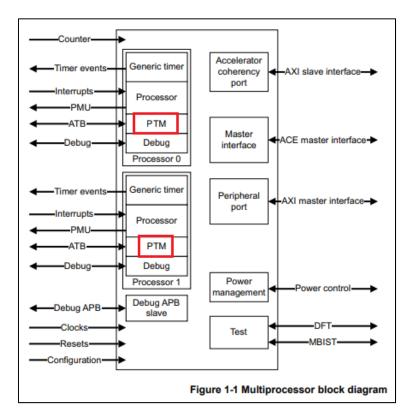


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

The PTM is a real-time instruction flow trace module that complies with the *Program Flow Trace* (PFTv1.1) architecture. The PTM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5.

For more information see:

- ARM<sup>®</sup> CoreSight<sup>™</sup> Architecture Specification (ARM IHI 0029).
- ARM<sup>®</sup> CoreSight<sup>™</sup> SoC Technical Reference Manual (ARM DDI 0480).

Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

### Embedded Trace Macrocell architecture

The Cortex-A53 processor implements the ETMv4 architecture. See the ARM<sup>®</sup> ETM<sup>™</sup> Architecture Specification, ETMv4.

Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D cortex a53 r0p2 trm.p

<u>df</u>

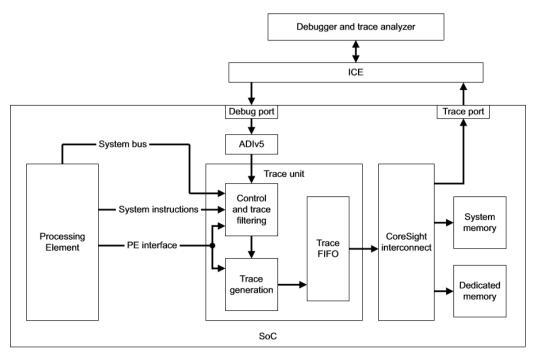


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

#### Embedded Trace Macrocell architecture

The processor implements the ETMv4 architecture. See the *ARM*<sup>®</sup> *Embedded Trace Macrocell Architecture Specification, ETMv4.* 

Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

<u>100095\_0001\_02\_en.pdf</u>

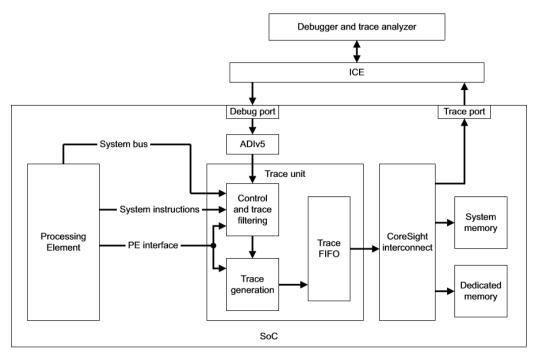


Figure 1-1 Example SoC with a trace unit

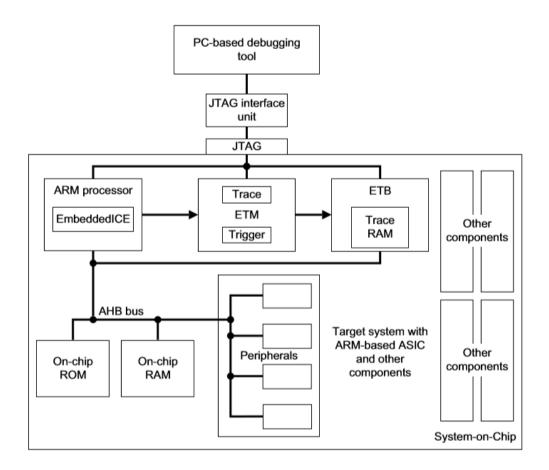
Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

## About the ETM The ETM is a CoreSight<sup>™</sup> component designed for use with the CoreSight Design Kit. CoreSight is the ARM extensible, system-wide debug and trace architecture. The Cortex-A8 processor implements the ETM architecture v3.3.

Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K\_cortex\_a8\_r3p2\_trm.pdf



Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

About controlling	tracing	
You control tracin	ng in two ways:	
Triggering	Triggering controls when the collection of the trace data occurs. Setting a trigger enables you to focus trace collection around your region of interest.	
Filtering	Filtering controls the type of trace information that is collected. It is important to optimize usage of the trace port bandwidth, especially when a narrow trace port is used. Filtering the trace serves two purposes:	
	<ul> <li>It prevents overflow of the internal FIFO by minimizing the number of data transfers traced. This is especially important when the FIFO is small or the trace port is narrow.</li> </ul>	
	<ul> <li>It limits the amount of trace stored by the trace capture device (TCD), for example a TPA or an on-chip trace buffer. This enables more useful information to be stored around the trigger.</li> </ul>	
	You can filter the instruction trace or the data trace as follows:	
	<ul> <li>Filter the instruction trace by enabling and disabling trace generation. This is the TraceEnable function.</li> </ul>	
	<ul> <li>Filter the data trace by indicating the specific data accesses that must be traced. This is the ViewData function.</li> </ul>	

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <u>https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</u>

In this specification:

- An ETM is said to be tracing when **TraceEnable** is active and no condition exists that prohibits tracing. Conditions that prohibit tracing include:
  - The processor is in Debug state.
    - The processor is in a Wait For Interrupt (WFI) or Wait For Event (WFE) condition. See Wait For Interrupt and Wait For Event on page 4-251.

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <u>https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</u>

99. The service processor unit of the accused products includes a control unit, a buffer memory, an analysis engine, and a bus interface.

100. The accused products include a multiplicity of probe lines configured to capture and propagate one or more of said one or more system operation signals from said logic blocks to said service processor unit during normal system operation.

101. The accused products include said analysis engine configured to align signals received from said probe lines during normal system operation.

102. Defendants have had knowledge of the '716 Patent at least as of the date when they were notified of the filing of this action.

103. On November 23, 2005, the great-great-grandparent of the '716 Patent (U.S.

Patent No. 6,687,865) was cited by the Examiner during prosecution of U.S. Patent No.

7,567,892, which is assigned to Broadcom Corp. The Examiner in that prosecution explained that the great-great-grandparent of the '716 Patent was pertinent because "Dervisoglu et al. (U.S. Patent No. 6,687,865) discloses an on-chip service processor for testing and debugging of integrated circuits." Broadcom employees Geoff Barrett, Simon Christopher Dequin Clemow, and Andrew Jon Dawson, who are listed as inventors on U.S. Patent No. 7,567,892, Robert

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 82 of 109

Sokohl, Jeffrey S. Weaver, and others involved in the prosecution of the patent, have had knowledge of the '716 Patent well before this suit was filed.

104. On March 6, 2006, the great-great grandparent of the '716 Patent (U.S. Patent No. 6,687,865) was cited in an IDS during prosecution of U.S. Patent No. 7,533,315, which is assigned to Mediatek Inc. During that same prosecution, the Examiner also cited the grandparent of the '716 Patent (U.S. Patent No. 7,080,301) on June 18, 2008. MediaTek employees I-Chieh Han and You-Ming Chiu, who are listed as inventors on U.S. Patent No. 7,533,315, Daniel R. McClure, and others involved in the prosecution of the patent, have had knowledge of the '716 Patent well before this suit was filed.

105. American Patents has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants are liable to American Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

106. American Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '716 Patent.

82

#### COUNT IV

## **DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,996,938**

107. On March 31, 2015, United States Patent No. 8,996,938 ("the '938 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "On-Chip Service Processor."

108. American Patents is the owner of the '938 Patent, with all substantive rights in

and to that patent, including the sole and exclusive right to prosecute this action and enforce the '938 Patent against infringers, and to collect damages for all relevant times.

109. MediaTek made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its MT6595, Helio X10, and Helio X27 families of products that include advanced on-chip service capabilities ("accused products")<sup>10</sup>:

# MT6595

The world's first octa-core 4G LTE smartphone chip with the new ARM Cortex-A17 processor

MediaTek MT6795 is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6595 embeds a range of MediaTek technologies, including: MediaTek CorePilot<sup>™</sup> heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion<sup>™</sup> technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6595

<sup>&</sup>lt;sup>10</sup> A non-exhaustive list of additional accused products includes the MT6739, MT6750, MT6752, MT6753, Helio P, Helio A22, MT7622, MT7623, MT8x series (including MT8173, MT8176, MT8783, MT8785, and MT8163), and Helio X series (including Helio X20, Helio X23, and Helio X25) families of products that include advanced on-chip service capabilities.

# Processor

CPU Cluster 1: ARM-A17 @ 2.5GHz

CPU Cluster 2:

ARM-A7 @ 1.7GHz

Source: https://www.mediatek.com/products/smartphones/mt6595

## **MediaTek Helio X10**

64-bit true octa-core SoC with LTE and world's first 2K display support

MediaTek Helio XIO (MT6795) is a high-performance SoC which satisfies multimedia requirements of even the most demanding users, featuring multimedia subsystems that support many technologies never before possible or seen in a smartphone, including support for 120Hz displays and the capability to create and playback 480 frames per second (fps) 1080p Full HD Super-Slow Motion videos. MT6795 embeds a range of MediaTek technologies, including: MediaTek CorePilot™ heterogeneous multiprocessing technology which unlocks the power of all eight cores for outstanding performance with ultra-low power consumption and thermal control, as well as dual-channel LPDDR3 clocked at 933MHz for top-end memory bandwidth in a smartphone. MediaTek ClearMotion™ technology to eliminate motion jitter and ensure smooth video playback on mobile devices.

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

## Processor

CPU Cluster 1: ARM-A53 @ 2.0GHz

CPU Cluster 2: ARM-A53 @ 2.0GHz

Cores:

Octa (8)

CPU Bit:

64-bit

Heterogeneous Multi-Processing: Yes

Source: https://www.mediatek.com/products/smartphones/mt6795-helio-x10

MediaTek Helio X27

Premium clocked tri-cluster, deca-core 64-bit WorldMode LTE platform

MediaTek Helio X27 (MT6797X) provides three processor clusters, each designed to more efficiently handle different types of workloads. The premium MediaTek Helio X27 features a maximized clock frequency across all three clusters, with an unequaled maximum of 2.6GHz on the powerful ARM Cortex-A72 cluster.

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

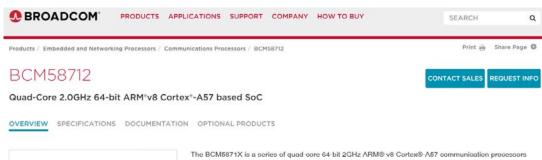
## Processor

**CPU Cluster 1:** ARM-A72 @ 2.6GHz **CPU Cluster 2:** ARM-A53 @ 2.0GHz

Source: https://www.mediatek.com/products/smartphones/mt6797x-helio-x27

110. Broadcom made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its BCM58712 and BCM58713 families of products that include advanced on-chip service capabilities ("accused products"):

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 86 of 109

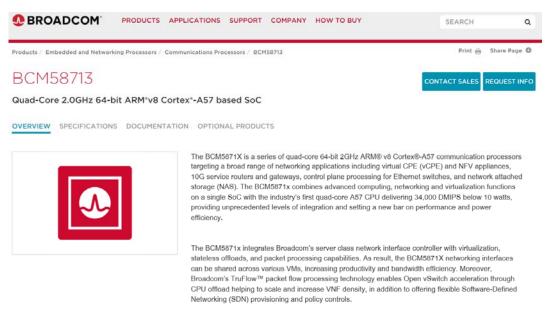




The BCMS871X is a series of quad-core 64-bit 2GHz ARM® v8 Cortex® A57 communication processors targeting a broad range of networking applications including virtual CPE (vCPE) and NFV appliances, 10G service routers and gateways, control plane processing for Ethernet switches, and network attached storage (NAS). The BCM5871x combines advanced computing, networking and virtualization functions on a single SoC with the industry's first quad-core A57 CPU delivering 34,000 DMIPS below 10 watts, providing unprecedented levels of integration and setting a new bar on performance and power efficiency.

The BCM5871x integrates Broadcom's server class network interface controller with virtualization, stateless offloads, and packet processing capabilities. As result, the BCM5871X networking interfaces can be shared across various VMs, increasing productivity and bandwidth efficiency. Moreover, Broadcom's TruFlow™ packet flow processing technology enables Open vSwitch acceleration through CPU offload helping to scale and increase VNF density, in addition to offering flexible Software-Defined Networking (SDN) provisioning and policy controls.

## Source: https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58712/



Source: <u>https://www.broadcom.com/products/embedded-and-networking-processors/communications/bcm58713/</u>

111. Lenovo made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its Lenovo Tab 4 8, Lenovo Tab 4 10, and Lenovo Tab 3 10 families of products that include advanced on-chip service capabilities ("accused products"):

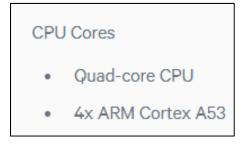
## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 87 of 109

Home $\times$ Tablets $\times$ Android Tablets $\times$ Tab 4 Series $\times$ Tab 4 8 Tab 4 8	
A tablet for the whole family	
Whether it's for homework, online shopping, or a screen- time treat, the Tab 4 8 is ideal for the whole family. Stylish yet rugged, this smooth-performing tablet has a vibrant 8" display, enhanced audio, and long battery life. Everyone can have their own account and there are optional add-ons aimed specifically for the younger ones.	10:08
Starting at: \$116.99	

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08</u>

Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> MSM8917 Processor (1.4 GHz)
Operating System	Android <sup>™</sup> Nougat 7.1

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-8504/p/ZZITZTATB08</u>



Source: https://www.qualcomm.com/products/snapdragon/processors/425

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 88 of 109

Home + Tablets + Android Tablets + Tab 4 Series + Tab 4 10 Tab 4 10	
From entertaining the kids to creating key presentations, the Tab 4 10 is ideal for the whole family. This stylish yet robust device offers seamless performance, a 10.1° display, immersive audio, and great battery life. What's more, everyone can have their own account and, with optional add-ons, the Tab 4 10 can be a designated kid's tablet or a more productive 2-in-1. Starting at: \$169.99	
VIEW MODELS ***** Credit & Leasing Options >	

Source: <u>https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-X304/p/ZZITZTATB0X</u>

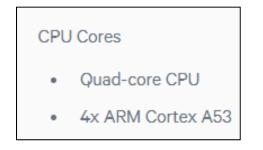
	Processor	Qualcomm <sup>®</sup> Snapdragon <sup>™</sup> APQ8017 Processor (1.40GHz)	
--	-----------	---	--

٦

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab-4-series/Lenovo-TB-

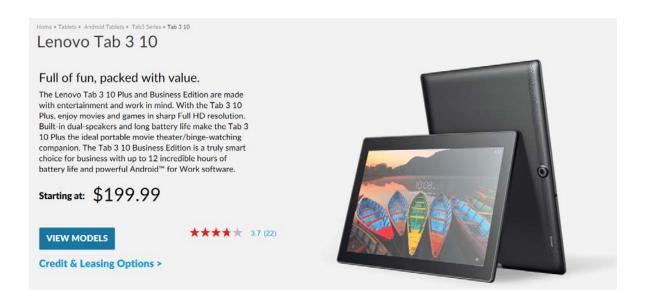
X304/p/ZZITZTATB0X

Г



Source: https://www.qualcomm.com/products/snapdragon/processors/425

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 89 of 109



Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

## Business/p/ZZITZTATB2F

Processor Media
-----------------

Source: https://www.lenovo.com/us/en/tablets/android-tablets/tab3-series/Lenovo-Tab-3-10-

#### Business/p/ZZITZTATB2F

The MediaTek MT8161 is an ARM based entry-level to mid-range SoC for (Android based) tablets. It offers four ARM Cortex-A53 processor cores (quad-core) that are clocked with up to 1.3 GHz. Furthermore, an ARM Mali-720 graphics card, a LPDDR3 memory controller (e.g., accessing 1 GB in the Lenovo Tab 2 A8-50), Bluetooth 4.0 and dual-band 802.11 b/g/n are integrated in the SoC.

Source: https://www.notebookcheck.net/Mediatek-MT8161-Tablet-SoC.145089.0.html

112. NXP made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its i.MX516, S32V234,

and i.MX 8QuadMax families of products that include advanced on-chip service capabilities

("accused products")<sup>11</sup>:

	ONS SUPPORT ABO	DUT				ALL - Search		
Processors and Microcont	trollers ~ Arm#-Based Processors	s and MCUs 👻 i.MX App	plications Processors 👻 i MX Matu	ure Processors ~ I.MX516				
			Processors - Mu cy, ARM® Corte	-	Performa	Ince,	∞ ≤	
	OVERVIEW	OCUMENTATION	SOFTWARE & TOOLS	BUY/PARAMETRICS	PACKAGE/QUA	LITY TRAINING & SU	JPPORT	
d-mcus/i.i	s://www.nxp mx-applicatio high-perform	ons-proce	essors/i.mx-n	nature-proce	ssors/ap	olications-pr	ocessors-	ssors
	TIONS SUPPORT	ABOUT				2	ALL - Search	1 ACCOUL
DUCTS SOLU Processors and Microc			S32 Automotive Platform ~ 4	\$32V234 Vision and Sensor	Fusion Processor F		ALL - Search	1 ACCOUN
	controllers ~ Arm*-Based Proc S32V234: `	cessors and MCUs ~ Vision Pre	S32 Automotive Platform ~ 3 ocessor for Fr nd Sensor Fus	ront and Sur	round Vie	amily	ALL - Search Fotow	I ACCOU
	controllers ~ Arm*-Based Proc S32V234: `	cessors and MCUs ~ Vision Pre	ocessor for Fr nd Sensor Fus	ront and Sur sion Applicat	round Vie	amily	ALL - Search Follow TRAINING & SUPP	⊠ <
	S32V234: Machine L	vision Pro	ocessor for Fr nd Sensor Fus	ront and Sur sion Applicat	round Vie tions RAMETRICS	<sup>amily</sup> ew Camera,	Follow	⊠ <

Source: <u>https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/s32-automotive-platform/vision-processor-for-front-and-surround-view-camera-machine-learning-and-sensor-fusion-applications:S32V234</u>

<sup>&</sup>lt;sup>11</sup> A non-exhaustive list of additional accused products includes the i.MX 7 series, i.MX 8 series, i.MX Mature series, QorIQ Layerscape series, i.MX534, i.MX535, i.MX537, i.MX8M, and i.MX 8QuadPlus families of products that include advanced on-chip service capabilities.

Feature	i.MX 8QuadMax	i.MX 8QuadPlus
ARM <sup>e</sup> Core	2 x ARM Cortex®-A72	1 x Cortex-A72
ARM Core	4 x Cortex-A53	4 x Cortex-A53
ARM Core	2 x Cortex-M4F	2 x Cortex-M4F

Source: fact sheet downloaded from https://www.nxp.com/docs/en/fact-sheet/IMX8FAMFS.pdf

113. Qualcomm made, had made, used, imported, provided, supplied, distributed, sold,

and/or offered for sale products and/or systems including, for example, its Snapdragon 410E and

Snapdragon 650 families of products that include advanced on-chip service capabilities

("accused products")<sup>12</sup>:

Designed to meet the demanding requirements of embedded computing applications with its high performance, energy efficiency, multimedia features, integrated connectivity and long-term support, the Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 410E embedded platform is an ideal platform for the Internet of Things.

### Source: https://www.qualcomm.com/products/apq8016e

CPU

CPU Clock Speed: Up to 1.2 GHz CPU Cores: Quad-core CPU, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit, 32-bit

Source: <a href="https://www.qualcomm.com/products/apq8016e">https://www.qualcomm.com/products/apq8016e</a>

<sup>&</sup>lt;sup>12</sup> A non-exhaustive list of additional accused products includes the Snapdragon 400 tier (including Snapdragon 439 (SDM439), Snapdragon 450, Snapdragon 427 (MSM8920), and Snapdragon 435 (MSM8940)), MSM8956, the Snapdragon 600 tier (including Snapdragon 652 (MSM8976), and Snapdragon 653 (MSM8976 Pro)) families of products that include advanced on-chip service capabilities.

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 92 of 109



The Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> 650 mobile platform supports high-quality, efficient performance, multimedia, gaming and connectivity, thanks to its powerful 64-bit capable hexa-core CPUs, integrated Qualcomm<sup>®</sup> Snapdragon<sup>®</sup> X8 LTE with Cat 7 speeds, Qualcomm<sup>®</sup> Adreno<sup>®</sup> 510 GPU, and support for 4K Ultra HD video.

Source: https://www.qualcomm.com/products/snapdragon/processors/650

CPU

CPU Clock Speed: Up to 1.8 GHz CPU Cores: Hexa-core CPU, 2x ARM Cortex A72, 4x ARM Cortex A53 CPU Bit Architecture: 64-bit

Source: https://www.qualcomm.com/products/snapdragon/processors/650

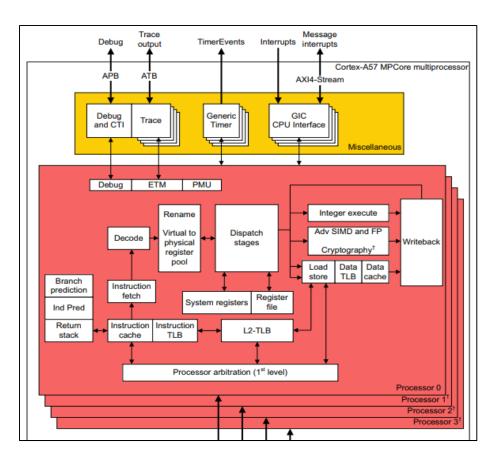
114. By doing so, Defendants have directly infringed (literally and/or under the doctrine of equivalents) at least Claim 1 of the '938 Patent. Defendants' infringement in this regard is ongoing.

115. Defendants have infringed the '938 Patent by making, having made, using,

importing, providing, supplying, distributing, selling or offering for sale integrated circuits

having advanced on-chip service capabilities.

116. The accused products include one or more logic blocks configured to generate one or more system operation signals at one or more system operation clock rates.

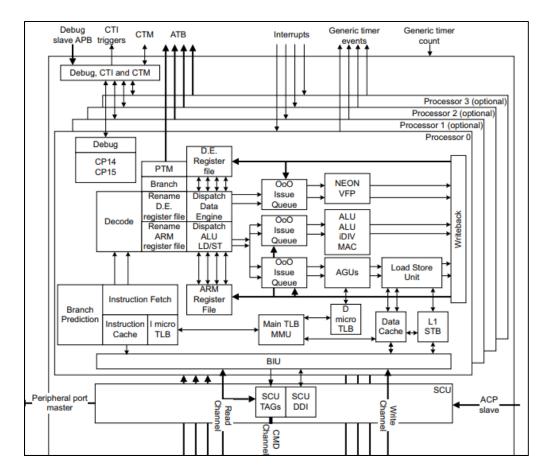


Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C cortex a57 mpcore r1p

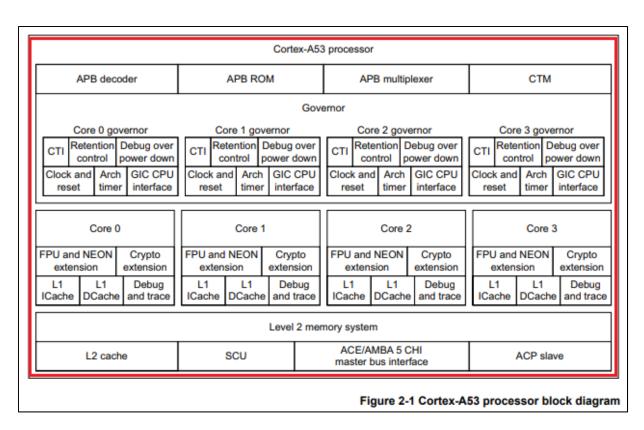
0\_trm.pdf

### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 94 of 109



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

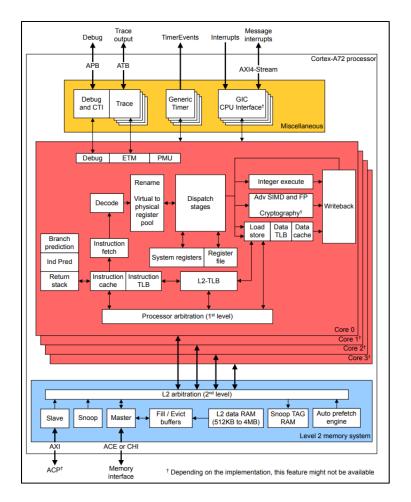
https://static.docs.arm.com/ddi0535/b/DDI0535B cortex a17 r1p0 trm.pdf



Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D\_cortex\_a53\_r0p2\_trm.p

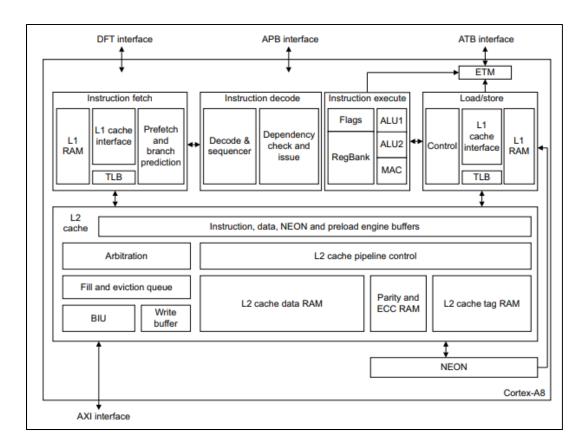
<u>df</u>



Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095 0001 02 en/cortex a72 mpcore trm

\_100095\_0001\_02\_en.pdf



#### Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K cortex a8 r3p2 trm.pdf

117. The accused products include a service processor unit configured to perform one

or more debug operations on one or more of said logic blocks.

#### Embedded Trace Macrocell architecture

The multiprocessor implements the ETMv4 architecture. See the ARM<sup>®</sup> Embedded Trace Macrocell Architecture Specification, ETMv4.

Source: ARM Cortex-A57 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0488c/DDI0488C\_cortex\_a57\_mpcore\_r1p

0\_trm.pdf

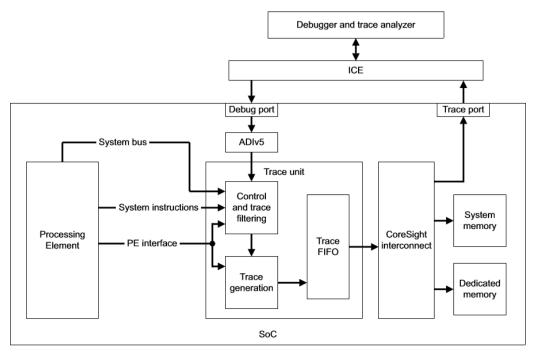
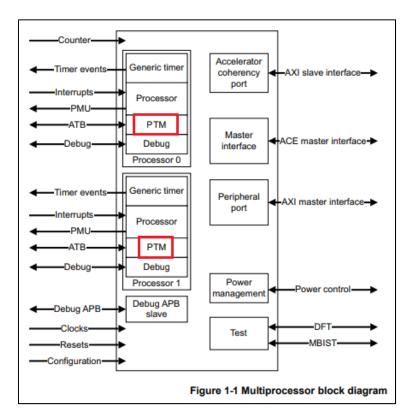


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf



Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

The PTM is a real-time instruction flow trace module that complies with the *Program Flow Trace* (PFTv1.1) architecture. The PTM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5.

For more information see:

- ARM<sup>®</sup> CoreSight<sup>™</sup> Architecture Specification (ARM IHI 0029).
- ARM<sup>®</sup> CoreSight<sup>™</sup> SoC Technical Reference Manual (ARM DDI 0480).

Source: ARM Cortex-A17 MPCore Processor manual downloaded from

https://static.docs.arm.com/ddi0535/b/DDI0535B\_cortex\_a17\_r1p0\_trm.pdf

### Embedded Trace Macrocell architecture

The Cortex-A53 processor implements the ETMv4 architecture. See the ARM<sup>®</sup> ETM<sup>™</sup> Architecture Specification, ETMv4.

Source: ARM Cortex-A53 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0500d/DDI0500D cortex a53 r0p2 trm.p

<u>df</u>

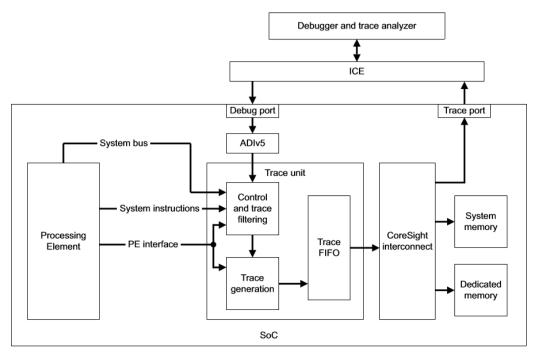


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

#### Embedded Trace Macrocell architecture

The processor implements the ETMv4 architecture. See the *ARM*<sup>®</sup> *Embedded Trace Macrocell Architecture Specification, ETMv4.* 

Source: ARM Cortex-A72 MPCore Processor manual downloaded from

http://infocenter.arm.com/help/topic/com.arm.doc.100095\_0001\_02\_en/cortex\_a72\_mpcore\_trm

100095 0001 02 en.pdf

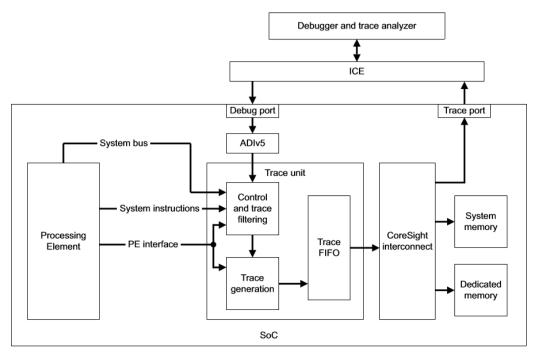


Figure 1-1 Example SoC with a trace unit

Source: ARM Embedded Trace Macrocell Architecture Specification downloaded from

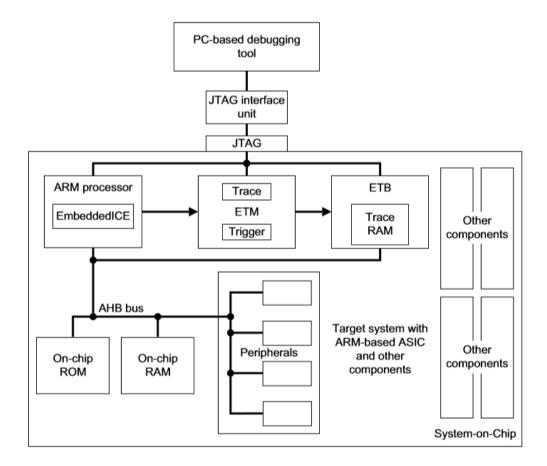
https://static.docs.arm.com/ihi0064/d/IHI0064D\_etm\_v4\_architecture\_spec.pdf

## About the ETM The ETM is a CoreSight<sup>™</sup> component designed for use with the CoreSight Design Kit. CoreSight is the ARM extensible, system-wide debug and trace architecture. The Cortex-A8 processor implements the ETM architecture v3.3.

Source: ARM Cortex-A8 Technical Reference Manual downloaded from

https://static.docs.arm.com/ddi0344/k/DDI0344K\_cortex\_a8\_r3p2\_trm.pdf

## Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 102 of 109



Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification

downloaded from https://static.docs.arm.com/ihi0014/q/IHI0014.pdf

About controlling	tracing		
You control traci	ng in two ways:		
Triggering	Triggering controls when the collection of the trace data occurs. Setting a trigger enables you to focus trace collection around your region of interest.		
Filtering	Filtering controls the type of trace information that is collected. It is important to optimize usage of the trace port bandwidth, especially when a narrow trace port is used. Filtering the trace serves two purposes:		
	<ul> <li>It prevents overflow of the internal FIFO by minimizing the number of data transfers traced. This is especially important when the FIFO is small or the trace port is narrow.</li> </ul>		
	<ul> <li>It limits the amount of trace stored by the <i>trace capture device</i> (TCD), for example a TPA or an on-chip trace buffer. This enables more useful information to be stored around the trigger.</li> </ul>		
	You can filter the instruction trace or the data trace as follows:		
	<ul> <li>Filter the instruction trace by enabling and disabling trace generation. This is the TraceEnable function.</li> </ul>		
	<ul> <li>Filter the data trace by indicating the specific data accesses that must be traced. This is the ViewData function.</li> </ul>		

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from https://static.docs.arm.com/ihi0014/g/IHI0014.pdf

In this specification:

- An ETM is said to be tracing when **TraceEnable** is active and no condition exists that prohibits tracing. Conditions that prohibit tracing include:
  - The processor is in Debug state.
    - The processor is in a Wait For Interrupt (WFI) or Wait For Event (WFE) condition. See Wait For Interrupt and Wait For Event on page 4-251.

Source: ARM Embedded Trace Macrocell ETMv1.0 to ETMv3.5 Architecture Specification downloaded from <a href="https://static.docs.arm.com/ihi0014/q/IHI0014.pdf">https://static.docs.arm.com/ihi0014/q/IHI0014.pdf</a>

118. The service processor unit of the accused products includes a control unit configured to control the service processor unit, a memory, an analysis engine, and a bus interface.

119. The accused products include a multiplicity of probe lines configured to capture and propagate one or more of the one or more system operation signals from said logic blocks to the service processor unit.

120. Defendants have had knowledge of the '938 Patent at least as of the date when they were notified of the filing of this action.

121. On November 23, 2005, the great-great-great-grandparent of the '938 Patent (U.S. Patent No. 6,687,865) was cited by the Examiner during prosecution of U.S. Patent No. 7,567,892, which is assigned to Broadcom Corp. The Examiner in that prosecution explained that the great-great-great-grandparent of the '938 Patent was pertinent because "Dervisoglu et al. (U.S. Patent No. 6,687,865) discloses an on-chip service processor for testing and debugging of integrated circuits." Broadcom employees Geoff Barrett, Simon Christopher Dequin Clemow, and Andrew Jon Dawson, who are listed as inventors on U.S. Patent No. 7,567,892, Robert

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 104 of 109

Sokohl, Jeffrey S. Weaver, and others involved in the prosecution of the patent, have had knowledge of the '938 Patent well before this suit was filed.

122. On March 6, 2006, the great-great grandparent of the '938 Patent (U.S. Patent No. 6,687,865) was cited in an IDS during prosecution of U.S. Patent No. 7,533,315, which is assigned to MediaTek Inc. During that same prosecution, the Examiner also cited the great grandparent of the '938 Patent (U.S. Patent No. 7,080,301) on June 18, 2008. MediaTek employees I-Chieh Han and You-Ming Chiu, who are listed as inventors on U.S. Patent No. 7,533,315, Daniel R. McClure, and others involved in the prosecution of the patent, have had knowledge of the '938 Patent well before this suit was filed.

123. American Patents has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants are liable to American Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

124. American Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '938 Patent.

#### ADDITIONAL ALLEGATIONS REGARDING INDIRECT INFRINGEMENT

125. Defendants have also indirectly infringed the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent by inducing others to directly infringe the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent. Defendants have induced the end-users, its customers, to directly infringe (literally and/or under the doctrine of equivalents) the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent by using the accused products. Defendants took active steps, directly and/or through contractual relationships with others, with the specific

104

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 105 of 109

intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, Claim 5 of the '001 Patent, Claim 7 of the '371 Patent, Claim 1 of the '716 Patent, and Claim 1 of the '938 Patent. Such steps by Defendants included, among other things, advising or directing customers and end-users to use the accused products in an infringing manner; advertising and promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner. Defendants are performing these steps, which constitute induced infringement, with the knowledge of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent and with the knowledge that the induced acts constitute infringement. Defendants were and are aware that the normal and customary use of the accused products by Defendants' customers would infringe the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent. Defendants' inducement is ongoing.

126. Defendants have also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to directly infringe (literally and/or under the doctrine of equivalents) the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent by importing, selling or offering to sell the accused products. Defendants took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, Claim 5 of the '001 Patent, Claim 7 of the '371 Patent, Claim 1 of the '716 Patent, and Claim 1 of the '938 Patent. Such steps by Defendants included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing that such importation or sale would occur; and directing, facilitating, or influencing its

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 106 of 109

affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its behalf, to import, sell, or offer to sell the accused products in an infringing manner. Defendants performed these steps, which constitute induced infringement, with the knowledge of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent and with the knowledge that the induced acts would constitute infringement. Defendants performed such steps in order to profit from the eventual sale of the accused products in the United States. Defendants' inducement is ongoing.

127. Defendants have also indirectly infringed by contributing to the infringement of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent. Defendants have contributed to the direct infringement of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent by the end-user of the accused products. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent, including, for example, Claim 5 of the '001 Patent, Claim 7 of the '371 Patent, Claim 1 of the '716 Patent, and Claim 1 of the '938 Patent. The special features include advanced on-chip service capabilities in a manner that infringes the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent. The special features constitute a material part of the invention of one or more of the claims of the '001 Patent, the '371 Patent, the '716 Patent and are not staple articles of commerce suitable for substantial non-infringing use. Defendants' contributory infringement is ongoing.

128. Furthermore, Defendants have a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of American Patents' patent rights.

106

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 107 of 109

129. Defendants' actions are at least objectively reckless as to the risk of infringing valid patents and this objective risk was either known or should have been known by Defendants.

130. Defendants' direct and indirect infringement of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent is, has been, and continues to be willful, intentional, deliberate, and/or in conscious disregard of American Patents' rights under the patents.

131. American Patents has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants are liable to American Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

#### JURY DEMAND

American Patents hereby requests a trial by jury on all issues so triable by right.

#### PRAYER FOR RELIEF

American Patents requests that the Court find in its favor and against Defendants, and that the Court grant American Patents the following relief:

a. Judgment that one or more claims of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent have been infringed, either literally and/or under the doctrine of equivalents, by Defendants and/or all others acting in concert therewith;

b. A permanent injunction enjoining Defendants and their officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the '001 Patent, the '371 Patent, the '716 Patent, and the '938 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the '001 Patent, the '371 Patent, the '716 Patent; and the '938 Patent;

e. Judgment that Defendants account for and pay to American Patents all damages to

107

#### Case 6:18-cv-00339-ADA Document 1 Filed 11/14/18 Page 108 of 109

and costs incurred by American Patents because of Defendants' infringing activities and other conduct complained of herein, including an award of all increased damages to which American Patents is entitled under 35 U.S.C. § 284;

f. That American Patents be granted pre-judgment and post-judgment interest on the damages caused by Defendants' infringing activities and other conduct complained of herein;

g. That this Court declare this an exceptional case and award American Patents its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285; and

h. That American Patents be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: November 14, 2018

Respectfully submitted,

<u>/s/ Stafford Davis</u> Stafford Davis State Bar No. 24054605 sdavis@stafforddavisfirm.com Catherine Bartles (*not yet admitted*) Texas Bar No. 24104849 cbartles@stafforddavisfirm.com THE STAFFORD DAVIS FIRM The People's Petroleum Building 102 North College Avenue, 13th Floor Tyler, Texas 75702 (903) 593-7000 (903) 705-7369 fax

Matthew J. Antonelli (*not yet admitted*) Texas Bar No. 24068432 matt@ahtlawfirm.com Zachariah S. Harrington (*not yet admitted*) Texas Bar No. 24057886 zac@ahtlawfirm.com Larry D. Thompson, Jr. (*not yet admitted*) Texas Bar No. 24051428 larry@ahtlawfirm.com Christopher Ryan Pinckney (*not yet admitted*) Texas Bar No. 24067819 ryan@ahtlawfirm.com Michael D. Ellis Texas Bar No. 24081586 michael@ahtlawfirm.com

ANTONELLI, HARRINGTON & THOMPSON LLP 4306 Yoakum Blvd., Ste. 450 Houston, TX 77006 (713) 581-3000

Attorneys for American Patents LLC