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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALTAIR LOGIX LLC, Plaintiff, v. **ACER AMERICA CORPORATION,** Defendant.	PATENT Case No. _______________ **ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT AGAINST ACER AMERICA CORPORATION** **DEMAND FOR JURY TRIAL**

Plaintiff Altair Logix LLC files this Original Complaint for Patent Infringement against Acer America Corporation, and would respectfully show the Court as follows:

I. THE PARTIES

1. Plaintiff Altair Logix LLC ("Altair Logix" or "Plaintiff") is a Texas limited liability company with its principal place of business at 15922 Eldorado Pkwy, Suite 500 #1513, Frisco, TX 75035.

2. On information and belief, Defendant Acer America Corporation ("Defendant") is a corporation organized and existing under the laws of California, with a place of business at 333 W. San Carlos St., Ste 1500, San Jose, CA 95110. Defendant has a registered agent at CT Corporation System, 818 West Seventh Street, Suite 930, Los Angeles, CA 90017.

II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the California Long-Arm Statute, due at least to its business in this forum, including at least a portion of the infringements alleged herein. Furthermore, Defendant is subject to this Court's specific and general personal jurisdiction because Defendant is a California corporation.

5. Without limitation, on information and belief, within this State and this District, Defendant has used the patented inventions thereby committing, and continuing to commit, acts of patent infringement alleged herein. In addition, on information and belief, Defendant has derived revenues from its infringing acts occurring within California and the Northern District of California. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in California and the Northern District of California. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within California and the Northern District of California. Defendant has committed such purposeful acts and/or transactions in California and the Northern District of California such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, Defendant is incorporated in California, and it has a place of business within this District.

On information and belief, from and within this District Defendant has committed at least a portion of the infringements at issue in this case.

7. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

III. COUNT I
(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,289,434)

8. Plaintiff incorporates the above paragraphs herein by reference.

9. On September 11, 2001, United States Patent No. 6,289,434 ("the '434 Patent") was duly and legally issued by the United States Patent and Trademark Office. The application leading to the '434 patent was filed on February 27, 1998. (Ex. A at cover).

10. The '434 Patent is titled "Apparatus and Method of Implementing Systems on Silicon Using Dynamic-Adaptive Run-Time Reconfigurable Circuits for Processing Multiple, Independent Data and Control Streams of Varying Rates." A true and correct copy of the '434 Patent is attached hereto as Exhibit A and incorporated herein by reference.

11. Plaintiff is the assignee of all right, title and interest in the '434 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the '434 Patent. Accordingly, Plaintiff possesses the exclusive right and standing to prosecute the present action for infringement of the '434 Patent by Defendant.

12. The invention in the '434 Patent relates to the field of runtime reconfigurable dynamic-adaptive digital circuits which can implement a myriad of digital processing functions related to systems control, digital signal processing, communications, image processing, speech and voice recognition or synthesis, three-dimensional graphics rendering, and video processing. (Ex. A at col. 1:32-38). The object of the invention is to provide a new method and apparatus for implementing systems on silicon or other chip material which will enable the user a means for

achieving the performance of fixed-function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:1).

13. The most common method of implementing various functions on an integrated circuit is by specifically designing the function or functions to be performed by placing on silicon an interconnected group of digital circuits in a non-modifiable manner (hard-wired or fixed function implementation). (*Id.* at col. 1:42-47). These circuits are designed to provide the fastest possible operation of the circuit in the least amount of silicon area. (*Id.* at col. 1:47-49). In general, these circuits are made up of an interconnection of various amounts of random-access memory and logic circuits. (*Id.* at col. 1:49-51). Complex systems on silicon are broken up into separate blocks and each block is designed separately to only perform the function that it was intended to do. (*Id.* at col. 1:51-54). Each block has to be individually tested and validated, and then the whole system has to be tested to make sure that the constituent parts work together. (*Id.* at col. 1:54-56). This process is becoming increasingly complex as we move into future generations of single-chip system implementations. (*Id.* at col. 1:57-59). Systems implemented in this way generally tend to be the highest performing systems since each block in the system has been individually tuned to provide the expected level of performance. (*Id.* at col. 1:59-62). This method of implementation may be the smallest (cheapest in terms of silicon area) method when compared to three other distinct ways of implementing such systems. (*Id.* at col. 1:62-65). Each of the other three have their problems and generally do not tend to be the most cost-effective solution. (*Id.* at col. 1:65-67).

14. The first way is implemented in software using a microprocessor and associated computing system, which can be used to functionally implement any system. (*Id.* at col. 2:1-2). However, such systems would not be able to deliver real-time performance in a cost-effective manner for the class of applications that was described above. (*Id.* at col. 2:3-5). Their use is

best for modeling the subsequent hard-wired/fixed-function system before considerable design effort is put into the system design. (*Id.* at col. 2:5-8).

15. The second way of implementing such systems is by using an ordinary digital signal processor (DSP). (*Id.* at col. 2:9-10). This class of computing machines is useful for real-time processing of certain speech, audio, video and image processing problems and in certain control functions. (*Id.* at col. 2:10-13). However, they are not cost-effective when it comes to performing certain real time tasks which do not have a high degree of parallelism in them or tasks that require multiple parallel threads of operation such as three-dimensional graphics. (*Id.* at col. 2:13-17).

16. The third way of implementing such systems is by using field programmable gate arrays (FPGA). (*Id.* at col. 2:18-19). These devices are made up of a two-dimensional array of fine grained logic and storage elements which can be connected together in the field by downloading a configuration stream which essentially routes signals between these elements. (*Id.* at col. 2:19-23). This routing of the data is performed by pass-transistor logic. (*Id.* at col. 2:24-25). FPGAs are by far the most flexible of the three methods mentioned. (*Id.* at col. 2:25-26). The problem with trying to implement complex real-time systems with FPGAs is that although there is a greater flexibility for optimizing the silicon usage in such devices, the designer has to trade it off for increase in cost and decrease in performance. (*Id.* at col. 2:26-30). The performance may (in some cases) be increased considerably at a significant cost, but still would not match the performance of hard-wired fixed function devices. (*Id.* at col. 2:30-33).

17. These three ways do not reduce the cost or increase the performance over fixed-function systems. (*Id.* at col. 2:35-37). In terms of performance, fixed-function systems still outperform the three ways for the same cost. (*Id.* at col. 2:37-39).

18. The three systems can theoretically reduce cost by removing redundancy from the system. (*Id.* at col. 2:40-41). Redundancy is removed by re-using computational blocks and memory. (*Id.* at col. 2:41-42). The only problem is that these systems themselves are increasingly complex, and therefore, their computational density when compared with fixed-function devices is very high. (*Id.* at col. 2:42-45).

19. Most systems on silicon are built up of complex blocks of functions that have varying data bandwidth and computational requirements. (*Id.* at col. 2:46-48). As data and control information moves through the system, the processing bandwidth varies enormously. (*Id.* at col. 2:48-50). Regardless of the fact that the bandwidth varies, fixed-function systems have logic blocks that exhibit a "temporal redundancy" that can be exploited to drastically reduce the cost of the system. (*Id.* at col. 2:50-53). This is true, because in fixed function implementations all possible functional requirements of the necessary data processing must be implemented on the silicon regardless of the final application of the device or the nature of the data to be processed. (*Id.* at col. 2:53-57). Therefore, if a fixed function device must adaptively process data, then it must commit silicon resources to process all possible flavors of the data. (*Id.* at col. 2:58-60). Furthermore, state-variable storage in all fixed function systems are implemented using area inefficient storage elements such as latches and flip-flops. (*Id.* at col. 2:60-63).

20. The inventors therefore sought to provide a new apparatus for implementing systems on a chip that will enable the user to achieve performance of fixed-function implementation at a lower cost. (*Id.* at col. 2:64 – col. 3:1). The lower cost is achieved by removing redundancy from the system. (*Id.* at col. 3:1-2). The redundancy is removed by re-using groups of computational and storage elements in different configurations. (*Id.* at col. 3:2-4). The cost is further reduced by employing only static or dynamic ram as a means for holding

the state of the system. (*Id.* at col. 3:4-6). This invention provides a way for effectively adapting the configuration of the circuit to varying input data and processing requirements. (*Id.* at col. 3:6-8). All of this reconfiguration can take place dynamically in run-time without any degradation of performance over fixed-function implementations. (*Id.* at col. 3:8-11).

21. The present invention is therefore an apparatus for adaptively dynamically reconfiguring groups of computations and storage elements in run-time to process multiple separate streams of data and control at varying rates. (*Id.* at col. 3:14-18). The '434 patent refers to the aggregate of the dynamically reconfigurable computational and storage elements as a "media processing unit."

22. The claimed apparatus has addressable memory for storing data and a plurality of instructions that can be provided through a plurality of inputs/outputs that is couple to the input/output of a plurality of media processing units. (*Id.* at col. 55:21-30). The media processing unit comprises a multiplier, an arithmetic unit, and arithmetic logic unit and a bit manipulation unit. (*Id.* at col. 55:31 – col. 56:20). The '434 patent provides examples to explain each of the parts of the media processing unit. (*Id.* at col. 16:27-61 (multiplier and adder); *Id.* at col. 16:62 – col. 17:1-9 (arithmetic logic unit); and *Id.* at col. 17:10 – col. 17:43 (bit manipulation unit)). Each of the parts has a data input coupled to the media processing unit input/output, an instruction input coupled to the mediate processing unit input/output, and a data output coupled to the mediate processing unit input/output. (*Id.* at col. 55:31 – col. 56:20). Furthermore, the arithmetic logic unit must be capable of operating concurrently with either the multiplier and arithmetic unit. (*Id.* at col. 56:6-12). And the bit manipulation unit must be capable of operating concurrently with the arithmetic logic unit and at least either the multiplier or the arithmetic unit. (*Id.* at col. 56:13-20). Each of the plurality of media processing units must be capable of performing an operating simultaneously with the performance of other

operations by other media processing units. (*Id.* at col. 56:21-24). An operation comprises the media processing unit receiving an instruction and data from memory, processing the data responsive to the instruction to produce a result, and providing the result to the media processor input/output. (*Id.* at col. 56:26-33).

23. An exemplary block diagram of the claimed systems is shown in Figure 3 of the '434 patent:

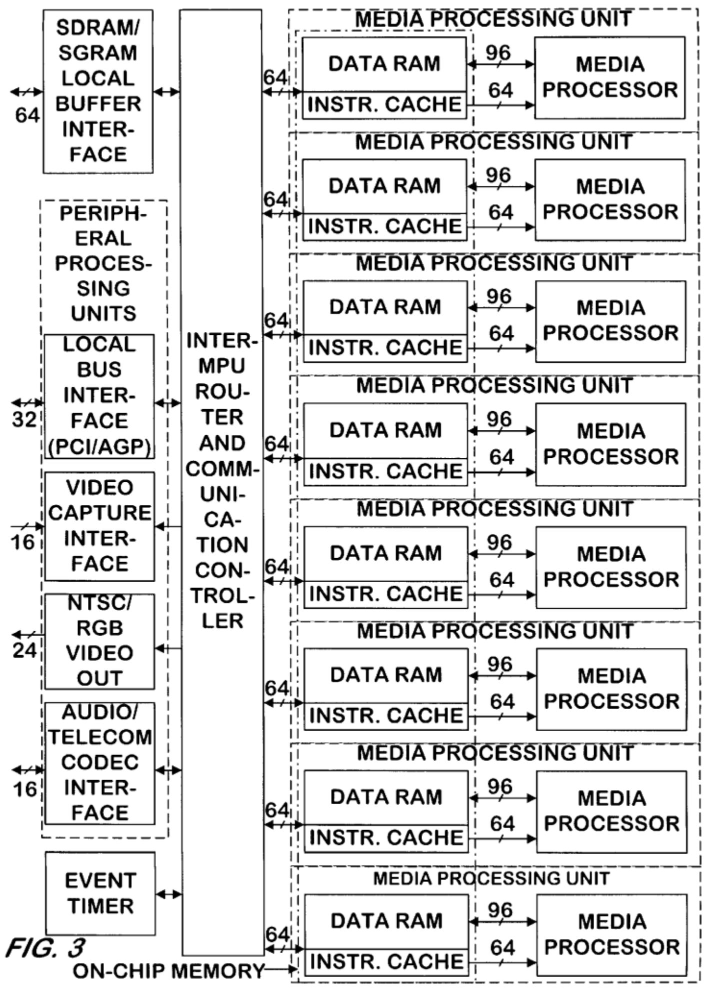

FIG. 3

(*Id.* at Fig. 3). Exemplary architecture and coding for the apparatus is disclosed in the '599 patent. (*E.g.*, *Id.* at col. 16:15 – col. 52:20; Figs. 9 – 106).

24. As further demonstrated by the prosecution history of the '434 patent, the claimed invention in the '434 patent was unconventional. Claim 1 of the '434 patent was an originally

filed claim that issued without any amendment. There was no rejection in the prosecution history contending that claim 1 was anticipated by any prior art.

25. A key element behind the invention is one of reconfigurability and reusability. (*Id.* at col. 13:26-27). Each apparatus is therefore made up of very high-speed core elements that on a pipelined basis can be configured to form a more complex function. (*Id.* at col. 13:27-30). This leads to a lower gate count, thereby giving a smaller die size and ultimately a lower cost. (*Id.* at col. 13:30-31). Since the apparatuses are virtually identical to each other, writing software becomes very easy. (*Id.* at col. 13:32-33). The RISC-like nature of each of the media processing units also allows for a consistent hardware platform for simple operating system and driver development. (*Id.* at col. 13:33-36). Any one of the media processing units can take on a supervisory role and act as a central controller if necessary. (*Id.* at col. 13:36-37). This can be very useful in set top applications where a controlling CPU may not be necessary, further reducing system cost. (*Id.* at col. 13:37-40). The claimed apparatus is therefore an unconventional way of implementing processors that can achieve the performance of fixed-function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:11).

26. **Direct Infringement.** Upon information and belief, Defendant has been directly infringing claims of the '434 patent in California and the Northern District of California, and elsewhere in the United States, by making, using, selling, and offering for sale an apparatus for processing data for media processing that satisfies each and every limitation of at least claim 1, including without limitation the Acer Chromebook R 13 ("Accused Instrumentality"). (*E.g.*, https://www.acer.com/ac/en/US/content/model/NX.GL4AA.003; https://www.mediatek.com/blog/acer-chromebook-r13).

27. The Accused Instrumentality comprises a processing unit (*e.g.*, MediaTek M8173C) which has multiple media processing units (*e.g.*, ARM Quad core Cortex-A53). (*E.g.*,

https://www.acer.com/ac/en/US/content/model/NX.GL4AA.003; https://www.mediatek.com/blog/acer-chromebook-r13; https://www.mediatek.com/products/tablets/mt8173; https://www.mediatek.com/news-events/press-releases/mediatek-to-redefine-the-android-tablet-industry-with-world-first-arm-cortex-a72-based-tablet-soc-mt8173). The Accused Instrumentality comprises an addressable memory (*e.g.*, memory system of the Accused Instrumentality) for storing the data, and a plurality of instructions, and having a plurality of input/outputs, each said input/output for providing and receiving at least one selected from the data and the instructions. As shown below, the Accused Instrumentality comprises a memory system which is coupled to multicore ARM processors through multiple internal inputs/outputs. The memory system provides instructions and stored data for processing and receives processed data.

Specifications

Processor

CPU Cluster 1:
ARM-A72 @ 2.0GHz

CPU Cluster 2:
ARM-A53 @ 1.3GHz

CPU Core:
Quad (4)

CPU Bits:
64-bit

Heterogeneous Multi Processing:
Yes

Memory:
DDR3, LPDDR3 (Single Channel)

Connectivity

Connectivity:
Bluetooth, FM Radio, GNSS: GPS, Glonass, Beidou, Galileo, Wi-Fi

Wi-Fi (IEEE 802.11):
a/b/g/n/ac

Wi-Fi Frequency:
2.4GHz, 5GHz

Camera

Camera ISP:
20MP

Recording Resolution:
1920 x 1080

(*E.g.*, https://www.mediatek.com/products/tablets/mt8173).

The MT8173 is designed with a 64-bit Multi-core big.LITTLE architecture that combines two Cortex-A72 CPUs and two Cortex-A53 CPUs, extending performance and power efficiency further. MT8173 boasts a six-fold increase in performance compared to the MT8125 released in 2013. MT8173 offers up to 2.4GHz performance, supporting OpenCL with the deployment of MediaTek Corepilot® 2.0, and enables heterogeneous computing between the CPU and GPU. The SoC also ensures the ultimate in display clarity and motion fluency on 120Hz display, promising smooth scrolling with crystal clarity as compared to a normal 60Hz display.

"MT8173 highlights the significant shift in how mobile devices, such as Android tablets, are used and, with the combination of ARM's latest technology, we are delivering a platform that answers the growing demand for improved mobile multimedia performance and power usage. By presenting CPU specs that outperform any other device currently on the market, we are bringing PC-like performance to tablet form factor, reinforcing MediaTek's continued commitment to deliver premium technology to everyone across the globe." said Joe Chen, Senior Vice President of MediaTek.

"MediaTek has been a strong adopter of ARM big.LITTLE processing architecture, extending it with CorePilot, to deliver extreme performance, while maintaining power efficiency," said Noel Hurley, General Manager, CPU group, ARM. *"Decisively and quickly incorporating the second-generation of our 64-bit technology into a market-ready product, underscores the partnership between ARM and MediaTek."*

True Heterogeneous 64-bit Multi-Core big.LITTLE architecture up to 2.4GHz

- Features ARM Cortex®-A72 and ARM Cortex®-A53 64-bit CPU
- Big cores and LITTLE cores can run at full speed at the same time for peak performance requirement
- Performance of up to 2.4GHz

Imagination PowerVR GX6250 GPU

- Supports OpenGL ES 3.1, OpenCL for future applications
- Delivers 350Mtri/s and 2.8 Gpix/s performance
- Provides uncompromised user experience for WQXGA display at 60fps

Comprehensive Multimedia Features

- 120Hz mobile display
- Ultra HD 30fps H.264/HEVC(10-bit)/VP9 hardware video playback
- WQXGA display support with TV-grade picture quality enhancement
- HDMI and Miracast support for multi-screen applications
- 20MP camera ISP with video face beautify and LOMO effects

(*E.g.*, https://www.mediatek.com/news-events/press-releases/mediatek-to-redefine-the-android-tablet-industry-with-world-first-arm-cortex-a72-based-tablet-soc-mt8173f).

Overview Documentation

Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	• AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • TrustZone security technology • NEON advanced SIMD • DSP & SIMD extensions • VFPv4 floating point • Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(*E.g.* https://developer.arm.com/products/processors/cortex-a/cortex-a53).

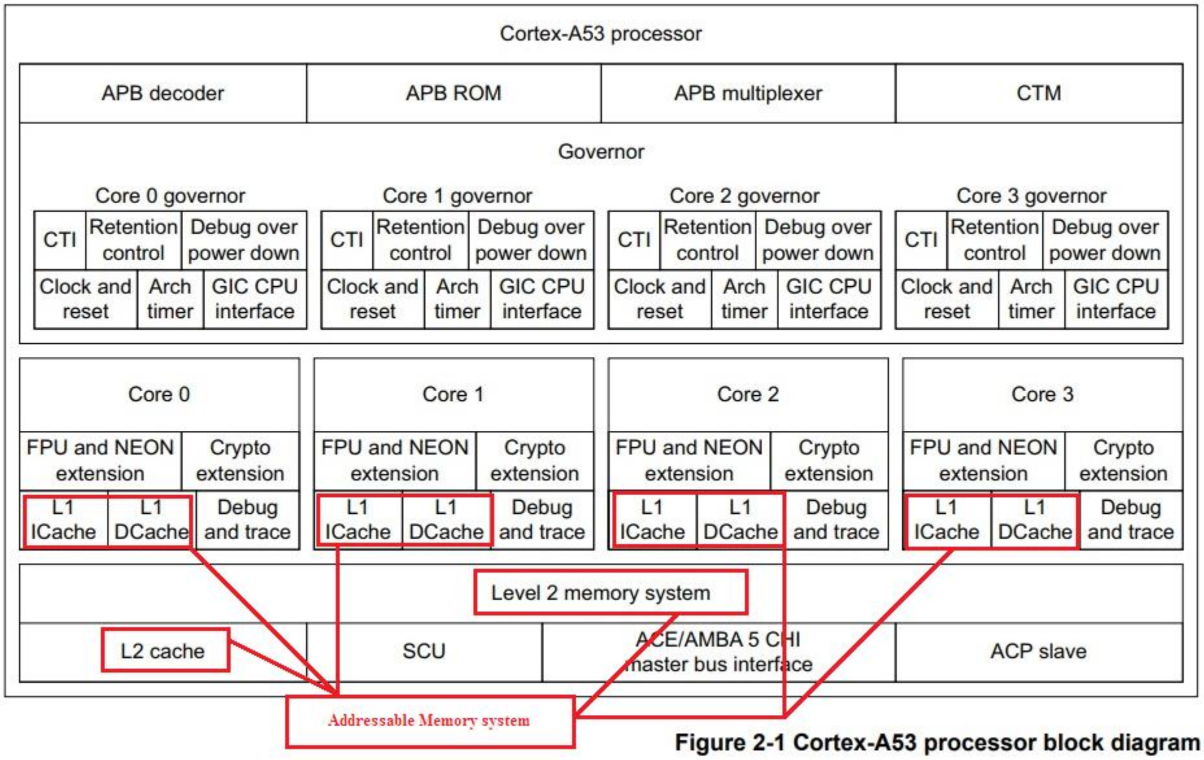

Figure 2-1 Cortex-A53 processor block diagram

(*E.g.* http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

28. The Accused Instrumentality comprises a plurality of media processing units (*e.g.*, ARM cortex-A53 multicore processors), each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs. As shown below, the Accused Instrumentality comprises ARM cortex-A53 multicore processors, each processor comprises a NEON media coprocessor and acts as a media processing unit. The ARM processors are coupled to the memory system. The processors receive instructions and data from the memory system by multiple internal inputs and provides processed data to the memory system by multiple internal outputs.

Specifications

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CPU Cluster 1:
ARM-A72 @ 2.0GHz

CPU Cluster 2:
ARM-A53 @ 1.3GHz

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Quad (4)

CPU Bits:
64-bit

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Yes

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Bluetooth, FM Radio, GNSS: GPS, Glonass, Beidou, Galileo, Wi-Fi

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Camera ISP:
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Debug & Trace	CoreSight DK-A53

(*e.g.*¸ https://developer.arm.com/products/processors/cortex-a/cortex-a53).

Advanced SIMD and floating-point Extension

The optional Advanced SIMD and floating-point Extension implements:

- ARM NEON technology, a media, and signal processing architecture that adds instructions that are targeted at audio, video, 3-D graphics, image, and speech processing. Advanced SIMD instructions are available in AArch64 and AArch32 states.

(*e.g.*, http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

L2 memory system

> The Cortex-A53 L2 memory system contains the L2 cache pipeline and all logic required to maintain memory coherence between the cores of the cluster. It has the following features:
>
> - An SCU that connects the cores to the external memory system through the master memory interface. The SCU maintains data cache coherency between the cores and arbitrates L2 requests from the cores.
>
>   When the Cortex-A53 processor is implemented with a single core, it still includes the *Snoop Control Unit* (SCU). See *Implementation options* on page 1-7 for more information.

(*E.g.*, http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

29. The Accused Instrumentality comprises media processors with each processor comprising a multiplier (*e.g.*, an Integer MUL or FP MUL) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises a multiplier which is coupled to the inputs/outputs of the processor. Upon information and belief, the multiplier comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.

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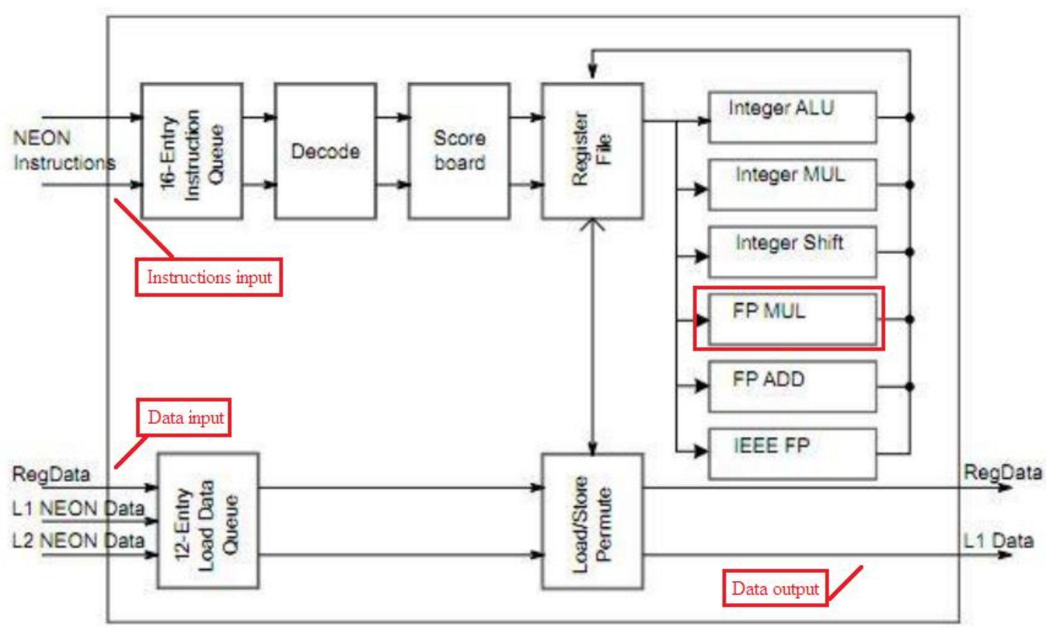
Debug & Trace	CoreSight DK-A53

(*E.g.*, https://developer.arm.com/products/processors/cortex-a/cortex-a53).



(*E.g.*, http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf).

30. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic unit (*e.g.*, an FP ADD) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processor,

each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.

Overview Documentation

Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
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Debug & Trace	CoreSight DK-A53

(*E.g.*, https://developer.arm.com/products/processors/cortex-a/cortex-a53).

Advanced SIMD and floating-point Extension

The optional Advanced SIMD and floating-point Extension implements:

- ARM NEON technology, a media, and signal processing architecture that adds instructions that are targeted at audio, video, 3-D graphics, image, and speech processing. Advanced SIMD instructions are available in AArch64 and AArch32 states.

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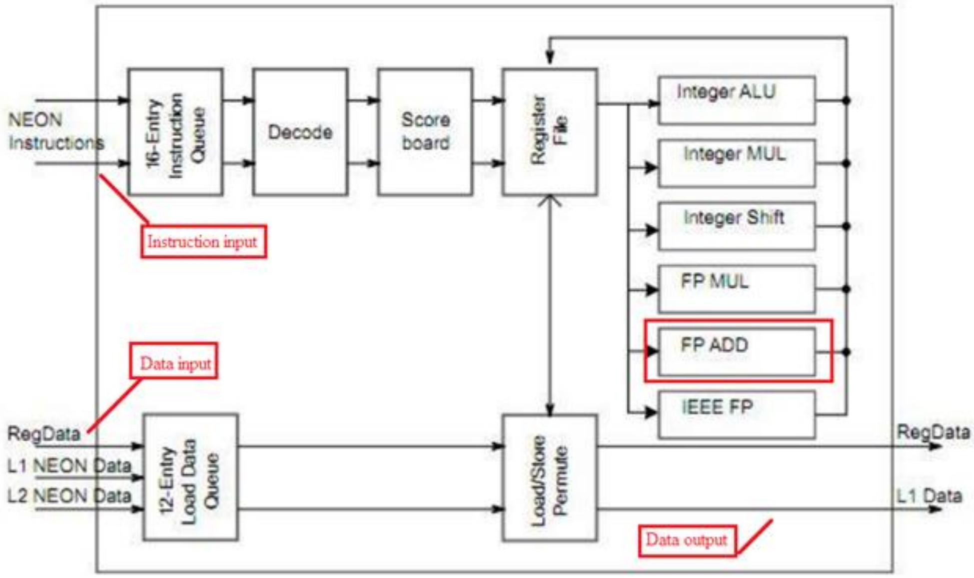
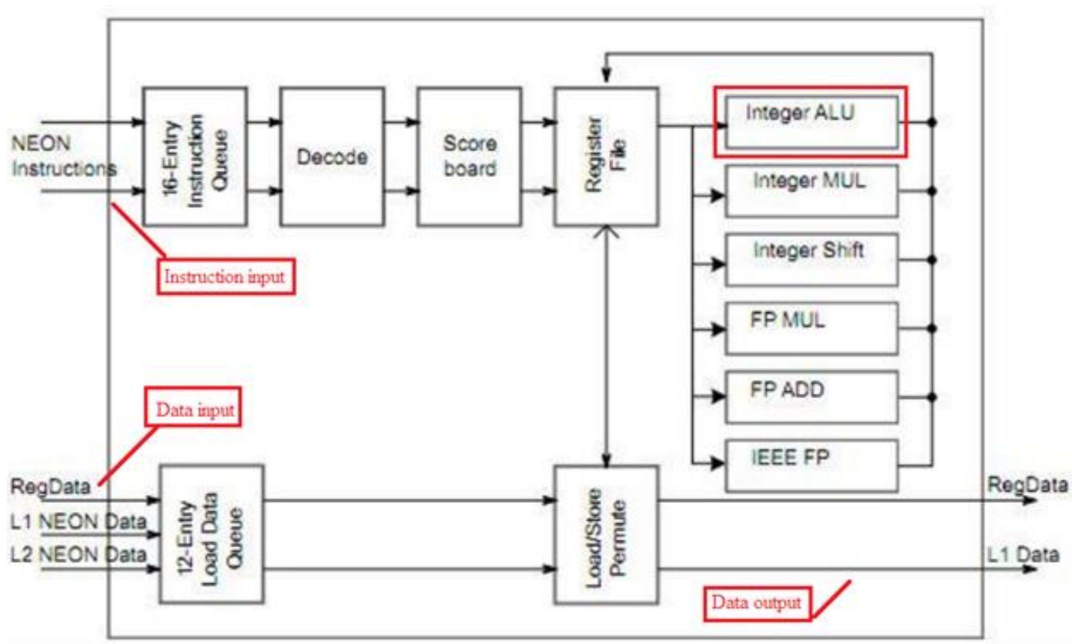


(*E.g.*, http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf).

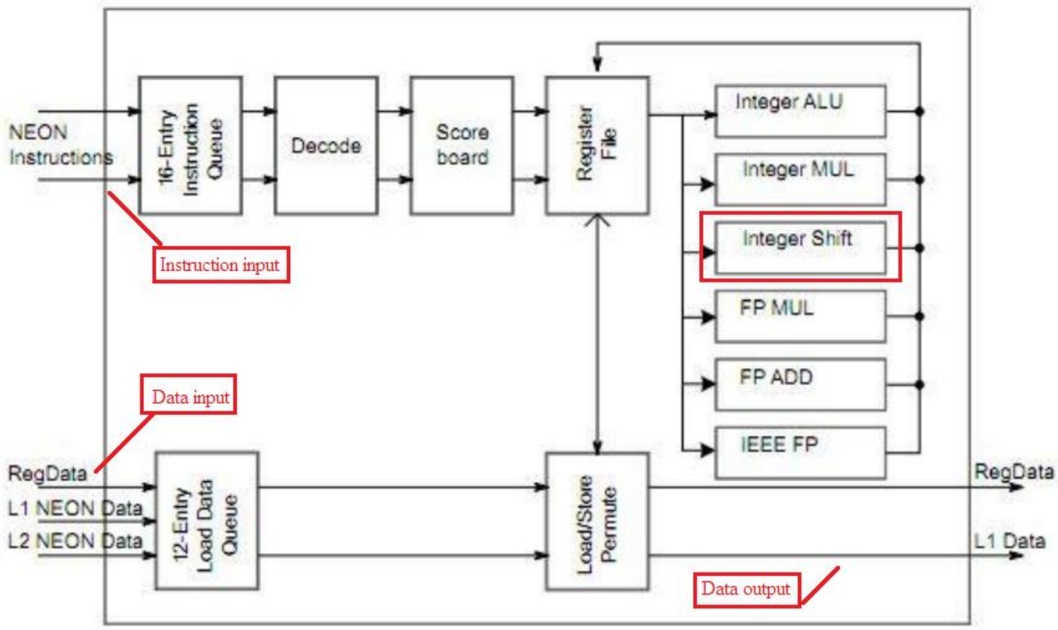
31. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic logic unit (*e.g.*, an ALU) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with at least one selected from the multiplier (*e.g.*, an Integer MUL or FP MUL) and arithmetic unit (*e.g.*, a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic logical unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic logical unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the arithmetic logical unit (*e.g.*, the Integer ALU) is capable of operating concurrently with at least one selected from the multiplier (*e.g.*, the Integer MUL or FP MUL) and arithmetic unit (*e.g.*, the FP ADD).



(*E.g.*, http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf).

32. The Accused Instrumentality comprises media processors with each processor comprising a bit manipulation unit (*e.g.*, an Integer Shift unit) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with the arithmetic logic unit (*e.g.*, an Integer ALU) and at least one selected from the multiplier (*e.g.*, an Integer MUL or FP MUL) and arithmetic unit (*e.g.*, a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A53 multicore processors, each processor comprising a NEON media coprocessor that acts as a media processing unit. The NEON media coprocessor comprises an integer shift unit (*i.e.*, bit manipulation unit) which is coupled to the inputs/outputs of the processor. Upon information and belief, the integer shift unit (*i.e.*, bit manipulation unit) comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the integer shift unit (*i.e.*, bit manipulation unit) is capable of operating concurrently with

the arithmetic logic unit (*e.g.*, the Integer ALU) and at least one selected from the multiplier (*e.g.*, the Integer MUL or FP MUL) and arithmetic unit (*e.g.*, the FP ADD).



(*E.g.*, http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf).

33. The Accused Instrumentality comprises a plurality of media processors (*e.g.*, ARM cortex-A53 multicore processors) for performing at least one operation, simultaneously with the performance of other operations by other media processing units (*e.g.*, other ARM cortex-A53 multicore processors on the same chip).

64-bit ARM Cortex-A72/A53 heterogenous multi-processor with CorePilot

MediaTek MT8173 is a highly integrated SOC which incorporates a 64-bit quad-core, with clusters of ARM Cortex-A53 and high performance Cortex-A72 processors operating at up to 2.0GHz. The Imagination PowerVR GX6250 GPU offers OpenGL ES 3.0. To complement, integrated is a high-end 20MP camera ISP, LPDDR3 at up to 933MHz, Ultra HD 2160p video decoding and WQXGA display capability. The MT8173 helps tablet manufacturers to build very high-performance multimedia tablets with a PC-like browser, close to console-level 3D gaming and cinema class home entertainment experiences.

MT6630

On the MT8173 platform, Wi-Fi and Bluetooth functions are supplied by the MT6630 platform companion chip.

(*E.g.*, https://www.mediatek.com/products/tablets/mt8173).

Specifications

Processor

CPU Cluster 1:
ARM-A72 @ 2.0GHz

CPU Cluster 2:
ARM-A53 @ 1.3GHz

CPU Core:
Quad (4)

CPU Bits:
64-bit

Heterogeneous Multi Processing:
Yes

Memory:
DDR3, LPDDR3 (Single Channel)

Connectivity

Connectivity:
Bluetooth, FM Radio, GNSS: GPS, Glonass, Beidou, Galileo, Wi-Fi

Wi-Fi (IEEE 802.11):
a/b/g/n/ac

Wi-Fi Frequency:
2.4GHz, 5GHz

Camera

Camera ISP:
20MP

Recording Resolution:
1920 x 1080

(*Id.*).

The MT8173 is designed with a 64-bit Multi-core big.LITTLE architecture that combines two Cortex-A72 CPUs and two Cortex-A53 CPUs, extending performance and power efficiency further. MT8173 boasts a six-fold increase in performance compared to the MT8125 released in 2013. MT8173 offers up to 2.4GHz performance, supporting OpenCL with the deployment of MediaTek Corepilot® 2.0, and enables heterogeneous computing between the CPU and GPU. The SoC also ensures the ultimate in display clarity and motion fluency on 120Hz display, promising smooth scrolling with crystal clarity as compared to a normal 60Hz display.

"MT8173 highlights the significant shift in how mobile devices, such as Android tablets, are used and, with the combination of ARM's latest technology, we are delivering a platform that answers the growing demand for improved mobile multimedia performance and power usage. By presenting CPU specs that outperform any other device currently on the market, we are bringing PC-like performance to tablet form factor, reinforcing MediaTek's continued commitment to deliver premium technology to everyone across the globe." said Joe Chen, Senior Vice President of MediaTek.

"MediaTek has been a strong adopter of ARM big.LITTLE processing architecture, extending it with CorePilot, to deliver extreme performance, while maintaining power efficiency," said Noel Hurley, General Manager, CPU group, ARM. *"Decisively and quickly incorporating the second-generation of our 64-bit technology into a market-ready product, underscores the partnership between ARM and MediaTek."*

True Heterogeneous 64-bit Multi-Core big.LITTLE architecture up to 2.4GHz

- Features ARM Cortex®-A72 and ARM Cortex®-A53 64-bit CPU
- Big cores and LITTLE cores can run at full speed at the same time for peak performance requirement
- Performance of up to 2.4GHz

Imagination PowerVR GX6250 GPU

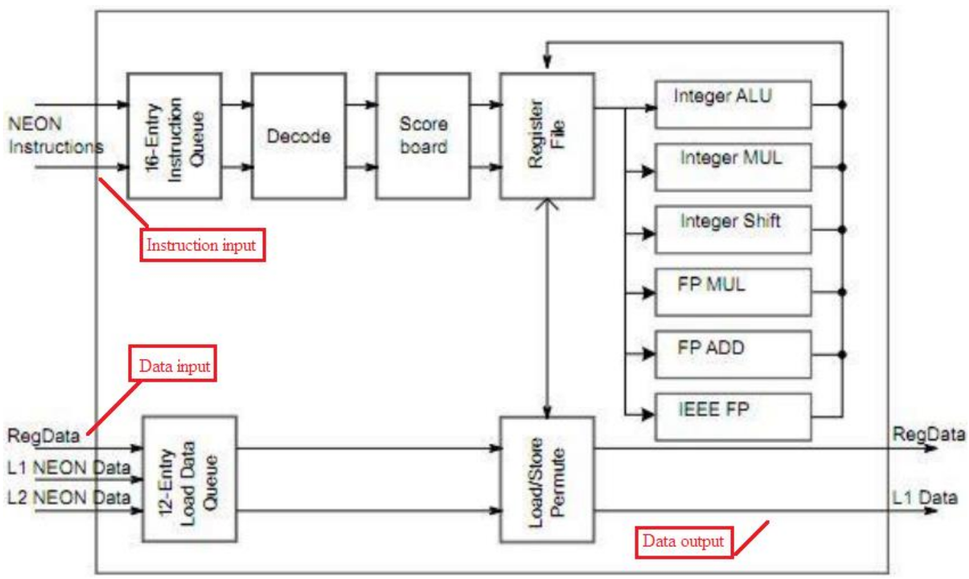
- Supports OpenGL ES 3.1, OpenCL for future applications
- Delivers 350Mtri/s and 2.8 Gpix/s performance
- Provides uncompromised user experience for WQXGA display at 60fps

Comprehensive Multimedia Features

- 120Hz mobile display
- Ultra HD 30fps H.264/HEVC(10-bit)/VP9 hardware video playback
- WQXGA display support with TV-grade picture quality enhancement
- HDMI and Miracast support for multi-screen applications
- 20MP camera ISP with video face beautify and LOMO effects

(*E.g.*, https://www.mediatek.com/news-events/press-releases/mediatek-to-redefine-the-android-tablet-industry-with-world-first-arm-cortex-a72-based-tablet-soc-mt8173).

34. The Accused Instrumentality comprises a plurality of media processors (*e.g.*, ARM cortex-A53 multicore processors), each processor receiving at the media processor input/output an instruction and data from the memory, and processing the data responsive to the instruction received to produce at least one result. As previously shown, each ARM cortex-A53 multicore media processor comprises a NEON media coprocessor which receives instructions and data from memory and processes the data responsive to the instruction received in order to produce a result.



(*E.g.*, http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf).

Specifications

Processor

CPU Cluster 1:
ARM-A72 @ 2.0GHz

CPU Cluster 2:
ARM-A53 @ 1.3GHz

CPU Core:
Quad (4)

CPU Bits:
64-bit

Heterogeneous Multi Processing:
Yes

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DDR3, LPDDR3 (Single Channel)

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Camera

Camera ISP:
20MP

Recording Resolution:
1920 x 1080

(*E.g.*, https://www.mediatek.com/products/tablets/mt8173).

L2 memory system

The Cortex-A53 L2 memory system contains the L2 cache pipeline and all logic required to maintain memory coherence between the cores of the cluster. It has the following features:

- An SCU that connects the cores to the external memory system through the master memory interface. The SCU maintains data cache coherency between the cores and arbitrates L2 requests from the cores.

  When the Cortex-A53 processor is implemented with a single core, it still includes the *Snoop Control Unit* (SCU). See *Implementation options* on page 1-7 for more information.

(*E.g.*, http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

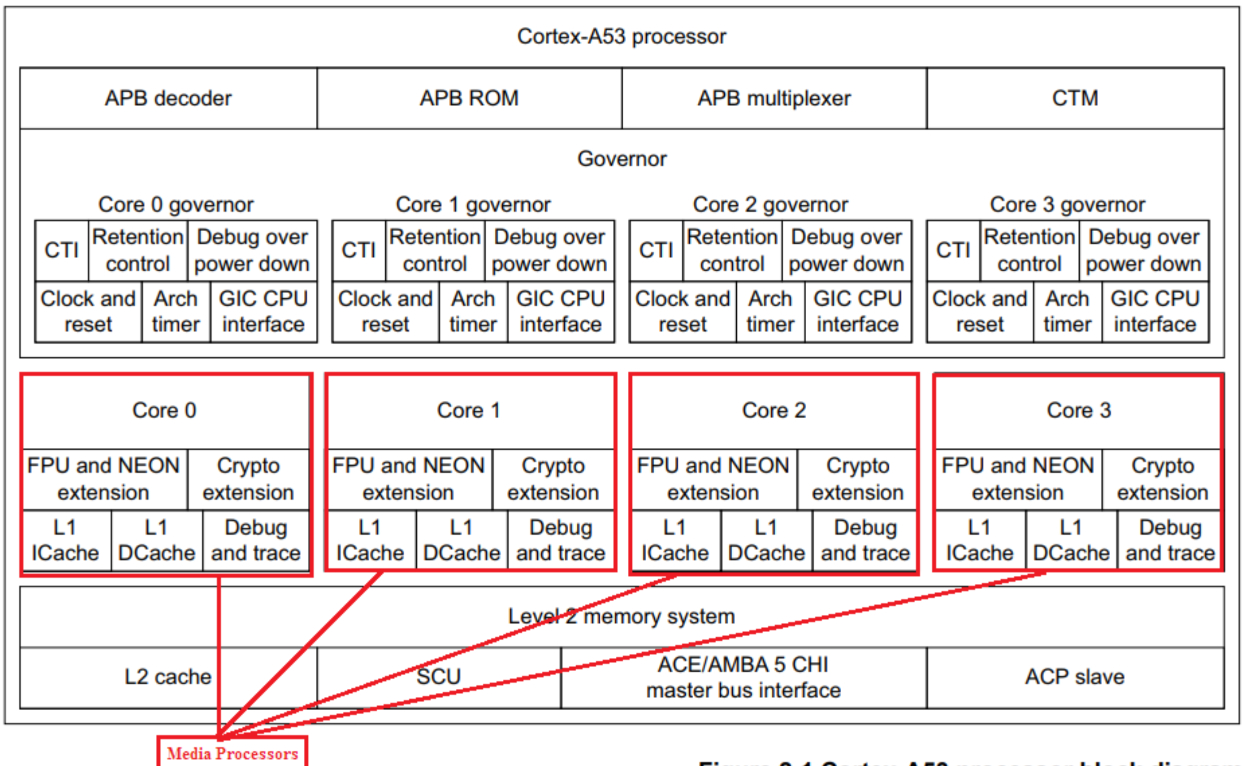

Figure 2-1 Cortex-A53 processor block diagram

(*E.g.*, http://docs-api-peg.northeurope.cloudapp.azure.com/assets/ddi0500/g/DDI0500G_cortex_a53_trm.pdf).

35. The Accused Instrumentality comprises a plurality of media processors (*e.g.*, ARM cortex-A53 multicore processors), each processor providing at least one of the at least one result at the media processor input/output. (*Supra* ¶34).

64-bit ARM Cortex-A72/A53 heterogenous multi-processor with CorePilot

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(*Id.*).

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(*E.g.*, https://www.mediatek.com/news-events/press-releases/mediatek-to-redefine-the-android-tablet-industry-with-world-first-arm-cortex-a72-based-tablet-soc-mt8173).

Overview Documentation

Architecture	Armv8-A
Multicore	1-4x Symmetrical Multiprocessing (SMP) within a single processor cluster, and multiple coherent SMP processor clusters through AMBA 4 technology
ISA Support	• AArch32 for full backward compatibility with Armv7 • AArch64 for 64-bit support and new architectural features • TrustZone security technology • NEON advanced SIMD • DSP & SIMD extensions • VFPv4 floating point • Hardware virtualization support
Debug & Trace	CoreSight DK-A53

(*E.g.*, https://developer.arm.com/products/processors/cortex-a/cortex-a53).

36. Plaintiff has been damaged as a result of Defendant's infringing conduct. Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '434 patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

37. On information and belief, Defendant has had at least constructive notice of the '434 patent by operation of law, and there are no marking requirements that have not been complied with.

IV. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of United States Patent No. 6,289,434 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;

b. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein;

c. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein;

d. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

November 26, 2018

By /s/*Steven A. Nielsen*

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JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

November 26, 2018

By *_/s/Steven A. Nielsen_*

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