Dmitry Kheyfits (SBN 321326)
dkheyfits@kblit.com
KHEYFITS BELENKY LLP
4 Embarcadero Center, Suite 1400
San Francisco, CA 94111
Tel: 415-429-1739
Fax: 415-429-6347

Andrey Belenky (*pro hac vice* to be filed)
abelenky@kblit.com
Hanna G. Cohen (*pro hac vice* to be filed)
hgcohen@kblit.com
KHEYFITS BELENKY LLP
1140 Avenue of the Americas, 9th Floor
New York, NY 10036
Tel: 212-203-5399
Fax: 212-203-6445

Attorneys for Plaintiff
Complex Memory LLC

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

COMPLEX MEMORY LLC,

Plaintiff

v.

BROADCOM CORPORATION,

Defendant

Case No.: 5:18-cv-07530

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Complex Memory LLC ("Complex Memory"), for its Complaint against Defendant Broadcom Corp. ("Broadcom" or "Defendant"), hereby alleges as follows:

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 17330 Preston Road, Suite 200D, Dallas, Texas 75252.

2. On information and belief, Defendant Broadcom is a California corporation with a principal place of business at 1320 Ridder Park Drive, San Jose, CA 95131.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Broadcom of claims of U.S. Patent Nos. 5,890,195; 5,963,481; 6,658,576; 6,968,469; and 7,730,330 ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. Broadcom is subject to personal jurisdiction of this Court because, inter alia, on information and belief, (i) Broadcom is headquartered in the State of California, (ii) Broadcom maintains office locations in the State of California; (iii) Broadcom is registered to transact business in the State of California; and (iv) Broadcom has committed and continues to commit acts of patent infringement in the State of California, including by making, using, offering to sell, and/or selling accused products and services in California, and/or importing the Accused Products into California.

6. Venue is proper as to Broadcom in this district because, inter alia, on information and belief, Broadcom is headquartered in, and maintains a regular and established place of business, in this judicial district, and Broadcom has committed and continues to commit acts of

patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district, and/or importing accused products and services into this district.

BACKGROUND

7. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM". A copy of the '195 Patent is attached as Exhibit A.

8. G.R. Mohan Rao invented the technology claimed in the '195 Patent.

9. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 ("the '481 Patent"), entitled "Embedded Enhanced DRAM, And Associated Method." A copy of the '481 Patent is attached as Exhibit B.

10. Michael Alwais and Michael Peters invented the technology claimed in the '481 Patent.

11. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 ("the '576 Patent"), entitled "Energy-Conserving Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction." A copy of the '576 Patent is attached as Exhibit C.

12. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

13. On November 22, 2005, the United States Patent and Trademark Office duly and lawfully issued U.S . Patent No. 6,968,469 ("the '469 Patent"), entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored." A copy of the '469 Patent is

attached as Exhibit D.

14. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '469 Patent.

15. On June 1, 2010, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,730,330 ("the '330 Patent"), entitled "System and Method For Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set." A copy of the '330 Patent is attached as Exhibit E.

16. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '330 Patent.

17. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

18. By letter dated April 26, 2018, Complex Memory notified Broadcom of the existence of the Patents-in-Suit, and of infringement thereof by Broadcom and its customers. Complex Memory's letter identified exemplary infringing Broadcom products and an exemplary infringed claim for each of the Patents-in-Suit.

19. As of the date of this Complaint, Complex Memory has not received any response from Broadcom.

20. Accordingly, Broadcom has received notice of the Patents-in-Suit and of infringement thereof by Broadcom and its customers.

COUNT I: INFRINGEMENT OF THE '195 PATENT

21. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

22. On information and belief, Broadcom has infringed the '195 Patent pursuant to 35

U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9, A15, A57 and other ARM Cortex-A architectures, including the products identified in Attachment A ("Accused Broadcom Products").

23. For example, on information and belief, Broadcom has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. The Accused Broadcom Products include the BCM5871X platform. On information and belief, the BCM5871X platform includes ARM Cortex-A57, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, BCM5871X Series Processors block diagram. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. In performing the method of claim 6, processors in the Accused Broadcom Products receive an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller) or an address channel of a bus. Accused Broadcom Products compare the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When [the cache controller] receives a request from the core, it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." Ex. 3, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.2 Cache controller. When a match between the received address and a matching address stored in one of the latches occurred, the Accused Broadcom Products perform the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match, known as a hit, and the line is marked valid, then the

read or write occurs the cache memory." *Id*. When a match between the received address and an address stored in one of the latches does not occur, the Accused Broadcom Products perform the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "If the address is not found in the L1 cache but is in the L2 cache, then the cache line is loaded into the L1 cache from the L2 cache and the data is returned to the core. . . . If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 cache from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3. Inclusive and exclusive caches. When the match does not occur, the Accused Broadcom Products further store the received address in one of the latches corresponding to the selected register. For example, the Accused Broadcom Products store the received address, such as the tag, corresponding to the register being accessed, in the cache memory system latches, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches. *See, e.g.*, Ex. 2, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1 Cache terminology. The Accused Broadcom Products further modify the received address to generate a modified address. For example, the hardware autoprefetcher in the Accused Broadcom Products prefetches data or instructions stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5, ARM Cortex-A57 MPCore Processor Technical Reference Manual, Chapter 7.4 L2 cache prefetcher ("prefetch address = current address + (stride × programmed distance)"). *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher. "[P]refetch address = current address + (stride x programmed distance)." On information and belief, the Accused Broadcom Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The

Accused Broadcom Products further exchange data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "If the address is not in either the L1 or L2 caches, data is loaded into both the L1 and L2 caches from external memory and supplied to the core." Ex. 4, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 11.1.3 Inclusive and exclusive caches. The Accused Broadcom Products then store the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stores the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way register latches.

24. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

25. On information and belief, Broadcom's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

COUNT II: INFRINGEMENT OF THE '481 PATENT

26. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

27. On information and belief, Broadcom has infringed the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States devices that interface with DDRxL and/or DDR3/4 memories, including the Accused Broadcom Products identified in Attachment A.

28. For example, on information and belief, Broadcom has infringed at least claim 16 of the '481 Patent by performing a method of accessing data. Specifically, on information and belief, the Accused Broadcom Products access DDR3/3L/4 memory. See, e.g., Ex. 1,

BCM5871X datasheet ("The memory system supports the latest DDR4 memories in addition to DDR3 and DDR3L."). DDR3 memory accessed by Broadcom products is a memory system comprising multiple banks with multiple rows. *See, e.g.*, Ex. 8, DDR3 Standard, JEDEC JSD79-3D at p. 18 ("The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM"). The Accused Broadcom Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id*. ("Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" on page 15 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register."). On information and belief, in DDR3 memory accessed by Broadcom products, the memory locations of the first memory row are disposed upon a substrate. The Accused Broadcom Products access the data stored at the memory locations identified in the first access request. *Id*. While the data stored at the memory locations identified by the first access request is being accessed, the Accused Broadcom Products generate a second access request for accessing data stored at memory locations of a second memory row. *See id.* at p. 55 ("… where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters."). In DDR3 memory accessed by the Accused Broadcom Products, the memory locations of the second memory row are also

disposed upon the substrate at which the memory locations of the first memory row are disposed. *See id.* at pp. 3-4. The Accused Broadcom Products also access the data stored at the memory locations identified in the second access request. *Id*. at p. 18.

29. On information and belief, Broadcom has induced, and continues to induce, infringement of the ’481 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Broadcom website.

30. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

31. On information and belief, Broadcom’s infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

32. On information and belief, Broadcom knew the ’481 Patent existed, knew of an exemplary infringed claim of the ’481 Patent, and knew of exemplary infringing Broadcom products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’481 Patent.

COUNT III: INFRINGEMENT OF THE ’576 PATENT

33. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

34. On information and belief, Broadcom has infringed, and continues to infringe, the ’576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by

making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A57 and other ARM Cortex-A architectures, including the Accused Broadcom Products identified in Attachment A.

35. For example, on information and belief, Broadcom has infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. For example, on information and belief, the Broadcom BCM 5871X platform includes an SoC based on ARM Cortex-57 architecture. *See* Ex. 1, BCM6871X Series Processors Datasheet ("The BCM5871X series of processors represent a new generation of 64-bit ARM-based SoCs that set a new bar on performance and power efficiency."). "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." Ex. 7, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 15 Power Management. The Accused Broadcom Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. *See* Ex. 9, Broadcom BCM58712 website description ("Advanced power management modes (WoL, WoWLAN, WoActivity)"). If detecting a power-up signal, the Accused Broadcom Products power up to provide a main operation that utilizes main microprocessor circuitry, such as a Cortex-A57 MPCore, and a set of main operating instructions. *Id.* The Accused Broadcom Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, if the Accused Broadcom Products detect a power-down signal, such as a software instruction, they power down main Cortex-A57 processing cores (main microprocessor circuitry) while waiting

for a wakeup signal. *Id*. In the Accused Broadcom Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id*.

36. On information and belief, Broadcom has induced, and continues to induce, infringement of the '576 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Broadcom website.

37. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

38. On information and belief, Broadcom's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

39. On information and belief, Broadcom knew the '576 Patent existed, knew of an exemplary infringed claim of the '576 Patent, and knew of exemplary infringing Broadcom products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '576 Patent.

COUNT IV: INFRINGEMENT OF THE '469 PATENT

40. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

41. On information and belief, Broadcom has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by

making, using, offering to sell, selling in the United States or importing into the United States devices incorporating ARM Cortex-A57 and other ARM Cortex-A architectures, including the Accused Broadcom Products identified in Attachment A.

42. For example, on information and belief, Broadcom infringes at least Claim 14 of the '469 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused Broadcom Products, such as the Broadcom BCM5871X platforms, which are computer systems. On information and belief, the Accused Broadcom Products include a processor, such as the Cortex-A57 MPCore processor or MPCore that boots the device. *See* Ex. 1, BCM6871X Series Processors Datasheet. The Accused Broadcom Products include a first memory accessible by said processor, such as the System SRAM. *See id.* On information and belief, the Accused Broadcom Products also include a second memory accessible only to said processor, wherein said second memory is internal to said processor. For example, Cortex-based processors include memory within L2 cache which is internal to the Cortex MPCore processor, and accessible only to said processor, such as memory that is non-shareable. *See, e.g.*, Ex. 10, ARM Cortex-A57 MPCore Technical Reference Manual, Chapter 2.1.1 Components of the processor ("The main components of the processor are…L2 memory system…"). *See also* Ex. 11, ARM Cortex-A Series Programmer's Guide for ARMv8-A, Chapter 13.3.1 Cacheable and shareable memory attributes. On information and belief, in the Accused Broadcom Products, power to said second memory is controlled separately from power to said processor and to said first memory. *See* Ex. 12, ARM Cortex-A57 MPCore Technical Reference Manual, Chapter 2.4.2 Power domains ("The processor supports the following power domains: … Each core in the device…The L2 cache and Snoop Tag RAMs…A domain for…The L2 control."). *See also* Ex. 13, ARM Cortex-A57 MPCore Processor Technical Reference Manual, Chapter 2.4.3 Power modes. In the Accused Broadcom Products, power is

maintained to the second memory when power is removed from said processor. *See, e.g.,* Ex. 13. In the Accused Broadcom Products, the second memory maintains internal context of the processor when power is removed from said processor. For example, in "dormant" mode, where power is removed from core power domains, the L2 cache RAMs are powered up and retain state. On information and belief, the Accused Broadcom Products also include a third memory external to the processor and accessible only to the processor. For example, the Accused Broadcom Products include a flash memory or ROM including boot code, which is external to the processor, and accessible only to the processor. Id. On information and belief, in the Accused Broadcom Products, the power to the flash memory or ROM is controlled separately from power to the processor, and to the main system memory and to the L2 cache memory. *See id*. In another example, the Accused Broadcom Products include a portion of a flash memory, the access to which is limited by, for example, BroadSAFE/TrustZone functionality, only to the A57 MPCore processor. On information and belief, power to that flash memory, and the portion accessible only by the A57 MPCore processor, is provided separately from the processor, the first memory (the System SRAM), and the second memory (the corresponding L2 cache).

43. On information and belief, Broadcom has induced, and continues to induce, infringement of the '469 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Broadcom website.

44. Upon information and belief, Broadcom has committed the foregoing infringing activities without a license.

45. On information and belief, Broadcom's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

46. On information and belief, Broadcom knew the '469 Patent existed, knew of an exemplary infringed claim of the '469 Patent, and knew of exemplary infringing Broadcom products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '469 Patent.

COUNT V: INFRINGEMENT OF THE '330 PATENT

47. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

48. On information and belief, Broadcom has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States devices based on ARM Cortex-A architecture, including the Accused Broadcom Products identified in Attachment A.

49. For example, on information and belief, Broadcom infringes at least Claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused Broadcom Products include a central processing unit, such as the Cortex-A57 CPU. *See* Ex. 1, BCM5871X Series Processors. On information and belief, CPUs in the Accused Broadcom Products execute the "A32 instruction set," the "T32 instruction set," and the "A64 instruction set." Ex. 14, ARM Cortex-A57 MPCore Processor Technical Reference Manual, Chapter 3.1 About the programmers model. Other Broadcom processors execute ARM and

Thumb instruction sets. On information and belief, the Accused Broadcom Products include one or more registers holding a state, such as the system and control registers. *See, e.g.*, Ex. 13, ARM Cortex-A57 MPCore Processor Technical Reference Manual, Chapter 2.4.3 Power modes. On information and belief, in the Accused Broadcom Products, the CPU is adapted, upon executing a first instruction from the first instruction set (such as an instruction from a program in an A32, T32, or A64 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save the state in a memory without executing any additional instructions from the first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs, such as A64) (*see, e.g.,* Ex. 13 at p. 2-56 ("Before entering Dormant mode, the architectural state of the processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")), and (ii) to initiate an action that may cause the state of the registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which may result in registers having UNKNOWN values). *See, e.g.,* ARM Cortex-A57 MPCore Technical Reference Manual, Chapter 4.2. On information and belief, in the Accused Broadcom Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from the first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). See, e.g., Ex. 13 at p. 2-56 ("To exit from Dormant mode to Run mode, the SoC must perform a full powerup reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the processor exits

the powerup reset sequence, and the architectural state must be restored.").

50. On information and belief, Broadcom has induced, and continues to induce, infringement of the '330 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the Broadcom website.

51. Upon information and belief, Broadcom has committed the foregoing infringing activities without a license.

52. On information and belief, Broadcom's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

53. On information and belief, Broadcom knew the '330 Patent existed, knew of an exemplary infringed claim of the '330 Patent, and knew of exemplary infringing Broadcom products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '330 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Complex Memory prays for the judgment in its favor against Broadcom, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against Broadcom on all counts;

B. Entry of judgment that Broadcom has infringed the Patents-in-Suit;

C. Entry of judgment that Broadcom's infringement of the Patents-in-Suit has been

willful;

D. Award of compensatory damages adequate to compensate Complex Memory for Broadcom's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Declaration and finding that Broadcom's conduct in this case is exceptional under 35 U.S.C. § 285;

F. Award of reasonable attorneys' fees and expenses against Broadcom pursuant to 35 U.S.C. § 285;

G. Award of Complex Memory's costs;

H. Pre-judgment and post-judgment interest on Complex Memory's award; and

I. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff Complex Memory hereby demands trial by jury in this action of all claims so triable.

Dated: December 14, 2018

Respectfully submitted,

/s/ Dmitry Kheyfits

Dmitry Kheyfits (SBN 321326)
dkheyfits@kblit.com
KHEYFITS BELENKY LLP
4 Embarcadero Center, Suite 1400
San Francisco, CA 94111
Tel: 415-429-1739
Fax: 415-429-6347

Andrey Belenky
(*pro hac vice* to be filed)
Hanna G. Cohen
(*pro hac vice* to be filed)
hgcohen@kblit.com
KHEYFITS BELENKY LLP
1140 Avenue of the Americas, 9th Floor

New York, NY 10036
Tel: 212-203-5399
Fax: 212-203-6445

Attorneys for Plaintiff
Complex Memory LLC