IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

DYNAMIC DATA TECHNOLOGIES, LLC, *Plaintiff,* v. NVIDIA CORPORATION, *Defendant*.	Civil Action No. 18-cv-01726-CFC **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Dynamic Data Technologies, LLC ("Dynamic Data") bring this action and make the following allegations of patent infringement relating to U.S. Patent Nos.: 8,189,105 (the "'105 patent"); 8,135,073 (the "'073 patent"); 8,073,054 (the "'054A patent"); 6,774,918 (the "'918 patent"); 8,184,689 (the "'689 patent"); 6,996,177 (the "'177 patent"); 7,010,039 (the "'039 patent"); 8,311,112 (the "'112 patent"); 7,894,529 (the "'529 patent"); 7,542,041 (the "'041 patent"); 7,571,450 (the "'450 patent"); 7,750,979 (the "'979 patent"); 6,421,090 (the "'090 patent"); and 6,782,054 (the "'054B patent") (collectively, the "patents-in-suit"). Defendant NVIDIA Corporation ("NVIDIA" or "Defendant") infringes each of the patents-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq*.

INTRODUCTION

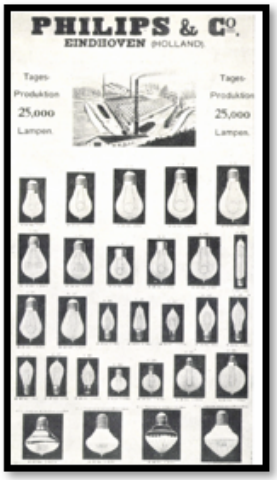
1. Dynamic Data's portfolio of over 1,200 patent assets encompasses core technologies in the field of image and video processing. The patent portfolio held by Dynamic Data is international in scope and includes several hundred European and Chinese patent grants.

2. In addition to ensuring that its intellectual property is appropriately licensed, Dynamic Data has expanded its portfolio of motion estimation and motion compensation patents.

On November 19, 2018, Dynamic Data acquired a further set of 85 patent assets from NXP B.V. relating to motion estimation and motion compensation. Dynamic Data is asserting one of these recently-acquired patents in this First Amended Complaint.[1]

DYNAMIC DATA'S LANDMARK INVENTIONS

3. The groundbreaking inventions in image and video processing taught in the patents-in-suit were pioneered by Philips. Video and image processing were at the heart of Philips' business for over fifty years. In 1891, Philips, then known as Philips & Company, was founded in Eindhoven, Netherlands to manufacture carbon-filament lamps.[2] In the 1920s, Philips began to produce vacuum tubes and small radios, which would augur Philips' later entry into video and audio processing.



N.A. Halbertsma, *The Birth of a Lamp Factory In 1891*, PHILIPS TECHNICAL REVIEW, Vol. 23 at 230, 234 (1961).

4. In 1962, Philips introduced the first audio cassette tape.[3] A year later, Philips launched a small battery-powered audio tape recorder that used a cassette instead of a loose spool.[4]

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[1] *See infra* Count XIV (Asserting U.S. Patent No. 6,782,054).

[2] Gerard O'Regan, A BRIEF HISTORY OF COMPUTING at 99 (2012).

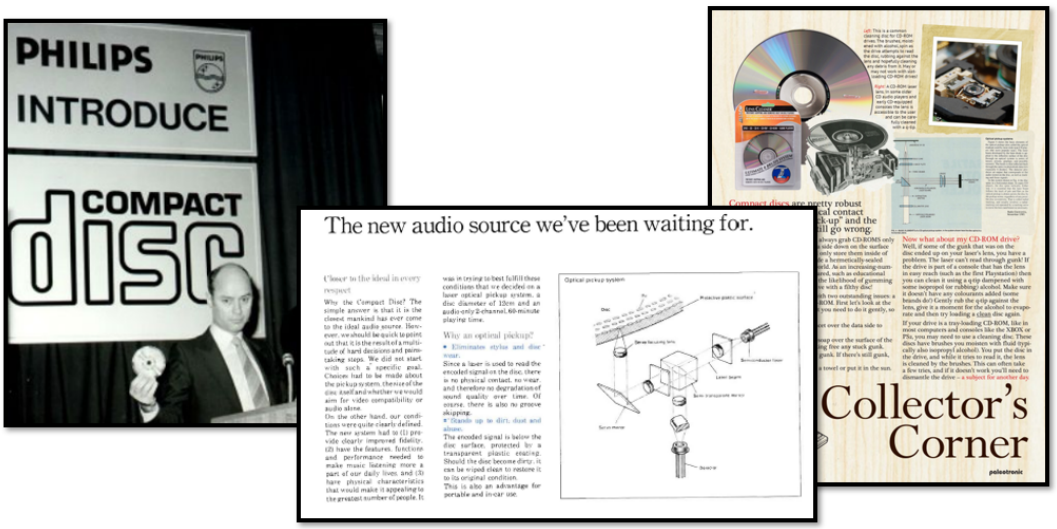
[3] Gerard O'Regan, PILLARS OF COMPUTING: A COMPENDIUM OF SELECT, PIVOTAL TECHNOLOGY FIRMS at 172 (2015) ("Philips invented the compact cassette for audio storage in 1962.")

[4] Anthony Pollard, GRAMOPHONE: THE FIRST 75 YEARS at 231 (1998).

Philips C-cassette was later used as the first mass storage device for early personal computers in the 1970s and 1980s.

THE ROTARIAN MAGAZINE, Vol. 101 No. 6 at 70 (December 1962) (advertisement showing Philips Norelco device which used cassettes for recording audio for transcription); Fred Chandler, *European Mfrs. Bid For Market Share*, BILLBOARD MAGAZINE AT P-6 (April 8, 1967) (image of the Philips EL 3300 battery-operated tape recorder which was released in 1963); Jan Syrjala*, Car Stereo: How Does The Music Sound?,* N.Y. TIMES at 2-M (September 25, 1966) (showing Philips's Norelco Cassette "the Philips device has two tiny reels inside it, with the tape traveling from one to the other").

5. In 1971, Philips demonstrated the world's first videocassette records (VCR). A year later, Philips launched the world's first home video cassette recorder, the N1500. In 1982, Philips teamed with Sony to launch the Compact Disc; this format evolved into the DVD and later Blu-ray, which Philips launched with Sony in 1997 and 2006 respectively.



Hans Peek, Jan Bergmans, Jos Van Haaren, Frank Toolenaar, and Sorin Stan, ORIGINS AND SUCCESSORS OF THE COMPACT DISC: CONTRIBUTIONS OF PHILIPS TO OPTICAL STORAGE at 15 (2009) (showing image of Joop Sinjou of Philips introducing the compact disc in March 1979); Advertisements for Philip's Compact Disc Products (1982).

6. In the late 1990s and early 2000s, Philips pioneered the development of technologies for encoding and decoding of video and audio content. At the time most of the technologies claimed by the patents in Dynamic Data's portfolio were invented, Philips' subsidiary primarily responsible for Philips' work in this field, Philips Semiconductor was the world's sixth largest semiconductor company.[5] The video encoding technologies developed by Philips Semiconductor enable video streaming on set-top boxes, smartphones, popular gaming consoles, Internet-connected computers, and numerous other types of media streaming devices.

7. Philips Semiconductor dedicated significant research and development resources to advancing the technology of video compression and transmission by reducing file sizes and

[5] *Company News; Philips in $1 Billion Deal for VLSI Technology*, THE NEW YORK TIMES (May 4, 1999), *available at*: https://www.nytimes.com/1999/05/04/business/company-news-philips-in-1-billion-deal-for-vlsi-technology.html.

decreasing the processing resources required to transmit the data.[6] Philips Semiconductor was among the first companies aggressively driving innovation in the field of video processing:

> The late 1980s and early 1990s saw the announcement of several complex, programmable VSPs. Important examples include chips from Matsushita, NTT, Philips [Semiconductors], and NEC. All of these processors were high-performance parallel processors architected from the ground up for real-time video signal processing. . . . The Philips VSP-1 and NEC processor were probably the most heavily used of these chips.[7]

8. Starting in the 1960s Philips pioneered the development of audio and video technologies that would establish itself as a leader in the field that would later develop into the audio and video encoding fields. Continuing Philips' pioneering history in these fields, the patents-in-suit disclose cutting-edge video compression and transmission technologies.

DYNAMIC DATA'S PATENT PORTFOLIO

9. Dynamic Data's patent portfolio includes over 1,200 patent assets, with over 470 issued patents granted by patent offices around the world. Dynamic Data owns numerous patents issued by the United States Patent and Trademark Office, including each of the patents-in-suit, The State Intellectual Property Office of the People's Republic of China,[8] the European Patent Office,[9] the German Patent and Trademark Office,[10] the Japan Patent Office,[11] and many other national patent offices.

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[6] HU, YU HEN, PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: ARCHITECTURE, PROGRAMMING, AND APPLICATIONS, at 190 (Dec. 6, 2001) ("Philips Semiconductors developed early dedicated video chips for specialized video processors.").

[7] *Id.* at 191.

[8] *See, e.g.,* CN100504925C; CN100438609C; CN1679052B; CN1333373C; CN1329870C; CN1303818C.

[9] *See, e.g.,* European Patent Nos. EP1032921B1; EP1650978B1; EP1213700B1; EP1520409B1.

[10] *See, e.g.,* German Patent Nos. DE60120762; DE50110537; DE60126151; DE60348978; DE602004049357.

[11] *See, e.g.,* Japanese Patent Nos. JP4583924B2; JP5059855B2; JP5153336B2; JP4637585B2.

10. Philips Semiconductor's pioneering work in the area of video processing and encoding has resulted in various inventions that are fundamental to today's video processing technologies. Dynamic Data is the owner by assignment of over 1,200 of these patent assets, which include over 470 patents issued by patent offices around the world.

11. Highlighting the importance of the patents-in-suit is the fact that the patents-in-suit have been cited by over 470 U.S. and international patents and patent applications by a wide variety of the largest companies operating in the field. For example, the patents-in-suit have been cited by companies such as:

- Samsung Electronics Co., Ltd.[12]
- Qualcomm Inc.[13]
- Google LLC[14]
- Intel Corporation[15]
- Broadcom Corporation[16]
- Microsoft Corporation[17]
- Sony Corporation[18]
- Fujitsu Ltd.[19]
- Panasonic Corporation[20]
- Matsushita Electric Industrial Company Limited[21]

[12] *See, e.g.*, U.S. Patent Nos. 6,930,729; 7,911,537; 7,532,764; 8,605,790; and 8,095,887.
[13] *See, e.g.*, U.S. Patent Nos. 7,840,085; 8,649,437; 8,750,387; 8,918,533; 9,185,439; 9,209,934; 9,281,847; 9,319,448; 9,419,749; 9,843,844; 9,917,874; and 9,877,033.
[14] *See, e.g.*, U.S. Patent No. 8,787,454 and U.S. Patent Appl. No. 10/003,793.
[15] *See, e.g.*, U.S. Patent Nos. 7,554,559; 7,362,377; and 8,462,164.
[16] *See, e.g.*, U.S. Patent Nos. 8,325,273 and 9,377,987.
[17] *See, e.g.*, U.S. Patent Nos. 7,453,939; 7,670,227; 7,408,986; 7,421,129; 7,558,320; and 7,929,599.
[18] *See, e.g.*, U.S. Patent Nos. 7,218,354 and 8,174,615.
[19] *See, e.g.*, U.S. Patent Nos. 7,092,032 and 8,290,308.
[20] *See, e.g.*, U.S. Patent Nos. 8,164,687 and 8,432,495.
[21] *See, e.g.*, U.S. Patent Nos. 7,362,378 and 7,423,961.

THE PARTIES

DYNAMIC DATA TECHNOLOGIES, LLC

12. Dynamic Data Technologies, LLC ("Dynamic Data" or "Plaintiff") is a limited liability company organized under the laws of Delaware.

13. In an effort to obtain compensation for Philips' pioneering work in the fields of video data encoding, decoding, and transmission, Dynamic Data acquired the patents-in-suit along with the several hundred additional issued United States and international Patents.

14. Dynamic Data pursues the reasonable royalties owed for NVIDIA's use of the inventions claimed in Dynamic Data's patent portfolio, which primarily arise from Philips' groundbreaking technology, both here in the United States and throughout the world.

NVIDIA CORPORATION

15. On information and belief, NVIDIA Corporation ("NVIDIA"), is a Delaware corporation with its principal place of business at 2701 San Tomas Expressway, Santa Clara, CA 95050. NVIDIA may be served through its registered agent – Corporation Service Company, 251 Little Falls Drive, Wilmington, DE 19808.

JURISDICTION AND VENUE

16. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

17. Upon information and belief, this Court has personal jurisdiction over NVIDIA in this action because NVIDIA has committed acts within the State of Delaware giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over NVIDIA would not offend traditional notions of fair play and substantial justice. Defendant

NVIDIA, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patents-in-suit. Moreover, NVIDIA actively directs its activities to customers located in the State of Delaware.

18. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Defendant NVIDIA resides in the State of Delaware, upon information and belief, has transacted business in the State of Delaware, and has committed acts of direct and indirect infringement in the State of Delaware.

THE ASSERTED PATENTS

U.S. PATENT NO. 8,189,105

19. U.S. Patent No. 8,189,105 entitled, *Systems and Methods of Motion and Edge Adaptive Processing Including Motion Compensation Features*, was filed on October 17, 2007. The '105 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1258 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '105 Patent. A true and correct copy of the '105 Patent is attached hereto as Exhibit 1.

20. The '105 patent discloses novel systems and methods for processing pixel information based on received motion and edge data.

21. The '105 patent further discloses the use of a blending component (implemented by hardware, software, firmware, combinations thereof, etc.) that implements interpolating intensity of the pixel to equal to the first intensity estimate if motion reliability data is below a threshold.

22. The '105 patent in one embodiment teaches using segmentation to average four contiguous pixels into one averaged pixel segment during motion detection.

23. The ’105 Patent and its underlying patent applications and foreign counterparts have been cited by 46 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’105 Patent and its underlying patent application as relevant prior art:

- Flextronics Ap, LLC
- Qingdao Hisense Electronics Co., Ltd.
- Hon Hai Precision Industry Co., Ltd.
- Intel Corporation
- Sony Corporation
- Fujitsu Corporation
- Himax Media Solutions, Inc.
- Ati Technologies Ulc
- Sharp Kabushiki Kaisha
- Xerox Corporation

U.S. PATENT NO. 8,135,073

24. U.S. Patent No. 8,135,073 (the “’073 patent”) entitled, *Enhancing Video Images Depending On Prior Image Enhancements*, was filed on December 12, 2003, and claims priority to December 19, 2002. The ‘073 patent is subject to a 35 U.S.C. § 154(b) term extension of 1,799 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘073 patent. A true and correct copy of the ‘073 patent is attached hereto as Exhibit 2.

25. The ‘073 patent discloses novel methods and systems for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

26. The inventions disclosed in the ‘073 patent reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

27. Accordingly, the technologies disclosed in the ‘073 patent enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

28. The ‘073 patent discloses a video decoder comprising an input for receiving a video stream containing encoded frame-based video information including an encoded first frame and an encoded second frame.

29. The ‘073 patent discloses a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame.

30. The ‘073 patent discloses a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers the motion vectors for the second frame.

31. The ‘073 patent discloses a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

32. The ‘073 patent and its underlying patent application have been cited by 36 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘073 patent and its underlying patent application as relevant prior art:

- Canon Inc.
- Microsoft Corporation

- International Business Machines Corporation
- Qualcomm Inc.
- Digital Fountain Incorporated
- Samsung Electronics Co., Ltd.
- SK Planet Co. Ltd.

U.S. PATENT NO. 8,073,054

33. U.S. Patent No. 8,073,054 (the "'054A patent") entitled, *Unit For And Method Of Estimating A Current Motion Vector*, was filed on December 12, 2002, and claims priority to January 17, 2002. The '054A patent is subject to a 35 U.S.C. § 154(b) term extension of 1,162 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '054A patent. A true and correct copy of the '054A patent is attached hereto as Exhibit 3.

34. The '054A patent discloses novel methods and apparatuses for estimating a current motion vector for a group of pixels of an image.

35. The inventions disclosed in the '054A patent enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

36. The '054A patent discloses a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

37. The '054A patent discloses a motion estimation unit comprising a match error unit for calculating match errors of respective candidate motion vectors.

38. The '054A patent discloses a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by means of comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by

calculating the further candidate motion vector on basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

39. The '054A patent discloses a motion estimation unit that calculates the further candidate motion vector on basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different.

40. The '054A patent discloses a motion estimation unit that arranges to calculate the further candidate motion vector by means of calculating a difference between the second motion vector and the first motion vector.

41. The '054A patent and its underlying patent application have been cited by 14 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '054A patent and its underlying patent application as relevant prior art:

- Canon Inc.
- Huawei Technologies, Ltd.
- Imagination Technologies Ltd.
- MediaTek Inc.
- Panasonic Corp.
- Samsung Electronics Co., Ltd.
- Siemens Healthcare GmbH
- Tencent Technology (Shenzhen) Co., Ltd.

U.S. PATENT NO. 6,774,918

42. U.S. Patent No. 6,774,918 ("the '918 patent") entitled, *Video Overlay Processor with Reduced Memory And Bus Performance Requirements*, was filed on June 28, 2000. The '918 patent is subject to a 35 U.S.C. § 154(b) term extension of 591 days. Dynamic Data is the owner

by assignment of all right, title, and interest in the '918 patent. A true and correct copy of the '918 patent is attached hereto as Exhibit 4.

43. The '918 patent claims specific methods and systems for providing an overlay such as a cursor in an on-screen display in a consumer electronic device. On-screen display (OSD) data for generating an image on a display device are downloaded to an OSD unit on an integrated circuit.

44. The '918 patent discloses downloading on-screen display (OSD) data for generating an image on a display device.

45. The '918 patent further discloses downloading the on-screen display (OSD) data in segments separated by gaps.

46. The '918 patent further discloses, during a gap in downloading the on-screen display data, downloading an amount of overlay data for generating an overlay on the image generated on a display device.

47. Further, the '918 patent discloses that the overlay data downloaded during a gap comprises a portion of the overlay data.

48. The inventions disclosed in the '918 patent improve the operation and efficiency of computer components because only a portion of the overlay data is downloaded during each burst gap, thus reducing the amount of memory needed to store the overlay data. The inventions disclosed in the '918 patent further eliminate the requirement that on-chip memory be large enough to hold the data needed for an entire overlay. Instead, only one line or a part of one line of the overlay needs to be stored on-chip.

49. The '918 patent claims a technical solution to a problem unique to video processing.

50. The '918 patent has been cited by several United States patents and patent applications as relevant prior art. Specifically, patents issued to Realtek Semiconductor Corp., Samsung Electronics Co., Ltd., and Thomson Licensing SA have all cited the '918 patent as relevant prior art.

U.S. PATENT NO. 8,184,689

51. U.S. Patent No. 8,184,689 (the "'689 patent") entitled, *Method Video Encoding And Decoding Preserving Cache Localities*, was filed on August 7, 2006, and claims priority to August 17, 2005. The '689 patent is subject to a 35 U.S.C. § 154(b) term extension of 948 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '689 patent. A true and correct copy of the '689 patent is attached hereto as Exhibit 5.

52. The '689 patent discloses novel methods and apparatuses for encoding and decoding video data.

53. The inventions disclosed in the '689 patent processing time and power consumption associated with encoding and decoding video stream data is reduced by reducing off-chip memory accesses through using simultaneous encoded/decoded images as a reference image for encoding/decoding at least one of the other simultaneously encoded/decoded images.

54. The '689 patent discloses a method for encoding and decoding a video stream, including a plurality of images in a video processing apparatus having a processing unit coupled to a first memory, further comprising a second memory.

55. The '689 patent discloses a method for encoding and decoding a video stream comprising providing a subset of image data stored in the second memory in the first memory.

56. The '689 patent discloses a method for encoding and decoding a video stream comprising simultaneous encoding/decoding of more than one image of the video stream, by

accessing said subset, wherein the simultaneously encoding/decoding is performed by access sharing to at least one image.

57. The '689 patent and its underlying patent application have been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to Fujitsu Ltd., Qualcomm Inc., Sony Corporation, Sun Patent Trust, and VIXS Systems Incorporated have all cited the '689 patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 6,996,177

1. U.S. Patent No. 6,996,177 (the "'177 patent") entitled, *Motion Estimation*, was filed on July 24, 2000, and claims priority to August 22, 1999. The '177 patent is subject to a 35 U.S.C. § 154(b) term extension of 1,103 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '177 patent. A true and correct copy of the '177 patent is attached hereto as Exhibit 6.

2. The '177 patent claims specific methods and devices for motion estimation and motion-compensated picture signal processing.

3. The '177 patent discloses a motion vector estimation method and device that carries out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors.

4. The '177 patent discloses a motion vector estimation method and device that determines at least a most frequently occurring block-based motion vector.

5. The '177 patent discloses a motion vector estimation method and device that carries out a global motion vector estimation process using at least the most frequently occurring block-based motion vector to obtain a global motion vector.

6. The ‘177 patent discloses a motion vector estimation method and device that applies the global motion vector as a candidate vector to the block-based motion vector estimation process.

7. The inventions disclosed in the ‘177 patent improve the operation of the computer components necessary to the performance of picture signal processing by reducing the load on the central processing unit.

8. The ‘177 patent has been cited by 16 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘177 patent as relevant prior art:

- Qualcomm Incorporated
- LG Electronics
- Microsoft Corporation
- Samsung Electronics Co., Ltd.
- VIXS Systems Incorporated
- General Instrument Corporation

U.S. PATENT NO. 7,010,039

9. U.S. Patent No. 7,010,039 (the “‘039 patent”) entitled, *Motion Estimator for Reduced Halos in MC Up-Conversion*, was filed on May 15, 2001, and claims priority to May 18, 2000. The ‘039 patent is subject to a 35 U.S.C. § 154(b) term extension of 768 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘039 patent. A true and correct copy of the ‘039 patent is attached hereto as Exhibit 7.

10. The ‘039 patent claims specific methods and apparatuses detecting motion at a temporal intermediate position between previous and next images. The inventions disclosed in the ‘039 patent solve a problem wherein an estimator estimating motion between two successive pictures from a video sequence cannot perform well in areas where covering or uncovering occurs.

11. The ‘039 patent solves this problem by carrying out the optimization at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

12. The ‘039 patent discloses a method and apparatus for detecting motion at a temporal intermediate position between previous and next images.

13. The ‘039 patent discloses the use of a criterion function for selecting and optimizing candidate vectors.

14. The ‘039 patent further discloses a criterion function that depends on data from both previous and next images and in which the optimizing is carried out at the temporal intermediate position in non-covering and non-uncovering areas, characterized in that the optimizing is carried out at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

15. The ‘039 patent and its related patents have been cited by 30 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘039 patent family as relevant prior art:

- Qualcomm Incorporated
- Panasonic Corporation
- Samsung Electronics Co., Ltd.
- Matsushita Electric Industrial Co., Ltd.
- Sharp Kabushiki Kaisha
- Integrated Device Technology, Inc.
- Zoran Corporation

U.S. PATENT NO. 8,311,112

58. U.S. Patent No. 8,311,112 (the “’112 patent”) entitled, *System And Method For Video Compression Using Predictive Coding*, was filed on December 31, 2008. The ‘112 patent is subject to a 35 U.S.C. § 154(b) term extension of 847 days. Dynamic Data is the owner by

assignment of all right, title, and interest in the '112 patent. A true and correct copy of the '112 patent is attached hereto as Exhibit 8.

59. The '112 patent discloses novel methods and systems for video compression.

60. The '112 patent discloses novel technologies for video compression that perform predictive coding on a macroblock of a video frame such that a set of pixels of the macroblock is coded using some of the pixels from the same video frame as reference pixels and the rest of the macroblock is coded using reference pixels from at least one other video frame.

61. The '112 patent discloses a system for video compression comprising an intra-frame coding unit configured to perform predictive coding on a set of pixels of a macroblock of pixels using a first group of reference pixels, the macroblock of pixels and the first group of reference pixels being from a video frame.

62. The '112 patent discloses a system for video compression comprising an inter-frame coding unit configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels, the second group of reference pixels being from at least one other video frame.

63. The '112 patent and its underlying patent application have been cited by 10 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '112 patent and its underlying patent application as relevant prior art:

- British Broadcasting Corporation
- Google LLC
- Megachips Corp.
- Olympus Corp.
- Samsung Electronics Co., Ltd.
- Sony Corporation
- Toshiba Corporation

U.S. PATENT NO. 7,894,529

64. U.S. Patent No. 7,894,529 (the "'529 patent") entitled, *Method And Device For Determining Motion Vectors*, was filed on June 1, 2006, and claims priority to June 3, 2005. The '529 patent is subject to a 35 U.S.C. § 154(b) term extension of 1,301 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '529 patent. A true and correct copy of the '529 patent is attached hereto as Exhibit 9.

65. The '529 patent discloses novel methods and apparatuses for determining motion vectors that are each assigned to individual image regions.

66. The inventions disclosed in the '529 patent enable an increase in the resolution of video and image signals during the motion estimation process.

67. The '529 patent discloses a method for determining motion vectors which are assigned to individual image regions of an image.

68. The '529 patent discloses a method wherein an image is subdivided into a number of image blocks, and a motion estimation technique is implemented to assign at least one motion vector to each of the image blocks where a modified motion vector is generated for at least a first image block.

69. The '529 patent discloses a method that determines at least a second image block through which the motion vector assigned to the first image block at least partially passes.

70. The '529 patent discloses a method that generates the modified motion vector as a function of a motion vector assigned to at least the second image block.

71. The '529 patent discloses a method that assigns the modified motion vector as the motion vector to the first image block.

72. The '529 patent and its underlying patent application have been cited by multiple patents and patent applications as relevant prior art. Specifically, patents issued to Fujifilm Corp.,

and Samsung Electronics Co., Ltd. have cited the '529 patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,542,041

73. U.S. Patent No. 7,542,041 (the "041 patent") entitled, *Runtime Configurable Virtual Video Pipeline*, was filed on April 2, 2004, and claims priority to April 3, 2003. The '041 patent is subject to a 35 U.S.C. § 154(b) term extension of 288 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '041 patent. A true and correct copy of the '041 patent is attached hereto as Exhibit 10.

74. The '041 patent discloses novel systems for dynamically configuring a multi-pipe pipeline system.

75. The inventions disclosed in the '041 patent enable a multiple-pipeline system that is dynamically configurable to effect various combinations of functions for each pipeline.

76. The inventions disclosed in the '041 patent teach a multiple pipeline system that includes a pool of auxiliary function blocks that are provided as required to select pipelines.

77. In one embodiment of the '041 patent, each pipeline of the multiple-pipeline system is configured to include a homogenous set of core functions. A pool of auxiliary functions is provided for selective insertion of auxiliary functions between core functions of select pipelines.

78. In one embodiment of the '041 patent, each auxiliary function includes a multiplexer that allows it to be selectively coupled within each pipeline.

79. The '041 patent discloses, in one embodiment, a processing system that includes a plurality of pipelines, with each pipeline of the plurality including a plurality of core pipeline elements that are configured to sequentially process data as it traverses the pipeline.

80. The ‘041 patent discloses, in one embodiment, a processing system that includes a plurality of auxiliary elements, each auxiliary element of the plurality of auxiliary elements being configured to be selectively coupled to multiple pipelines of the plurality of pipelines.

81. The ‘041 patent discloses, in one embodiment, a processing system wherein the auxiliary elements are responsive to external coupling-select signals.

82. The ‘041 patent discloses, in one embodiment, a processing system wherein a plurality of auxiliary elements are within a selected pipeline of the multiple pipelines, between a pair of core pipeline elements of the plurality of core pipeline elements to process the data as it traverses between the pair of core elements.

83. The ‘041 patent has been cited by several United States patents and patent applications as relevant prior art. Specifically, patents and patent applications issued to Microsoft Corporation, Xilinx Inc., Canon Inc., Intel Corporation, and Nokia Oyj have cited the ‘041 patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,571,450

84. U.S. Patent No. 7,571,450 (the “’450 patent”) entitled, *System For And Method Of Displaying Information*, was filed on February 12, 2003, and claims priority to March 11, 2002. The ‘450 patent is subject to a 35 U.S.C. § 154(b) term extension of 846 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘450 patent. A true and correct copy of the ‘450 patent is attached hereto as Exhibit 11.

85. The ‘450 patent discloses novel methods and systems for displaying information. The inventions disclosed in the ‘450 patent enable methods and systems wherein a user does not need to make a new selection after being switched from one service to a second service.

86. The inventions disclosed in the ‘450 patent permit a user of an information display system to have selections made on a first service also presented when the user switches to a second service without requiring the user to browse through the menus to define the type of information to be displayed a second time.

87. In one embodiment of the ‘450 patent, the user selection being made on the basis of the provided options while the first service was selected is used to select the appropriate data elements of the stream of the second service.

88. The inventions disclosed in the ‘450 patent enable various content sources to share similar information models.

89. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein receiving a transport stream comprises services, with the services having elementary streams of video and of data elements.

90. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein user actions of making a user selection of a type of information to be displayed on the device are received.

91. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein filtering to select a data element of a first one of the services on the basis of the user selection is performed.

92. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein rendering to calculate an output image to be displayed on the display device, on the basis of the first data element selected by the filer is performed.

93. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein switching from the first one of the services to a second one of the

services, characterized in comprising a second step of filtering to select a second data-element of the second one of the services, on basis of the user selection is performed.

94. The ‘450 patent, in one embodiment, discloses a method of displaying information on a display device wherein being switched from the first one of the services to the second one of the services, with the data-element and the second data-element being mutually semantically related and a second step of rendering to calculate the output image to be displayed on the display device, on basis of the second data-element selected by the filter is performed.

95. The ‘450 patent and its underlying patent application have been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to AT&T Intellectual Property I LP, Nokia Oyj, Samsung Electronics Co., Ltd., and ZTE Corporation have all cited the ‘450 patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,750,979

96. U.S. Patent No. 7,750,979 (the “’979 patent”) entitled, *Pixel-Data Line Buffer Approach Having Variable Sampling Patterns*, was filed on October 26, 2001. The ‘979 patent is subject to a 35 U.S.C. § 154(b) term extension of 2,749 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘979 patent. A true and correct copy of the ‘979 patent is attached hereto as Exhibit 12.

97. The ‘979 patent discloses novel methods and systems for motion compensation in video signal processing.

98. The ‘979 patent discloses methods and systems that use line buffers that are decoupled and that can deliver a fixed number of pixels, as may be required by a video processing stage, using a sampling pattern that is defined as one among several selectable sampling windows.

99. The '979 patent discloses a video processing circuit having an input stream of pixels corresponding to an array of video pixels.

100. The '979 patent further discloses having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array.

101. The '979 patent further discloses having a video processing stage that inputs pixels using a fixed number of pixels.

102. The '979 patent further discloses a method for delivering the input stream of pixels to the video processing stage.

103. The '979 patent further discloses a method comprising establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels.

104. The '979 patent further discloses a method comprising storing pixels from the input stream into a first set of line butters, the pixels stored in the first set of line butters including pixels for the established window size.

105. The '979 patent further discloses a method comprising prefetching the stored pixels from the first set of line butters into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size.

106. The '979 patent further discloses a method comprising fetching the fixed number of pixels from the second set of line buffers for the video processing stage.

U.S. PATENT NO. 6,421,090

107. U.S. Patent No. 6,421,090 (the "'090 patent") entitled, *Motion And Edge Adaptive Deinterlacing*, was filed on August 27, 1999. Dynamic Data is the owner by assignment of all

right, title, and interest in the '090 patent. A true and correct copy of the '090 patent is attached hereto as Exhibit 13.

108. The '090 patent discloses novel methods and apparatuses for interpolating a pixel during the deinterlacing of video signals. The various embodiments of the '090 patent utilize multiple, interlaced scan lines of video signal, with each scan line including a series of pixels with intensity values.

109. The '090 patent discloses generating a motion value representative of the motion between successive frames about the pixel by segmenting an image into multi-pixel segments and comparing the differences with respect to each segment in successive frames.

110. The '090 patent discloses detecting an edge direction about the pixel and performing an edge adaptive interpolation at the pixel using a generated motion value.

111. The '090 patent further discloses generating a motion value by comparing segments of pixels about the pixel from at least three successive frames.

112. The '090 patent and its underlying patent application have been cited by 86 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '090 patent and its underlying patent application as relevant prior art:

- Samsung Electronics Co., Ltd.
- LG Electronics Inc.
- Qualcomm Inc.
- Microsoft Corporation
- Panasonic Corporation
- STMicroelectronics SRL
- Matsushita Electric Industrial Company Ltd.
- Sanyo Electric Company Ltd.
- Fujitsu Limited
- AVerMedia Technologies Inc.
- Sony Corporation
- Himax Technologies Inc.
- Mitsubishi Electric Corporation
- Hewlett-Packard Development Company L.P.

- MediaTek Inc.
- Realtek Semiconductor Corp.
- Imagination Technologies Limited
- Integrated Device Technology Incorporated
- Intel Corporation
- MStar Semiconductor Incorporated

U.S. PATENT NO. 6,782,054

113. U.S. Patent No. 6,782,054 entitled, *Method And Apparatus For Motion Vector Estimation*, was filed on April 20, 2001. The '054B Patent is subject to a 35 U.S.C. § 154(b) term extension of 485 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '054B Patent. A true and correct copy of the '054B Patent is attached hereto as Exhibit 14.

114. The '054B Patent discloses novel methods and systems for motion estimation in a sequence of moving video pictures.

115. The inventions disclosed in the '054B Patent increase the speed of convergence of motion vectors to improve the convergence process.

116. The '054B Patent discloses a method to enhance motion estimation that includes selecting a displacement vector as a best motion vector for a region in a field from a plurality of at least two candidate motion vectors by applying an error function to each of said plural candidate motion vectors, wherein the candidate motion vector with the least error is selected as the displacement vector for the region in the field.

117. The '054B Patent discloses a method to enhance motion estimation that includes an error function comprising a first penalty term that depends on a type of the candidate motion vector and a second penalty term that depends on the position and size of the candidate motion vector.

118. The ’054B Patent and its underlying patent application have been cited by 54 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’054B Patent and its underlying patent application as relevant prior art:

- Samsung Electronics Co., Ltd.
- Sony Corporation
- MediaTek Inc.
- Qualcomm Incorporated
- Micronas GmbH
- Google Inc.
- Thomson Licensing
- Brightscale, Inc.
- Genesis Microchip Inc.
- STMicroelectronics SA
- Toshiba Corp.

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 8,189,105

119. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

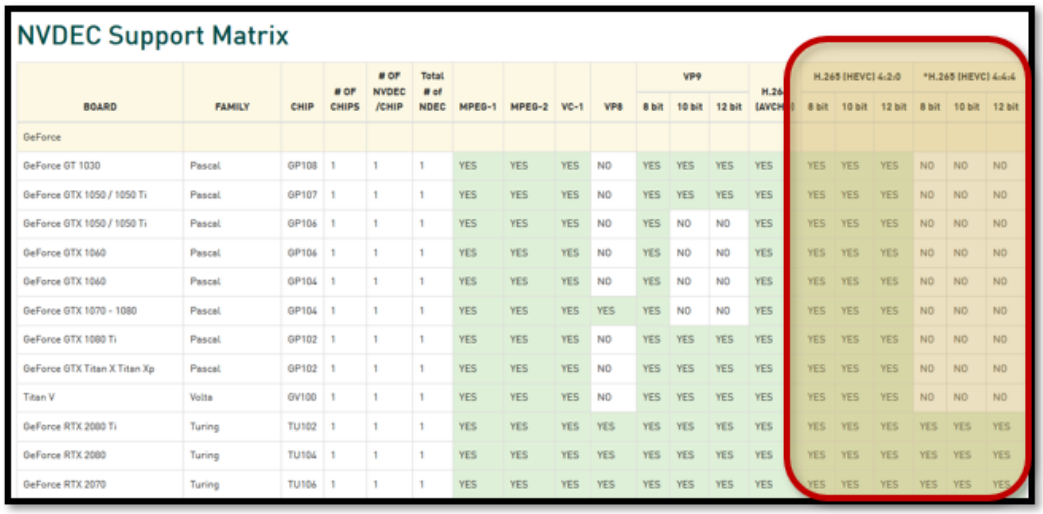
120. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion compensation in video signal processing.

121. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for processing pixel information based on received motion and edge data.

122. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA products, including the following: GeForce GT 1030, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000 / P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla M4, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 750 GeForce GTX 950 - 960, GeForce GT 1030, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, and Quadro P1000 (collectively, the “NVIDIA ‘105 Product(s)”).

123. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '105 Products in regular business operations.

124. On information and belief, the NVIDIA '105 Products perform video processing complaint with the HEVC standard. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '105 Products comply with the HEVC standard for decoding data.

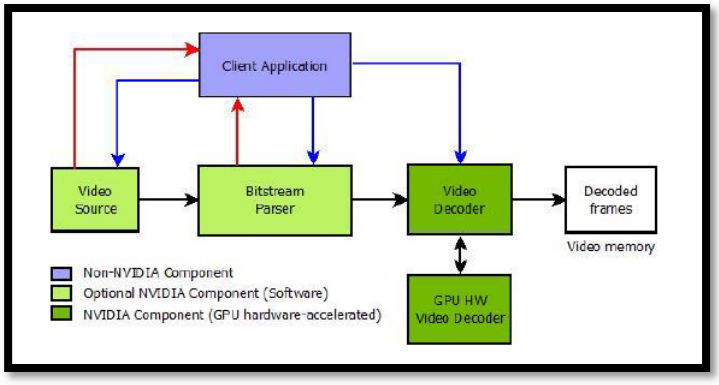


NVDEC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVDEC /CHIP	Total # of NDEC	MPEG-1	MPEG-2	VC-1	VP8	VP9			H.264 (AVCHD)	H.265 (HEVC) 4:2:0			H.265 (HEVC) 4:4:4		
										8 bit	10 bit	12 bit		8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
GeForce																			
GeForce GT 1030	Pascal	GP108	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP104	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1070 - 1080	Pascal	GP104	1	1	1	YES	YES	YES	YES	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1080 Ti	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
Titan V	Volta	GV100	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce RTX 2080 Ti	Turing	TU102	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC decoding in compliance with the HEVC standard).

125. The NVIDIA '105 Products comply with the HEVC standard in decoding video data. The NVIDIA document shows the NVDEC interface for decoding video data.



NVIDIA Video Decoder (NVDEC) Interface, NVIDIA PROGRAMMING GUIDE at 4 (June 2016) (annotations added) (showing the functionality for decoding video data for on-screen display).

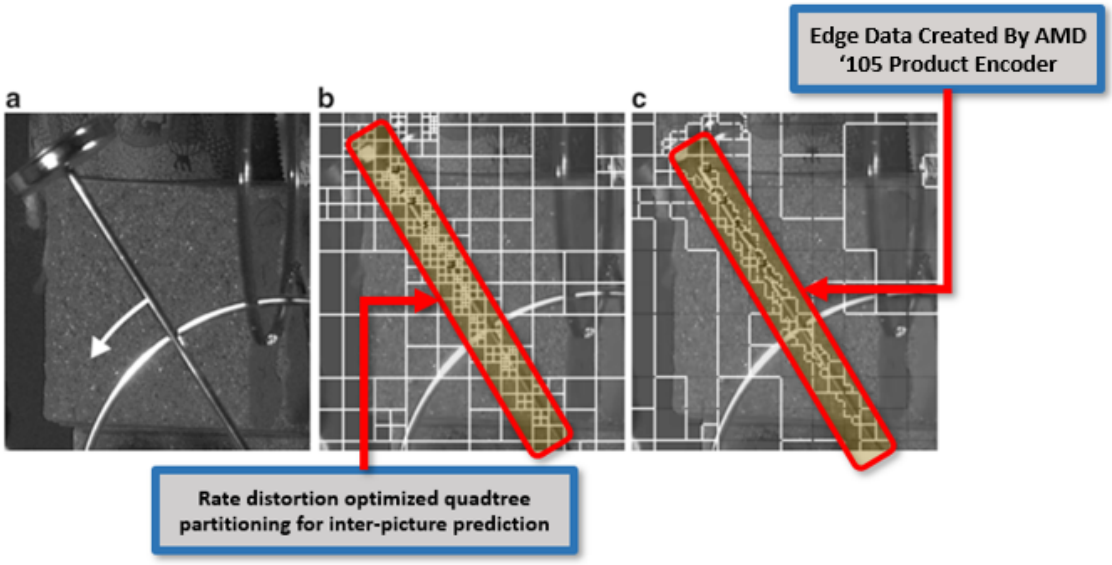
126. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '105 Products - necessarily infringe the '105 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '105 patent, including but not limited to claim 1 of the '105 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '105 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

127. On information and belief, the NVIDIA '105 Products comply with the HEVC standard, which requires processing edge data from edge-adaptive interpolation processing.

128. The NVIDIA '105 Products use two types of prediction methods for processing pixel information when encoding and decoding video data in HEVC format: inter prediction and intra prediction. Inter prediction utilizes motion vectors for block-based inter prediction to exploit

temporal statistical dependencies between different pictures. Intra prediction uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. The HEVC Specification (*e.g., High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) sets forth the standard that is followed by HEVC compliant devices such as the NVIDIA '105 Products, and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the NVIDIA '105 Products perform a method for encoding a video signal comprised of pixels using motion vectors when performing encoding of H.265/HEVC video data.

129. During the encoding process the NVIDIA '105 products process pixel information based on edge data. The edge data is generated by the NVIDIA '105 products using merge mode estimation. Specifically, the NVIDIA '105 Products generate merge estimation regions which identify edge information within a video frame. The merge estimation regions are comprised of prediction units ("PU") that contain luma values. For example, in the below diagram PUs are shown. The encoding process then identifies along the edges of each prediction unit a merge estimation region ("MER"). The MER regions thus identify the edges and the PU contains the intensity estimate for the pixels.



Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (annotations added).

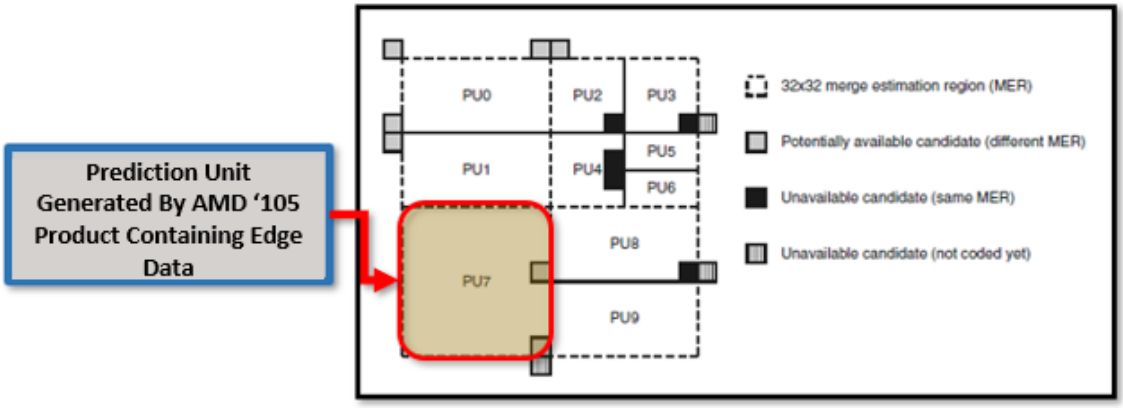
130. The NVIDIA '105 Products in the process of encoding video content in HEVC format generate merge estimation regions generate edge data that include luma location and luma values which include a first intensity estimate. The HEVC standards describes this process as leading to the generation of luma motion vector mvL0 and mvL1.

> [T]he derivation process for luma motion vectors for merge mode as specified in clause I.8.5.3.2.7 is invoked with the luma location (xCb, yCb), the luma location (xPb, yPb), the variables nCbS, nPbW, nPbH, and the partition index partIdx as inputs, and the output being the luma motion vectors mvL0, mvL1, the reference indices refIdxL0, refIdxL1, the prediction list utilization flags predFlagL0 and predFlagL1, the flag ivMcFlag, the flag vspMcFlag, and the flag subPbMotionFlag.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.2.1 (February 2018) (emphasis added).

131. The NVIDIA '105 Products perform the step of processing edge data from an edge adaptive interpolation process wherein the edge data includes a first intensity estimate of the pixel. Specifically, the NVIDIA '105 Products implement HEVC encoding which utilizes Parallel Merge Mode and Merge Estimation Regions (MER's) within the interpolation process to determine pixel edges. Parallel Merge Mode Estimation identifies the edge data within a prediction unit. The

below diagram shows how video data is portioned into 10 prediction units and edge data is calculated and passed to the encoder.



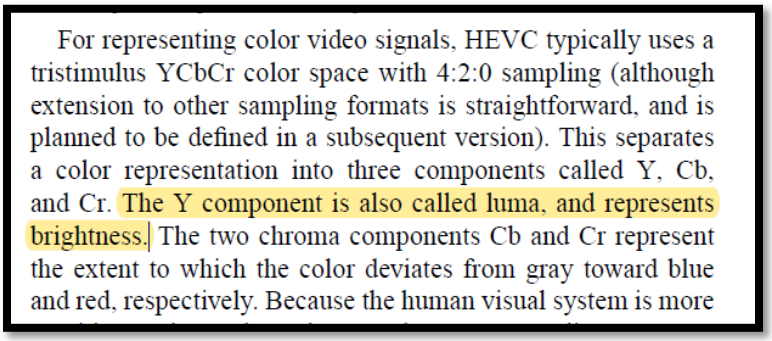
Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 127 (September 2014) (annotations added).

132. The merge estimation processes implemented by the NVIDIA '105 Products is "adaptive." The below excerpt from documentation regarding the HEVC encoding process describes that the "merge estimation level is adaptive."

> In order to enable an encoder to trade-off parallelism and coding efficiency, the parallel merge estimation level is adaptive and signaled as `log2_parallel_merge_level_minus2` in the picture parameter set. The following MER sizes are allowed: 4×4 (no parallel merge estimation possible), 8×8, 16×16, 32×32 and 64×64. A higher degree of parallelization, enabled by a larger MER, excludes more potential candidates from the merge candidate list.

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 128 (September 2014) (emphasis added).

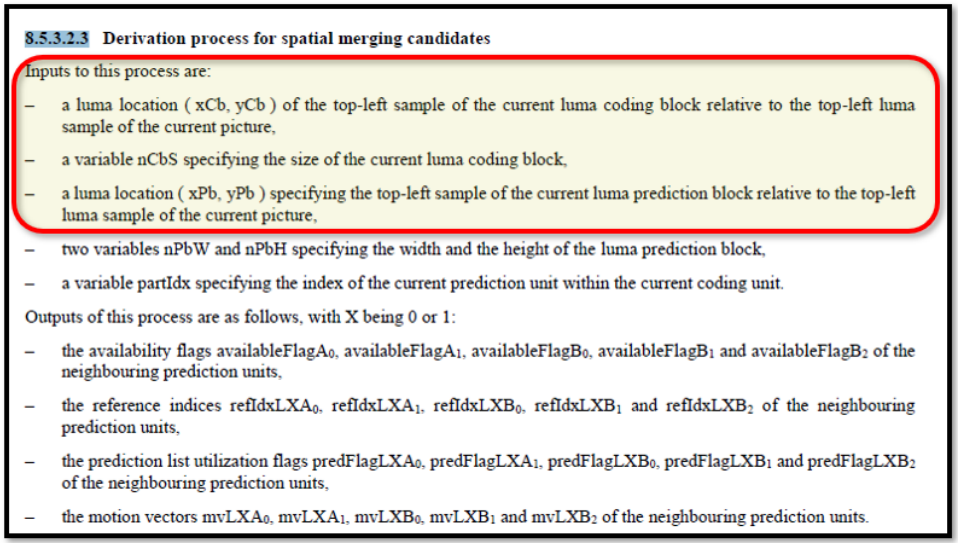
133. The edge data that is processed from the edge adaptive interpolation process includes intensity estimates for pixels such as pixels in the merge estimation region. The intensity estimate or brightness estimate is referred to as "luma" in the encoding functionality implemented by the NVIDIA '105 Products.



For representing color video signals, HEVC typically uses a tristimulus YCbCr color space with 4:2:0 sampling (although extension to other sampling formats is straightforward, and is planned to be defined in a subsequent version). This separates a color representation into three components called Y, Cb, and Cr. The Y component is also called luma, and represents brightness. The two chroma components Cb and Cr represent the extent to which the color deviates from gray toward blue and red, respectively. Because the human visual system is more

Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1654 (December 2012) (emphasis added).

134. The motion estimation region ("MER") is an adaptive interpolation process in which the edges of images are calculated and include the intensity estimates of pixels by way of a luma value. The below excerpt from the HEVC specification describes how during the generation of merge estimation regions edge data includes luminosity values (intensity estimates) for pixels within a region.



8.5.3.2.3 Derivation process for spatial merging candidates

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

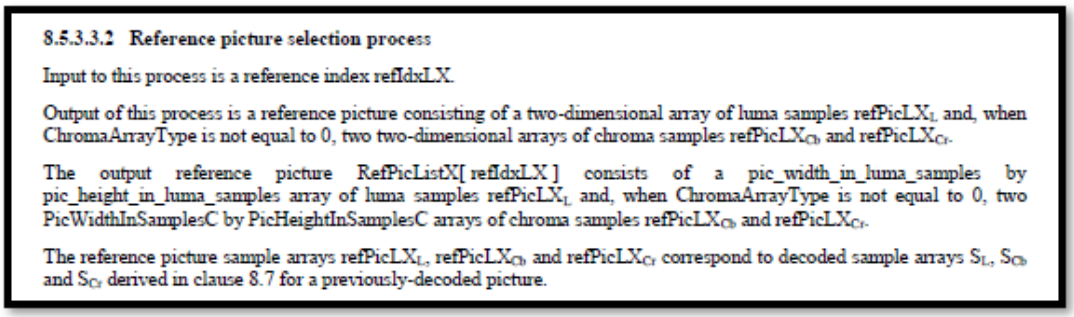
Outputs of this process are as follows, with X being 0 or 1:

- the availability flags availableFlagA$_0$, availableFlagA$_1$, availableFlagB$_0$, availableFlagB$_1$ and availableFlagB$_2$ of the neighbouring prediction units,
- the reference indices refIdxLXA$_0$, refIdxLXA$_1$, refIdxLXB$_0$, refIdxLXB$_1$ and refIdxLXB$_2$ of the neighbouring prediction units,
- the prediction list utilization flags predFlagLXA$_0$, predFlagLXA$_1$, predFlagLXB$_0$, predFlagLXB$_1$ and predFlagLXB$_2$ of the neighbouring prediction units,
- the motion vectors mvLXA$_0$, mvLXA$_1$, mvLXB$_0$, mvLXB$_1$ and mvLXB$_2$ of the neighbouring prediction units.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § I.8.5.2.3 (February 2018) (emphasis added).

135. The NVIDIA '105 Products process motion data associated with motion compensation. The motion data processed by the NVIDIA '105 Products include a first estimated

motion vector of pixels within a reference frame prior to the current frame and a second estimated motion vector within the reference field after the current field. Specifically, the NVIDIA '105 products generate motion data in the form of a bi-directional prediction unit (PU) which has two motion vectors (referencing a prior frame and a subsequent frame in the sequence). The two motion vectors are combined to make a "bi-predictive merge candidate." One of the motion vectors is obtained from "reference picture list0" and the other motion vector is obtained from "reference picture list1."



8.5.3.3.2 Reference picture selection process

Input to this process is a reference index refIdxLX.

Output of this process is a reference picture consisting of a two-dimensional array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two two-dimensional arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The output reference picture RefPicListX[refIdxLX] consists of a pic_width_in_luma_samples by pic_height_in_luma_samples array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two PicWidthInSamplesC by PicHeightInSamplesC arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The reference picture sample arrays $refPicLX_L$, $refPicLX_{Cb}$ and $refPicLX_{Cr}$ correspond to decoded sample arrays S_L, S_{Cb} and S_{Cr} derived in clause 8.7 for a previously-decoded picture.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.3 (February 2018).

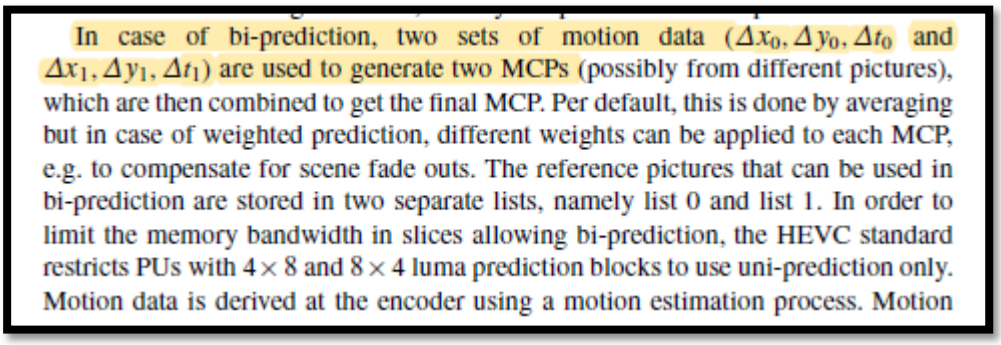
136. The reference pictures that are used to generate a motion vector comprise both the forward and prior reference pictures which are referred to in the HEVC encoding process implemented by the NVIDIA '105 Products as "refPicLXcb" and "refPicLXcr." The following excerpt describing the implementation of the encoding process in the NVIDIA '105 Products which use bi-predictive slices.

> Since a merge candidate comprises all motion data and the TMVP is only one motion vector, the derivation of the whole motion data only depends on the slice type. For bi-predictive slices, a TMVP is derived for each reference picture list. Depending on the availability of the TMVP for each list, the prediction type is set to bi-prediction or to the list for which the TMVP is available. All associated reference picture indices are set equal to zero. Consequently for uni-predictive slices, only the TMVP for list 0 is derived together with the reference picture index equal to zero.

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added) (describing the use of bi-prediction in which

motion data is derived from the forward and prior reference pictures in generating temporal arrays/vectors).

137. The NVIDIA '105 Products interpolation process contains bi-prediction functionality that computes a first estimated motion prediction and a second estimated motion prediction. The below excerpt from documentation of the encoding method used by the NVIDIA '105 products describes that the encoding process includes functionality for generating a second intensity estimate for the pixel data and the edge data determined according to motion. In bi-prediction, the second estimate is defined as Δx_1, Δy_1, Δt_1.



In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (emphasis added).

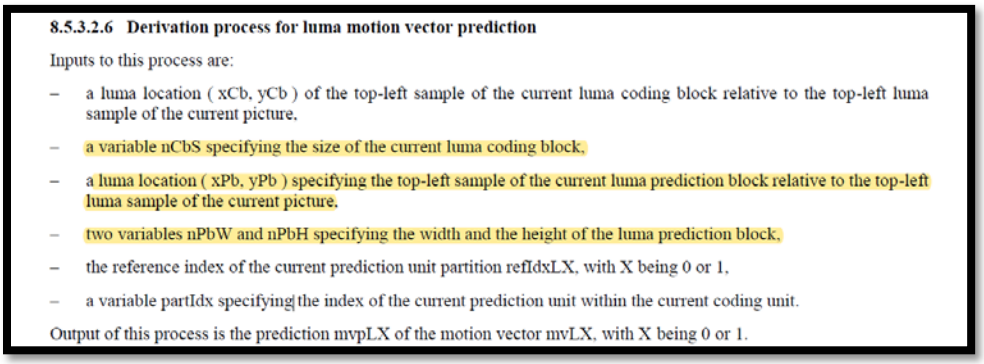
138. In AMVP the system generates a temporal intermediate candidate based on bi-directional motion data. The "inter_pred_idc [x0] [y0] specifies whether list0, list1, or bi-prediction is used for the current prediction unit" according to the below referenced table. "The array indices x0, y0 specify the location (x0, y0) of the top-left luma sample of the considered prediction block relative to the top-left luma sample of the picture."

Table 7-11 – Name association to inter prediction mode

inter_pred_idc	Name of inter_pred_idc	
	(nPbW + nPbH) != 12	(nPbW + nPbH) == 12
0	PRED_L0	PRED_L0
1	PRED_L1	PRED_L1
2	PRED_BI	na

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.9.6 (February 2018).

139. The NVIDIA '105 products generate a second intensity estimate based on the edge data and the motion data. The edge data is combined with the temporal intermediate candidate to generate the temporal candidate. The prediction unit based on the first and second motion vector (motion data) is then combined with the edge data to generate a second intensity estimate. Once the reference picture for obtaining the co-located PU is selected then the position of the co-located Pu will be selected among two candidate positions. A second intensity estimate is generated by using the bi-directional motion vectors and the edge data. The below excerpt from the HEVC specification describes that for a luma motion vector prediction the generation of a second intensity estimate is based on the motion data and the edge data. The edge data here is comprised by the luma location and luma prediction block information. Further, the luma motion vectors mvLO and mvL1 are combined with the edge data including luma location xCB yCB xBL and yBl to generate a second intensity estimate.



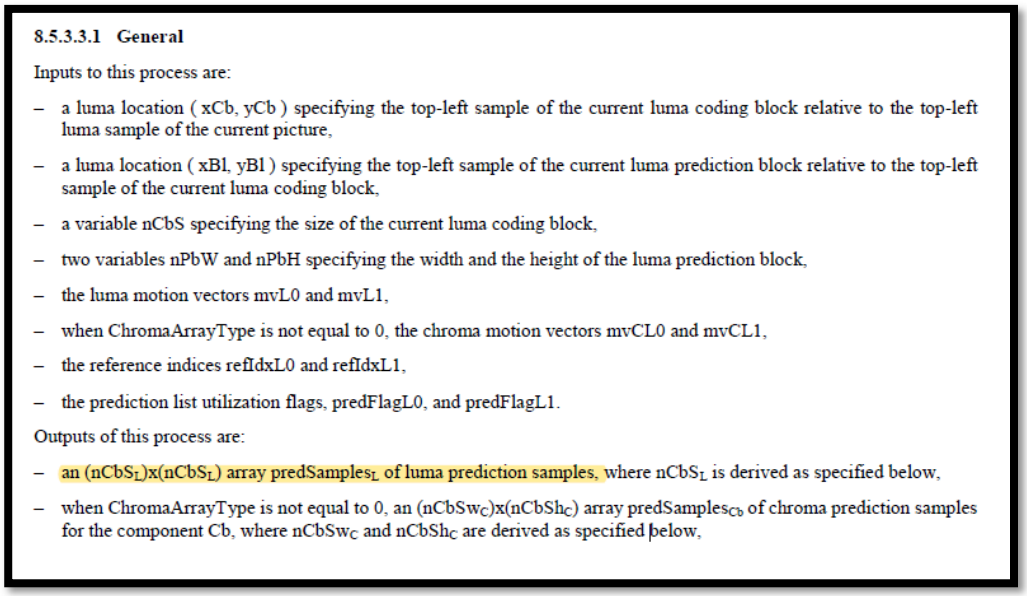
8.5.3.2.6 Derivation process for luma motion vector prediction

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the reference index of the current prediction unit partition refIdxLX, with X being 0 or 1,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

Output of this process is the prediction mvpLX of the motion vector mvLX, with X being 0 or 1.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.2.6 (February 2018) (emphasis added).



8.5.3.3.1 General

Inputs to this process are:

- a luma location (xCb, yCb) specifying the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a luma location (xBl, yBl) specifying the top-left sample of the current luma prediction block relative to the top-left sample of the current luma coding block,
- a variable nCbS specifying the size of the current luma coding block,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the luma motion vectors mvL0 and mvL1,
- when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1,
- the reference indices refIdxL0 and refIdxL1,
- the prediction list utilization flags, predFlagL0, and predFlagL1.

Outputs of this process are:

- an $(nCbS_L)x(nCbS_L)$ array $predSamples_L$ of luma prediction samples, where $nCbS_L$ is derived as specified below,
- when ChromaArrayType is not equal to 0, an $(nCbSw_C)x(nCbSh_C)$ array $predSamples_{Cb}$ of chroma prediction samples for the component Cb, where $nCbSw_C$ and $nCbSh_C$ are derived as specified below,

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.1 (February 2018) (emphasis added).

140. The NVIDIA '215 Products perform a mixing process in which the final edge/motion data of a pixel is calculated based on a first intensity estimate, second intensity estimate, and motion reliability data. Specifically, the NVIDIA '215 Products encode pixel data using bi-prediction wherein use two types of mixing functions: average mixing and weighted mixing.

In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added).

141. The HEVC standard includes functionality to perform a mixing process. In MERGE mode, an up-to five-entry MERGE candidate list is first constructed with four (MV, Refldx) pairs from spatial neighbor blocks and one (MV, Refldx) pair from temporal bottom-right or collocated neighbor block, where Refldx is the index of the reference picture that the MV pointed to. After that, the encoder decides to use which candidate (MV, Refldx) pair to encode current block and then encode the candidate index into bitstream. In MERGE mode, the selected (MV, Refldx) pair is directly used to encode current block, and no MVD information needs to be coded. The number of merge candidates could be configured at encoder, with up to five merge candidates."

8.5.3.3.4 Weighted sample prediction process

8.5.3.3.4.1 General

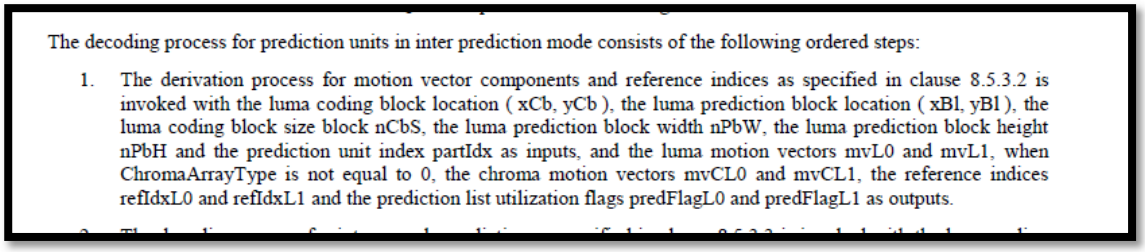
Inputs to this process are:

- two variables nPbW and nPbH specifying the width and the height of the current prediction block,
- two (nPbW)x(nPbH) arrays predSamplesL0 and predSamplesL1,
- the prediction list utilization flags, predFlagL0 and predFlagL1,
- the reference indices refIdxL0 and refIdxL1,
- a variable cIdx specifying colour component index.

Output of this process is the (nPbW)x(nPbH) array pbSamples of prediction sample values.

HIGH EFFICIENCY VIDEO CODING, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.4.1 (February 2018) (emphasis added).

142. The variables predFlagL0 and predFlagL1 are reliability values that are generated by the decoding process. The predFlagL0 and L1 values are prediction utilization values that are used to generate prediction utilization and reliability of the vectors.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

143. On information and belief, any implementation of the HEVC standard would infringe the '105 patent as every possible implementation of the standard requires: processing edge data from edge-adaptive interpolation processing, including a first intensity estimate for the pixel as well as data pertaining to one or more pixels that neighbor the pixel; processing motion data associated with motion compensation processing, wherein the motion data includes a first estimated motion vector for a pixel in a reference field prior to the present field and a second estimated motion vector for a pixel in a reference field subsequent to the present field; determining a second intensity estimate for the pixel as a function of the edge data and the motion data; and performing a blending process wherein final edge/motion data of the pixel is calculated as a function of the first intensity estimate, the second intensity estimate, and motion reliability data characterizing reliability of the motion data.

144. On information and belief, the NVIDIA '105 Products are available to businesses and individuals throughout the United States.

145. On information and belief, the NVIDIA '105 Products are provided to businesses and individuals located in the State of Delaware.

146. By making, using, testing, offering for sale, and/or selling products and services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the NVIDIA '037 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '105 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

147. On information and belief, NVIDIA also indirectly infringes the '105 patent by actively inducing infringement under 35 USC § 271(b).

148. NVIDIA has had knowledge of the '105 patent since at least service of this First Amended Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '105 patent and knew of its infringement, including by way of this lawsuit.

149. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '105 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '105 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '105 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '105 Products that have the capability of operating in a manner that infringe one or more of the claims of the '105 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '105 Products to utilize the products in a manner that directly infringe one or more claims of the '105 patent.[22] By providing instruction and training to customers and end-users on

[22] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017);

how to use the NVIDIA '105 Products in a manner that directly infringes one or more claims of the '105 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '105 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '105 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '105 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '105 patent, knowing that such use constitutes infringement of the '105 patent.

150. The '105 patent is well-known within the industry as demonstrated by multiple citations to the '105 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '105 patent without paying a reasonable royalty. NVIDIA is infringing the '105 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

151. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '105 patent.

152. As a result of NVIDIA's infringement of the '105 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for

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NVIDIA GeForce GTX 1080, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT II
INFRINGEMENT OF U.S. PATENT NO. 8,135,073

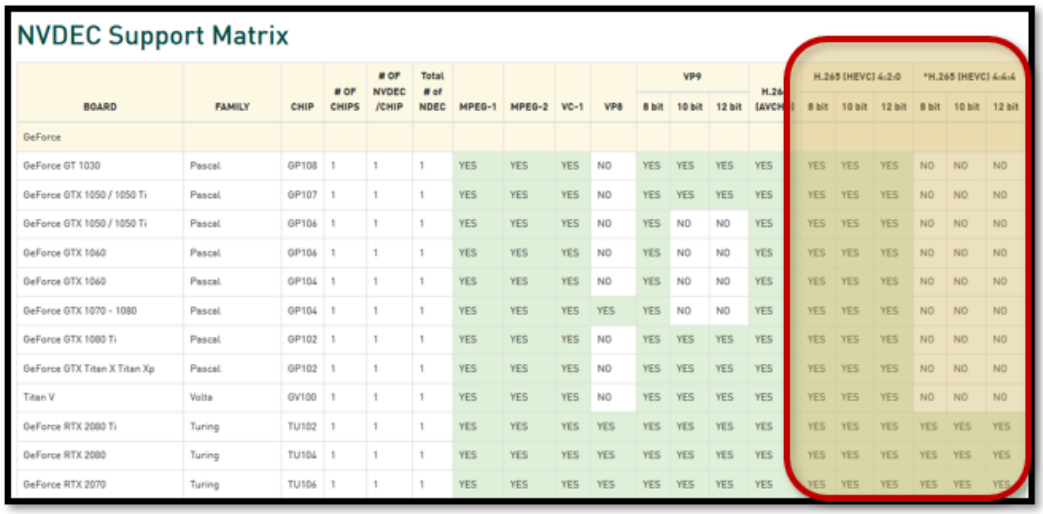
153. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

154. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

155. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA products, including the following: GeForce GT 1030, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000 / P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla M4, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 750 GeForce GTX 950 - 960, GeForce GT 1030, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, and Quadro P1000 (collectively, the "NVIDIA '073 Product(s)").

156. On information and belief, the NVIDIA '073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the NVIDIA '073 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by NVIDIA '073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

157. The NVIDIA '073 Products enable HEVC video decoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '073 Products comply with the HEVC standard for decoding data.

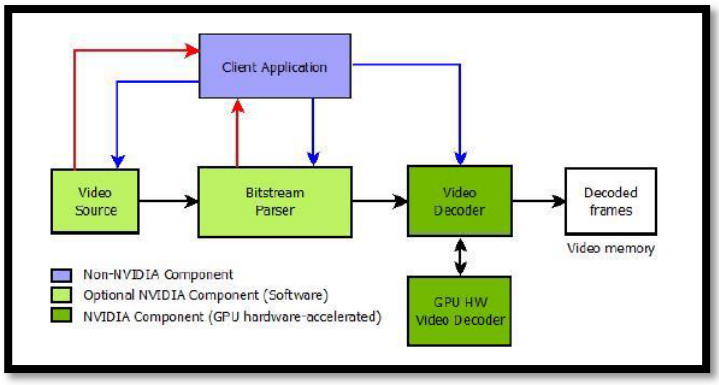


NVDEC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVDEC /CHIP	Total # of NDEC	MPEG-1	MPEG-2	VC-1	VP8	VP9			H.264 (AVCHD)	H.265 (HEVC) 4:2:0			*H.265 (HEVC) 4:4:4		
										8 bit	10 bit	12 bit		8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
GeForce																			
GeForce GT 1030	Pascal	GP108	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP104	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1070 - 1080	Pascal	GP104	1	1	1	YES	YES	YES	YES	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1080 Ti	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
Titan V	Volta	GV100	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce RTX 2080 Ti	Turing	TU102	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC decoding in compliance with the HEVC standard).

158. The NVIDIA '073 Products comply with the HEVC standard in decoding video data. The NVIDIA document shows the NVDEC interface for decoding video data.



NVIDIA Video Decoder (NVDEC) Interface, NVIDIA PROGRAMMING GUIDE at 4 (June 2016) (annotations added) (showing the functionality for decoding video data for on-screen display).

159. On information and belief, the NVIDIA '073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the NVIDIA '073

Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by NVIDIA '073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

160. The NVIDIA Products have an input for receiving frame-based encoded video information. Specifically, the NVIDIA Products receive frame-based encoded video information in the form of video data that is encoded in the High Efficiency Video Coding (HEVC/H.265) format set by the ITU-T Video Coding Experts Group. Documentation and analysis of the circuity of the NVIDIA Product further confirms the NVIDIA Products contain multiple inputs for receiving frame-based encoded video information as shown in the following image.

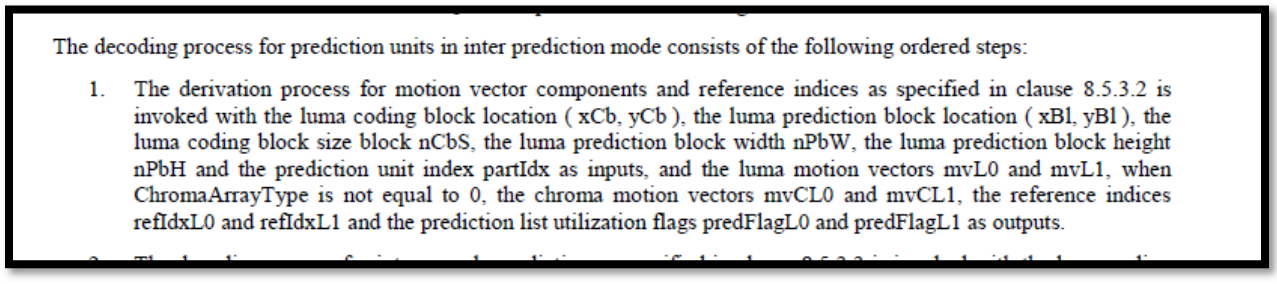
NVIDIA GEFORCE GTX 1080 TEARDOWN (2018).

161. On information and belief, the NVIDIA '073 Products, incorporate a decoding unit for decoding the frame of the received video data. The encoding and decoding process for video data received by the NVIDIA '073 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

162. On information and belief, one or more of the NVIDIA '073 Products include technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

163. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '073 Products - necessarily infringe the '073 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '073 patent, including but not limited to claim 14 of the '073 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '073 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

164. On information and belief, the NVIDIA '073 Products comply with the HEVC standard, which requires that motion vectors are recovered from the second frame in the video stream.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

165. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '073 patent by, among other things, making, using, offering for sale, and/or selling technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the NVIDIA '073 Products. The following excerpt explains how HEVC is a form of frame-based encoded video information.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess. *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

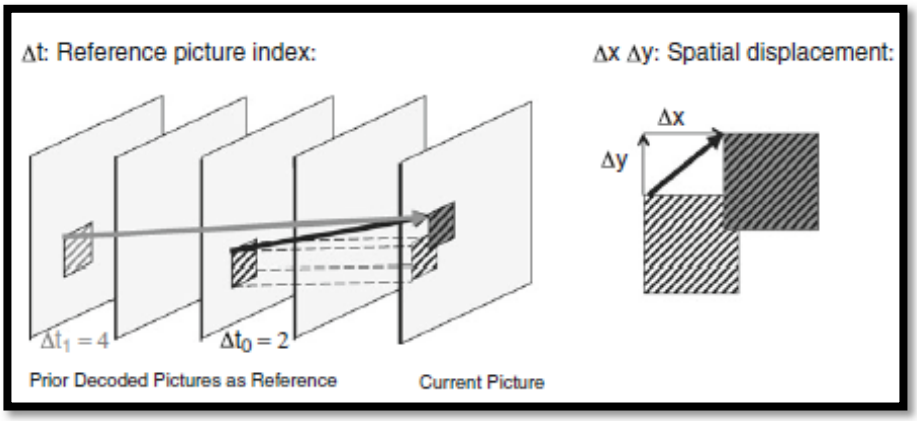
166. On information and belief, the NVIDIA '073 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the NVIDIA '073 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the NVIDIA '073 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

167. The encoded video stream received by the NVIDIA '073 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a

motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



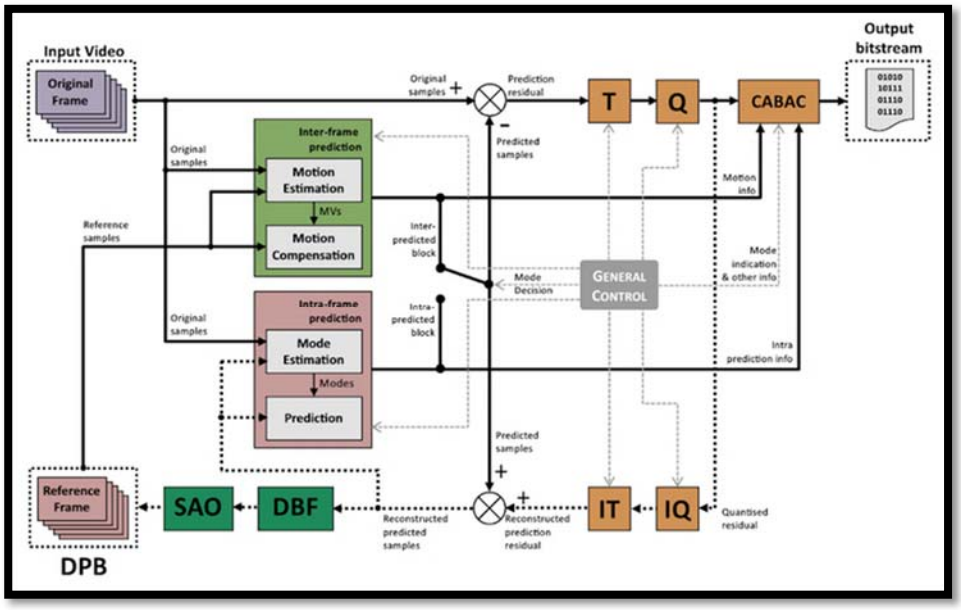
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

168. The following excerpt from an article describing the architecture of the encoded video stream received by the NVIDIA '073 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."

HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

169. The following diagram shows how the NVIDIA Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across a first and second frame.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

170. On information and belief, one or more of the NVIDIA '073 Products reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

> So, this reduces guessing with frame dropping. Let's go over what we've learned. So, with HEVC hierarchical encoding, we have improved temporal scalability. There's a much more obvious frame dropping pattern and it removes frame drop guessing during playback. We also have improved motion compensation, the reference frames are much closer to each other, so we can use more parts of other frames and it also improves compression.

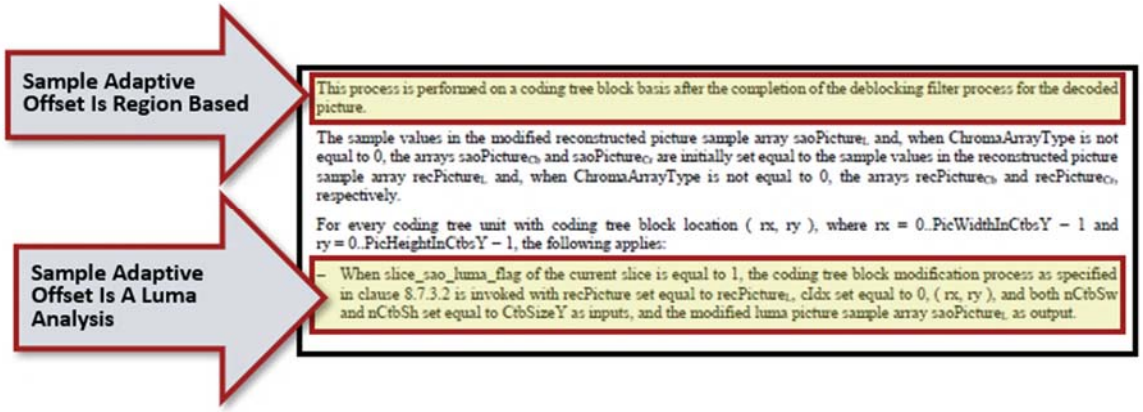
Erik Turnquist and Brad Ford, *Working with HEIF and HEVC*, NVIDIA WORLDWIDE DEVELOPER CONFERENCE 2017: SESSION 511 Transcript (2017) (emphasis added), *available at*: https://developer.NVIDIA.com/videos/play/wwdc2017/511.

171. On information and belief, any implementation of the HEVC standard would infringe the '073 patent as every possible implementation of the standard requires: receiving a video stream containing encoded frame based video information (including both an encoded first

frame and an encoded second frame); the encoded second frame that is received depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame; the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame; decoding the video stream by recovering the motion vectors in the second stream; and determining a re-mapping strategy for the video enhancement of the decoded first frame using a region-based analysis where the first frame is remapped using a remapping strategy and at least one region of the second frame is remapped depending on the re-mapping strategy for corresponding regions of the first frame.

172. On information and belief, the NVIDIA '073 Products use of sample adaptive offset is a region-based luma analysis that is applied to the decoded first frame (reference picture). "The SAO reduces sample distortion by first classifying the samples in the region into multiple categories with as selected classifier and adding a specific offset to each sample depending on its category. The classifier index and the offsets for each region are signaled in the bitstream." Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 185 (September 2014) (emphasis added).

173. Further, the HEVC documentation requires that the application of a sample adaptive offset be region based (*e.g.*, applied to a coding block) ("This process is performed on a coding block basis after the completion for the deblocking filter process for the decoded picture").

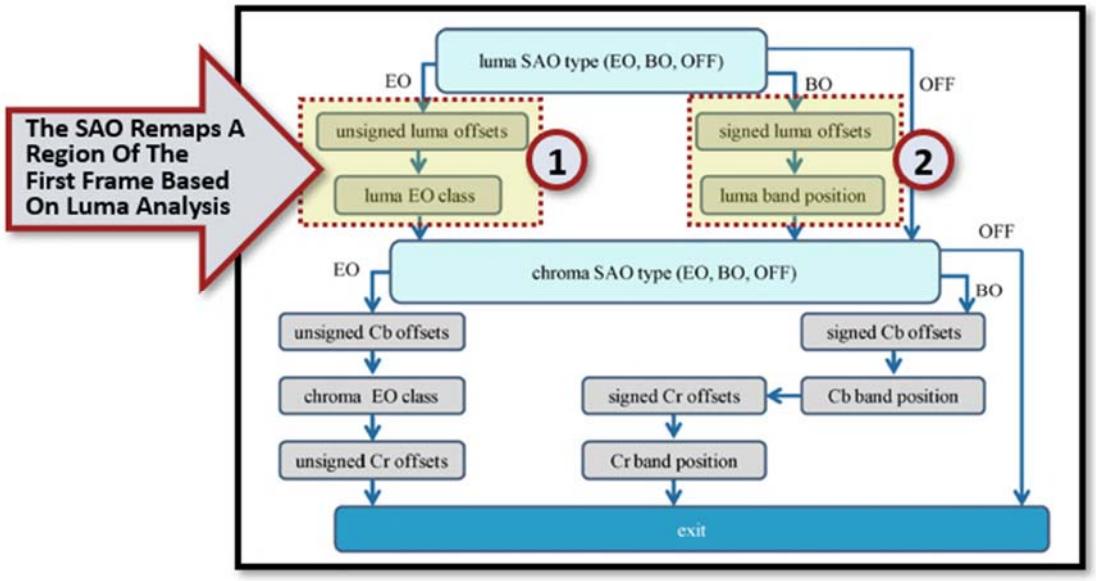


High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 8.7.3.1 (April 2015) (annotations added).

174. On information and belief, the NVIDIA '073 Products contain functionality wherein a decoder applies sample adaptive offset to a decoded reference frame (first frame). Further, the NVIDIA '073 Products apply the sample adaptive offset functions to remap a portion of the region based on luminance values (luma). "SAO can be applied to not only luma but also chroma." Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 at 1765 (December 2012).

175. On information and belief, the NVIDIA '073 Products apply the sample adaptive offset to a coding tree unit (region in the first frame), a luminance analysis is performed using two luminance analysis techniques: Edge Offset ("EO") and Band Offset ("BO"). Edge Offset "uses four 1-D directional patterns for sample classification: horizontal, vertical, 135° diagonal, and 45° diagonal." Chih-Ming Fu, *et al.*, Sample Adaptive Offset in the HEVC Standard, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1757 (December 2012). Band Offset "implies one offset is added to all samples of the same band. The sample value range is equally divided into 32 bands." *Id*. at 1757. The below diagram shows that

the NVIDIA '073 Products use different sample adaptive offsets in a region of the first frame in conducting a luminance analysis.



Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1759 (December 2012) (annotations added showing (1) edge offset and (2) band offset luma analysis).

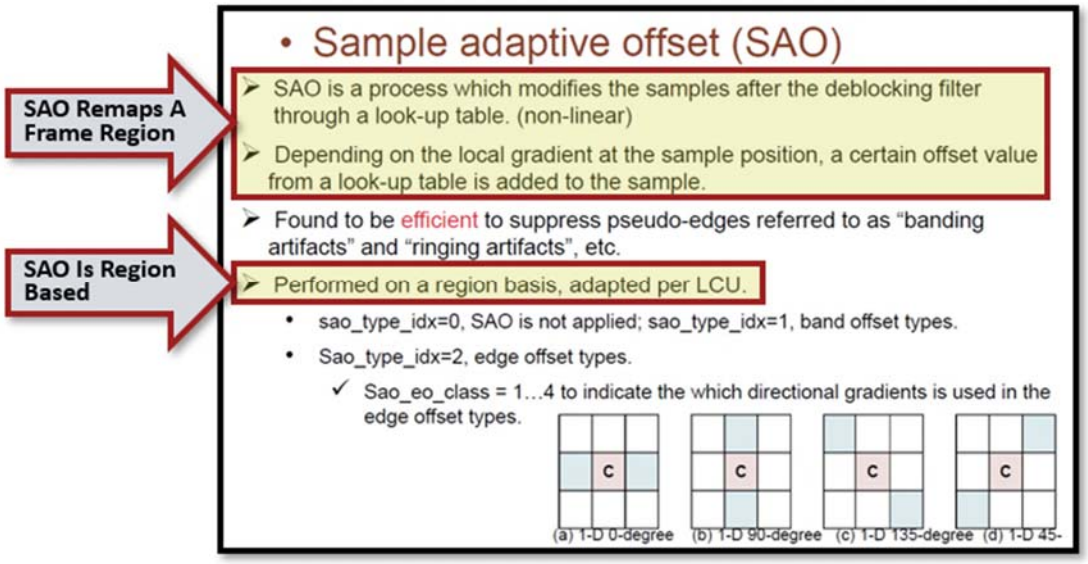
176. Further, HEVC documentation makes clear that the application of the standard adaptive offset remapping policy is based on a luminance analysis. The below shows that slices of a region have a standard adaptive offset applied based on a "luma flag."

if(sample_adaptive_offset_enabled_flag) {	
slice_sao_luma_flag	u(1)
if(ChromaArrayType != 0)	
slice_sao_chroma_flag	u(1)

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § F.7.3.6.1 (April 2015) ("sample_adaptive_offset_enabled_flag equal to 1 specifies that the sample adaptive offset process is applied to the reconstructed picture after the deblocking filter process.").

177. Commentary on the use of sample adaptive offset functionality in decoding HEVC video further confirms that the use of Sample Adaptive Offset (such as that implemented by the

NVIDIA '073 Products) is region based and remaps pixel values in a region of a frame by modifying pixels based on an offset value. "[A]fter the deblocking filter through a look-up table . . . [and applying] a certain offset value from a look-up-table is added to the sample."[23]



Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013) (annotations added).

178. On information and belief, when the NVIDIA '073 Products decode a second frame, the application of the remapping policy (sample adaptive offset) will be determined based on the application of sample adaptive offset to the first frame (reference picture). Thus, the application of the remapping policy (sample adaptive offset) to the first frame has the effect of increasing the quality of the reference picture such that the second frame might no longer require the application of sample adaptive offset (remapping policy).[24]

> The second in-loop filter, SAO, is applied to the output of the deblocking filter and further improves the quality of the decoded picture by attenuating ringing artifacts and changes in sample intensity of some areas of a picture. The most important

[23] Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013).

[24] Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 171 (September 2014) ("HEVC defines two in-loop filters, deblocking and sample adaptive offset (SAO), which significantly improve the subjective quality of decoded video sequences as well as compression efficiency by increasing the quality of the reconstructed/ reference pictures.").

> advantage of the in-loop filters is improved subjective quality of reconstructed pictures. In addition, using the filters in the decoding loop also increases the quality of the reference pictures and hence also the compression efficiency.

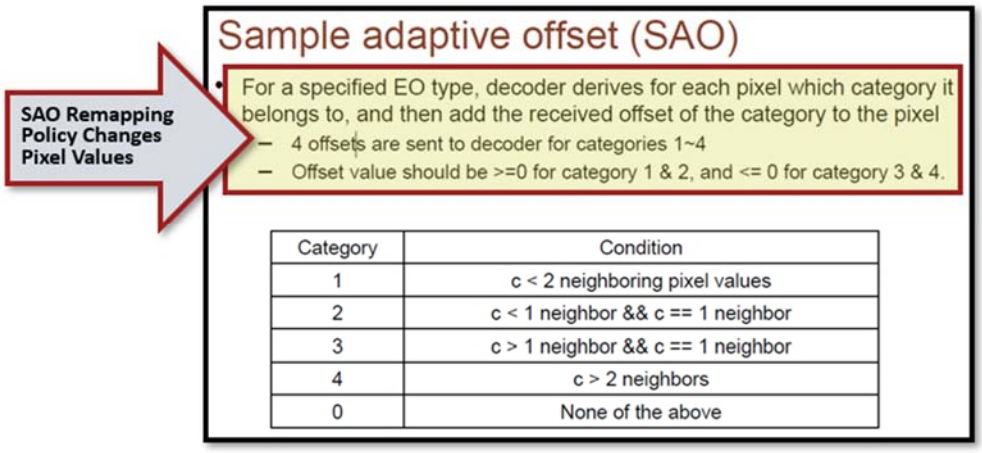
Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 171 (September 2014) (annotations added).

179. Sample adaptive offset as implemented by the NVIDIA '073 Products is a policy that remaps the values of pixels. If sample adaptive offset is applied to a reference frame, regions in a second frame might not require the application of the remapping policy as the reference frame that was used to generate the second frame was of a better quality.

> SAO classifies each pixel into one of four bands or one of four edge types and adds an offset to it. For band offsets, the band of each pixel depends on its value and the position of the four bands. For edge offsets, the edge of each pixel depends on the whether its value is larger or smaller than two of its neighbors. The selection between band offsets and edge offsets, position of bands, choice of neighbors for edge offsets, and values of the offsets are signaled at the CTU level for luma and chroma separately.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 335 (September 2014).

180. The following excerpt from a presentation describing HEVC decoding provides details on how the application of sample adaptive offset remaps pixel values by adding an offset to the pixel value based on a luma analysis.

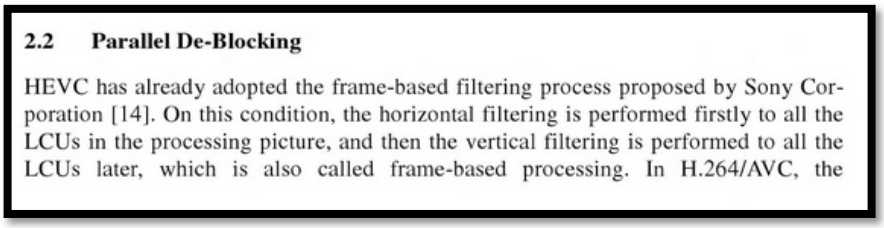


Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 44 (October 2013) (annotation added).

181. The NVIDIA ‘073 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the NVIDIA ‘073 Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx and Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

182. On information and belief, one or more of the NVIDIA ‘073 Products enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

183. On information and belief, one or more of the NVIDIA ‘073 Products include an input for receiving a video stream containing encoded frame-based video information including an encoded first frame and an encoded second frame.

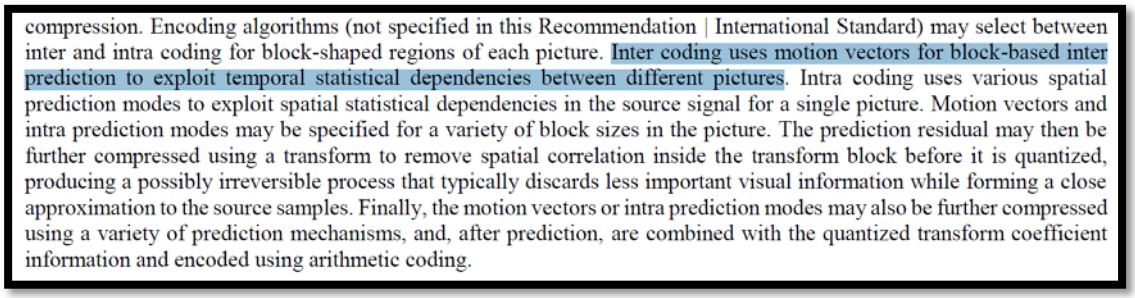


2.2 Parallel De-Blocking

HEVC has already adopted the frame-based filtering process proposed by Sony Corporation [14]. On this condition, the horizontal filtering is performed firstly to all the LCUs in the processing picture, and then the vertical filtering is performed to all the LCUs later, which is also called frame-based processing. In H.264/AVC, the

Ming-Ting Sun, *et al*., *Advances in Multimedia Information Processing*, PCM 2012: 13TH PACIFIC-RIM CONFERENCE ON MULTIMEDIA PROCEEDINGS VOLUME 7674 at 274 (December 4-6, 2012) ("HEVC has already adopted the frame-based filtering process proposed by Sony Corporation.").

184. On information and belief, one or more of the NVIDIA '073 Products include a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame. The Overview of Design Characteristics in the HEVC Standard describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."

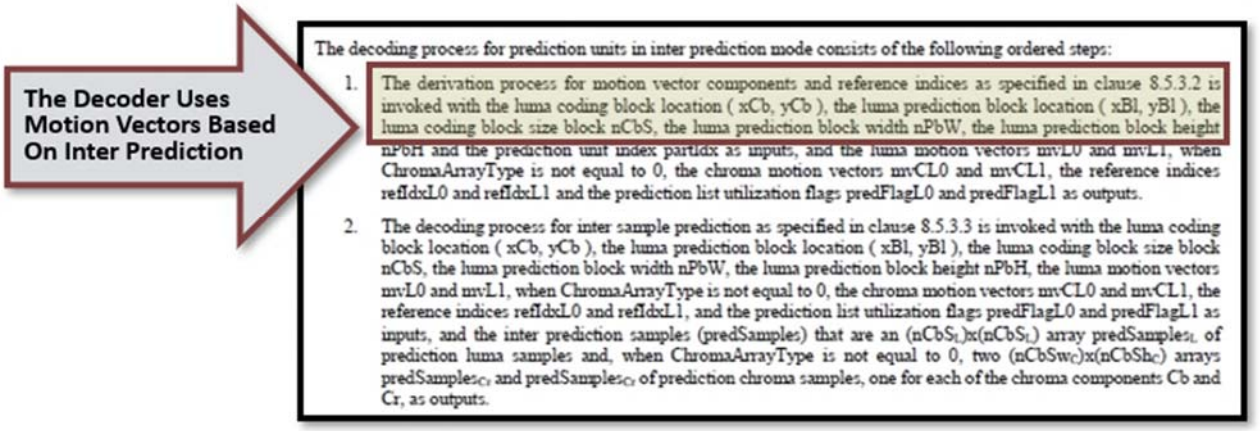


compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 0.7 (April 2015) (annotation added).

185. On information and belief, one or more of the NVIDIA '073 Products include a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers the motion vectors for the second frame. Further, HEVC documentation shows that

"motion vectors are used during the decoding process for prediction units in inter prediction mode."



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (April 2015) (annotation added).

186. On information and belief, one or more of the NVIDIA '073 Products include a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

187. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '073 Products in regular business operations.

188. On information and belief, the NVIDIA '073 Products are available to businesses and individuals throughout the United States.

189. On information and belief, the NVIDIA '073 Products are provided to businesses and individuals located in Delaware.

190. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '073 Patent by, among other things, making, using, offering for sale, and/or selling

technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the NVIDIA '073 Products.

191. By making, using, testing, offering for sale, and/or selling products for resampling a primitive from texture space to screen space, including but not limited to the NVIDIA '073 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '073 Patent, including at least claim 14 pursuant to 35 U.S.C. § 271(a).

192. On information and belief, NVIDIA also indirectly infringes the '073 Patent by actively inducing infringement under 35 USC § 271(b).

193. NVIDIA has had knowledge of the '073 Patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '073 Patent and knew of its infringement, including by way of this lawsuit.

194. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '073 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '073 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '073 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '073 Products that have the capability of operating in a manner that infringe one or more of the claims of the '073 patent, including at least claim 14, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '073 Products to utilize the products in a manner that directly infringe one or more

claims of the '073 patent.[25] By providing instruction and training to customers and end-users on how to use the NVIDIA '073 Products in a manner that directly infringes one or more claims of the '073 patent, including at least claim 14, NVIDIA specifically intended to induce infringement of the '073 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '073 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '073 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '073 patent, knowing that such use constitutes infringement of the '073 patent.

195. The '073 patent is well-known within the industry as demonstrated by multiple citations to the '073 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '073 patent without paying a reasonable royalty. NVIDIA is infringing the '073 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

196. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '073 patent.

[25] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

197. As a result of NVIDIA's infringement of the '073 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT III
INFRINGEMENT OF U.S. PATENT NO. 8,073,054

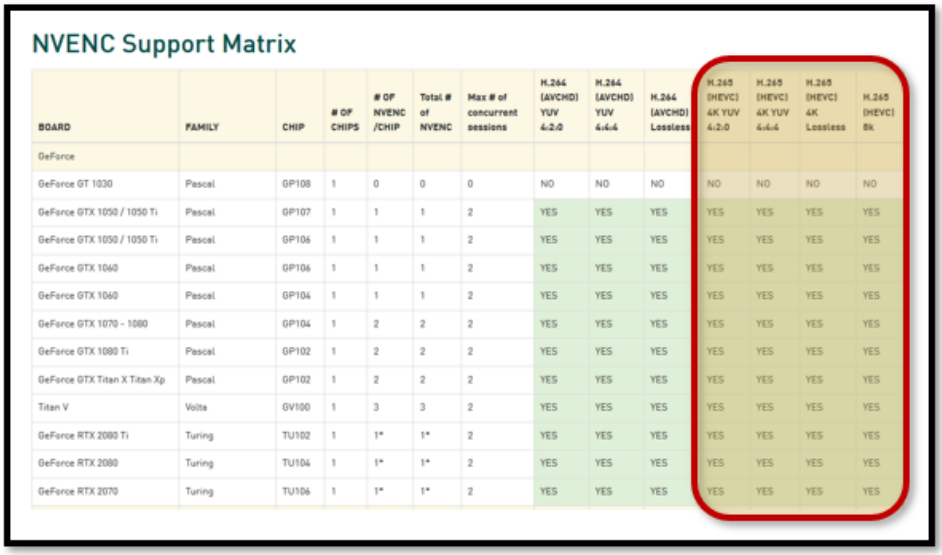
198. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

199. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for estimating a current motion vector for a group of pixels of an image.

200. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA Products containing H.265 encoding technology, including: GeForce GTX 1050 / 1050 Ti, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Tesla M4, Tesla M40, Tesla M6, Tesla M60, Tesla P4, Tesla P6, Tesla P40, Tesla P100, and Tesla V100 (collectively, the "NVIDIA '054A Product(s)").

201. Documentation from NVIDIA shows that the NVIDIA '054A Products perform a motion vector estimation method. NVIDIA '054A Products perform the method of encoding video content using High Efficiency Video Coding ("HEVC").

202. The NVIDIA '054A Products enable HEVC video encoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '054A Products comply with the HEVC standard for encoding data.

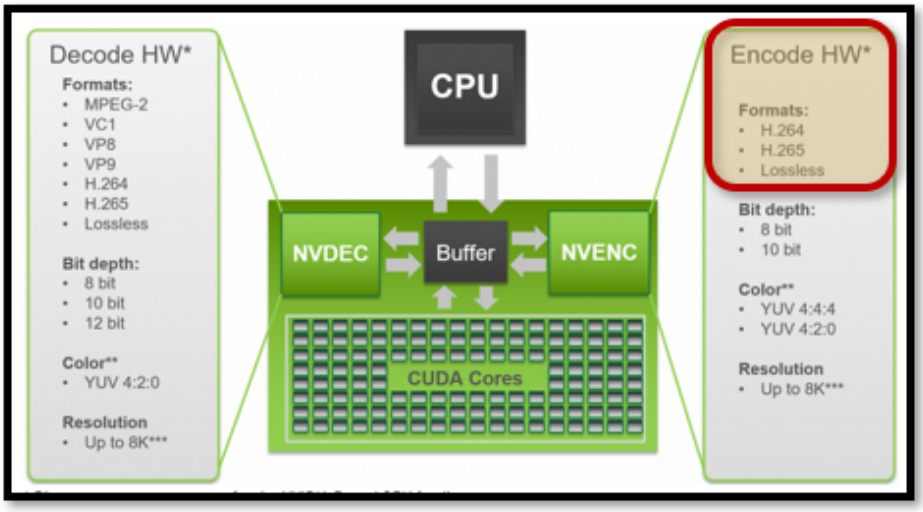


NVENC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVENC /CHIP	Total # of NVENC	Max # of concurrent sessions	H.264 (AVCHD) YUV 4:2:0	H.264 (AVCHD) YUV 4:4:4	H.264 (AVCHD) Lossless	H.265 (HEVC) 4K YUV 4:2:0	H.265 (HEVC) 4K YUV 4:4:4	H.265 (HEVC) 4K Lossless	H.265 (HEVC) 8k
GeForce													
GeForce GT 1030	Pascal	GP108	1	0	0	0	NO	NO	NO	NO	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP104	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1070 - 1080	Pascal	GP104	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1080 Ti	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
Titan V	Volta	GV100	1	3	3	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080 Ti	Turing	TU102	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC encoding in compliance with the HEVC standard).

203. The NVIDIA '054A Products contain hardware base encoding that meets the requirements of the HEVC standard. The below excerpt from NVIDIA documentation shows that H.265 encoding is supported by the "NVENC" (the NVIDIA Video Encoder).



NVIDIA Video Codec SDK, NVIDIA WEBSITE (last visited October 2018), *available at*: https://developer.nvidia.com/nvidia-video-codec-sdk (annotation showing support for the H.265 encoding standard).

204. NVIDIA documentation establishes that the NVIDIA '054A Products contain all the functionality required for the H.265 Main Profile and are complaint with the HEVC standard.

Feature	Description	Kepler GPUs	First generation Maxwell GPUs	Second generation Maxwell GPUs
H.264 Base, Main, High Profiles	YUV 4:2:0 Encoding.	✓	✓	✓
H.264 4:4:4 and Lossless	Regular YUV 4:4:4 and Lossless Encoding.	×	✓	✓
H.265 Main Profile	YUV 4:2:0 Encoding.	×	×	✓
H264 Motion Estimation (ME) only Mode	Capability to provide Macroblock level motion vectors and intra/inter modes	×	✓	✓
Support for ARGB Input	Capability to accept RGB input for limited color spaces.	✓	✓	✓

NVIDIA VIDEO ENCODER APPLICATION NOTE at 7 (November 2015) (emphasis added).

205. On information and belief, the NVIDIA '054A Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the NVIDIA Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by NVIDIA Products, a reference picture

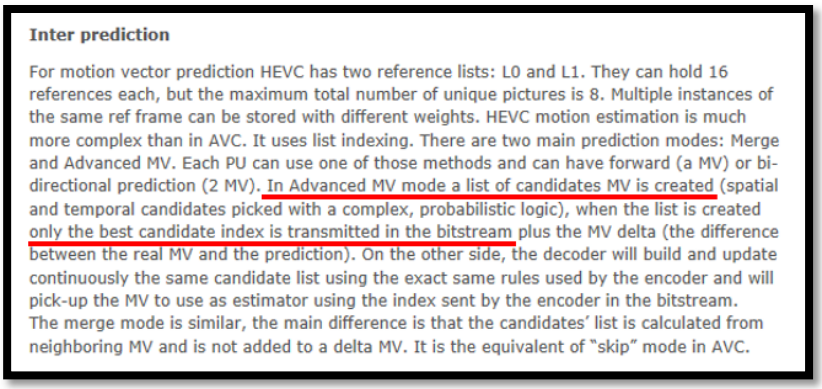
(first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

206. On information and belief, the NVIDIA '054A Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center. On information and belief, one or more of the NVIDIA '054A Products include technology for estimating a current motion vector for a group of pixels of an image

207. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '054A patent by, among other things, making, using, offering for sale, and/or selling technology for estimating a current motion vector for a group of pixels of an image, including but not limited to the NVIDIA '054A Products.

208. On information and belief, by complying with the HEVC standard, NVIDIA's devices – such as the NVIDIA '054A Products - necessarily infringe the '054A patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '054A patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '054A patent: "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

209. On information and belief, the NVIDIA '054A Products comprise functionality for generating a set of candidate motion vectors for a grouping of pixels (prediction unit). The HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, only the best candidate index is transmitted.



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

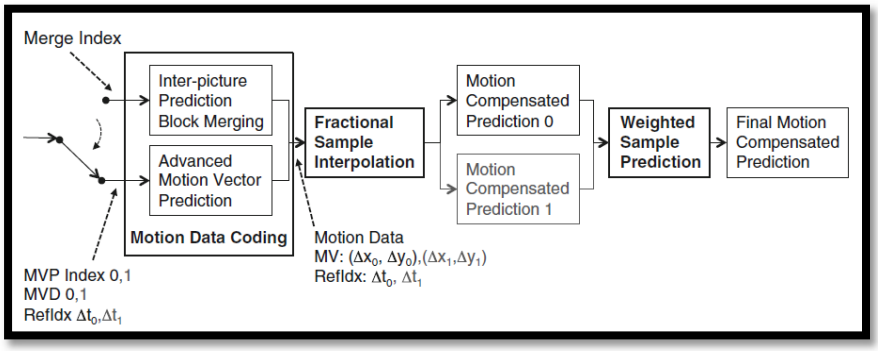
210. On information and belief, one or more of the NVIDIA '054A Products enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

> HEVC introduces a so-called merge mode, which sets all motion parameters of an inter picture predicted block equal to the parameters of a merge candidate [6]. The merge mode and the motion vector prediction process optionally allow a picture to reuse motion vectors of prior pictures for motion vector coding,

Frank Bossen, *et al*., *HEVC Complexity and Implementation Analysis,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY VOL. 22 NO. 12 at 1686 (December (2012).

211. On information and belief, the following block diagram illustrates the form of encoded video data received by the NVIDIA '054A Products. Specifically, the encoded video data received by the NVIDIA '054A Products is encoded using inter-picture prediction where the motion data of a block is correlated with neighboring blocks. To exploit this correlation, motion

data is not directly coded in the bitstream, but predictively coded based on neighboring motion data. Further, the NVIDIA '054A Products receive data that is encoded using advanced motion vector prediction where the best predictor for each motion block is signaled to the decoder. In addition, inter-prediction block merging derives all motion data of a block from the neighboring blocks.



Benjamin Bross, *et al*., *Inter-Picture Prediction in HEVC,* In HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (2014).

212. On information and belief, the NVIDIA '054A products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The NVIDIA '054A Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.

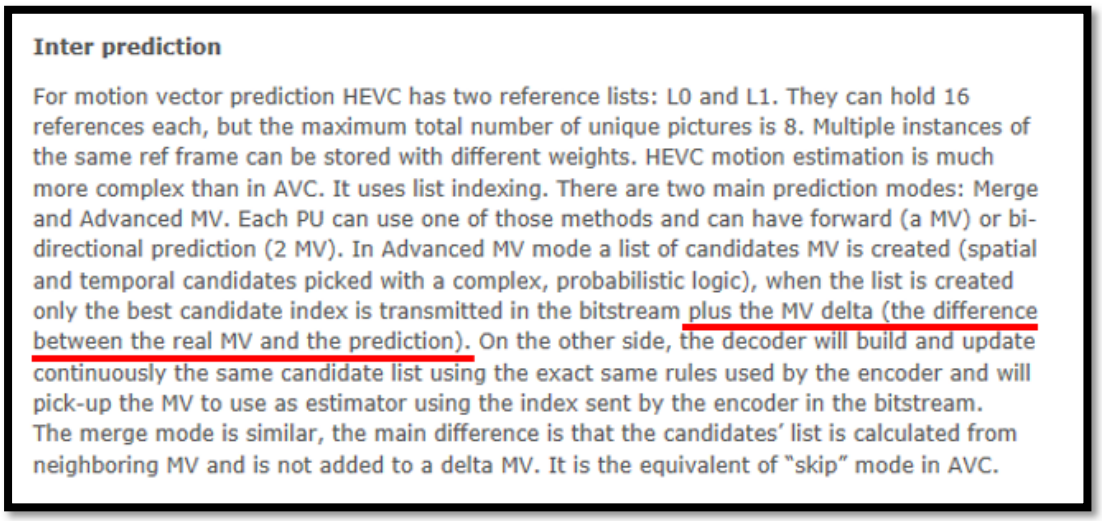
> three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in*

HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22 No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

213. On information and belief, one or more of the NVIDIA '054A Products include a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

214. On information and belief, the NVIDIA '054A Products contain functionality for generating match errors of the respective candidate motion vectors. The HEVC standard calculates match errors of respective candidate motion vectors. The match errors are referred to as the MV delta. The MV delta is the difference between the real MV and the candidate predication.



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

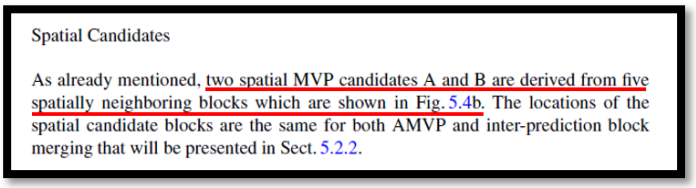
Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

215. On information and belief, any implementation of the HEVC standard would infringe the '054A patent as every implementation of the standard requires the elements in one or more claims of the '054A patent, including but not limited to claim 1, by way of example: a match error unit for calculating match errors of respective candidate motion vectors and calculating the

further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

216. On information and belief, one or more of the NVIDIA '054A Products include a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

217. On information and belief, the NVIDIA '054A Products select the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors. The first motion vector is labeled 'A' and the second motion vector is labeled 'B.'



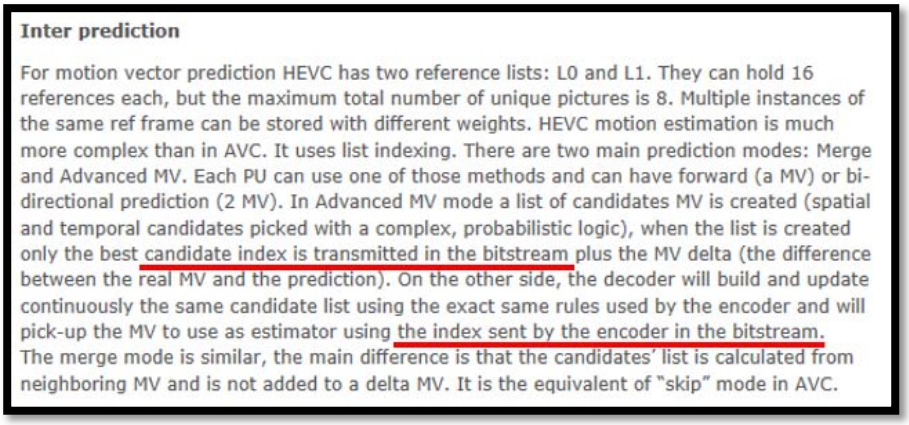
Spatial Candidates

As already mentioned, two spatial MVP candidates A and B are derived from five spatially neighboring blocks which are shown in Fig. 5.4b. The locations of the spatial candidate blocks are the same for both AMVP and inter-prediction block merging that will be presented in Sect. 5.2.2.

Gary Sullivan, *et al*., HIGH EFFICIENCY VIDEO CODING (HEVC) ALGORITHMS AND ARCHITECTURES at 117 (2014) (emphasis added).

218. Further, the NVIDIA '054A Products perform motion vector "competition / weighted sample prediction" by comparing the match errors of the candidate motion vectors. The match errors generated by the NVIDIA '054A Products comprise the difference value between the

second motion vector and the first motion vector. Documentation of the encoding process states that the encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

219. On information and belief, the NVIDIA '054A Products calculate the square of the difference between two corresponding pixels of the spatial position of the candidate block where the motion vector is located and the spatial position where the reference motion vector is located. As a result, this value is used to assess the similarity, or the matching degree, of a candidate block. Thus, in order to obtain the best matching vector, the NVIDIA '054A Products apply a penalty value to every candidate block with a different motion vector (*MVx, MVy*) within the search window defined by the search range in the reference frame. Finally, a candidate block with the minimum penalty value will be denoted as the best matching block and used to calculate the best motion vector from the candidate motion vectors. The below excerpt from an article discussing the selection of a best motion vector describes that the selection of a motion vector is based on the position of the motion vector.

> The entire ME process is made up of three coarse-to-fine procedures, namely, MV prediction, integer-pixel ME and fractional-pixel ME. First, MV prediction predicts the start search position for the following motion search by utilizing the neighboring motion information. In HEVC, Advanced Motion Vector Prediction (AMVP), a new and effective technology that predicts the starting search position by referencing the motion vector (MV) information of spatial and temporal motion vector candidates, is adopted, which derives several most probable candidates based on data from adjacent PBs and the reference picture. The displacement between the starting search position and the current coding PU is called a predictive motion vector (PMV). HEVC also introduces a merge mode to derive the motion information from spatially or temporally neighboring blocks [1].

Yongfei Zhang, Chao Zhang, and Rui Fan, *Fast Motion Estimation in HEVC Inter Coding: An Overview of Recent Advances*, PROCEEDINGS, APSIPA ANNUAL SUMMIT AND CONFERENCE 2018 at 1 (November 2018) (emphasis added).

220. On information and belief, one or more of the NVIDIA '054A Products include a motion estimation unit that calculates the further candidate motion vector on the basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different. Specifically, the HEVC standard arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process (see the red box in the below diagram).

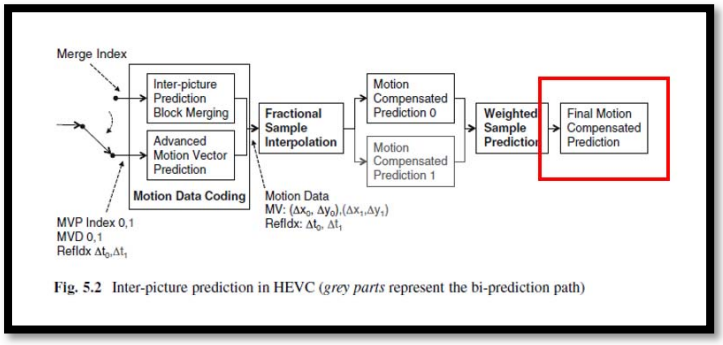


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

221. On information and belief, one or more of the NVIDIA '054A Products include a motion estimation unit that arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

222. On information and belief, the NVIDIA '054A Products are available to businesses and individuals throughout the United States.

223. On information and belief, the NVIDIA '054A Products are provided to businesses and individuals located in the State of Delaware.

224. By making, using, testing, offering for sale, and/or selling products and services for estimating a current motion vector for a group of pixels of an image, including but not limited to the NVIDIA '054A Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '054A Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

225. On information and belief, NVIDIA also indirectly infringes the '054A Patent by actively inducing infringement under 35 USC § 271(b).

226. NVIDIA has had knowledge of the '054A Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '054A Patent and knew of its infringement, including by way of this lawsuit.

227. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '054A Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '054A patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge

of the '054A patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '054A Products that have the capability of operating in a manner that infringe one or more of the claims of the '054A patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '054A Products to utilize the products in a manner that directly infringe one or more claims of the '054A patent.[26] By providing instruction and training to customers and end-users on how to use the NVIDIA '054A Products in a manner that directly infringes one or more claims of the '054A patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '054A patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '054A Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '054A patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '054A patent, knowing that such use constitutes infringement of the '054A patent.

228. The '054A patent is well-known within the industry as demonstrated by multiple citations to the '054A patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '054A

[26] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015); *Release 387 Graphics Drivers for Windows, Version 388.71*, RELEASE NOTES (Dec. 20, 2017).

patent without paying a reasonable royalty. NVIDIA is infringing the '054A patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

229. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '054A patent.

230. As a result of NVIDIA's infringement of the '054A patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

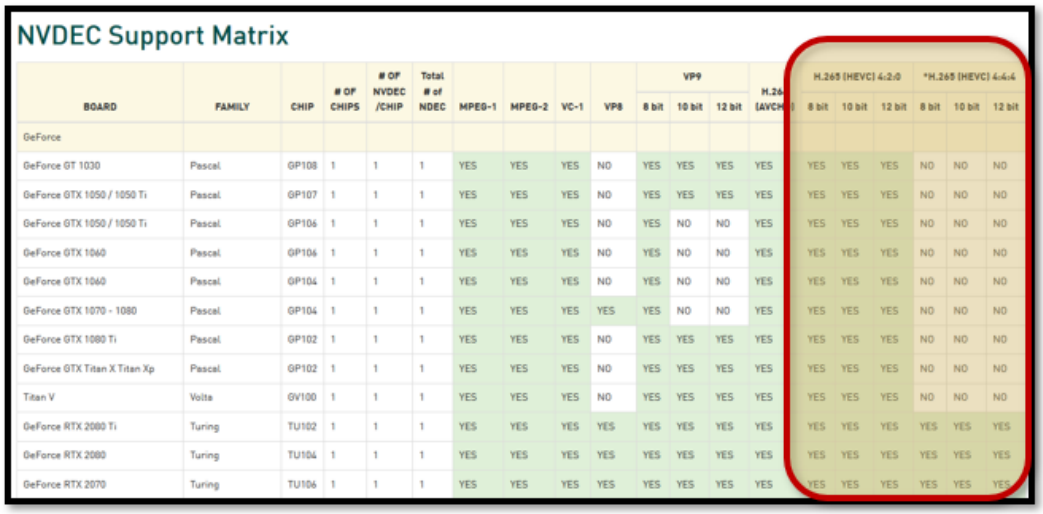
COUNT IV
INFRINGEMENT OF U.S. PATENT NO. 6,774,918

231. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

232. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for image processing.

233. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA products that support overlay functionality, including the following products: GeForce GT 1030, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000 / P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 750 GeForce GTX 950 - 960, Quadro M2000, Quadro P620, Quadro P1000, Quadro P6000, and Quadro GP100 (collectively, the "NVIDIA '918 Product(s)").

234. The NVIDIA '918 Products enable HEVC video decoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '918 Products comply with the HEVC standard for decoding data.

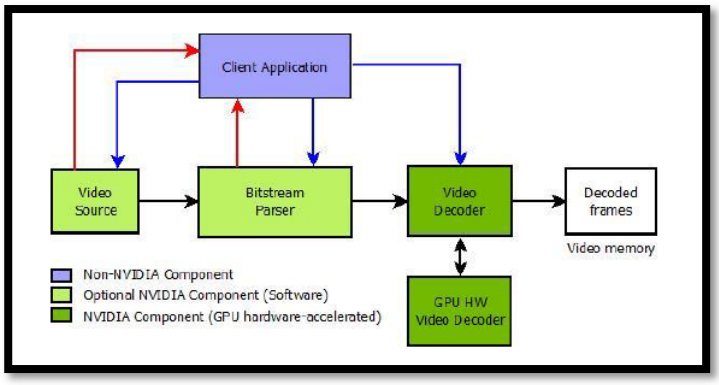


NVDEC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVDEC /CHIP	Total # of NDEC	MPEG-1	MPEG-2	VC-1	VP8	VP9			H.264 (AVCHD)	H.265 (HEVC) 4:2:0			*H.265 (HEVC) 4:4:4		
										8 bit	10 bit	12 bit		8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
GeForce																			
GeForce GT 1030	Pascal	GP108	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP104	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1070 - 1080	Pascal	GP104	1	1	1	YES	YES	YES	YES	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1080 Ti	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
Titan V	Volta	GV100	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce RTX 2080 Ti	Turing	TU102	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC decoding in compliance with the HEVC standard).

235. The NVIDIA '918 Products comply with the HEVC standard in decoding video data. The NVIDIA document shows the NVDEC interface for decoding video data.



NVIDIA Video Decoder (NVDEC) Interface, NVIDIA PROGRAMMING GUIDE at 4 (June 2016) (annotations added) (showing the functionality for decoding video data for on-screen display).

236. On information and belief, the NVIDIA '918 Products use two types of prediction methods for decoding video data: inter prediction and intra prediction. Inter prediction utilizes

motion vectors as well as an offset center and creates a list of possible motion vectors (MV) for the search area. The HEVC Specification (*e.g., High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (April 2015)) sets forth the standard that is followed by HEVC compliant devices and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the NVIDIA Products perform a method for decoding a video signal using motion vectors when performing encoding of H.265/HEVC video data. For example, the NVIDIA Products contain functionality for decoding a video signal using motion vectors and motion estimation.

237. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '918 Products - necessarily infringe the '918 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '918 patent, including but not limited to claim 18. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '918 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

238. On information and belief, the NVIDIA '918 Products receive a bitstream in which the data is segmented into Network Abstraction Layer ("NAL") Units. NAL Units are segments

of data that can include video data and overlay data (such as captions and overlay images). The NVIDIA Products support the receipt of VCL and non-VCL NAL units. The VCL NAL units contain the data that represents the values of the samples in the video pictures, and the non-VCL NAL units contain any associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

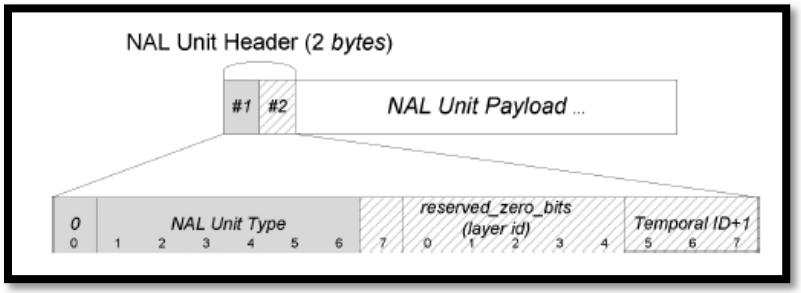
Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

239. On information and belief, the VCL NAL Units contain segments of data which are used to generate an image (*e.g.*, HEVC image) on a display device. Each VCL NAL Unit comprises a discrete number of bites which make up a segment. The following excerpt from the HEVC specification describes the NAL unit as being a segment with a "demarcation" setting forth where the segment ends and begins.

> NumBytesInNalUnit specifies the size of the NAL unit in bytes. This value is required for decoding of the NAL unit. Some form of demarcation of NAL unit boundaries is necessary to enable inference of NumBytesInNalUnit. One such demarcation method is specified in Annex B for the byte stream format. Other methods of demarcation may be specified outside of this Specification.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 7.4.2.1 (February 2018) (emphasis added).

240. On information and belief, VCL NAL Units comprise discrete video data that ends. It is between the receipt of VCL NAL Units that the overlay data (Non-VCL NAL Unit) data is received by the NVIDIA Products.



Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, VOL.* 22, NO. 12 at 1875 (December 2012).

241. On information and belief, the NVIDIA '918 Products are available to businesses and individuals throughout the United States.

242. On information and belief, the NVIDIA '918 Products are provided to businesses and individuals located in the State of Delaware.

243. On information and belief, the HEVC bitstream structure is comprised of discreet data. In the gaps between the receipt by the NVIDIA '918 Products of VCL NAL Units Non-VCL NAL Units are received by the NVIDIA Products' decoder.

> An HEVC bitstream consists of a number of access units, each including coded data associated with a picture that has a distinct capturing or presentation time. Each access unit is divided into NAL units, including one or more VCL NAL units (i.e., coded slice NAL units) and zero or more non-VCL NAL units, e.g., parameter set NAL units or supplemental enhancement information (SEI) NAL units. Each NAL unit includes an NAL unit header and an NAL unit payload. Information in the NAL unit header can be (conveniently) accessed by media gateways, also known as media aware network elements (MANEs), for intelligent, media aware operations on the stream, such as stream adaptation.

Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, VOL.* 22, NO. 12 at 1873 (December 2012).

244. On information and belief, Non-VCL NAL unit types include data such as supplemental enhancement information that is used to create overlays for display on the device.

Table 2.2 The 32 HEVC non-VCL NAL unit types

Non-VCL NAL unit types			
Parameter sets	32	VPS_NUT	Video parameter set
	33	SPS_NUT	Sequence parameter set
	34	PPS_NUT	Picture parameter set
Delimiters	35	AUD_NUT	Access unit delimiter
	36	EOS_NUT	End of sequence
	37	EOB_NUT	End of bitstream
Filler data	38	FD_NUT	Filler data
Supplemental enhancement information (SEI)	39	PREFIX_SEI_NUT	
	40	SUFFIX_SEI_NUT	
Reserved	41–47	RSV	
Unspecified	48–63	UNSPEC	

Gary J. Sullivan et al, HIGH EFFICIENCY VIDEO CODING (HEVC) at 29 (September 2014).

245. On information and belief, Non-VCL NAL Units include supplemental enhancement information ("SEI") messages. The SEI data that is received contains overlay information that can be combined with the image data that has already been received.

sei_message( ) {	Descriptor
payloadType = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadType += 255	
}	
last_payload_type_byte	u(8)
payloadType += last_payload_type_byte	
payloadSize = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadSize += 255	
}	
last_payload_size_byte	u(8)
payloadSize += last_payload_size_byte	
sei_payload(payloadType, payloadSize)	
}	

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.3.5 (February 2018).

246. On information and belief, the NVIDIA '918 Products combine the VCL NAL Unit and Non-VCL NAL Unit information to create images that contain overlay information.

> The NAL units are decoded by the decoder to produce the decoded pictures that are output from the decoder. Both the encoder and decoder store pictures in a decoded picture buffer (DPB). This buffer is mainly used for storing pictures so that previously coded pictures can be used to generate prediction signals to use when coding other pictures. These stored pictures are called reference pictures. . . . There are two classes of NAL units in HEVC—video coding layer (VCL) NAL units and non-VCL NAL units. Each VCL NAL unit carries one slice segment of coded picture data while the non-VCL NAL units contain control information that

> typically relates to multiple coded pictures. One coded picture, together with the non-VCL NAL units that are associated with the coded picture, is called an HEVC access unit.

Gary J. Sullivan et al, HIGH EFFICIENCY VIDEO CODING (HEVC) at 14-15 (September 2014) (emphasis added).

247. By making, using, testing, offering for sale, and/or selling products for downloading on-screen display (OSD) data for generating an image on a display device., including but not limited to the NVIDIA '918 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '918 Patent, including at least claim 18 pursuant to 35 U.S.C. § 271(a).

248. On information and belief, NVIDIA also indirectly infringes the '918 Patent by actively inducing infringement under 35 USC § 271(b).

249. On information and belief, NVIDIA has had knowledge of the '918 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '918 Patent and knew of its infringement, including by way of this lawsuit.

250. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '918 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '918 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '918 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '918 Products that have the capability of operating in a manner that infringe one or more of the claims of the '918 patent, including at least claim 18, and

NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '918 Products to utilize the products in a manner that directly infringe one or more claims of the '918 patent.[27] By providing instruction and training to customers and end-users on how to use the NVIDIA '918 Products in a manner that directly infringes one or more claims of the '918 patent, including at least claim 18, NVIDIA specifically intended to induce infringement of the '918 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '918 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '918 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '918 patent, knowing that such use constitutes infringement of the '918 patent.

251. The '918 patent is well-known within the industry as demonstrated by multiple citations to the '918 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '918 patent without paying a reasonable royalty. NVIDIA is infringing the '918 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

[27] *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015); *Release 396 Graphics Drivers for Windows, Version 399.07*, RELEASE NOTES (Aug. 27, 2018); *Release 390 Graphics Drivers for Windows, Version 390.77*, RELEASE NOTES (Jan. 29, 2018).

252. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '918 patent.

253. As a result of NVIDIA's infringement of the '918 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT V
INFRINGEMENT OF U.S. PATENT NO. 8,184,689

254. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

255. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for encoding and decoding video data.

256. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA processing units, including: GeForce GTX Titan Z, GeForce GTX Titan Black, GeForce GTX Titan, GeForce GTX 780 Ti, GeForce GTX 780, GeForce GT 640 (GDDR5), GeForce GT 630 v2, GeForce GT 730, GeForce GT 720, GeForce GT 710, GeForce GT 740M (64-bit, DDR3), GeForce GT 920M, GeForce GTX 750 Ti, GeForce GTX 750, GeForce GTX 960M, GeForce GTX 950M, GeForce 940M, GeForce 930M, GeForce GTX 860M, GeForce GTX 850M, GeForce 845M, GeForce 840M, GeForce 830M, GeForce GTX 870M, Titan Xp, Titan X, GeForce GTX 1080 Ti, GTX 1080, GTX 1070 Ti, GTX 1070, GTX 1060, GTX 1050 Ti, GTX 1050, GT 1030, MX150, Titan V, GeForce RTX 2080 Ti, RTX 2080, RTX 2070, Quadro K6000, Quadro K5200, Quadro M6000 24GB, Quadro M6000, Quadro M5000, Quadro M4000, Quadro M2000, Quadro M5500, Quadro M5000M, Quadro M4000M, Quadro M3000M, Quadro GP100, Quadro P6000,

Quadro P5000, Quadro P4000, Quadro P2000, Quadro P1000, Quadro P600, Quadro P400, Quadro P5000 (Mobile), Quadro P4000 (Mobile), Quadro P3000 (Mobile), Quadro GV100, Quadro RTX 8000, Quadro RTX 6000, and Quadro RTX 5000 (collectively, the "NVIDIA '689 Product(s)").

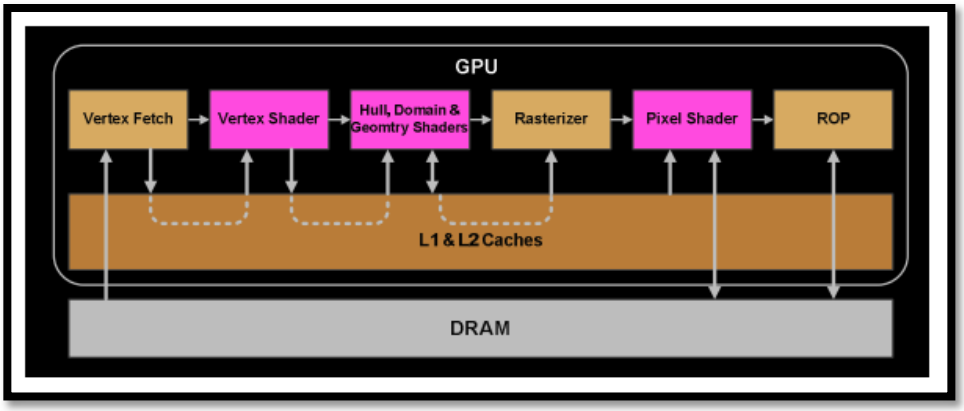
257. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '689 Products in regular business operations.

258. On information and belief, one or more of the NVIDIA '689 Products include technology for encoding and decoding video data.

16. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '689 patent by, among other things, making, using, offering for sale, and/or selling technology for encoding and decoding video data, including but not limited to the NVIDIA '689 Products.

259. On information and belief, one or more of the NVIDIA '689 Products reduce processing time and power consumption associated with encoding and decoding video stream data by reducing off-chip memory accesses through using simultaneous encoded/decoded images as a reference image for encoding/decoding at least one of the other simultaneously encoded/decoded images.

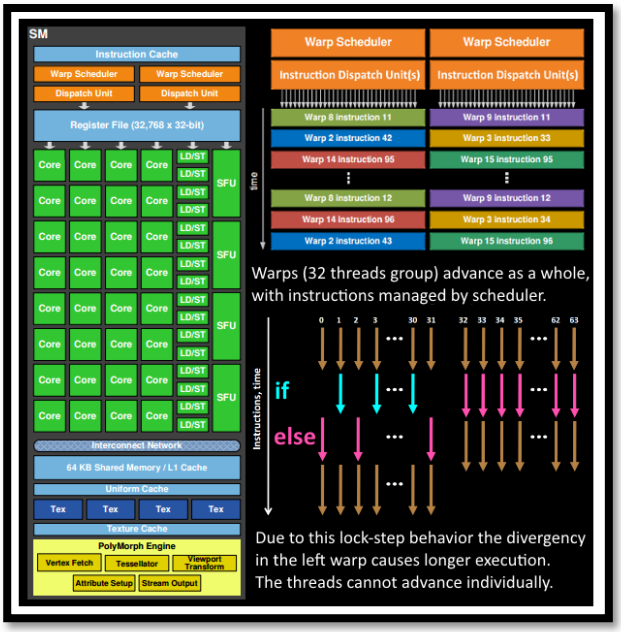
260. On information and belief, the NVIDIA'689 Products perform the step of providing a subset of image data stored in the second memory in the first memory. Specifically, the NVIDIA Products include memory in the form of cached memory, solid state storage, and on chip memory.



Chris Kubisch, *Life of a Triangle – NVIDIA's Logical Pipeline*, NVIDIA DEVELOPER WEBSITE (March 16, 2015) ("This is the key concept how GPUs overcome latency of memory reads, they simply switch out groups of active threads. To make this switching very fast, all threads managed by the scheduler have their own registers in the register-file. The more registers a shader program needs, the less threads/warps have space. The less warps we can switch between, the less useful work we can do while waiting for instructions to complete (foremost memory fetches).").

261. On information and belief, one or more of the NVIDIA '689 Products perform a method for encoding and decoding a video stream, including a plurality of images in a video processing apparatus having a processing unit coupled to a first memory, further comprising a second memory.

262. NVIDIA documentation relating to the NVIDIA '689 Products shows structures in the NVIDIA '689 Product's functionality wherein an external motion vector field can be retrieved from an external unit. For example, the NVIDIA '689 Products include memory that is in the form of cached memory, solid state storage and on chip memory.



Chris Kubisch, *Life of a Triangle – NVIDIA's Logical Pipeline*, NVIDIA DEVELOPER WEBSITE (March 16, 2015) ("The GPU is partitioned into multiple Graphics Processing Cluster), each has multiple SMs (Streaming Multiprocessor) and one Raster Engine**.** There is lots of interconnects in this process, most notably a Crossbar that allows work migration across GPCs or other functional units like ROP (render output unit) subsystems.").

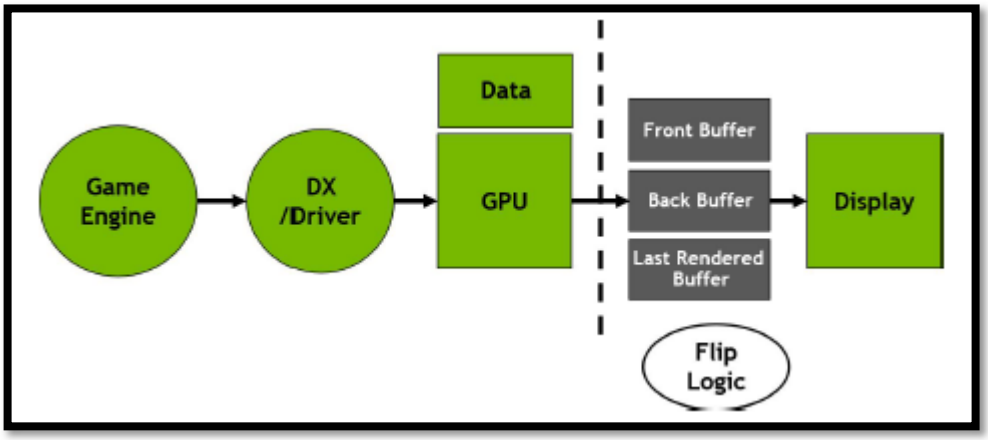
263. On information and belief, one or more of the NVIDIA '689 Products perform a method for encoding and decoding a video stream comprising providing a subset of image data stored in the second memory in the first memory.

> The SM is a highly parallel multiprocessor that schedules warps (groups of 32 threads) to CUDA cores and other execution units within the SM. The SM is one of the most important hardware units within the GPU; almost all operations flow through the SM at some point in the rendering pipeline. With 20 SMs, the GeForce GTX 1080 ships with a total of 2560 CUDA cores and 160 texture units.

NVIDIA GeForce GTX 1080, NVIDIA WHITEPAPER at 8 (2016).

264. On information and belief, one or more of the NVIDIA '689 Products perform a method for encoding and decoding a video stream comprising simultaneous encoding/decoding of more than one image of the video stream, by accessing said subset, wherein the simultaneously encoding/decoding is performed by access sharing to at least one image.

265. On information and belief, the NVIDIA '689 Products support Fast Sync which contains a Front Buffer and Back Buffer.



NVIDIA GeForce GTX 1080, NVIDIA WHITEPAPER at 36 (2016) ("One way to think about Fast Sync is to imagine that three areas in the frame buffer have been allocated in three different ways. The first two buffers are very similar to double-buffered VSYNC in classic GPU pipelines. The Front Buffer (FB) is the buffer scanned out to the display. It is a fully rendered surface. The Back Buffer (BB) is the buffer that is currently being rendered to and it can't be scanned out until it is completed.")

17. On information and belief, the NVIDIA '689 Products are available to businesses and individuals throughout the United States.

18. On information and belief, the NVIDIA '689 Products are provided to businesses and individuals located in Delaware.

19. By making, using, testing, offering for sale, and/or selling products and services for encoding and decoding video data, including but not limited to the NVIDIA '689 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '689 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

266. On information and belief, NVIDIA also indirectly infringes the '689 patent by actively inducing infringement under 35 USC § 271(b).

267. NVIDIA has had knowledge of the '689 patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '689 patent and knew of its infringement, including by way of this lawsuit.

268. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '689 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '689 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '689 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '689 Products that have the capability of operating in a manner that infringe one or more of the claims of the '689 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '689 Products to utilize the products in a manner that directly infringe one or more claims of the '689 patent.[28] By providing instruction and training to customers and end-users on how to use the NVIDIA '689 Products in a manner that directly infringes one or more claims of the '689 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '689 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '689 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to

[28] *See, e.g.*, *Release 410 Quadro, Tesla, and Notebook Drivers for Windows, Version 411.81*, RELEASE NOTES (Oct. 23, 2018) NVIDIA *GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

infringe the '689 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '689 patent, knowing that such use constitutes infringement of the '689 patent.

269. The '689 patent is well-known within the industry as demonstrated by multiple citations to the '689 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '689 patent without paying a reasonable royalty. NVIDIA is infringing the '689 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

270. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '689 patent.

271. As a result of NVIDIA's infringement of the '689 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT VI
INFRINGEMENT OF U.S. PATENT NO. 6,996,177

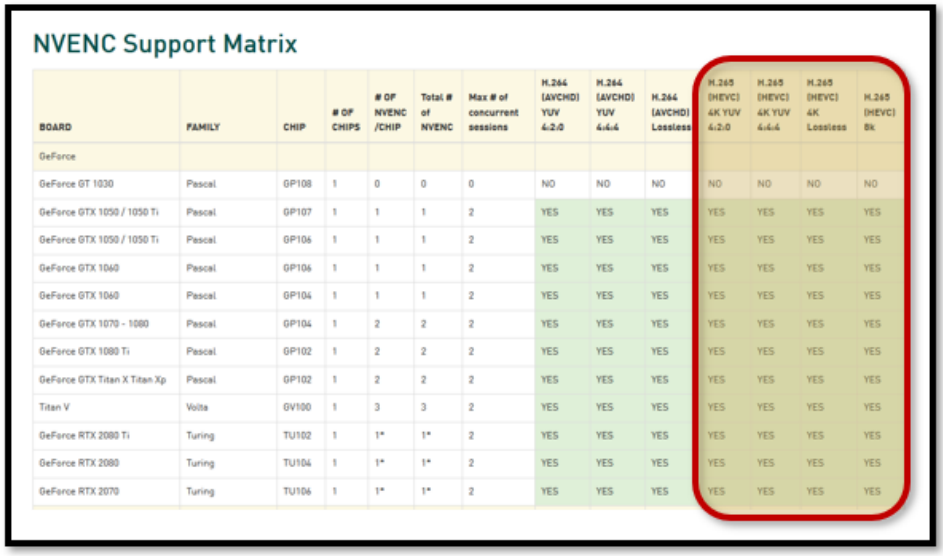
272. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

273. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion estimation.

274. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA Products containing H.265 encoding technology, including: GeForce GTX 1050 / 1050 Ti,

GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Tesla M4, Tesla M40, Tesla M6, and Tesla M60 (collectively, the "NVIDIA '177 Product(s)").

275. The NVIDIA '177 Products enable HEVC video encoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '177 Products comply with the HEVC standard for encoding data.

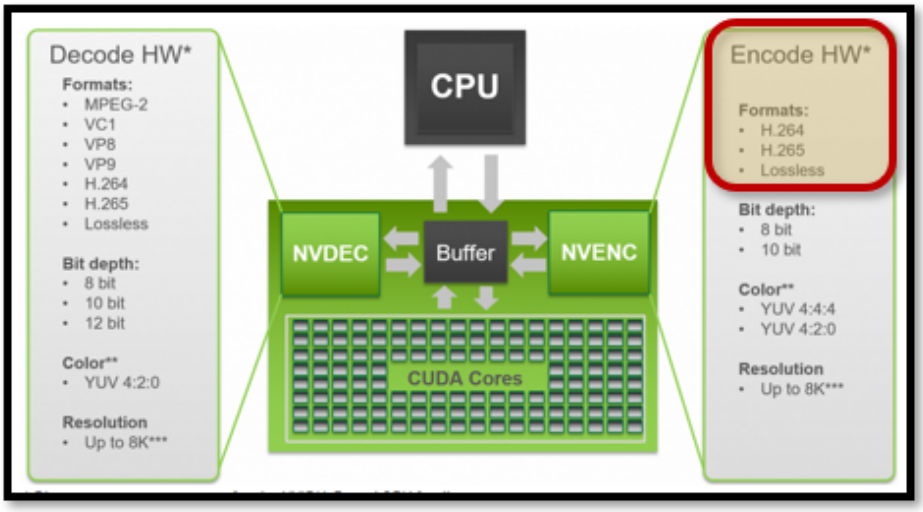


NVENC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVENC /CHIP	Total # of NVENC	Max # of concurrent sessions	H.264 (AVCHD) YUV 4:2:0	H.264 (AVCHD) YUV 4:4:4	H.264 (AVCHD) Lossless	H.265 (HEVC) 4K YUV 4:2:0	H.265 (HEVC) 4K YUV 4:4:4	H.265 (HEVC) 4K Lossless	H.265 (HEVC) 8K
GeForce													
GeForce GT 1030	Pascal	GP108	1	0	0	0	NO	NO	NO	NO	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP104	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1070 - 1080	Pascal	GP104	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1080 Ti	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
Titan V	Volta	GV100	1	3	3	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080 Ti	Turing	TU102	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC encoding in compliance with the HEVC standard).

276. The NVIDIA '177 Products contain hardware base encoding that meets the requirements of the HEVC standard. The below excerpt from NVIDIA documentation shows that H.265 encoding is supported by the "NVENC" (the NVIDIA Video Encoder).



NVIDIA Video Codec SDK, NVIDIA WEBSITE (last visited October 2018), *available at*: https://developer.nvidia.com/nvidia-video-codec-sdk (annotation showing support for the H.265 encoding standard).

277. NVIDIA documentation establishes that the NVIDIA '177 Products contain all the functionality required for the H.265 Main Profile and are complaint with the HEVC standard.

Feature	Description	Kepler GPUs	First generation Maxwell GPUs	Second generation Maxwell GPUs
H.264 Base, Main, High Profiles	YUV 4:2:0 Encoding.	✓	✓	✓
H.264 4:4:4 and Lossless	Regular YUV 4:4:4 and Lossless Encoding.	×	✓	✓
H.265 Main Profile	YUV 4:2:0 Encoding.	×	×	✓
H264 Motion Estimation (ME) only Mode	Capability to provide Macroblock level motion vectors and intra/inter modes	×	✓	✓
Support for ARGB Input	Capability to accept RGB input for limited color spaces.	✓	✓	✓

NVIDIA VIDEO ENCODER APPLICATION NOTE at 7 (November 2015) (emphasis added).

278. Documentation from NVIDIA shows that the NVIDIA '177 Products perform a motion vector estimation method.

279. On information and belief, the NVIDIA '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to the determine block-based motion vectors.

280. On information and belief, the NVIDIA '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center.

281. On information and belief, the NVIDIA '177 Products use a Prediction Unit matching method wherein the motion vector represents the displacement between the current Prediction Unit in the current frame and the matching Prediction Unit in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

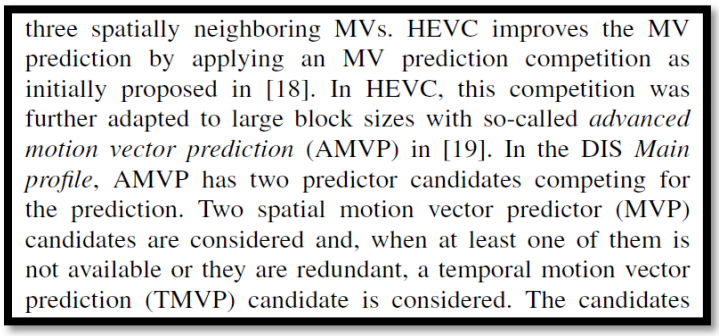
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

282. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '177 Products - necessarily infringe the '177 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '177 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '177 patent: "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

283. On information and belief, one or more of the NVIDIA '177 Products include technology for motion estimation and motion-compensated picture signal processing.

284. On information and belief, one or more of the NVIDIA '177 Products include technology for estimating a current motion vector for a group of pixels of an image.

285. On information and belief, the NVIDIA '177 Products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The NVIDIA '177 Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.



three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC,* IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. *22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

286. On information and belief, the NVIDIA '177 Products utilize a motion vector selection process wherein the candidate motion vectors are constructed into an index and then the motion vectors are compared. "In AMVP, the motion vector selection process is composed by two steps in encoder implementation. The first step is the motion vector candidate set construction process and the second step is the best motion vector selection step. In the first step, the motion vector candidate set is organized by selecting the motion vectors spatially and temporally." Gwo-

Long Li, Chuen-Ching Wang, and Kuang-Hung Chiang, *An Efficient Motion Vector Prediction Method for Avoiding AMVP Data Dependency For HEVC*, 2014 IEEE INTERNATIONAL CONFERENCE ON ACOUSTIC, SPEECH AND SIGNAL PROCESSING (ICASSP) at 13 (2014).

287. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '177 Products in regular business operations.

288. On information and belief, the NVIDIA '177 Products are available to businesses and individuals throughout the United States.

289. On information and belief, the NVIDIA '177 Products are provided to businesses and individuals located in the State of Delaware.

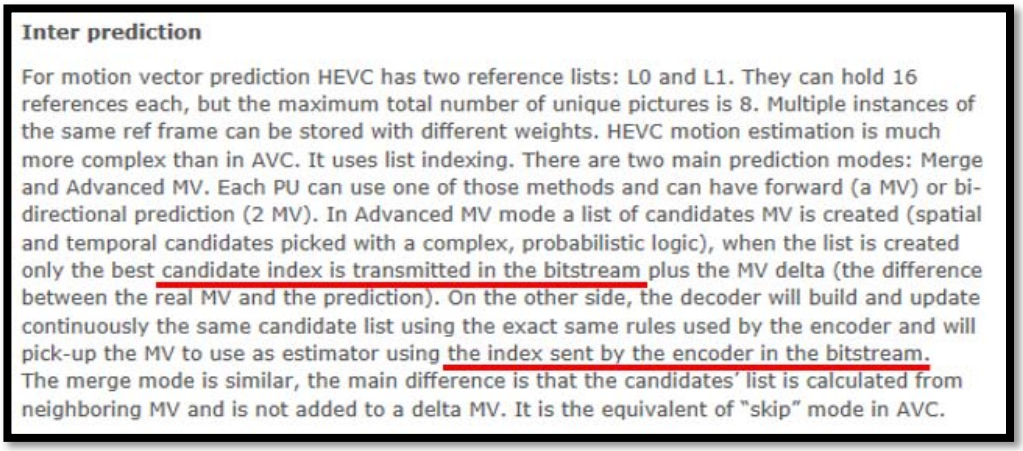
290. The HEVC Standard provides details regarding what would be required for a compliant HEVC encoder—e.g., the standard uses terms such as "encoding," "coding," "compressing," and other similar terms to describe the encoding process.

291. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '177 patent by, among other things, making, using, offering for sale, and/or selling products and services for motion estimation and motion-compensated picture signal processing.

292. On information and belief, the NVIDIA '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to determine block-based motion vectors. The NVIDIA '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image.

293. On information and belief, the NVIDIA '177 Products determine at least a most frequently occurring block-based motion vector. The NVIDIA '177 Products contain functionality wherein the motion vector prediction performed includes the ability to transmit in the bitstream the candidate index of motion vectors. Documentation of the encoding process states that the

encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

294. On information and belief, any implementation of the HEVC standard would infringe the '177 patent as every possible implementation of the standard requires: compliant devices to carry out a global motion vector estimation process using the most frequently occurring block-based motion vectors. This process of vector candidate selection allows the NVIDIA '177 Products to obtain a global motion vector. Specifically, the HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, if there are two spatial motion vectors that are identical, that is determined to be the most frequently occurring block-based motion vector and the frequently occurring spatial motion vector and temporal motion vector candidate are used to generate the global motion vector. "In HEVC, this competition was further adapted to large block sizes with so-called advanced motion vector prediction (AMVP). In the DIS Main profile, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion

vector prediction (TMVP) candidate is considered." Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 (December 2012).

295. On information and belief, the NVIDIA '177 Products apply a global motion vector as a candidate vector to the block-based motion vector estimation process. Specially, the NVIDIA '177 Products calculate the global motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process diagram below (as shown in the below figure) and applied to the block-based motion vector estimation process.

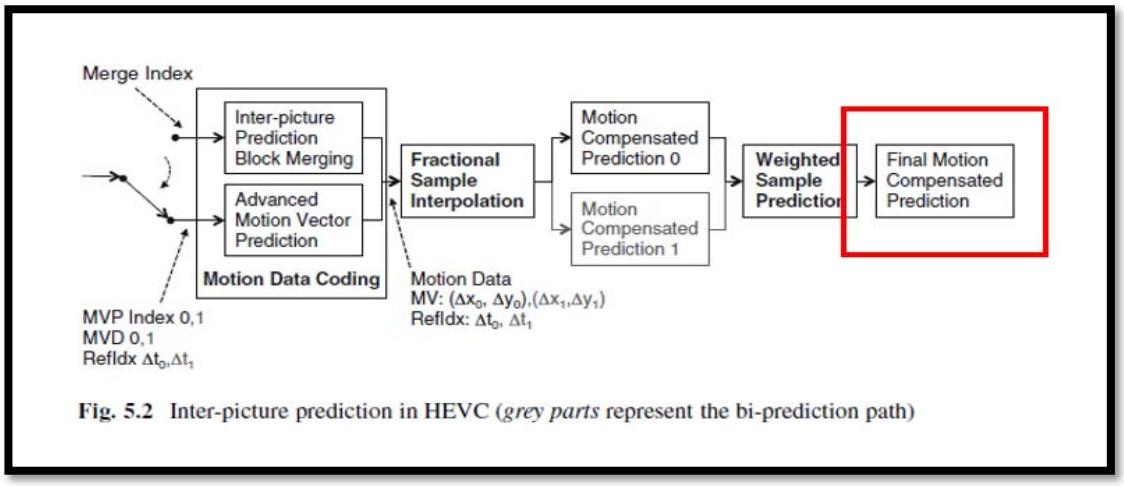


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

296. Further, the NVIDIA '177 Products enable AMVP wherein several of the most probable candidate vectors based on data from adjacent prediction blocks are used to create a global estimation vector and that vector is applied to the block-based motion estimation functionality.

> Motion vector signaling: Advanced motion vector prediction (AMVP) is used, including derivation of several most probable candidates based on data from adjacent PBs and the reference picture. A "merge" mode for MV coding can be

> also used, allowing the inheritance of MVs from neighboring PBs. Moreover, compared to H.264/MPEG-4 AVC, improved "skipped" and "direct" motion inference are also specified.

Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, PRE-PUBLICATION DRAFT, TO APPEAR IN IEEE TRANS. ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY at 3 (December 2012) (emphasis added).

297. On information and belief, the NVIDIA '177 Products are available to businesses and individuals throughout the United States.

298. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '177 Products in regular business operations.

299. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '177 Patent by, among other things, making, using, offering for sale, and/or selling technology for determining motion vectors that are each assigned to individual image regions, including but not limited to the NVIDIA '177 Products.

300. On information and belief, the NVIDIA '177 Products are provided to businesses and individuals located in Delaware.

301. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the NVIDIA '177 Products, NVIDIA has injured Dynamic Data and is liable for directly infringing one or more claims of the '177 Patent, including at least claim 1, pursuant to 35 U.S.C. § 271(a).

302. On information and belief, NVIDIA also indirectly infringes the '177 Patent by actively inducing infringement under 35 USC § 271(b).

303. On information and belief, NVIDIA has had knowledge of the '177 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '177 Patent and knew of its infringement, including by way of this lawsuit.

304. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '177 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '177 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '177 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '177 Products that have the capability of operating in a manner that infringe one or more of the claims of the '177 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '177 Products to utilize the products in a manner that directly infringe one or more claims of the '177 patent.[29] By providing instruction and training to customers and end-users on how to use the NVIDIA '177 Products in a manner that directly infringes one or more claims of the '177 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '177 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '177 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '177 patent. Accordingly, NVIDIA has induced and continues to induce users of the

[29] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

accused products to use the accused products in their ordinary and customary way to infringe the '177 patent, knowing that such use constitutes infringement of the '177 patent.

305. The '177 patent is well-known within the industry as demonstrated by multiple citations to the '177 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '177 patent without paying a reasonable royalty. NVIDIA is infringing the '177 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

306. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '177 patent.

307. As a result of NVIDIA's infringement of the '177 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT VII
INFRINGEMENT OF U.S. PATENT NO. 7,010,039

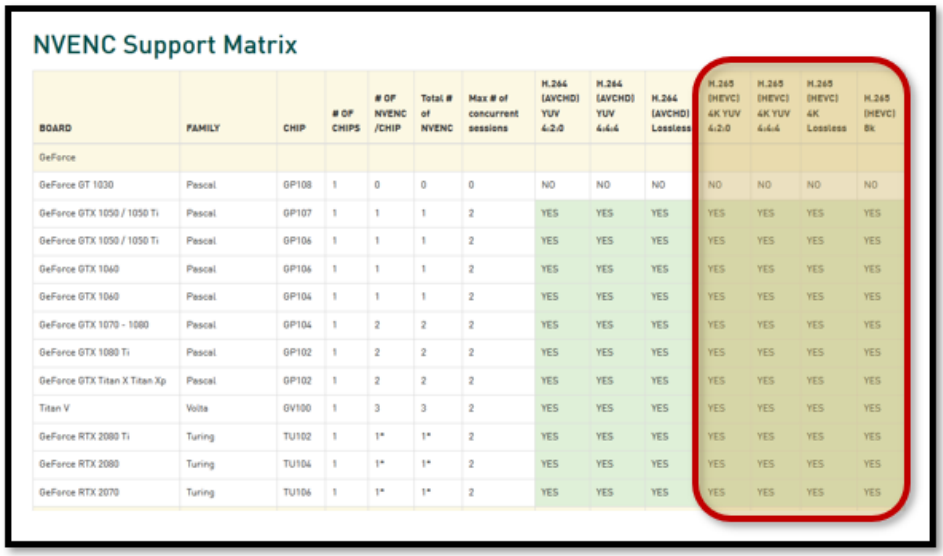
308. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

309. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for detecting motion.

310. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses Products containing H.265 encoding technology, including: GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan

V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Tesla M4, Tesla M40, Tesla M6, and Tesla M60 (collectively, the "NVIDIA '039 Product(s)").

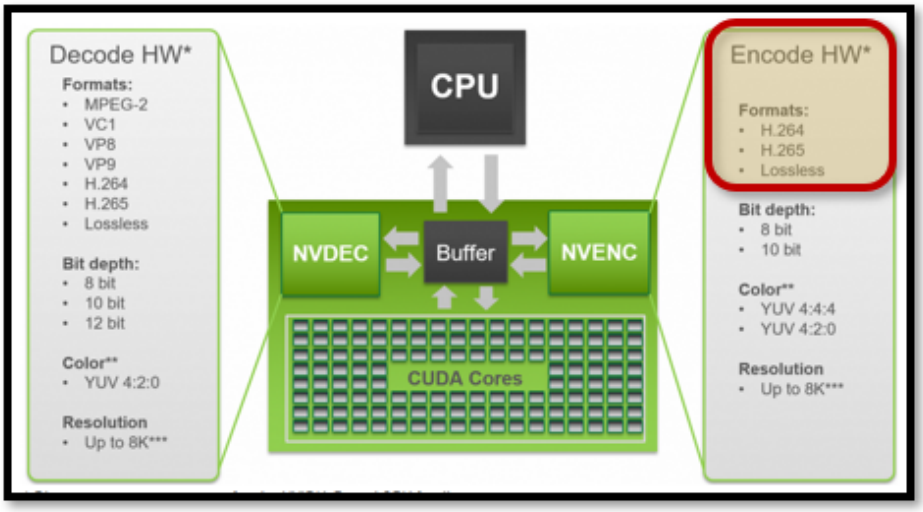
311. The NVIDIA '039 Products enable HEVC video encoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '039 Products comply with the HEVC standard for encoding data.



NVENC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVENC /CHIP	Total # of NVENC	Max # of concurrent sessions	H.264 (AVCHD) YUV 4:2:0	H.264 (AVCHD) YUV 4:4:4	H.264 (AVCHD) Lossless	H.265 (HEVC) 4K YUV 4:2:0	H.265 (HEVC) 4K YUV 4:4:4	H.265 (HEVC) 4K Lossless	H.265 (HEVC) 8k
GeForce													
GeForce GT 1030	Pascal	GP108	1	0	0	0	NO	NO	NO	NO	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP104	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1070 - 1080	Pascal	GP104	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1080 Ti	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
Titan V	Volta	GV100	1	3	3	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080 Ti	Turing	TU102	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC encoding in compliance with the HEVC standard).



NVIDIA Video Codec SDK, NVIDIA WEBSITE (last visited October 2018), *available at*: https://developer.nvidia.com/nvidia-video-codec-sdk (annotation showing support for the H.265 encoding standard).

312. NVIDIA documentation establishes that the NVIDIA '039 Products contain all the functionality required for the H.265 Main Profile and are complaint with the HEVC standard.

Feature	Description	Kepler GPUs	First generation Maxwell GPUs	Second generation Maxwell GPUs
H.264 Base, Main, High Profiles	YUV 4:2:0 Encoding.	✓	✓	✓
H.264 4:4:4 and Lossless	Regular YUV 4:4:4 and Lossless Encoding.	×	✓	✓
H.265 Main Profile	YUV 4:2:0 Encoding.	×	×	✓
H264 Motion Estimation (ME) only Mode	Capability to provide Macroblock level motion vectors and intra/inter modes	×	✓	✓
Support for ARGB Input	Capability to accept RGB input for limited color spaces.	✓	✓	✓

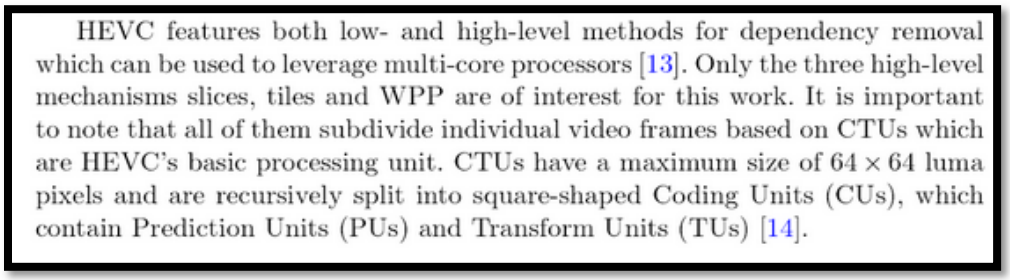
NVIDIA VIDEO ENCODER APPLICATION NOTE at 7 (November 2015) (emphasis added).

313. On information and belief, the NVIDIA '039 Products contain functionality wherein a criterion function for candidate vectors is optimized. The criterion function depends on data obtained from the previous and next images in the video data stream. The optimizing is carried out at a temporal intermediate position in non-covered and covered areas. The following

excerpts explain how HEVC is a form of encoding video information using a temporal intermediate position between previous and next images.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess. Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC), UPTEC STS 16006 at 4 (March 2016)



HEVC features both low- and high-level methods for dependency removal which can be used to leverage multi-core processors [13]. Only the three high-level mechanisms slices, tiles and WPP are of interest for this work. It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC's basic processing unit. CTUs have a maximum size of 64×64 luma pixels and are recursively split into square-shaped Coding Units (CUs), which contain Prediction Units (PUs) and Transform Units (TUs) [14].

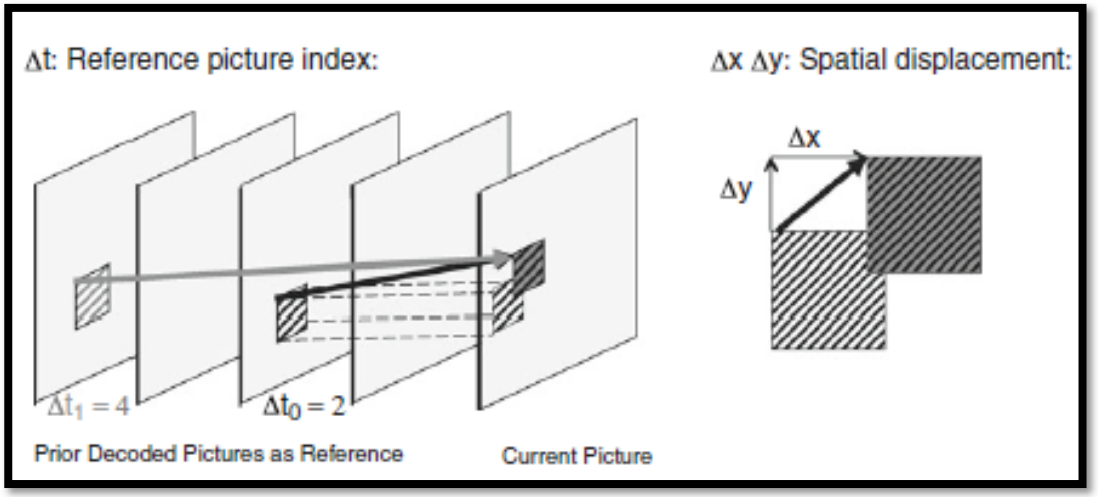
Stefan Radicke, *et al*., *Many-Core HEVC Encoding Based on Wavefront Parallel Processing and GPU -accelerated Motion Estimation*, E-BUSINESS AND TELECOMMUNICATIONS: 11TH INTERNATIONAL JOINT CONFERENCE at 296 (2015) ("HEVC feature both low- and high-level methods for dependency removal which can be used to leverage multi-core processors. . . It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC' basic processing unit.").

314. On information and belief, the NVIDIA '039 Products receive encoded video data that is encoded using inter-frame coding. The encoded video stream received by the NVIDIA Products are coded using its predecessor frame and subsequent frame. Inter-prediction used in the encoded video data received by the NVIDIA Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit ***temporal statistical dependences,*** intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

315. The encoded video stream received by the NVIDIA Products are encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



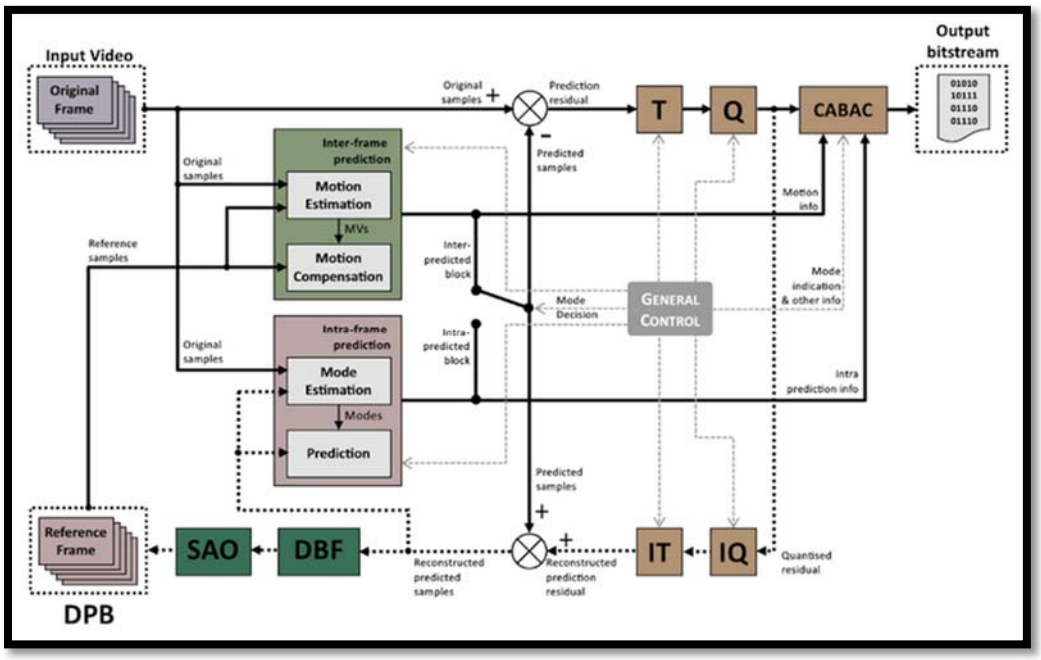
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

316. On information and belief, the following excerpt from an article describing the architecture of the encoded video stream received by the NVIDIA '39 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . or two reference frames (bi-prediction) to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

317. On information and belief, the following diagram shows how the NVIDIA '039 Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across frames.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

318. On information and belief, the NVIDIA '039 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the NVIDIA

Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

319. The NVIDIA '39 Products optimize the selection of candidate vectors by calculation a temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas. Specifically, the encoding process for video data received by the NVIDIA Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

320. On information and belief, the "Overview of Design Characteristics" in the HEVC specification describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."

compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 0.7 (April 2015) (annotation added).

321. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '039 Products - necessarily infringe the '039 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '039 patent, including but not limited to claim 13. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '039 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

322. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '039 Products in regular business operations.

323. On information and belief, the NVIDIA '039 Products are available to businesses and individuals throughout the United States.

324. On information and belief, the NVIDIA '039 Products are provided to businesses and individuals located in Delaware.

325. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '039 Patent by, among other things, making, using, offering for sale, and/or selling technology for detecting motion, including but not limited to the NVIDIA '039 Products.

326. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the NVIDIA '039 Products, NVIDIA has injured Dynamic Data and

is liable for directly infringing one or more claims of the '039 Patent, including at least claim 13, pursuant to 35 U.S.C. § 271(a).

327. On information and belief, NVIDIA also indirectly infringes the '039 Patent by actively inducing infringement under 35 USC § 271(b).

328. On information and belief, NVIDIA has had knowledge of the '039 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '039 Patent and knew of its infringement, including by way of this lawsuit.

329. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '039 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '039 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '039 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '039 Products that have the capability of operating in a manner that infringe one or more of the claims of the '039 patent, including at least claim 13, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '039 Products to utilize the products in a manner that directly infringe one or more claims of the '039 patent.[30] By providing instruction and training to customers and end-users on

[30] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018);

how to use the NVIDIA '039 Products in a manner that directly infringes one or more claims of the '039 patent, including at least claim 13, NVIDIA specifically intended to induce infringement of the '039 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '039 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '039 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '039 patent, knowing that such use constitutes infringement of the '039 patent.

330. The '039 patent is well-known within the industry as demonstrated by multiple citations to the '039 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '039 patent without paying a reasonable royalty. NVIDIA is infringing the '039 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

331. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '039 patent.

332. As a result of NVIDIA's infringement of the '039 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

NVIDIA Tesla M60 GPU Accelerator, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

COUNT VIII
INFRINGEMENT OF U.S. PATENT NO. 8,311,112

333. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

334. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for video compression.

335. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses Products containing H.265 encoding technology, including: GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Tesla M4, Tesla M40, Tesla M6, and Tesla M60 (collectively, the "NVIDIA '112 Product(s)").

336. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '112 Products in regular business operations.

337. On information and belief, one or more of the NVIDIA '112 Products include technology for video compression.

20. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '112 patent by, among other things, making, using, offering for sale, and/or selling technology for video compression, including but not limited to the NVIDIA '112 Products.

338. On information and belief, one or more of the NVIDIA '112 Products perform predictive coding on a macroblock of a video frame such that a set of pixels of the macroblock is

coded using some of the pixels from the same video frame as reference pixels and the rest of the macroblock is coded using reference pixels from at least one other video frame.

339. On information and belief, one or more of the NVIDIA '112 Products include a system for video compression comprising an intra-frame coding unit configured to perform predictive coding on a set of pixels of a macroblock of pixels using a first group of reference pixels, the macroblock of pixels and the first group of reference pixels being from a video frame.

21. On information and belief, one or more of the NVIDIA '112 Products include a system for video compression comprising an inter-frame coding unit configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels, the second group of reference pixels being from at least one other video frame.

22. On information and belief, the NVIDIA '112 Products are available to businesses and individuals throughout the United States.

23. On information and belief, the NVIDIA '112 Products are provided to businesses and individuals located in Delaware.

24. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the NVIDIA '112 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '112 patent, including at least claim 11 pursuant to 35 U.S.C. § 271(a).

340. On information and belief, NVIDIA also indirectly infringes the '112 patent by actively inducing infringement under 35 USC § 271(b).

341. NVIDIA has had knowledge of the '112 patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '112 patent and knew of its infringement, including by way of this lawsuit.

342. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '112 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '112 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '112 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '112 Products that have the capability of operating in a manner that infringe one or more of the claims of the '112 patent, including at least claim 11, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '112 Products to utilize the products in a manner that directly infringe one or more claims of the '112 patent.[31] By providing instruction and training to customers and end-users on how to use the NVIDIA '112 Products in a manner that directly infringes one or more claims of the '112 patent, including at least claim 11, NVIDIA specifically intended to induce infringement of the '112 patent. On information and belief, NVIDIA engaged in such inducement to promote

[31] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

the sales of the NVIDIA '112 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '112 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '112 patent, knowing that such use constitutes infringement of the '112 patent.

343. The '112 patent is well-known within the industry as demonstrated by multiple citations to the '112 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '112 patent without paying a reasonable royalty. NVIDIA is infringing the '112 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

344. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '112 patent.

345. As a result of NVIDIA's infringement of the '112 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

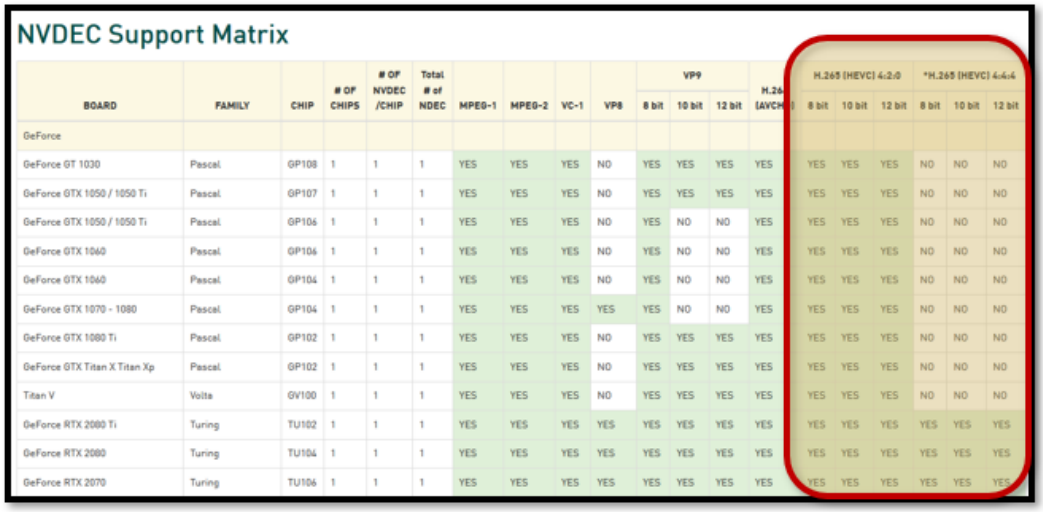
COUNT IX
INFRINGEMENT OF U.S. PATENT NO. 7,894,529

346. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

347. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for determining motion vectors that are each assigned to individual image regions.

348. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses Products containing H.265 decoding technology, including: GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Tesla M4, Tesla M40, Tesla M6, and Tesla M60 (collectively, the "NVIDIA '529 Product(s)").

349. The NVIDIA '529 Products enable HEVC video decoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '529 Products comply with the HEVC standard for decoding data.

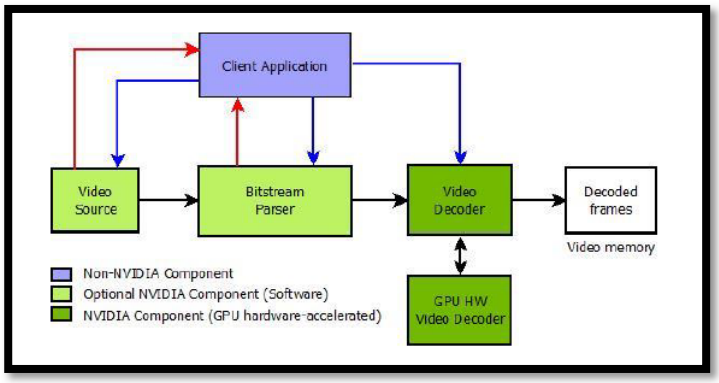


NVDEC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVDEC /CHIP	Total # of NDEC	MPEG-1	MPEG-2	VC-1	VP8	VP9			H.264 (AVCHD)	H.265 (HEVC) 4:2:0			*H.265 (HEVC) 4:4:4		
										8 bit	10 bit	12 bit		8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
GeForce																			
GeForce GT 1030	Pascal	GP108	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP104	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1070 - 1080	Pascal	GP104	1	1	1	YES	YES	YES	YES	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1080 Ti	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
Titan V	Volta	GV100	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce RTX 2080 Ti	Turing	TU102	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC decoding in compliance with the HEVC standard).

350. The NVIDIA '529 Products comply with the HEVC standard in decoding video data. The NVIDIA document shows the NVDEC interface for decoding video data.



NVIDIA Video Decoder (NVDEC) Interface, NVIDIA PROGRAMMING GUIDE at 4 (June 2016) (annotations added) (showing the functionality for decoding video data for on-screen display).

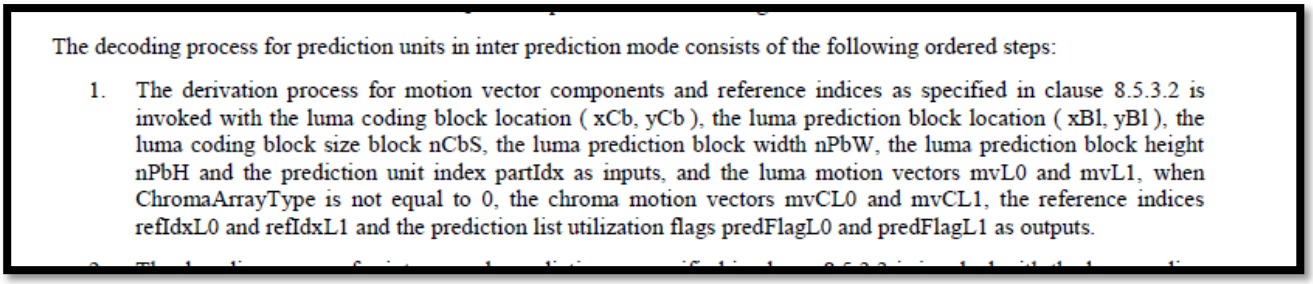
351. The NVIDIA '529 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the NVIDIA '529 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by NVIDIA '529 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

352. The NVIDIA '529 Products contain video processing functionality that complies with the HEVC standard.

353. The NVIDIA '529 Products incorporate a decoding unit for decoding the frame of the received video data. The decoding utilizes a second frame recovery unit that is a decoding motion vector. Specifically, the encoding and decoding process for video data received by the NVIDIA '529 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

354. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '529 Products - necessarily infringe the '529 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '529 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '529 patent: "3.110 Prediction Unit Definition;" "6.3.2 Block and quadtree structures;" "6.3.3 Spatial or component-wise partitioning;" "6.4.2 Derivation process for prediction block availability;" "7.3.8.5 Coding unit syntax;" "7.3.8.6 Prediction unit syntax;" "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process."

355. On information and belief, the NVIDIA '529 Products comply with the HEVC standard, which requires determining motion vectors assigned to individual image regions of an image.



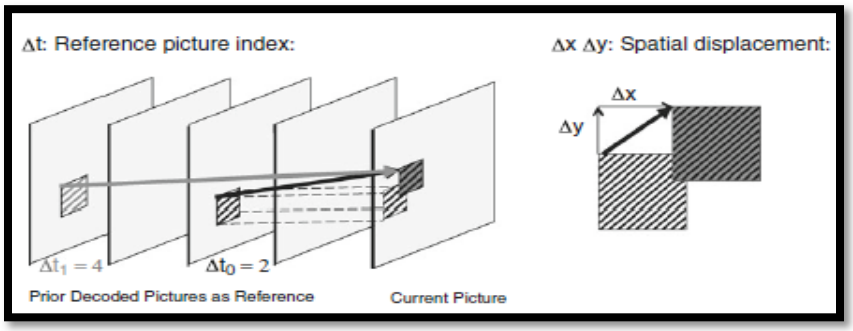
The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 8.5.3.1 (February 2018).

356. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '529 patent by, among other things, making, using, offering for sale, and/or selling technology for implementing a motion estimation technique that assigns at least one motion vector to each of the image blocks and generating a modification motion vector for at least the first image block.

357. On information and belief, the encoded video stream received by the NVIDIA '529 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

358. On information and belief, the NVIDIA '529 Products perform the step of selecting a second image block where the motion vector that is assigned to the first image block passes. Specifically, the NVIDIA '529 Products, in the use of inter-picture prediction, look at two or more blocks in different frames wherein the vector passes through both the first and second image block.

The following excerpts from documentation relating the video estimation technique used by the NVIDIA '529 Products explains how HEVC uses motion estimation to determine a temporal intermediate position between two images wherein two image blocks are selected that have a motion vector passing in both the first and second image block.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

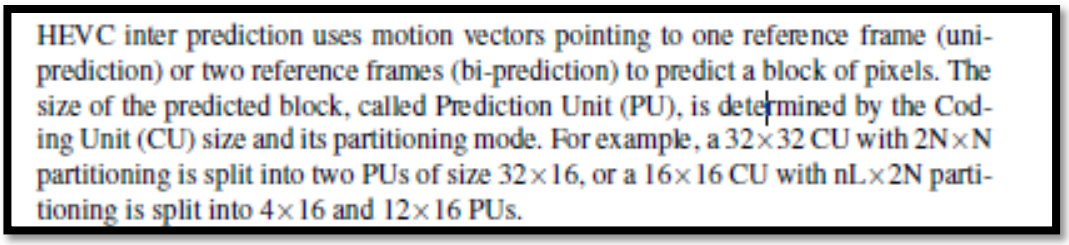
Johan Bartelmess, *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

359. On information and belief, the NVIDIA '529 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the NVIDIA '529 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the NVIDIA '529 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., Vol. 22, No. 12, p. 1654 (December 2012) (emphasis added).

360. The following excerpt from an article describing the architecture of the video stream received by the NVIDIA '529 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."



HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

361. On information and belief, any implementation of the HEVC standard infringes the '529 patent as every possible implementation of the standard requires: determining at least a second image block through which the motion vector assigned to the first image block at least partially passes; generating the modified motion vector as a function of a motion vector assigned to at least the second image block; and assigning the modified motion vector as the motion vector to the first image block. Further, the functionality of the motion estimation process in HEVC uses "motion vector[s]: A two-dimensional vector used for *inter prediction* that provides an offset from the coordinates in the decoded picture to the coordinates in a reference picture," as defined in definition 3.83 of the *ITU-T H.265 Series H: Audiovisual and Multimedia Systems* (2018) (emphasis added); *see also, e.g.,* Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1650 (December 2012) ("The encoder and decoder generate identical inter picture prediction signals by applying motion compensation (MC) using the MV and mode decision data.").

362. The motion estimation done by the NVIDIA '529 Products is done through a PU matching method where the motion vector represents the displacement between the current PU in the current frame and the matching PU in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference

> to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

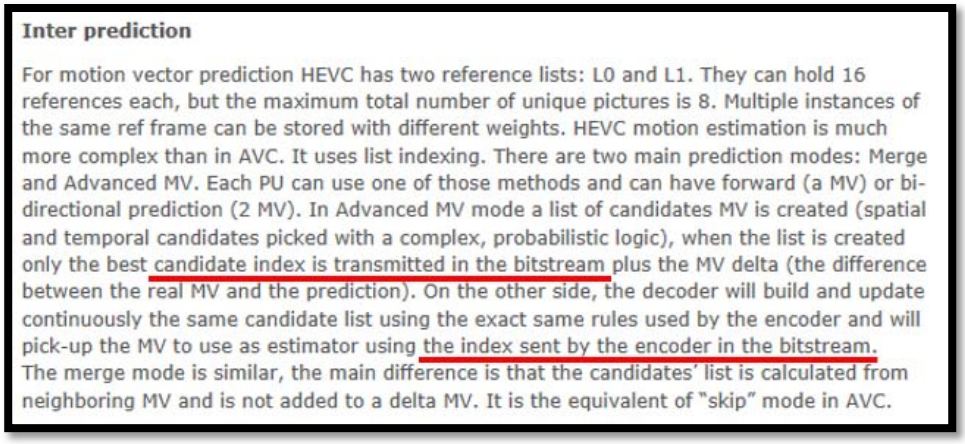
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

363. On information and belief, the NVIDIA '529 Products perform the step of assigning the modified motion vector as the motion vector to the first image block. Specifically, the NVIDIA '529 Products, through the use of AMVP and Merge Mode, select the modified motion vector and assign it to a first block. The displacement between the current prediction unit and the matching prediction unit in the second image (reference image) is signaled using a motion vector. Further, the NVIDIA '529 Products take the modified motion vector "computed from corresponding regions of previously decoded pictures" and transmit the residual.

> A block-wise prediction residual ***is computed from corresponding regions of previously decoded pictures (inter-picture motion compensated prediction) or neighboring previously decoded samples from the same picture (intra-picture spatial prediction***). The residual is then processed by a block transform, and the transform coefficients are quantized and entropy coded. Side information data such as motion vectors and mode switching parameters are also encoded and transmitted.

Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, Vol. 7, No. 6 at 1002 (December 2013) (emphasis added).

364. On information and belief, the NVIDIA '529 Products transmit into the bitstream the candidate index of motion vectors. HEVC documentation states that the coding process will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

365. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '529 Products in regular business operations.

366. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '529 Patent by, among other things, making, using, offering for sale, and/or selling technology for determining motion vectors that are each assigned to individual image regions, including but not limited to the NVIDIA '529 Products.

367. On information and belief, the NVIDIA '529 Products are available to businesses and individuals throughout the United States.

368. On information and belief, the NVIDIA '529 Products are provided to businesses and individuals located in Delaware.

369. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the NVIDIA '529 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '529 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

370. On information and belief, NVIDIA also indirectly infringes the '529 Patent by actively inducing infringement under 35 USC § 271(b).

371. NVIDIA has had knowledge of the '529 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '529 Patent and knew of its infringement, including by way of this lawsuit.

372. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '529 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '529 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '529 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '529 Products that have the capability of operating in a manner that infringe one or more of the claims of the '529 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '529 Products to utilize the products in a manner that directly infringe one or more claims of the '529 patent.[32] By providing instruction and training to customers and end-users on how to use the NVIDIA '529 Products in a manner that directly infringes one or more claims of

[32] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

the '529 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '529 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '529 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '529 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '529 patent, knowing that such use constitutes infringement of the '529 patent.

373. The '529 patent is well-known within the industry as demonstrated by multiple citations to the '529 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '529 patent without paying a reasonable royalty. NVIDIA is infringing the '529 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

374. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '529 patent.

375. As a result of NVIDIA's infringement of the '529 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT X
INFRINGEMENT OF U.S. PATENT NO. 7,542,041

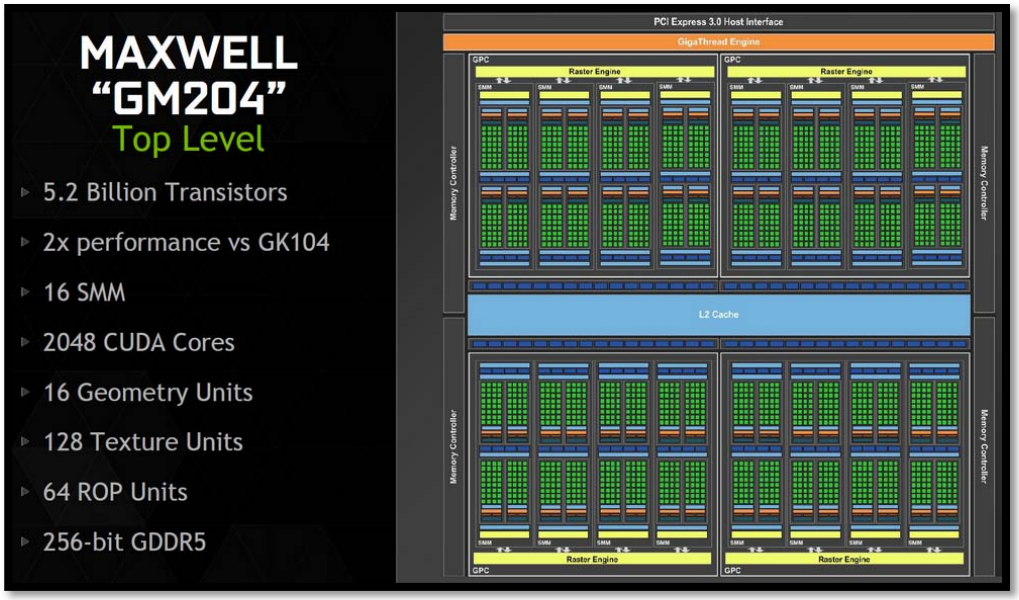
376. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

377. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for dynamically configuring a multi-pipe pipeline system.

378. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA graphics processing units, including: GeForce 700 series (GeForce GTX 745, GeForce GTX 750, GeForce GTX 750 Ti, GeForce GTX 760 192-Bit, GeForce GTX 760, GeForce GTX 760 Ti, GeForce GTX 770, GeForce GTX 780, GeForce GTX 780 Ti, GeForce GTX Titan, GeForce GTX Titan Black, GeForce GTX Titan Z); GeForce 800M series (GeForce 800M, GeForce 820M, GeForce 830M, GeForce 840M, GeForce GTX 850M, GeForce GTX 860M, GeForce GTX 870M, GeForce GTX 880M); GeForce 900 series (GeForce GTX 950, GeForce GTX 960, GeForce GTX 970, GeForce GTX 980, GeForce GTX 980 Ti, GeForce GTX Titan X); GeForce 10 series (GeForce GT 1030, GeForce GTX 1050, GeForce GTX 1050 Ti, GeForce GTX 1060, GeForce GTX 1070, GeForce GTX 1070 Ti, GeForce GTX 1080, GeForce GTX 1080 Ti, Titan X, Titan Xp); and GeForce 20 Series (GeForce RTX 2070, GeForce RTX 2080, GeForce RTX 2080) (collectively, the "NVIDIA '041 Product(s)").

379. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '041 Products in regular business operations.

380. On information and belief, one or more of the NVIDIA '041 Products include technology for dynamically configuring a multi-pipe pipeline system. Specifically, the NVIDIA Products comprise multiple vector pipelines that process data as it traverses the pipeline.



Chris Kubisch, *Life of a Triangle – NVIDIA's Logical Pipeline*, NVIDIA DEVELOPER WEBSITE (March 16, 2015) ("The GPU is partitioned into multiple GPCs (Graphics Processing Cluster), each has multiple SMs (Streaming Multiprocessor) and one Raster Engine**.** There is lots of interconnects in this process, most notably a Crossbar that allows work migration across GPCs or other functional units like ROP (render output unit) subsystems.").

381. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '041 patent by, among other things, making, using, offering for sale, and/or selling technology for dynamically configuring a multi-pipe pipeline system, including but not limited to the NVIDIA '041 Products.

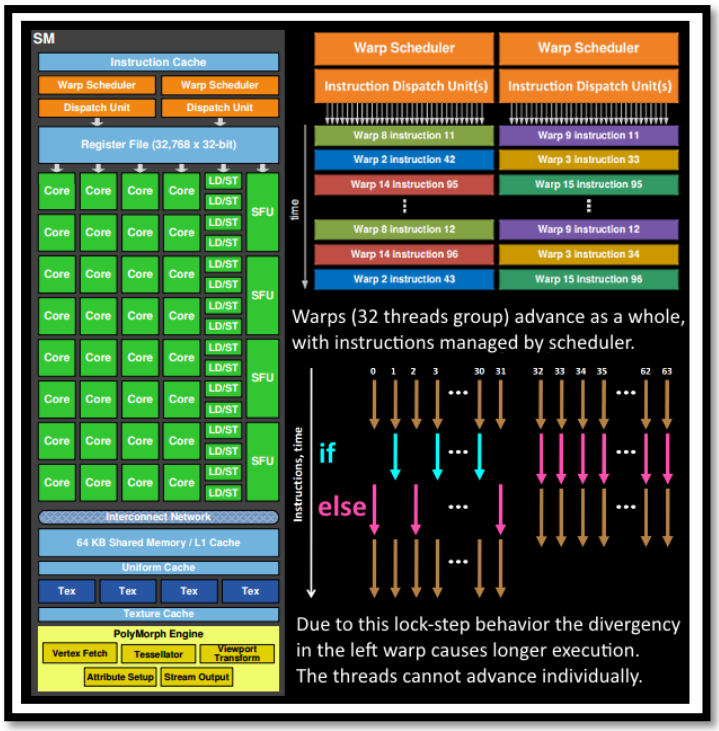
382. The NVIDIA '041 Products are synchronized and process data in order such that correct triangle order is maintained.

> Thread Level Preemption for compute operates similarly to Pixel Level Preemption for graphics. Compute workloads are composed of multiple grids of thread blocks, each grid containing many threads. When a preemption request is received, the threads that are currently running on the SMs are completed. Other units save their current position to be ready to pick up where they left off later, and then the GPU is ready to switch tasks. The entire process of switching tasks can complete in less than 100 µs after the currently running threads finish.

NVIDIA GeForce GTX 1080, NVIDIA WHITEPAPER at 16 (2016).

383. On information and belief, one or more of the NVIDIA '041 Products enable a multiple-pipeline system that is dynamically configurable to effect various combinations of functions for each pipeline.

384. The NVIDIA Product comprise a plurality of pipelines. Each pipeline contains multiple core pipeline elements that are configured to process data as it flows through the pipeline. The below excerpt from NVIDIA reference documentation describes that product uses multiple compute pipelines that sequentially process data.



Chris Kubisch, *Life of a Triangle – NVIDIA's Logical Pipeline*, NVIDIA DEVELOPER WEBSITE (March 16, 2015) ("The GPU is partitioned into multiple GPCs (Graphics Processing Cluster), each has multiple SMs (Streaming Multiprocessor) and one Raster Engine**.** There is lots of interconnects in this process, most notably a **Crossbar** that allows work migration across GPCs or other functional units like ROP (render output unit) subsystems.").

385. The NVIDIA '041 Products contain a "Scheduler" that enables to data to be processed in a subsequent manner as it traverses the pipeline. The below excerpt from NVIDIA documentation shows the scheduler.

> To ensure that rendering results are predictable, the DX API has always specified "in order" processing rules for the raster pipeline, in particular the Color and Z units ("ROP"). Given two triangles sent to the GPU in order—first triangle "A," then "B"—that touch the same XY screen location, the GPU hardware guarantees that triangle "A" will blend its color result before "B" blends it. Special interlock hardware in the ROP is responsible for enforcing this ordering requirement

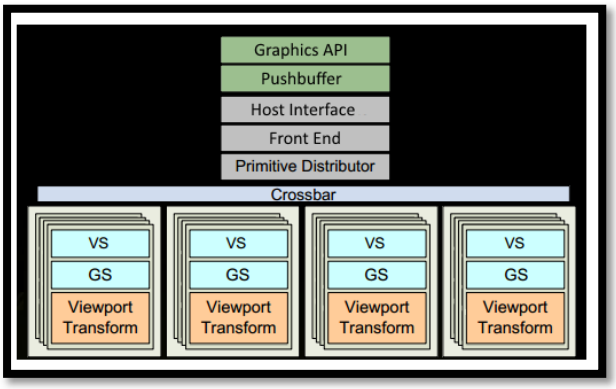
NVIDIA GeForce GTX 980 Whitepaper, NVIDIA MAXWELL DOCUMENTATION at 24 (2014).

386. On information and belief, one or more of the NVIDIA '041 Products include a multiple pipeline system that includes a pool of auxiliary function blocks that are provided as required to select pipelines.

387. On information and belief, one or more of the NVIDIA '041 Products consist of a multiple-pipeline system wherein each pipeline is configured to include a homogenous set of core functions.

388. On information and belief, one or more of the NVIDIA '041 Products include a pool of auxiliary functions is provided for selective insertion of auxiliary functions between core functions of select pipelines.

389. The NVIDIA '041 Products comprise a plurality of pipelines for processing data. These pipelines are coupled to a plurality of auxiliary elements that control the function of the pipelines. Specifically, axillary elements can pass signals to multiple pipelines using crossbar fabrics.



Chris Kubisch, *Life of a Triangle – NVIDIA's Logical Pipeline*, NVIDIA DEVELOPER WEBSITE (March 16, 2015) ("Now it gets exciting, our triangle is about to be chopped up and potentially

leaving the GPC it currently lives on. The bounding box of the triangle is used to decide which raster engines need to work on it, as each engine covers multiple tiles of the screen. It sends out the triangle to one or multiple GPCs via the Work Distribution Crossbar**.** We effectively split our triangle into lots of smaller jobs now.").

390. On information and belief, one or more of the NVIDIA '041 Products includes auxiliary functions wherein each auxiliary function includes a multiplexer that allows it to be selectively coupled within each pipeline.

391. On information and belief, one or more of the NVIDIA '041 Products contain a processing system that includes a plurality of pipelines, with each pipeline of the plurality including a plurality of core pipeline elements that are configured to sequentially process data as it traverses the pipeline.

392. On information and belief, one or more of the NVIDIA '041 Products contain a processing system that includes a plurality of auxiliary elements, each auxiliary element of the plurality of auxiliary elements being configured to be selectively coupled to multiple pipelines of the plurality of pipelines.

393. On information and belief, one or more of the NVIDIA '041 Products contain a processing system wherein the auxiliary elements are responsive to external coupling-select signals.

394. On information and belief, one or more of the NVIDIA '041 Products contain a processing system wherein a plurality of auxiliary elements are within a selected pipeline of the multiple pipelines, between a pair of core pipeline elements of the plurality of core pipeline elements to process the data as it traverses between the pair of core elements.

25. On information and belief, the NVIDIA '041 Products are available to businesses and individuals throughout the United States.

26. On information and belief, the NVIDIA '041 Products are provided to businesses and individuals located in Delaware.

27. By making, using, testing, offering for sale, and/or selling products and services for dynamically configuring a multi-pipe pipeline system, including but not limited to the NVIDIA '041 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '041 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

395. On information and belief, NVIDIA also indirectly infringes the '041 patent by actively inducing infringement under 35 USC § 271(b).

396. NVIDIA has had knowledge of the '041 patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '041 patent and knew of its infringement, including by way of this lawsuit.

397. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '041 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '041 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '041 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '041 Products that have the capability of operating in a manner that infringe one or more of the claims of the '041 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '041 Products to utilize the products in a manner that directly infringe one or more

claims of the '041 patent.[33] By providing instruction and training to customers and end-users on how to use the NVIDIA '041 Products in a manner that directly infringes one or more claims of the '041 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '041 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '041 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '041 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '041 patent, knowing that such use constitutes infringement of the '041 patent.

398. The '041 patent is well-known within the industry as demonstrated by multiple citations to the '041 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '041 patent without paying a reasonable royalty. NVIDIA is infringing the '041 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

399. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '041 patent.

400. As a result of NVIDIA's infringement of the '041 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for

[33] *GeForce GTX 980*, INSTALLATION GUIDE (2014); *NIVIDIA GeForce GTX 750 Ti*, NVIDIA WHITEPAPER (2014); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *Release 396 Graphics Drivers for Windows, Version 399.07*, RELEASE NOTES (Aug. 27, 2018); *Release 390 Graphics Drivers for Windows, Version 390.77*, RELEASE NOTES (Jan. 29, 2018); *Titan X*, NVIDIA USER GUIDE (2016).

NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT XI
INFRINGEMENT OF U.S. PATENT NO. 7,571,450

401. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

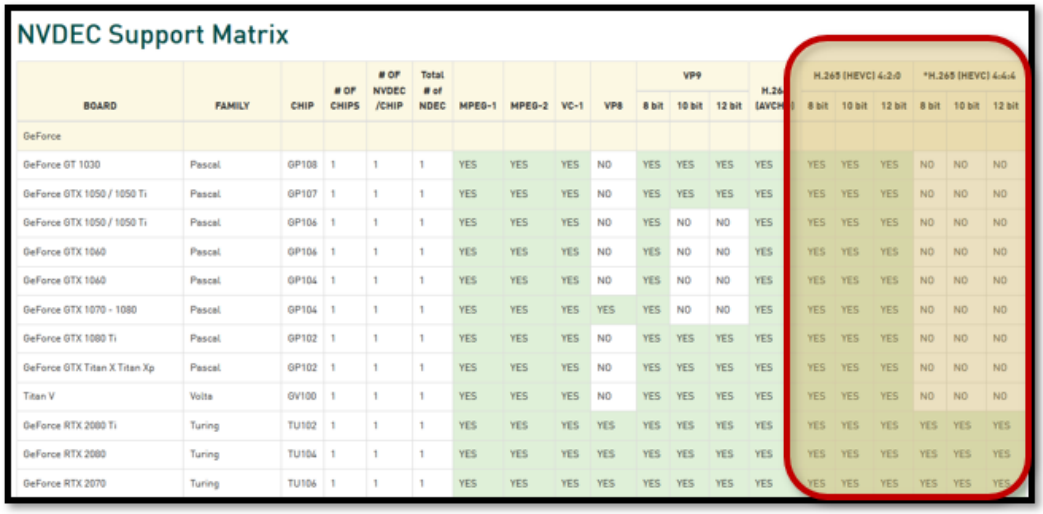
402. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for displaying information.

403. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA products, including the: GeForce GTX 750, GeForce GTX 950 - 960, GeForce GT 1030, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X, Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000 / P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, Tesla M4, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, and Quadro P1000 (collectively, the "NVIDIA '450 Product(s)").

404. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '450 Products in regular business operations.

405. On information and belief, one or more of the NVIDIA '450 Products include technology for decoding HEVC data for display in compliance with the HEVC standard.

406. The NVIDIA '450 Products enable HEVC video decoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '450 Products comply with the HEVC standard for decoding data.

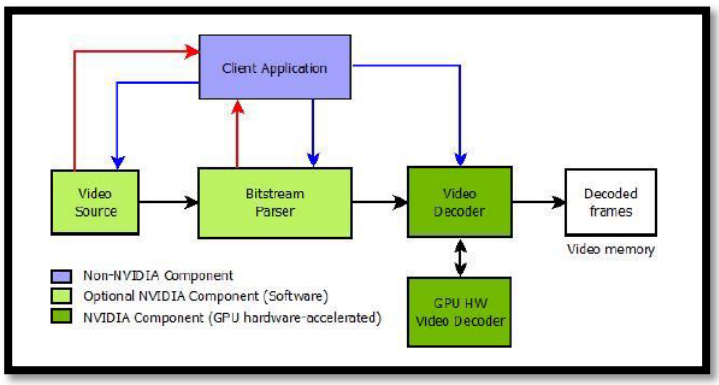


NVDEC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVDEC /CHIP	Total # of NDEC	MPEG-1	MPEG-2	VC-1	VP8	VP9			H.264 (AVCHD)	H.265 (HEVC) 4:2:0			*H.265 (HEVC) 4:4:4		
										8 bit	10 bit	12 bit		8 bit	10 bit	12 bit	8 bit	10 bit	12 bit
GeForce																			
GeForce GT 1030	Pascal	GP108	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP106	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1060	Pascal	GP104	1	1	1	YES	YES	YES	NO	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1070 - 1080	Pascal	GP104	1	1	1	YES	YES	YES	YES	YES	NO	NO	YES	YES	YES	YES	NO	NO	NO
GeForce GTX 1080 Ti	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
Titan V	Volta	GV100	1	1	1	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES	YES	NO	NO	NO
GeForce RTX 2080 Ti	Turing	TU102	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1	1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC decoding in compliance with the HEVC standard).

407. The NVIDIA '450 Products comply with the HEVC standard in decoding video data. The NVIDIA document shows the NVDEC interface for decoding video data.



NVIDIA Video Decoder (NVDEC) Interface, NVIDIA PROGRAMMING GUIDE at 4 (June 2016) (annotations added) (showing the functionality for decoding video data for on-screen display).

408. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '450 Products - necessarily infringe the '450 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '450 patent, including but not limited to claim 8. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO

REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '450 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

409. On information and belief, the NVIDIA '450 Products receive data that is segmented into Network Abstraction Layer ("NAL") Units. NAL Units are segments of data that can include video data and overlay data (such as captions and overlay images). The NVIDIA '450 Products support the receipt of VCL and non-VCL NAL units. The VCL NAL units contain the data that represents the values of the samples in the video pictures, and the non-VCL NAL units contain any associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

410. The NVIDIA '450 Products process data in the form of VCL NAL Units that contain segments of data which are used to generate an image (e.g., HEVC image) on a display device. Each VCL NAL Unit comprises a discrete number of bites which make up a segment.

The following excerpt from the HEVC specification describes a NAL unit as being a segment with a "demarcation" setting forth where the segment ends and begins.

> NumBytesInNalUnit specifies the size of the NAL unit in bytes. This value is required for decoding of the NAL unit. Some form of demarcation of NAL unit boundaries is necessary to enable inference of NumBytesInNalUnit. One such demarcation method is specified in Annex B for the byte stream format. Other methods of demarcation may be specified outside of this Specification.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.2.1 (February 2018) (emphasis added).

411. The NVIDIA '450 Products receive VCL NAL units that contain the data that represents the values of the samples in the video pictures, and non-VCL NAL units that contain associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

412. The NVIDIA'450 Products perform filtering, wherein the filtering enables a user to select a data element based on the user's selection. Specifically, a user can select the display of Non-VCL NAL Unit data which can include closed captions or other overlay information that is selected based on the user interaction. The data that is selected by the user is parsed by the system and filtered. The Non-VCL NAL Units include supplemental enhancement information ("SEI") messages. The SEI data that is received contains overlay information that can be combined with the image data that has already been received.

sei_message( ) {	Descriptor
payloadType = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadType += 255	
}	
last_payload_type_byte	u(8)
payloadType += last_payload_type_byte	
payloadSize = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadSize += 255	
}	
last_payload_size_byte	u(8)
payloadSize += last_payload_size_byte	
sei_payload(payloadType, payloadSize)	
}	

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.3.5 (February 2018).

413. The NVIDIA '450 Products perform rendering of an output image to be displayed on a display device on the basis of the first data-element selected by the filter. The overlay data is used to render overlays of the display data. The amount of overlay data that is downloaded in the form of Non-VCL data comprises a portion of the overlay that is displayed.

414. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '450 Patent by, among other things, making, using, offering for sale, and/or selling technology for displaying information, including but not limited to the NVIDIA '450 Products.

415. On information and belief, one or more of the NVIDIA '450 Products enable methods and systems wherein a user does not need to make a new selection after being switched from one service to a second service.

416. On information and belief, one or more of the NVIDIA '450 Products perform a method of displaying information on a display device wherein receiving a transport stream comprises services, with the services having elementary streams of video and of data elements.

417. On information and belief, one or more of the NVIDIA ‘450 Products perform a method of displaying information on a display device wherein user actions of making a user selection of a type of information to be displayed on the device are received.

418. On information and belief, one or more of the NVIDIA ‘450 Products perform a method of displaying information on a display device wherein filtering to select a data element of a first one of the services on the basis of the user selection is performed.

419. On information and belief, one or more of the NVIDIA ‘450 Products perform a method of displaying information on a display device wherein rendering to calculate an output image to be displayed on the display device, on the basis of the first data element selected by the filer is performed.

420. On information and belief, one or more of the NVIDIA ‘450 Products perform a method of displaying information on a display device wherein switching from the first one of the services to a second one of the services, characterized in comprising a second step of filtering to select a second data-element of the second one of the services, on the basis of the user selection is performed.

421. On information and belief, one or more of the NVIDIA ‘450 Products perform a method of displaying information on a display device wherein being switched from the first one of the services to the second one of the services, with the data-element and the second data-element being mutually semantically related and a second step of rendering to calculate the output image to be displayed on the display device, on the basis of the second data-element selected by the filter is performed.

422. On information and belief, the NVIDIA ‘450 Products are available to businesses and individuals throughout the United States.

423. On information and belief, the NVIDIA '450 Products are provided to businesses and individuals located in Delaware.

424. By making, using, testing, offering for sale, and/or selling products and services for displaying information, including but not limited to the NVIDIA '450 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '450 Patent, including at least claim 8 pursuant to 35 U.S.C. § 271(a).

425. On information and belief, NVIDIA also indirectly infringes the '450 Patent by actively inducing infringement under 35 USC § 271(b).

426. NVIDIA has had knowledge of the '450 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, NVIDIA knew of the '450 Patent and knew of its infringement, including by way of this lawsuit.

427. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '450 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '450 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '450 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '450 Products that have the capability of operating in a manner that infringe one or more of the claims of the '450 patent, including at least claim 8, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '450 Products to utilize the products in a manner that directly infringe one or more

claims of the '450 patent.[34] By providing instruction and training to customers and end-users on how to use the NVIDIA '450 Products in a manner that directly infringes one or more claims of the '450 patent, including at least claim 8, NVIDIA specifically intended to induce infringement of the '450 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '450 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '450 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '450 patent, knowing that such use constitutes infringement of the '450 patent.

428. The '450 patent is well-known within the industry as demonstrated by multiple citations to the '450 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '450 patent without paying a reasonable royalty. NVIDIA is infringing the '450 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

429. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '450 patent.

[34] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

430. As a result of NVIDIA's infringement of the '450 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT XII
INFRINGEMENT OF U.S. PATENT NO. 7,750,979

431. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

432. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion compensation in video signal processing.

433. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA System on Chip products, including: Tegra 4, Tegra 4i, Tegra K1, Tegra X1, and Tegra X2 (collectively, the "NVIDIA '979 Product(s)").

434. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '979 Products in regular business operations.

435. On information and belief, one or more of the NVIDIA '979 Products include technology for motion compensation in video signal processing.

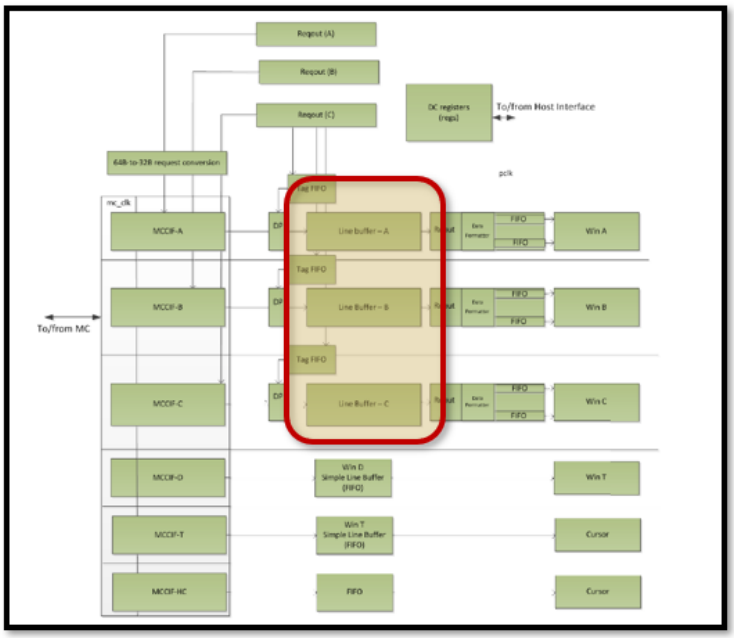
436. The NVIDIA '979 Products support video encoding and decoding of video signals as shown in the below whitepaper about Tegra 4.

Video	
Decode	**H.264 HP/MP/BP** 4k x 2k 62.5Mbps @ 24p,1440p 62.5Mbps @ 30p;1080p 62.5Mbps @ 60p; **VC1 AP/MP/SP** 1080p 40Mbps @ 60i/30p; **MPEG4 SP** 1080p 10Mbps @ 30 fps; **WebM VP8** 1080p 60Mbps @ 60p, 1440p 60Mbps @ 30p; **MPEG-2 MP** 1080p 80Mbps @ 60i/60p
Encode	**H.264 (BP/MP/HP)**1080p 50Mbps @ 60p, 1440p 50Mbps @ 30p; **MPEG4 SP** D1 1Mbps 30p; **VP8** 1080p 20Mbps @ 60p, 1440p 50 Mbps @ 30 fps
Audio	
Decode	AAC, AAC-LC, AAC+, eAAC+, MP3, WAV/PCM, AMR-NB, AMR-WB, BSAC, MPEG-2 Audio, Ogg Vorbis, WMA 10, WMA Lossless, WMA Pro LBR 10, MPEG-2, AC3
Encode	AAC LC, AMR-NB, AMR-WB

NVIDIA Tegra 4 Family GPU Architecture, NVIDIA WHITEPAPER at 24 (February 2013).

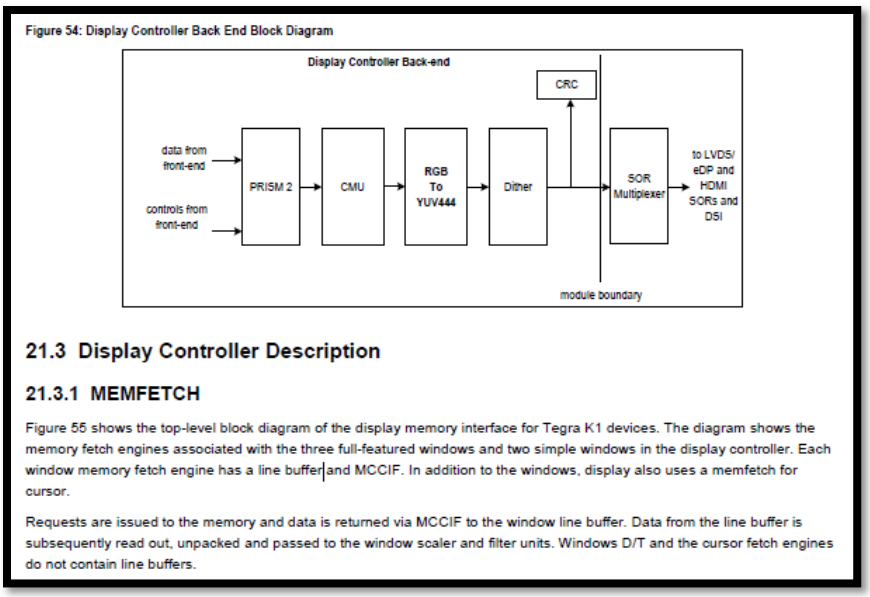
28. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '979 patent by, among other things, making, using, offering for sale, and/or selling technology for motion compensation in video signal processing, including but not limited to the NVIDIA '979 Products.

437. On information and belief, one or more of the NVIDIA '979 Products use line buffers that are decoupled and that can deliver a fixed number of pixels, as may be required by a video processing stage, using a sampling pattern that is defined as one among several selectable sampling windows. The following diagram from NVIDIA's documentation shows the memory fetch engines associated with the three full-featured windows and two simple windows in the display controller. Each window memory fetch engine has a line buffer and MCCIF. "Requests are issued to the memory and data is returned via MCCIF to the window line buffer. Data from the line buffer subsequently read out, unpacked and passed to the window scaler and filter units."



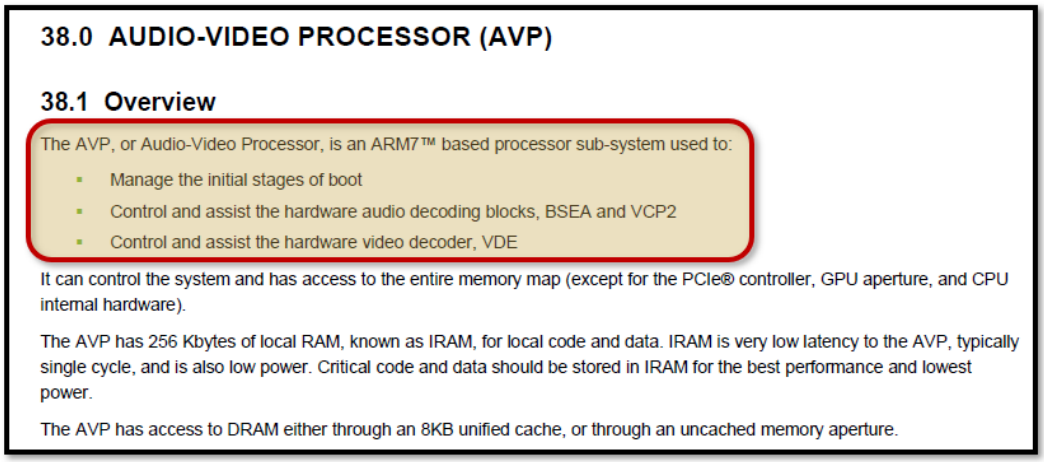
Tegra K1 Technical Reference Manual, NVIDIA DOCUMENTATION at 1453 (2014) (annotation showing the line buffers).

438. On information and belief, one or more of the NVIDIA '979 Products have a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array.



Tegra K1 Technical Reference Manual, NVIDIA DOCUMENTATION at 145 (2013) (showing the display controller backend).

439. On information and belief, one or more of the NVIDIA '979 Products have a video processing stage that inputs pixels using a fixed number of pixels.



38.0 AUDIO-VIDEO PROCESSOR (AVP)

38.1 Overview

The AVP, or Audio-Video Processor, is an ARM7™ based processor sub-system used to:

- Manage the initial stages of boot
- Control and assist the hardware audio decoding blocks, BSEA and VCP2
- Control and assist the hardware video decoder, VDE

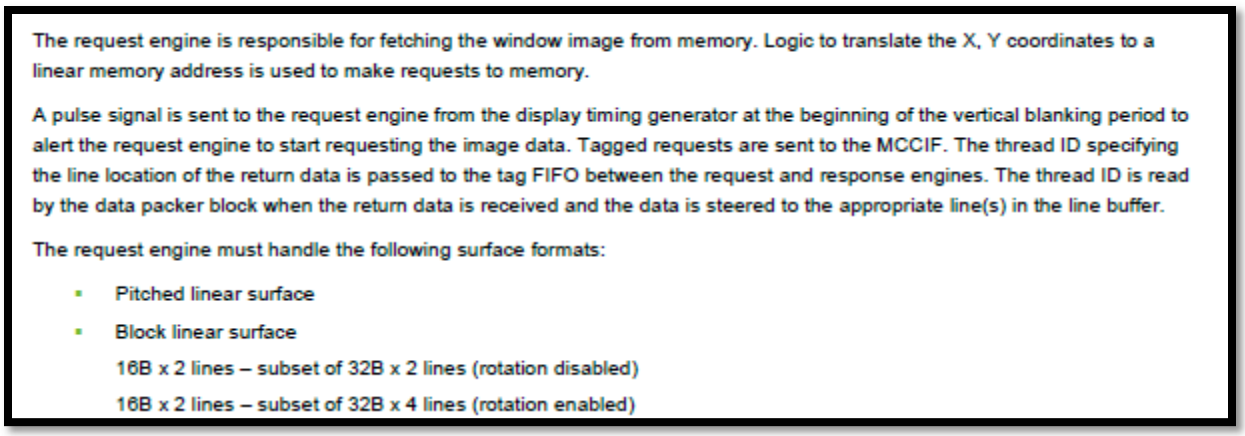
It can control the system and has access to the entire memory map (except for the PCIe® controller, GPU aperture, and CPU internal hardware).

The AVP has 256 Kbytes of local RAM, known as IRAM, for local code and data. IRAM is very low latency to the AVP, typically single cycle, and is also low power. Critical code and data should be stored in IRAM for the best performance and lowest power.

The AVP has access to DRAM either through an 8KB unified cache, or through an uncached memory aperture.

Tegra K1 Technical Reference Manual, NVIDIA DOCUMENTATION at 145 (2014) (showing the audio-video processor).

440. On information and belief, one or more of the NVIDIA '979 Products performs a method for delivering the input stream of pixels to the video processing stage.



The request engine is responsible for fetching the window image from memory. Logic to translate the X, Y coordinates to a linear memory address is used to make requests to memory.

A pulse signal is sent to the request engine from the display timing generator at the beginning of the vertical blanking period to alert the request engine to start requesting the image data. Tagged requests are sent to the MCCIF. The thread ID specifying the line location of the return data is passed to the tag FIFO between the request and response engines. The thread ID is read by the data packer block when the return data is received and the data is steered to the appropriate line(s) in the line buffer.

The request engine must handle the following surface formats:

- Pitched linear surface
- Block linear surface

  16B x 2 lines – subset of 32B x 2 lines (rotation disabled)

  16B x 2 lines – subset of 32B x 4 lines (rotation enabled)

Tegra K1 Technical Reference Manual, NVIDIA DOCUMENTATION at 1454 (2014).

441. On information and belief, one or more of the NVIDIA '979 Products performs a method comprising establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels.

442. On information and belief, one or more of the NVIDIA '979 Products performs a method comprising storing pixels from the input stream into a first set of line butters, the pixels stored in the first set of line butters including pixels for the established window size.

443. On information and belief, one or more of the NVIDIA '979 Products performs a method comprising prefetching the stored pixels from the first set of line butters into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size.

29. On information and belief, one or more of the NVIDIA '979 Products performs a method comprising fetching the fixed number of pixels from the second set of line buffers for the video processing stage.

30. On information and belief, one or more of the NVIDIA '979 Products performs a method wherein storing pixels from the input stream into a first set of line butters, the pixels stored in the first set of line butters including pixels for the established window size, prefetching the stored pixels from the first set of line butters into a second set of line buffers, and fetching the fixed number of pixels from the second set of line buffers for the video processing stage are performed concurrently.

31. On information and belief, the NVIDIA '979 Products are available to businesses and individuals throughout the United States.

32. On information and belief, the NVIDIA '979 Products are provided to businesses and individuals located in Delaware.

33. By making, using, testing, offering for sale, and/or selling products and services for motion compensation in video signal processing, including but not limited to the NVIDIA '979

Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '979 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

444. On information and belief, NVIDIA also indirectly infringes the '979 patent by actively inducing infringement under 35 USC § 271(b).

445. NVIDIA has had knowledge of the '979 patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '979 patent and knew of its infringement, including by way of this lawsuit.

446. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '979 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '979 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '979 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '979 Products that have the capability of operating in a manner that infringe one or more of the claims of the '979 patent, including at least claim 1, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '979 Products to utilize the products in a manner that directly infringe one or more claims of the '979 patent.[35] By providing instruction and training to customers and end-users on how to use the NVIDIA '979 Products in a manner that directly infringes one or more claims of

[35] *See, e.g.*, *NVIDIA Tegra 4 Family CPU Architecture*, NVIDIA WHITEPAPER (2013); Salini Gupta, *Introduction to OpenCV for Tegra*, GPU TECHNOLOGY CONFERENCE PRESENTATION; *NVIDIA Tegra K1 Mobile Processor*, NVIDIA TECHNICAL REFERENCE MANUAL (Oct. 15, 2014); *NVIDIA Tegra X1 Mobile Processor*, NVIDIA TECHNICAL REFERENCE MANUAL (Dec. 6, 2016); *NVIDIA Jetson TX2*, NVIDIA OEM PRODUCT DESIGN GUIDE (Sept. 12, 2017).

the '979 patent, including at least claim 1, NVIDIA specifically intended to induce infringement of the '979 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '979 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '979 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '979 patent, knowing that such use constitutes infringement of the '979 patent.

447. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '979 patent.

448. As a result of NVIDIA's infringement of the '979 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

COUNT XIII
INFRINGEMENT OF U.S. PATENT NO. 6,421,090

449. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

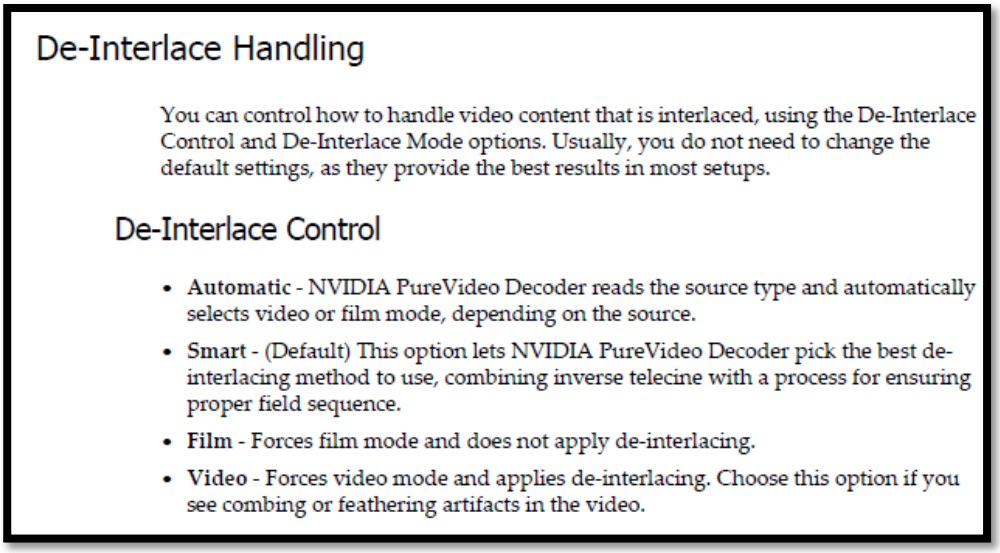
450. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for interpolating a pixel during the interlacing of video signals.

451. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA GTX graphics cards, including the: GeForce GTX 1080 Ti; GeForce GTX 1080; GeForce GTX 1070 Ti; GeForce GTX 1070; GeForce GTX 1060 Ti; GeForce GTX 1060; and NVIDIA Titan Xp (collectively, the "NVIDIA '090 Product(s)").

452. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '090 Products in regular business operations.

453. On information and belief, one or more of the NVIDIA '090 Products include technology for interpolating a pixel during the interlacing of a video signal.

454. The NVIDIA '090 Products then use various algorithms to deinterlace the video signal including through generating a motion value representative of the motion between successive frames about the pixel by segmenting an image into a plurality of multi-pixel segments and comparing the differences with respect to each segment in successive frames. For example, in the below excerpt from NVIDIA documentation adaptive deinterlacing is used wherein motion between frames is detected in the interlaced video stream.



De-Interlace Handling

You can control how to handle video content that is interlaced, using the De-Interlace Control and De-Interlace Mode options. Usually, you do not need to change the default settings, as they provide the best results in most setups.

De-Interlace Control

- **Automatic** - NVIDIA PureVideo Decoder reads the source type and automatically selects video or film mode, depending on the source.
- **Smart** - (Default) This option lets NVIDIA PureVideo Decoder pick the best de-interlacing method to use, combining inverse telecine with a process for ensuring proper field sequence.
- **Film** - Forces film mode and does not apply de-interlacing.
- **Video** - Forces video mode and applies de-interlacing. Choose this option if you see combing or feathering artifacts in the video.

NVIDIA PUREVIDEO DECODER USER'S GUIDE – VERSION 1.02-196 at 14 (2006).

455. On information and belief, one or more of the NVIDIA '090 Products process a video signal including at least two fields of interlaced scan lines, with each scan line containing a series of pixels having intensity values.

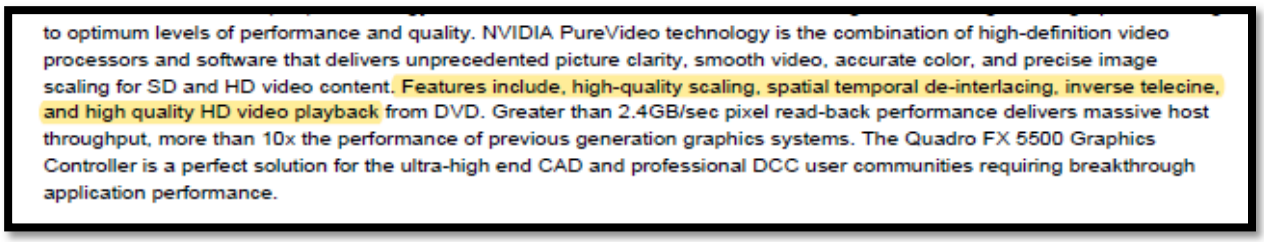
456. NVIDIA '090 Products in HD post-processing improve the quality of a video stream by taking the interlaced video signal and detecting an edge direction about the pixel in the

interlaced video stream and then performing an edge adaptive interpolation at the pixel using the detected edge direction.

> NVIDIA PureVideo technology provides hardware acceleration for decoding H.264, VC-1, WMV and MPEG-2 movies and performs post processing techniques on the decoded high definition content, including spatial-temporal de-interlacing and inverse telecine. This provides consumers with precise images that have up to six times the detail of standard DVD movies. The PureVideo discrete video processing core offloads the CPU and 3D engine of complex video tasks, freeing the PC to run multiple applications simultaneously, while consuming less power.

NVIDIA First To Deliver High-Definition Video Processing For All Desktop and Notebook PC Market Segments, NVIDIA PRESS RELEASE (2006).

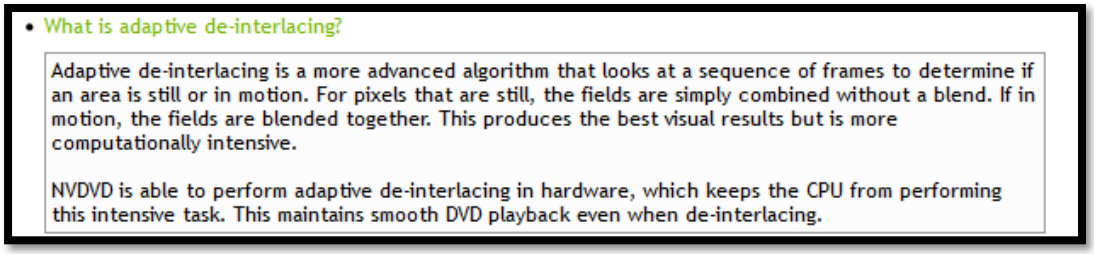
457. On information and belief, one or more of the NVIDIA '090 Products generate a motion value representative of the motion between successive frames about the pixel. The purpose of considering multiple frames is described in a summary of the NVIDIA '090 Product deinterlacing technologies.


to optimum levels of performance and quality. NVIDIA PureVideo technology is the combination of high-definition video processors and software that delivers unprecedented picture clarity, smooth video, accurate color, and precise image scaling for SD and HD video content. Features include, high-quality scaling, spatial temporal de-interlacing, inverse telecine, and high quality HD video playback from DVD. Greater than 2.4GB/sec pixel read-back performance delivers massive host throughput, more than 10x the performance of previous generation graphics systems. The Quadro FX 5500 Graphics Controller is a perfect solution for the ultra-high end CAD and professional DCC user communities requiring breakthrough application performance.

NVIDIA Quadro FX 5500 PCIe Graphics Board and Optional G-Sync Card, NVIDIA DATASHEET at 1 (2007) (emphasis added).

458. On information and belief, one or more of the NVIDIA '090 Products detect an edge direction about the pixel.

459. On information and belief, one or more of the NVIDIA '090 Products perform a motion adaptive interpolation at the pixel. As described in the following excerpt from NVIDIA's documentation the NVIDIA PureVideo technology (which is incorporated into NVIDIA's Products) generates vectors and selects the best data to build a progressive frame from video data that is interpolated from several vectors using video frames that are in front of the frame that is being constructed.



NVIDIA FAQ, NVIDIA WEBSITE (last visited October 2018), *available at*: https://www.nvidia.com/object/nvdvd_faq.

460. On information and belief, the NVIDIA '090 Products are available to businesses and individuals throughout the United States.

461. On information and belief, the NVIDIA '090 Products are provided to businesses and individuals located in Delaware.

462. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '090 patent by, among other things, making, using, offering for sale, and/or selling technology for interpolating a pixel during the deinterlacing of a video signal, including but not limited to the NVIDIA '090 Products.

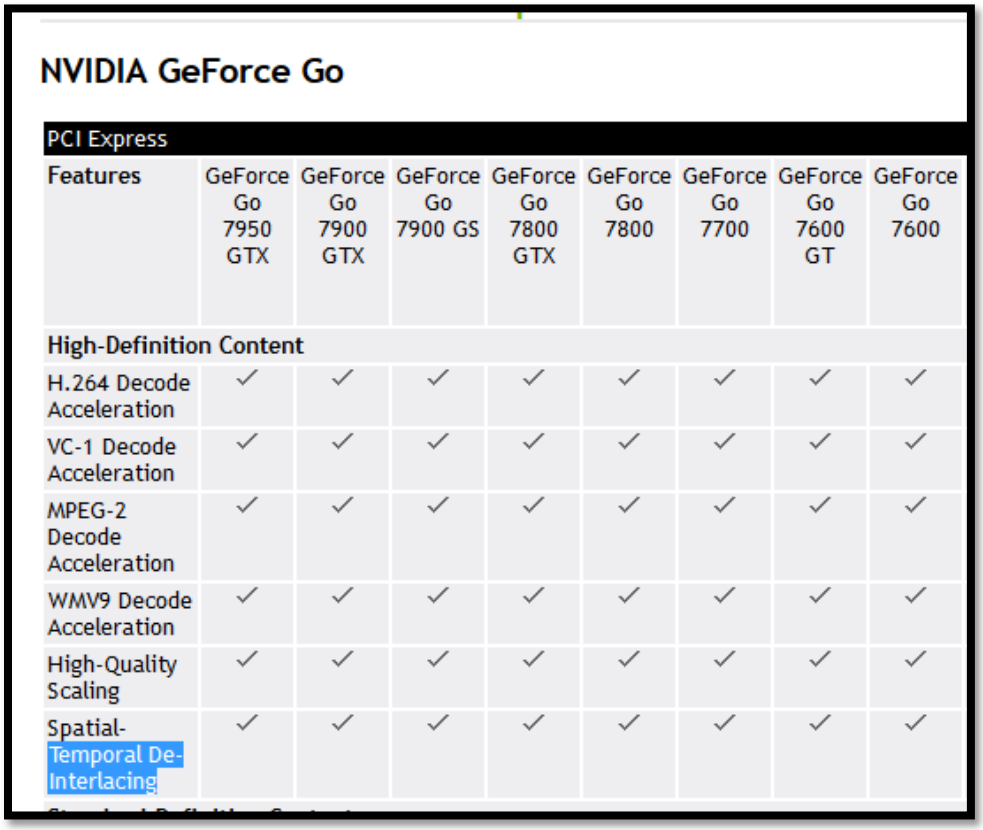
463. On information and belief, the NVIDIA '090 Products interpolate a pixel during the deinterlacing of video signals.

464. On information and belief, the NVIDIA '090 Products process video signals that include at least two fields of interlaced scan lines. Each scan line in the video signal includes a series of pixels having respective intensity values.

465. On information and belief, the NVIDIA '090 Products generate a motion value representative of the motion between successive frames about the pixel by segmenting an image into a plurality of multi-pixel segments and compares the differences with respect to each segment in successive frames.

466. On information and belief, the NVIDIA '090 Products detect an edge direction about the pixel.

467. On information and belief, the NVIDIA '090 Products perform an edge adaptive interpolation at the pixel using the detected edge direction. The NVIDIA '090 Products in HD post-processing improve the quality of a video stream by taking the interlaced video signal and detecting an edge direction about the pixel in the interlaced video stream and then performing an edge adaptive interpolation at the pixel using the detected edge direction.



NVIDIA GeForce Go

PCI Express

Features	GeForce Go 7950 GTX	GeForce Go 7900 GTX	GeForce Go 7900 GS	GeForce Go 7800 GTX	GeForce Go 7800	GeForce Go 7700	GeForce Go 7600 GT	GeForce Go 7600
High-Definition Content								
H.264 Decode Acceleration	✓	✓	✓	✓	✓	✓	✓	✓
VC-1 Decode Acceleration	✓	✓	✓	✓	✓	✓	✓	✓
MPEG-2 Decode Acceleration	✓	✓	✓	✓	✓	✓	✓	✓
WMV9 Decode Acceleration	✓	✓	✓	✓	✓	✓	✓	✓
High-Quality Scaling	✓	✓	✓	✓	✓	✓	✓	✓
Spatial-Temporal De-Interlacing	✓	✓	✓	✓	✓	✓	✓	✓

PureVideo – Product Comparison, NVIDIA WEBSITE (last visited October 2018), *available at*: https://www.nvidia.com/object/purevideo_geforcego_comparison.html.

468. On information and belief, the NVIDIA '090 Products perform a motion adaptive interpolation at the pixel using the generated motion value by comparing segments of pixels about the pixel from at least three successive frames.

469. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the NVIDIA '090 Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '090 patent, including at least claim 5 pursuant to 35 U.S.C. § 271(a).

470. On information and belief, NVIDIA also indirectly infringes the '090 patent by actively inducing infringement under 35 USC § 271(b).

471. NVIDIA has had knowledge of the '090 patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '090 patent and knew of its infringement, including by way of this lawsuit.

472. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '090 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '090 patent. NVIDIA performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '090 patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '090 Products that have the capability of operating in a manner that infringe one or more of the claims of the '090 patent, including at least claim 5, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '090 Products to utilize the products in a manner that directly infringe one or more claims of the '090 patent.[36] By providing instruction and training to customers and end-users on

[36] *See, e.g.*, *Release 396 Graphics Drivers for Windows, Version 399.07*, RELEASE NOTES (Aug. 27, 2018); *Release 390 Graphics Drivers for Windows, Version 390.77*, RELEASE NOTES (Jan.

how to use the NVIDIA '090 Products in a manner that directly infringes one or more claims of the '090 patent, including at least claim 5, NVIDIA specifically intended to induce infringement of the '090 patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '090 Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '090 patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '090 patent, knowing that such use constitutes infringement of the '090 patent.

473. The '090 patent is well-known within the industry as demonstrated by multiple citations to the '090 patent in published patents and patent applications assigned to technology companies and academic institutions. NVIDIA is utilizing the technology claimed in the '090 patent without paying a reasonable royalty. NVIDIA is infringing the '090 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

474. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '090 patent.

475. As a result of NVIDIA's infringement of the '090 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

29, 2018); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017).

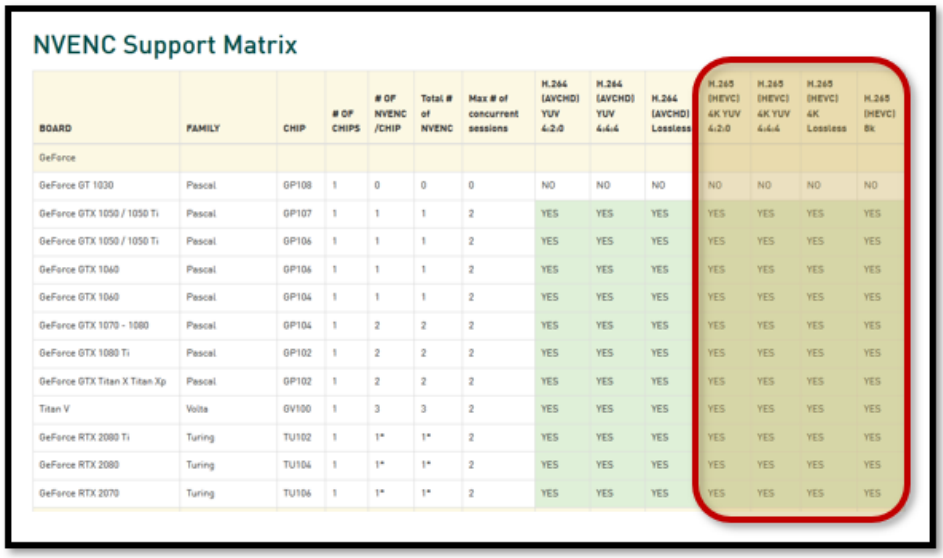
COUNT XIV
INFRINGEMENT OF U.S. PATENT NO. 6,782,054

476. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

477. NVIDIA designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion estimation in a sequence of moving video pictures.

478. NVIDIA designs, makes, sells, offers to sell, imports, and/or uses NVIDIA products containing H.265 encoding technology including: GeForce GTX 1050 / 1050 Ti, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X Titan Xp, Titan V, Quadro P400 - P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla P4 / P6, Tesla P40, Tesla P100, Tesla V100, GeForce GTX 960 Ti - 980, GeForce GTX 980 Ti, GeForce GTX Titan X, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1050 / 1050 Ti, GeForce GTX 1060, GeForce GTX 1060, GeForce GTX 1070 - 1080, GeForce GTX 1080 Ti, GeForce GTX Titan X Titan Xp, Titan V, Quadro M4000, Quadro M5000, Quadro M6000, Quadro M2000, Quadro P400, Quadro P600, Quadro P620, Quadro P1000, Quadro P2000, Quadro P4000, Quadro P5000, Quadro P6000, Quadro GP100, Quadro GV100, Tesla M4, Tesla M40, Tesla M6, Tesla M60, Tesla P4, Tesla P6, Tesla P40, Tesla P100, and Tesla V100 (collectively, the "NVIDIA '054B Products").

479. The NVIDIA '054B Products enable HEVC video encoding. The following excerpt from the NVIDIA Video Encode and Decode GPU Support Matrix identifies that the NVIDIA '054B Products comply with the HEVC standard for encoding data.

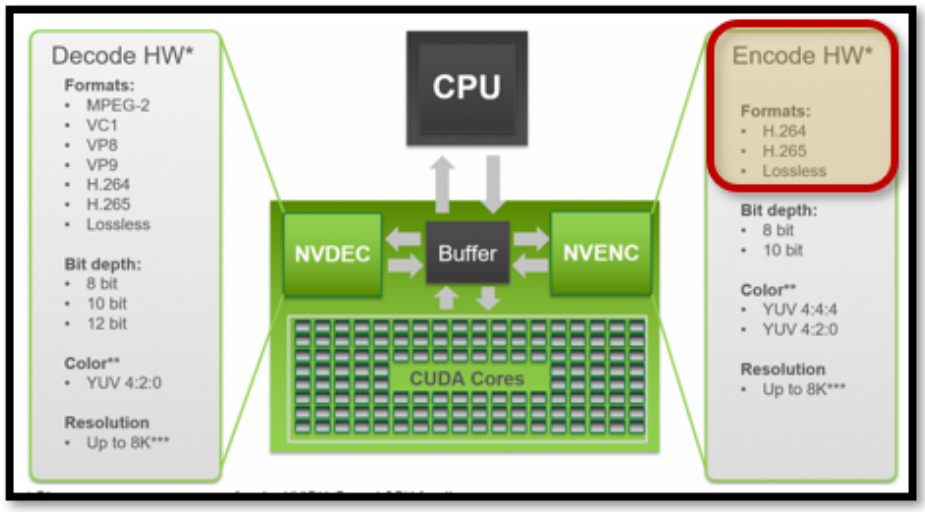


NVENC Support Matrix

BOARD	FAMILY	CHIP	# OF CHIPS	# OF NVENC /CHIP	Total # of NVENC	Max # of concurrent sessions	H.264 (AVCHD) YUV 4:2:0	H.264 (AVCHD) YUV 4:4:4	H.264 (AVCHD) Lossless	H.265 (HEVC) 4K YUV 4:2:0	H.265 (HEVC) 4K YUV 4:4:4	H.265 (HEVC) 4K Lossless	H.265 (HEVC) 8k
GeForce													
GeForce GT 1030	Pascal	GP108	1	0	0	0	NO	NO	NO	NO	NO	NO	NO
GeForce GTX 1050 / 1050 Ti	Pascal	GP107	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1050 / 1050 Ti	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP106	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1060	Pascal	GP104	1	1	1	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1070 - 1080	Pascal	GP104	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX 1080 Ti	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
GeForce GTX Titan X Titan Xp	Pascal	GP102	1	2	2	2	YES	YES	YES	YES	YES	YES	YES
Titan V	Volta	GV100	1	3	3	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080 Ti	Turing	TU102	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2080	Turing	TU104	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES
GeForce RTX 2070	Turing	TU106	1	1*	1*	2	YES	YES	YES	YES	YES	YES	YES

NVIDIA Video Encode and Decode GPU Support Matrix, NVIDIA DEVELOPER WEBSITE, *available at*: https://developer.nvidia.com/video-encode-decode-gpu-support-matrix (annotation showing products that enable HEVC encoding in compliance with the HEVC standard).

480. The NVIDIA '054B Products contain hardware base encoding that meets the requirements of the HEVC standard. The below excerpt from NVIDIA documentation shows that H.265 encoding is supported by the "NVENC" (the NVIDIA Video Encoder).



NVIDIA Video Codec SDK, NVIDIA WEBSITE (last visited October 2018), *available at*: https://developer.nvidia.com/nvidia-video-codec-sdk (annotation showing support for the H.265 encoding standard).

481. NVIDIA documentation establishes that the NVIDIA '054B Products contain all the functionality required for the H.265 Main Profile and are complaint with the HEVC standard.

Feature	Description	Kepler GPUs	First generation Maxwell GPUs	Second generation Maxwell GPUs
H.264 Base, Main, High Profiles	YUV 4:2:0 Encoding.	✓	✓	✓
H.264 4:4:4 and Lossless	Regular YUV 4:4:4 and Lossless Encoding.	×	✓	✓
H.265 Main Profile	YUV 4:2:0 Encoding.	×	×	✓
H264 Motion Estimation (ME) only Mode	Capability to provide Macroblock level motion vectors and intra/inter modes	×	✓	✓
Support for ARGB Input	Capability to accept RGB input for limited color spaces.	✓	✓	✓

NVIDIA VIDEO ENCODER APPLICATION NOTE at 7 (November 2015) (emphasis added).

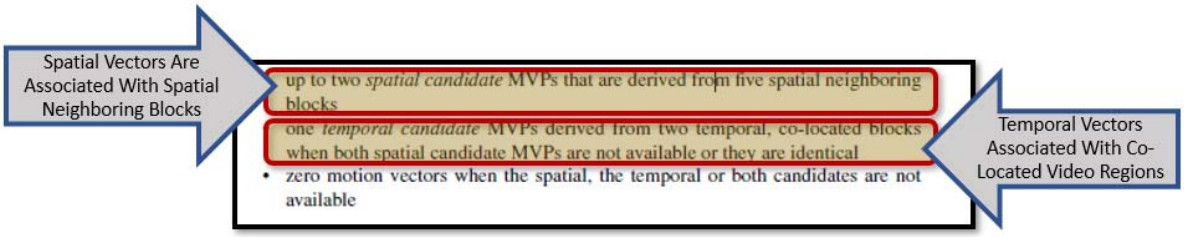
482. On information and belief, one or more NVIDIA subsidiaries and/or affiliates use the NVIDIA '054B Products in regular business operations.

On information and belief, one or more of the NVIDIA '054B Products include technology for motion estimation in a sequence of moving video pictures. In addition, the NVIDIA '054B Products perform H.265 video encoding using a motion estimator. "Furthermore, the encoder needs to perform motion estimation, which is one of the most computationally expensive operations in the encoder, and complexity is reduced by allowing a small number of candidates." Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 at 1661 (December 2012).

483. On information and belief, NVIDIA has directly infringed and continues to directly infringe the '054B patent by, among other things, making, using, offering for sale, and/or selling

technology for motion estimation in a sequence of moving video pictures, including but not limited to the NVIDIA '054B Products.

484. The NVIDIA '054B Products obtain two or more candidate motion vectors from the motion estimator. The candidate motion vectors are associated with a video region. Specifically, the motion estimator generates a set of candidate motion vectors for a grouping of pixels (prediction unit). The NVIDIA '054B Products generate a set of candidate motion vectors for the group of pixels. The group of pixels that are associated with the motion vector are referred to as a prediction unit and comprise a video region. The below excerpt from documentation regarding the HEVC Encoding process describes that "Motion vectors of the current block are usually correlated with the motion vectors of neighboring blocks in the current picture or in the earlier coded pictures."



Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 116 (September 2014).

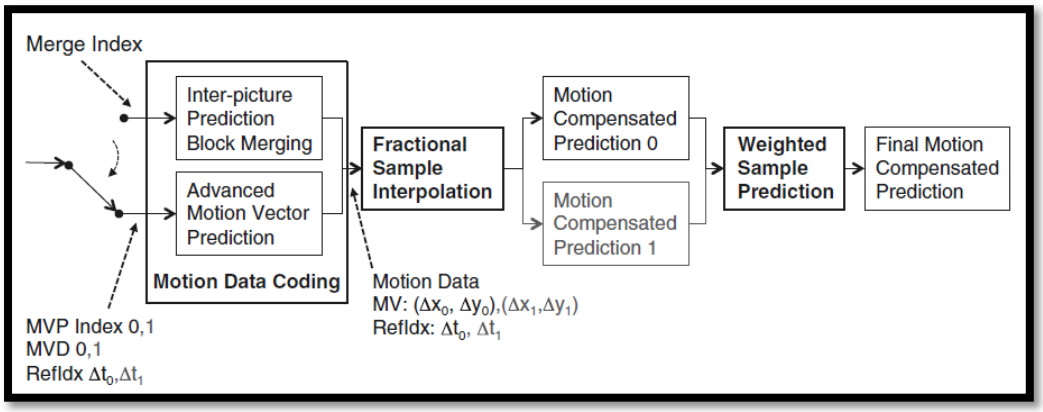
485. The advanced motion vector prediction technologies in the NVIDIA '054B Products perform the steps of motion vector estimation. Specifically, the NVIDIA '054BProducts receive video content and as part of the encoding process divide the video content into coding blocks (aka coding units). The NVIDIA '054B Products further encode video by creating prediction units (PU) that are a basic unit for prediction. The NVIDIA '054B Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates. In

AMVP, the motion vector selection process is composed by two steps wherein the candidate motion vectors are constructed into an index and then the motion vectors are compared. "In AMVP, the motion vector selection process is composed by two steps in encoder implementation. The first step is the motion vector candidate set construction process and the second step is the best motion vector selection step. In the first step, the motion vector candidate set is organized by selecting the motion vectors spatially and temporally." Gwo-Long Li, Chuen-Ching Wang, and Kuang-Hung Chiang, *An Efficient Motion Vector Prediction Method For Avoiding AMVP Data Dependency For HEVC*, 2014 IEEE INTERNATIONAL CONFERENCE ON ACOUSTIC, SPEECH AND SIGNAL PROCESSING (ICASSP) at 7412-13 (2014) (emphasis added).

486. The candidate motion vectors are extracted from a set of previous motion vectors and are associated with a video region by the NVIDIA '054B Products. Specifically, the NVIDIA '054B '572 Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list.

487. The following block diagram illustrates the motion vector selection process in the NVIDIA '054B Products. Specifically, the encoded video data received by the NVIDIA '054B Products is encoded using inter-picture prediction where the motion data of a block is correlated with neighboring blocks. Further, the NVIDIA '054B Products receive data that is encoded using

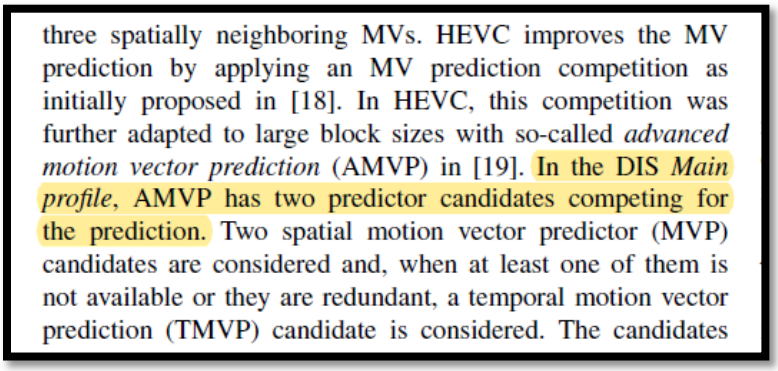
advanced motion vector prediction where the best predictor for each motion block is based on applying a penalty value (also referred to as a cost) to each candidate motion vector.



Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 116 (September 2014).

488. On information and belief, any implementation of the HEVC standard would infringe the '054B patent as every possible implementation of the standard requires: selecting a displacement vector as a best motion vector for a region in a field from a plurality of at least two candidate motion vectors by applying an error function to each of said plural candidate motion vectors, wherein the candidate motion vector with the least error is selected as the displacement vector for the region in the field; wherein said error function comprises a first penalty term that depends on a type of said candidate motion vector and a second penalty term that depends on the position and size of said candidate motion vector.

489. The NVIDIA '054B Products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The NVIDIA '054B Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.

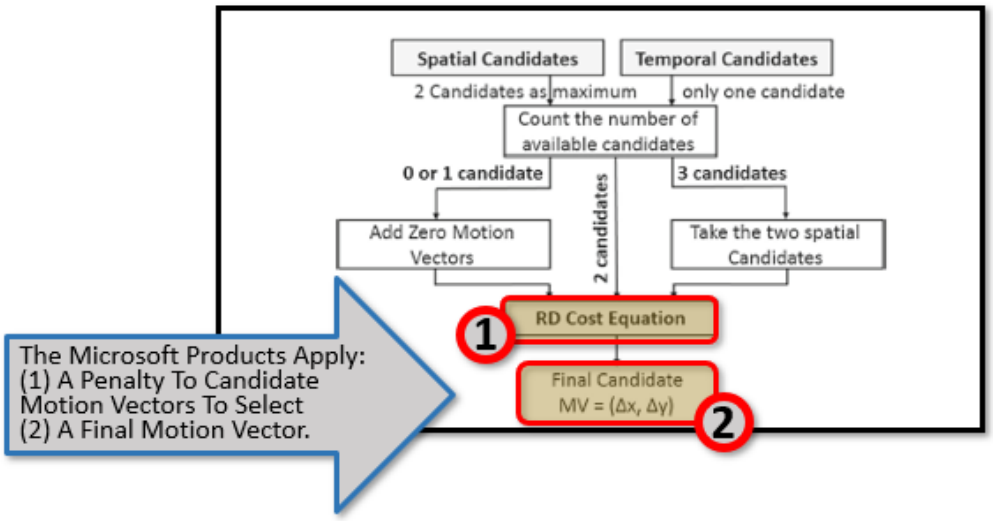


three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle et al, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 at 1723 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

490. The NVIDIA '054B Products apply a cost function (also referred to as an error function and/or penalty). Specifically, the NVIDIA '054B Products apply a rate distortion cost calculation to the two or move candidate motion vectors to select the most suitable candidate in advanced motion vector prediction. The cost function / penalty applied to the candidate motion vectors is based on the type of motion vector and a second penalty based on both the size of the candidate motion vector and the spatial position of the video region within the video image.

491. The following block diagram shows (1) the "RD Cost Equation" which is the error function and (2) the use of the error function to create a "Final Candidate MV." Further, as shown below the motion vectors that is used always contains at least two motion vectors and can be comprised of spatial and temporal candidate motion vectors. The prior pruning of temporal candidates or spatial candidates acts as a first penalty function based on the type of motion vector.



Ahmed M. Abdelsalam, Ahmed Shalaby, Mohammed S. Sayed, *Towards An FPGA-Based HEVC Encoder: A Low Complexity Rate Distortion Scheme For AMVP,* CIRCUITS SYST. SIGNAL PROCESS at 7 (February 10, 2017) (annotations added).

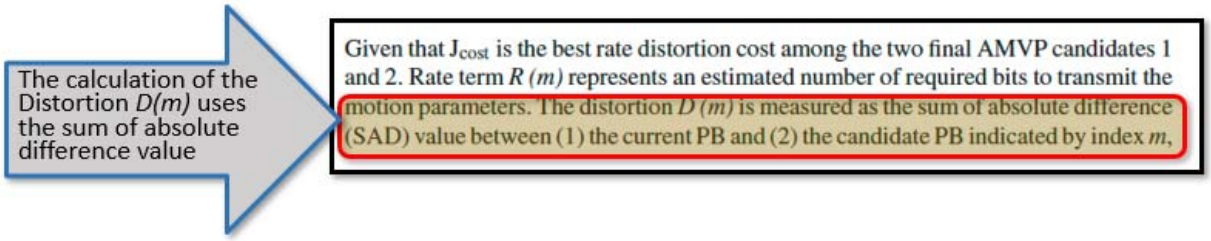
492. NVIDIA's '054B Products use a rate distortion cost ("RD Cost Equation") that selects the best motion vector based on the size of the motion vector and the spatial position of the motion vector. The formula is selected based on the following equation:

$$Jcost = \arg\min_{m \in \{1,2\}} D(m) + \lambda . R(m)$$

493. The NVIDIA '054B Products apply a second penalty based on the RD Cost Equation wherein *J*cost "is the best rate distortion cost among the final two motion vector candidates." Ahmed M. Abdelsalam, Ahmed Shalaby, Mohammed S. Sayed, *Towards An FPGA-Based HEVC Encoder: A Low Complexity Rate Distortion Scheme For AMVP,* CIRCUITS SYST. SIGNAL PROCESS at 7 (February 10, 2017). The two primary factors that are used in calculating the rate distortion cost take into account the size of the motion vectors and the spatial position of the motion vectors.

494. The NVIDIA '054B Products, in calculating the penalty value care the size of the motion vectors. "Rate term R(*m*) represents an estimated number of required bits to transmit the motion parameters." *Id*.

495. The NVIDIA '054B Products, in calculating the penalty value depend on the spatial position of the motion vectors to compare the motion vectors using the distortion D(*m*). The distortion D(*m*) is measured as the sum of absolute difference (SAD) value between (1) the current prediction block and (2) the candidate prediction block indicated by index *m*,

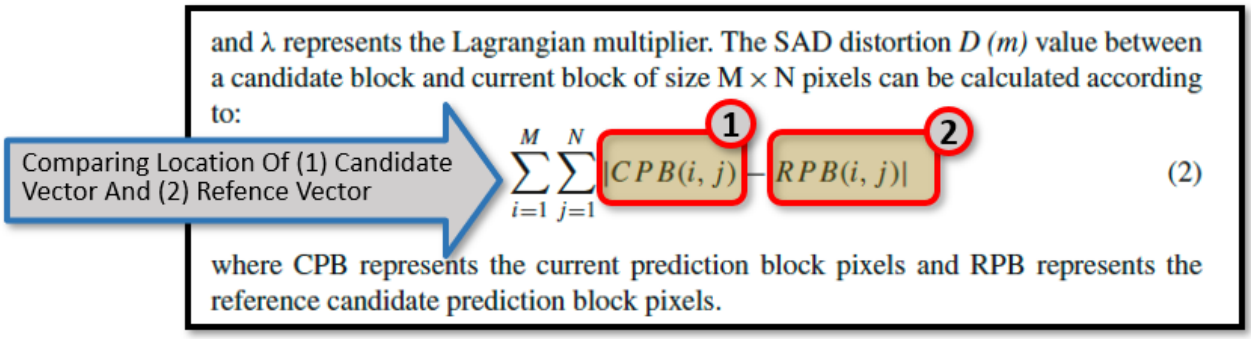


Ahmed M. Abdelsalam, Ahmed Shalaby, Mohammed S. Sayed, *Towards An FPGA-Based HEVC Encoder: A Low Complexity Rate Distortion Scheme For AMVP,* CIRCUITS SYST. SIGNAL PROCESS at 7 (February 10, 2017) (annotations added).

496. On information and belief, by complying with the HEVC standard, the NVIDIA devices – such as the NVIDIA '054B Products - necessarily infringe the '054B patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '054B patent, including but not limited to claim 13. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to NVIDIA's infringement of the '054B patent: "3.110 Prediction Unit Definition;" "6.3.2 Block and quadtree structures;" "6.3.3 Spatial or component-wise partitioning;" "6.4.2 Derivation process for prediction block availability;" "7.3.8.5 Coding unit syntax;" "7.3.8.6 Prediction unit syntax;" "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and

array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process."

497. The NVIDIA '054B Products calculate the penalty based in part on the sum of absolute difference distortion value calculated by comparing the block where the candidate motion vector is located against the location of the reference candidate prediction block. The formula for the calculation of the sum of absolute difference distortion value is shown in the following excerpt relating to the HEVC encoding used by the NVIDIA '054B products.



Ahmed M. Abdelsalam, Ahmed Shalaby, Mohammed S. Sayed, *Towards An FPGA-Based HEVC Encoder: A Low Complexity Rate Distortion Scheme For AMVP,* CIRCUITS SYST. SIGNAL PROCESS at 7 (February 10, 2017) (annotations added).

498. On information and belief, one or more of the NVIDIA '054B Products increase the speed of convergence of motion vectors to improve the convergence process.

499. On information and belief, one or more of the NVIDIA '054B Products perform a method to enhance motion estimation that includes selecting a displacement vector as a best motion vector for a region in a field from a plurality of at least two candidate motion vectors by applying an error function to each of said plural candidate motion vectors, wherein the candidate motion vector with the least error is selected as the displacement vector for the region in the field.

500. On information and belief, one or more of the NVIDIA '054B Products perform a method to enhance motion estimation that includes an error function comprising a first penalty term that depends on a type of the candidate motion vector and a second penalty term that depends on the position and size of the candidate motion vector.

501. On information and belief, the NVIDIA '054B Products are available to businesses and individuals throughout the United States.

502. On information and belief, the NVIDIA '054B Products are provided to businesses and individuals located in Delaware.

503. By making, using, testing, offering for sale, and/or selling products and services for motion estimation in a sequence of moving video pictures, including but not limited to the NVIDIA '054B Products, NVIDIA has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '054B Patent, including at least claim 13 pursuant to 35 U.S.C. § 271(a).

504. On information and belief, NVIDIA also indirectly infringes the '054B Patent by actively inducing infringement under 35 USC § 271(b).

505. NVIDIA has had knowledge of the '054B Patent since at least service of this First Amended Complaint or shortly thereafter, and on information and belief, NVIDIA knew of the '054B Patent and knew of its infringement, including by way of this lawsuit.

506. On information and belief, NVIDIA intended to induce patent infringement by third-party customers and users of the NVIDIA '054B Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. NVIDIA specifically intended and was aware that the normal and customary use of the accused products would infringe the '054B Patent. NVIDIA performed the

acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '054B Patent and with the knowledge that the induced acts would constitute infringement. For example, NVIDIA provides the NVIDIA '054B Products that have the capability of operating in a manner that infringe one or more of the claims of the '054B Patent, including at least claim 13, and NVIDIA further provides documentation and training materials that cause customers and end users of the NVIDIA '054B Products to utilize the products in a manner that directly infringe one or more claims of the '054B Patent.[37] By providing instruction and training to customers and end-users on how to use the NVIDIA '054B Products in a manner that directly infringes one or more claims of the '054B Patent, including at least claim 13, NVIDIA specifically intended to induce infringement of the '054B Patent. On information and belief, NVIDIA engaged in such inducement to promote the sales of the NVIDIA '054B Products, e.g., through NVIDIA user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '054B Patent. Accordingly, NVIDIA has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '054B Patent, knowing that such use constitutes infringement of the '054B Patent.

507. The '054B Patent is well-known within the industry as demonstrated by multiple citations to the '054B Patent in published patents and patent applications assigned to technology

[37] *See, e.g.*, *NVIDIA Quadro P4000*, NVIDIA DATASHEET (2017); *The Right Tools for Professionals: NVIDIA Workstation GPUs*, NVIDIA PROFESSIONAL SOLUTION GUIDE (2017); *NVIDIA GeForce GTX 1080*, NVIDIA WHITEPAPER (2016); *GeForce GTX 1060*, NVIDIA USER GUIDE (2016); *GeForce GTX 1070*, NVIDIA USER GUIDE (2016); *Titan Xp*, NVIDIA USER GUIDE (2017); *NVIDIA Tesla P40 GPU Accelerator*, NVIDIA DATASHEET (2017); *GRID Virtual GPU*, NVIDIA USER GUIDE (Nov. 2016); *Virtual GPU Software*, NVIDIA USER GUIDE (Oct. 2018); *NVIDIA Tesla M60 GPU Accelerator*, NVIDIA DATASHEET (2016); *Real Interactive Expression: NVIDIA Quadro M6000*, NVIDIA DATASHEET (2015); *NVIDIA Tesla V100 GPU Architecture*, NVIDIA WHITEPAPER (2015).

companies and academic institutions. NVIDIA is utilizing the technology claimed in the '054B Patent without paying a reasonable royalty. NVIDIA is infringing the '054B Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

508. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '054B Patent. As a result of NVIDIA's infringement of the '054B Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for NVIDIA's infringement, but in no event less than a reasonable royalty for the use made of the invention by NVIDIA together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Dynamic Data respectfully requests that this Court enter:

A. A judgment in favor of Dynamic Data that NVIDIA has infringed, either literally and/or under the doctrine of equivalents, the '105, '073, '054A, '918, '689, '177, '039, '112, '529, '041, '450, '979, '090, and '054B patents;

B. An award of damages resulting from NVIDIA's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order finding that NVIDIA's infringement was willful, wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate within the meaning of 35 U.S.C. § 284 and awarding to Dynamic Data enhanced damages.

D. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Dynamic Data its reasonable attorneys' fees against NVIDIA.

E. Any and all other relief to which Dynamic Data may show themselves to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Dynamic Data Technologies, LLC requests a trial by jury of any issues so triable by right.

Dated: January 28, 2019

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