IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

DYNAMIC DATA TECHNOLOGIES, LLC, *Plaintiff,* v. ADVANCED MICRO DEVICES, INC., *Defendant*.	Civil Action No. 18-cv-01715-CFC **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Dynamic Data Technologies, LLC ("Dynamic Data") brings this action and makes the following allegations of patent infringement relating to U.S. Patent Nos.: 8,189,105 (the "'105 Patent"); 8,135,073 (the "'073 Patent"); 7,532,220 (the "'220 Patent"); 6,714,257 (the "'257 Patent"); 8,073,054 (the "'054 Patent"); 6,774,918 (the "'918 Patent"); 8,184,689 (the "'689 Patent"); 6,996,177 (the "'177 Patent"); 7,010,039 (the "'039 Patent"); 8,311,112 (the "'112 Patent"); 6,646,688 (the "'688 Patent"); 7,894,529 (the "'529 Patent"); 7,542,041 (the "'041 Patent"); 7,571,450 (the "'450 Patent"); 7,750,979 (the "'979 Patent"); 7,058,227 (the "'227 Patent"); and 6,421,090 (the "'090 Patent") (collectively, the "patents-in-suit"). Defendant Advanced Micro Devices, Inc. ("AMD" or "Defendant") infringes each of the patents-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq*.

CO-PENDING ENFORCEMENT PROCEEDINGS IN THE PEOPLE'S REPUBLIC OF CHINA AND PATENT PORTFOLIO EXPANSION

1. Dynamic Data's portfolio of over 1,200 patent assets encompasses core technologies in the field of image and video processing. The patent portfolio held by Dynamic Data is international in scope and includes several hundred European and Chinese patent grants.

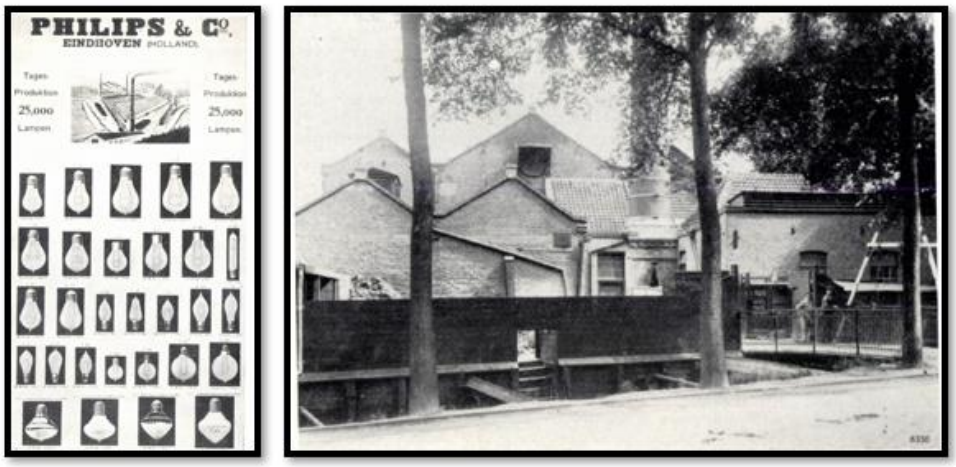
2. In an effort to facilitate the licensing of Philips' foundational technology, Dynamic Data is pursuing remedies for infringement of its patents in venues throughout the world. Contemporaneous to the filing of this First Amended Complaint, Dynamic Data is filing a patent enforcement action against Advanced Micro Devices (China) Co., Ltd. in the Beijing IP Specialized Intellectual Property Tribunal in the People's Republic of China. Dynamic Data is seeking injunctive relief relating to the sale of the following products: AMD Ryzen 3 2200G with Radeon Vega 8 Graphics, AMD Ryzen 3 2200GE with Radeon Vega 8 Graphics, AMD Ryzen 3

3. Dynamic Data's patents arose from the research and development efforts of Koninklijke Philips N.V. ("Philips"). Founded in 1891, for well over a century, Philips pioneered ground breaking technologies, including compact audio cassettes, magnetic resonance imaging (MRI) machines, and compact discs.

4. Dynamic Data's patents arose from the research and development efforts of Koninklijke Philips N.V. ("Philips"). Founded in 1891, for well over a century, Philips pioneered ground breaking technologies, including compact audio cassettes, magnetic resonance imaging (MRI) machines, and compact discs.

5. The groundbreaking inventions in image and video processing taught in the patents-in-suit were pioneered by Philips. Video and image processing were at the heart of Philips' business for over fifty years. In 1891, Philips, then known as Philips & Company, was founded in Eindhoven, Netherlands to manufacture carbon-filament lamps.[1] In the 1920s, Philips began to produce vacuum tubes and small radios, which would augur Philips' later entry into video and audio processing.

[1] Gerard O'Regan, A BRIEF HISTORY OF COMPUTING at 99 (2012).



N.A. Halbertsma, *The Birth of a Lamp Factory In 1891*, PHILIPS TECHNICAL REVIEW, Vol. 23 at 230, 234 (1961).

6. In 1962, Philips introduced the first audio cassette tape.[2] A year later, Philips launched a small battery-powered audio tape recorder that used a cassette instead of a loose spool.[3] Philips C-cassette was later used as the first mass storage device for early personal computers in the 1970s and 1980s.

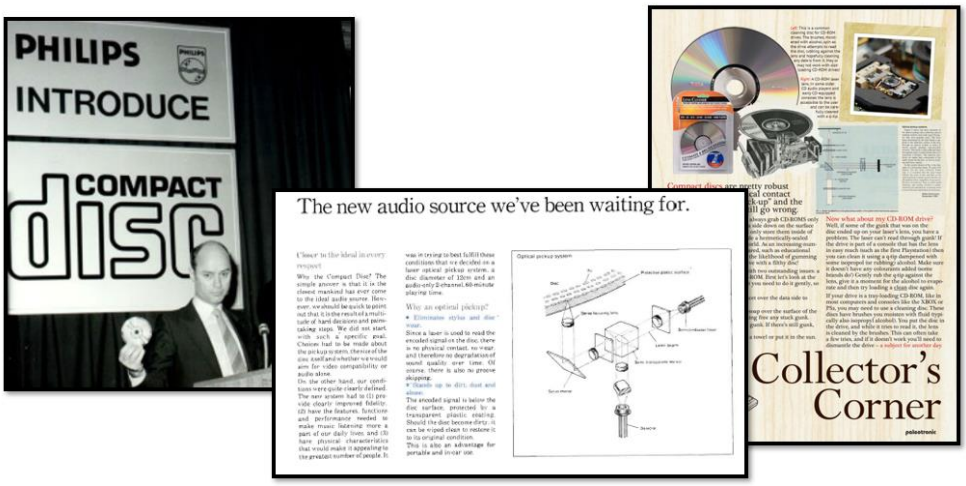
THE ROTARIAN MAGAZINE, Vol. 101 No. 6 at 70 (December 1962) (advertisement showing Philips Norelco device which used cassettes for recording audio for transcription); Fred Chandler, *European Mfrs. Bid For Market Share*, BILLBOARD MAGAZINE AT P-6 (April 8, 1967) (image of the Philips EL 3300 battery-operated tape recorder which was released in 1963); Jan Syrjala, *Car*

[2] Gerard O'Regan, PILLARS OF COMPUTING: A COMPENDIUM OF SELECT, PIVOTAL TECHNOLOGY FIRMS at 172 (2015) ("Philips invented the compact cassette for audio storage in 1962.")

[3] Anthony Pollard, GRAMOPHONE: THE FIRST 75 YEARS at 231 (1998).

Stereo: How Does The Music Sound?, N.Y. TIMES at 2-M (September 25, 1966) (showing Philips's Norelco Cassette "the Philips device has two tiny reels inside it").

7. In 1971, Philips demonstrated the world's first videocassette records (VCR). A year later, Philips launched the world's first home video cassette recorder, the N1500. In 1982, Philips teamed with Sony to launch the Compact Disc; this format evolved into the DVD and later Blu-ray, which Philips launched with Sony in 1997 and 2006 respectively.



Hans Peek, Jan Bergmans, Jos Van Haaren, Frank Toolenaar, and Sorin Stan, ORIGINS AND SUCCESSORS OF THE COMPACT DISC: CONTRIBUTIONS OF PHILIPS TO OPTICAL STORAGE at 15 (2009) (showing image of Joop Sinjou of Philips introducing the compact disc in March 1979); Advertisements for Philip's Compact Disc Products (1982).

8. In the late 1990s and early 2000s, Philips pioneered the development of technologies for encoding and decoding of video and audio content. At the time most of the technologies claimed by the patents in Dynamic Data's portfolio were invented, Philips' subsidiary primarily responsible for Philips' work in this field, Philips Semiconductor was the world's sixth largest semiconductor company.[4] The video encoding technologies developed by Philips

[4] *Company News; Philips in $1 Billion Deal for VLSI Technology*, THE NEW YORK TIMES (May 4, 1999), *available at*: https://www.nytimes.com/1999/05/04/business/company-news-philips-in-1-billion-deal-for-vlsi-technology.html.

Semiconductor enable video streaming on set-top boxes, smartphones, popular gaming consoles, Internet-connected computers, and numerous other types of media streaming devices.

9. Philips Semiconductor dedicated significant research and development resources to advancing the technology of video compression and transmission by reducing file sizes and decreasing the processing resources required to transmit the data.[5] Philips Semiconductor was among the first companies aggressively driving innovation in the field of video processing:

10. The late 1980s and early 1990s saw the announcement of several complex, programmable VSPs. Important examples include chips from Matsushita, NTT, Philips [Semiconductors], and NEC. All of these processors were high-performance parallel processors architected from the ground up for real-time video signal processing. . . . The Philips VSP-1 and NEC processor were probably the most heavily used of these chips.[6]

11. Starting in the 1960s Philips pioneered the development of audio and video technologies that would establish itself as a leader in the field that would later develop into the audio and video encoding fields. Continuing Philips' pioneering history in these fields, the patents-in-suit disclose cutting-edge video compression and transmission technologies.

12. Dynamic Data's patent portfolio includes over 1,200 patent assets, with over 470 issued patents granted by patent offices around the world. Dynamic Data owns numerous patents issued by the United States Patent and Trademark Office, including each of the patents-in-suit, The State Intellectual Property Office of the People's Republic of China,[7] the European Patent

[5] HU, YU HEN, PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: ARCHITECTURE, PROGRAMMING, AND APPLICATIONS, at 190 (Dec. 6, 2001) ("Philips Semiconductors developed early dedicated video chips for specialized video processors.").

[6] *Id.* at 191.

[7] *See, e.g.,* CN100504925C; CN100438609C; CN1679052B; CN1333373C; CN1329870C; CN1303818C.

Office,[8] the German Patent and Trademark Office,[9] the Japan Patent Office,[10] and many other national patent offices.

13. Philips Semiconductor's pioneering work in the area of video processing and encoding has resulted in various inventions that are fundamental to today's video processing technologies. Dynamic Data is the owner by assignment of over 1,200 of these patent assets, which include over 475 patents issued by patent offices around the world.

14. Highlighting the importance of the patents-in-suit is the fact that the patents-in-suit have been cited by over 400 U.S. and international patents and patent applications by a wide variety of the largest companies operating in the field. For example, the patents-in-suit have been cited by companies such as:

- Samsung Electronics Co., Ltd.[11]
- Qualcomm Inc.[12]
- Google LLC[13]
- Intel Corporation[14]
- Broadcom Corporation[15]
- Microsoft Corporation[16]
- Sony Corporation[17]
- Fujitsu Ltd.[18]
- Panasonic Corporation[19]

[8] *See, e.g.*, European Patent Nos. EP1032921B1; EP1650978B1; EP1213700B1; EP1520409B1.

[9] *See, e.g.*, German Patent Nos. DE60120762; DE50110537; DE60126151; DE60348978; DE602004049357.

[10] *See, e.g.*, Japanese Patent Nos. JP4583924B2; JP5059855B2; JP5153336B2; JP4637585B2.

[11] *See, e.g.*, U.S. Patent Nos. 6,930,729; 7,911,537; 7,532,764; 8,605,790; and 8,095,887.

[12] *See, e.g.*, U.S. Patent Nos. 7,840,085; 8,649,437; 8,750,387; 8,918,533; 9,185,439; 9,209,934; 9,281,847; 9,319,448; 9,419,749; 9,843,844; 9,917,874; and 9,877,033.

[13] *See, e.g.*, U.S. Patent No. 8,787,454 and U.S. Patent Appl. No. 10/003,793.

[14] *See, e.g.*, U.S. Patent Nos. 7,554,559; 7,362,377; and 8,462,164.

[15] *See, e.g.*, U.S. Patent Nos. 8,325,273 and 9,377,987.

[16] *See, e.g.*, U.S. Patent Nos. 7,453,939; 7,670,227; 7,408,986; 7,421,129; 7,558,320; and 7,929,599.

[17] *See, e.g.*, U.S. Patent Nos. 7,218,354 and 8,174,615.

[18] *See, e.g.*, U.S. Patent Nos. 7,092,032 and 8,290,308.

[19] *See, e.g.*, U.S. Patent Nos. 8,164,687 and 8,432,495.

- Matsushita Electric Industrial Company Limited[20]

THE PARTIES

DYNAMIC DATA TECHNOLOGIES, LLC

15. Dynamic Data Technologies, LLC ("Dynamic Data" or "Plaintiff") is a limited liability company organized under the laws of Delaware.

16. In an effort to obtain compensation for Philips' pioneering work in the fields of video data encoding, decoding, and transmission, Dynamic Data acquired the patents-in-suit along with the several hundred additional issued United States and international Patents.

17. Dynamic Data pursues the reasonable royalties owed for AMD use of the inventions claimed in Dynamic Data's patent portfolio, which primarily arise from Philips' groundbreaking technology, both here in the United States and throughout the world.

ADVANCED MICRO DEVICES, INC.

18. On information and belief, Advanced Micro Devices, Inc. ("AMD"), is a Delaware corporation with its principal place of business at One AMD Place, Sunnyvale, California 94085. AMD may be served through its registered agent for service of process – The Corporation Trust Company, Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801.

JURISDICTION AND VENUE

19. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

20. Upon information and belief, this Court has personal jurisdiction over AMD in this action because AMD has committed acts within the District of Delaware giving rise to this action

[20] *See, e.g.*, U.S. Patent Nos. 7,362,378 and 7,423,961.

and has established minimum contacts with this forum such that the exercise of jurisdiction over AMD would not offend traditional notions of fair play and substantial justice. Defendant AMD, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patents-in-suit. Moreover, AMD is a Delaware corporation and actively directs its activities to customers located in the State of Delaware.

21. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Defendant AMD is a corporation organized and existing under the law of the State of Delaware, and therefore resides in the District of Delaware.

THE ASSERTED PATENTS

U.S. PATENT NO. 8,189,105

22. U.S. Patent No. 8,189,105 entitled, *Systems and Methods of Motion and Edge Adaptive Processing Including Motion Compensation Features*, was filed on October 17, 2007. The '105 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1258 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '105 Patent. A true and correct copy of the '105 Patent is attached hereto as Exhibit 1.

23. The '105 patent discloses novel systems and methods for processing pixel information based on received motion and edge data.

24. The '105 patent further discloses the use of a blending component (implemented by hardware, software, firmware, combinations thereof, etc.) that implements interpolating intensity of the pixel to equal to the first intensity estimate if motion reliability data is below a threshold.

25. The ‘105 patent in one embodiment teaches using segmentation to average four contiguous pixels into one averaged pixel segment during motion detection.

26. The ’105 Patent and its underlying patent applications and foreign counterparts have been cited by 46 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’105 Patent and its underlying patent application as relevant prior art:

- Flextronics Ap, LLC
- Qingdao Hisense Electronics Co., Ltd.
- Hon Hai Precision Industry Co., Ltd.
- Intel Corporation
- Sony Corporation
- Fujitsu Corporation
- Himax Media Solutions, Inc.
- Ati Technologies Ulc
- Sharp Kabushiki Kaisha
- Xerox Corporation

U.S. PATENT NO. 8,135,073

27. U.S. Patent No. 8,135,073 entitled, *Enhancing Video Images Depending On Prior Image Enhancements*, was filed on December 12, 2003, and claims priority to December 19, 2002. The ‘073 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,799 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘073 Patent. A true and correct copy of the ‘073 Patent is attached hereto as Exhibit 2.

28. The ‘073 Patent discloses novel methods and systems for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

29. The inventions disclosed in the ‘073 Patent reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

30. Accordingly, the technologies disclosed in the ‘073 Patent enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

31. The ‘073 Patent discloses a video decoder comprising an input for receiving a video stream containing encoded frame based video information including an encoded first frame and an encoded second frame.

32. The ‘073 Patent discloses a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame.

33. The ‘073 Patent discloses a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers the motion vectors for the second frame.

34. The ‘073 Patent discloses a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

35. The ‘073 Patent and its underlying patent application have been cited by 36 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘073 Patent and its underlying patent application as relevant prior art:

- Canon Inc.
- Microsoft Corporation

- International Business Machines Corporation
- Qualcomm Inc.
- Digital Fountain Incorporated
- Samsung Electronics Co., Ltd.
- SK Planet Co. Ltd.

U.S. PATENT NO. 7,532,220

36. U.S. Patent No. 7,532,220 entitled, *System For Adaptive Resampling In Texture Mapping*, was filed on July 21, 2004, and claims priority to July 30, 2003. The '220 Patent is subject to a 35 U.S.C. § 154(b) term extension of 446 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '220 Patent. A true and correct copy of the '220 Patent is attached hereto as Exhibit 3.

37. The '220 Patent discloses novel methods and apparatuses for resampling a primitive from texture space to screen space.

38. The inventions disclosed in the '220 Patent enable an optimal resampling algorithm for primitives in three-dimensional graphics models by choosing between algorithms dynamically per primitive, based upon the size of the primitive.

39. The inventions disclosed in the '220 Patent further enable optimal resampling for primitives by balancing between the quality of the resampling, thus rendering a more realistic three-dimensional graphic, and considering system limitations such as available processor capacity and memory size.

40. The inventions disclosed in the '220 Patent solve a technical problem of creating realistic three-dimensional graphic images through enhanced graphics processing techniques.

41. The inventions disclosed in the '220 Patent improve the operations of computer components utilized in graphics processing by balancing system limitations such as processor

capacity and memory size with the objective of creating a high-quality three-dimensional graphic image.

42. In one embodiment, the ‘220 Patent discloses an apparatus for mapping primitives of a three-dimensional graphics model from a texture space to a screen space. The apparatus includes a texture memory for storing texture maps.

43. In one embodiment, the ‘220 Patent discloses an apparatus includes a resampler being operative to, for each primitive, resample data from a texture map that corresponds to the primitive to corresponding pixel data defining a portion of a display image that corresponds to the primitive. The resampler is operative to select a resampling algorithm for performing the resampling from multiple resampling algorithms. The selection is dependent on a size of the primitive.

44. The ‘220 Patent and its underlying patent application have been cited by 18 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘220 Patent and its underlying patent application as relevant prior art:

- Intel Corporation
- Microsoft Corporation
- Nvidia Corporation
- Panasonic Corporation
- Qualcomm Inc.
- Disney Enterprises Inc.
- China Digital Video (Beijing) Limited

U.S. PATENT NO. 6,714,257

45. U.S. Patent No. 6,714,257 entitled, *Color Key Preservation During Sample Rate Conversion*, was filed on June 29, 2001. The ‘257 Patent is subject to a 35 U.S.C. § 154(b) term extension of 445 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘257 Patent. A true and correct copy of the ‘257 Patent is attached hereto as Exhibit 4.

46. The ‘257 Patent claims specific methods and systems for processing a keyed image. For example, one or more of the ‘257 Patent claims describe a method for scaling a keyed image where a key-only image corresponding to key regions in the keyed images is created. The key-only image is scaled to form a scaled key-only image. The keyed image is scaled for form a scaled keyed image, and the scaled key-only image is merged with the scaled keyed image.

47. The ‘257 Patent discloses additional improvements to scaling and filtering color-keyed images.

48. The inventions taught in the ‘257 Patent achieve improvements in scaling and filtering color-keyed images by allowing the replacement of color-keyed regions with background image information, without introducing visible artifacts.

49. The ‘257 Patent discloses embodiments that extract the color-keyed regions from a color-keyed image, and independently scale the color-keyed regions and the non-color keyed regions.

50. The ‘257 Patent discloses that blurring of edges in non-color-key regions are minimized by extending the non-color-key colors into color-keyed regions after the color-keyed information is extracted from the color-keyed image.

51. The ‘257 Patent has been cited by several United States and International patents and patent applications as relevant prior art. Specifically, patents issued to Microsoft Corporation, Texas Instruments Incorporated, Samsung Corporation, Marvell International Limited, Innolux Corporation, and China Digital Video (Beijing) Limited have all cited the ‘257 patent as relevant prior art.

U.S. PATENT NO. 8,073,054

52. U.S. Patent No. 8,073,054 entitled, *Unit For And Method Of Estimating A Current Motion Vector*, was filed on December 12, 2002, and claims priority to January 17, 2002. The

‘054 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,162 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘054 Patent. A true and correct copy of the ‘054 Patent is attached hereto as Exhibit 5.

53. The ‘054 Patent discloses novel methods and apparatuses for estimating a current motion vector for a group of pixels of an image.

54. The inventions disclosed in the ‘054 Patent enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

55. The ‘054 Patent discloses a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

56. The ‘054 Patent discloses a motion estimation unit comprising a match error unit for calculating match errors of respective candidate motion vectors.

57. The ‘054 Patent discloses a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

58. The ‘054 Patent discloses a motion estimation unit that calculates the further candidate motion vector on the basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion

vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different.

59. The ‘054 Patent discloses a motion estimation unit that arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

60. The ‘054 Patent and its underlying patent application have been cited by 14 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘054 Patent and its underlying patent application as relevant prior art:

- Canon Inc.
- Huawei Technologies, Ltd.
- Imagination Technologies Ltd.
- MediaTek Inc.
- Panasonic Corp.
- Samsung Electronics Co., Ltd.
- Siemens Healthcare GmbH
- Tencent Technology (Shenzhen) Co., Ltd.

U.S. PATENT NO. 6,774,918

61. U.S. Patent No. 6,774,918 entitled, *Video Overlay Processor with Reduced Memory And Bus Performance Requirements*, was filed on June 28, 2000. The ‘918 Patent is subject to a 35 U.S.C. § 154(b) term extension of 591 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘918 Patent. A true and correct copy of the ‘918 Patent is attached hereto as Exhibit 6.

62. The ‘918 Patent claims specific methods and systems for providing an overlay such as a cursor in an on-screen display in a consumer electronic device. On-screen display (OSD) data for generating an image on a display device are downloaded to an OSD unit on an integrated circuit.

63. The ‘918 Patent discloses downloading on-screen display (OSD) data for generating an image on a display device.

64. The ‘918 Patent further discloses downloading the on-screen display (OSD) data in segments separated by gaps.

65. The ‘918 Patent further discloses, during a gap in downloading the on-screen display data, downloading an amount of overlay data for generating an overlay on the image generated on a display device.

66. Further, the ‘918 Patent discloses that the overlay data downloaded during a gap comprises a portion of the overlay data.

67. The inventions disclosed in the ‘918 Patent improve the operation and efficiency of computer components because only a portion of the overlay data is downloaded during each burst gap, thus reducing the amount of memory needed to store the overlay data. The inventions disclosed in the ‘918 Patent further eliminate the requirement that on-chip memory be large enough to hold the data needed for an entire overlay. Instead, only one line or a part of one line of the overlay needs to be stored on-chip.

68. The ‘918 Patent claims a technical solution to a problem unique to video processing.

69. The ‘918 Patent has been cited by several United States patents and patent applications as relevant prior art. Specifically, patents issued to Realtek Semiconductor Corp., Samsung Electronics Co., Ltd., and Thomson Licensing SA have all cited the ‘918 Patent as relevant prior art.

U.S. PATENT NO. 8,184,689

70. U.S. Patent No. 8,184,689 entitled, *Method Video Encoding And Decoding Preserving Cache Localities*, was filed on August 7, 2006, and claims priority to August 17, 2005.

The ‘689 Patent is subject to a 35 U.S.C. § 154(b) term extension of 948 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘689 Patent. A true and correct copy of the ‘689 Patent is attached hereto as Exhibit 7.

71. The ‘689 Patent discloses novel methods and apparatuses for encoding and decoding video data.

72. The inventions disclosed in the ‘689 Patent processing time and power consumption associated with encoding and decoding video stream data is reduced by reducing off-chip memory accesses through using simultaneous encoded/decoded images as a reference image for encoding/decoding at least one of the other simultaneously encoded/decoded images.

73. The ‘689 Patent discloses a method for encoding and decoding a video stream, including a plurality of images in a video processing apparatus having a processing unit coupled to a first memory, further comprising a second memory.

74. The ‘689 Patent discloses a method for encoding and decoding a video stream comprising providing a subset of image data stored in the second memory in the first memory.

75. The ‘689 Patent discloses a method for encoding and decoding a video stream comprising simultaneous encoding/decoding of more than one image of the video stream, by accessing said subset, wherein the simultaneously encoding/decoding is performed by access sharing to at least one image.

76. The ‘689 Patent and its underlying patent application have been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to Fujitsu Ltd., Qualcomm Inc., Sony Corporation, Sun Patent Trust, and VIXS Systems Incorporated have all cited the ‘689 Patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 6,996,177

77. U.S. Patent No. 6,996,177 entitled, *Motion Estimation*, was filed on July 24, 2000, and claims priority to August 22, 1999. The '177 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,103 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '177 Patent. A true and correct copy of the '177 Patent is attached hereto as Exhibit 8.

78. The '177 Patent claims specific methods and devices for motion estimation and motion-compensated picture signal processing.

79. The '177 Patent discloses a motion vector estimation method and device that carries out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors.

80. The '177 Patent discloses a motion vector estimation method and device that determines at least a most frequently occurring block-based motion vector.

81. The '177 Patent discloses a motion vector estimation method and device that carries out a global motion vector estimation process using at least the most frequently occurring block-based motion vector to obtain a global motion vector.

82. The '177 Patent discloses a motion vector estimation method and device that applies the global motion vector as a candidate vector to the block-based motion vector estimation process.

83. The inventions disclosed in the '177 Patent improve the operation of the computer components necessary to the performance of picture signal processing by reducing the load on the central processing unit.

84. The '177 Patent has been cited by 16 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '177 Patent as relevant prior art:

- Qualcomm Incorporated
- LG Electronics
- Microsoft Corporation
- Samsung Electronics Co., Ltd.
- VIXS Systems Incorporated
- General Instrument Corporation

U.S. PATENT NO. 7,010,039

85. U.S. Patent No. 7,010,039 (the "'039 Patent") entitled, *Motion Estimator for Reduced Halos in MC Up-Conversion*, was filed on May 15, 2001, and claims priority to May 18, 2000. The '039 Patent is subject to a 35 U.S.C. § 154(b) term extension of 768 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '039 Patent. A true and correct copy of the '039 Patent is attached hereto as Exhibit 9.

86. The '039 Patent claims specific methods and apparatuses detecting motion at a temporal intermediate position between previous and next images. The inventions disclosed in the '039 Patent solve a problem wherein an estimator estimating motion between two successive pictures from a video sequence cannot perform well in areas where covering or uncovering occurs.

87. The '039 Patent solves this problem by carrying out the optimization at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

88. The '039 Patent discloses a method and apparatus for detecting motion at a temporal intermediate position between previous and next images.

89. The '039 Patent discloses the use of a criterion function for selecting and optimizing candidate vectors.

90. The '039 Patent further discloses a criterion function that depends on data from both previous and next images and in which the optimizing is carried out at the temporal intermediate position in non-covering and non-uncovering areas, characterized in that the

optimizing is carried out at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

91. The ‘039 Patent and its related patents have been cited by 30 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘039 Patent family as relevant prior art:

- Qualcomm Incorporated
- Panasonic Corporation
- Samsung Electronics Co., Ltd.
- Matsushita Electric Industrial Co., Ltd.
- Sharp Kabushiki Kaisha
- Integrated Device Technology, Inc.
- Zoran Corporation

U.S. PATENT NO. 8,311,112

92. U.S. Patent No. 8,311,112 entitled, *System And Method For Video Compression Using Predictive Coding*, was filed on December 31, 2008. The ‘112 Patent is subject to a 35 U.S.C. § 154(b) term extension of 847 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘112 Patent. A true and correct copy of the ‘112 Patent is attached hereto as Exhibit 10.

93. The ‘112 Patent discloses novel methods and systems for video compression.

94. The ‘112 Patent discloses novel technologies for video compression that perform predictive coding on a macroblock of a video frame such that a set of pixels of the macroblock is coded using some of the pixels from the same video frame as reference pixels and the rest of the macroblock is coded using reference pixels from at least one other video frame.

95. The ‘112 Patent discloses a system for video compression comprising an intra-frame coding unit configured to perform predictive coding on a set of pixels of a macroblock of

pixels using a first group of reference pixels, the macroblock of pixels and the first group of reference pixels being from a video frame.

96. The ‘112 Patent discloses a system for video compression comprising an inter-frame coding unit configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels, the second group of reference pixels being from at least one other video frame.

97. The ‘112 Patent and its underlying patent application have been cited by 10 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘112 Patent and its underlying patent application as relevant prior art:

- British Broadcasting Corporation
- Google LLC
- Megachips Corp.
- Olympus Corp.
- Samsung Electronics Co., Ltd.
- Sony Corporation
- Toshiba Corporation

U.S. PATENT NO. 6,646,688

98. U.S. Patent No. 6,646,688 entitled, *High Quality Video and Graphics Pipeline*, was filed on November 10, 2000. The ‘688 Patent is subject to a 35 U.S.C. § 154(b) term extension of 407 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘688 Patent. A true and correct copy of the ‘688 Patent is attached hereto as Exhibit 11.

99. The ‘688 Patent discloses multiple embodiments for optimally processing high quality video and graphics.

100. The ‘688 Patent discloses a video/graphics data processing method wherein a stream of digital video/graphics data is pre-processed to output pre-processed data.

101. The ‘688 Patent further discloses substituting the color key with a pre-selected color in the processing of a color key from the pre-processed data to output resulting data.

102. The ‘688 Patent discloses processing and transforming the data resulting from the processing a color key from the pre-processed data to output resulting data.

103. The ‘688 Patent has been cited by multiple United States patents and patent applications as relevant prior art. Specifically, patents and patent applications issued to Broadcom Corporation, Eastman Kodak Company, Nvidia Corporation, and Quantel Ltd. cited the ‘688 Patent family as relevant prior art.

U.S. PATENT NO. 7,894,529

104. U.S. Patent No. 7,894,529 entitled, *Method And Device For Determining Motion Vectors*, was filed on June 1, 2006, and claims priority to June 3, 2005. The ‘529 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,301 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘529 Patent. A true and correct copy of the ‘529 Patent is attached hereto as Exhibit 12.

105. The ‘529 Patent discloses novel methods and apparatuses for determining motion vectors that are each assigned to individual image regions.

106. The inventions disclosed in the ‘529 Patent enable an increase in the resolution of video and image signals during the motion estimation process.

107. The ‘529 Patent discloses a method for determining motion vectors which are assigned to individual image regions of an image.

108. The ‘529 Patent discloses a method wherein an image is subdivided into a number of image blocks, and a motion estimation technique is implemented to assign at least one motion

vector to each of the image blocks where a modified motion vector is generated for at least a first image block.

109. The ‘529 Patent discloses a method that determines at least a second image block through which the motion vector assigned to the first image block at least partially passes.

110. The ‘529 Patent discloses a method that generates the modified motion vector as a function of a motion vector assigned to at least the second image block.

111. The ‘529 Patent discloses a method that assigns the modified motion vector as the motion vector to the first image block.

112. The ‘529 Patent and its underlying patent application have been cited by multiple patents and patent applications as relevant prior art. Specifically, patents issued to Fujifilm Corp., and Samsung Electronics Co., Ltd. have cited the ‘529 Patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,542,041

113. U.S. Patent No. 7,542,041 entitled, *Runtime Configurable Virtual Video Pipeline*, was filed on April 2, 2004, and claims priority to April 3, 2003. The ‘041 patent is subject to a 35 U.S.C. § 154(b) term extension of 288 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘041 Patent. A true and correct copy of the ‘041 Patent is attached hereto as Exhibit 13.

114. The ‘041 Patent discloses novel systems for dynamically configuring a multi-pipe pipeline system.

115. The inventions disclosed in the ‘041 Patent enable a multiple-pipeline system that is dynamically configurable to effect various combinations of functions for each pipeline.

116. The inventions disclosed in the ‘041 Patent teach a multiple pipeline system that includes a pool of auxiliary function blocks that are provided as required to select pipelines.

117. In one embodiment of the ‘041 Patent, each pipeline of the multiple-pipeline system is configured to include a homogenous set of core functions. A pool of auxiliary functions is provided for selective insertion of auxiliary functions between core functions of select pipelines.

118. In one embodiment of the ‘041 Patent, each auxiliary function includes a multiplexer that allows it to be selectively coupled within each pipeline.

119. The ‘041 Patent discloses, in one embodiment, a processing system that includes a plurality of pipelines, with each pipeline of the plurality including a plurality of core pipeline elements that are configured to sequentially process data as it traverses the pipeline.

120. The ‘041 Patent discloses, in one embodiment, a processing system that includes a plurality of auxiliary elements, each auxiliary element of the plurality of auxiliary elements being configured to be selectively coupled to multiple pipelines of the plurality of pipelines.

121. The ‘041 Patent discloses, in one embodiment, a processing system wherein the auxiliary elements are responsive to external coupling-select signals.

122. The ‘041 Patent discloses, in one embodiment, a processing system wherein a plurality of auxiliary elements are within a selected pipeline of the multiple pipelines, between a pair of core pipeline elements of the plurality of core pipeline elements to process the data as it traverses between the pair of core elements.

123. The ‘041 Patent has been cited by several United States patents and patent applications as relevant prior art. Specifically, patents and patent applications issued to Microsoft Corporation, Xilinx Inc., Canon Inc., Intel Corporation, and Nokia Oyj have cited the ‘041 Patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,571,450

124. U.S. Patent No. 7,571,450 entitled, *System For And Method Of Displaying Information*, was filed on February 12, 2003, and claims priority to March 11, 2002. The '450 Patent is subject to a 35 U.S.C. § 154(b) term extension of 846 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '450 Patent. A true and correct copy of the '450 Patent is attached hereto as Exhibit 14.

125. The '450 Patent discloses novel methods and systems for displaying information. The inventions disclosed in the '450 Patent enable methods and systems wherein a user does not need to make a new selection after being switched from one service to a second service.

126. The inventions disclosed in the '450 Patent permit a user of an information display system to have selections made on a first service also presented when the user switches to a second service without requiring the user to browse through the menus to define the type of information to be displayed a second time.

127. In one embodiment of the '450 Patent, the user selection being made on the basis of the provided options while the first service was selected is use to select the appropriate data elements of the stream of the second service.

128. The inventions disclosed in the '450 Patent enable various content sources to share similar information models.

129. The '450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein receiving a transport stream comprises services, with the services having elementary streams of video and of data elements.

130. The '450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein user actions of making a user selection of a type of information to be displayed on the device are received.

131. The ‘450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein filtering to select a data element of a first one of the services on the basis of the user selection is performed.

132. The ‘450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein rendering to calculate an output image to be displayed on the display device, on the basis of the first data element selected by the filer is performed.

133. The ‘450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein switching from the first one of the services to a second one of the services, characterized in comprising a second step of filtering to select a second data-element of the second one of the services, on the basis of the user selection is performed.

134. The ‘450 Patent, in one embodiment, discloses a method of displaying information on a display device wherein being switched from the first one of the services to the second one of the services, with the data-element and the second data-element being mutually semantically related and a second step of rendering to calculate the output image to be displayed on the display device, on the basis of the second data-element selected by the filter is performed.

135. The ‘450 Patent and its underlying patent application have been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to AT&T Intellectual Property I LP, Nokia Oyj, Samsung Electronics Co., Ltd., and ZTE Corporation have all cited the ‘450 Patent and its underlying patent application as relevant prior art.

U.S. PATENT NO. 7,750,979

136. U.S. Patent No. 7,750,979 entitled, *Pixel-Data Line Buffer Approach Having Variable Sampling Patterns*, was filed on October 26, 2001. The ‘979 Patent is subject to a 35 U.S.C. § 154(b) term extension of 2,749 days. Dynamic Data is the owner by assignment of all

right, title, and interest in the '979 Patent. A true and correct copy of the '979 Patent is attached hereto as Exhibit 15.

137. The '979 Patent discloses novel methods and systems for motion compensation in video signal processing.

138. The '979 Patent discloses methods and systems that use line buffers that are decoupled and that can deliver a fixed number of pixels, as may be required by a video processing stage, using a sampling pattern that is defined as one among several selectable sampling windows.

139. The '979 Patent discloses a video processing circuit having an input stream of pixels corresponding to an array of video pixels.

140. The '979 Patent further discloses having a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array.

141. The '979 Patent further discloses having a video processing stage that inputs pixels using a fixed number of pixels.

142. The '979 Patent further discloses a method for delivering the input stream of pixels to the video processing stage.

143. The '979 Patent further discloses a method comprising establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels.

144. The '979 Patent further discloses a method comprising storing pixels from the input stream into a first set of line butters, the pixels stored in the first set of line butters including pixels for the established window size.

145. The ‘979 Patent further discloses a method comprising prefetching the stored pixels from the first set of line butters into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size.

146. The ‘979 Patent further discloses a method comprising fetching the fixed number of pixels from the second set of line buffers for the video processing stage.

U.S. PATENT NO. 7,058,227

147. U.S. Patent No. 7,058,227 entitled, *Problem Area Location In An Image Signal*, was filed on July 17, 2002, and claims priority to August 21, 1998. The ’227 Patent is subject to a 35 U.S.C. § 154(b) term extension of 723 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ’227 Patent. A true and correct copy of the ’227 Patent is attached hereto as Exhibit 16.

148. The ’227 Patent discloses novel methods and systems for detecting occlusion and reducing halo effects in motion compensated pictures.

149. The ’227 Patent further discloses a method and device for interpolating images between existing images.

150. The ’227 Patent discloses technologies capable of adapting the interpolation strategy depending on a segmentation of the image in various areas.

151. The ’227 Patent discloses a method of locating problem areas in an image signal that includes estimating a motion vector field for the image signal.

152. The ’227 Patent discloses a method of locating problem areas in an image signal that includes detecting edges in the motion vectors field.

153. The ’227 Patent discloses a method of locating problem areas in an image signal that includes comparing edge locations in successive field periods to identify both foreground and background.

154. The ’227 Patent and its underlying patent application have been cited by 43 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ’227 Patent and its underlying patent application as relevant prior art:

- Integrated Device Technology, Inc.
- Qualcomm Inc.
- MediaTek Inc.
- Mitsubishi Denki Kabushiki Kaisha
- Panasonic Corporation
- Samsung Electronics Co., Ltd.
- Sony Corporation

U.S. PATENT NO. 6,421,090

155. U.S. Patent No. 6,421,090 entitled, *Motion And Edge Adaptive Deinterlacing*, was filed on August 27, 1999. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘090 Patent. A true and correct copy of the ‘090 Patent is attached hereto as Exhibit 17.

156. The ‘090 Patent discloses novel methods and apparatuses for interpolating a pixel during the deinterlacing of video signals. The various embodiments of the ‘090 Patent utilize multiple, interlaced scan lines of video signal, with each scan line including a series of pixels with intensity values.

157. The ‘090 Patent discloses generating a motion value representative of the motion between successive frames about the pixel by segmenting an image into multi-pixel segments and comparing the differences with respect to each segment in successive frames.

158. The ‘090 Patent discloses detecting an edge direction about the pixel and performing an edge adaptive interpolation at the pixel using a generated motion value.

159. The ‘090 Patent further discloses generating a motion value by comparing segments of pixels about the pixel from at least three successive frames.

160. The ‘090 Patent and its underlying patent application have been cited by 86 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘090 Patent and its underlying patent application as relevant prior art:

- Samsung Electronics Co., Ltd.
- LG Electronics Inc.
- Qualcomm Inc.
- Microsoft Corporation
- Panasonic Corporation
- STMicroelectronics SRL
- Matsushita Electric Industrial Company Ltd.
- Sanyo Electric Company Ltd.
- Fujitsu Limited
- AVerMedia Technologies Inc.
- Sony Corporation
- Himax Technologies Inc.
- Mitsubishi Electric Corporation
- Hewlett-Packard Development Company L.P.
- MediaTek Inc.
- Realtek Semiconductor Corp.
- Imagination Technologies Limited
- Integrated Device Technology Incorporated
- Intel Corporation
- MStar Semiconductor Incorporated

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 8,189,105

161. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

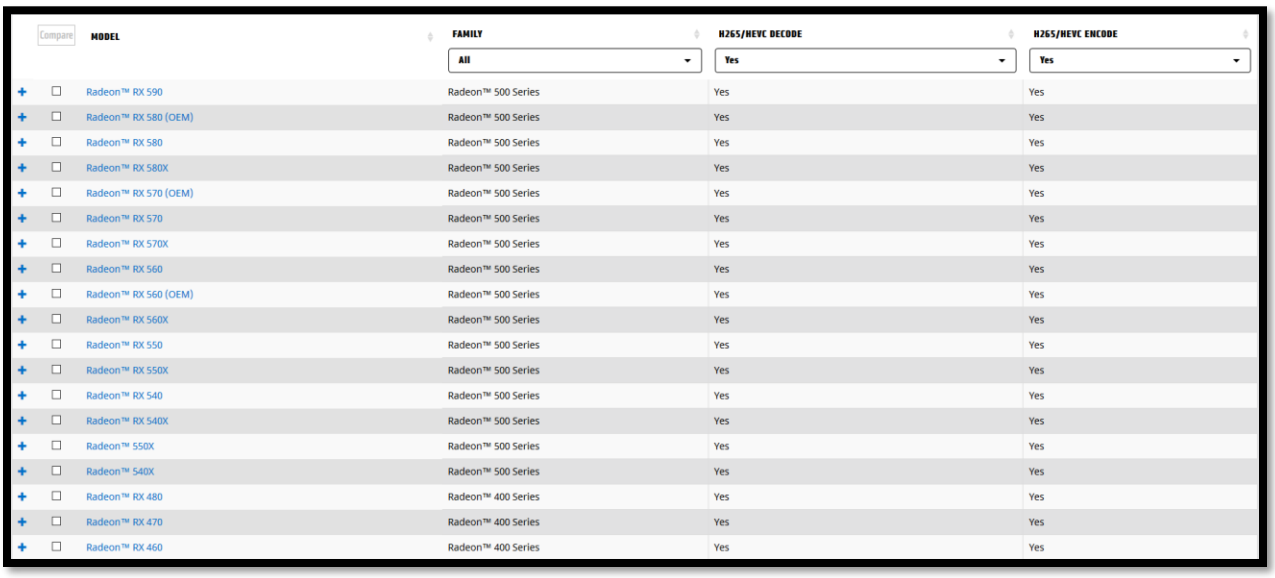
162. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion compensation in video signal processing.

163. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for processing pixel information based on received motion and edge data.

164. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") processing functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '105 Product(s)").

165. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '105 Products in regular business operations.

166. On information and belief, the AMD '105 Products perform video processing compliant with the HEVC standard.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products

perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

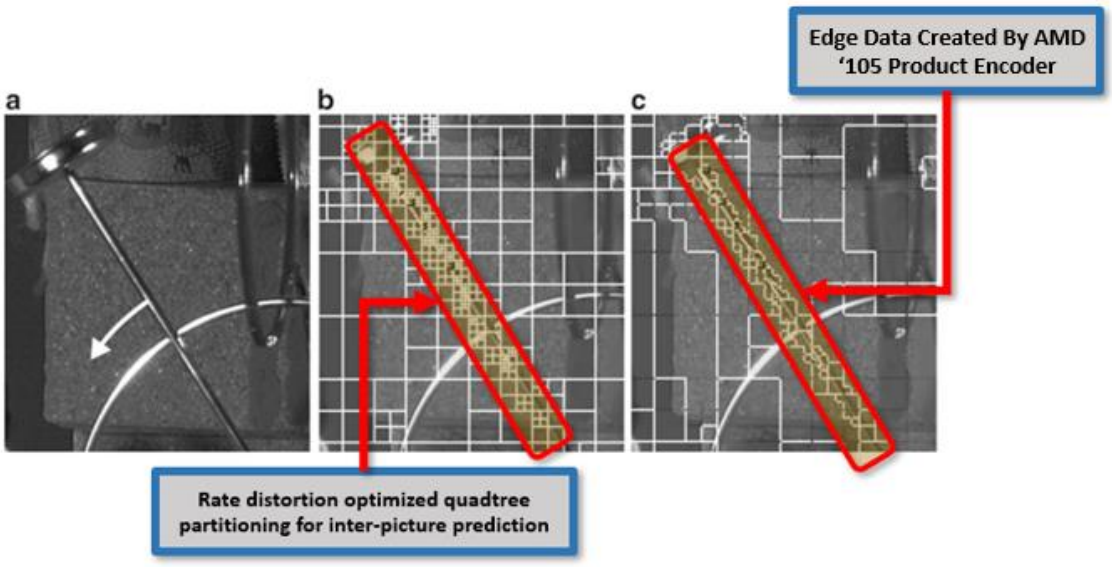
167. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '105 Products - necessarily infringe the '105 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '105 patent, including but not limited to claim 1 of the '105 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to AMD's infringement of the '105 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

168. On information and belief, the AMD '105 Products comply with the HEVC standard, which requires processing edge data from edge-adaptive interpolation processing.

169. The AMD '105 Products use two types of prediction methods for processing pixel information when encoding and decoding video data in HEVC format: inter prediction and intra prediction. Inter prediction utilizes motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra prediction uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture.

The HEVC Specification (*e.g.*, *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) sets forth the standard that is followed by HEVC compliant devices such as the AMD '105 Products, and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the AMD '105 Products perform a method for encoding a video signal comprised of pixels using motion vectors when performing encoding of H.265/HEVC video data.

170. During the encoding process the AMD '105 products process pixel information based on edge data. The edge data is generated by the AMD '105 products using merge mode estimation. Specifically, the AMD '105 Products generate merge estimation regions which identify edge information within a video frame. The merge estimation regions are comprised of prediction units ("PU") that contain luma values. For example, in the below diagram PUs are shown. The encoding process then identifies along the edges of each prediction unit a merge estimation region ("MER"). The MER regions thus identify the edges and the PU contains the intensity estimate for the pixels.



Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (annotations added).

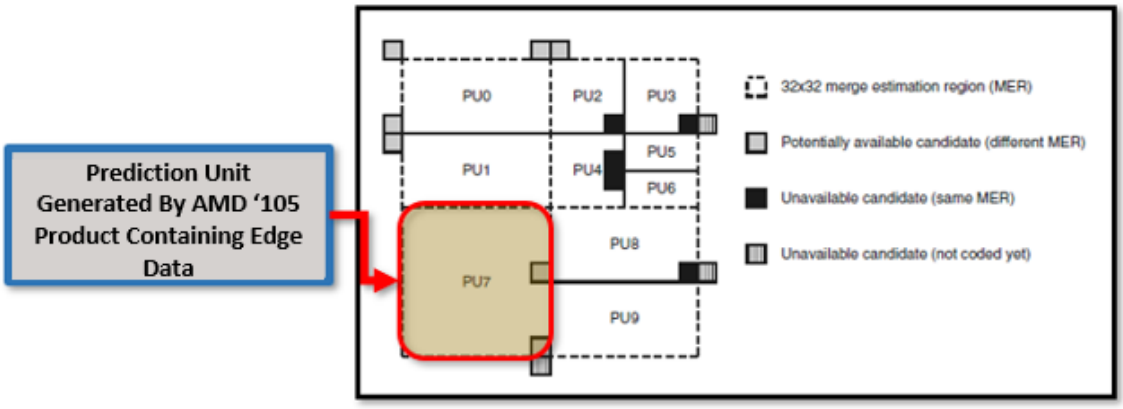
171. The AMD '105 Products in the process of encoding video content in HEVC format generate merge estimation regions generate edge data that include luma location and luma values which include a first intensity estimate. The HEVC standards describes this process as leading to the generation of luma motion vector mvL0 and mvL1.

> [T]he derivation process for luma motion vectors for merge mode as specified in clause I.8.5.3.2.7 is invoked with the luma location (xCb, yCb), the luma location (xPb, yPb), the variables nCbS, nPbW, nPbH, and the partition index partIdx as inputs, and the output being the luma motion vectors mvL0, mvL1, the reference indices refIdxL0, refIdxL1, the prediction list utilization flags predFlagL0 and predFlagL1, the flag ivMcFlag, the flag vspMcFlag, and the flag subPbMotionFlag.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.2.1 (February 2018) (emphasis added).

172. The AMD '105 Products perform the step of processing edge data from an edge adaptive interpolation process wherein the edge data includes a first intensity estimate of the pixel. Specifically, the AMD '105 Products implement HEVC encoding which utilizes Parallel Merge Mode and Merge Estimation Regions (MER's) within the interpolation process to determine pixel edges. Parallel Merge Mode Estimation identifies the edge data within a prediction unit. The

below diagram shows how video data is portioned into 10 prediction units and edge data is calculated and passed to the encoder.



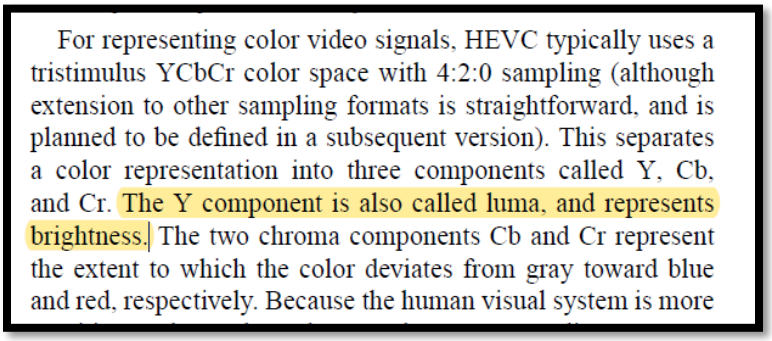
Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 127 (September 2014) (annotations added).

173. The merge estimation processes implemented by the AMD '105 Products is "adaptive." The below excerpt from documentation regarding the HEVC encoding process describes that the "merge estimation level is adaptive."

> In order to enable an encoder to trade-off parallelism and coding efficiency, the parallel merge estimation level is adaptive and signaled as `log2_parallel_merge_level_minus2` in the picture parameter set. The following MER sizes are allowed: 4×4 (no parallel merge estimation possible), 8×8, 16×16, 32×32 and 64×64. A higher degree of parallelization, enabled by a larger MER, excludes more potential candidates from the merge candidate list.

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 128 (September 2014) (emphasis added).

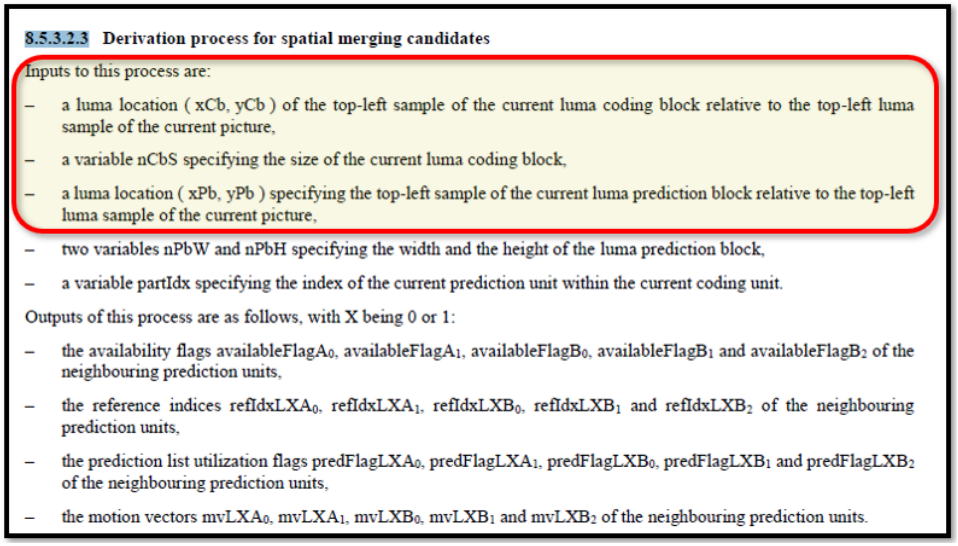
174. The edge data that is processed from the edge adaptive interpolation process includes intensity estimates for pixels such as pixels in the merge estimation region. The intensity estimate or brightness estimate is referred to as "luma" in the encoding functionality implemented by the AMD '105 Products.



For representing color video signals, HEVC typically uses a tristimulus YCbCr color space with 4:2:0 sampling (although extension to other sampling formats is straightforward, and is planned to be defined in a subsequent version). This separates a color representation into three components called Y, Cb, and Cr. The Y component is also called luma, and represents brightness. The two chroma components Cb and Cr represent the extent to which the color deviates from gray toward blue and red, respectively. Because the human visual system is more

Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1654 (December 2012) (emphasis added).

175. The motion estimation region ("MER") is an adaptive interpolation process in which the edges of images are calculated and include the intensity estimates of pixels by way of a luma value. The below excerpt from the HEVC specification describes how during the generation of merge estimation regions edge data includes luminosity values (intensity estimates) for pixels within a region.



8.5.3.2.3 Derivation process for spatial merging candidates

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

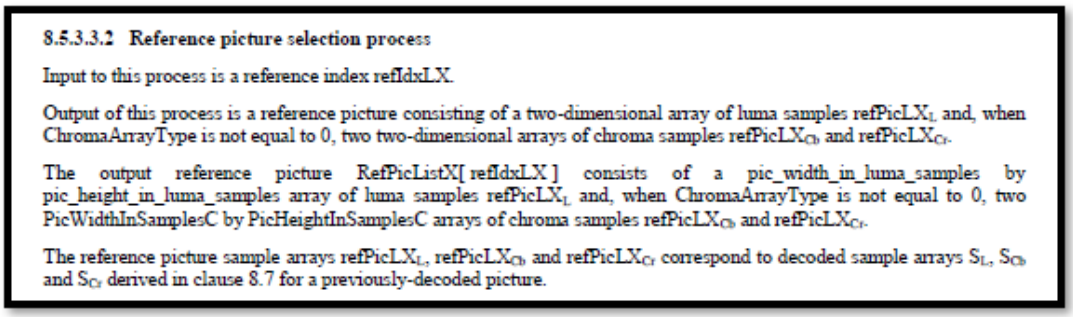
Outputs of this process are as follows, with X being 0 or 1:

- the availability flags availableFlagA$_0$, availableFlagA$_1$, availableFlagB$_0$, availableFlagB$_1$ and availableFlagB$_2$ of the neighbouring prediction units,
- the reference indices refIdxLXA$_0$, refIdxLXA$_1$, refIdxLXB$_0$, refIdxLXB$_1$ and refIdxLXB$_2$ of the neighbouring prediction units,
- the prediction list utilization flags predFlagLXA$_0$, predFlagLXA$_1$, predFlagLXB$_0$, predFlagLXB$_1$ and predFlagLXB$_2$ of the neighbouring prediction units,
- the motion vectors mvLXA$_0$, mvLXA$_1$, mvLXB$_0$, mvLXB$_1$ and mvLXB$_2$ of the neighbouring prediction units.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § I.8.5.2.3 (February 2018) (attached hereto as Exhibit 8) (emphasis added).

176. The AMD '105 Products process motion data associated with motion compensation. The motion data processed by the AMD '105 Products include a first estimated

motion vector of pixels within a reference frame prior to the current frame and a second estimated motion vector within the reference field after the current field. Specifically, the AMD '105 products generate motion data in the form of a bi-directional prediction unit (PU) which has two motion vectors (referencing a prior frame and a subsequent frame in the sequence). The two motion vectors are combined to make a "bi-predictive merge candidate." One of the motion vectors is obtained from "reference picture list0" and the other motion vector is obtained from "reference picture list1."



8.5.3.3.2 Reference picture selection process

Input to this process is a reference index refIdxLX.

Output of this process is a reference picture consisting of a two-dimensional array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two two-dimensional arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The output reference picture RefPicListX[refIdxLX] consists of a pic_width_in_luma_samples by pic_height_in_luma_samples array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two PicWidthInSamplesC by PicHeightInSamplesC arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The reference picture sample arrays $refPicLX_L$, $refPicLX_{Cb}$ and $refPicLX_{Cr}$ correspond to decoded sample arrays S_L, S_{Cb} and S_{Cr} derived in clause 8.7 for a previously-decoded picture.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.3 (February 2018).

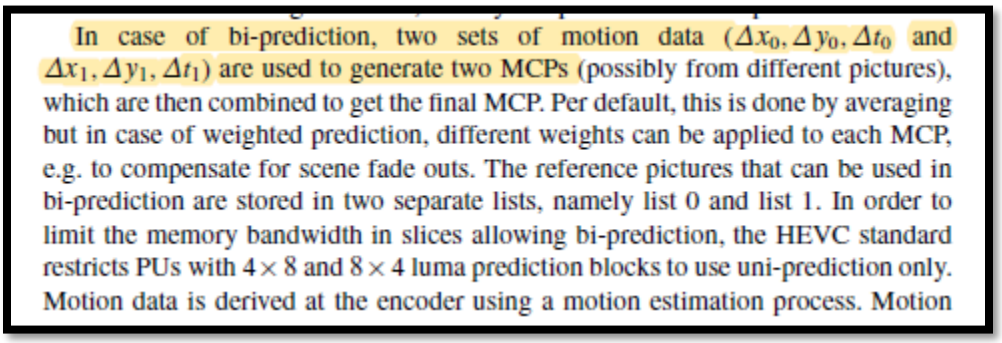
177. The reference pictures that are used to generate a motion vector comprise both the forward and prior reference pictures which are referred to in the HEVC encoding process implemented by the AMD '105 Products as "refPicLXcb" and "refPicLXcr." The following excerpt describing the implementation of the encoding process in the AMD '105 Products which use bi-predictive slices.

> Since a merge candidate comprises all motion data and the TMVP is only one motion vector, the derivation of the whole motion data only depends on the slice type. For bi-predictive slices, a TMVP is derived for each reference picture list. Depending on the availability of the TMVP for each list, the prediction type is set to bi-prediction or to the list for which the TMVP is available. All associated reference picture indices are set equal to zero. Consequently for uni-predictive slices, only the TMVP for list 0 is derived together with the reference picture index equal to zero.

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added) (describing the use of bi-prediction in which

motion data is derived from the forward and prior reference pictures in generating temporal arrays/vectors).

178. The AMD '105 Products interpolation process contains bi-prediction functionality that computes a first estimated motion prediction and a second estimated motion prediction. The below excerpt from documentation of the encoding method used by the AMD '105 products describes that the encoding process includes functionality for generating a second intensity estimate for the pixel data and the edge data determined according to motion. In bi-prediction, the second estimate is defined as Δx_1, Δy_1, Δt_1.



In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (emphasis added).

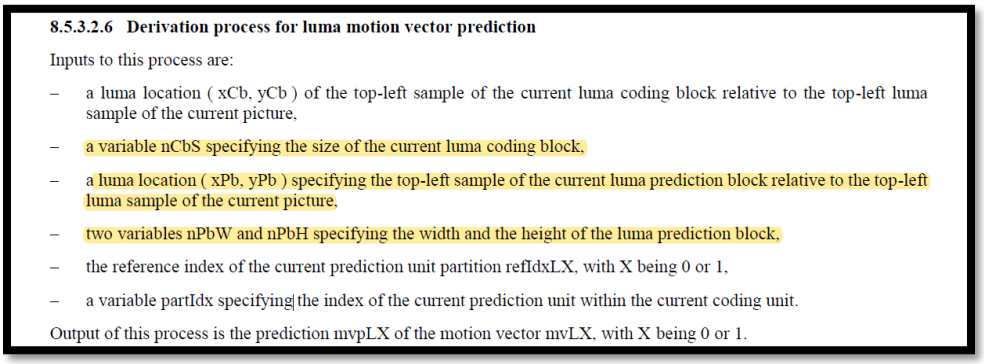
179. In AMVP the system generates a temporal intermediate candidate based on bi-directional motion data. The "inter_pred_idc [x0] [y0] specifies whether list0, list1, or bi-prediction is used for the current prediction unit" according to the below referenced table. "The array indices x0, y0 specify the location (x0, y0) of the top-left luma sample of the considered prediction block relative to the top-left luma sample of the picture."

Table 7-11 – Name association to inter prediction mode

inter_pred_idc	Name of inter_pred_idc	
	(nPbW + nPbH) != 12	(nPbW + nPbH) == 12
0	PRED_L0	PRED_L0
1	PRED_L1	PRED_L1
2	PRED_BI	na

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.9.6 (February 2018).

180. The AMD '105 products generate a second intensity estimate based on the edge data and the motion data. The edge data is combined with the temporal intermediate candidate to generate the temporal candidate. The prediction unit based on the first and second motion vector (motion data) is then combined with the edge data to generate a second intensity estimate. Once the reference picture for obtaining the co-located PU is selected then the position of the co-located Pu will be selected among two candidate positions. A second intensity estimate is generated by using the bi-directional motion vectors and the edge data. The below excerpt from the HEVC specification describes that for a luma motion vector prediction the generation of a second intensity estimate is based on the motion data and the edge data. The edge data here is comprised by the luma location and luma prediction block information. Further, the luma motion vectors mvLO and mvL1 are combined with the edge data including luma location xCB yCB xBL and yBl to generate a second intensity estimate.



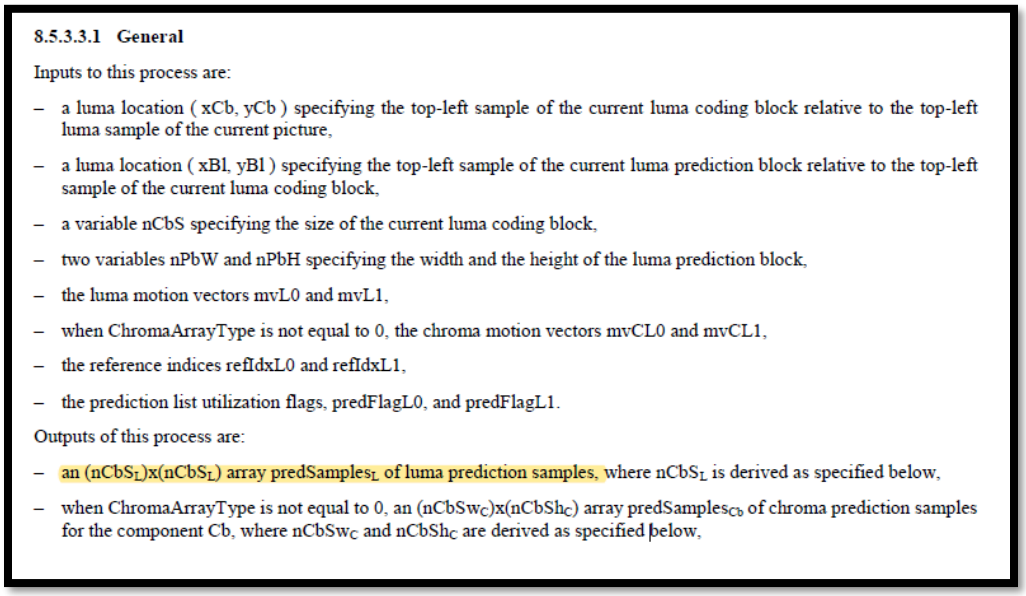
8.5.3.2.6 Derivation process for luma motion vector prediction

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the reference index of the current prediction unit partition refIdxLX, with X being 0 or 1,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

Output of this process is the prediction mvpLX of the motion vector mvLX, with X being 0 or 1.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.2.6 (February 2018) (emphasis added).



8.5.3.3.1 General

Inputs to this process are:

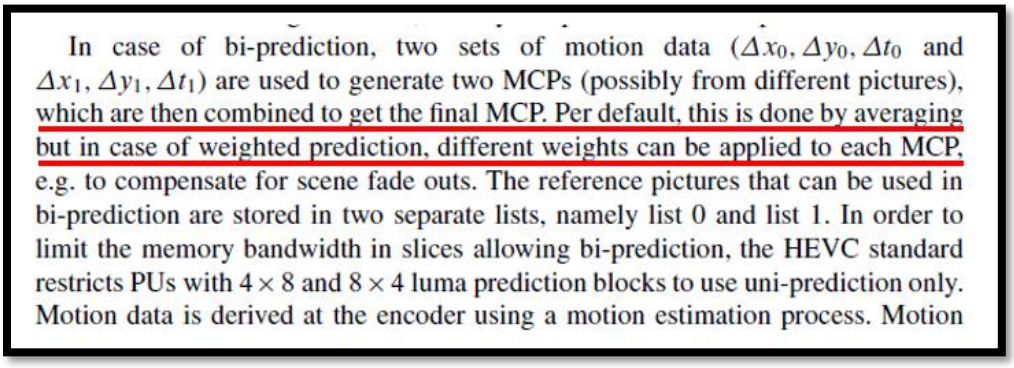
- a luma location (xCb, yCb) specifying the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a luma location (xBl, yBl) specifying the top-left sample of the current luma prediction block relative to the top-left sample of the current luma coding block,
- a variable nCbS specifying the size of the current luma coding block,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the luma motion vectors mvL0 and mvL1,
- when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1,
- the reference indices refIdxL0 and refIdxL1,
- the prediction list utilization flags, predFlagL0, and predFlagL1.

Outputs of this process are:

- an $(nCbS_L)x(nCbS_L)$ array $predSamples_L$ of luma prediction samples, where $nCbS_L$ is derived as specified below,
- when ChromaArrayType is not equal to 0, an $(nCbSw_C)x(nCbSh_C)$ array $predSamples_{Cb}$ of chroma prediction samples for the component Cb, where $nCbSw_C$ and $nCbSh_C$ are derived as specified below,

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.1 (February 2018) (emphasis added).

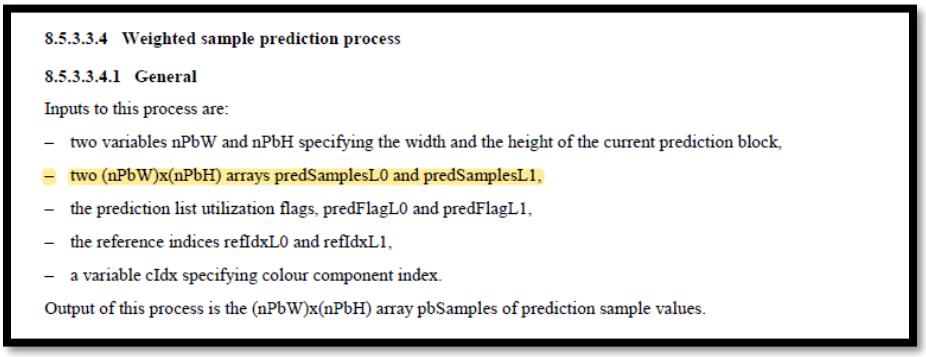
181. The AMD '215 Products perform a mixing process in which the final edge/motion data of a pixel is calculated based on a first intensity estimate, second intensity estimate, and motion reliability data. Specifically, the AMD '215 Products encode pixel data using bi-prediction wherein use two types of mixing functions: average mixing and weighted mixing.



In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added).

182. The HEVC standard includes functionality to perform a mixing process. In MERGE mode, an up-to five-entry MERGE candidate list is first constructed with four (MV, Refldx) pairs from spatial neighbor blocks and one (MV, Refldx) pair from temporal bottom-right or collocated neighbor block, where Refldx is the index of the reference picture that the MV pointed to. After that, the encoder decides to use which candidate (MV, Refldx) pair to encode current block and then encode the candidate index into bitstream. In MERGE mode, the selected (MV, Refldx) pair is directly used to encode current block, and no MVD information needs to be coded. The number of merge candidates could be configured at encoder, with up to five merge candidates."



8.5.3.3.4 Weighted sample prediction process

8.5.3.3.4.1 General

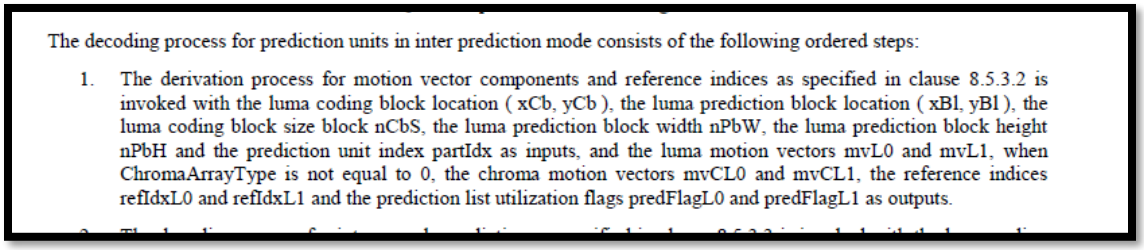
Inputs to this process are:

- two variables nPbW and nPbH specifying the width and the height of the current prediction block,
- two (nPbW)x(nPbH) arrays predSamplesL0 and predSamplesL1,
- the prediction list utilization flags, predFlagL0 and predFlagL1,
- the reference indices refIdxL0 and refIdxL1,
- a variable cIdx specifying colour component index.

Output of this process is the (nPbW)x(nPbH) array pbSamples of prediction sample values.

HIGH EFFICIENCY VIDEO CODING, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.4.1 (February 2018) (emphasis added).

183. The variables predFlagL0 and predFlagL1 are reliability values that are generated by the decoding process. The predFlagL0 and L1 values are prediction utilization values that are used to generate prediction utilization and reliability of the vectors.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

184. On information and belief, any implementation of the HEVC standard would infringe the '105 patent as every possible implementation of the standard requires: processing edge data from edge-adaptive interpolation processing, including a first intensity estimate for the pixel as well as data pertaining to one or more pixels that neighbor the pixel; processing motion data associated with motion compensation processing, wherein the motion data includes a first estimated motion vector for a pixel in a reference field prior to the present field and a second estimated motion vector for a pixel in a reference field subsequent to the present field; determining a second intensity estimate for the pixel as a function of the edge data and the motion data; and performing a blending process wherein final edge/motion data of the pixel is calculated as a function of the first intensity estimate, the second intensity estimate, and motion reliability data characterizing reliability of the motion data.

185. On information and belief, the AMD '105 Products are available to businesses and individuals throughout the United States.

186. On information and belief, the AMD '105 Products are provided to businesses and individuals located in the State of Delaware.

187. By making, using, testing, offering for sale, and/or selling products and services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the AMD '037 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '105 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

188. On information and belief, AMD also indirectly infringes the '105 patent by actively inducing infringement under 35 USC § 271(b).

189. AMD has had knowledge of the '105 patent since at least service of this First Amended Complaint or shortly thereafter, and on information and belief, AMD knew of the '105 patent and knew of its infringement, including by way of this lawsuit.

190. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '105 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '105 patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '105 patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '105 Products that have the capability of operating in a manner that infringe one or more of the claims of the '105 patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '105 Products to utilize the products in a manner that directly infringe one or more claims of the '105 patent.[21] By providing instruction and training to customers and end-users on how to use the AMD

[21] *See, e.g., AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD

'105 Products in a manner that directly infringes one or more claims of the '105 patent, including at least claim 1, AMD specifically intended to induce infringement of the '105 patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '105 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '105 patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '105 patent, knowing that such use constitutes infringement of the '105 patent.

191. The '105 patent is well-known within the industry as demonstrated by multiple citations to the '105 patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '105 patent without paying a reasonable royalty. AMD is infringing the '105 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

192. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '105 patent.

193. As a result of AMD's infringement of the '105 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

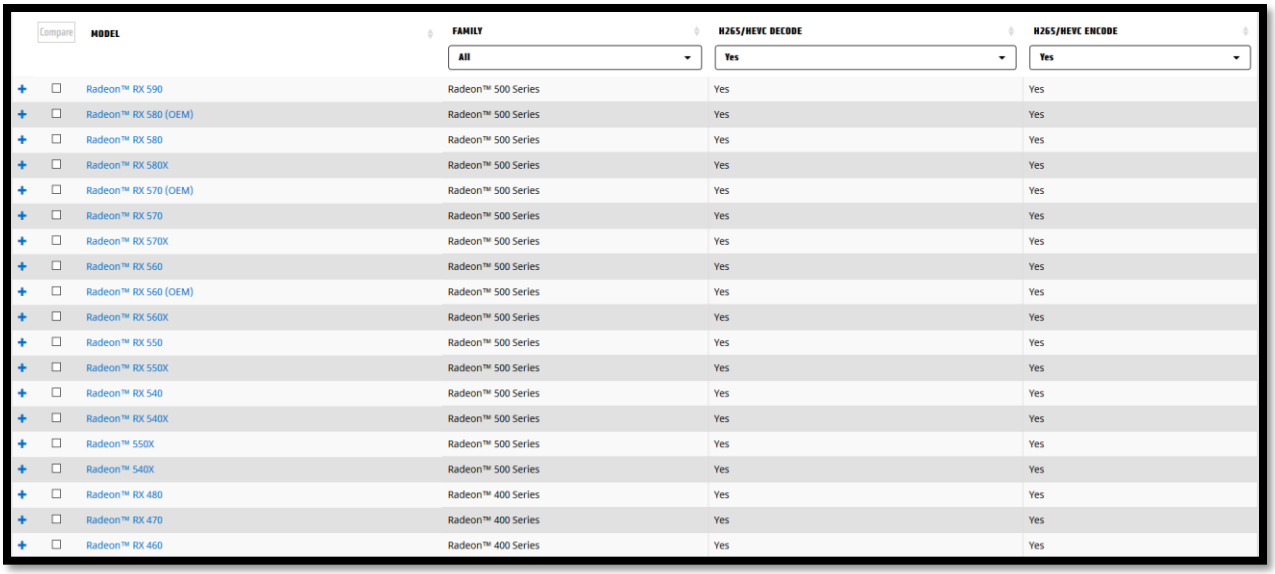
COUNT II
INFRINGEMENT OF U.S. PATENT NO. 8,135,073

194. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

195. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

196. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") decoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '073 Product(s)").

197. On information and belief, the AMD '073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the AMD '073 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by AMD '073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

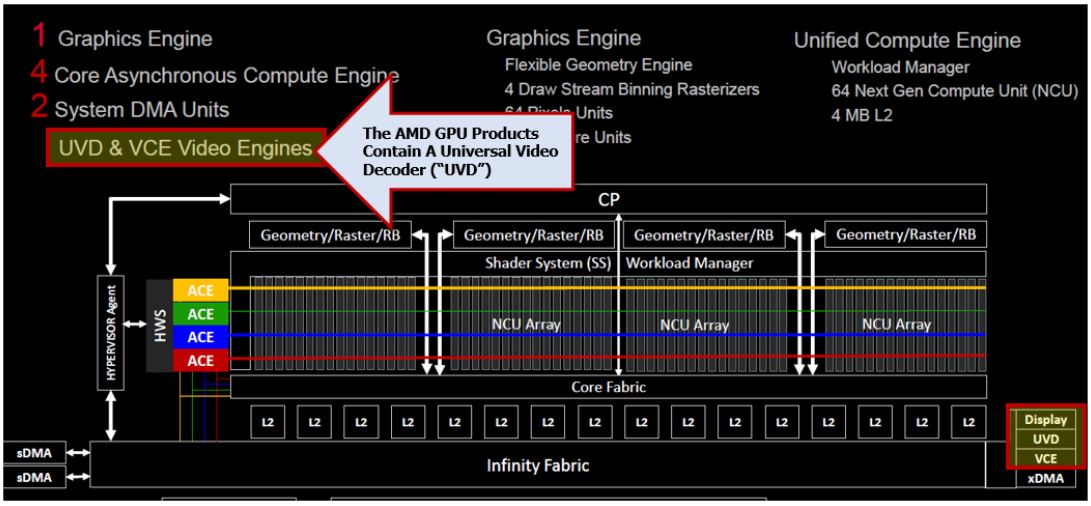
198. On information and belief, the AMD '073 Products, the AMD '073 Products comprise a video decoder for decoding video images. The following excerpt from AMD's documentation relating to the AMD '073 Products identifies the accused devices as decoding video data using a first and second frame of video data. Specifically, the AMD '073 Products contain functionality for video decoding through H.265/High Efficiency Video Coding ("HEVC") decoding.

> Vega" 10 naturally includes the latest versions of AMD's video encode and decode acceleration engines, as well. Like "Polaris," "Vega" offers hardware-based decode of HEVC/H.265 main10 profile videos at resolutions up to 3840x2160 at 60Hz, with 10-bit color for HDR content. Dedicated decoding of the H.264 format is also supported at up to 4K and 60Hz. "Vega" can also decode the VP9 format at resolutions up to 3840x2160 using a hybrid approach where the video and shader engines collaborate to offload work from the CPU. "Vega's" video encode

accelerator also supports today's most popular formats. It can encode HEVC/H.265 at 1080p240, 1440p120, and 2160p60.

Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER at 13-14 (2017) (emphasis added).

199. On information and belief, the AMD '073 Products comprise an infringing video decoder that is identified in block diagram of the below excerpts from AMD's documentation.



AMD's Radeon Next Generation GPU Architecture "Vega 10", RADEON PRESENTATION at 12 (2017) (annotations added) (showing that in the AMD Products H.265 decoder is identified as "UVD").

200. On information and belief, the AMD '073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the AMD '073 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by AMD '073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

201. The AMD Products have an input for receiving frame-based encoded video information. Specifically, the AMD Products receive frame-based encoded video information in the form of video data that is encoded in the High Efficiency Video Coding (HEVC/H.265) format set by the ITU-T Video Coding Experts Group. Documentation and analysis of the circuity of the

AMD Product further confirms the AMD Products contain multiple inputs for receiving frame-based encoded video information as shown in the following image.

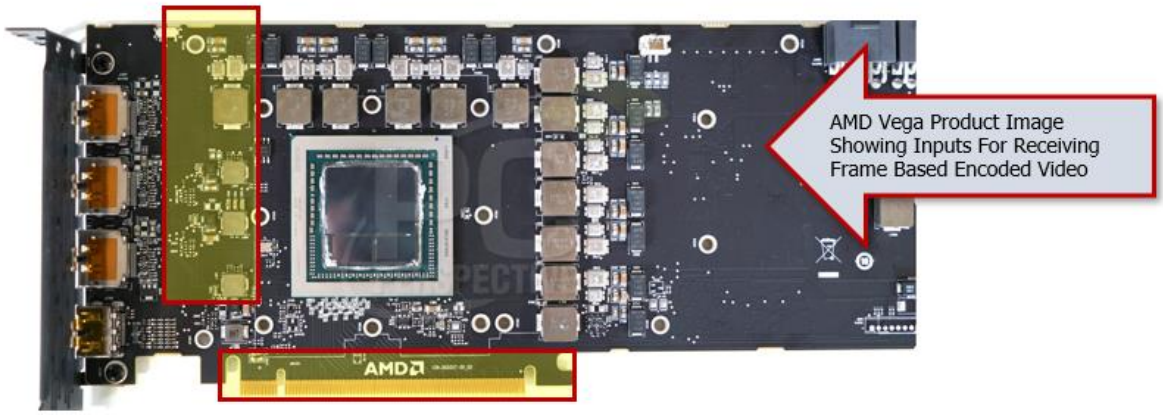
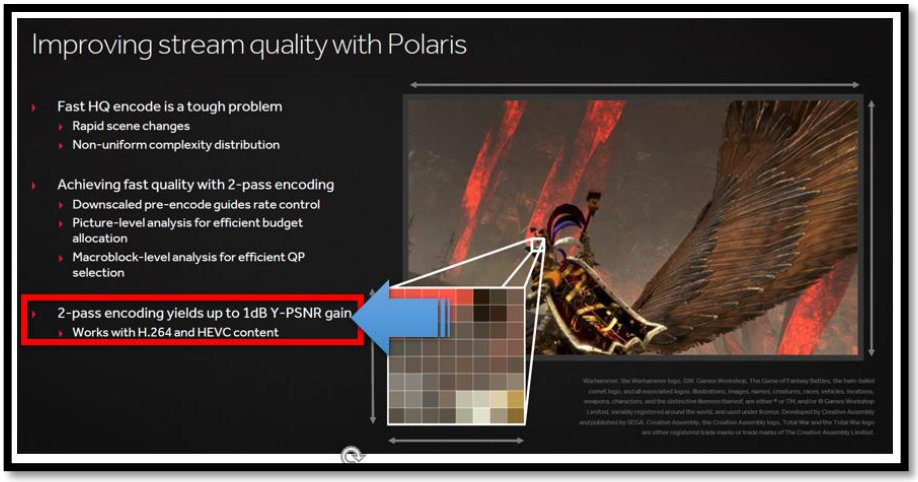


IMAGE OF AMD PRODUCT CIRCUIT BOARD: DETAILED PRODUCT ANALYSIS (2018) (annotation added) (showing inputs including: USB, Wi-Fi, and external memory).

202. On information and belief, the AMD '073 Products include inputs for receiving and decoding HEVC video data. "The Infinity Fabric logic links the graphics core to other on-chip units like the multimedia, display, and I/O blocks. I n 'Vega' 10, this fabric is clocked separately from the graphics cores a result, the GPU can maintain high clock speeds in the Infinity Fabric domain in order to facilitate fast DMA data transfers in workloads that feature little to no graphics activity, such as video transcoding." *Radeon's Next-Generation Vega Architecture*, AMD WHITEPAPER at 13 (2017).



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 36 (2016) (annotation added) (stating "2-pass encoding yields up to 1db Y-PSNR gain . . . works with H.264 and HEVC content).

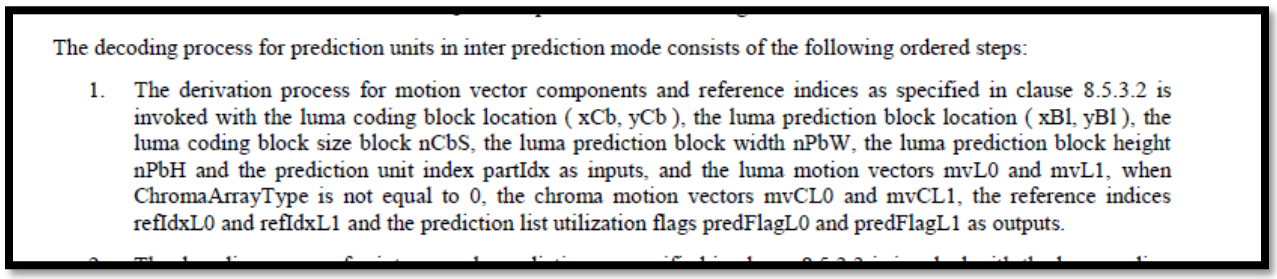
203. On information and belief, the AMD '073 Products, incorporate a decoding unit for decoding the frame of the received video data. The encoding and decoding process for video data received by the AMD '073 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

204. On information and belief, one or more of the AMD '073 Products include technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

205. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '073 Products - necessarily infringe the '073 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '073 patent, including but not limited to claim 14 of the '073 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to AMD's infringement of the '073 patent: "8.3.2 Decoding process for

reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

206. On information and belief, the AMD '073 Products comply with the HEVC standard, which requires that motion vectors are recovered from the second frame in the video stream.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

207. On information and belief, AMD has directly infringed and continues to directly infringe the '073 patent by, among other things, making, using, offering for sale, and/or selling technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the AMD '073 Products. The following excerpt explains how HEVC is a form of frame-based encoded video information.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a

> specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

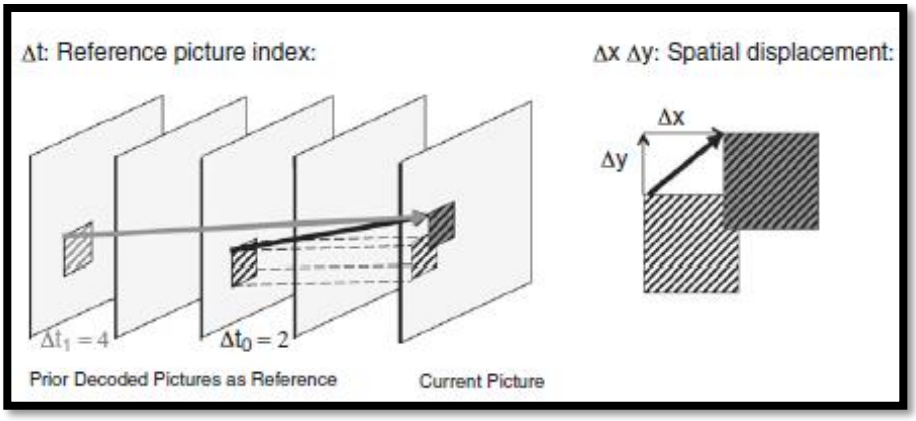
Johan Bartelmess. *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

208. On information and belief, the AMD '073 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the AMD '073 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the AMD '073 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

209. The encoded video stream received by the AMD '073 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



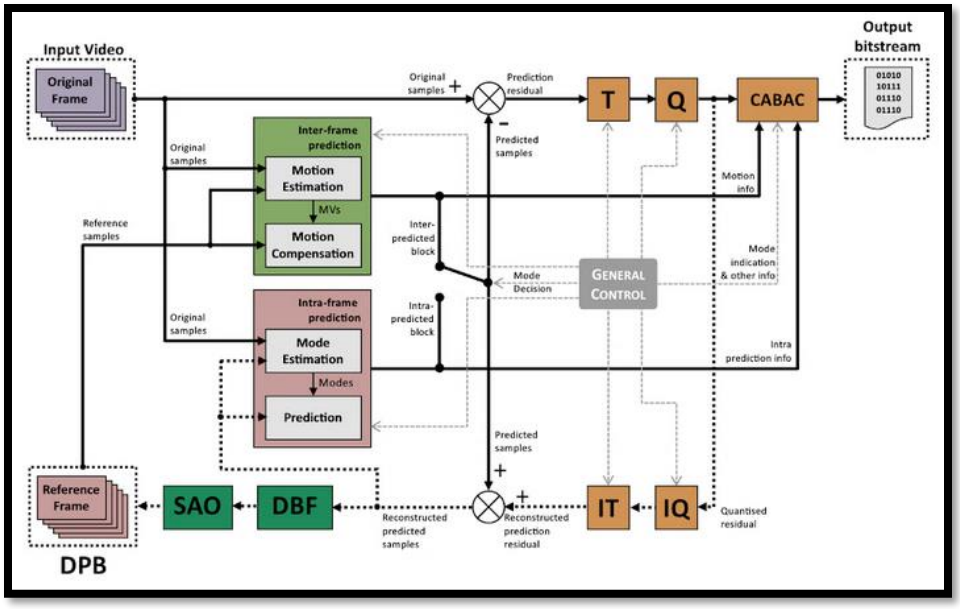
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

210. The following excerpt from an article describing the architecture of the encoded video stream received by the AMD '073 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

211. The following diagram shows how the AMD Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across a first and second frame.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

212. On information and belief, one or more of the AMD '073 Products reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

> So, this reduces guessing with frame dropping. Let's go over what we've learned. So, with HEVC hierarchical encoding, we have improved temporal scalability. There's a much more obvious frame dropping pattern and it removes frame drop guessing during playback. We also have improved motion compensation, the reference frames are much closer to each other, so we can use more parts of other frames and it also improves compression.

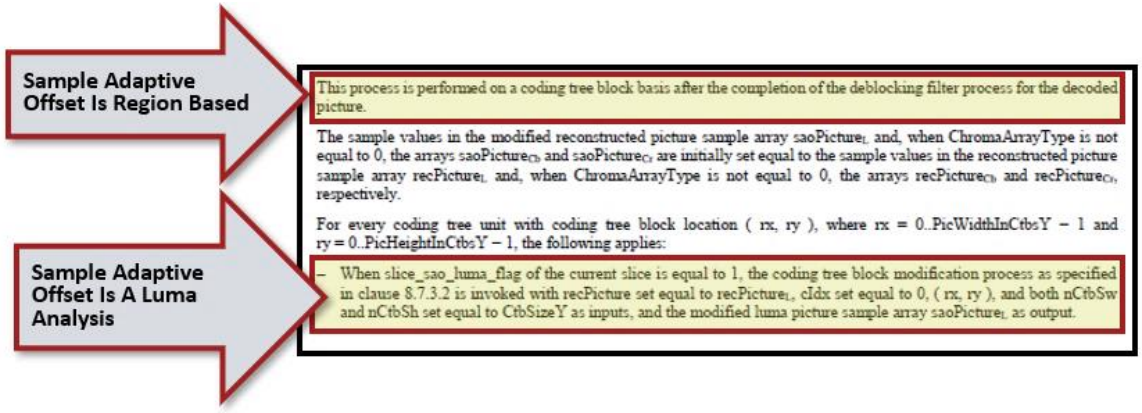
Erik Turnquist and Brad Ford, *Working with HEIF and HEVC*, AMD WORLDWIDE DEVELOPER CONFERENCE 2017: SESSION 511 Transcript (2017) (emphasis added), *available at*: https://developer.AMD.com/videos/play/wwdc2017/511.

213. On information and belief, any implementation of the HEVC standard would infringe the '073 patent as every possible implementation of the standard requires: receiving a video stream containing encoded frame based video information (including both an encoded first frame and an encoded second frame); the encoded second frame that is received depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first

frame; the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame; decoding the video stream by recovering the motion vectors in the second stream; and determining a re-mapping strategy for the video enhancement of the decoded first frame using a region-based analysis where the first frame is remapped using a remapping strategy and at least one region of the second frame is remapped depending on the re-mapping strategy for corresponding regions of the first frame.

214. On information and belief, the AMD '073 Products use of sample adaptive offset is a region-based luma analysis that is applied to the decoded first frame (reference picture). "The SAO reduces sample distortion by first classifying the samples in the region into multiple categories with as selected classifier and adding a specific offset to each sample depending on its category. The classifier index and the offsets for each region are signaled in the bitstream." Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 185 (September 2014) (emphasis added).

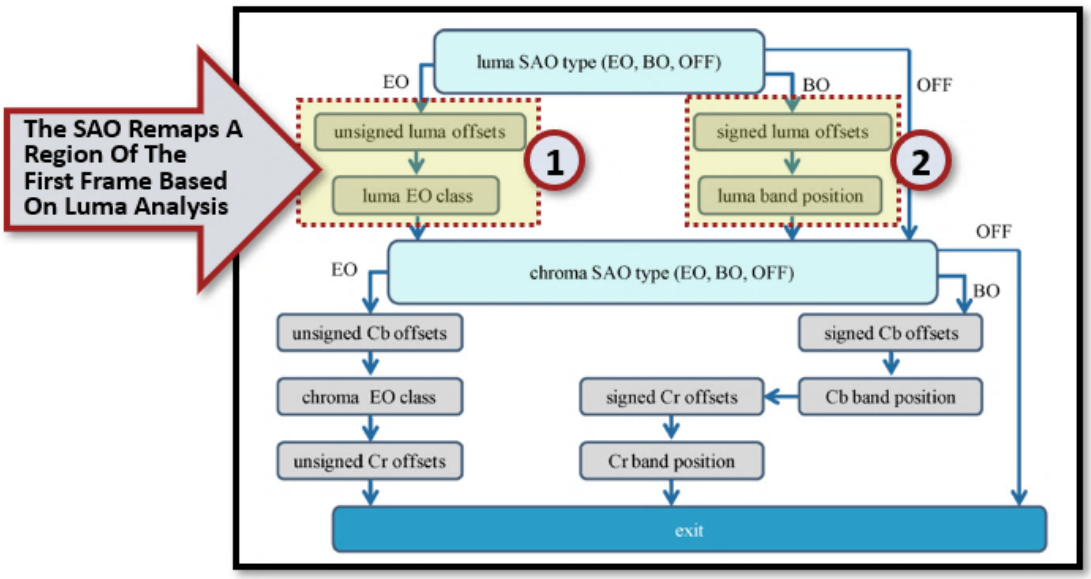
215. Further, the HEVC documentation requires that the application of a sample adaptive offset be region based (*e.g.*, applied to a coding block) ("This process is performed on a coding block basis after the completion for the deblocking filter process for the decoded picture").



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.7.3.1 (April 2015) (annotations added).

216. On information and belief, the AMD '073 Products contain functionality wherein a decoder applies sample adaptive offset to a decoded reference frame (first frame). Further, the AMD '073 Products apply the sample adaptive offset functions to remap a portion of the region based on luminance values (luma). "SAO can be applied to not only luma but also chroma." Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 at 1765 (December 2012).

217. On information and belief, the AMD '073 Products apply the sample adaptive offset to a coding tree unit (region in the first frame), a luminance analysis is performed using two luminance analysis techniques: Edge Offset ("EO") and Band Offset ("BO"). Edge Offset "uses four 1-D directional patterns for sample classification: horizontal, vertical, 135° diagonal, and 45° diagonal." Chih-Ming Fu, *et al.*, Sample Adaptive Offset in the HEVC Standard, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1757 (December 2012). Band Offset "implies one offset is added to all samples of the same band. The sample value range is equally divided into 32 bands." *Id*. at 1757. The below diagram shows that the AMD '073 Products use different sample adaptive offsets in a region of the first frame in conducting a luminance analysis.



Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1759 (December 2012) (annotations added showing (1) edge offset and (2) band offset luma analysis).

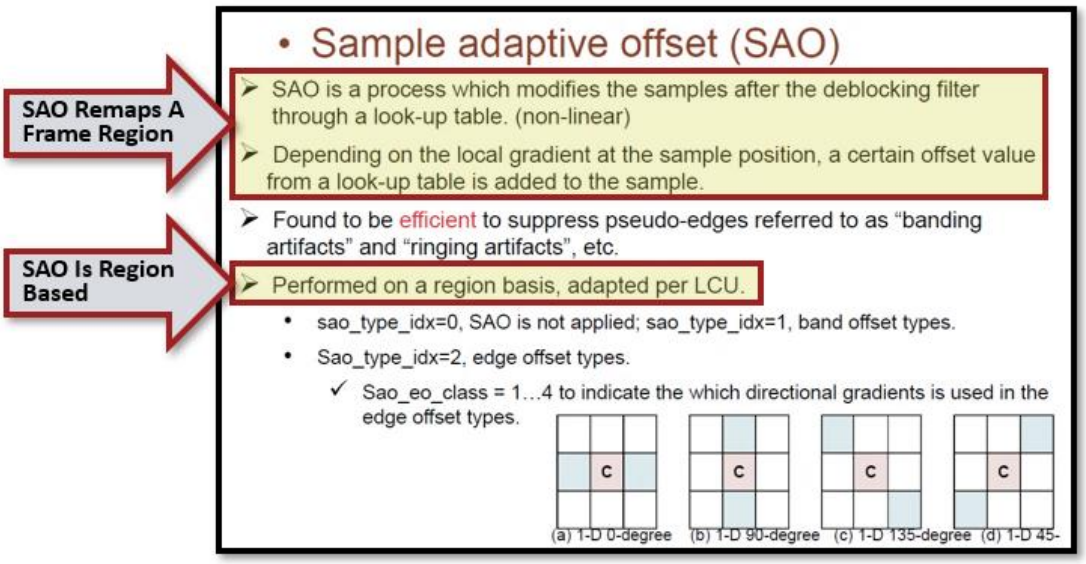
218. Further, HEVC documentation makes clear that the application of the standard adaptive offset remapping policy is based on a luminance analysis. The below shows that slices of a region have a standard adaptive offset applied based on a "luma flag."

if(sample_adaptive_offset_enabled_flag) {	
slice_sao_luma_flag	u(1)
if(ChromaArrayType != 0)	
slice_sao_chroma_flag	u(1)

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § F.7.3.6.1 (April 2015) ("sample_adaptive_offset_enabled_flag equal to 1 specifies that the sample adaptive offset process is applied to the reconstructed picture after the deblocking filter process.").

219. Commentary on the use of sample adaptive offset functionality in decoding HEVC video further confirms that the use of Sample Adaptive Offset (such as that implemented by the AMD '073 Products) is region based and remaps pixel values in a region of a frame by modifying

pixels based on an offset value. "[A]fter the deblocking filter through a look-up table . . . [and applying] a certain offset value from a look-up-table is added to the sample."[22]



Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013) (annotations added).

220. On information and belief, when the AMD '073 Products decode a second frame, the application of the remapping policy (sample adaptive offset) will be determined based on the application of sample adaptive offset to the first frame (reference picture). Thus, the application of the remapping policy (sample adaptive offset) to the first frame has the effect of increasing the quality of the reference picture such that the second frame might no longer require the application of sample adaptive offset (remapping policy).[23]

> The second in-loop filter, SAO, is applied to the output of the deblocking filter and further improves the quality of the decoded picture by attenuating ringing artifacts and changes in sample intensity of some areas of a picture. The most important advantage of the in-loop filters is improved subjective quality of reconstructed

[22] Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013).

[23] Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 171 (September 2014) ("HEVC defines two in-loop filters, deblocking and sample adaptive offset (SAO), which significantly improve the subjective quality of decoded video sequences as well as compression efficiency by increasing the quality of the reconstructed/ reference pictures.").

> pictures. In addition, using the filters in the decoding loop also increases the quality of the reference pictures and hence also the compression efficiency.

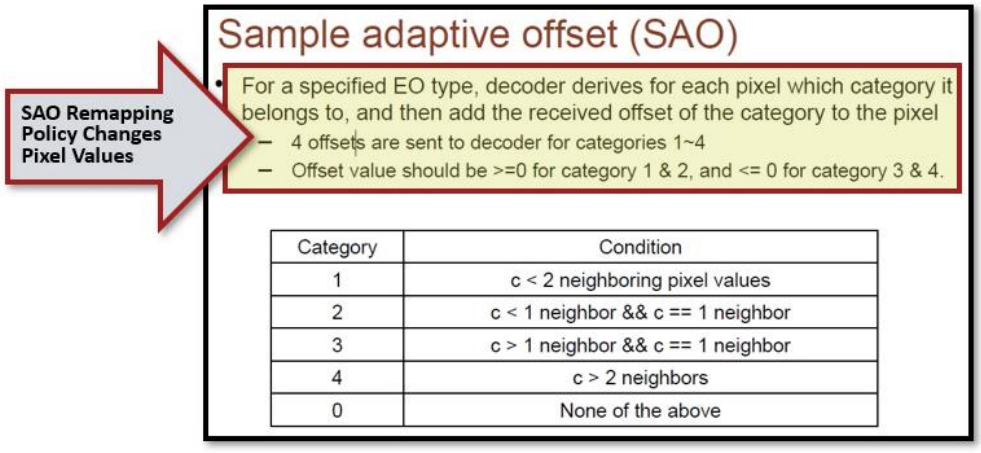
Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 171 (September 2014) (annotations added).

221. Sample adaptive offset as implemented by the AMD '073 Products is a policy that remaps the values of pixels. If sample adaptive offset is applied to a reference frame, regions in a second frame might not require the application of the remapping policy as the reference frame that was used to generate the second frame was of a better quality.

> SAO classifies each pixel into one of four bands or one of four edge types and adds an offset to it. For band offsets, the band of each pixel depends on its value and the position of the four bands. For edge offsets, the edge of each pixel depends on the whether its value is larger or smaller than two of its neighbors. The selection between band offsets and edge offsets, position of bands, choice of neighbors for edge offsets, and values of the offsets are signaled at the CTU level for luma and chroma separately.

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 335 (September 2014).

222. The following excerpt from a presentation describing HEVC decoding provides details on how the application of sample adaptive offset remaps pixel values by adding an offset to the pixel value based on a luma analysis.

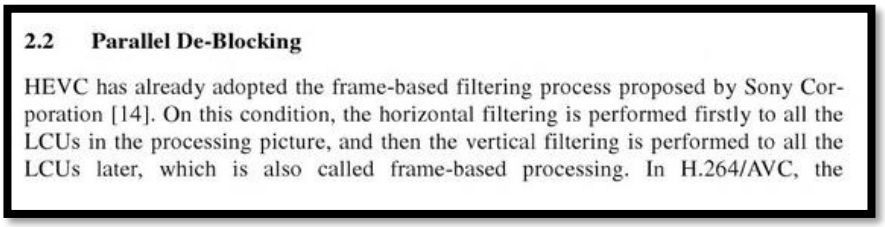


Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 44 (October 2013) (annotation added).

223. The AMD ‘073 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the AMD ‘073 Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx and Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

224. On information and belief, one or more of the AMD ‘073 Products enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

225. On information and belief, one or more of the AMD ‘073 Products include an input for receiving a video stream containing encoded frame-based video information including an encoded first frame and an encoded second frame.

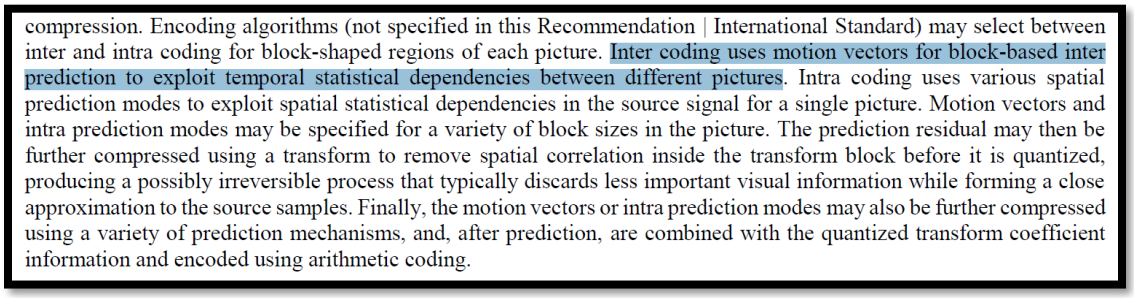


2.2 Parallel De-Blocking

HEVC has already adopted the frame-based filtering process proposed by Sony Corporation [14]. On this condition, the horizontal filtering is performed firstly to all the LCUs in the processing picture, and then the vertical filtering is performed to all the LCUs later, which is also called frame-based processing. In H.264/AVC, the

Ming-Ting Sun, *et al.*, *Advances in Multimedia Information Processing*, PCM 2012: 13TH PACIFIC-RIM CONFERENCE ON MULTIMEDIA PROCEEDINGS VOLUME 7674 at 274 (December 4-6, 2012) ("HEVC has already adopted the frame-based filtering process proposed by Sony Corporation.").

226. On information and belief, one or more of the AMD '073 Products include a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame. The Overview of Design Characteristics in the HEVC Standard describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."



compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

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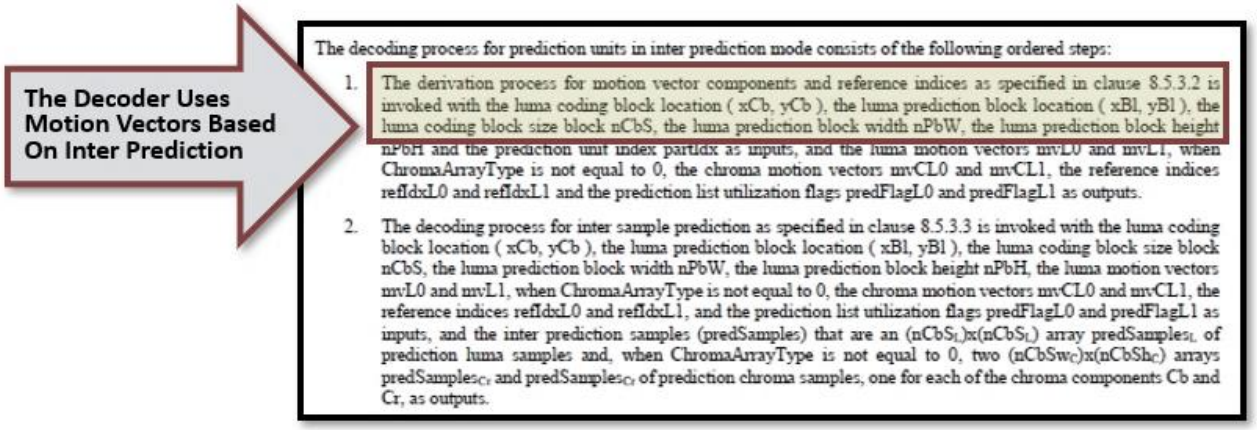
227. On information and belief, one or more of the AMD '073 Products include a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers

the motion vectors for the second frame. Further, HEVC documentation shows that "motion vectors are used during the decoding process for prediction units in inter prediction mode."



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (April 2015) (annotation added).

228. On information and belief, one or more of the AMD '073 Products include a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

229. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '073 Products in regular business operations.

230. On information and belief, the AMD '073 Products are available to businesses and individuals throughout the United States.

231. On information and belief, the AMD '073 Products are provided to businesses and individuals located in Delaware.

232. On information and belief, AMD has directly infringed and continues to directly infringe the '073 Patent by, among other things, making, using, offering for sale, and/or selling

technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the AMD '073 Products.

233. By making, using, testing, offering for sale, and/or selling products for resampling a primitive from texture space to screen space, including but not limited to the AMD '073 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '073 Patent, including at least claim 14 pursuant to 35 U.S.C. § 271(a).

234. On information and belief, AMD also indirectly infringes the '073 Patent by actively inducing infringement under 35 USC § 271(b).

235. AMD has had knowledge of the '073 Patent since at least service of the Original Complaint or shortly thereafter, and on information and belief, AMD knew of the '073 Patent and knew of its infringement, including by way of this lawsuit.

236. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '073 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '073 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '073 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '073 Products that have the capability of operating in a manner that infringe one or more of the claims of the '073 Patent, including at least claim 14, and AMD further provides documentation and training materials that cause customers and end users of the AMD '073 Products to utilize the products in a manner that directly infringe one or more claims of the '073

Patent.[24] By providing instruction and training to customers and end-users on how to use the AMD '073 Products in a manner that directly infringes one or more claims of the '073 Patent, including at least claim 14, AMD specifically intended to induce infringement of the '073 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '073 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '073 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '073 Patent, knowing that such use constitutes infringement of the '073 Patent.

237. The '073 Patent is well-known within the industry as demonstrated by multiple citations to the '073 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '073 Patent without paying a reasonable royalty. AMD is infringing the '073 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

238. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '073 Patent.

239. As a result of AMD's infringement of the '073 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's

[24] *See, e.g., AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT III
INFRINGEMENT OF U.S. PATENT NO. 7,532,220

240. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

241. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for resampling a primitive from texture space to screen space.

242. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD graphic processing units ("GPU") and accelerated processing units ("APU") containing Graphics Core Next ("GCN") 5th Generation functionality, including: Radeon RX Vega 56, Radeon RX Vega 64, Radeon RX Vega 64 Liquid, Radeon Vega Frontier Edition (Air Cooled), Radeon Vega Frontier Edition (Liquid Cooled), Radeon Instinct MI25, Radeon Pro WX 8200, Radeon Pro WX 9100, Radeon Pro V340, Radeon Pro V340 MxGPU, Ryzen 3 2200GE, Ryzen 3 Pro 2200GE, Ryzen 3 2200G, Ryzen 3 Pro 2200G, Ryzen 5 2400GE, Ryzen 5 Pro 2400GE, Ryzen 5 2400G, Ryzen 5 Pro 2400G (collectively, the "AMD '220 Product(s)").

243. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '220 Products in regular business operations.

244. On information and belief, one or more of the AMD '220 Products include technology for resampling a primitive from texture space to screen space.

245. On information and belief, the AMD '220 Products further enable the resampling of data from the texture map based on the primitive data based on corresponding pixel data that defines a portion of the display image using a 3D graphic model. This is accomplished through the sampling of textual map data that is stored based on the primitive pixels that are set to be

displayed on the device. Vector Memory operations transfer the resample data between the VGPRs and memory through the texture cache ("TC"). In the AMD '220 Products the texture maps are referred to as image objects and image objects / texture maps are accessed through dimension addresses. The below excerpt from AMD documentation describes that the vector memory operation sends texture fetch instructions. The texture fetch instructions contain a data mask that retrieves data specific to the primitive pixel data that is required for display on the device.

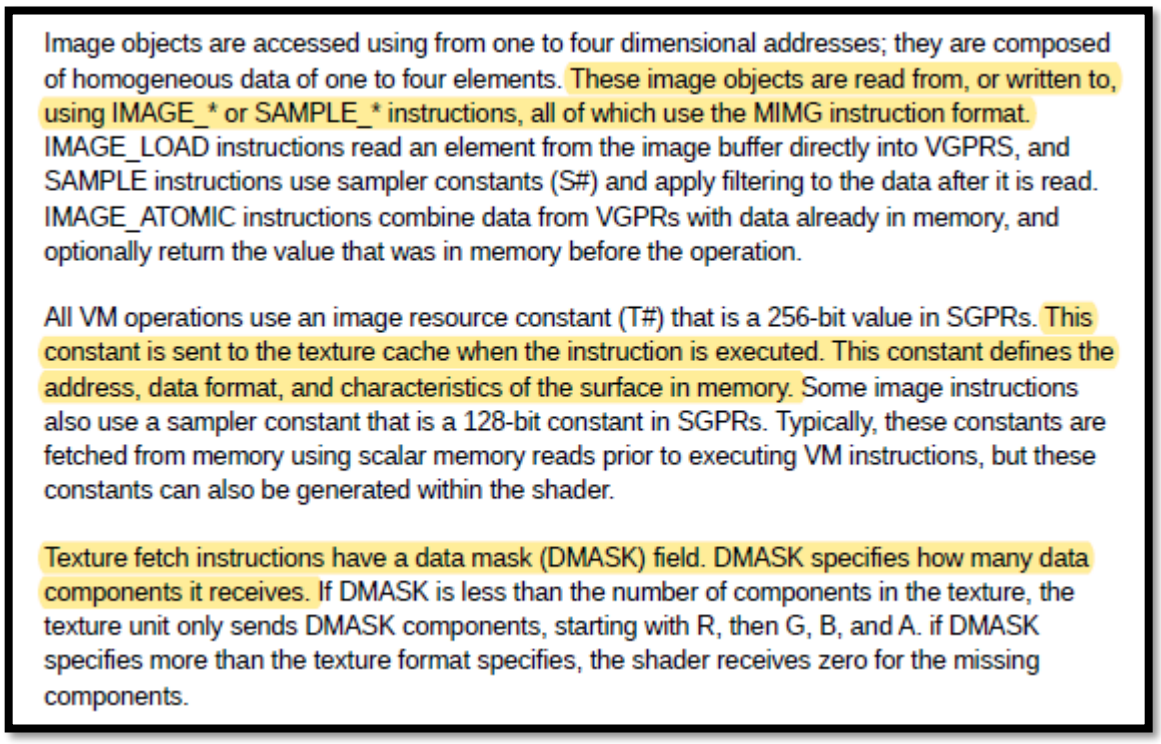


Image objects are accessed using from one to four dimensional addresses; they are composed of homogeneous data of one to four elements. These image objects are read from, or written to, using IMAGE_* or SAMPLE_* instructions, all of which use the MIMG instruction format. IMAGE_LOAD instructions read an element from the image buffer directly into VGPRS, and SAMPLE instructions use sampler constants (S#) and apply filtering to the data after it is read. IMAGE_ATOMIC instructions combine data from VGPRs with data already in memory, and optionally return the value that was in memory before the operation.

All VM operations use an image resource constant (T#) that is a 256-bit value in SGPRs. This constant is sent to the texture cache when the instruction is executed. This constant defines the address, data format, and characteristics of the surface in memory. Some image instructions also use a sampler constant that is a 128-bit constant in SGPRs. Typically, these constants are fetched from memory using scalar memory reads prior to executing VM instructions, but these constants can also be generated within the shader.

Texture fetch instructions have a data mask (DMASK) field. DMASK specifies how many data components it receives. If DMASK is less than the number of components in the texture, the texture unit only sends DMASK components, starting with R, then G, B, and A. if DMASK specifies more than the texture format specifies, the shader receives zero for the missing components.

"*Vega" Instruction Set Architecture*, AMD REFERENCE GUIDE at § 8.2 (July 28, 2017) (emphasis added).

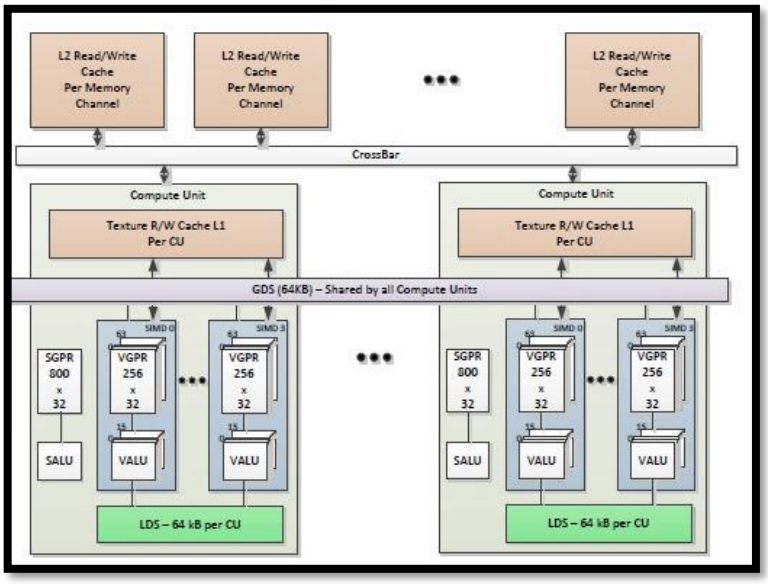
246. On information and belief, AMD has directly infringed and continues to directly infringe the '220 Patent by, among other things, making, using, offering for sale, and/or selling technology for resampling a primitive from texture space to screen space, including but not limited to the AMD '220 Products.

247. On information and belief, one or more of the AMD '220 Products enable an optimal resampling algorithm for primitives in three-dimensional graphics models by choosing between algorithms dynamically per primitive, based upon the size of the primitive.

248. On information and belief, one or more of the AMD '220 Products enable optimal resampling for primitives by balancing between the quality of the resampling, thus rendering a more realistic three-dimensional graphic, and considering system limitations such as available processor capacity and memory size.

249. On information and belief, the AMD '220 products can share data between different work-items. Data sharing pulls the texture map that is stored in the L1 memory cache.

250. On information and belief, the below diagram shows how the AMD Products comprise a GCN stream processor that stores texture data in memory. Specifically, data sharing pulls the texture map that is stored in the L1 memory cache. The following diagram shows the memory hierarchy that is available to each work-item.



AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 at § 2.3 (August 2016).

251. On information and belief, the AMD '220 Products comprise an apparatus that includes a texture memory for storing texture maps. Specifically, the AMD Products support storing texture maps as Image Objects that are then retrieved for display on the associated primitive.

> To improve efficiency and reduce overhead, the flexible memory hierarchy is re-used for graphics, with a little dedicated hardware. The address generation unit receives 4 texture addresses per cycle, and then calculates 16 sampling addresses for the nearest neighbors. The samples are read from the L1 data cache and decompressed in the Texture Mapping Unit (or TMU). The TMU then filters adjacent samples to produce as many as 4 final interpolated texels per clock. The TMU output is converted to the desired format and ultimately written into the vector register file for further use. The format conversion hardware is also used for writing some values out to memory in graphics kernels.

AMD Graphic Cores Next ("GCN") Architecture, AMD WHITEPAPER at 9 (June 2012) (emphasis added).

252. On information and belief, one or more of the AMD '220 Products maps primitives of a three-dimensional graphics model from a texture space to a screen space.

253. On information and belief, the below excerpt from AMD documentation shows how the texture maps are placed in memory as Image Objects that are then sampled using Texture Samplers. Texture Samples describe how a texture map samples texel data and handles mip-maps.

State	Access by GCN S/W	Access by Host S/W	Width (bits)	Description
Texture Samplers	R	W	128	A texture sampler describes how a texture map sample instruction (IMAGE) filters texel data and handles mip-maps. Texture samplers must first be loaded into four contiguous SGPRs prior to use by an IMAGE instruction.
Texture Resources	R	W	128 or 256	A texture resource describes the location, layout, and data type of a texture map in memory. A texture resource must be loaded into four or eight contiguous SGPRs prior to use by an IMAGE instruction.

AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 at § 2.2 (August 2016).

254. On information and belief, one or more of the AMD '220 Products include a texture memory for storing texture maps.

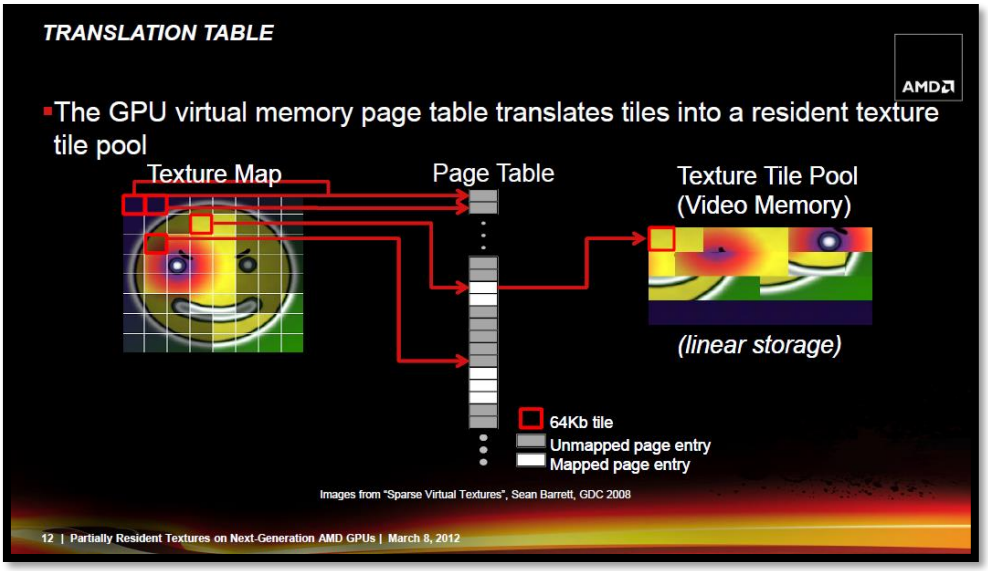
255. On information and belief, one or more of the AMD '220 Products includes a resampler being operative to, for each primitive, resample data from a texture map that corresponds to the primitive to corresponding pixel data defining a portion of a display image that corresponds to the primitive.

256. On information and belief, the AMD Products contain an Image sampler that defines what operations to perform on the resampled texture map data read by "sample instructions." *"Vega" Instruction Set Architecture*, AMD REFERENCE GUIDE at § 8.4.3 (July 28, 2017).

257. On information and belief, the resample commands can include two or more algorithms including "Lod Bias" (the distance from the viewer the switch to lower resolution mip maps takes place), "PCF" (percentage close filtering), and "LOD Clamp."

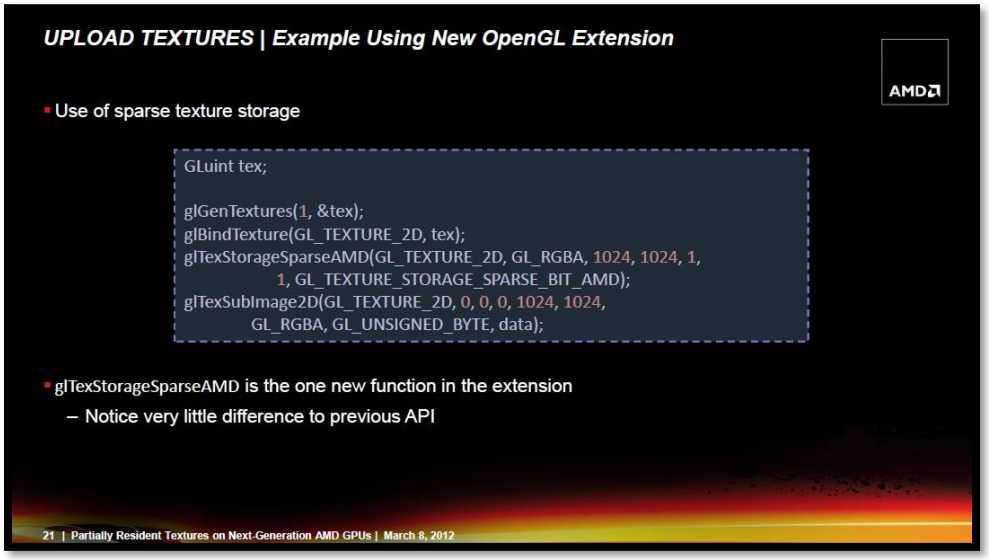
258. On information and belief, the AMD Products in resampling the texture map, perform the resampling based on the size of the primitive that is required and can include two or more algorithms that define the resampling. For example, the image_sample value is defined by the spatial coordinates of the primitive. *"Vega" Instruction Set Architecture*, AMD REFERENCE GUIDE at § 8.4.3 (July 28, 2017).

259. On information and belief, the AMD Products also perform the resampling of texture map data corresponding to a primitive that defines a portion of a display image through the use of partially resident textures ("PRT"). The below excerpt from AMD documentation describes that AMD's PRT technology places texture maps into the GPU video memory with an associated page table that comprises a memory page table that corresponds texture tiles into a resident texture tile pool.



Bill Bilodeau, Graham Sellers, Karl Hillesland, *Partially Resident Textures on Next Generation GPUs*, AMD PRESENTATION at 12 (March 8, 2012).

260. On information and belief, the below excerpt from an AMD developer presentation shows one mechanism in which the AMD '220 Products place texture maps into texture storage.

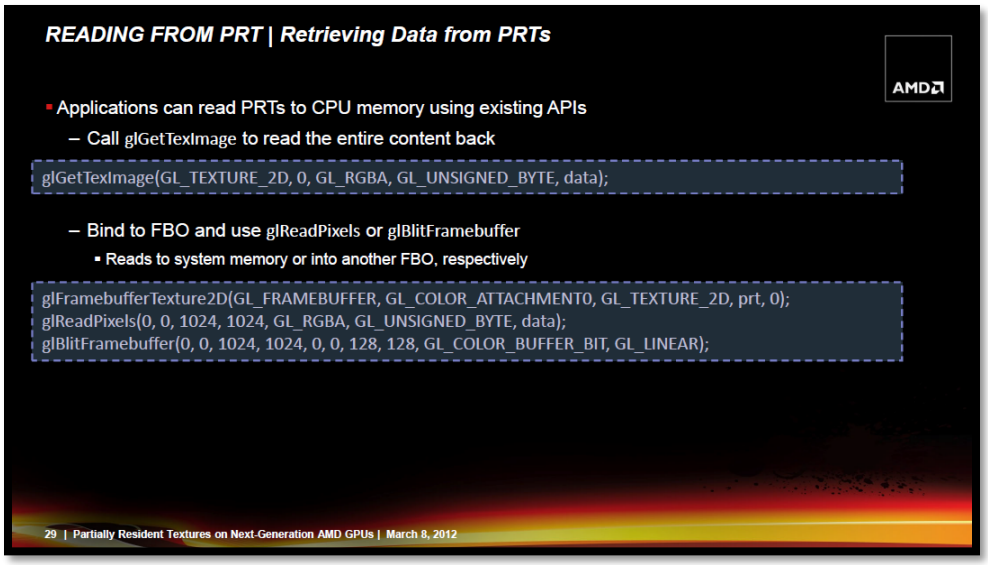


Bill Bilodeau, Graham Sellers, Karl Hillesland, *Partially Resident Textures on Next Generation GPUs*, AMD PRESENTATION at 21 (March 8, 2012).

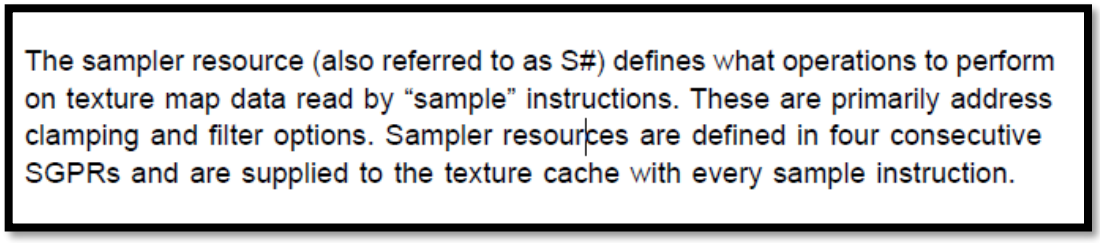
261. On information and belief, texture map data is placed in memory and the AMD '220 Products can resample the texture map (read data from the PRT) that corresponds to the primitive pixels that are to be displayed on the device. For example, the below excerpt from an

AMD Presentation states that these read commands can include "glGetTexImage" the retrieved data is then placed in the Frame Buffer for display.

262. On information and belief, the AMD Products contain samplers that enable the "resampling" of texture map data that is stored in data. The following excerpts describe this process.



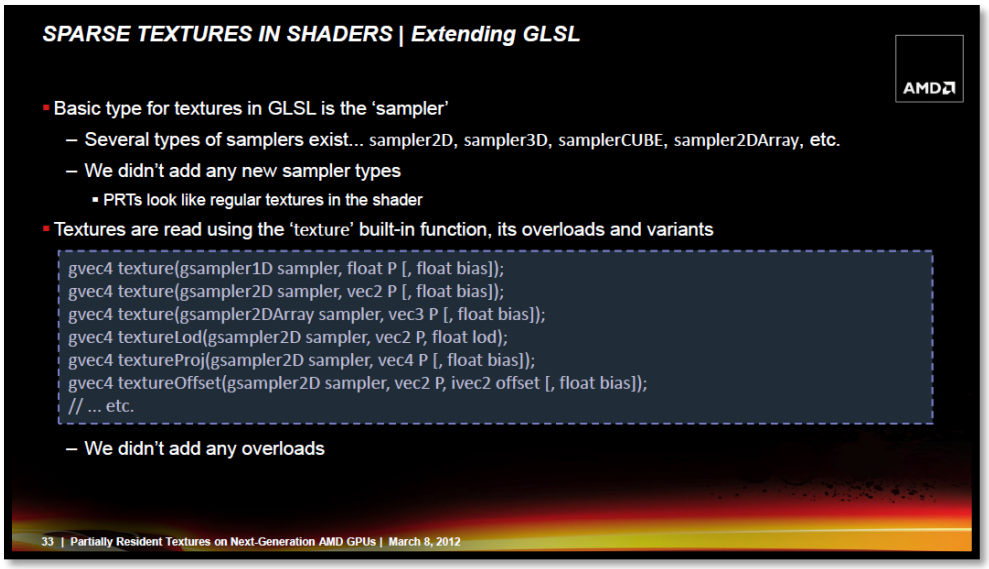
AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 at § 8.2.6 (August 2016).



Bill Bilodeau, Graham Sellers, Karl Hillesland, *Partially Resident Textures on Next Generation GPUs*, AMD PRESENTATION at 29 (March 8, 2012).

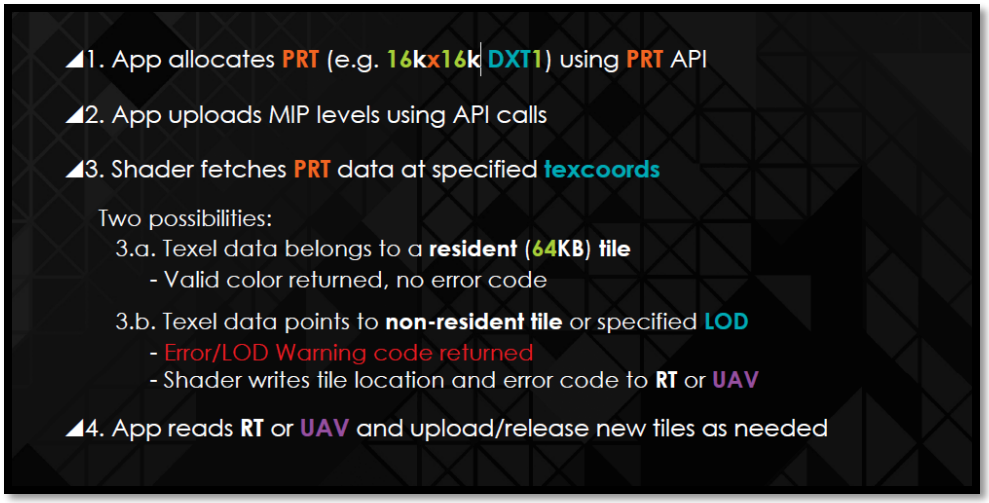
263. On information and belief, one or more of the AMD '220 Products include a "resampler" that selects a resampling algorithm for performing the resampling from multiple resampling algorithms. The selection is dependent on at least the size of the primitive.

264. On information and belief, the resampling of data from the texture map can be performed based on two or more sampling algorithms these sampler algorithms include "sampler3D," "samplerCUBE," "sampler2DArragy." The below excerpt from an AMD Presentation describes how the resampler can fetch the texture map data associated with primitive pixel data based on a variety of sampler algorithms.



Bill Bilodeau, Graham Sellers, Karl Hillesland, *Partially Resident Textures on Next Generation GPUs*, AMD PRESENTATION at 29 (March 8, 2012) (box showing the various sampler algorithms that can be used to resample data from the texture map).

265. On information and belief, the below excerpt from an AMD document shows that resampling of texture map data occurs "at specific TexCoords." TexCoords are an array of texture coordinates. The use of TexCoords to retrieve data from the texture map for display is further evidence establishing that the resampling of data from the texture map is performed based on a size of the primitive.



Layla Mah, *Powering the Next Generation of Graphics: AMD GCN Architecture*, AMD GCN PRESENTATION at 92 (March 2013).

266. On information and belief, the below excerpt from AMD documentation describes some of the instruction commands that trigger resampling of texture data.

32	IMAGE_SAMPLE	sample texture map.
33	IMAGE_SAMPLE_CL	sample texture map, with LOD clamp specified in shader.
34	IMAGE_SAMPLE_D	sample texture map, with user derivatives
35	IMAGE_SAMPLE_D_CL	sample texture map, with LOD clamp specified in shader, with user derivatives.
36	IMAGE_SAMPLE_L	sample texture map, with user LOD.
37	IMAGE_SAMPLE_B	sample texture map, with lod bias.
38	IMAGE_SAMPLE_B_CL	sample texture map, with LOD clamp specified in shader, with lod bias.
39	IMAGE_SAMPLE_LZ	sample texture map, from level 0.
40	IMAGE_SAMPLE_C	sample texture map, with PCF.
41	IMAGE_SAMPLE_C_CL	SAMPLE_C, with LOD clamp specified in shader.

"Vega" Instruction Set Architecture, AMD REFERENCE GUIDE at § 12.16 (July 28, 2017) (emphasis added).

267. On information and belief, the AMD '220 Products are available to businesses and individuals throughout the United States.

268. On information and belief, the AMD '220 Products are provided to businesses and individuals located in Delaware.

269. By making, using, testing, offering for sale, and/or selling products for resampling a primitive from texture space to screen space, including but not limited to the AMD '220 Products,

AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '220 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

270. On information and belief, AMD also indirectly infringes the '220 Patent by actively inducing infringement under 35 USC § 271(b).

271. AMD has had knowledge of the '220 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '220 Patent and knew of its infringement, including by way of this lawsuit.

272. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '220 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '220 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '220 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '220 Products that have the capability of operating in a manner that infringe one or more of the claims of the '220 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '220 Products to utilize the products in a manner that directly infringe one or more claims of the '220 Patent.[25] By providing instruction and training to customers and end-users on how to use the AMD '220 Products in a manner that directly infringes one or more claims of the '220 Patent, including

[25] *See, e.g.*, *Vega Instruction Set Architecture*, AMD REFERENCE GUIDE (July 28, 2017); *AMD Graphic Cores Next ("GCN") Architecture,* AMD WHITEPAPER (June 2012); AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 (August 2016); Bill Bilodeau, Graham Sellers, Karl Hillesland, *Partially Resident Textures on Next Generation GPUs*, AMD PRESENTATION (March 8, 2012); Layla Mah, *Powering the Next Generation of Graphics: AMD GCN Architecture*, AMD GCN PRESENTATION (March 2013).

at least claim 1, AMD specifically intended to induce infringement of the '220 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '220 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '220 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '220 Patent, knowing that such use constitutes infringement of the '220 Patent.

273. The '220 Patent is well-known within the industry as demonstrated by multiple citations to the '220 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '220 Patent without paying a reasonable royalty. AMD is infringing the '220 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

274. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '220 Patent.

275. As a result of AMD's infringement of the '220 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT IV
INFRINGEMENT OF U.S. PATENT NO. 6,714,257

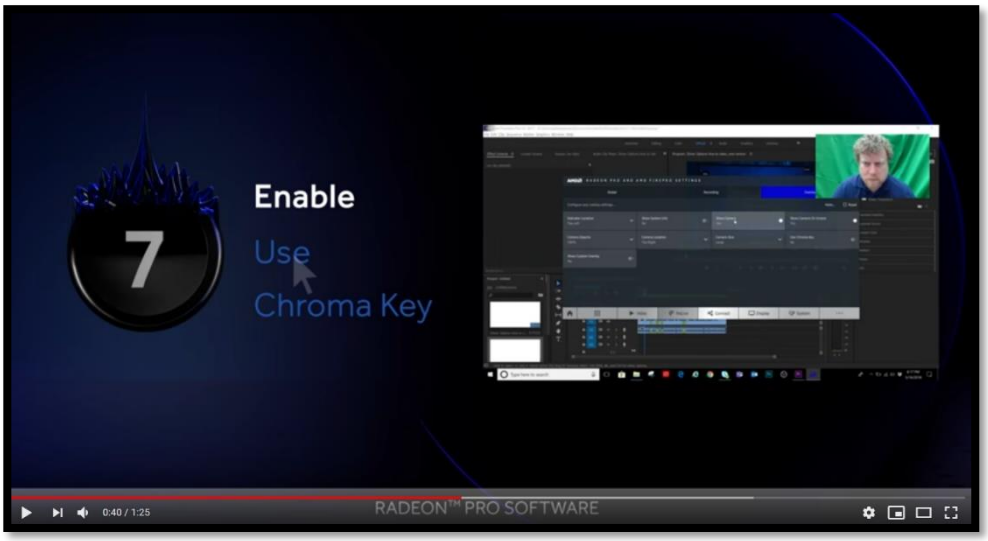
276. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

277. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for image processing.

278. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Graphics Core Next (GCN) Architecture-based Desktop Graphics products supporting Radeon ReLive, including the following models: Radeon RX Vega Series, Radeon RX 500 Series, Radeon RX 400 Series, Radeon Pro Duo, AMD Radeon R9 Fury, R9 300, R7 300 Series, AMD Radeon R9 200, R7 200, R5 300, R5 240 Series, AMD Radeon HD 8500 – HD 8900 Series, and AMD Radeon HD 7700 – HD 7900 Series (collectively, the "AMD '257 Product(s)").

279. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '257 Products in regular business operations.

280. On information and belief, the AMD '257 Products enable the processing of a stream of digital video data wherein a Chroma Key is used to output pre-processed data. The below excerpt from a 2018 AMD presentation shows how the chroma key is applied to a pre-processed stream of digital video that is captured using a web camera.



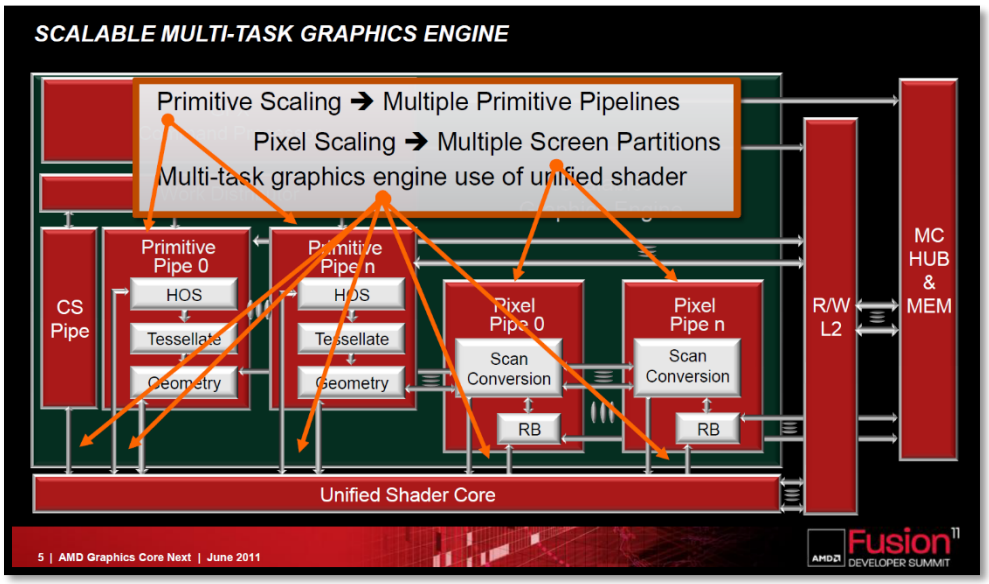
Radeon Pro ReLive: How to Set up & Use Chroma Key, AMD YOUTUBE.COM VIDEO (July 3, 2018). available at: https://www.youtube.com/watch?v=-j7KopH1pFo

281. On information and belief, the AMD '257 Products include Graphics Core Next ("GCN") technology which takes the key-only image corresponding to key only regions and converts the image into vector data that can then be scaled.

> GCN also adds new media and image processing instructions in the vector ALUs. Specifically, there are two new instructions: a 4x1 sum-of-absolute-differences (SAD) and quad SAD that operate on 32-bit pixels with 8-bit colors. Using these new instructions, a Compute Unit can execute 64 SADs/cycle which translates into 256 operations per clock. These instructions are very powerful and essential for emerging GPU applications such as gesture recognition or video search. For example, AMD's Steady Video 2.0 technology uses the new SAD and QSAD instructions to remove shakiness from recorded or streaming videos in real time.

AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 7 (June 2012) (emphasis added).

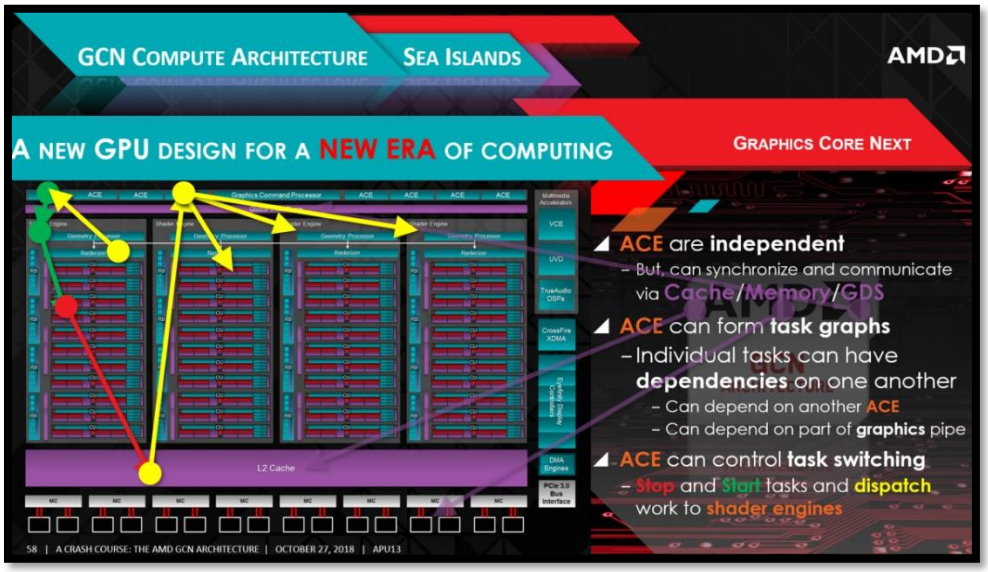
282. On information and belief, the following excerpt from AMD Documentation shows how the graphic pipeline in the AMD Products (specifically the GCN technology) converts image data into vector data that can then be scaled and displayed.



Michael Mantor and Mike Houston, *AMD Graphic Core Next: Low Power High Performance Graphics & Parallel Compute*, AMD FUSION DEVELOPER SUMMIT PRESENTATION at 5 (2011).

283. On information and belief, the AMD '257 Products comprise a command processor which is responsible for merging the scaled key-only image and the scaled keyed image "on the

fly." Specifically, the Asynchronous Compute Engines (ACE) are responsible for managing compute shaders, while a graphics command processor handles graphics shaders and fixed function hardware. "Each ACE can handle a parallel stream of commands, and the graphics command processor can have a separate command stream for each shader type, creating an abundance of work to take advantage of GCN's multi-tasking." *AMD Graphics Cores Next (GCN) Architecture*, AMD WHITE PAPER at 11 (June 2012). The below excerpt from an AMD Developer Conference presentation shows how the ACE as part of the graphic pipeline can perform functions such as merging images.



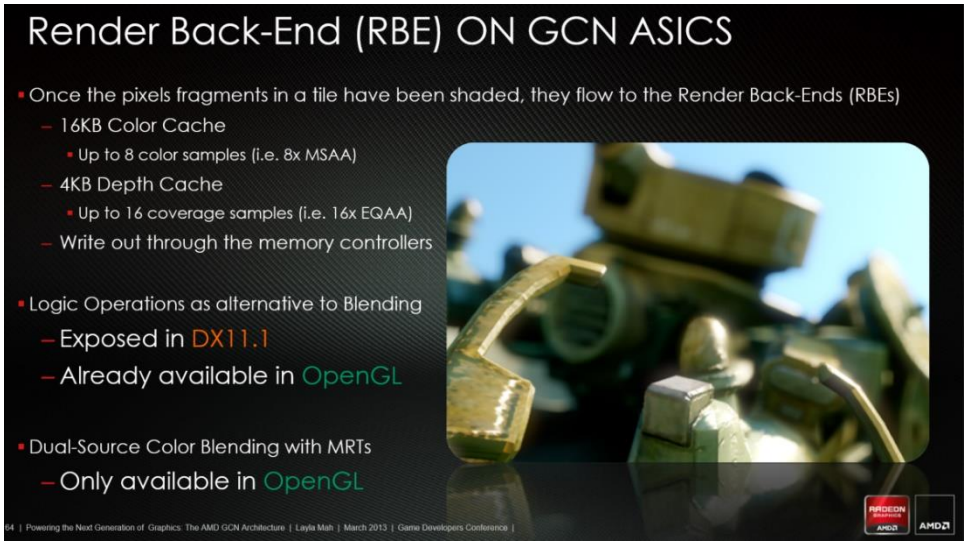
Layla Mah, *Powering the Next Generation of Graphics: The AMD GCN Architecture*, AMD DEVELOPERS CONFERENCE PRESENTATION at 64 (March 2013) (yellow arrows showing the ACE functionality ability to perform multiple dispatch tasks on the image data).

284. On information and belief, the AMD '257 Products scale the keyed image to form a scaled keyed image. Specifically, the AMD '257 Products graphics engine exports data from a shared memory where it is stored as vectors. The scaled vector image is placed in the graphics pipeline in the global shared memory ("GDS"). The Export unit is the Compute Unit's window to the fixed function graphics hardware as well as the global data share (GDS).

> When all the computations have been finished, the results are typically sent to other units in the graphics pipeline. For example, once pixels have been shaded, they are typically sent to the render back-ends for depth and stencil tests and any blending before the final output to the display. The export unit writes results from the programmable stages of the graphics pipeline to the fixed function ones, such as tessellation, rasterization and the render back-ends.

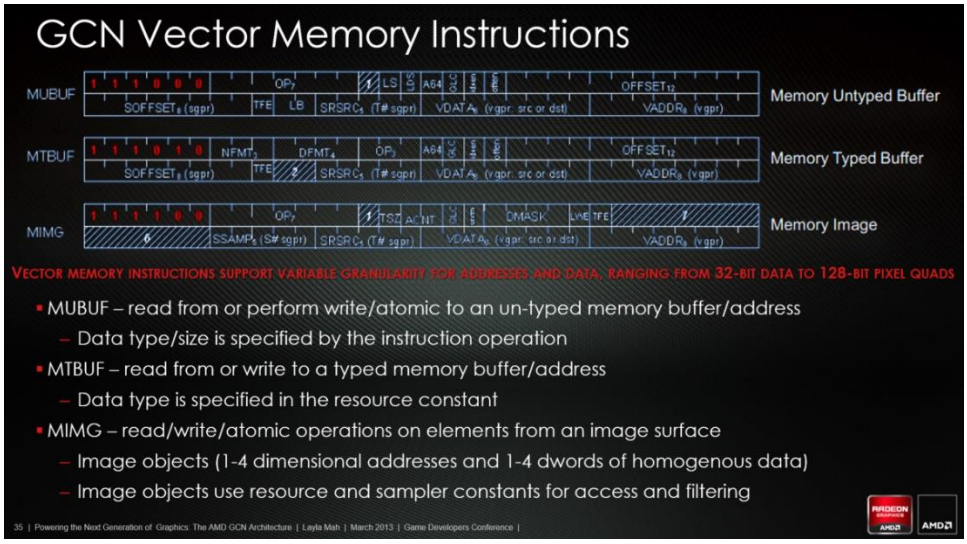
AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 8 (June 2012).

285. On information and belief, the AMD '257 Products merge the scaled key-only image and the scaled keyed image. The scaled image can be merged by the AMD GSN and then rendered to the user using render back-ends ("RBEs"). The below excerpt from an AMD presentation illustrates the process wherein the AMD system renders the merged image by writing the image out through the memory controllers.



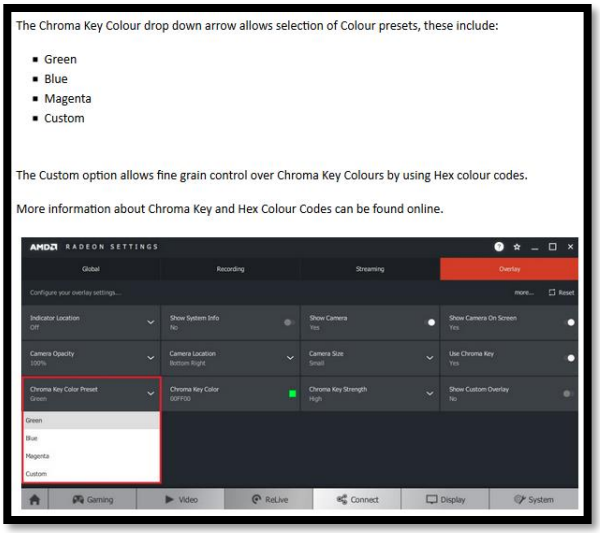
Layla Mah, *Powering the Next Generation of Graphics: The AMD GCN Architecture,* AMD DEVELOPERS CONFERENCE PRESENTATION at 64 (March 2013).

286. On information and belief, the AMD '257 Products contain GCN Vector memory instructions that take image objects and use resource and sampler constraints wherein the key-only image is written as a series of vectors that can then be scaled and displayed on the device interface.



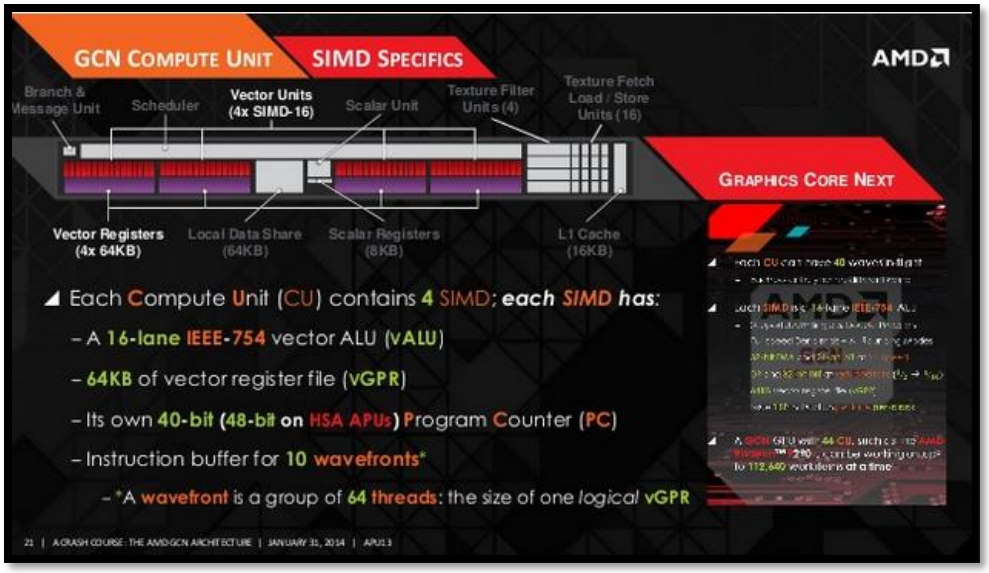
Layla Mah, *Powering the Next Generation of Graphics: The AMD GCN Architecture*, AMD DEVELOPERS CONFERENCE PRESENTATION at 35 (March 2013).

287. On information and belief, the AMD '257 Products include functionality for creating a key-only image corresponding to key regions in the keyed image. The following excerpt from AMD documentation describes that the Chroma Key can be used for, "Chroma Key provides background transparency when using a web camera for streaming content. Chroma Key can be fine-tuned with color removal strength pre-sets and custom colors." *How to Capture Your Gameplay Using Radeon ReLive*, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018).



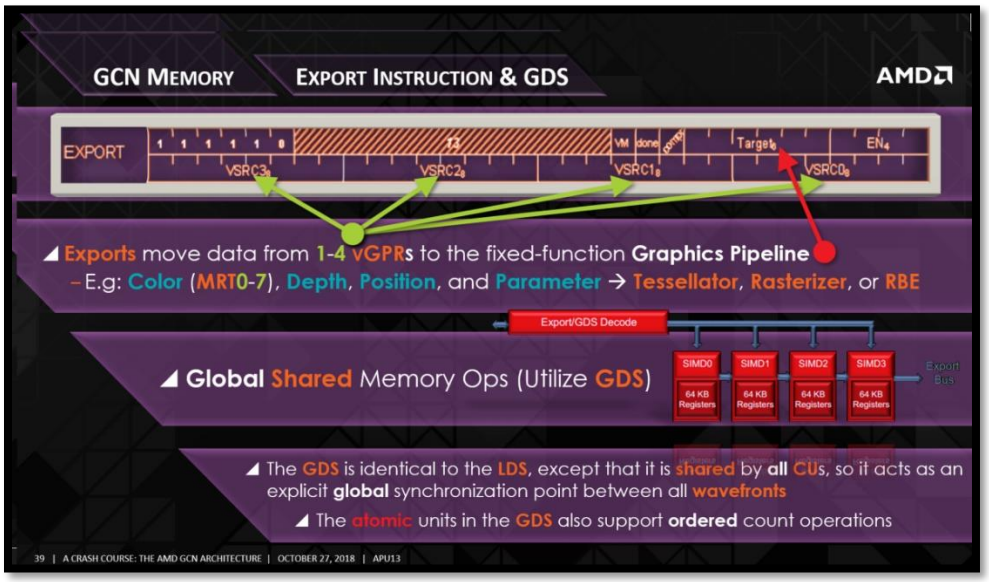
How to Capture Your Gameplay Using Radeon ReLive, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018).

288. On information and belief, the AMD '257 Products scale the key-only image to form a scaled key-only image. Specifically, the AMD Products import the key-only image and convert it to vector units where it is stored and then scaled. By storing the color-key-only image in the GCN processor, the sample rate conversion process corresponding to the converter is automatically provided by the conventional sample rate converter that scales the color-key-extracted image. The below excerpt from an AMD presentation about the architecture of GCN shows that the image is placed in memory and converted to vector units that can then be scaled.



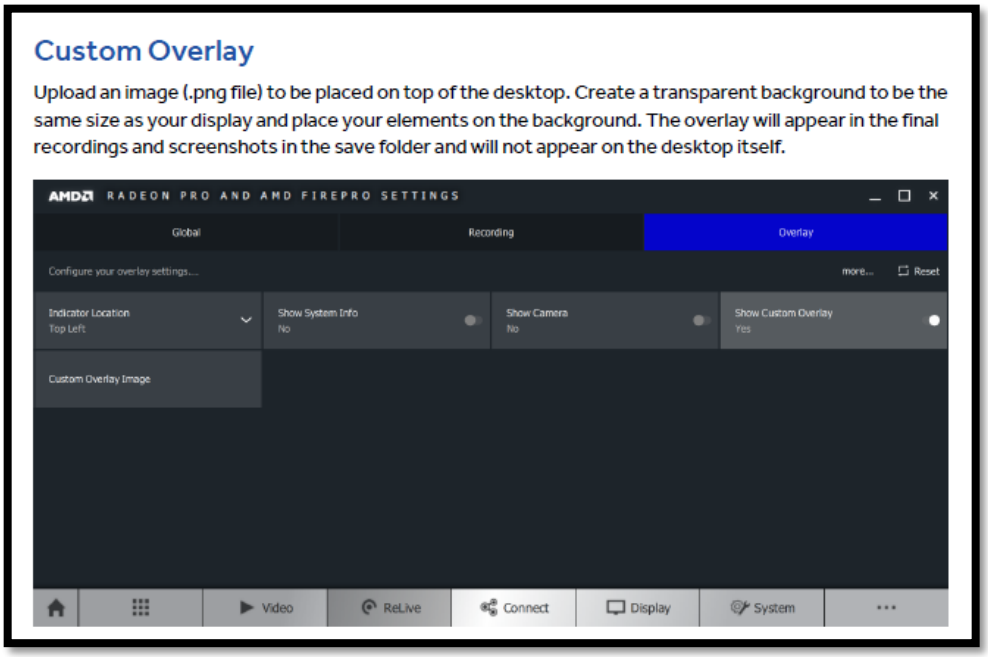
Layla Mah, *GS-4106 The AMD GCN Architecture - A Crash Course,* AMD DEVELOPER PRESENTATION at 21 (January 31, 2014).

289. On information and belief, the below excerpt from a 2018 presentation from AMD shows that the scaled image is placed in the GDS for export to the Export Bus where it is made available for display on the device.



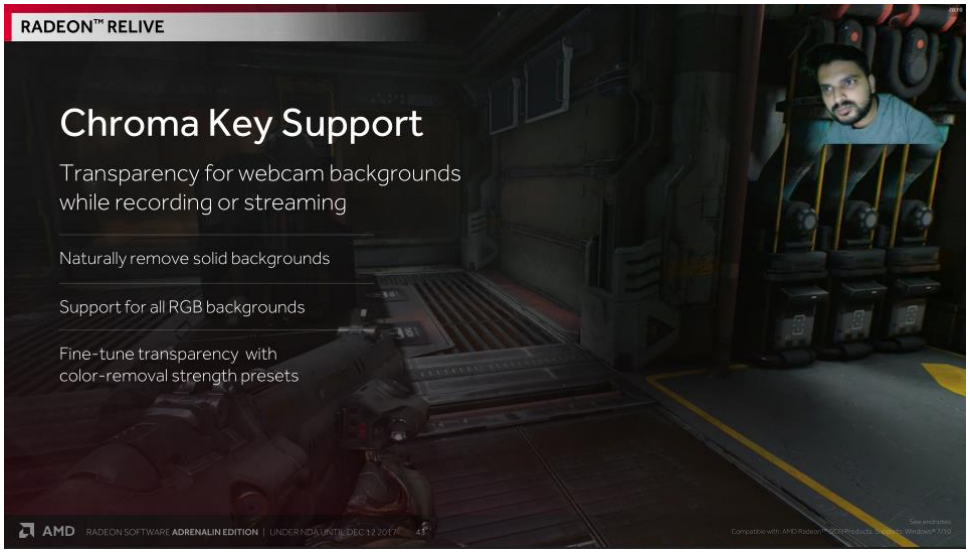
Layla Mah, *The AMD GCN Architecture: A Crash Course,* AMD DEVELOPER SUMMIT PRESENTATION at 39 (October 18, 2018) (the green arrows show that the data is moved from the vGPRs to the fixed function graphics pipeline as part of the export process).

290. On information and belief, in the AMD '257 Products a color key is used to generate a transparent background in the video stream and then a custom overlay image (.png file) is placed into the data stream (or saved to a folder on the desktop).



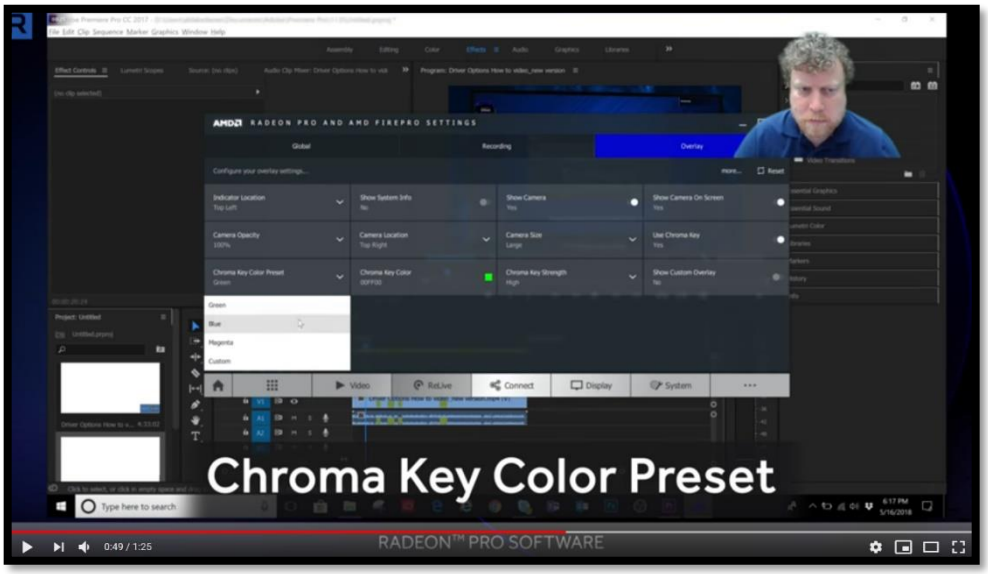
Radeon Pro ReLive in AMD Radeon Pro Settings, AMD USER GUIDE at 16 (2018).

291. On information and belief, the AMD '257 Products enable a feature that streamers use to create transparent webcam backgrounds. Once enabled, there are options for Chroma Key Color Preset, Chroma Key Color, and Chroma Key Strength.



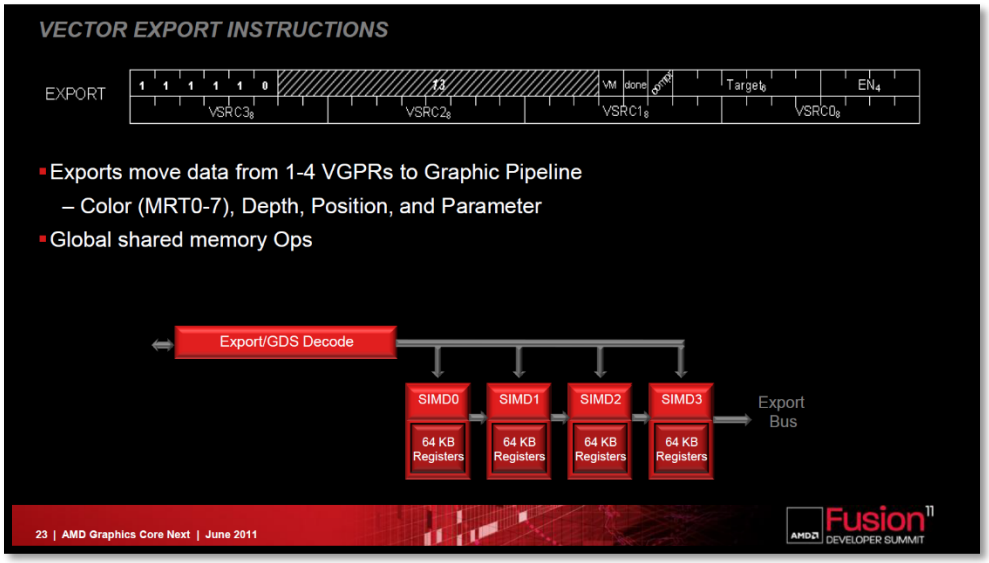
Nate Oh, *AMD Releases Radeon Software Adrenalin Edition: Overlay, App & More for 2017,* ANANDTECH.COM WEBSITE (December 12, 2017), available at: https://www.anandtech.com/show/12147/amd-releases-radeon-software-adrenalin-edition/4 ("ReLive Adrenalin also comes with Chroma Key support, a feature that streamers use to create transparent webcam backgrounds. Once enabled, there are options for Chroma Key Color Preset, Chroma Key Color, and Chroma Key Strength. Using the strength presets, transparency can be increased or decreased.").

292. On information and belief, the below excerpt from an AMD video tutorial shows how the scaled keyed image and key-only image are merged and displayed on the device.



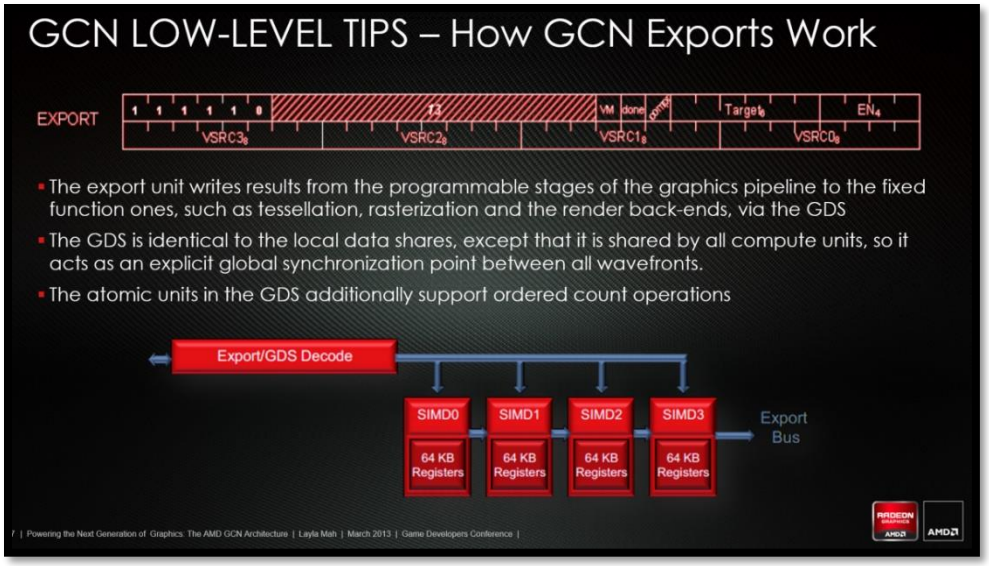
Radeon Pro ReLive: How to Set up & Use Chroma Key, AMD YOUTUBE.COM VIDEO (July 3, 2018). available at: https://www.youtube.com/watch?v=-j7KopH1pFo

293. On information and belief, the AMD '257 Products convert the key-only image data into a set of vector instructions in the graphic pipeline that then are scaled for display on the device.



Michael Mantor and Mike Houston, *AMD Graphic Core Next: Low Power High Performance Graphics & Parallel Compute*, AMD FUSION DEVELOPER SUMMIT PRESENTATION at 23 (2011).

294. On information and belief, the AMD '257 Products export the vectorized key-only image by writing the results via the graphics pipeline using tessellation, rasterization, and render back-ends via the memory on the AMD GCN processor.



Layla Mah, *Powering the Next Generation of Graphics: The AMD GCN Architecture*, AMD DEVELOPERS CONFERENCE PRESENTATION at 37 (March 2013).

295. On information and belief, the AMD '257 Products are available to businesses and individuals throughout the United States.

296. On information and belief, the AMD '257 Products are provided to businesses and individuals located in Delaware.

297. On information and belief, AMD has directly infringed and continues to directly infringe the '257 Patent by, among other things, making, using, offering for sale, and/or selling technology for image processing, including but not limited to the AMD '257 Products.

298. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the AMD '257 Products, AMD has injured Dynamic Data and is liable for directly infringing one or more claims of the '257 Patent, including at least claim 9, pursuant to 35 U.S.C. § 271(a).

299. On information and belief, AMD also indirectly infringes the '257 Patent by actively inducing infringement under 35 USC § 271(b).

300. On information and belief, AMD has had knowledge of the '257 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '257 Patent and knew of its infringement, including by way of this lawsuit.

301. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '257 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '257 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '257 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '257 Products that have the capability of operating in a manner that infringe one or more of the claims of the '257 Patent, including at least claim 9, and AMD further provides documentation and training materials that cause customers and end users of the AMD '257 Products to utilize the products in a manner that directly infringe one or more claims of the '257 Patent.[26] By providing instruction and training to customers and end-users on how to use the AMD '257 Products in a manner that directly infringes one or more claims of the '257 Patent, including at least claim 9, AMD specifically intended to induce infringement of the '257 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '257

[26] *See, e.g.*, *How to Capture Your Gameplay Using Radeon ReLive*, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018); *Radeon Pro ReLive: How to Set up & Use Chroma Key*, AMD YOUTUBE.COM VIDEO (July 3, 2018). *available at*: https://www.youtube.com/watch?v=-j7KopH1pFo; *Radeon Pro ReLive in AMD Radeon Pro Settings*, AMD USER GUIDE (2018); Nate Oh, *AMD Releases Radeon Software Adrenalin Edition: Overlay, App & More for 2017*, ANANDTECH WEBSITE (December 12, 2017), *available at*: https://www.anandtech.com/show/12147/amd-releases-radeon-software-adrenalin-edition/4 (excerpting AMD's presentation regarding the Radeon ReLive product).

Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '257 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '257 Patent, knowing that such use constitutes infringement of the '257 patent.

302. The '257 Patent is well-known within the industry as demonstrated by multiple citations to the '257 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '257 Patent without paying a reasonable royalty. AMD is infringing the '257 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

303. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '257 Patent.

304. As a result of AMD's infringement of the '257 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT V
INFRINGEMENT OF U.S. PATENT NO. 8,073,054

305. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

306. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for estimating a current motion vector for a group of pixels of an image.

307. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '054 Product(s)").

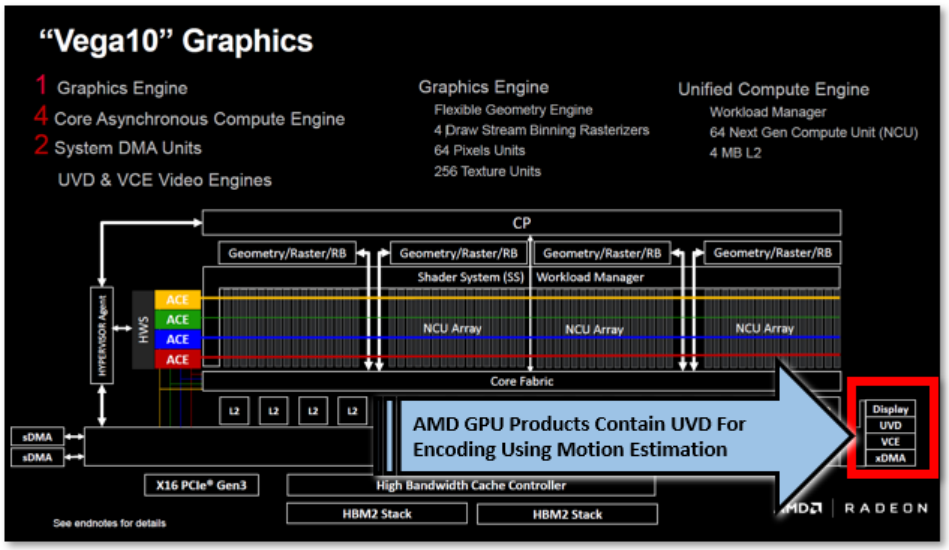
308. Documentation from AMD shows that the AMD '054 Products perform a motion vector estimation method. AMD '054 Products perform the method of encoding video content using High Efficiency Video Coding ("HEVC").

Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm

Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

309. On information and belief, the AMP '054 Products contain a "UVD" that functions to encode video using motion estimation values in addition to motion vectors. The following diagram from AMD's documentation of the AMD Vega 10 product identifies that the video coding engine incorporated in the AMD GPU Products uses motion estimation.



AMD's Radeon Next Generation GPU Architecture "Vega 10", RADEON PRESENTATION at 12 (2017) (annotations added) (showing that in the AMD Products H.265 encoding hardware is included and identified as UVD).

310. On information and belief, the AMD '054 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the AMD Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by AMD Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

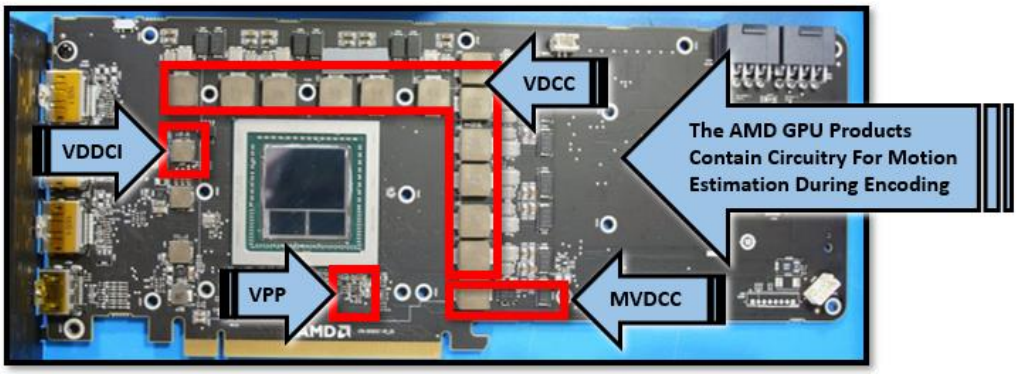
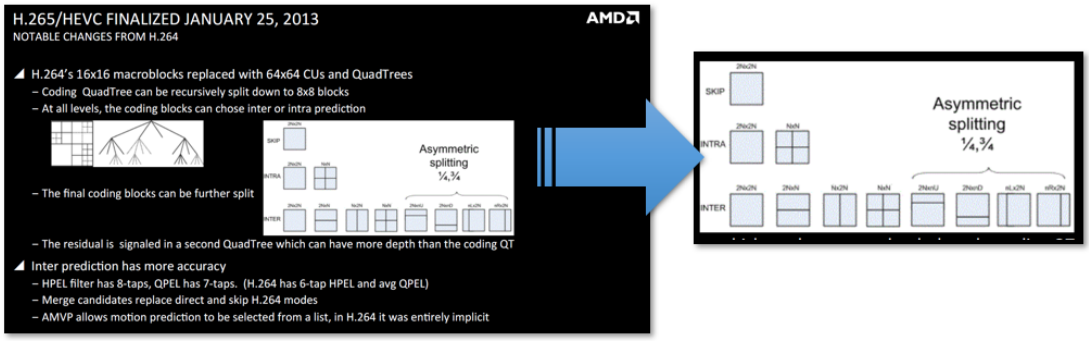
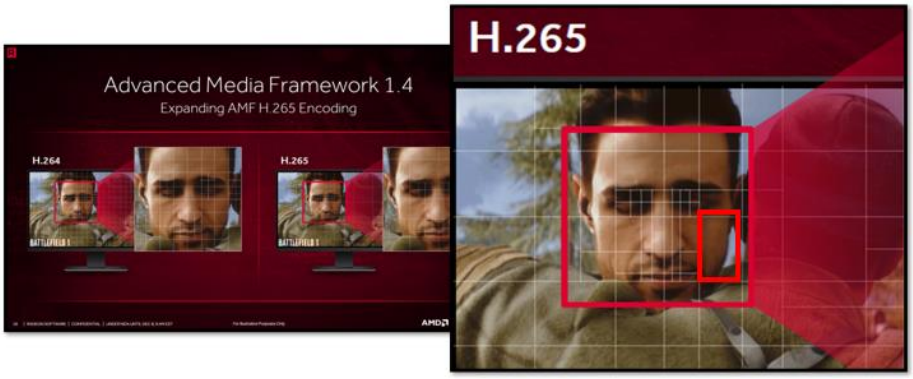


IMAGE OF AMD VEGA PRODUCT CIRCUIT BOARD: DETAILED PRODUCT ANALYSIS (2018) (annotation added) (showing the processor for encoding video data).

311. On information and belief, the AMD '054 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center. The following excerpt from an AMD presentation regarding the H.265 encoder states that during the encoding process, "Asymmetric Splitting" in which "at all levels, the coding blocks can choose inter or intra prediction" is performed."



X265 Open Source H.265 Encoder: Optimization Details, AMD DEVELOPER SUMMIT PRESENTATION at 4 (November 19, 2013) (annotations added) (showing that the AMD Products use asymmetric splitting in the encoding process).



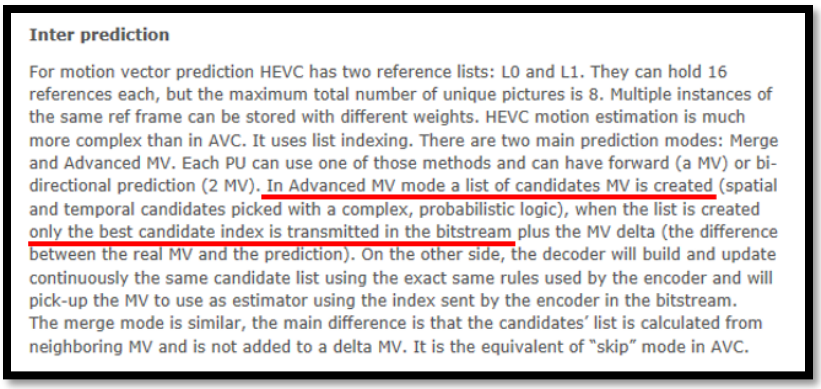
RADEON SOFTWARE PRESENTATION at 16 (2017) (showing that the encoding functionality allows offset from a center position).

312. On information and belief, one or more of the AMD '054 Products include technology for estimating a current motion vector for a group of pixels of an image

313. On information and belief, AMD has directly infringed and continues to directly infringe the '054 patent by, among other things, making, using, offering for sale, and/or selling technology for estimating a current motion vector for a group of pixels of an image, including but not limited to the AMD '054 Products.

314. On information and belief, by complying with the HEVC standard, AMD's devices – such as the AMD '054 Products - necessarily infringe the '054 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '054 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to AMD's infringement of the '054 patent: "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

315. On information and belief, the AMD '054 Products comprise functionality for generating a set of candidate motion vectors for a grouping of pixels (prediction unit). The HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, only the best candidate index is transmitted.



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

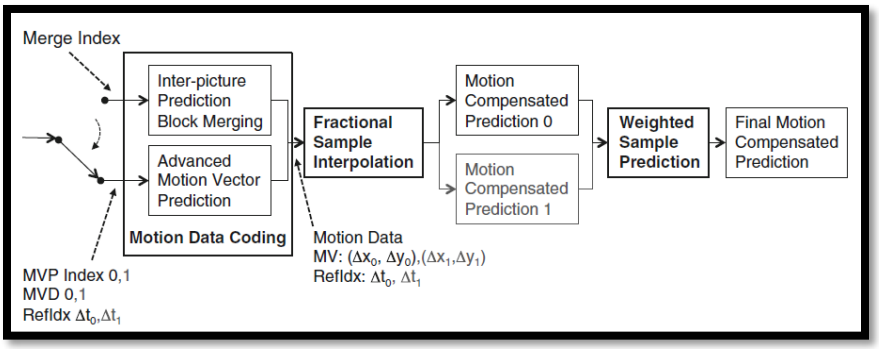
316. On information and belief, one or more of the AMD '054 Products enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

> HEVC introduces a so-called merge mode, which sets all motion parameters of an inter picture predicted block equal to the parameters of a merge candidate [6]. The merge mode and the motion vector prediction process optionally allow a picture to reuse motion vectors of prior pictures for motion vector coding,

Frank Bossen, *et al*., *HEVC Complexity and Implementation Analysis*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY VOL. 22 NO. 12 at 1686 (December (2012).

317. On information and belief, the following block diagram illustrates the form of encoded video data received by the AMD '054 Products. Specifically, the encoded video data received by the AMD '054 Products is encoded using inter-picture prediction where the motion data of a block is correlated with neighboring blocks. To exploit this correlation, motion data is

not directly coded in the bitstream, but predictively coded based on neighboring motion data. Further, the AMD '054 Products receive data that is encoded using advanced motion vector prediction where the best predictor for each motion block is signaled to the decoder. In addition, inter-prediction block merging derives all motion data of a block from the neighboring blocks.



Benjamin Bross, *et al*., *Inter-Picture Prediction in HEVC,* In HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (2014).

318. On information and belief, the AMD '054 products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The AMD '054 Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.

three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector

predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

319. On information and belief, one or more of the AMD '054 Products include a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

320. On information and belief, the AMD '054 Products contain functionality for generating match errors of the respective candidate motion vectors. The HEVC standard calculates match errors of respective candidate motion vectors. The match errors are referred to as the MV delta. The MV delta is the difference between the real MV and the candidate predication.

Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

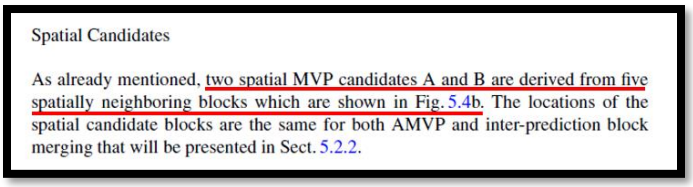
Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

321. On information and belief, any implementation of the HEVC standard would infringe the '054 patent as every implementation of the standard requires the elements in one or more claims of the '054 patent, including but not limited to claim 1, by way of example: a match error unit for calculating match errors of respective candidate motion vectors and calculating the

further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

322. On information and belief, one or more of the AMD '054 Products include a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

323. On information and belief, the AMD '054 Products select the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors. The first motion vector is labeled 'A' and the second motion vector is labeled 'B.'



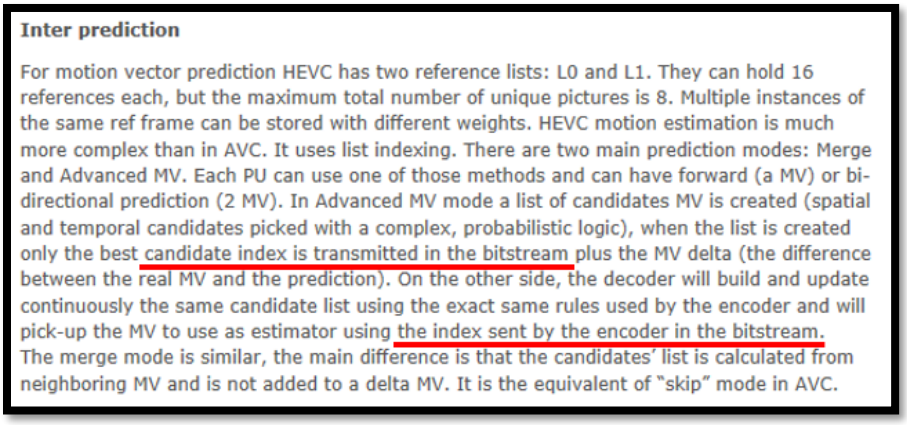
Spatial Candidates

As already mentioned, two spatial MVP candidates A and B are derived from five spatially neighboring blocks which are shown in Fig. 5.4b. The locations of the spatial candidate blocks are the same for both AMVP and inter-prediction block merging that will be presented in Sect. 5.2.2.

Gary Sullivan, *et al*., HIGH EFFICIENCY VIDEO CODING (HEVC) ALGORITHMS AND ARCHITECTURES at 117 (2014) (emphasis added).

324. Further, the AMD '054 Products perform motion vector "competition / weighted sample prediction" by comparing the match errors of the candidate motion vectors. The match errors generated by the AMD '054 Products comprise the difference value between the second

motion vector and the first motion vector. Documentation of the encoding process states that the encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

325. On information and belief, the AMD '054 Products calculate the square of the difference between two corresponding pixels of the spatial position of the candidate block where the motion vector is located and the spatial position where the reference motion vector is located. As a result, this value is used to assess the similarity, or the matching degree, of a candidate block. Thus, in order to obtain the best matching vector, the AMD '054 Products apply a penalty value to every candidate block with a different motion vector (*MVx, MVy*) within the search window defined by the search range in the reference frame. Finally, a candidate block with the minimum penalty value will be denoted as the best matching block and used to calculate the best motion vector from the candidate motion vectors. The below excerpt from an article discussing the selection of a best motion vector describes that the selection of a motion vector is based on the position of the motion vector.

> The entire ME process is made up of three coarse-to-fine procedures, namely, MV prediction, integer-pixel ME and fractional-pixel ME. First, MV prediction predicts the start search position for the following motion search by utilizing the neighboring motion information. In HEVC, Advanced Motion Vector Prediction (AMVP), a new and effective technology that predicts the starting search position by referencing the motion vector (MV) information of spatial and temporal motion vector candidates, is adopted, which derives several most probable candidates based on data from adjacent PBs and the reference picture. The displacement between the starting search position and the current coding PU is called a predictive motion vector (PMV). HEVC also introduces a merge mode to derive the motion information from spatially or temporally neighboring blocks [1].

Yongfei Zhang, Chao Zhang, and Rui Fan, *Fast Motion Estimation in HEVC Inter Coding: An Overview of Recent Advances*, PROCEEDINGS, APSIPA ANNUAL SUMMIT AND CONFERENCE 2018 at 1 (November 2018) (emphasis added).

326. On information and belief, one or more of the AMD '054 Products include a motion estimation unit that calculates the further candidate motion vector on the basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different. Specifically, the HEVC standard arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process (see the red box in the below diagram).

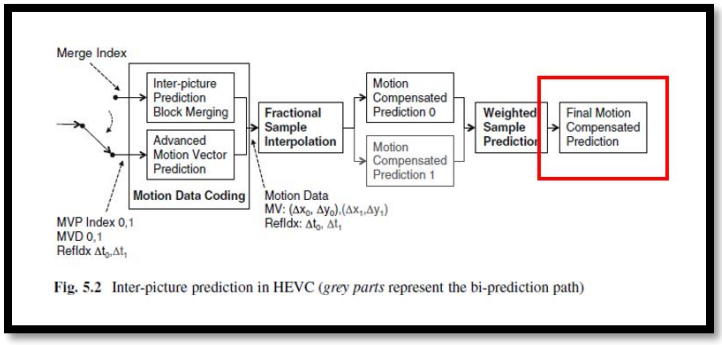


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

327. On information and belief, one or more of the AMD '054 Products include a motion estimation unit that arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

328. On information and belief, the AMD '054 Products are available to businesses and individuals throughout the United States.

329. On information and belief, the AMD '054 Products are provided to businesses and individuals located in the State of Delaware.

330. By making, using, testing, offering for sale, and/or selling products and services for estimating a current motion vector for a group of pixels of an image, including but not limited to the AMD '054 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '054 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

331. On information and belief, AMD also indirectly infringes the '054 Patent by actively inducing infringement under 35 USC § 271(b).

332. AMD has had knowledge of the '054 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '054 Patent and knew of its infringement, including by way of this lawsuit.

333. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '054 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '054 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '054 Patent

and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '054 Products that have the capability of operating in a manner that infringe one or more of the claims of the '054 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '054 Products to utilize the products in a manner that directly infringe one or more claims of the '054 Patent.[27] By providing instruction and training to customers and end-users on how to use the AMD '054 Products in a manner that directly infringes one or more claims of the '054 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '054 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '054 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '054 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '054 Patent, knowing that such use constitutes infringement of the '054 Patent.

334. The '054 Patent is well-known within the industry as demonstrated by multiple citations to the '054 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '054 Patent without paying a reasonable royalty. AMD is infringing the '054 Patent in a manner best described

[27] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

335. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '054 Patent.

336. As a result of AMD's infringement of the '054 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT VI
INFRINGEMENT OF U.S. PATENT NO. 6,774,918

337. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

338. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for image processing.

339. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors and products incorporating these chips. The infringing AMD Radeon graphic processors include: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '918 Product(s)").

340. On information and belief, the AMD '918 Products contain functionality for downloading on-screen display (OSD) data for generating an image on a display device. Specifically, the AMD Products have an input for receiving frame-based encoded video information. The AMD Products receive frame-based encoded video information in the form of video data that is encoded in the High Efficiency Video Coding (HEVC/H.265) format set by the ITU-T Video Coding Experts Group. Documentation and analysis of the circuity of the AMD Vega Product further confirms the AMD Products contain multiple inputs for receiving frame-based encoded video information as shown in the following image of the AMD Products circuity.

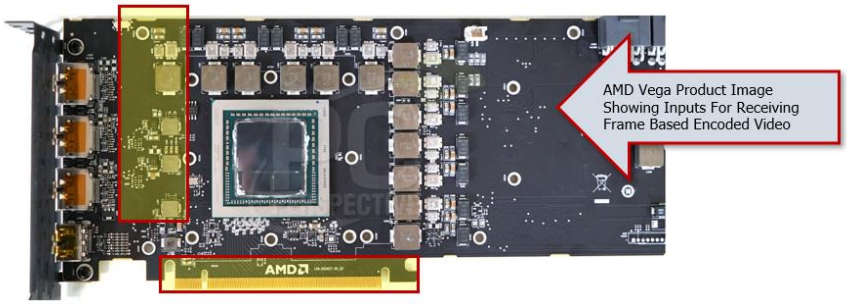
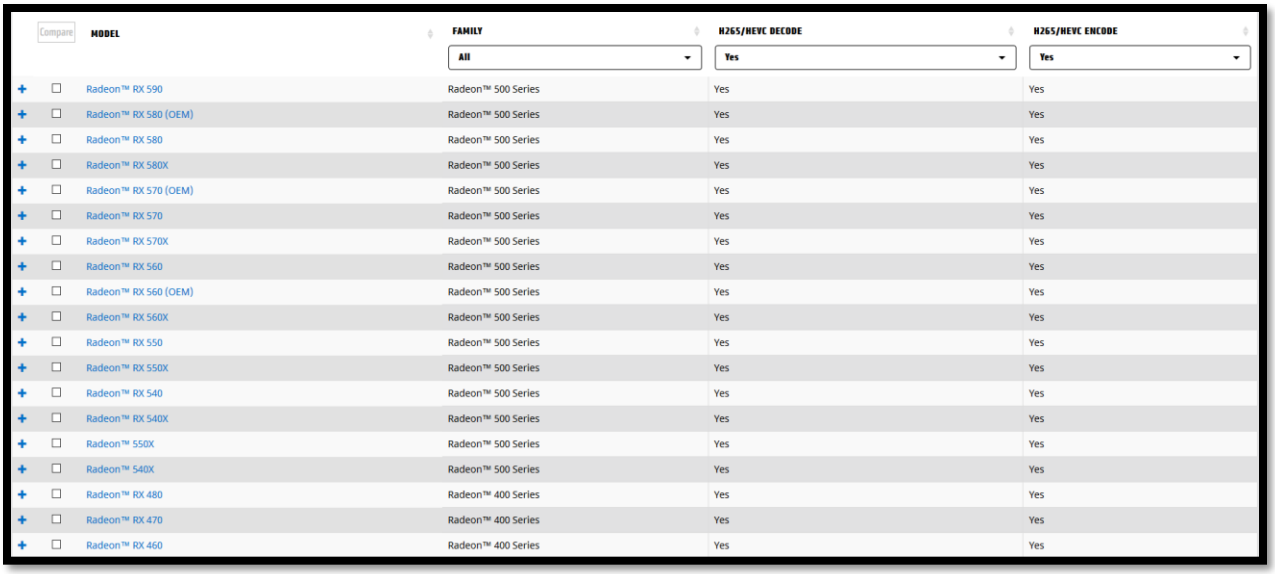


IMAGE OF AMD VEGA PRODUCT CIRCUIT BOARD: DETAILED PRODUCT ANALYSIS (2018) (annotation added) (showing inputs including: USB, Wi-Fi, and external memory).

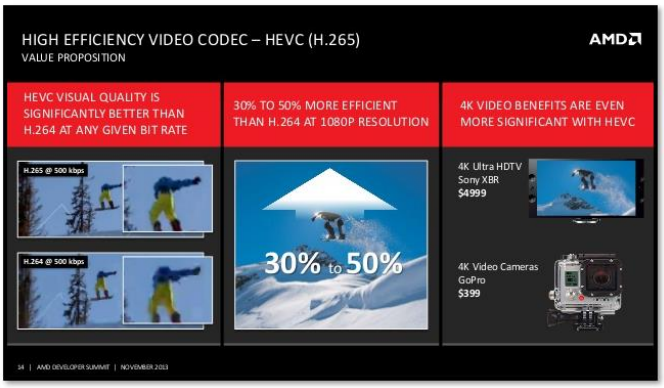
341. On information and belief, the AMD '918 Products include inputs for receiving and decoding HEVC video data. "The Infinity Fabric logic links the graphics core to other on-chip units like the multimedia, display, and I/O blocks. In 'Vega' 10, this fabric is clocked separately from the graphics cores a result, the GPU can maintain high clock speeds in the Infinity Fabric domain in order to facilitate fast DMA data transfers in workloads that feature little to no graphics activity, such as video transcoding." *Radeon's Next-Generation Vega Architecture,* AMD WHITEPAPER at 13 (2017).



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

342. On information and belief, AMD has identified that the inclusion of HEVC decoding in the AMD Products is a critical "value proposition." The below excerpt from an AMD Developer Summit presentation describes the importance of HEVC decoding in the AMD Products.



Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION at 14 (2013).

343. On information and belief, the AMD '918 Products use two types of prediction methods for decoding video data: inter prediction and intra prediction. Inter prediction utilizes motion vectors as well as an offset center and creates a list of possible motion vectors (MV) for the search area. The HEVC Specification (*e.g.*, *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (April 2015)) sets forth the standard that is followed by HEVC compliant devices, and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the AMD Products perform a method for decoding a video signal using motion vectors when performing encoding of H.265/HEVC video data. For example, the AMD Products contain functionality for decoding a video signal using motion vectors and motion estimation.

344. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '918 Products - necessarily infringe the '918 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '918 patent, including but not limited to claim 18. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO

REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to AMD's infringement of the '918 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

345. On information and belief, the AMD '918 Products receive a bitstream in which the data is segmented into Network Abstraction Layer ("NAL") Units. NAL Units are segments of data that can include video data and overlay data (such as captions and overlay images). The AMD Products support the receipt of VCL and non-VCL NAL units. The VCL NAL units contain the data that represents the values of the samples in the video pictures, and the non-VCL NAL units contain any associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

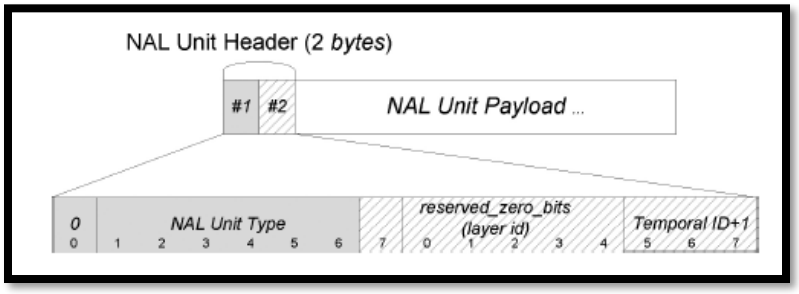
346. On information and belief, the VCL NAL Units contain segments of data which are used to generate an image (*e.g.*, HEVC image) on a display device. Each VCL NAL Unit comprises a discrete number of bites which make up a segment. The following excerpt from the

HEVC specification describes the NAL unit as being a segment with a "demarcation" setting forth where the segment ends and begins.

> NumBytesInNalUnit specifies the size of the NAL unit in bytes. This value is required for decoding of the NAL unit. Some form of demarcation of NAL unit boundaries is necessary to enable inference of NumBytesInNalUnit. One such demarcation method is specified in Annex B for the byte stream format. Other methods of demarcation may be specified outside of this Specification.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 7.4.2.1 (February 2018) (emphasis added).

347. On information and belief, VCL NAL Units comprise discrete video data that ends. It is between the receipt of VCL NAL Units that the overlay data (Non-VCL NAL Unit) data is received by the AMD Products.



Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, VOL.* 22, NO. 12 at 1875 (December 2012).

348. On information and belief, the AMD '918 Products are available to businesses and individuals throughout the United States.

349. On information and belief, the AMD '918 Products are provided to businesses and individuals located in the State of Delaware.

350. On information and belief, the HEVC bitstream structure is comprised of discreet data. In the gaps between the receipt by the AMD '918 Products of VCL NAL Units Non-VCL NAL Units are received by the AMD Products' decoder.

> An HEVC bitstream consists of a number of access units, each including coded data associated with a picture that has a distinct capturing or presentation time. Each access unit is divided into NAL units, including one or more VCL NAL units (i.e., coded slice NAL units) and zero or more non-VCL NAL units, e.g., parameter set NAL units or supplemental enhancement information (SEI) NAL units. Each NAL unit includes an NAL unit header and an NAL unit payload. Information in the NAL unit header can be (conveniently) accessed by media gateways, also known as media aware network elements (MANEs), for intelligent, media aware operations on the stream, such as stream adaptation.

Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY*, *VOL.* 22, NO. 12 at 1873 (December 2012).

351. On information and belief, Non-VCL NAL unit types include data such as supplemental enhancement information that is used to create overlays for display on the device.

Table 2.2 The 32 HEVC non-VCL NAL unit types

Non-VCL NAL unit types			
Parameter sets	32	VPS_NUT	Video parameter set
	33	SPS_NUT	Sequence parameter set
	34	PPS_NUT	Picture parameter set
Delimiters	35	AUD_NUT	Access unit delimiter
	36	EOS_NUT	End of sequence
	37	EOB_NUT	End of bitstream
Filler data	38	FD_NUT	Filler data
Supplemental enhancement information (SEI)	39	PREFIX_SEI_NUT	
	40	SUFFIX_SEI_NUT	
Reserved	41–47	RSV	
Unspecified	48–63	UNSPEC	

Gary J. Sullivan et al, HIGH EFFICIENCY VIDEO CODING (HEVC) at 29 (September 2014).

352. On information and belief, Non-VCL NAL Units include supplemental enhancement information ("SEI") messages. The SEI data that is received contains overlay information that can be combined with the image data that has already been received.

sei_message( ) {	Descriptor
payloadType = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadType += 255	
}	
last_payload_type_byte	u(8)
payloadType += last_payload_type_byte	
payloadSize = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadSize += 255	
}	
last_payload_size_byte	u(8)
payloadSize += last_payload_size_byte	
sei_payload(payloadType, payloadSize)	
}	

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 7.3.5 (February 2018).

353. On information and belief, the AMD '918 Products combine the VCL NAL Unit and Non-VCL NAL Unit information to create images that contain overlay information.

> The NAL units are decoded by the decoder to produce the decoded pictures that are output from the decoder. Both the encoder and decoder store pictures in a decoded picture buffer (DPB). This buffer is mainly used for storing pictures so that previously coded pictures can be used to generate prediction signals to use when coding other pictures. These stored pictures are called reference pictures. . . . There are two classes of NAL units in HEVC—video coding layer (VCL) NAL units and non-VCL NAL units. Each VCL NAL unit carries one slice segment of coded picture data while the non-VCL NAL units contain control information that typically relates to multiple coded pictures. <u>One coded picture, together with the non-VCL NAL units that are associated with the coded picture, is called an HEVC access unit</u>.

Gary J. Sullivan et al, HIGH EFFICIENCY VIDEO CODING (HEVC) at 14-15 (September 2014) (emphasis added).

354. By making, using, testing, offering for sale, and/or selling products for downloading on-screen display (OSD) data for generating an image on a display device., including but not limited to the AMD '918 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '918 Patent, including at least claim 18 pursuant to 35 U.S.C. § 271(a).

355. On information and belief, AMD also indirectly infringes the '918 Patent by actively inducing infringement under 35 USC § 271(b).

356. On information and belief, AMD has had knowledge of the '918 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '918 Patent and knew of its infringement, including by way of this lawsuit.

357. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '918 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '918 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '918 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '918 Products that have the capability of operating in a manner that infringe one or more of the claims of the '918 Patent, including at least claim 18, and AMD further provides documentation and training materials that cause customers and end users of the AMD '918 Products to utilize the products in a manner that directly infringe one or more claims of the '918 Patent.[28] By providing instruction and training to customers and end-users on how to use the AMD '918 Products in a manner that directly infringes one or more claims of the '918 Patent, including

[28] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, AMD RADEON PRESENTATION (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITEPAPER (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017).

at least claim 18, AMD specifically intended to induce infringement of the '918 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '918 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '918 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '918 Patent, knowing that such use constitutes infringement of the '918 Patent.

358. The '918 Patent is well-known within the industry as demonstrated by multiple citations to the '918 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '918 Patent without paying a reasonable royalty. AMD is infringing the '918 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

359. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '918 Patent.

360. As a result of AMD's infringement of the '918 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT VII
INFRINGEMENT OF U.S. PATENT NO. 8,184,689

361. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

362. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for encoding and decoding video data.

363. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD graphic processing units ("GPU") and accelerated processing units ("APU") containing Graphics Core Next ("GCN") 5th Generation functionality including: Radeon RX Vega 56, Radeon RX Vega 64, Radeon RX Vega 64 Liquid, Radeon Vega Frontier Edition (Air Cooled), Radeon Vega Frontier Edition (Liquid Cooled), Radeon Instinct MI25, Radeon Pro WX 8200, Radeon Pro WX 9100, Radeon Pro V340, Radeon Pro V340 MxGPU, Ryzen 3 2200GE, Ryzen 3 Pro 2200GE, Ryzen 3 2200G, Ryzen 3 Pro 2200G, Ryzen 5 2400GE, Ryzen 5 Pro 2400GE, Ryzen 5 2400G, Ryzen 5 Pro 2400G (collectively, the "AMD '689 Product(s)").

364. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '689 Products in regular business operations.

365. On information and belief, AMD has directly infringed and continues to directly infringe the '689 Patent by, among other things, making, using, offering for sale, and/or selling technology for encoding and decoding video data, including but not limited to the AMD '689 Products.

366. On information and belief, the AMD '689 Products encompass an image processing component that enables the storing in memory of video frames including at least a first and second frame. The below image shows a teardown of the AMD Product showing that AMD Products contain an image processing unit that receives, at a minimum, two frames of a video from memory. These frames are then processed by the video compensation unit of the AMD Products. Further, the AMD Products contain an encoder for motion estimation.

367. On information and belief, the AMD '689 Products use advanced motion vector prediction ("AMVP"). AVMP uses a derivation of several most probable candidates based on data from adjacent prediction blocks and the reference picture. The below image identifies an exemplar of the image processing component in the AMD Products.

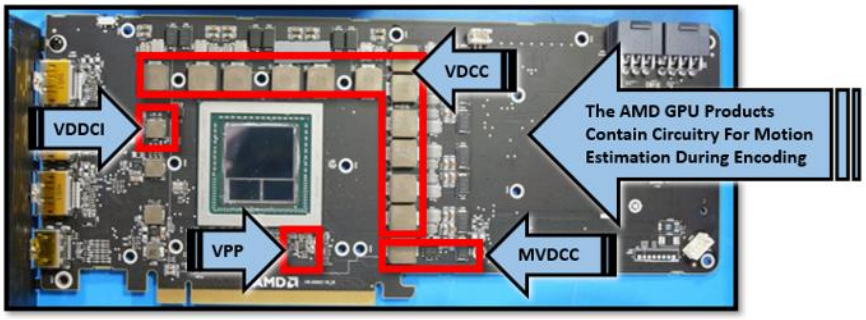
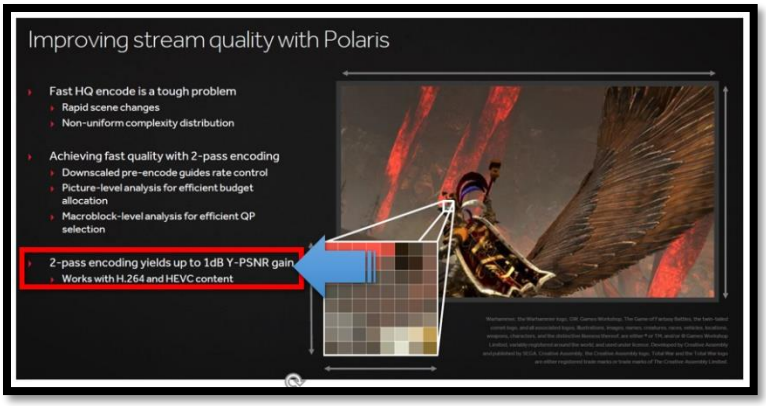


IMAGE OF AMD PRODUCT CIRCUIT BOARD: DETAILED PRODUCT ANALYSIS (2018) (annotations added).

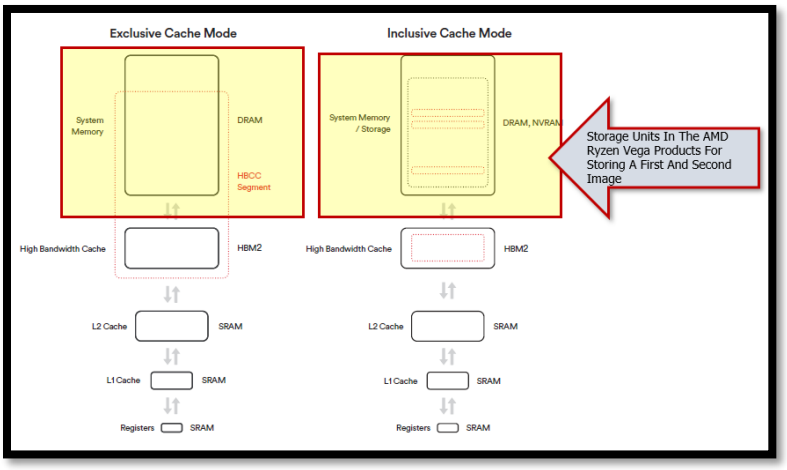
368. Further, AMD documentation establishes that the AMD Products include inputs for receiving and decoding HEVC video data. "The Infinity Fabric logic links the graphics core to other on-chip units like the multimedia, display, and I/O blocks. In 'Vega' 10, this fabric is clocked separately from the graphics cores a result, the GPU can maintain high clock speeds in the Infinity Fabric domain in order to facilitate fast DMA data transfers in workloads that feature little to no graphics activity, such as video transcoding." *Radeon's Next-Generation Vega Architecture,* AMD WHITEPAPER at 13 (2017).



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 36 (2016) (annotation added) (stating "2-pass encoding yields up to 1db Y-PSNR gain . . . works with H.264 and HEVC content).

369. On information and belief, the AMD '689 Products, perform the step of providing a subset of image data stored in the second memory in the first memory.

370. On information and belief, the AMD '689 Products include memory in the form of cached memory, solid state storage, and on chip memory. The below image shows the storage unit that enables the storing of a first input image and a second input image.

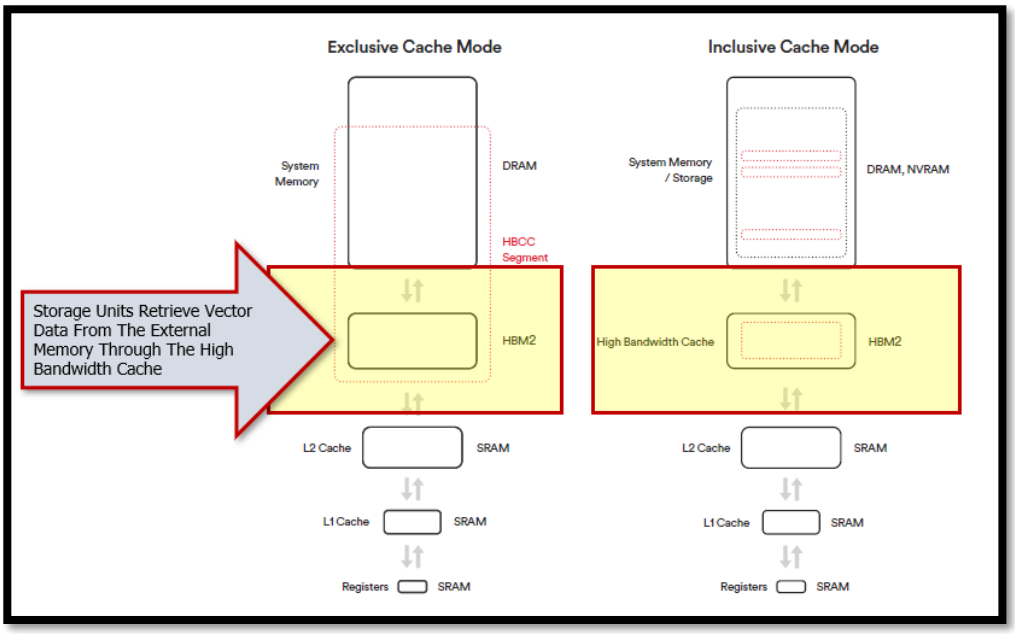


Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER at 5 (2017).

371. Although further motion vectors are selectively received by the AMD Product's motion compensation unit from a motion estimator or an external unit, at the system level the latency of fetching the data from the external unit (e.g., DRAM) is hidden by allowing for a

separate motion vector (dispatch stage in the pipeline) prior to the prediction stage. Thus, while the reference data of a given block is being fetched, the previous block is undergoing prediction.

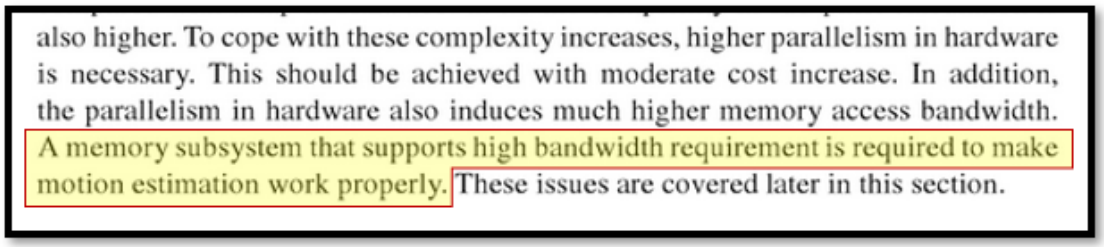
372. On information and belief, the below diagram from AMD documentation shows structures in the AMD '689 Product's functionality wherein an external motion vector field can be retrieved from an external unit. For example, the AMD Products include memory that is in the form of cached memory, solid state storage and on chip memory.



AMD Products Documentation, VEGA ARCHITECTURE WHITEPAPER AT at 5 (2017) (annotations added) (showing that the AMD Products comprise various forms of external memory).

373. On information and belief, the circuity of the AMD '689 Products contain multiple inputs for receiving frame-based encoded video information.

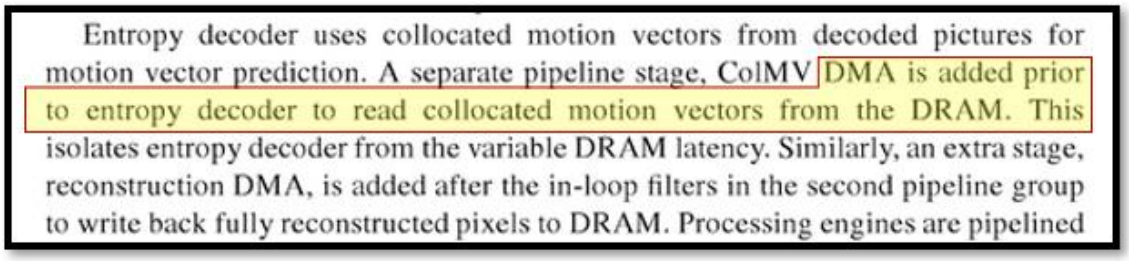
374. On infomratiom and belief, the AMD '689 Products include functionality for retrieving a motion vector field from a memory device that is attached to the image processing unit. The following excerpt from an analysis of the HEVC decoding process states that, because of the complexity of the motion vector prediction performed by HEVC, "[a] ***memory subsystem*** that supports high bandwidth requirement is required to make motion estimation work properly."



also higher. To cope with these complexity increases, higher parallelism in hardware is necessary. This should be achieved with moderate cost increase. In addition, the parallelism in hardware also induces much higher memory access bandwidth. A memory subsystem that supports high bandwidth requirement is required to make motion estimation work properly. These issues are covered later in this section.

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 348 (September 2014) (emphasis added).

375. The memory subsystem that is required places motion vector data in a motion estimation engine and an external unit (e.g., DRAM). For example, the reference design for an HVEC decoder states that "DMA [Direct Memory Access] is added prior to entropy decoder to read collocated motion vectors from the DRAM."



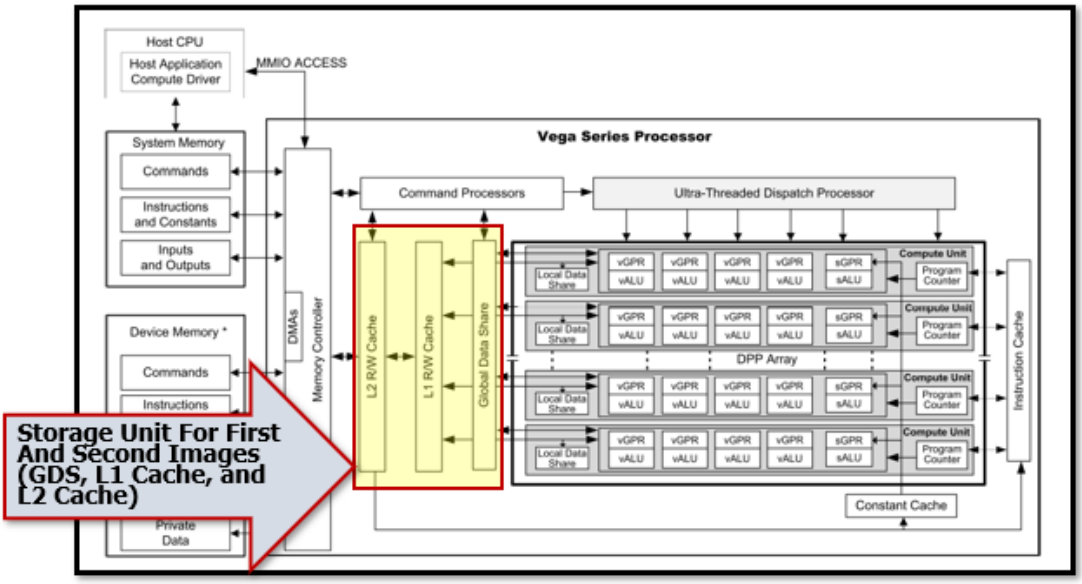
Entropy decoder uses collocated motion vectors from decoded pictures for motion vector prediction. A separate pipeline stage, ColMV DMA is added prior to entropy decoder to read collocated motion vectors from the DRAM. This isolates entropy decoder from the variable DRAM latency. Similarly, an extra stage, reconstruction DMA, is added after the in-loop filters in the second pipeline group to write back fully reconstructed pixels to DRAM. Processing engines are pipelined

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 306 (September 2014) (emphasis added).

376. The AMD '689 Products perform the step of simultaneously encoding and decoding more than one image of the video stream by accessing the subset of image data stored in a first and second memory. Further, the AMD '689 Products simultaneously encode and decode by access sharing to at least one image.

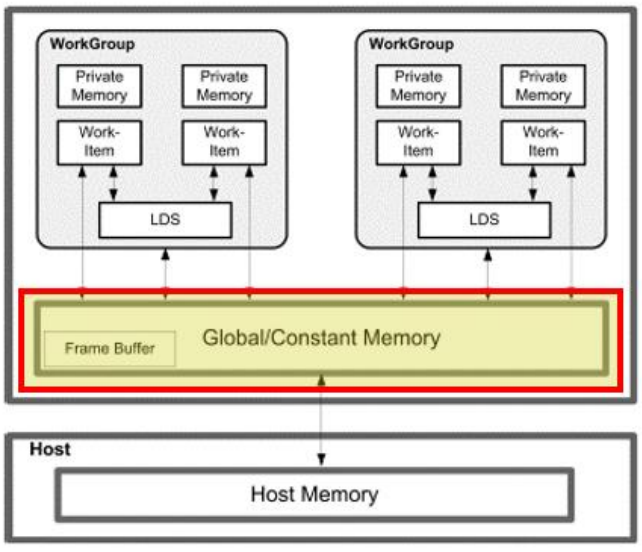
377. On information and belief, the AMD '689 Products include a storage unit in the form of memory structures including the Global Data Share ("GDS" or "Global Constant Memory"), L1 Cache, and L2 Cache. The below image shows a storage unit in one or more of the

AMD '689 Products. First and second input images are written to the storage unit via the memory controller and then retrieved to generate motion vectors.



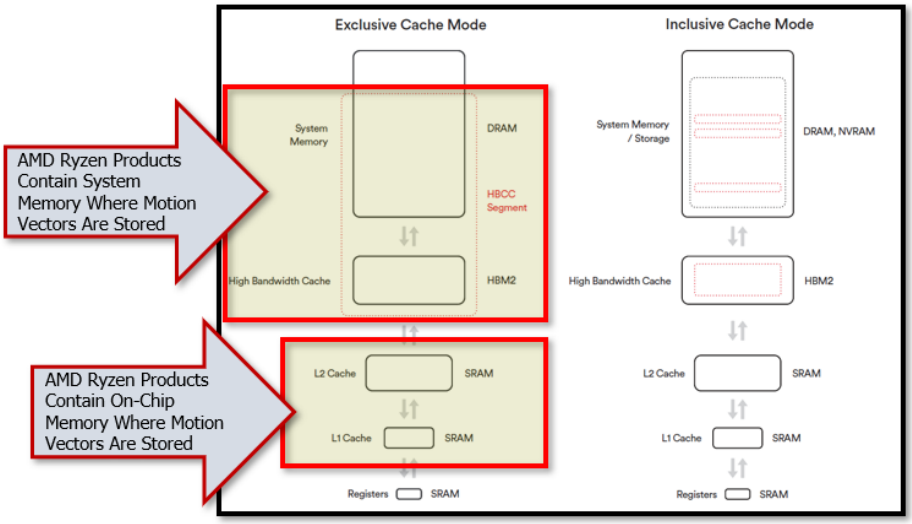
"Vega" Instruction Set Architecture, AMD REFERENCE GUIDE at 4 (July 28, 2017) (annotation added).

378. On information and belief, one or more of the AMD '689 Products include a processor where the Global Data Share contains a "Frame Buffer" for the storage of first and second images.



"Vega" Instruction Set Architecture, AMD REFERENCE GUIDE at 74 (July 28, 2017) (annotation added).

379. On information and belief, the AMD '689 Products contain a motion compensation unit designed to selectively receive further motion vector fields. As an illustrative example, the following excerpt from documentation regarding the High-Bandwidth Cache Controller in one or more of the AMD '689 Products shows that, through the use of the High-Bandwidth Cache Controller, data for video processing is retrieved from both external memory and the motion estimation unit.



Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER at 5 (2017) (annotations added) ("This capability is made possible by an addition to the memory controller logic called the High-Bandwidth Cache Controller (HBCC). It provides a set of features that allow remote memory to behave like local video memory and local video memory to behave like a last-level cache.")

380. On information and belief, the AMD '689 Products are available to businesses and individuals throughout the United States.

381. On information and belief, the AMD '689 Products are provided to businesses and individuals located in Delaware.

382. By making, using, testing, offering for sale, and/or selling products and services for encoding and decoding video data, including but not limited to the AMD '689 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '689 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

383. On information and belief, AMD also indirectly infringes the '689 Patent by actively inducing infringement under 35 USC § 271(b).

384. AMD has had knowledge of the '689 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '689 Patent and knew of its infringement, including by way of this lawsuit.

385. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '689 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '689 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '689 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '689 Products that have the capability of operating in a manner that infringe one or more of the claims of the '689 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '689 Products to utilize the products in a manner that directly infringe one or more claims of the '689 Patent.[29] By providing instruction and training to customers and end-users on how to use the AMD '689 Products in a manner that directly infringes one or more claims of the '689 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '689 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '689

[29] *See, e.g.*, RYZEN MASTER 1.4 – QUICK REFERENCE GUIDE (Aug. 2018); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *AMD Graphic Cores Next ("GCN") Architecture*, AMD WHITEPAPER (June 2012); *BKDG for AMD Family 15h Models 70h-7Fh Processors*, AMD DOCUMENT NO. 55072 REV. 3.09 (June 2018); *Radeon Instinct MI25*, AMD DATASHEET (2017); *Radeon Pro WX 8200*, AMD DATASHEET (2017).

Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '689 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '689 Patent, knowing that such use constitutes infringement of the '689 Patent.

386. The '689 Patent is well-known within the industry as demonstrated by multiple citations to the '689 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '689 Patent without paying a reasonable royalty. AMD is infringing the '689 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

387. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '689 Patent.

388. As a result of AMD's infringement of the '689 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT VIII
INFRINGEMENT OF U.S. PATENT NO. 6,996,177

389. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

390. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion estimation.

391. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '177 Product(s)").

392. Documentation from AMD shows that the AMD '177 Products perform a motion vector estimation method. AMD '177 Products perform the method of encoding video content using High Efficiency Video Coding ("HEVC").

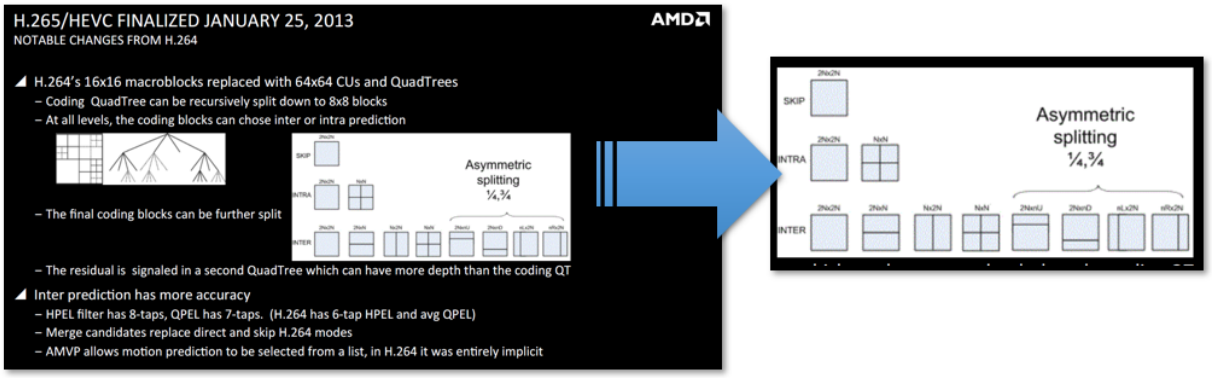
Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm

Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

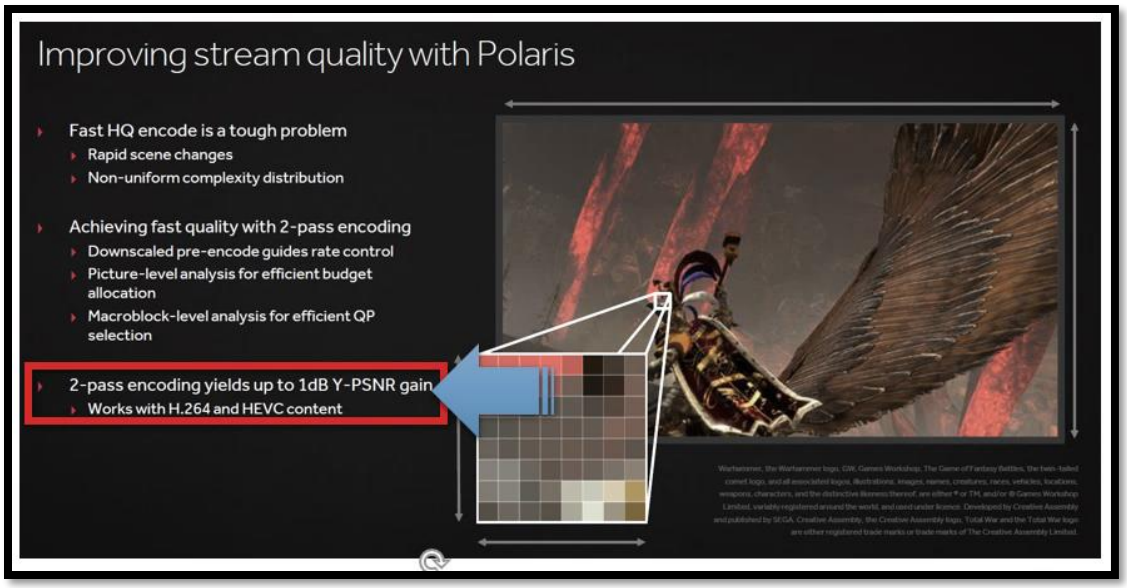
393. On information and belief, the AMD '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to the determine block-based motion vectors.

394. On information and belief, the AMD '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center. The following excerpt from an AMD presentation regarding the H.265 encoder states that during the encoding process, the AMD '177 Products perform "Asymmetric Splitting" in which "at all levels, the coding blocks can choose inter or intra prediction."

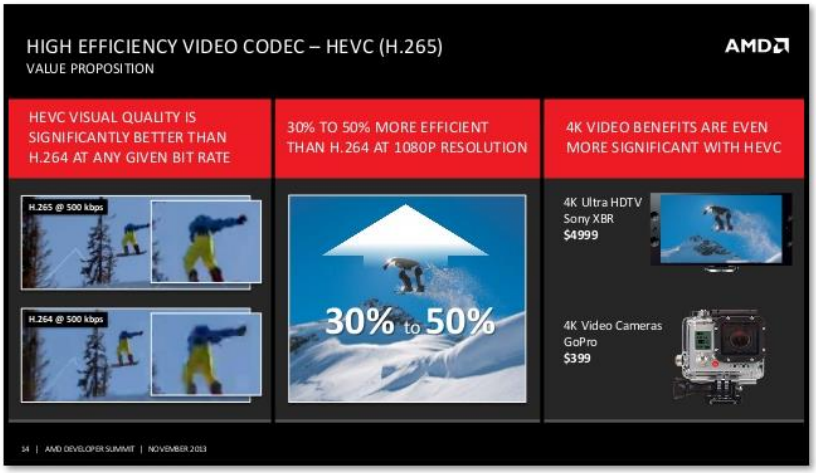


X265 Open Source H.265 Encoder: Optimization Details, AMD DEVELOPER SUMMIT PRESENTATION at 4 (November 19, 2013) (annotations added) (showing that the AMD Products use asymmetric splitting in the encoding process).

395. On information and belief, documentation from AMD provides additional evidence that the AMD '177 products contain H.265 encoding.



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 36 (2016) (annotation added) (stating "2-pass encoding yields up to 1db Y-PSNR gain . . . works with H.264 and HEVC content).



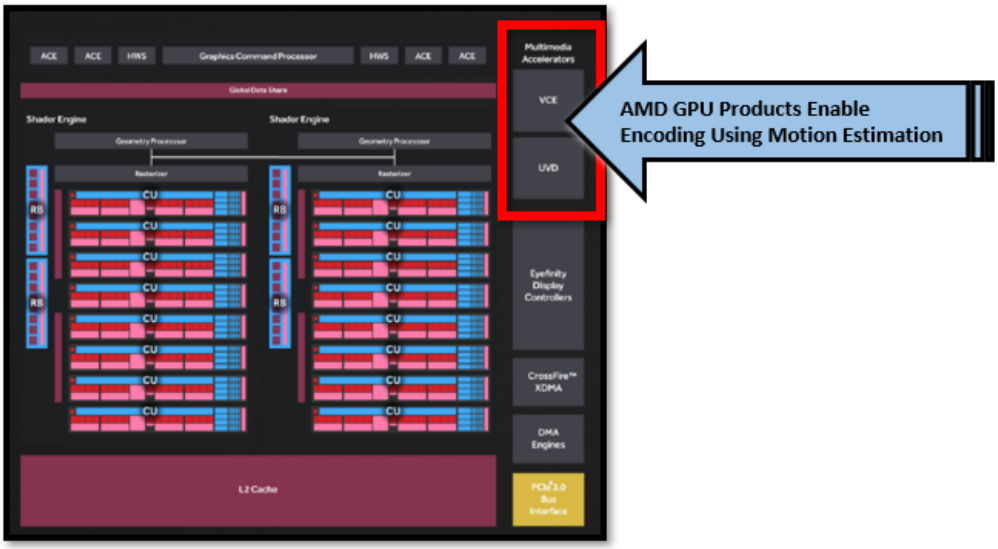
Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION at 14 (2013).

396. On information and belief, the following excerpt from a 2016 whitepaper from AMD describes the incorporation of H.265/HEVC encoding technologies into the AMD '177 Products.

> On the encode side, H.264 encode acceleration is carried forward from previous-generation products at 1080p120, 1440p60 or 2160p30 rates. AMD has worked with a variety of application vendors—including Plays.tv, AMD Gaming Evolved Powered by Raptr, and OBS Studio™—to expose this functionality. As streaming platforms and services transition over to HEVC/H.265 to improve quality and data rates, the Polaris architecture has also been updated to include H.265 encode acceleration at 1080p240, 1440p120 and 2160p60 rates.

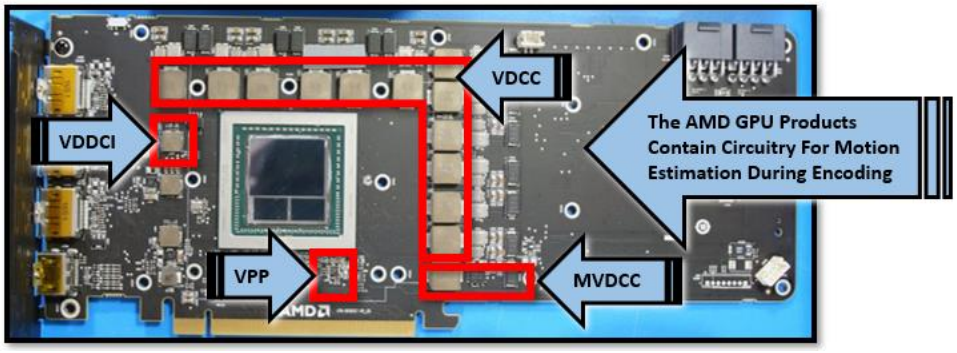
The Polaris Architecture, AMD WHITEPAPER at 18 (2016) ("As streaming platforms and services transition over to HEVC/H.265 to improve quality and data rates, the Polaris architecture has also been updated to include H.265 encode acceleration at 1080p240, 1440p120 and 2160p60 rates.").

397. On information and belief, the AMD '177 Products contain a video coding engine ("VCE") that functions to encode video using motion vectors. The following excerpt from a 2016 presentation regarding the AMD Polaris Architecture (the predecessor to AMD's "Vega" architecture) shows the utilization of VCE.



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 61 (2016) (annotations added).

398. On information and belief, analysis of the AMD '177 Product circuitry shows that the product contains circuitry for motion estimation during the encoding of video data using motion vectors.



AMD VEGA FRONTIER TEARDOWN (2018) (annotations added) (showing the circuitry of the AMD Vega Frontier 56 8GB board).

399. On information and belief, the AMD '177 Products use a Prediction Unit matching method wherein the motion vector represents the displacement between the current Prediction Unit in the current frame and the matching Prediction Unit in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

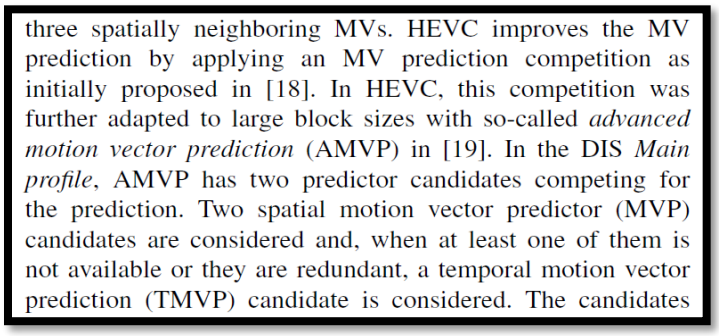
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

400. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '177 Products - necessarily infringe the '177 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '177 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to AMD's infringement of the '177 patent: "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

401. On information and belief, one or more of the AMD '177 Products include technology for motion estimation and motion-compensated picture signal processing.

402. On information and belief, one or more of the AMD '177 Products include technology for estimating a current motion vector for a group of pixels of an image.

403. On information and belief, the AMD '177 Products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The AMD '177 Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.



three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC*, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. *22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

404. On information and belief, the AMD '177 Products utilize a motion vector selection process wherein the candidate motion vectors are constructed into an index and then the motion vectors are compared. "In AMVP, the motion vector selection process is composed by two steps in encoder implementation. The first step is the motion vector candidate set construction process and the second step is the best motion vector selection step. In the first step, the motion vector candidate set is organized by selecting the motion vectors spatially and temporally." Gwo-Long

Li, Chuen-Ching Wang, and Kuang-Hung Chiang, *An Efficient Motion Vector Prediction Method for Avoiding AMVP Data Dependency For HEVC,* 2014 IEEE INTERNATIONAL CONFERENCE ON ACOUSTIC, SPEECH AND SIGNAL PROCESSING (ICASSP) at 13 (2014).

405. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '177 Products in regular business operations.

406. On information and belief, the AMD '177 Products are available to businesses and individuals throughout the United States.

407. On information and belief, the AMD '177 Products are provided to businesses and individuals located in the State of Delaware.

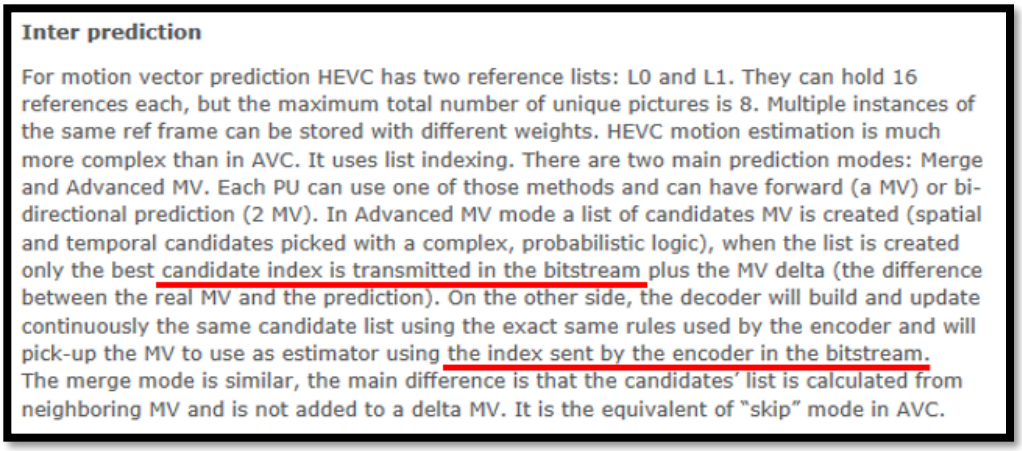
408. The HEVC Standard provides details regarding what would be required for a compliant HEVC encoder—e.g., the standard uses terms such as "encoding," "coding," "compressing," and other similar terms to describe the encoding process.

409. On information and belief, AMD has directly infringed and continues to directly infringe the '177 patent by, among other things, making, using, offering for sale, and/or selling products and services for motion estimation and motion-compensated picture signal processing.

410. On information and belief, the AMD '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to determine block-based motion vectors. The AMD '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image.

411. On information and belief, the AMD '177 Products determine at least a most frequently occurring block-based motion vector. The AMD '177 Products contain functionality wherein the motion vector prediction performed includes the ability to transmit in the bitstream the candidate index of motion vectors. Documentation of the encoding process states that the

encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

412. On information and belief, any implementation of the HEVC standard would infringe the '177 patent as every possible implementation of the standard requires: compliant devices to carry out a global motion vector estimation process using the most frequently occurring block-based motion vectors. This process of vector candidate selection allows the AMD '177 Products to obtain a global motion vector. Specifically, the HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, if there are two spatial motion vectors that are identical, that is determined to be the most frequently occurring block-based motion vector and the frequently occurring spatial motion vector and temporal motion vector candidate are used to generate the global motion vector. "In HEVC, this competition was further adapted to large block sizes with so-called advanced motion vector prediction (AMVP). In the DIS Main profile, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion

vector prediction (TMVP) candidate is considered." Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 (December 2012).

413. On information and belief, the AMD '177 Products apply a global motion vector as a candidate vector to the block-based motion vector estimation process. Specially, the AMD '177 Products calculate the global motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process diagram below (as shown in the below figure) and applied to the block-based motion vector estimation process.

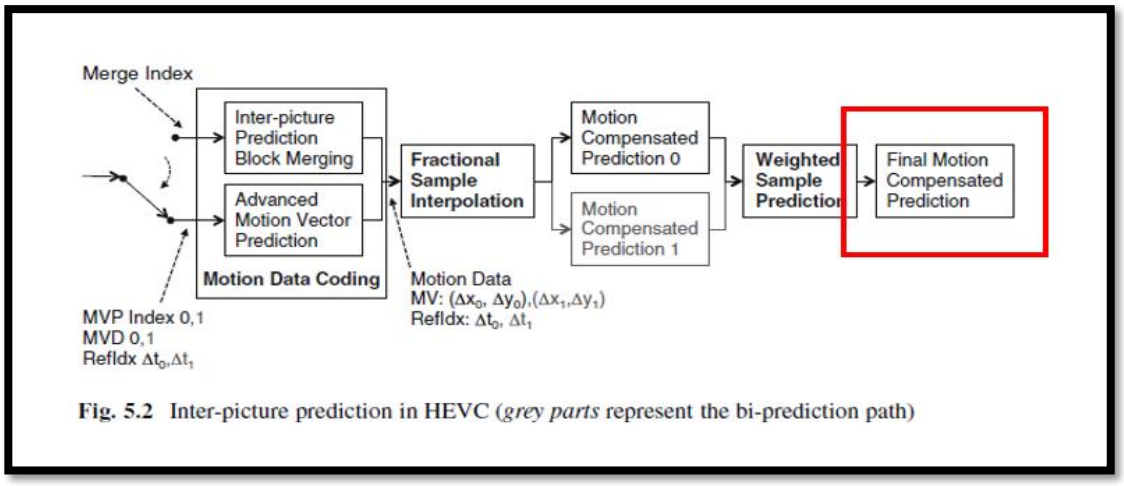


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

414. Further, the AMD '177 Products enable AMVP wherein several of the most probable candidate vectors based on data from adjacent prediction blocks are used to create a global estimation vector and that vector is applied to the block-based motion estimation functionality.

> Motion vector signaling: Advanced motion vector prediction (AMVP) is used, including derivation of several most probable candidates based on data from adjacent PBs and the reference picture. A "merge" mode for MV coding can be

> also used, allowing the inheritance of MVs from neighboring PBs. Moreover, compared to H.264/MPEG-4 AVC, improved "skipped" and "direct" motion inference are also specified.

Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, PRE-PUBLICATION DRAFT, TO APPEAR IN IEEE TRANS. ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY at 3 (December 2012) (emphasis added).

415. On information and belief, the AMD '177 Products are available to businesses and individuals throughout the United States.

416. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '177 Products in regular business operations.

417. On information and belief, AMD has directly infringed and continues to directly infringe the '177 Patent by, among other things, making, using, offering for sale, and/or selling technology for determining motion vectors that are each assigned to individual image regions, including but not limited to the AMD '177 Products.

418. On information and belief, the AMD '177 Products are provided to businesses and individuals located in Delaware.

419. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the AMD '177 Products, AMD has injured Dynamic Data and is liable for directly infringing one or more claims of the '177 Patent, including at least claim 1, pursuant to 35 U.S.C. § 271(a).

420. On information and belief, AMD also indirectly infringes the '177 Patent by actively inducing infringement under 35 USC § 271(b).

421. On information and belief, AMD has had knowledge of the '177 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '177 Patent and knew of its infringement, including by way of this lawsuit.

422. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '177 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '177 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '177 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '177 Products that have the capability of operating in a manner that infringe one or more of the claims of the '177 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '177 Products to utilize the products in a manner that directly infringe one or more claims of the '177 Patent.[30] By providing instruction and training to customers and end-users on how to use the AMD '177 Products in a manner that directly infringes one or more claims of the '177 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '177 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '177 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '177 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the

[30] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

accused products in their ordinary and customary way to infringe the '177 Patent, knowing that such use constitutes infringement of the '177 Patent.

423. The '177 Patent is well-known within the industry as demonstrated by multiple citations to the '177 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '177 Patent without paying a reasonable royalty. AMD is infringing the '177 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

424. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '177 Patent.

425. As a result of AMD's infringement of the '177 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT IX
INFRINGEMENT OF U.S. PATENT NO. 7,010,039

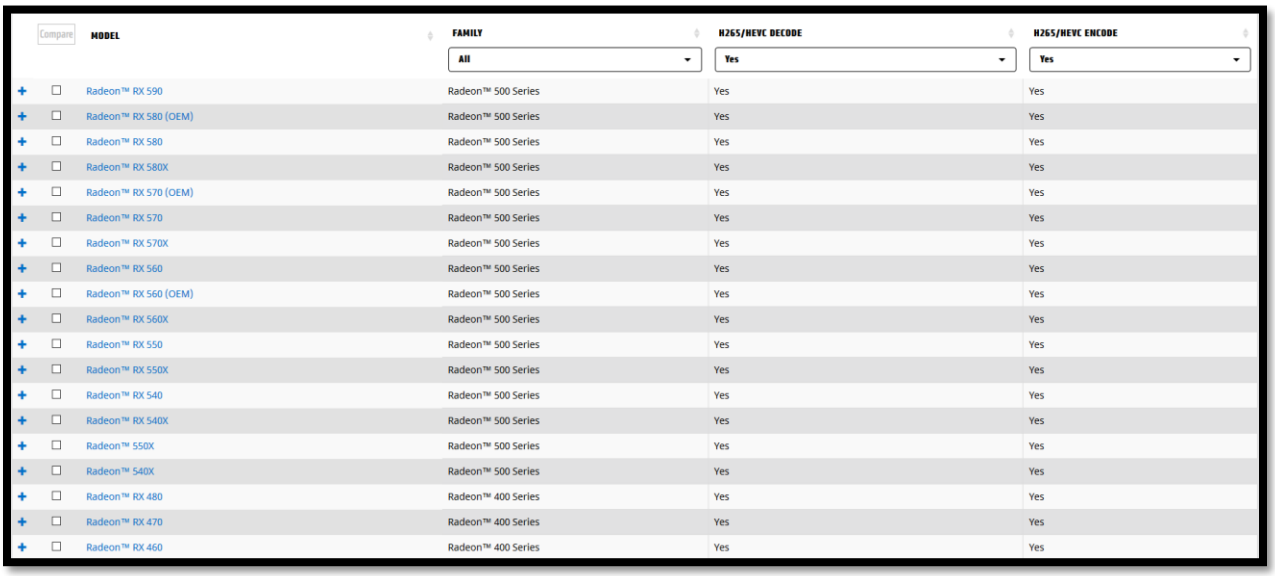
426. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

427. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for detecting motion.

428. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580,

Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '039 Product(s)").

429. On information and belief, the AMD '039 Products comply with the HEVC standard for video processing.



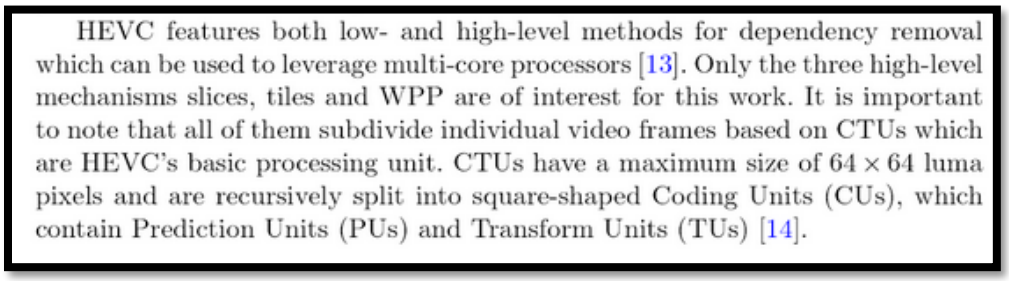
Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

430. On information and belief, the AMD '039 Products contain functionality wherein a criterion function for candidate vectors is optimized. The criterion function depends on data obtained from the previous and next images in the video data stream. The optimizing is carried out at a temporal intermediate position in non-covered and covered areas. The following excerpts explain how HEVC is a form of encoding video information using a temporal intermediate position between previous and next images.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess. Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC), UPTEC STS 16006 at 4 (March 2016)



HEVC features both low- and high-level methods for dependency removal which can be used to leverage multi-core processors [13]. Only the three high-level mechanisms slices, tiles and WPP are of interest for this work. It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC's basic processing unit. CTUs have a maximum size of 64×64 luma pixels and are recursively split into square-shaped Coding Units (CUs), which contain Prediction Units (PUs) and Transform Units (TUs) [14].

Stefan Radicke, *et al*., *Many-Core HEVC Encoding Based on Wavefront Parallel Processing and GPU -accelerated Motion Estimation*, E-BUSINESS AND TELECOMMUNICATIONS: 11TH INTERNATIONAL JOINT CONFERENCE at 296 (2015) ("HEVC feature both low- and high-level methods for dependency removal which can be used to leverage multi-core processors. . . It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC' basic processing unit.").

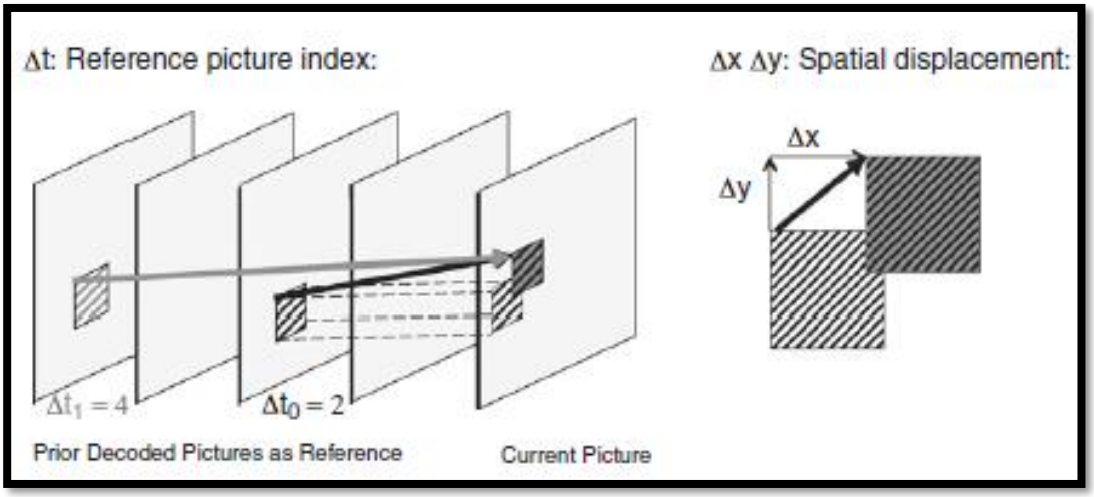
431. On information and belief, the AMD '039 Products receive encoded video data that is encoded using inter-frame coding. The encoded video stream received by the AMD Products are coded using its predecessor frame and subsequent frame. Inter-prediction used in the encoded video data received by the AMD Products allows a transform block to span across multiple

prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit ***temporal statistical dependences,*** intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

432. The encoded video stream received by the AMD Products are encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



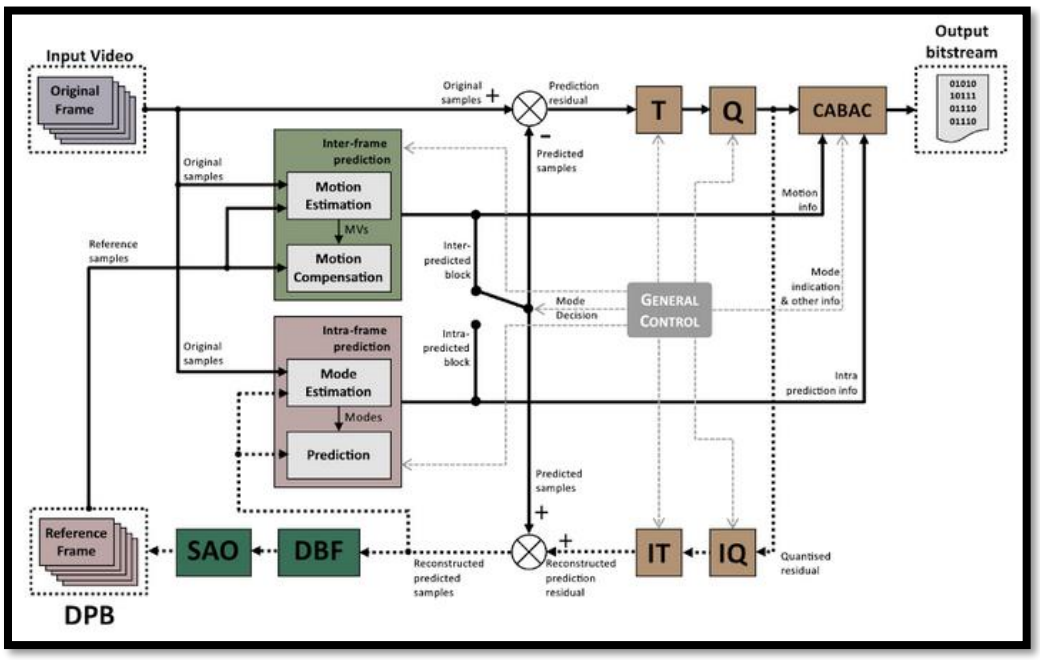
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

433. On information and belief, the following excerpt from an article describing the architecture of the encoded video stream received by the AMD '39 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . or two reference frames (bi-prediction) to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

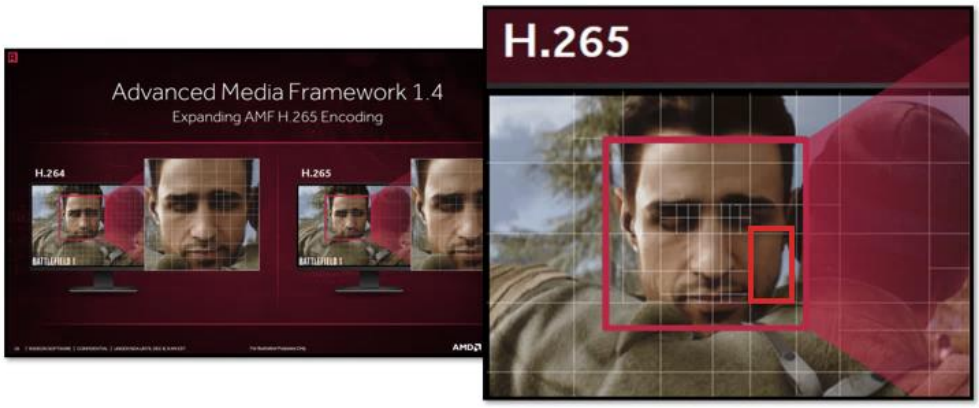
434. On information and belief, the following diagram shows how the AMD '039 Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across frames.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

435. On information and belief, the AMD ‘039 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the AMD Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

436. The AMD ’39 Products optimize the selection of candidate vectors by calculation a temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas. Specifically, the encoding process for video data received by the AMD Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.



RADEON SOFTWARE PRESENTATION at 16 (2017) (showing that the encoding functionality allows offset from a center position).

437. On information and belief, the "Overview of Design Characteristics" in the HEVC specification describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."

> compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 0.7 (April 2015) (annotation added).

438. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '039 Products - necessarily infringe the '039 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '039 patent, including but not limited to claim 13. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to AMD's infringement of the '039 patent: "5.3 Logical operators;" "5.10 Variables, syntax

elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

439. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '039 Products in regular business operations.

440. On information and belief, the AMD '039 Products are available to businesses and individuals throughout the United States.

441. On information and belief, the AMD '039 Products are provided to businesses and individuals located in Delaware.

442. On information and belief, AMD has directly infringed and continues to directly infringe the '039 Patent by, among other things, making, using, offering for sale, and/or selling technology for detecting motion, including but not limited to the AMD '039 Products.

443. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the AMD '039 Products, AMD has injured Dynamic Data and is liable for directly infringing one or more claims of the '039 Patent, including at least claim 13, pursuant to 35 U.S.C. § 271(a).

444. On information and belief, AMD also indirectly infringes the '039 Patent by actively inducing infringement under 35 USC § 271(b).

445. On information and belief, AMD has had knowledge of the '039 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and

belief, AMD knew of the '039 Patent and knew of its infringement, including by way of this lawsuit.

446. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '039 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '039 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '039 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '039 Products that have the capability of operating in a manner that infringe one or more of the claims of the '039 Patent, including at least claim 13, and AMD further provides documentation and training materials that cause customers and end users of the AMD '039 Products to utilize the products in a manner that directly infringe one or more claims of the '039 Patent.[31] By providing instruction and training to customers and end-users on how to use the AMD '039 Products in a manner that directly infringes one or more claims of the '039 Patent, including at least claim 13, AMD specifically intended to induce infringement of the '039 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '039 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '039 Patent.

[31] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '039 Patent, knowing that such use constitutes infringement of the '039 Patent.

447. The '039 Patent is well-known within the industry as demonstrated by multiple citations to the '039 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '039 Patent without paying a reasonable royalty. AMD is infringing the '039 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

448. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '039 Patent.

449. As a result of AMD's infringement of the '039 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT X
INFRINGEMENT OF U.S. PATENT NO. 8,311,112

450. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

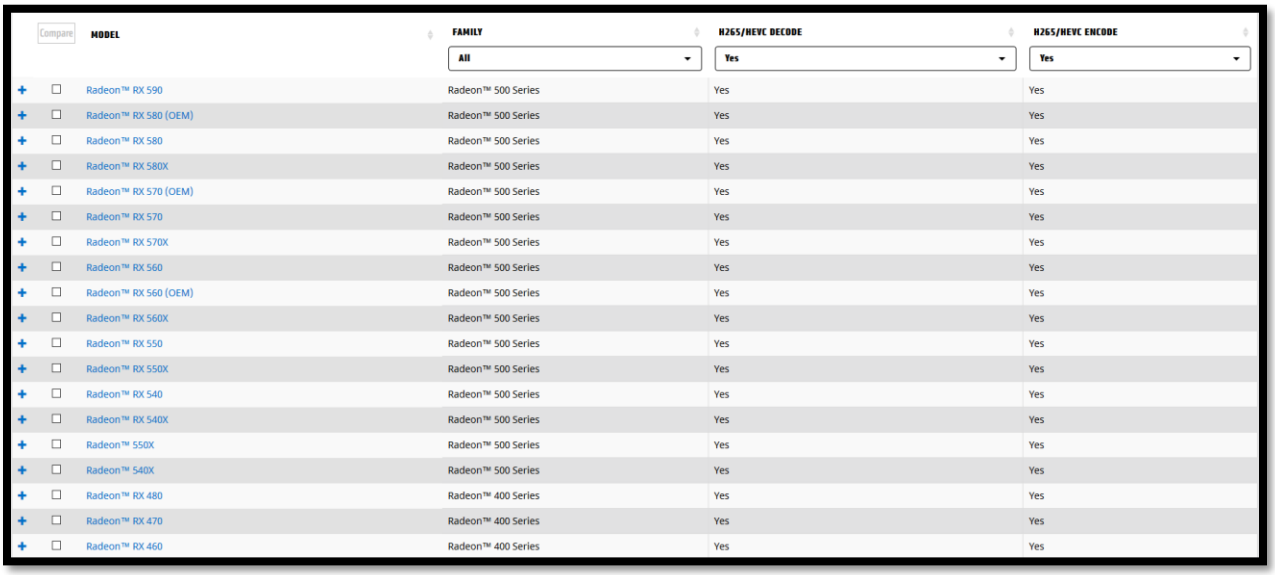
451. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for video compression.

452. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 580, Radeon RX 580X,

Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '112 Product(s)").

453. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '112 Products in regular business operations.

454. The AMD '112 Products perform HEVC encoding for video compression in compliance with the HEVC standard.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

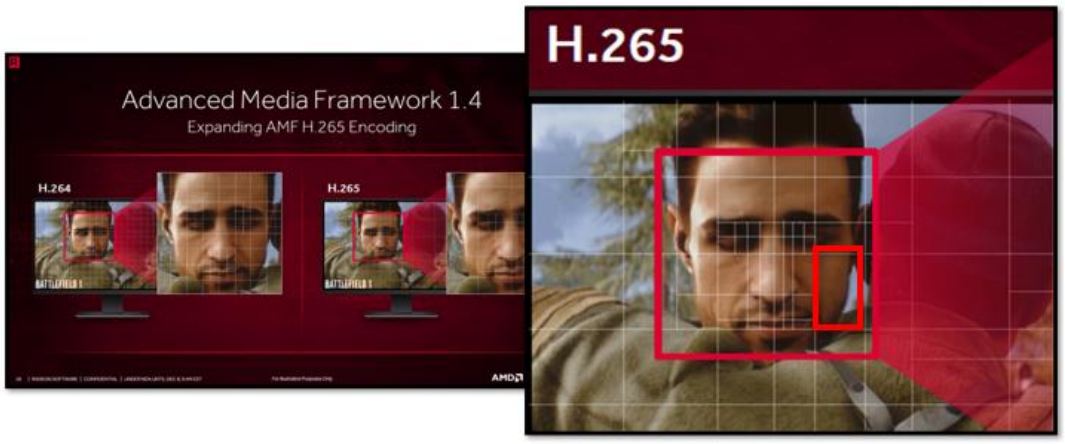
AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"*

AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

455. On information and belief, the AMD '112 Products select the selected image selection area based on a range of possible motion vectors in the selected image search area. Further, the search area of the selected image segment has a center. Specifically, the AMD '112 Products contain functionality for selecting a coding unit. The coding unit comprises a selected image segment. The below presentation shows that the AMD '112 Products select a content unit (e.g., selected image segment).

X265 Open Source H.265 Encoder: Optimization Details, AMD DEVELOPER SUMMIT PRESENTATION at 7 (November 19, 2013).

456. On information and belief, the H.265/HEVC encoding performed by the AMD '112 Products enables the selection of an image segment of a given image corresponding to an image segment of a first video image. The selected image segment has a center and a search area is defined around the image segment. The below excerpt from a 2017 AMD presentation relating to the AMD '112 Products shows how the H.265 encoding process enables the selection of an image center that is an offset of an image center.

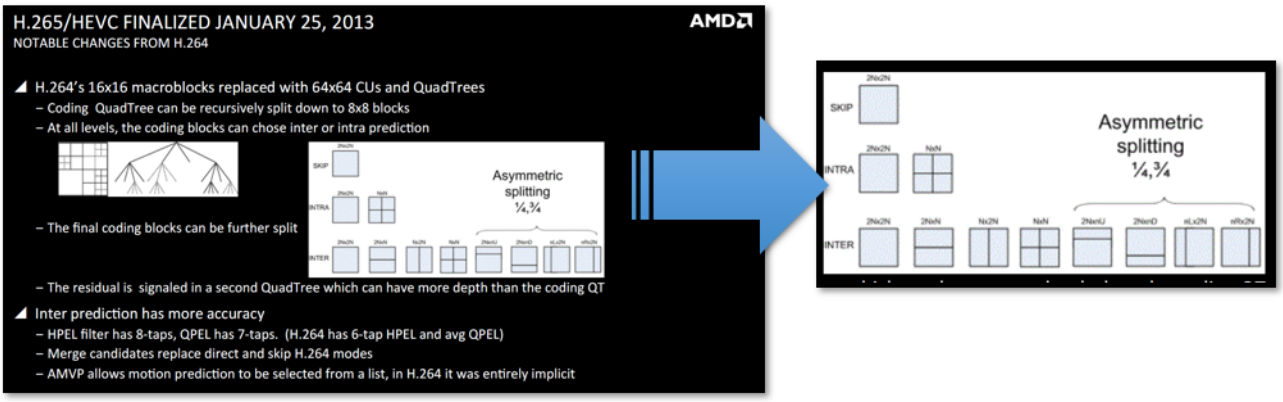


RADEON SOFTWARE PRESENTATION at 16 (2017) (showing that the encoding functionality allows offset from a center position).

457. The AMD '112 Products contain an image processing unit that receives, at a minimum, two frames of a video from memory. These frames are then processed by the video compensation unit of the AMD Products. Further, the AMD Products contain an encoder for motion estimation. "[***T]he encoder needs to perform motion estimation***, which is one of the most computationally expensive operations in the encoder, and complexity is reduced by allowing less candidates."[32]

458. The below image identifies an exemplar of the image processing component in the AMD '112 Products.

[32] Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, PRE-PUBLICATION DRAFT, TO APPEAR IN IEEE TRANS. ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY at 13 (December 2012) (emphasis added).



X265 Open Source H.265 Encoder: Optimization Details, AMD DEVELOPER SUMMIT PRESENTATION at 4 (November 19, 2013) (annotations added) (showing that the AMD Products use coding tree units and prediction locks to encode motion vectors.

459. The AMD '112 Products perform encoding using motion compensation, specifically, inter-picture prediction wherein the AMD Product makes use of the temporal correlation between pictures in order to derive a motion-compensated prediction for a block of image samples. Each image is divided into blocks (prediction units) and the AMD '112 Product compares the prediction unit in a first image with the spatially neighboring prediction units in a second image (reference image). The displacement between the current prediction unit and the matching prediction unit in the second image (reference image) is signaled using a motion vector.

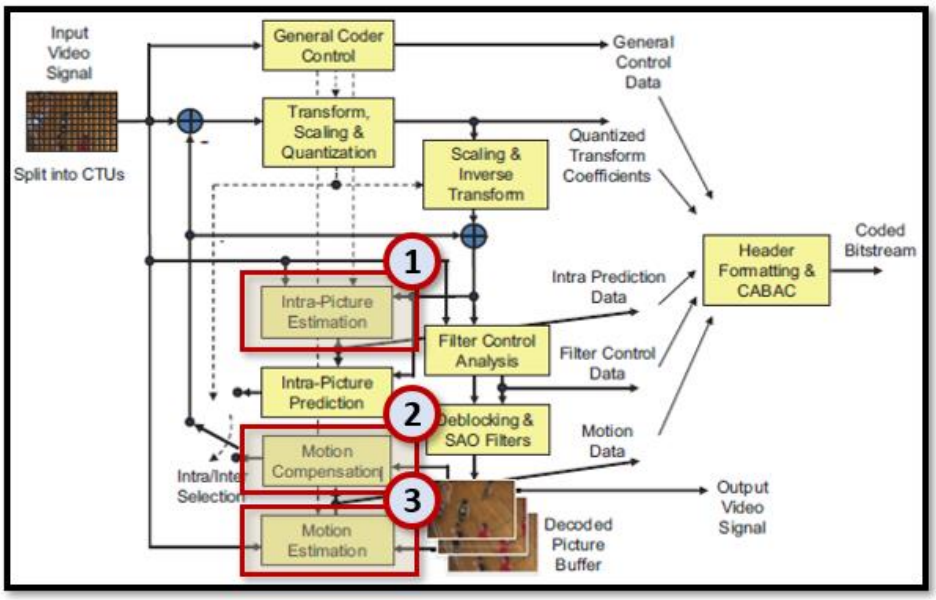
460. The AMD '112 Products contain functionality wherein during the motion estimation process the block size used for prediction units can range from 4 × 8/8 × 4 to 64 × 64.

> A block-wise prediction residual is computed from corresponding regions of previously decoded pictures (inter-picture motion compensated prediction) or neighboring previously decoded samples from the same picture (intra-picture spatial prediction). The residual is then processed by a block transform, and the transform coefficients are quantized and entropy coded. Side information data such as motion vectors and mode switching parameters are also encoded and transmitted.

Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, Vol. 7, No. 6 at 1002 (December 2013) (emphasis added).

461. The AMD '112 Products use intra-picture estimation between blocks (prediction units) within an image retrieved from memory. The frames are then processed using both motion compensation and motion estimation. The motion compensation functionality used by the AMD

Products include quarter-sample precision for the motion vectors and 7-tap or 8-tap filters that are used for interpolation of fractional-sample positions.



Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, VOL. 7, NO. 6 at 1002 (December 2013) (emphasis added) (the annotations showing (1) intra-picture prediction, (2) motion compensation, and (3) motion estimation).

462. The AMD '112 Products contain functionality for motion compensation where two or more motion vectors can be applied. Further, one or two motion vectors can be applied to the image processing process. The application of the motion vectors leads to uni-predictive or bi-predictive coding, respectively, where bi-predictive coding uses an averaged result of two predictions to form the final prediction.

Summary

Recommendation ITU-T H.265 | International Standard ISO/IEC 23008-2 represents an evolution of the existing video coding Recommendations (ITU-T H.261, ITU-T H.262, ITU-T H.263 and ITU-T H.264) and was developed in response to the growing need for higher compression of moving pictures for various applications such as Internet streaming, communication, videoconferencing, digital storage media and television broadcasting. It is also designed to enable the use of the coded video representation in a flexible manner for a wide variety of network environments. The use of this Recommendation | International Standard allows motion video to be manipulated as a form of computer data and to be stored on various storage media, transmitted and received over existing and future networks and distributed on existing and future broadcasting channels.

Series H: Audiovisual and Multimedia Systems- Infrastructure of Audiovisual Services – Coding of Moving Video, INTERNATIONAL TELECOMMUNICATIONS UNIONS - TU-T H.265, V.5 at I (February 2018).

463. AMD has directly infringed and continues to directly infringe the '112 Patent by, among other things, making, using, offering for sale, and/or selling technology for video compression, including but not limited to the AMD '112 Products.

464. The AMD '112 Products comprise a system wherein an intra-frame coding unit is configured to perform predictive coding on a set of pixels of a macroblock of pixels. Further, the predictive coding functionality uses a first group of reference pixels and a macroblock of pixels from the video frame. Specifically, the AMD Products, when selecting a temporal candidate for HEVC intra-frame encoding, default to the right bottom position just outside of the collocated prediction unit.

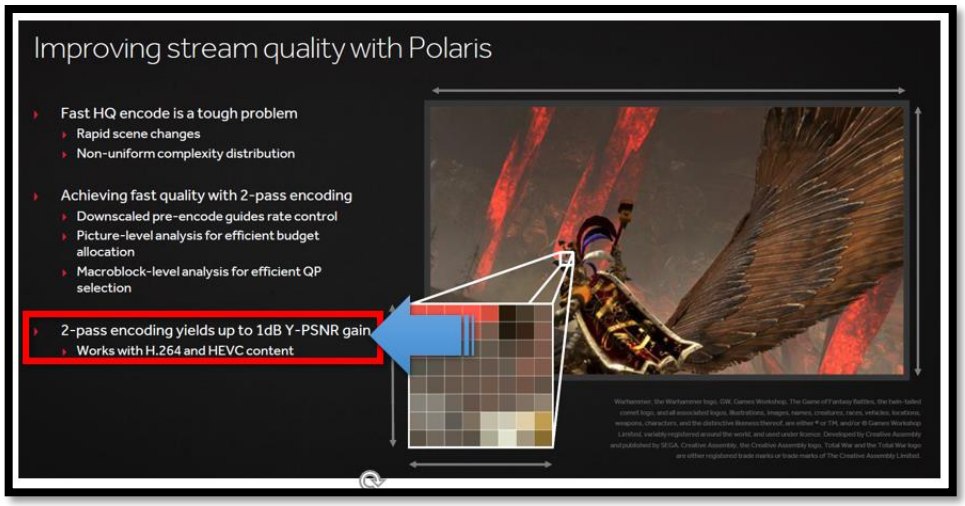
> It can be seen from Fig. 5.4b that only motion vectors from spatial neighboring blocks to the left and above the current block are considered as spatial MVP candidates. This can be explained by the fact that the blocks to the right and below the current block are not yet decoded and hence, their motion data is not available. Since the co-located picture is a reference picture which is already decoded, it is possible to also consider motion data from the block at the same position, from blocks to the right of the co-located block or from the blocks below**. *In HEVC, the block to the bottom right and at the center of the current block have been determined to be the most suitable to provide a good temporal motion vector predictor (TMVP).***

Benjamin Bross, *et al., Inter-picture prediction in HEVC*, in HIGH EFFICIENCY VIDEO CODING (HEVC) at 119 (2014) (emphasis added);

465. Descriptions of the HEVC encoding process, which are implemented by the AMD '112 Products, state "for the temporal candidate, the right bottom position just outside of the

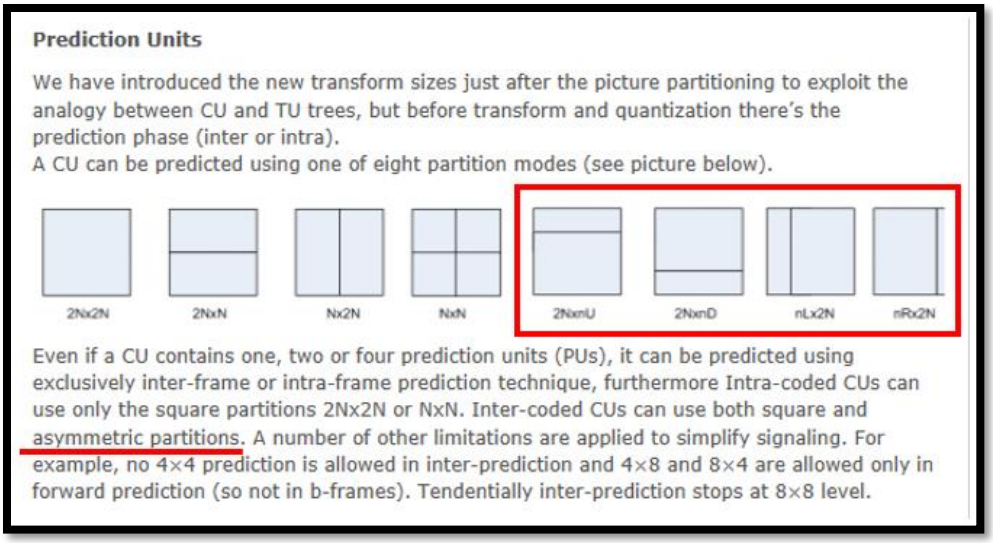
collocated PU of the reference picture is used if it is available. Otherwise, the center position is used instead." Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, IEEE TRANS. ON CIRCUIT AND SYSTEMS FOR VIDEO TECHNOLOGY at 13 (December 2012).

466. The AMD video encoder in the AMD '112 Products selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment further has an image segment center.



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 36 (2016) (annotation added) (stating "2-pass encoding yields up to 1db Y-PSNR gain . . . works with H.264 and HEVC content).

467. The AMD '112 Products encode video data such that a predetermined search area (S) center is offset from the center of the image segment. The predetermined search area is called a partition and there are eight different partition modes in the H.265 standard, these partition modes are shown in the figure below. The last four partition modes are asymmetric, meaning their center is offset from the overall CU center.



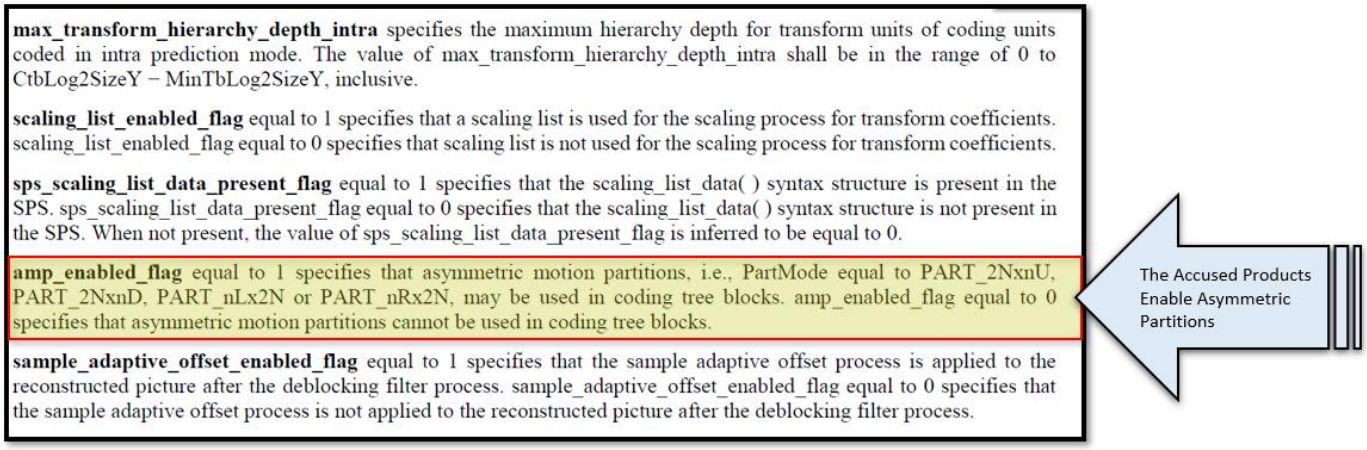
Prediction Units

We have introduced the new transform sizes just after the picture partitioning to exploit the analogy between CU and TU trees, but before transform and quantization there's the prediction phase (inter or intra).
A CU can be predicted using one of eight partition modes (see picture below).

Even if a CU contains one, two or four prediction units (PUs), it can be predicted using exclusively inter-frame or intra-frame prediction technique, furthermore Intra-coded CUs can use only the square partitions 2Nx2N or NxN. Inter-coded CUs can use both square and asymmetric partitions. A number of other limitations are applied to simplify signaling. For example, no 4×4 prediction is allowed in inter-prediction and 4×8 and 8×4 are allowed only in forward prediction (so not in b-frames). Tendentially inter-prediction stops at 8×8 level.

Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

468. The figure below shows the syntax as well as the instructions for enabling the asymmetric partitions within the H.265 standard which is used by the AMD '112 Products.



max_transform_hierarchy_depth_intra specifies the maximum hierarchy depth for transform units of coding units coded in intra prediction mode. The value of max_transform_hierarchy_depth_intra shall be in the range of 0 to CtbLog2SizeY − MinTbLog2SizeY, inclusive.

scaling_list_enabled_flag equal to 1 specifies that a scaling list is used for the scaling process for transform coefficients. scaling_list_enabled_flag equal to 0 specifies that scaling list is not used for the scaling process for transform coefficients.

sps_scaling_list_data_present_flag equal to 1 specifies that the scaling_list_data( ) syntax structure is present in the SPS. sps_scaling_list_data_present_flag equal to 0 specifies that the scaling_list_data( ) syntax structure is not present in the SPS. When not present, the value of sps_scaling_list_data_present_flag is inferred to be equal to 0.

amp_enabled_flag equal to 1 specifies that asymmetric motion partitions, i.e., PartMode equal to PART_2NxnU, PART_2NxnD, PART_nLx2N or PART_nRx2N, may be used in coding tree blocks. amp_enabled_flag equal to 0 specifies that asymmetric motion partitions cannot be used in coding tree blocks.

sample_adaptive_offset_enabled_flag equal to 1 specifies that the sample adaptive offset process is applied to the reconstructed picture after the deblocking filter process. sample_adaptive_offset_enabled_flag equal to 0 specifies that the sample adaptive offset process is not applied to the reconstructed picture after the deblocking filter process.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at 76 (April 2015) (annotation added).

469. The AMD '112 Products receive encoded video data that is encoded using intra-frame coding. Specifically, the encoded video stream received by the AMD '112 Products is coded using a reference group of pixels in the video frame. Intra-frame prediction used in the encoded video data received by the AMD '112 Products allows a transform block to span across multiple

prediction blocks for intra-frame-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit ***temporal statistical dependences,*** intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

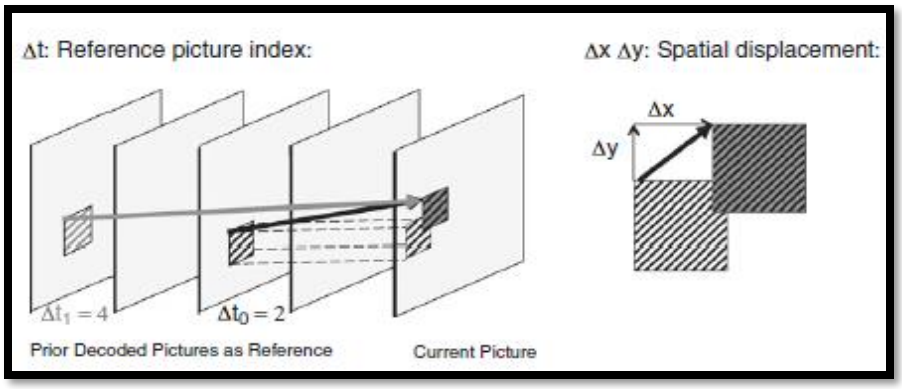
470. The AMD '112 Products comprise functionality for retrieving image motion data related to the search area. Specifically, the AMD '112 Products retrieve data relating to the motion search area. The data, which includes the motion vector index, is sent from the encoder and retrieved by the decoder.

> Since inter-picture prediction typically compensates for the motion of real-world objects between pictures of a video sequence, it is also referred to as motion-compensated prediction. While intra-picture prediction exploits the spatial redundancy between neighboring blocks inside a picture, motion-compensated prediction utilizes the large amount of temporal redundancy between pictures. In either case, the resulting prediction error, which is formed by taking the difference between the original block and its prediction, ***is transmitted using transform coding, which exploits the spatial redundancy inside a block and consists of a decorrelating linear transform, scalar quantization*** of the transform coefficients and entropy coding of the resulting transform coefficient levels.

Heiko Schwarz, Thomas Schierl, Detlev Marpe, *Block Structures and Parallelism Features in HEVC*, in HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 49 (September 2014) (emphasis added).

471. AMD '112 Products comprise an inter-frame coding unit that is configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels. The second group of reference pixels that are used to perform inter-frame coding are drawn from at least one other video frame. The image data processed by the AMD '112 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, an image is divided into rectangular blocks. Assuming

homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor (a second image). Both the first and second images are retrieved by the AMD '112 Product from storage such as on chip memory. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

472. On information and belief, the AMD '112 Products are available to businesses and individuals throughout the United States.

473. On information and belief, the AMD '112 Products are provided to businesses and individuals located in Delaware.

474. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '112 Products - necessarily infringe the '112 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '112 patent, including but not limited to claim 11 of the '112 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to AMD's infringement of the '112 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in

inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

475. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the AMD '112 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '112 Patent, including at least claim 11 pursuant to 35 U.S.C. § 271(a).

476. On information and belief, AMD also indirectly infringes the '112 Patent by actively inducing infringement under 35 USC § 271(b).

477. AMD has had knowledge of the '112 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '112 Patent and knew of its infringement, including by way of this lawsuit.

478. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '112 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '112 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '112 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '112 Products that have the capability of operating in a manner that infringe one or more of the claims of the '112 Patent, including at least claim 11, and AMD further provides documentation and training materials that cause customers and end users of the AMD '112

Products to utilize the products in a manner that directly infringe one or more claims of the '112 Patent.[33] By providing instruction and training to customers and end-users on how to use the AMD '112 Products in a manner that directly infringes one or more claims of the '112 Patent, including at least claim 11, AMD specifically intended to induce infringement of the '112 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '112 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '112 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '112 Patent, knowing that such use constitutes infringement of the '112 Patent.

479. The '112 Patent is well-known within the industry as demonstrated by multiple citations to the '112 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '112 Patent without paying a reasonable royalty. AMD is infringing the '112 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

480. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '112 Patent.

[33] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

481. As a result of AMD's infringement of the '112 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

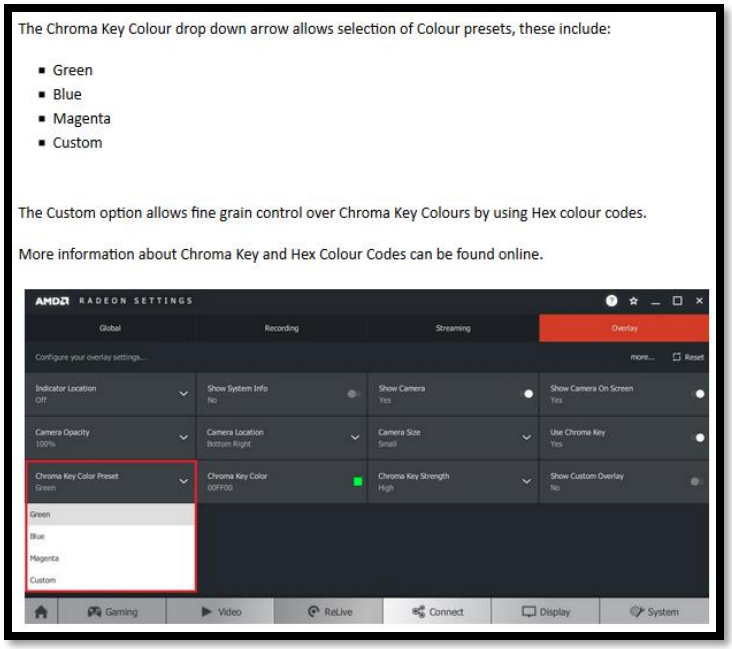
COUNT XI
INFRINGEMENT OF U.S. PATENT NO. 6,646,688

482. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

483. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for processing video and graphics data.

484. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Graphics Core Next (GCN) Architecture-based Desktop Graphics products supporting Radeon ReLive, including the following models: Radeon RX Vega Series, Radeon RX 500 Series, Radeon RX 400 Series, Radeon Pro Duo, AMD Radeon R9 Fury, R9 300, R7 300 Series, AMD Radeon R9 200, R7 200, R5 300, R5 240 Series, AMD Radeon HD 8500 – HD 8900 Series, and AMD Radeon HD 7700 – HD 7900 Series (collectively, the "AMD '688 Product(s)").

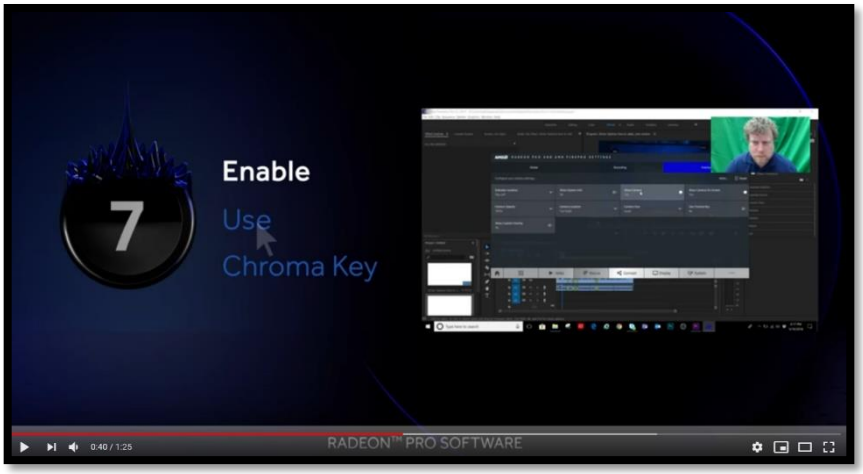
485. The AMD Products comprise a video/graphics data processing method that enables the processing of an image using a color key (aka chroma key). The following excerpt from AMD documentation describes that the Chroma Key "provides background transparency when using a web camera for streaming content. Chroma Key can be fine-tuned with colour removal strength pre-sets and custom colours." *How to Capture Your Gameplay Using Radeon ReLive,* AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018).



How to Capture Your Gameplay Using Radeon ReLive, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018).

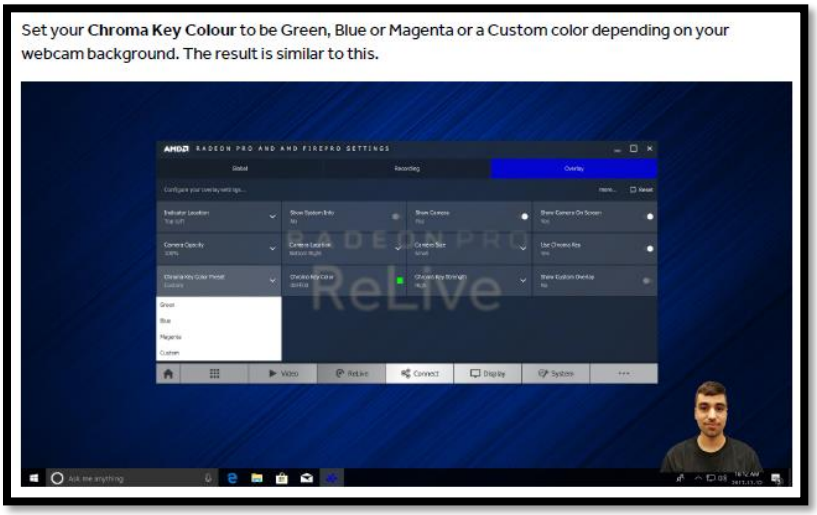
486. The AMD '688 Products comprise a system for pre-processing a stream of digital video/graphics data to output pre-processed data. Specifically, the AMD '688 Products are described in the below excerpt from AMD documentation as enabling "Capturing gameplay using Radeon ReLive is easy to configure and has a minimal impact on performance, which is measured in frames per second (FPS)." *How to Capture Your Gameplay Using Radeon ReLive*, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018).

487. The AMD '688 Products enable the processing of a stream of digital video data wherein a Chroma Key is used to output pre-processed data. The below excerpt from a 2018 AMD presentation describes how the chroma key is applied to a pre-processed stream of digital video that is captured using a web camera.



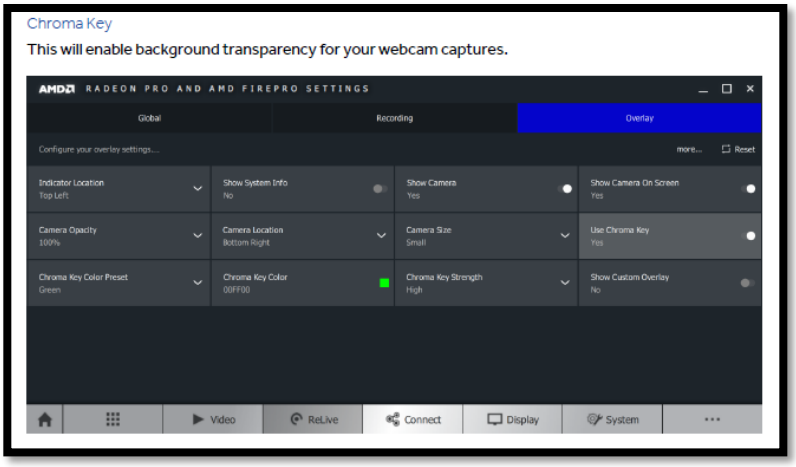
Radeon Pro ReLive: How to Set up & Use Chroma Key, AMD YOUTUBE.COM VIDEO (July 3, 2018). available at: https://www.youtube.com/watch?v=-j7KopH1pFo

488. The AMD '688 Products comprise a system wherein the chroma key is applied in the processing of video data as described in the below excerpt from AMD's documentation. In the below example a Chroma Key Colour that can be Green, Blue Magenta or a Custom color is applied to a webcam background that comprises a video data stream.



Radeon Pro ReLive in AMD Radeon Pro Settings, AMD USER GUIDE at 17 (2018).

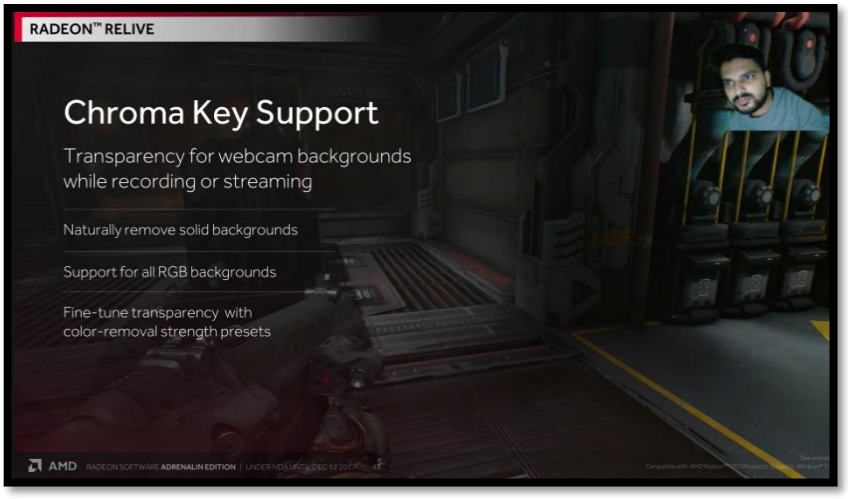
489. The below excerpt from AMD's documentation shows how a chroma key is enabled in the AMD '688 Products and by setting it to a specific color will output resulting data (*e.g.*, transparent backgrounds in a webcam data stream).



Radeon Pro ReLive in AMD Radeon Pro Settings, AMD USER GUIDE at 17 (2018).

490. The AMD '688 Products comprise a system wherein the data is transformed by substituting the color key with a preselected color. Specifically, Chroma Key can be preset to four different colors which are then used to substitute the color key with a preselected color.

491. The following excerpt from an AMD presentation relating to the AMD '688 Products describes how the AMD '688 Products include functionality with Chroma Key Support that enables "transparency for webcam backgrounds wile recording or streaming," "naturally remove solid backgrounds," "support for all RGB backgrounds," and "Fine-tune transparency with color-removal strength presets."



Nate Oh, *AMD Releases Radeon Software Adrenalin Edition: Overlay, App & More for 2017*, ANANDTECH WEBSITE (December 12, 2017), available at: https://www.anandtech.com/show/12147/amd-releases-radeon-software-adrenalin-edition/4 (excerpting AMD's presentation regarding the Radeon ReLive product).

492. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '688 Products in regular business operations.

493. On information and belief, the AMD '688 Products are available to businesses and individuals throughout the United States.

494. On information and belief, the AMD '688 Products are provided to businesses and individuals located in Delaware.

495. On information and belief, AMD has directly infringed and continues to directly infringe the '688 Patent by, among other things, making, using, offering for sale, and/or selling technology for processing video and/or graphics data, including but not limited to the AMD '688 Products.

496. On information and belief, the AMD '688 Products process a color key from the pre-processed data to output resulting data.

497. On information and belief, the AMD '688 Products substitute the color key with a pre-selected color.

498. On information and belief, the AMD '688 Products process and transform the data resulting from the processing a color key from the pre-processed data.

499. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the AMD '688 Products, AMD has injured Dynamic Data and is liable for directly infringing one or more claims of the '688 Patent, including at least claim 6, pursuant to 35 U.S.C. § 271(a).

500. On information and belief, AMD also indirectly infringes the '688 Patent by actively inducing infringement under 35 USC § 271(b).

501. On information and belief, AMD has had knowledge of the '688 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '688 Patent and knew of its infringement, including by way of this lawsuit.

502. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '688 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '688 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '688 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '688 Products that have the capability of operating in a manner that infringe one or more of the claims of the '688 Patent, including at least claim 6, and AMD further provides documentation and training materials that cause customers and end users of the AMD '688 Products to utilize the products in a manner that directly infringe one or more claims of the '688

Patent.[34] By providing instruction and training to customers and end-users on how to use the AMD '688 Products in a manner that directly infringes one or more claims of the '688 Patent, including at least claim 6, AMD specifically intended to induce infringement of the '688 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '688 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '688 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '688 Patent, knowing that such use constitutes infringement of the '688 Patent.

503. The '688 Patent is well-known within the industry as demonstrated by multiple citations to the '688 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '688 Patent without paying a reasonable royalty. AMD is infringing the '688 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

504. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '688 Patent.

505. As a result of AMD's infringement of the '688 Patent, Dynamic Data has suffered monetary damages, and seek recovery in an amount adequate to compensate for AMD's

[34] *See, e.g.*, *How to Capture Your Gameplay Using Radeon ReLive*, AMD HELP CENTER ARTICLE NUMBER: DH-02 (last visited October 2018); *Radeon Pro ReLive: How to Set up & Use Chroma Key*, AMD YOUTUBE.COM VIDEO (July 3, 2018). *available at*: https://www.youtube.com/watch?v=-j7KopH1pFo; *Radeon Pro ReLive in AMD Radeon Pro Settings*, AMD USER GUIDE (2018); Nate Oh, *AMD Releases Radeon Software Adrenalin Edition: Overlay, App & More for 2017*, ANANDTECH WEBSITE (December 12, 2017), *available at*: https://www.anandtech.com/show/12147/amd-releases-radeon-software-adrenalin-edition/4 (excerpting AMD's presentation regarding the Radeon ReLive product).

infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT XII
INFRINGEMENT OF U.S. PATENT NO. 7,894,529

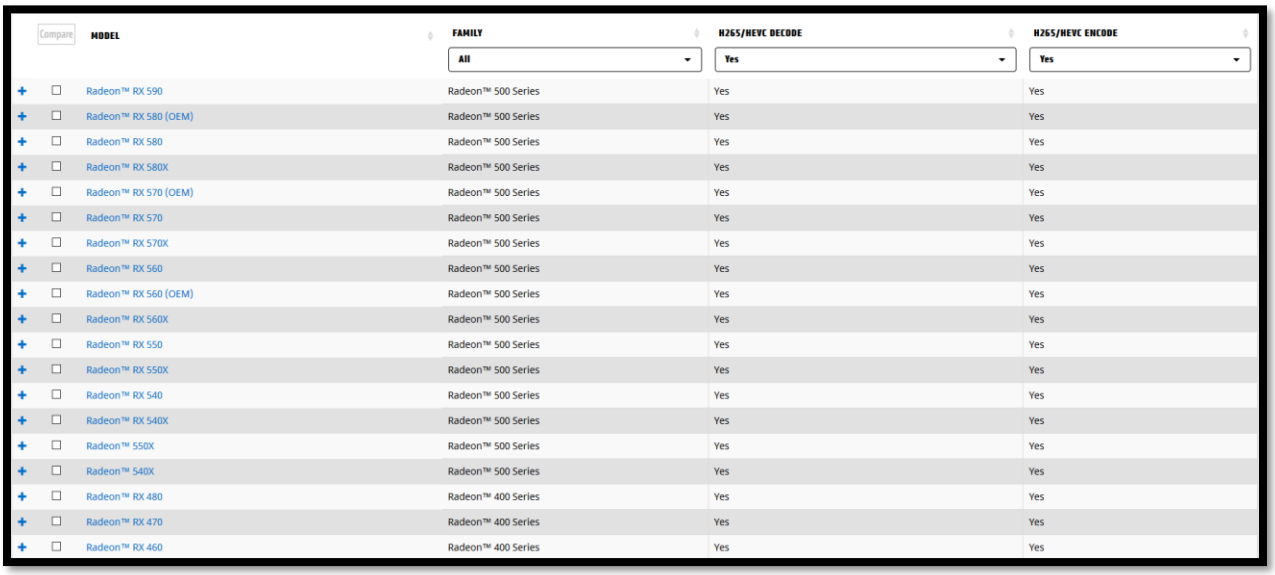
506. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

507. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for determining motion vectors that are each assigned to individual image regions.

508. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '529 Product(s)").

509. The AMD '529 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the AMD '529 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by AMD '529 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

510. The AMD '529 Products contain video processing functionality that complies with the HEVC standard.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

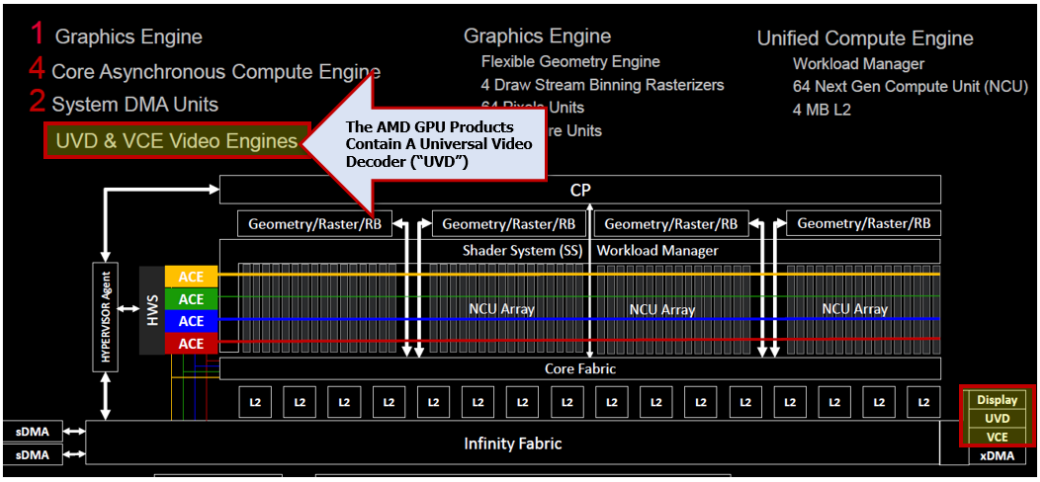
511. The AMD '529 Products comprise a video decoder for decoding video images. The following excerpt from AMD's documentation relating to the AMD '529 Products identifies the accused devices as decoding video data using a first and second frame of video data. Specifically, the AMD '529 Products contain functionality for video decoding through H.265/High Efficiency Video Coding ("HEVC") decoding.

> Vega" 10 naturally includes the latest versions of AMD's video encode and decode acceleration engines, as well. Like "Polaris," "Vega" offers hardware-based decode of HEVC/H.265 main10 profile videos at resolutions up to 3840x2160 at 60Hz, with 10-bit color for HDR content. Dedicated decoding of the H.264 format is also supported at up to 4K and 60Hz. "Vega" can also decode the VP9 format at resolutions up to 3840x2160 using a hybrid approach where the video and shader

> engines collaborate to offload work from the CPU. "Vega's" video encode accelerator also supports today's most popular formats. It can encode HEVC/H.265 at 1080p240, 1440p120, and 2160p60.

Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER at 13-14 (2017) (emphasis added).

512. The AMD '529 Products comprise a video decoder that is identified in block diagrams of the below excerpt from AMD's documentation.



AMD's Radeon Next Generation GPU Architecture "Vega 10", RADEON PRESENTATION at 12 (2017) (annotations added) (showing that in the AMD Products H.265 decoder is identified as "UVD").

513. The circuity of the AMD '529 Product confirms that the AMD '529 Products contain multiple inputs for receiving frame-based encoded video information.

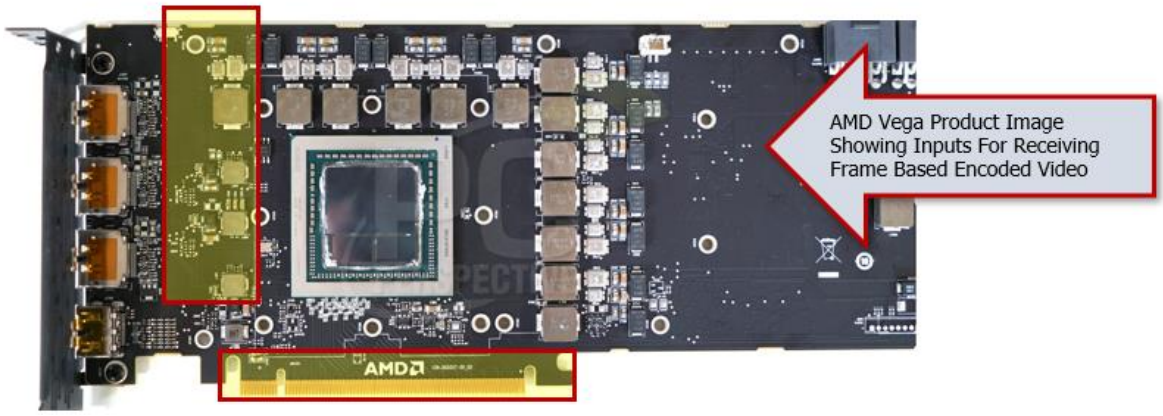
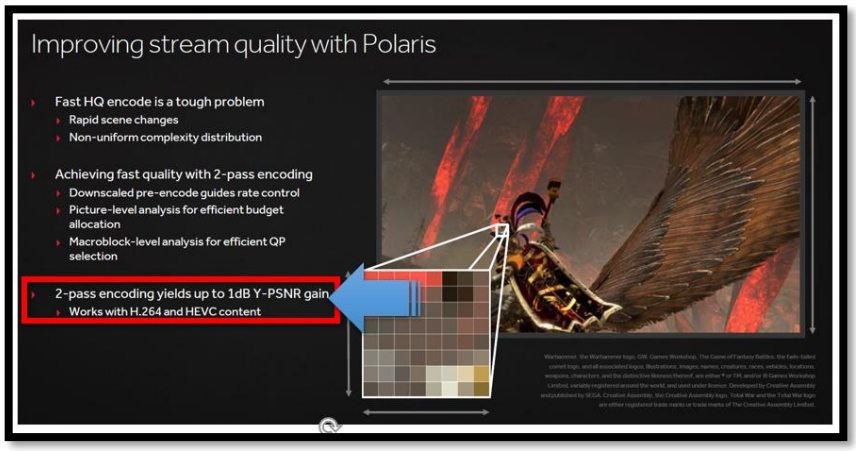


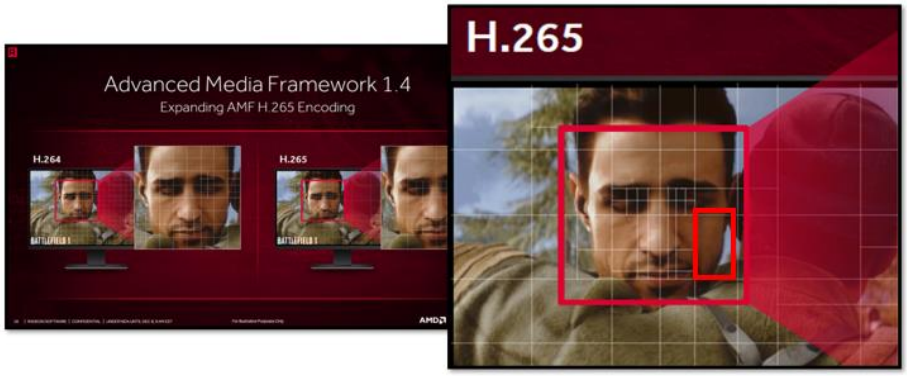
IMAGE OF AMD PRODUCT CIRCUIT BOARD: DETAILED PRODUCT ANALYSIS (2018) (annotation added) (showing inputs including: USB, Wi-Fi, and external memory).

514. The AMD '529 Products include input sfor receiving and decoding HEVC video data. "The Infinity Fabric logic links the graphics core to other on-chip units like the multimedia, display, and I/O blocks." Radeon's Next-Generation *Vega Architecture,* AMD WHITEPAPER at 13 (2017).



The Polaris Architecture: Features, Technologies and Process, AMD PRESENTATION at 36 (2016) (annotation added) (stating "2-pass encoding yields up to 1db Y-PSNR gain . . . works with H.264 and HEVC content).

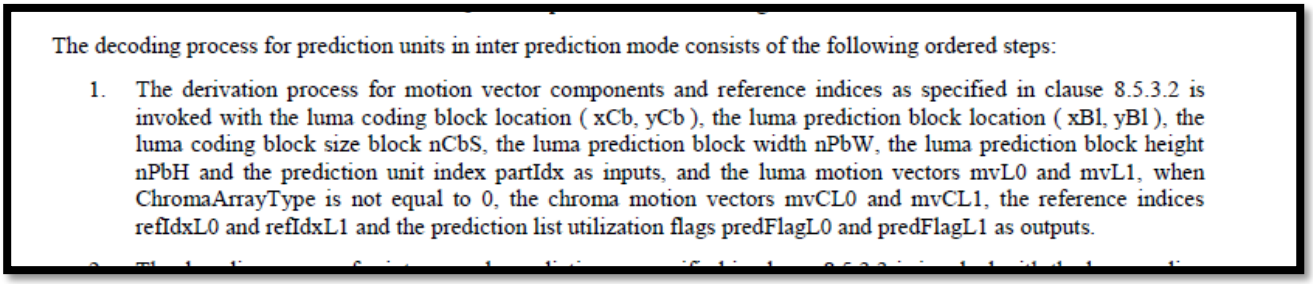
515. The AMD '529 Products incorporate a decoding unit for decoding the frame of the received video data. The decoding utilizes a second frame recovery unit that is a decoding motion vector. Specifically, the encoding and decoding process for video data received by the AMD '529 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.



RADEON SOFTWARE PRESENTATION at 16 (2017) (showing that the encoding and decoding functionality allows offset from a center position).

516. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '529 Products - necessarily infringe the '529 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '529 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to AMD's infringement of the '529 patent: "3.110 Prediction Unit Definition;" "6.3.2 Block and quadtree structures;" "6.3.3 Spatial or component-wise partitioning;" "6.4.2 Derivation process for prediction block availability;" "7.3.8.5 Coding unit syntax;" "7.3.8.6 Prediction unit syntax;" "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process."

517. On information and belief, the AMD '529 Products comply with the HEVC standard, which requires determining motion vectors assigned to individual image regions of an image.



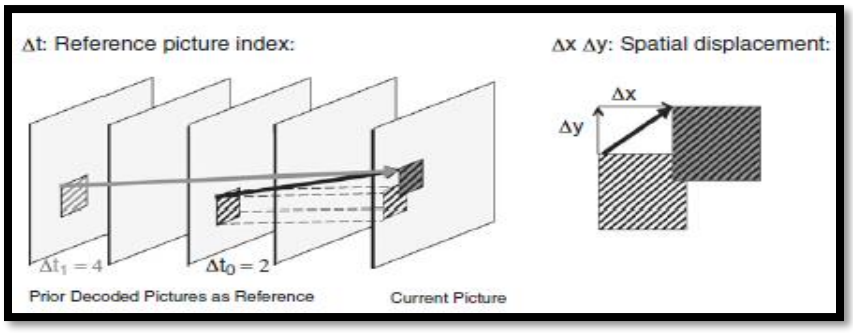
The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 8.5.3.1 (February 2018).

518. On information and belief, AMD has directly infringed and continues to directly infringe the '529 patent by, among other things, making, using, offering for sale, and/or selling technology for implementing a motion estimation technique that assigns at least one motion vector to each of the image blocks and generating a modification motion vector for at least the first image block.

519. On information and belief, the encoded video stream received by the AMD '529 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

520. On information and belief, the AMD '529 Products perform the step of selecting a second image block where the motion vector that is assigned to the first image block passes. Specifically, the AMD '529 Products, in the use of inter-picture prediction, look at two or more blocks in different frames wherein the vector passes through both the first and second image block.

The following excerpts from documentation relating the video estimation technique used by the AMD '529 Products explains how HEVC uses motion estimation to determine a temporal intermediate position between two images wherein two image blocks are selected that have a motion vector passing in both the first and second image block.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

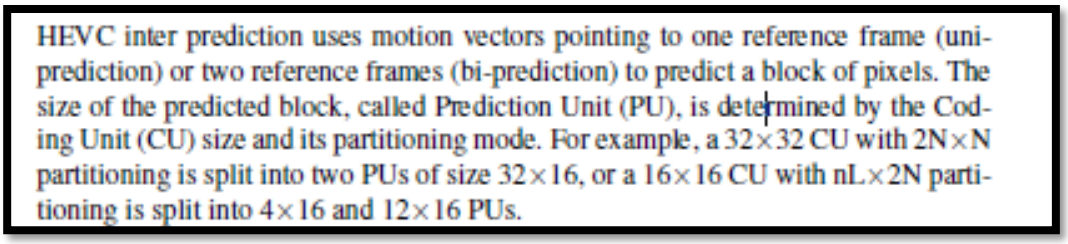
Johan Bartelmess, *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

521. On information and belief, the AMD '529 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the AMD '529 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the AMD '529 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., Vol. 22, No. 12, p. 1654 (December 2012) (emphasis added).

522. The following excerpt from an article describing the architecture of the video stream received by the AMD '529 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."



HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al.*, *Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

523. On information and belief, any implementation of the HEVC standard infringes the '529 patent as every possible implementation of the standard requires: determining at least a second image block through which the motion vector assigned to the first image block at least partially passes; generating the modified motion vector as a function of a motion vector assigned to at least the second image block; and assigning the modified motion vector as the motion vector to the first image block. Further, the functionality of the motion estimation process in HEVC uses "motion vector[s]: A two-dimensional vector used for *inter prediction* that provides an offset from the coordinates in the decoded picture to the coordinates in a reference picture," as defined in definition 3.83 of the *ITU-T H.265 Series H: Audiovisual and Multimedia Systems* (2018) (emphasis added); *see also, e.g.*, Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1650 (December 2012) ("The encoder and decoder generate identical inter picture prediction signals by applying motion compensation (MC) using the MV and mode decision data.").

524. The motion estimation done by the AMD '529 Products is done through a PU matching method where the motion vector represents the displacement between the current PU in the current frame and the matching PU in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference

> to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

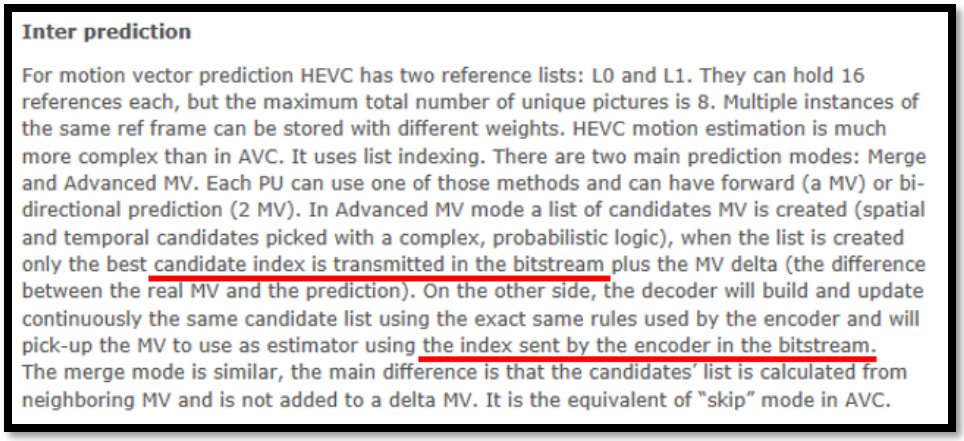
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

525. On information and belief, the AMD '529 Products perform the step of assigning the modified motion vector as the motion vector to the first image block. Specifically, the AMD '529 Products, through the use of AMVP and Merge Mode, select the modified motion vector and assign it to a first block. The displacement between the current prediction unit and the matching prediction unit in the second image (reference image) is signaled using a motion vector. Further, the AMD '529 Products take the modified motion vector "computed from corresponding regions of previously decoded pictures" and transmit the residual.

> A block-wise prediction residual ***is computed from corresponding regions of previously decoded pictures (inter-picture motion compensated prediction) or neighboring previously decoded samples from the same picture (intra-picture spatial prediction***). The residual is then processed by a block transform, and the transform coefficients are quantized and entropy coded. Side information data such as motion vectors and mode switching parameters are also encoded and transmitted.

Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, Vol. 7, No. 6 at 1002 (December 2013) (emphasis added).

526. On information and belief, the AMD '529 Products transmit into the bitstream the candidate index of motion vectors. HEVC documentation states that the coding process will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview*, VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

527. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '529 Products in regular business operations.

528. On information and belief, AMD has directly infringed and continues to directly infringe the '529 Patent by, among other things, making, using, offering for sale, and/or selling technology for determining motion vectors that are each assigned to individual image regions, including but not limited to the AMD '529 Products.

529. On information and belief, the AMD '529 Products are available to businesses and individuals throughout the United States.

530. On information and belief, the AMD '529 Products are provided to businesses and individuals located in Delaware.

531. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the AMD '529 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '529 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

532. On information and belief, AMD also indirectly infringes the '529 Patent by actively inducing infringement under 35 USC § 271(b).

533. AMD has had knowledge of the '529 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '529 Patent and knew of its infringement, including by way of this lawsuit.

534. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '529 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '529 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '529 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '529 Products that have the capability of operating in a manner that infringe one or more of the claims of the '529 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '529 Products to utilize the products in a manner that directly infringe one or more claims of the '529 Patent.[35] By providing instruction and training to customers and end-users on how to use the AMD '529 Products in a manner that directly infringes one or more claims of the '529 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '529 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '529 Products, e.g., through AMD user manuals, product support, marketing materials, and training

[35] *See, e.g.*, *AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

materials to actively induce the users of the accused products to infringe the '529 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '529 Patent, knowing that such use constitutes infringement of the '529 Patent.

535. The '529 Patent is well-known within the industry as demonstrated by multiple citations to the '529 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '529 Patent without paying a reasonable royalty. AMD is infringing the '529 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

536. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '529 Patent.

537. As a result of AMD's infringement of the '529 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT XIII
INFRINGEMENT OF U.S. PATENT NO. 7,542,041

538. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

539. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for dynamically configuring a multi-pipe pipeline system.

540. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD graphic processing units ("GPU") and accelerated processing units ("APU") containing Graphics Core

Next ("GCN") 5th Generation functionality, including: Radeon RX Vega 56, Radeon RX Vega 64, Radeon RX Vega 64 Liquid, Radeon Vega Frontier Edition (Air Cooled), Radeon Vega Frontier Edition (Liquid Cooled), Radeon Instinct MI25, Radeon Pro WX 8200, Radeon Pro WX 9100, Radeon Pro V340, Radeon Pro V340 MxGPU, Ryzen 3 2200GE, Ryzen 3 Pro 2200GE, Ryzen 3 2200G, Ryzen 3 Pro 2200G, Ryzen 5 2400GE, Ryzen 5 Pro 2400GE, Ryzen 5 2400G, Ryzen 5 Pro 2400G (collectively, the "AMD '041 Product(s)").

541. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '041 Products in regular business operations.

542. On information and belief, one or more of the AMD '041 Products include technology for dynamically configuring a multi-pipe pipeline system.

543. On information and belief, AMD has directly infringed and continues to directly infringe the '041 Patent by, among other things, making, using, offering for sale, and/or selling technology for dynamically configuring a multi-pipe pipeline system, including but not limited to the AMD '041 Products.

544. On information and belief, one or more of the AMD '041 Products consist of a multiple-pipeline system wherein each pipeline is configured to include a homogenous set of core functions.

545. On information and belief, one or more of the AMD '041 Products includes auxiliary functions wherein each auxiliary function includes a multiplexer that allows it to be selectively coupled within each pipeline.

546. The AMD '041 Products are a system for dynamically configuring a multi-pipe pipeline system, such as a video processing pipeline system.

547. The AMD ‘041 Products comprise multiple vector pipelines that process data as it traverses the pipeline.

> Each SIMD includes a 16-lane vector pipeline that is predicated and fully IEEE-754 compliant for single precision and double precision floating point operations, with full speed denormals and all rounding modes. Each lane can natively executes a single precision fused or unfused multiply-add or a 24-bit integer operation. The integer multiply-add is particularly useful for calculating addresses within a work-group. A wavefront is issued to a SIMD in a single cycle, but takes 4 cycles to execute operations for all 64 work items.

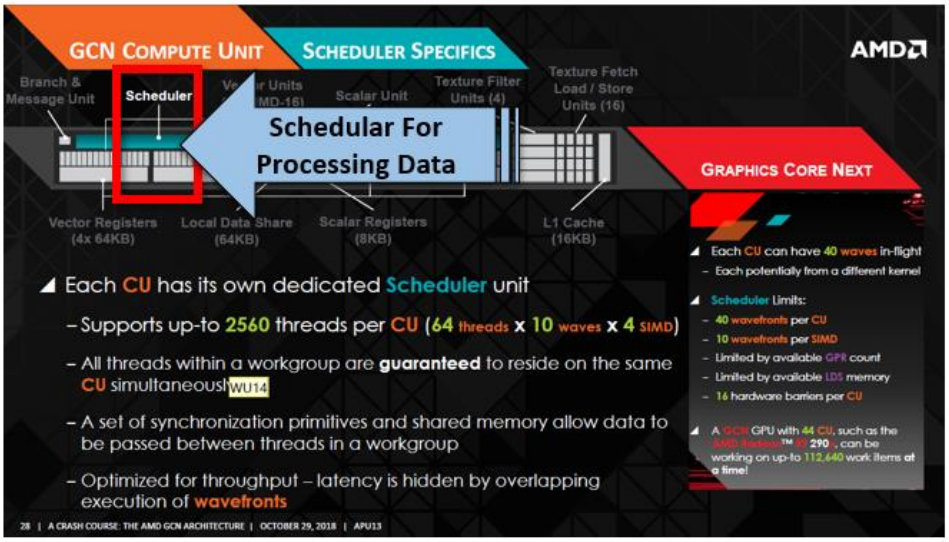
AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 7 (June 2012) (emphasis added).

548. The pipelines that are present in the AMD ‘041 Products enable sequential processing of data. For example, the AMD ‘041 Products are synchronized and process data in order such that correct order is maintained.

> The graphics command processor coordinates the traditional rendering pipeline. The 3D pipeline consists of several types of programmable shaders (e.g. vertex, hull, domain, geometry and pixel shaders) and a variety of fixed function hardware that manipulates triangles and pixels. The shader performance is quite scalable, so the real challenge lies with scaling the fixed function hardware. 3D rendering starts with primitive pipelines that assemble a single triangle per clock. The number of primitive Pipelines in GCN can vary according to performance requirements. Multiple primitive pipelines will partition the screen space and rely on synchronization to maintain the correct triangle order. Assembled triangles are then sent to the shader array for vertex and hull shading. The latter initiates tessellation by changing from vertex to tessellation co-ordinates and setting control information.

AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 12 (June 2012) (emphasis added).

549. The AMD ‘041 Products contain a “Scheduler” that enables data to be processed in a subsequent manner as it traverses the pipeline.



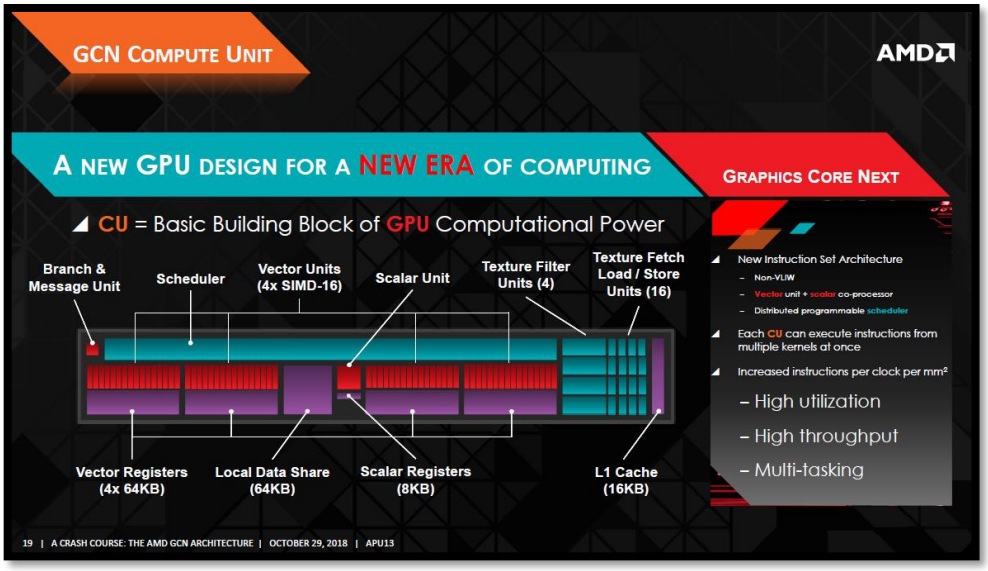
Layla Mah, *The AMD GCN Architecture Crash Course*, AMD DEVELOPER SUMMIT PRESENTATION SESSION GS-4106 at 19 (October 29, 2018) (annotation added).

550. The AMD '041 Products comprise a plurality of pipelines. Each pipeline contains multiple core pipeline elements that are configured to process data as it flows through the pipeline. The below excerpt from AMD reference documentation describes that GCN uses multiple compute pipelines that sequentially process data.

> The DPP array is the heart of the GCN processor. The array is organized as a set of compute unit pipelines, each independent from the others, that operate in parallel on streams of floating point or integer data. The compute unit pipelines can process data or, through the memory controller, transfer data to, or from, memory. Computation in a compute unit pipeline can be made conditional. Outputs written to memory can also be made conditional. When it receives a request, the compute unit pipeline loads instructions and data from memory, begins execution, and continues until the end of the kernel.

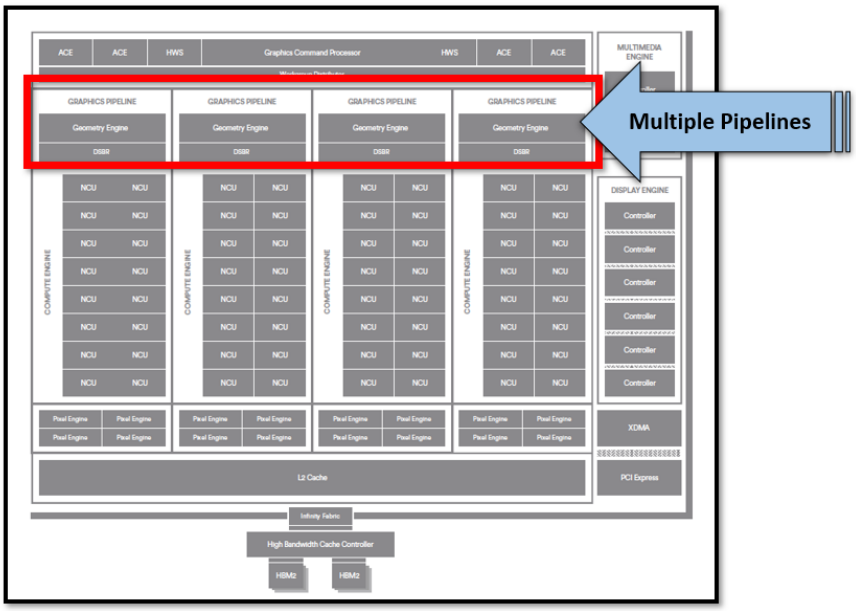
"Vega" Instruction Set Architecture, AMD REFERENCE GUIDE at § 12.16 (July 28, 2017) (emphasis added).

551. On information and belief, the AMD '041 Products sequentially processes data as it enters the pipeline. For example, as data enters the pipeline, scheduling, texture fetch, texture loading, and caching are performed.



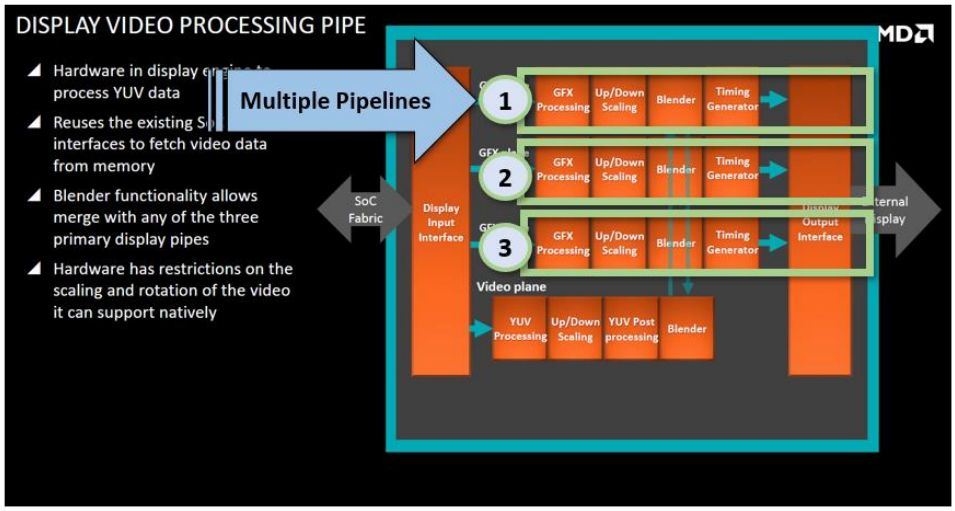
Layla Mah, *The AMD GCN Architecture Crash Course*, AMD DEVELOPER SUMMIT PRESENTATION SESSION GS-4106 at 19 (October 29, 2018) (showing the AMD GCN compute unit that comprises part of the pipeline that sequentially processes data as it traverses the pipeline).

552. AMD whitepapers describe the AMD '041 Products as containing multiple pipelines that process data sequentially. The below excerpt from AMD's documentation shows an instance with four graphics pipeline for the processing of data.



Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER AT 2 (2017) (annotation added).

553. The AMD '041 Products enable decoding and encoding of data using multiple video processing pipelines. The below excerpt from an AMD presentation shows three pipelines for processing video data. In each instance the data is sequentially processed as it moves through the pipeline for display.



Guhan Krishnan, Dan Bouvier, Louis Zhang, Praveen Dongara, ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU at 24 (August 2015) (annotations added)

554. The AMD '041 Products comprise auxiliary elements that can be selected to adjust pipeline settings as the data moves through the pipeline.

555. The AMD '041 Products contain an intelligent workload distributor that can adjust pipeline settings in one or more of the pipelines that are processing data.

> Another innovation of "Vega's" NGG is improved load balancing across multiple geometry engines. An intelligent workload distributor (IWD) continually adjusts pipeline settings based on the characteristics of the draw calls it receives in order to maximize utilization.

Radeon's Next-Generation Vega Architecture, AMD WHITEPAPER AT 2 (2017) (emphasis added).

556. On information and belief, the AMD '041 Products contain a compute unit front-end that can issue instructions while the pipeline is processing data that modify one or more of the pipelines as data is traversed through them. The below excerpt from an AMD white paper

describes the ability to issue up to five instructions to the scalar execution pipelines via registry files.

> The CU front-end can decode and issue seven different types of instructions: branches, scalar ALU or memory, vector ALU, vector memory, local data share, global data share or export, and special instructions. Only issue one instruction of each type can be issued at a time per SIMD, to avoid oversubscribing the execution pipelines. To preserve in-order execution, each instruction must also come from a different wavefront; with 10 wavefronts for each SIMD, there are typically many available to choose from. Beyond these two restrictions, any mix is allowed, giving the compiler plenty of freedom to issue instructions for execution. The CU front-end can issue five instructions every cycle, to a mix of six vector and scalar execution pipelines using two register files. The vector units provide the computational power that is critical for graphics shaders as well as general purpose applications. Together with the special instructions that are handled in the instruction buffers, the two scalar units are responsible for all control flow in the GCN Architecture.

AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 5 (June 2012) (emphasis added).

557. The AMD '041 Products comprise multiple vector pipelines that process data as it traverses the pipeline.

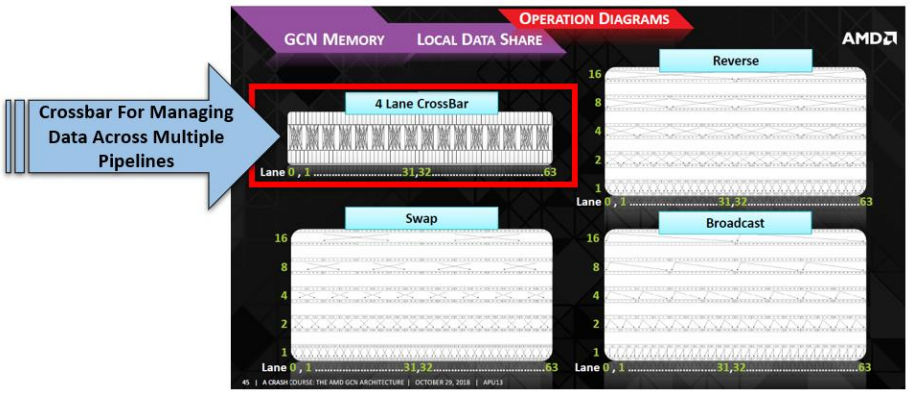
> Each SIMD includes a 16-lane vector pipeline that is predicated and fully IEEE-754 compliant for single precision and double precision floating point operations, with full speed denormals and all rounding modes. Each lane can natively executes a single precision fused or unfused multiply-add or a 24-bit integer operation. The integer multiply-add is particularly useful for calculating addresses within a work-group. A wavefront is issued to a SIMD in a single cycle, but takes 4 cycles to execute operations for all 64 work items.

AMD Graphics Cores Next (GCN) Architecture, AMD WHITE PAPER at 7 (June 2012) (emphasis added).

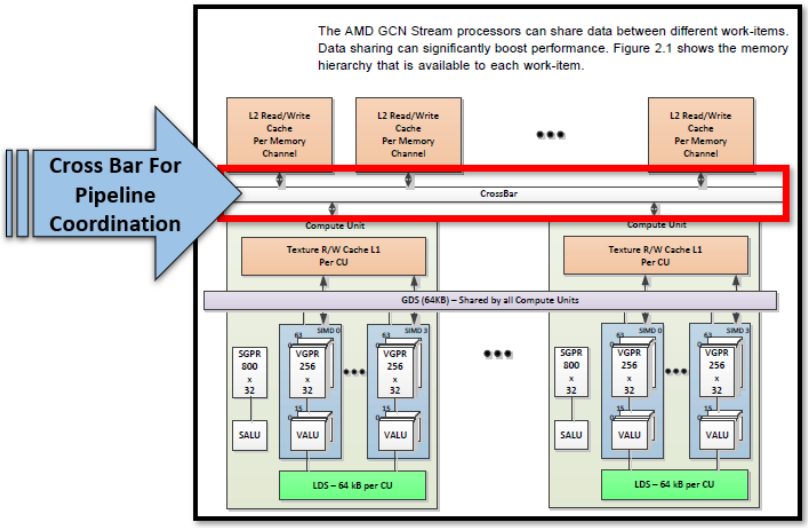
558. The AMD '041 Products contain pipelines that are coupled to a plurality of auxiliary elements that control the function of the pipelines. Specifically, axillary elements can pass signals to multiple pipelines using crossbar fabrics. "The graphics pipeline is orchestrated using the same set of techniques as the ACEs. Each stage of the 3D pipeline can operate concurrently, as can any ACEs. The primitive and pixel pipelines are connected to the programmable GCN shaders through crossbar fabrics. The task queues synchronize different

shaders and fixed function hardware through cache or memory." *AMD Graphics Cores Next (GCN) Architecture,* AMD WHITE PAPER at 13 (June 2012) (emphasis added).

559. The AMD '041 Products comprise multiple pipelines that are connected via a crossbar such that core pipelines elements process the data as it traverses the core pipeline elements.



Layla Mah, *The AMD GCN Architecture Crash Course,* AMD DEVELOPER SUMMIT PRESENTATION SESSION GS-4106 at 45 (October 29, 2018) (annotation added).



AMD Reference Guide: Graphics Core Next Architecture, Generation 3 Rev. 1.1 at § 2.3 (August 2016) (annotations added).

560. On information and belief, the AMD '041 Products are available to businesses and individuals throughout the United States.

561. On information and belief, the AMD ‘041 Products are provided to businesses and individuals located in Delaware.

562. By making, using, testing, offering for sale, and/or selling products and services for dynamically configuring a multi-pipe pipeline system, including but not limited to the AMD ‘041 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘041 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

563. On information and belief, AMD also indirectly infringes the ‘041 Patent by actively inducing infringement under 35 USC § 271(b).

564. AMD has had knowledge of the ‘041 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the ‘041 Patent and knew of its infringement, including by way of this lawsuit.

565. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD ‘041 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the ‘041 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the ‘041 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD ‘041 Products that have the capability of operating in a manner that infringe one or more of the claims of the ‘041 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD ‘041 Products to utilize the products in a manner that directly infringe one or more claims of the ‘041

Patent.[36] By providing instruction and training to customers and end-users on how to use the AMD '041 Products in a manner that directly infringes one or more claims of the '041 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '041 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '041 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '041 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '041 Patent, knowing that such use constitutes infringement of the '041 Patent.

566. The '041 Patent is well-known within the industry as demonstrated by multiple citations to the '041 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '041 Patent without paying a reasonable royalty. AMD is infringing the '041 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

567. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '041 Patent.

568. As a result of AMD's infringement of the '041 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's

[36] *See, e.g.*, *AMD Graphics Cores Next (GCN) Architecture*, AMD WHITE PAPER (June 2012); Layla Mah, *The AMD GCN Architecture Crash Course*, AMD DEVELOPER SUMMIT PRESENTATION SESSION GS-4106 (October 29, 2018); *Vega Instruction Set Architecture*, AMD REFERENCE GUIDE (July 28, 2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITEPAPER (2017); Guhan Krishnan, Dan Bouvier, Louis Zhang, Praveen Dongara, ENERGY EFFICIENT GRAPHICS AND MULTIMEDIA IN 28NM CARRIZO APU (August 2015); AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 (August 2016).

infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT XIV
INFRINGEMENT OF U.S. PATENT NO. 7,571,450

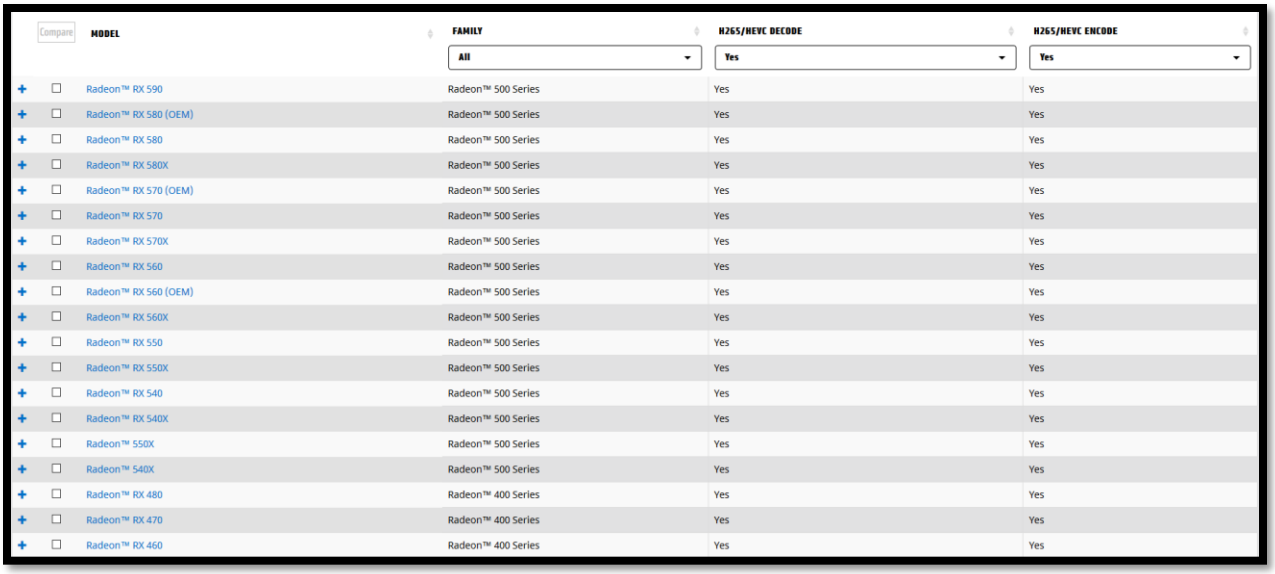
569. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

570. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for displaying information.

571. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors that supported H.265 decoding functionality. The infringing AMD Radeon graphic processors include: AMD Radeon 500 Series GPUs (Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '450 Product(s)").

572. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '450 Products in regular business operations.

573. On information and belief, one or more of the AMD '450 Products include technology for decoding HEVC data for display in compliance with the HEVC standard.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

574. On information and belief, by complying with the HEVC standard, the AMD devices – such as the AMD '450 Products - necessarily infringe the '450 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '450 patent, including but not limited to claim 8. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to AMD's infringement of the '450 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing

bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

575. On information and belief, the AMD '450 Products receive data that is segmented into Network Abstraction Layer ("NAL") Units. NAL Units are segments of data that can include video data and overlay data (such as captions and overlay images). The AMD '450 Products support the receipt of VCL and non-VCL NAL units. The VCL NAL units contain the data that represents the values of the samples in the video pictures, and the non-VCL NAL units contain any associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

576. The AMD '450 Products process data in the form of VCL NAL Units that contain segments of data which are used to generate an image (e.g., HEVC image) on a display device. Each VCL NAL Unit comprises a discrete number of bites which make up a segment. The following excerpt from the HEVC specification describes a NAL unit as being a segment with a "demarcation" setting forth where the segment ends and begins.

> NumBytesInNalUnit specifies the size of the NAL unit in bytes. This value is required for decoding of the NAL unit. Some form of demarcation of NAL unit boundaries is necessary to enable inference of NumBytesInNalUnit. One such demarcation method is specified in Annex B for the byte stream format. Other methods of demarcation may be specified outside of this Specification.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.2.1 (February 2018) (emphasis added).

577. The AMD '450 Products receive VCL NAL units that contain the data that represents the values of the samples in the video pictures, and non-VCL NAL units that contain associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg et al, *Overview of HEVC High-Level Syntax and Reference Picture Management*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

578. The AMD'450 Products perform filtering, wherein the filtering enables a user to select a data element based on the user's selection. Specifically, a user can select the display of Non-VCL NAL Unit data which can include closed captions or other overlay information that is selected based on the user interaction. The data that is selected by the user is parsed by the system and filtered. The Non-VCL NAL Units include supplemental enhancement information ("SEI") messages. The SEI data that is received contains overlay information that can be combined with the image data that has already been received.

sei_message( ) {	Descriptor
payloadType = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadType += 255	
}	
last_payload_type_byte	u(8)
payloadType += last_payload_type_byte	
payloadSize = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadSize += 255	
}	
last_payload_size_byte	u(8)
payloadSize += last_payload_size_byte	
sei_payload(payloadType, payloadSize)	
}	

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.3.5 (February 2018).

579. The AMD '450 Products perform rendering of an output image to be displayed on a display device on the basis of the first data-element selected by the filter. The overlay data is used to render overlays of the display data. The amount of overlay data that is downloaded in the form of Non-VCL data comprises a portion of the overlay that is displayed.

580. On information and belief, AMD has directly infringed and continues to directly infringe the '450 Patent by, among other things, making, using, offering for sale, and/or selling technology for displaying information, including but not limited to the AMD '450 Products.

581. On information and belief, one or more of the AMD '450 Products enable methods and systems wherein a user does not need to make a new selection after being switched from one service to a second service.

582. On information and belief, one or more of the AMD '450 Products perform a method of displaying information on a display device wherein receiving a transport stream comprises services, with the services having elementary streams of video and of data elements.

583. On information and belief, one or more of the AMD ‘450 Products perform a method of displaying information on a display device wherein user actions of making a user selection of a type of information to be displayed on the device are received.

584. On information and belief, one or more of the AMD ‘450 Products perform a method of displaying information on a display device wherein filtering to select a data element of a first one of the services on the basis of the user selection is performed.

585. On information and belief, one or more of the AMD ‘450 Products perform a method of displaying information on a display device wherein rendering to calculate an output image to be displayed on the display device, on the basis of the first data element selected by the filer is performed.

586. On information and belief, one or more of the AMD ‘450 Products perform a method of displaying information on a display device wherein switching from the first one of the services to a second one of the services, characterized in comprising a second step of filtering to select a second data-element of the second one of the services, on the basis of the user selection is performed.

587. On information and belief, one or more of the AMD ‘450 Products perform a method of displaying information on a display device wherein being switched from the first one of the services to the second one of the services, with the data-element and the second data-element being mutually semantically related and a second step of rendering to calculate the output image to be displayed on the display device, on the basis of the second data-element selected by the filter is performed.

588. On information and belief, the AMD ‘450 Products are available to businesses and individuals throughout the United States.

589. On information and belief, the AMD ‘450 Products are provided to businesses and individuals located in Delaware.

590. By making, using, testing, offering for sale, and/or selling products and services for displaying information, including but not limited to the AMD ‘450 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘450 Patent, including at least claim 8 pursuant to 35 U.S.C. § 271(a).

591. On information and belief, AMD also indirectly infringes the ‘450 Patent by actively inducing infringement under 35 USC § 271(b).

592. AMD has had knowledge of the ‘450 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the ‘450 Patent and knew of its infringement, including by way of this lawsuit.

593. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD ‘450 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the ‘450 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the ‘450 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD ‘450 Products that have the capability of operating in a manner that infringe one or more of the claims of the ‘450 Patent, including at least claim 8, and AMD further provides documentation and training materials that cause customers and end users of the AMD ‘450 Products to utilize the products in a manner that directly infringe one or more claims of the ‘450

Patent.[37] By providing instruction and training to customers and end-users on how to use the AMD '450 Products in a manner that directly infringes one or more claims of the '450 Patent, including at least claim 8, AMD specifically intended to induce infringement of the '450 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '450 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '450 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '450 Patent, knowing that such use constitutes infringement of the '450 Patent.

594. The '450 Patent is well-known within the industry as demonstrated by multiple citations to the '450 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '450 Patent without paying a reasonable royalty. AMD is infringing the '450 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

595. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '450 Patent.

596. As a result of AMD's infringement of the '450 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's

[37] *See, e.g.*, *The Polaris Architecture: Features, Technologies and Process,* AMD PRESENTATION (2016); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD RADEON PRESENTATION (2017); *Radeon's Next-Generation Vega Architecture,* AMD WHITEPAPER (2017); AMD VEGA PRODUCT SPECIFICATION SHEET (2018); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs,* AMD PRESS RELEASE (Sept. 27, 2016); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017).

infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT XV
INFRINGEMENT OF U.S. PATENT NO. 7,750,979

597. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

598. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion compensation in video signal processing.

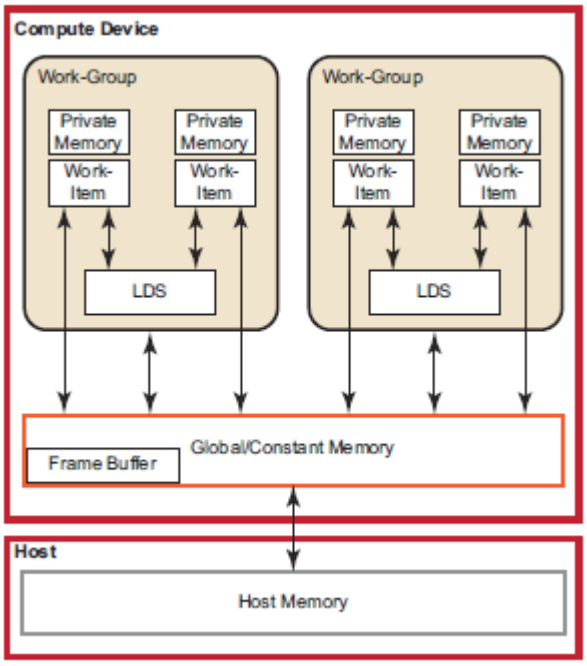
599. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Ryzen Series central processing units ("CPU"), including the following models: AMD Ryzen 3 1200, AMD Ryzen 3 1300X, AMD Ryzen 3 2200G, AMD Ryzen 3 2200GE, AMD Ryzen 3 PRO 1200, AMD Ryzen 3 PRO 1300, AMD Ryzen 5 1400, AMD Ryzen 5 1500X, AMD Ryzen 5 1600, AMD Ryzen 5 1600X, AMD Ryzen 5 2400G, AMD Ryzen 5 2400GE, AMD Ryzen 5 2600, AMD Ryzen 5 2600X, AMD Ryzen 5 PRO 1500, AMD Ryzen 5 PRO 1600, AMD Ryzen 7 1700, AMD Ryzen 7 1700X, AMD Ryzen 7 1800X, AMD Ryzen 7 2700, AMD Ryzen 7 2700X, AMD Ryzen 7 PRO 1700, AMD Ryzen 7 PRO 1700X, AMD Ryzen Threadripper 1900X, AMD Ryzen Threadripper 1920X, AMD Ryzen Threadripper 1950X, AMD Ryzen Threadripper 2920X, AMD Ryzen Threadripper 2950X, AMD Ryzen Threadripper 2970WX, and AMD Ryzen Threadripper 2990WX (collectively, the "AMD '979 Product(s)").

600. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '979 Products in regular business operations.

601. On information and belief, AMD has directly infringed and continues to directly infringe the '979 Patent by, among other things, making, using, offering for sale, and/or selling

technology for motion compensation in video signal processing, including but not limited to the AMD '979 Products.

602. The AMD '979 Products perform the step of establishing a window size. The below documentation shows how the AMD '979 Products pass the data for display in the window through a buffer.



AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 at § 10.1 (August 2016).

603. The AMD '979 Products contain functionality wherein the data that is passed to the buffer is of an established window size. The below excerpt from AMD documentation describes how the Render Back Ends calculate the window size and pass the corresponding data for the window display to the buffer.

> Once the pixels fragments in a tile have been shaded, they flow to the Render Back-Ends (RBEs). The RBEs apply depth, stencil and alpha tests to determine whether pixel fragments are visible in the final frame. The visible pixels fragments are then sampled for coverage and color to construct the final output pixels. The RBEs in GCN can access up to 8 color samples (i.e. 8x MSAA) from the 16KB color caches and 16 overage samples (i.e. for up to 16x EQAA) from the 4KB depth caches per pixel. The color samples are blended using weights determined by the coverage

> samples to generate a final anti-aliased pixel color. The results are written out to the frame buffer, through the memory controllers.

AMD Graphic Cores Next ("GCN") Architecture, AMD WHITEPAPER at 13 (June 2012) (emphasis added).

604. The AMD '979 Products place the data for the corresponding sample window in two buffers which are called the DMIF or Display Memory Interface FIFO and the line buffer. The data that is based to the DMIF and line buffer comprise data sufficient for display in the window.

> DRAM is most commonly placed in self-refresh due to stutter mode when the internal GPU is in use. The display buffer in the GPU is a combination of a large buffer known as the DMIF (Display Memory Interface FIFO) and a smaller line buffer. The DMIF takes data originating from DRAM and sends it to the line buffer to draw to the screen. When the data level in the DMIF is full, DRAM is placed in self-refresh, and incoming DRAM requests are queued. As the DMIF drains, it eventually falls below a predefined watermark level, at which point hardware pulls DRAM out of self-refresh and services all the requests in the queue. Once all the requests are complete and the DMIF is full again, a transition back into self-refresh occurs if the stutter mode conditions are still met.

BKDG for AMD Family 15h Models 70h-7Fh Processors, AMD DOCUMENT NO. 55072 REV. 3.09 at 73 (June 2018) (emphasis added)

605. In the AMD '979 Products the frame buffer comprises the portion of system memory dedicated for reading and writing of display information.

Table 55: Recommended Legacy Frame Buffer Configurations

System Memory Size	Frame Buffer Size
1 x 2 GB	UMA = 256 MB
1 x 4 GB	UMA = 512 MB
2 GB + 4 GB = 6 GB	UMA = 1 GB
2 x 4 GB = 8 GB	UMA = 1 GB

Table 56: Non-Legacy Mode (Default for Windows® 8.1 and Windows® 10) Carve Out Table

System Memory Size	Resolution		
	1920x1080 and below	2560x1600	3840x2160
2 GB and 3 GB	32 MB	48 MB	80 MB
4 GB	80 MB	80 MB	80 MB
6 GB	384 MB	384 MB	384 MB
8 GB	512 MB	512 MB	512 MB

BKDG for AMD Family 15h Models 70h-7Fh Processors, AMD DOCUMENT NO. 55072 REV. 3.09 at 157 (June 2018).

606. The AMD '979 Products enable the prefetching of data for display using the "Probe" command." Specifically, the "Probe" command allows the buffer to prefetch data from

the cache and place it into the buffers for display on the device. Th below excerpt from AMD documentation describes these commands for the AMD '979 Products.

35	S_DCACHE_WB_VOL	Write back dirty data in the scalar data cache volatile lines.
36	S_MEMTIME	Return current 64-bit timestamp.
37	S_MEMREALTIME	Return current 64-bit RTC.
38	S_ATC_PROBE	Probe or prefetch an address into the SQC data cache.
39	S_ATC_PROBE_BUFFER	Probe or prefetch an address into the SQC data cache.
40	S_DCACHE_DISCARD	Discard one dirty scalar data cache line. A cache line is 64 bytes. Normally, dirty cachelines (one which have been written by the shader) are written back to memory, but this instruction allows the shader to invalidate and not write back cachelines which it has previously written. This is a performance optimization to be used when the shader knows it no longer needs that data. Address is calculated the same as S_STORE_DWORD, except the 6 LSBs are ignored to get the 64 byte aligned address. LGKM count is incremented by 1 for this opcode.

"Vega" Instruction Set Architecture, AMD REFERENCE GUIDE at § 12. 6 (July 28, 2017) (emphasis added).

607. The AMD '979 Products perform the step at the video processing stage of fetching a fixed number of pixels from the second line buffers. Specifically, the AMD '979 Products contain functionality wherein the data that is passed to the buffer is of an established window size.

608. The AMD '979 Products support storing pixels from the input stream into a first set of line buffers. The pixels stored in the first set of line buffer include pixels for the established window size. The following excerpt from AMD documentation show that the sampling window size field is passed to the buffer for the storage of pixels.

609. Further, the AMD '979 Products pass the stream into the line buffer based on the "Frame Buffer Size" which is based on the window size that the data is being written to.

610. On information and belief, one or more of the AMD '979 Products use line buffers that are decoupled and that can deliver a fixed number of pixels, as may be required by a video processing stage, using a sampling pattern that is defined as one among several selectable sampling windows.

611. On information and belief, one or more of the AMD ‘979 Products have a variable window size for sampling subsets of the array as a two-dimensional window that spans the pixels in the array.

612. On information and belief, one or more of the AMD ‘979 Products have a video processing stage that inputs pixels using a fixed number of pixels.

613. On information and belief, one or more of the AMD ‘979 Products performs a method for delivering the input stream of pixels to the video processing stage.

614. On information and belief, one or more of the AMD ‘979 Products performs a method comprising establishing a window size and a sampling-window size, such that the window size is a multiple of the sampling-window size and the sampling-window size defines the fixed number of pixels.

615. On information and belief, one or more of the AMD ‘979 Products performs a method comprising storing pixels from the input stream into a first set of line butters, the pixels stored in the first set of line butters including pixels for the established window size.

616. On information and belief, one or more of the AMD ‘979 Products performs a method comprising prefetching the stored pixels from the first set of line butters into a second set of line buffers, the second set of line buffers being sufficiently long to store at least the pixels corresponding to the established sampling-window size.

617. On information and belief, one or more of the AMD ‘979 Products performs a method comprising fetching the fixed number of pixels from the second set of line buffers for the video processing stage.

618. On information and belief, one or more of the AMD ‘979 Products performs a method wherein storing pixels from the input stream into a first set of line butters, the pixels stored

in the first set of line butters including pixels for the established window size, prefetching the stored pixels from the first set of line butters into a second set of line buffers, and fetching the fixed number of pixels from the second set of line buffers for the video processing stage are performed concurrently.

619. On information and belief, the AMD '979 Products are available to businesses and individuals throughout the United States.

620. On information and belief, the AMD '979 Products are provided to businesses and individuals located in Delaware.

621. By making, using, testing, offering for sale, and/or selling products and services for motion compensation in video signal processing, including but not limited to the AMD '979 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '979 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

622. On information and belief, AMD also indirectly infringes the '979 Patent by actively inducing infringement under 35 USC § 271(b).

623. AMD has had knowledge of the '979 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '979 Patent and knew of its infringement, including by way of this lawsuit.

624. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '979 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '979 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '979 Patent

and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '979 Products that have the capability of operating in a manner that infringe one or more of the claims of the '979 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '979 Products to utilize the products in a manner that directly infringe one or more claims of the '979 Patent.[38] By providing instruction and training to customers and end-users on how to use the AMD '979 Products in a manner that directly infringes one or more claims of the '979 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '979 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD '979 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '979 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '979 Patent, knowing that such use constitutes infringement of the '979 Patent.

625. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '979 Patent.

626. As a result of AMD's infringement of the '979 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

[38] *See, e.g.*, AMD REFERENCE GUIDE: GRAPHICS CORE NEXT ARCHITECTURE, GENERATION 3 REV. 1.1 (August 2016); *AMD Graphic Cores Next ("GCN") Architecture,* AMD WHITEPAPER (June 2012); *BKDG for AMD Family 15h Models 70h-7Fh Processors*, AMD DOCUMENT NO. 55072 REV. 3.09 (June 2018); *Vega Instruction Set Architecture*, AMD REFERENCE GUIDE (July 28, 2017); AMD 990FX/990X/970 REGISTER REFERENCE GUIDE (2012); RYZEN MASTER 1.4 – QUICK REFERENCE GUIDE (Aug. 2018).

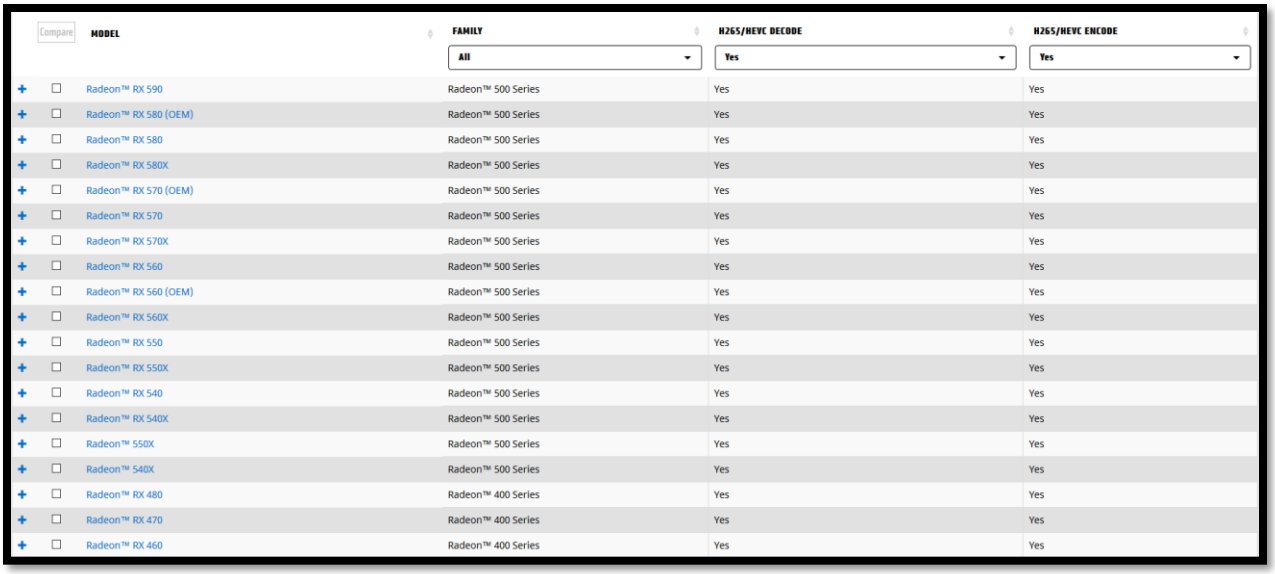
COUNT XVI
INFRINGEMENT OF U.S. PATENT NO. 7,058,227

627. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

628. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for detecting occlusion and reducing halo effects in motion compensated pictures.

629. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD Radeon graphic processors containing H.265/High Efficiency Video Coding ("HEVC") encoding functionality, including: AMD Radeon 500 Series GPUs (Radeon RX 580, Radeon RX 580X, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540X); AMD Radeon 400 Series GPUs (Radeon RX 480, Radeon RX 470, Radeon RX 460); AMD Radeon RX Vega Series GPUs (Radeon RX Vega 64, Radeon RX Vega 56, Radeon RX Vega 64 Liquid Cooled, Radeon Pro Vega 56, Radeon Pro Vega 64); and AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module) (collectively, the "AMD '227 Product(s)").

630. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD '227 Products that contain functionality for motion estimation and edge location detection and comparison in successive field periods in compliance with the HEVC standard.



Compare	MODEL	FAMILY	H265/HEVC DECODE	H265/HEVC ENCODE
		All	Yes	Yes
+ ☐	Radeon™ RX 590	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 580X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 570X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560 (OEM)	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 560X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 550X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ 540X	Radeon™ 500 Series	Yes	Yes
+ ☐	Radeon™ RX 480	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 470	Radeon™ 400 Series	Yes	Yes
+ ☐	Radeon™ RX 460	Radeon™ 400 Series	Yes	Yes

AMD Graphics Card Specifications, AMD SPECIFICATIONS WEBSITE, available at: https://www.amd.com/en/products/specifications/graphics (showing the following products perform HEVC encoding/decoding: Radeon RX 590, Radeon RX 580, Radeon RX 580X, Radeon RX570, Radeon RX 570, Radeon RX 570X, Radeon RX 560, Radeon RX 560X, Radeon RX 550, Radeon RX 550X, Radeon RX 540, Radeon RX 540X, Radeon 550X, Radeon 540Xm Radeon RX 480, Radeon RX 470, Radeon RX 460); *AMD High Performance Embedded GPUs*, AMD WEBSITE, available at: https://www.amd.com/en/products/embedded-graphics-high-performance (showing the following products perform HEVC encoding/decoding: AMD Embedded Radeon E9260 GPUs (Embedded Radeon E9260 MXM Module and Embedded Radeon E9260 PCIe Module); *AMD's Radeon Next Generation GPU Architecture "Vega 10,"* AMD PRESENTATION at 18 (2017) ("UVD (H.265) encode hardware acceleration now included, decode capable").

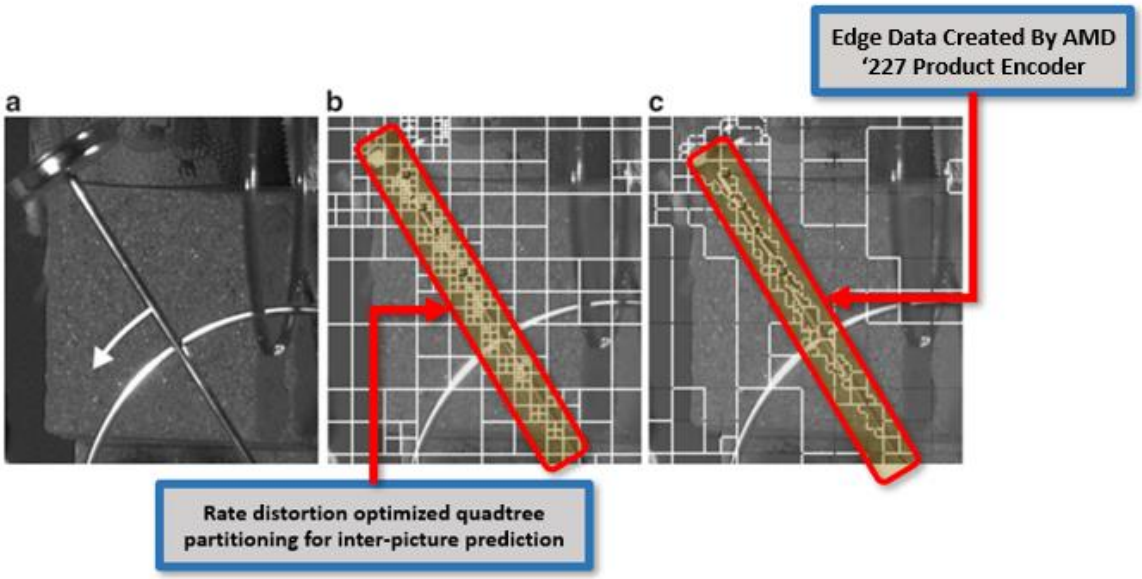
631. On information and belief, one or more AMD subsidiaries and/or affiliates use the AMD '227 Products in regular business operations.

632. On information and belief, the AMD '227 Products estimate a motion vector field for an image signal.

633. The AMD '227 Products use two types of prediction methods for processing pixel information when encoding and decoding video data in HEVC format: inter prediction and intra prediction. Inter prediction utilizes motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra prediction uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. The HEVC Specification (*e.g.*, *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND

MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) sets forth the standard that is followed by HEVC compliant devices such as the AMD '227 Products, and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the AMD '227 Products perform a method for encoding a video signal comprised of pixels using motion vectors when performing encoding of H.265/HEVC video data.

634. During the encoding process the AMD '227 products process pixel information based on edge data. The edge data is generated by the AMD '227 products using merge mode estimation. Specifically, the AMD '227 Products generate merge estimation regions which identify edge information within a video frame. The merge estimation regions are comprised of prediction units ("PU") that contain luma values. For example, in the below diagram PUs are shown. The encoding process then identifies along the edges of each prediction unit a merge estimation region ("MER"). The MER regions thus identify the edges and the PU contains the intensity estimate for the pixels.



Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (annotations added).

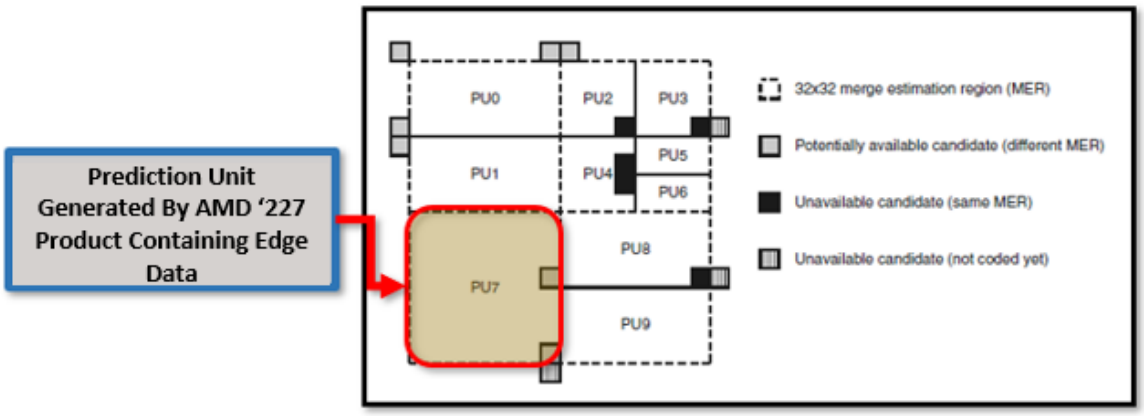
635. On information and belief, the AMD ’227 Products detect edges in the motion vector field.

636. The AMD ‘227 Products in the process of encoding video content in HEVC format generate merge estimation regions generate edge data that include luma location and luma values which include a first intensity estimate. The HEVC standards describes this process as leading to the generation of luma motion vector mvL0 and mvL1.

> [T]he derivation process for luma motion vectors for merge mode as specified in clause I.8.5.3.2.7 is invoked with the luma location (xCb, yCb), the luma location (xPb, yPb), the variables nCbS, nPbW, nPbH, and the partition index partIdx as inputs, and the output being the luma motion vectors mvL0, mvL1, the reference indices refIdxL0, refIdxL1, the prediction list utilization flags predFlagL0 and predFlagL1, the flag ivMcFlag, the flag vspMcFlag, and the flag subPbMotionFlag.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § I.8.5.3.2.1 (February 2018) (emphasis added).

637. The AMD ‘227 Products perform the step of processing edge data from an edge adaptive interpolation process wherein the edge data includes a first intensity estimate of the pixel. Specifically, the AMD ‘227 Products implement HEVC encoding which utilizes Parallel Merge Mode and Merge Estimation Regions (MER’s) within the interpolation process to determine pixel edges. Parallel Merge Mode Estimation identifies the edge data within a prediction unit. The below diagram shows how video data is portioned into 10 prediction units and edge data is calculated and passed to the encoder.



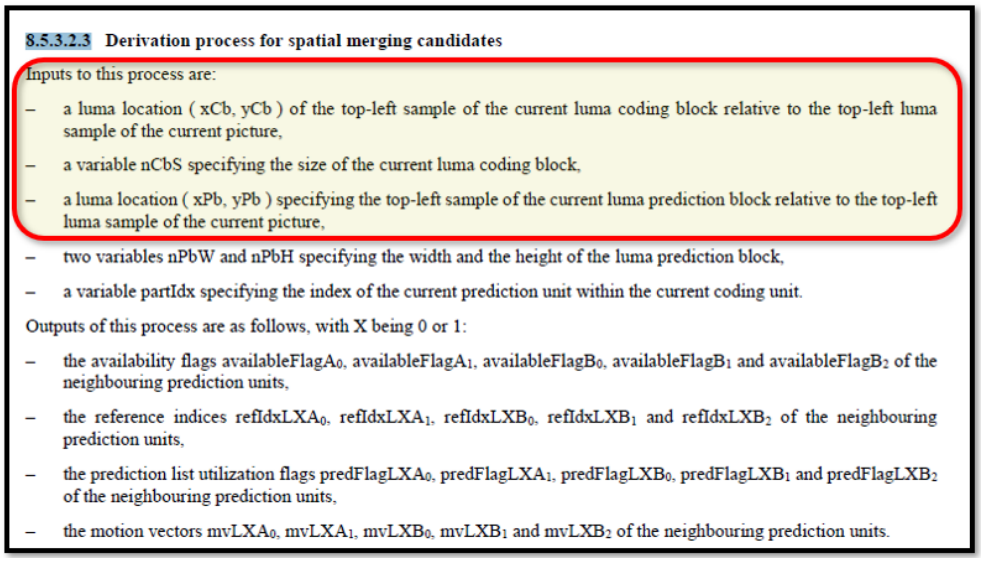
Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 127 (September 2014) (annotations added).

638. The merge estimation processes implemented by the AMD '227 Products is "adaptive." The below excerpt from documentation regarding the HEVC encoding process describes that the "merge estimation level is adaptive."

> In order to enable an encoder to trade-off parallelism and coding efficiency, the parallel merge estimation level is adaptive and signaled as `log2_parallel_merge_level_minus2` in the picture parameter set. The following MER sizes are allowed: 4×4 (no parallel merge estimation possible), 8×8, 16×16, 32×32 and 64 × 64. A higher degree of parallelization, enabled by a larger MER, excludes more potential candidates from the merge candidate list.

Benjamin Bross et al, *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 128 (September 2014) (emphasis added).

639. The motion estimation region ("MER") is an adaptive interpolation process in which the edges of images are calculated and include the intensity estimates of pixels by way of a luma value. The below excerpt from the HEVC specification describes how during the generation of merge estimation regions edge data includes luminosity values (intensity estimates) for pixels within a region.



8.5.3.2.3 Derivation process for spatial merging candidates

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

Outputs of this process are as follows, with X being 0 or 1:

- the availability flags availableFlagA$_0$, availableFlagA$_1$, availableFlagB$_0$, availableFlagB$_1$ and availableFlagB$_2$ of the neighbouring prediction units,
- the reference indices refIdxLXA$_0$, refIdxLXA$_1$, refIdxLXB$_0$, refIdxLXB$_1$ and refIdxLXB$_2$ of the neighbouring prediction units,
- the prediction list utilization flags predFlagLXA$_0$, predFlagLXA$_1$, predFlagLXB$_0$, predFlagLXB$_1$ and predFlagLXB$_2$ of the neighbouring prediction units,
- the motion vectors mvLXA$_0$, mvLXA$_1$, mvLXB$_0$, mvLXB$_1$ and mvLXB$_2$ of the neighbouring prediction units.

HIGH EFFICIENCY VIDEO CODING, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.2.3 (February 2018) (emphasis added).

640. On information and belief, the AMD ’227 Products compare edge locations in successive field periods to identify both foreground and background in an image.

641. On information and belief, AMD has directly infringed and continues to directly infringe the ’227 patent by, among other things, making, using, offering for sale, and/or selling technology for detecting occlusion and reducing halo effects in motion compensated pictures, including but not limited to the AMD ’227 Products.

642. On information and belief, one or more of the AMD ’227 Products perform a method of locating problem areas in an image signal that includes estimating a motion vector field for the image signal.

643. On information and belief, one or more of the AMD ’227 Products perform a method of locating problem areas in an image signal that includes detecting edges in the motion vectors field.

644. On information and belief, one or more of the AMD ’227 Products perform a method of locating problem areas in an image signal that includes comparing edge locations in successive field periods to identify both foreground and background.

645. On information and belief, the AMD ’227 Products are available to businesses and individuals throughout the United States.

646. On information and belief, the AMD ’227 Products are provided to businesses and individuals located in Delaware.

647. On information and belief, by complying with the HEVC standard, AMD’s devices – such as the AMD ‘227 Products - necessarily infringe the ‘227 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the ‘227 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to AMD’s infringement of the ‘227 patent: “7.3.4 Scaling list data syntax;” 7.3.6.1 General slice segment header syntax;” “7.3.6.3 Weighted prediction parameters syntax;” “7.3.8.14 Delta QP syntax;” “7.4.4 Profile, tier and level semantics;” and “7.4.7.3 Weighted prediction parameters semantics.”

648. By making, using, testing, offering for sale, and/or selling products and services for detecting occlusion and reducing halo effects in motion compensated pictures, including but not limited to the AMD ’227 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ’227 Patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

649. On information and belief, AMD also indirectly infringes the '227 Patent by actively inducing infringement under 35 USC § 271(b).

650. AMD has had knowledge of the '227 Patent since at least service of this First Amended Complaint or shortly thereafter, and on information and belief, AMD knew of the '227 Patent and knew of its infringement, including by way of this lawsuit.

651. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '227 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '227 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '227 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '227 Products that have the capability of operating in a manner that infringe one or more of the claims of the '227 Patent, including at least claim 1, and AMD further provides documentation and training materials that cause customers and end users of the AMD '227 Products to utilize the products in a manner that directly infringe one or more claims of the '227 Patent.[39] By providing instruction and training to customers and end-users on how to use the AMD '227 Products in a manner that directly infringes one or more claims of the '227 Patent, including at least claim 1, AMD specifically intended to induce infringement of the '227 Patent. On

[39] *See, e.g., AMD's Radeon Next Generation GPU Architecture "Vega 10"*, RADEON PRESENTATION (2017); *The Polaris Architecture: Features, Technologies and Process*, AMD PRESENTATION (2016); Phil Rogers, *The Programmer's Guide To Reaching For The Cloud*, AMD DEVELOPER SUMMIT PRESENTATION (2013); AORUS RX560 GAMING OC 4G SALES KIT PRESENTATION (2017); RADEON SOFTWARE PRESENTATION (2017); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture*, AMD WHITE PAPER (2017); *AMD High-Performance Embedded GPUs*, AMD PRODUCT BRIEF (2017); *AMD Takes Embedded Applications to the Next Level with New GPUs*, AMD PRESS RELEASE (Sept. 27, 2016).

information and belief, AMD engaged in such inducement to promote the sales of the AMD '227 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '227 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '227 Patent, knowing that such use constitutes infringement of the '227 Patent.

652. The '227 Patent is well-known within the industry as demonstrated by multiple citations to the '227 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the '227 Patent without paying a reasonable royalty. AMD is infringing the '227 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

653. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '227 Patent. As a result of AMD's infringement of the '227 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD's infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

COUNT XVII
INFRINGEMENT OF U.S. PATENT NO. 6,421,090

654. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

655. AMD designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for interpolating a pixel during the interlacing of video signals.

656. AMD designs, makes, sells, offers to sell, imports, and/or uses AMD graphics cards, including the following: the Radeon RX 500 Series (Radeon RX 590, Radeon RX 580, Radeon RX 570, Radeon RX 560, Radeon RX 550, Radeon RX 540) and Radeon RX Vega Series (Radeon RX Vega 64, Radeon RX Vega 56, Radeon Vega 64 Liquid) (collectively, the "AMD '090 Product(s)").

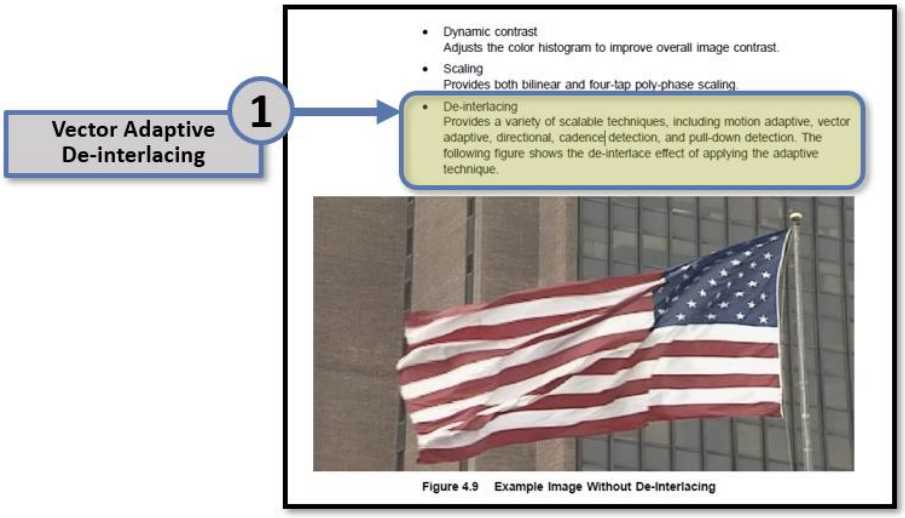
657. One or more AMD subsidiaries and/or affiliates use the AMD '090 Products in regular business operations.

658. One or more of the AMD '090 Products include technology for interpolating a pixel during the interlacing of a video signal. AMD documentation states that in HD post-processing "The video frames decoded from a video stream can go through post-processing to improve the image quality and correct visual artifacts from the source video introduced during production or distribution of the content (e.g. broadcasting or internet streaming). Main causes for these visual artifacts are video interlacing, resolution reduction and high compression or scaling." *AMD Unified Video Decoder (UVD),* AMD WHITE PAPER at 5 (June 2012) (emphasis added).

659. On information and belief, one or more of the AMD '090 Products process a video signal including at least two fields of interlaced scan lines, with each scan line containing a series of pixels having intensity values. Further, the AMD Product utilize a method of interpolating pixels during deinterlacing of a video signal. The interlaced video signal is comprised of two fields of interlaced scan signals. This format for the video signal that is received by the AMD Product is used to maximize the efficiency of transmitting data. The interlaced content received by the AMD Products is broken down into lines of even and odd lines which are combined to produce one frame. The AMD Products then use various algorithms to deinterlace the video signal including through generating a motion value representative of the motion between successive

frames about the pixel by segmenting an image into a plurality of multi-pixel segments and comparing the differences with respect to each segment in successive frames. For example, in the below excerpt from AMD documentation adaptive deinterlacing is used wherein motion between frames is detected in the interlaced video stream.

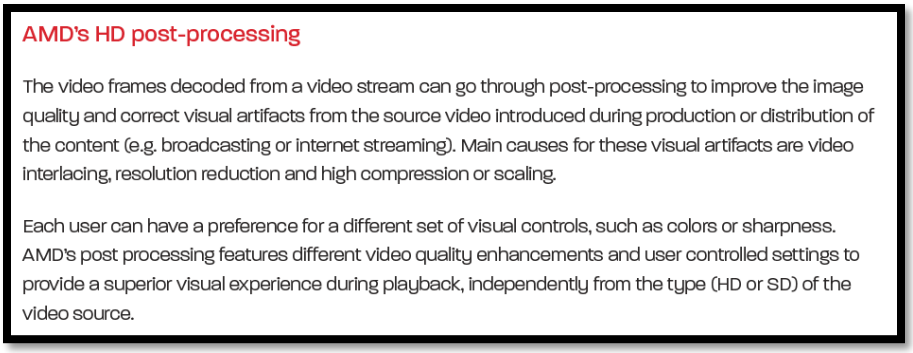
660. On information and belief, one or more of the AMD '090 Products generate a motion value representative of the motion between successive frames about the pixel. The AMD products in HD post-processing improve the quality of a video stream by taking the interlaced video signal and detecting an edge direction about the pixel in the interlaced video stream and then performing an edge adaptive interpolation at the pixel using the detected edge direction.



AMD Unified Video Decoder (UVD), AMD WHITE PAPER at 5 (June 2012).

661. On information and belief, one or more of the AMD '090 Products detect an edge direction about the pixel.

662. On information and belief, one or more of the AMD '090 Products perform a motion adaptive interpolation at the pixel.



AMD's HD post-processing

The video frames decoded from a video stream can go through post-processing to improve the image quality and correct visual artifacts from the source video introduced during production or distribution of the content (e.g. broadcasting or internet streaming). Main causes for these visual artifacts are video interlacing, resolution reduction and high compression or scaling.

Each user can have a preference for a different set of visual controls, such as colors or sharpness. AMD's post processing features different video quality enhancements and user controlled settings to provide a superior visual experience during playback, independently from the type (HD or SD) of the video source.

AMD MEDIA SDK USER GUIDE at § 4-7 (February 2014) (annotation added).

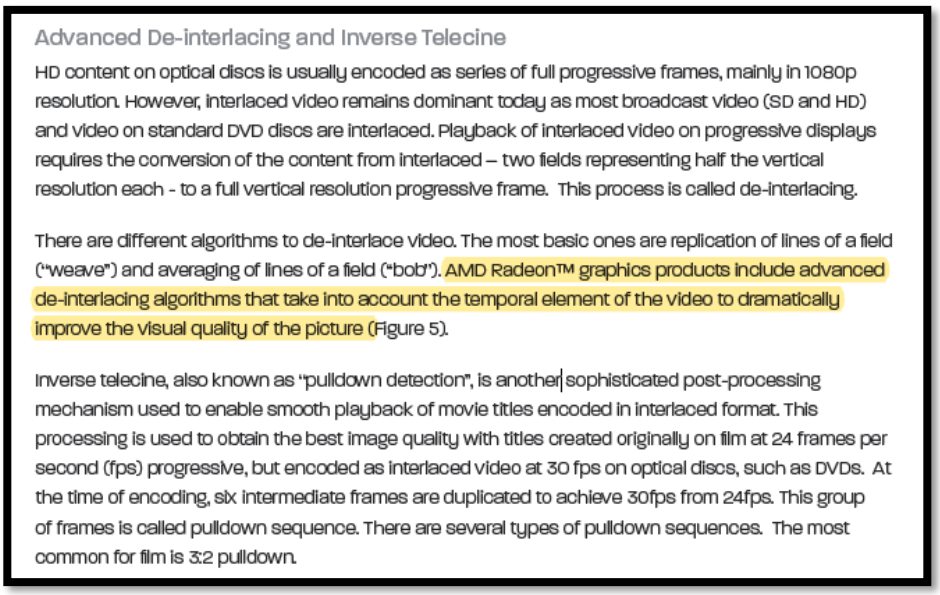
663. On information and belief, the AMD '090 Products are available to businesses and individuals throughout the United States.

664. On information and belief, the AMD '090 Products are provided to businesses and individuals located in Delaware.

665. On information and belief, AMD has directly infringed and continues to directly infringe the '090 Patent by, among other things, making, using, offering for sale, and/or selling technology for interpolating a pixel during the deinterlacing of a video signal, including but not limited to the AMD '090 Products.

666. On information and belief, the AMD '090 Products interpolate a pixel during the deinterlacing of video signals.

667. On information and belief, the AMD '090 Products process video signals that include at least two fields of interlaced scan lines. Each scan line in the video signal includes a series of pixels having respective intensity values.



Advanced De-interlacing and Inverse Telecine

HD content on optical discs is usually encoded as series of full progressive frames, mainly in 1080p resolution. However, interlaced video remains dominant today as most broadcast video (SD and HD) and video on standard DVD discs are interlaced. Playback of interlaced video on progressive displays requires the conversion of the content from interlaced – two fields representing half the vertical resolution each - to a full vertical resolution progressive frame. This process is called de-interlacing.

There are different algorithms to de-interlace video. The most basic ones are replication of lines of a field ("weave") and averaging of lines of a field ("bob"). AMD Radeon™ graphics products include advanced de-interlacing algorithms that take into account the temporal element of the video to dramatically improve the visual quality of the picture (Figure 5).

Inverse telecine, also known as "pulldown detection", is another sophisticated post-processing mechanism used to enable smooth playback of movie titles encoded in interlaced format. This processing is used to obtain the best image quality with titles created originally on film at 24 frames per second (fps) progressive, but encoded as interlaced video at 30 fps on optical discs, such as DVDs. At the time of encoding, six intermediate frames are duplicated to achieve 30fps from 24fps. This group of frames is called pulldown sequence. There are several types of pulldown sequences. The most common for film is 3:2 pulldown.

AMD Unified Video Decoder (UVD), AMD WHITE PAPER at 5 (July 2012) (emphasis added).

668. On information and belief, the AMD '090 Products generate a motion value representative of the motion between successive frames about the pixel by segmenting an image into a plurality of multi-pixel segments and compares the differences with respect to each segment in successive frames.

669. On information and belief, the AMD '090 Products detect an edge direction about the pixel.

670. On information and belief, the AMD '090 Products perform an edge adaptive interpolation at the pixel using the detected edge direction. For example, the AMD Products perform de-interlacing, wherein the difference in pixel values is considered across multiple lines and alternating frames (up to four frames) (using Pulldown detection on the interlaced video source), and then intelligently re-interpreted to produce smoother edges in interlaced video images.

671. On information and belief, the AMD '090 Products perform a motion adaptive interpolation at the pixel using the generated motion value by comparing segments of pixels about the pixel from at least three successive frames.

672. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the AMD '090 Products, AMD has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '090 Patent, including at least claim 5 pursuant to 35 U.S.C. § 271(a).

673. On information and belief, AMD also indirectly infringes the '090 Patent by actively inducing infringement under 35 USC § 271(b).

674. AMD has had knowledge of the '090 Patent since at least service of the Original Complaint in this matter or shortly thereafter, and on information and belief, AMD knew of the '090 Patent and knew of its infringement, including by way of this lawsuit.

675. On information and belief, AMD intended to induce patent infringement by third-party customers and users of the AMD '090 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. AMD specifically intended and was aware that the normal and customary use of the accused products would infringe the '090 Patent. AMD performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '090 Patent and with the knowledge that the induced acts would constitute infringement. For example, AMD provides the AMD '090 Products that have the capability of operating in a manner that infringe one or more of the claims of the '090 Patent, including at least claim 5, and AMD further provides documentation and training materials that cause customers and end users of the AMD '090 Products to utilize the products in a manner that directly infringe one or more claims of the '090 Patent.[40] By providing instruction and training to customers and end-users on how to use the AMD

[40] *See, e.g., AMD Unified Video Decoder (UVD),* AMD WHITE PAPER (June 2012); RADEON X1300 SERIES USER GUIDE (2005); RADEON RX 580 AND RX 570 REVIEWER'S GUIDE (2017); *Radeon's Next-Generation Vega Architecture,* AMD WHITE PAPER (2017).

‘090 Products in a manner that directly infringes one or more claims of the ‘090 Patent, including at least claim 5, AMD specifically intended to induce infringement of the ‘090 Patent. On information and belief, AMD engaged in such inducement to promote the sales of the AMD ‘090 Products, e.g., through AMD user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the ‘090 Patent. Accordingly, AMD has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the ‘090 Patent, knowing that such use constitutes infringement of the ‘090 Patent.

676. The ‘090 Patent is well-known within the industry as demonstrated by multiple citations to the ‘090 Patent in published patents and patent applications assigned to technology companies and academic institutions. AMD is utilizing the technology claimed in the ‘090 Patent without paying a reasonable royalty. AMD is infringing the ‘090 Patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

677. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ‘090 Patent.

678. As a result of AMD’s infringement of the ‘090 Patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for AMD’s infringement, but in no event less than a reasonable royalty for the use made of the invention by AMD together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Dynamic Data respectfully requests that this Court enter:

A. A judgment in favor of Dynamic Data that AMD has infringed, either literally and/or under the doctrine of equivalents, the '105, '073, '220, '257, '054, '918, '689, '177, '039, '112, '688, '529, '041, '450, '979, '227 and '090 Patents;

B. An award of damages resulting from AMD's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order finding that AMD's infringement was willful, wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate within the meaning of 35 U.S.C. § 284 and awarding to Dynamic Data enhanced damages.

D. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Dynamic Data its reasonable attorneys' fees against AMD.

E. Any and all other relief to which Dynamic Data may show themselves to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Dynamic Data Technologies, LLC requests a trial by jury of any issues so triable by right.

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