IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

DYNAMIC DATA TECHNOLOGIES, LLC, *Plaintiff,* v. MEDIATEK, INC., AND MEDIATEK USA, INC., *Defendants.*	Civil Action No. 18-cv-01906-CFC **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Dynamic Data Technologies, LLC ("Dynamic Data") brings this action and makes the following allegations of patent infringement relating to U.S. Patent Nos. 6,639,944 (the "'944 patent"); 6,760,376 (the "'376 patent"); 6,774,918 (the "'918 Patent"); 6,996,175 (the "'175 Patent"); 6,996,177 (the "'177 Patent"); 7,010,039 (the "'039 Patent"); 7,894,529 (the "'529 Patent"); 7,929,609 (the "'609 Patent"); 7,982,799 (the "'799 Patent"); 8,073,054 (the "'054 Patent"); 8,135,073 (the "'073 Patent"); 8,189,105 (the "'105 Patent"); and 8,311,112 (the "'112 Patent") (collectively, the "patents-in-suit"). Defendants MediaTek Inc. and MediaTek USA, Inc. (collectively, "MediaTek" or "Defendant") infringe each of the patents-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq*.

INTRODUCTION

1. Dynamic Data's portfolio of over 1,200 patent assets encompasses core technologies in the field of image and video processing. Dynamic Data's patents arose from the research and development efforts of Koninklijke Philips N.V. ("Philips"). Founded in 1891, for well over a century, Philips pioneered ground-breaking technologies, including compact audio cassettes, magnetic resonance imaging (MRI) machines, and compact discs.

2. To facilitate the licensing of Philips' foundational technology, Dynamic Data is pursuing remedies for infringement of its patents in venues throughout the world. Contemporaneous to the filing of this Complaint and complaints against other companies selling the technologies claimed by Dynamic Data's patent portfolio, Dynamic Data has filed patent enforcement actions against Apple Retail Germany B.V. & Co. KG, Apple Distribution International, and Apple, Inc. in Düsseldorf, Germany.[1] In the People's Republic of China, Dynamic Data has filed patent enforcement actions against Advanced Micro Devices (China) Co., Ltd.,[2] Apple Electronic Products Trading (Beijing) Co., Ltd.,[3] and Microsoft (China) Co., Ltd.[4]

3. MediaTek has cited the intellectual property assets in Dynamic Data's patent portfolio in 53 patents and published patent applications assigned to MediaTek.[5]

DYNAMIC DATA'S LANDMARK INVENTIONS

4. The groundbreaking inventions in image and video processing taught in the patents-in-suit were pioneered by Philips. Video and image processing were at the heart of Philips' business for over fifty years. In 1891, Philips, then known as Philips & Company, was founded in Eindhoven, Netherlands to manufacture carbon-filament lamps.[6] In the 1920s, Philips began to produce vacuum tubes and small radios, which would augur Philips' later entry into video and audio processing.

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[1] *See* In der Zivilsache Dynamic Data Technologies LLC gegen Apple Retail Germany B.V. & Co. KG u.a., AktNr: 010470-18.

[2] Asserting Patent No. ZL02817458.5.

[3] *See* Case Nos. (2019) Jing 73 Min Chu No. 235; (2019) Jing 73 Min Chu No. 234.

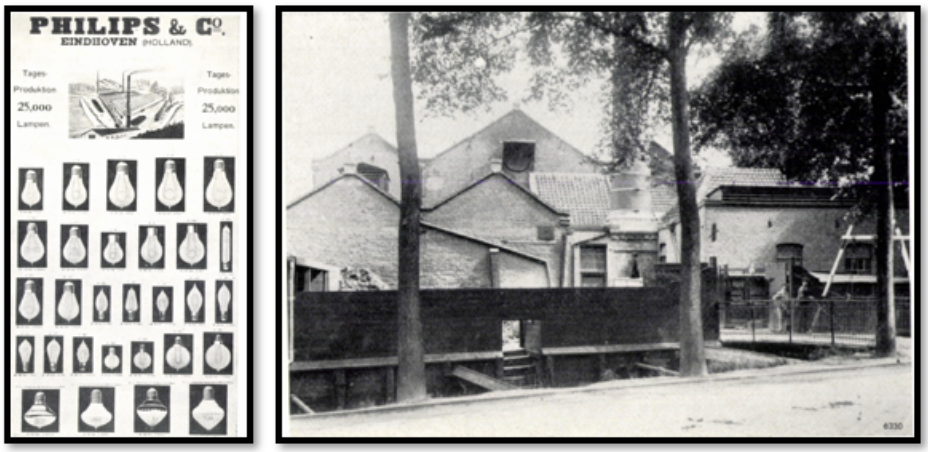
[4] *See* Case Nos. (2018) Su 01 Minchu 3500 ((2018)苏01民初3500号), (2018) Su 01 Minchu 3501 ((2018)苏01民初3501号), and (2018) Su 01 Minchu 3502 ((2018) 苏01民初3502号).

[5] *See e.g.,* U.S. Patent Nos. 7,397,973; 7,430,014; 7,453,524; 7,515,209; 7,605,872; 7,940,330; 7,940,331; 8,254,439; 8,446,523; 8,447,126; 8,643,776; 8,648,784; 8,861,882; 9,135,676; 9,277,167; 9,330,487; 9,563,960; 9,641,861; 9,838,701; and 9,917,988. These illustrative MediaTek patents are assigned to MStar Semiconductor, Inc. or MediaTek Inc.

[6] Gerard O'Regan, A BRIEF HISTORY OF COMPUTING at 99 (2012).

N.A. Halbertsma, *The Birth of a Lamp Factory In 1891*, PHILIPS TECHNICAL REVIEW, Vol. 23 at 230, 234 (1961).

5. In 1962, Philips introduced the first audio cassette tape.[7] A year later, Philips launched a small battery-powered audio tape recorder that used a cassette instead of a loose spool.[8] Philips C-cassette was later used as the first mass storage device for early personal computers in the 1970s and 1980s.



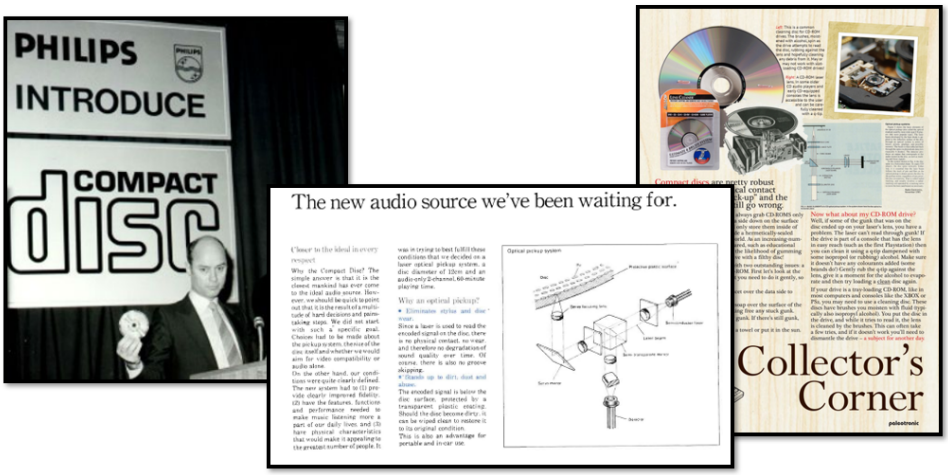
THE ROTARIAN MAGAZINE, Vol. 101 No. 6 at 70 (December 1962) (advertisement showing Philips Norelco device which used cassettes for recording audio for transcription); Fred Chandler, *European Mfrs. Bid For Market Share*, BILLBOARD MAGAZINE AT P-6 (April 8, 1967) (image of the Philips EL 3300 battery-operated tape recorder which was released in 1963); Jan Syrjala, *Car Stereo: How Does The Music Sound?,* N.Y. TIMES at 2-M (September 25, 1966) (showing Philips's

[7] Gerard O'Regan, PILLARS OF COMPUTING: A COMPENDIUM OF SELECT, PIVOTAL TECHNOLOGY FIRMS at 172 (2015) ("Philips invented the compact cassette for audio storage in 1962.")

[8] Anthony Pollard, GRAMOPHONE: THE FIRST 75 YEARS at 231 (1998).

Norelco Cassette "the Philips device has two tiny reels inside it, with the tape traveling from one to the other").

6. In 1971, Philips demonstrated the world's first videocassette records (VCR). A year later, Philips launched the world's first home video cassette recorder, the N1500. In 1982, Philips teamed with Sony to launch the Compact Disc; this format evolved into the DVD and later Blu-ray, which Philips launched with Sony in 1997 and 2006 respectively.



Hans Peek, Jan Bergmans, Jos Van Haaren, Frank Toolenaar, and Sorin Stan, ORIGINS AND SUCCESSORS OF THE COMPACT DISC: CONTRIBUTIONS OF PHILIPS TO OPTICAL STORAGE at 15 (2009) (showing image of Joop Sinjou of Philips introducing the compact disc in March 1979); Advertisements for Philip's Compact Disc Products (1982).

7. In the late 1990s and early 2000s, Philips pioneered the development of technologies for encoding and decoding of video and audio content. At the time most of the technologies claimed by the patents in Dynamic Data's portfolio were invented, Philips' subsidiary primarily responsible for Philips' work in this field, Philips Semiconductor was the world's sixth largest semiconductor company.[9] The video encoding technologies developed by Philips

[9] *Company News; Philips in $1 Billion Deal for VLSI Technology*, THE NEW YORK TIMES (May 4, 1999), *available at*: https://www.nytimes.com/1999/05/04/business/company-news-philips-in-1-billion-deal-for-vlsi-technology.html.

Semiconductor enable video streaming on set-top boxes, smartphones, popular gaming consoles, Internet-connected computers, and numerous other types of media streaming devices.

8. Philips Semiconductor dedicated significant research and development resources to advancing the technology of video compression and transmission by reducing file sizes and decreasing the processing resources required to transmit the data.[10] Philips Semiconductor was among the first companies aggressively driving innovation in the field of video processing:

> The late 1980s and early 1990s saw the announcement of several complex, programmable VSPs. Important examples include chips from Matsushita, NTT, Philips [Semiconductors], and NEC. All of these processors were high-performance parallel processors architected from the ground up for real-time video signal processing. . . . The Philips VSP-1 and NEC processor were probably the most heavily used of these chips.[11]

9. Starting in the 1960s Philips pioneered the development of audio and video technologies that would establish itself as a leader in the field that would later develop into the audio and video encoding fields. Continuing Philips' pioneering history in these fields, the patents-in-suit disclose cutting-edge video compression and transmission technologies.

DYNAMIC DATA'S PATENT PORTFOLIO

10. Dynamic Data's patent portfolio includes over 1,200 patent assets, with over 470 issued patents granted by patent offices around the world. Dynamic Data owns numerous patents issued by the United States Patent and Trademark Office, including each of the patents-in-suit, The State Intellectual Property Office of the People's Republic of China,[12] the European Patent

[10] HU, YU HEN, PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: ARCHITECTURE, PROGRAMMING, AND APPLICATIONS, at 190 (Dec. 6, 2001) ("Philips Semiconductors developed early dedicated video chips for specialized video processors.").

[11] *Id.* at 191.

[12] *See, e.g.,* CN100504925C; CN100438609C; CN1679052B; CN1333373C; CN1329870C; CN1303818C.

Office,[13] the German Patent and Trademark Office,[14] the Japan Patent Office,[15] and many other national patent offices.

11. Philips Semiconductor's pioneering work in the area of video processing and encoding has resulted in various inventions that are fundamental to today's video processing technologies. Dynamic Data is the owner by assignment of over 1,200 of these patent assets, which include over 470 patents issued by patent offices around the world.

12. Highlighting the importance of the patents-in-suit is the fact that the patents-in-suit have been cited by over 470 U.S. and international patents and patent applications by a wide variety of the largest companies operating in the field. For example, the patents-in-suit have been cited by companies such as:

- ***MediaTek Inc***.[16]
- Samsung Electronics Co., Ltd.[17]
- Qualcomm Inc.[18]
- Google LLC[19]
- Intel Corporation[20]
- Broadcom Corporation[21]
- Microsoft Corporation[22]
- Sony Corporation[23]

[13] *See, e.g.,* European Patent Nos. EP1032921B1; EP1650978B1; EP1213700B1; EP1520409B1.
[14] *See, e.g.,* German Patent Nos. DE60120762; DE50110537; DE60126151; DE60348978; DE602004049357.
[15] *See, e.g.,* Japanese Patent Nos. JP4583924B2; JP5059855B2; JP5153336B2; JP4637585B2.
[16] *See, e.g.*, U.S. Patent Nos. 7,397,973; 7,605,872; 8,179,984; 9,563,960; 9,917,988; and 9,641,861.
[17] *See, e.g.*, U.S. Patent Nos. 6,930,729; 7,911,537; 7,532,764; 8,605,790; and 8,095,887.
[18] *See, e.g.*, U.S. Patent Nos. 7,840,085; 8,649,437; 8,750,387; 8,918,533; 9,185,439; 9,209,934; 9,281,847; 9,319,448; 9,419,749; 9,843,844; 9,917,874; and 9,877,033.
[19] *See, e.g.*, U.S. Patent No. 8,787,454 and U.S. Patent Appl. No. 10/003,793.
[20] *See, e.g.*, U.S. Patent Nos. 7,554,559; 7,362,377; and 8,462,164.
[21] *See, e.g.*, U.S. Patent Nos. 8,325,273 and 9,377,987.
[22] *See, e.g.*, U.S. Patent Nos. 7,453,939; 7,670,227; 7,408,986; 7,421,129; 7,558,320; and 7,929,599.
[23] *See, e.g.*, U.S. Patent Nos. 7,218,354 and 8,174,615.

- Fujitsu Ltd.[24]
- Panasonic Corporation[25]
- Matsushita Electric Industrial Company Limited[26]

THE PARTIES

DYNAMIC DATA TECHNOLOGIES, LLC

13. Dynamic Data Technologies, LLC ("Dynamic Data" or "Plaintiff") is a limited liability company organized under the laws of the State of Delaware.

14. In an effort to obtain compensation for Philips' pioneering work in the fields of video data encoding, decoding, and transmission, Dynamic Data acquired the patents-in-suit along with the several hundred additional issued United States and international Patents.

15. Dynamic Data pursues the reasonable royalties owed for MediaTek's use of the inventions claimed in Dynamic Data's patent portfolio, which primarily arise from Philips' groundbreaking technology, both here in the United States and throughout the world.

MEDIATEK

16. MediaTek, Inc. is a corporation organized and existing under the laws of Taiwan, with its principal place of business located at No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu City 30078, Taiwan.

17. MediaTek USA, Inc. is a Delaware corporation with a place of business located at 120 Presidential Way, Woburn, MA 01801. MediaTek USA, Inc. may be served through its registered agent for service of process, The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801. MediaTek, Inc. is the parent of MediaTek USA, Inc. MediaTek, Inc. and MediaTek USA, Inc. are collectively referred to herein as "MediaTek."

[24] *See, e.g.*, U.S. Patent Nos. 7,092,032 and 8,290,308.
[25] *See, e.g.*, U.S. Patent Nos. 8,164,687 and 8,432,495.
[26] *See, e.g.*, U.S. Patent Nos. 7,362,378 and 7,423,961.

JURISDICTION AND VENUE

18. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

19. This Court has personal jurisdiction over MediaTek in this action because MediaTek has committed acts within Delaware giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over MediaTek would not offend traditional notions of fair play and substantial justice. Defendant MediaTek, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patents-in-suit. Moreover, MediaTek actively directs its activities to customers located in Delaware.

20. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b).

THE ASSERTED PATENTS

U.S. PATENT NO. 6,639,944

21. U.S. Patent No. 6,639,944 entitled, *Sub-Pixel Accurate Motion Vector Estimation and Compensated Interpolation*, was filed on April 26, 2000, and claims priority to April 26, 1999. Dynamic Data is the owner by assignment of all right, title, and interest in the '944 patent. A true and correct copy of the '944 patent is attached hereto as Exhibit 1.

22. The '944 patent discloses novel methods and systems for sub-pixel accurate motion vector estimation and motion-compensated interpolation or prediction.

23. The inventions disclosed in the '944 patent enables higher accuracy motion estimation at a lower cost through improvements in motion vector estimation and motion-compensated interpolation.

24. The ‘944 patent discloses a method of generating an intermediate image using sub-pixel accurate motion vectors having vector components that may have non-integer values, from first and second images having a given mutual temporal distance, the intermediate image being at a fractional distance from said first image, said fractional distance being a fraction of said given mutual temporal distance.

25. The ‘944 patent discloses a method that includes deriving first and second vectors from said sub-pixel accurate motion vectors.

26. The ‘944 patent discloses a method that includes generating an intermediate image by combining first positions in a first image shifted over first vectors and second positions in said second image shifted over second vectors.

27. The ‘944 patent discloses a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by multiplying the vector components of the sub-pixel accurate motion vectors by a fraction to obtain fractional vector components.

28. The ‘944 patent discloses a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by rounding the fractional vector components to obtain vector components of the first vectors, which have only integer vector components.

29. The ‘944 patent discloses a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by subtracting the first vector from the candidate vector to obtain the second vector, whereby the second vectors have vector components that, depending on the candidate vector and the fraction, may have non-integer values.

30. The ‘944 patent Family has been cited by 23 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘944

patent Family as relevant prior art: Himax Media Solutions, Inc.; Cyberlink Corp.; and Marvell International Ltd.

U.S. PATENT NO. 6,760,376

31. U.S. Patent No. 6,760,376 entitled, *Motion Compensated Upconversion For Video Scan Rate Conversion*, was filed on November 6, 2000. The '376 patent is subject to a 35 U.S.C. § 154(b) term extension of 697 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '376 patent. A true and correct copy of the '376 patent is attached hereto as Exhibit 2.

32. The '376 patent discloses novel methods and systems for motion compensated upconversion in a video image that uses motion compensation to generate an interpolated video field using motion vectors.

33. The inventions disclosed in the '376 patent provide a sharp video image by comparing a calculated correlation value of pixels with a threshold value.

34. The '376 patent discloses technologies that improve video image quality by selecting a motion compensated pixel that will provide a sharp video image by comparing a calculated correlation value of pixels with a threshold value.

35. The '376 patent discloses a method of motion compensation for use in a video image upconversion unit of the type that uses motion compensation to generate an interpolated field using motion vectors.

36. The '376 patent discloses a method of motion compensation that includes calculating a correlation value from the values of causal neighbor pixels of a generated field and from the values of corresponding neighbor pixels of a next field.

37. The '376 patent discloses a method of motion compensation that includes comparing the correlation value with a threshold value.

38. The ‘376 patent discloses a method of motion compensation that includes setting the value of a pixel to be created within the generated field to be equal to the value of a corresponding pixel of the next field if the correlation value is less than the threshold value.

39. The ‘376 patent Family has been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘376 patent Family as relevant prior art: Samsung Electronics Co., Ltd.; Blip X Ltd.; Himax Technologies Limited; and Snell Ltd.

U.S. PATENT NO. 6,774,918

40. U.S. Patent No. 6,774,918 entitled, *Video Overlay Processor with Reduced Memory and Bus Performance Requirements*, was filed on June 28, 2000. The ‘918 Patent is subject to a 35 U.S.C. § 154(b) term extension of 591 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘918 Patent. A true and correct copy of the ‘918 Patent is attached hereto as Exhibit 3.

41. The ‘918 Patent claims specific methods and systems for providing an overlay such as a cursor in an on-screen display in a consumer electronic device. On-screen display (OSD) data for generating an image on a display device are downloaded to an OSD unit on an integrated circuit.

42. The ‘918 Patent discloses downloading on-screen display (OSD) data for generating an image on a display device.

43. The ‘918 Patent further discloses downloading the on-screen display (OSD) data in segments separated by gaps.

44. The ‘918 Patent further discloses, during a gap in downloading the on-screen display data, downloading an amount of overlay data for generating an overlay on the image

generated on a display device.

45. Further, the '918 Patent discloses that the overlay data downloaded during a gap comprises a portion of the overlay data.

46. The inventions disclosed in the '918 Patent improves the operation and efficiency of computer components because only a portion of the overlay data is downloaded during each burst gap, thus reducing the amount of memory needed to store the overlay data. The inventions disclosed in the '918 Patent further eliminate the requirement that on-chip memory be large enough to hold the data needed for an entire overlay. Instead, only one line or a part of one line of the overlay needs to be stored on-chip.

47. The '918 Patent claims a technical solution to a problem unique to video processing.

48. The '918 Patent Family has been cited by several United States patents and patent applications as relevant prior art. Specifically, patents issued to Realtek Semiconductor Corp., Samsung Electronics Co., Ltd., and Thomson Licensing SA have all cited the '918 Patent Family as relevant prior art.

U.S. PATENT NO. 6,996,175

49. U.S. Patent No. 6,996,175 entitled, *Motion Vector Estimation*, was filed on December 7, 1999. The '175 Patent claims priority pursuant to 35 U.S.C. § 119(a)-(d) to European Patent Applications 99201556.0 and 98204149.3. *See Notice of Allowance* at 1, U.S. PATENT APPL. SER. NO. 09/455,662 (June 3, 2005) (identifying the claim or priority under 35 U.S.C. § 119(a)-(d)). The '175 Patent has a term which ends "twenty years from the filing date of the application in the United States [December 7, 1999]." MANUAL OF PATENT EXAMINING PROCEDURE ("MPEP") § 2701.III.

50. Dynamic Data is the owner by assignment of all right, title, and interest in the '175 patent. A true and correct copy of the '175 Patent is attached hereto as Exhibit 4.

51. The '175 Patent discloses novel methods and systems for recursive motion vector estimation. The inventions disclosed in the '175 Patent enable methods and systems where candidate vectors are generated from stored vectors and one of the candidate vectors is selected (the selected vector). The selected vector is then used to generate several test vectors. Finally, one of the test vectors is used to generate an output vector.

52. The inventions disclosed in the '175 Patent teach a device that performs motion estimation to significantly improve the performance of the device with respect to (1) coding efficiency, and (2) the perceptual quality of the coded pictures. Further, the '175 Patent discloses a system wherein recursive motion vector estimation keeps the computation load in a reasonably low range.

53. In one embodiment of the '175 Patent, an improvement to motion estimation is performed wherein a difference between the output and the input of the enhancement module gives a local information on the trend of the motion.

54. The inventions disclosed in the '175 Patent enable post processing to be done inside the recursion loop of any recursive motion estimation algorithm instead of outside the recursion loop, the convergence of the recursive motion estimation algorithm is speeded up.

55. The '175 Patent, in one embodiment, discloses a method of displaying information on a display device wherein being switched from the first one of the services to the second one of the services, with the data-element and the second data-element being mutually semantically related and a second step of rendering to calculate the output image to be displayed on the display device, on the basis of the second data-element selected by the filter is performed.

56. The ‘175 Patent Family has been cited by 21 patents and patent applications as relevant prior art. Specifically, patents issued to Sony Corporation, Samsung Electronics Co., Ltd., and International Business Machines have all cited the ‘175 Patent Family as relevant prior art.

U.S. PATENT NO. 6,996,177

57. U.S. Patent No. 6,996,177 entitled, *Motion Estimation*, was filed on July 24, 2000, and claims priority to August 22, 1999. The ‘177 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,103 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘177 Patent. A true and correct copy of the ‘177 Patent is attached hereto as Exhibit 5.

58. The ‘177 Patent claims specific methods and devices for motion estimation and motion-compensated picture signal processing.

59. The ‘177 Patent discloses a motion vector estimation method and device that carries out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors.

60. The ‘177 Patent discloses a motion vector estimation method and device that determines at least a most frequently occurring block-based motion vector.

61. The ‘177 Patent discloses a motion vector estimation method and device that carries out a global motion vector estimation process using at least the most frequently occurring block-based motion vector to obtain a global motion vector.

62. The ‘177 Patent discloses a motion vector estimation method and device that applies the global motion vector as a candidate vector to the block-based motion vector estimation process.

63. The inventions disclosed in the ‘177 Patent improve the operation of the computer components necessary to the performance of picture signal processing by reducing the load on the central processing unit.

64. The '177 Patent Family has been cited by 16 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '177 Patent Family as relevant prior art:

- Qualcomm Incorporated
- LG Electronics
- Microsoft Corporation
- Samsung Electronics Co., Ltd.
- VIXS Systems Incorporated
- General Instrument Corporation

U.S. PATENT NO. 7,010,039

65. U.S. Patent No. 7,010,039 entitled, *Motion Estimator for Reduced Halos in MC Up-Conversion*, was filed on May 15, 2001, and claims priority to May 18, 2000. The '039 Patent is subject to a 35 U.S.C. § 154(b) term extension of 768 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '039 Patent. A true and correct copy of the '039 Patent is attached hereto as Exhibit 6.

66. The '039 Patent claims specific methods and apparatuses detecting motion at a temporal intermediate position between previous and next images. The inventions disclosed in the '039 Patent solve a problem wherein an estimator estimating motion between two successive pictures from a video sequence cannot perform well in areas where covering or uncovering occurs.

67. The '039 Patent solves this problem by carrying out the optimization at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

68. The '039 Patent discloses a method and apparatus for detecting motion at a temporal intermediate position between previous and next images.

69. The '039 Patent discloses the use of a criterion function for selecting and optimizing candidate vectors.

70. The ‘039 Patent further discloses a criterion function that depends on data from both previous and next images and in which the optimizing is carried out at the temporal intermediate position in non-covering and non-uncovering areas, characterized in that the optimizing is carried out at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

71. The ‘039 Patent Family has been cited by 30 United States and International patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘039 Patent Family as relevant prior art:

- Qualcomm Incorporated
- Panasonic Corporation
- Samsung Electronics Co., Ltd.
- Matsushita Electric Industrial Co., Ltd.
- Sharp Kabushiki Kaisha
- Integrated Device Technology, Inc.
- Zoran Corporation

U.S. PATENT NO. 7,894,529

72. U.S. Patent No. 7,894,529 entitled, *Method And Device For Determining Motion Vectors*, was filed on June 1, 2006, and claims priority to June 3, 2005. The ‘529 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,301 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘529 Patent. A true and correct copy of the ‘529 Patent is attached hereto as Exhibit 7.

73. The ‘529 Patent discloses novel methods and apparatuses for determining motion vectors that are each assigned to individual image regions.

74. The inventions disclosed in the ‘529 Patent enable an increase in the resolution of video and image signals during the motion estimation process.

75. The ‘529 Patent discloses a method for determining motion vectors which are assigned to individual image regions of an image.

76. The ‘529 Patent discloses a method wherein an image is subdivided into a number of image blocks, and a motion estimation technique is implemented to assign at least one motion vector to each of the image blocks where a modified motion vector is generated for at least a first image block.

77. The ‘529 Patent discloses a method that determines at least a second image block through which the motion vector assigned to the first image block at least partially passes.

78. The ‘529 Patent discloses a method that generates the modified motion vector as a function of a motion vector assigned to at least the second image block.

79. The ‘529 Patent discloses a method that assigns the modified motion vector as the motion vector to the first image block.

80. The ‘529 Patent Family has been cited by multiple patents and patent applications as relevant prior art. Specifically, patents issued to Fujifilm Corp., and Samsung Electronics Co., Ltd. have cited the ‘529 Patent Family as relevant prior art.

U.S. PATENT NO. 7,929,609

81. U.S. Patent No. 7,929,609 entitled, *Motion Estimation And/Or Compensation*, was filed on September 9, 2002, and claims priority to September 12, 2001. The ‘609 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,242 days. Dynamic Data is the owner by assignment of all right, title, and interest in the ‘609 Patent. A true and correct copy of the ‘609 Patent is attached hereto as Exhibit 8.

82. The ‘609 Patent discloses novel methods and systems for compensation and estimation of motion in video images.

83. The inventions disclosed in the '609 Patent improve video signal processing functionality used in motion compensated prediction in encoding and compressing of digital video signals, motion compensated filtering in noise reduction, motion compensated interpolation in video format conversion, and motion compensated de-interlacing of interlaced video signals, among other video processing functionalities.

84. The '609 Patent discloses a method of estimating or compensating motion in video images that includes using a video processor to select an image segment of a given video image.

85. The '609 Patent discloses a method of estimating or compensating motion in video images that includes using the video processor to define an asymmetric search area surrounding the image segment based on ranges of possible motion vectors for the image segment.

86. The '609 Patent discloses a method of estimating or compensating motion in video images that includes using the video processor to retrieve image data related to the asymmetric search area.

87. The '609 Patent discloses a method of estimating or compensating motion in video images that includes a video processor that defines the asymmetric search area to have a center offset from a center of the image segment, the offset thereby defining asymmetry of the asymmetric search area, and statistically determines from an average vector of motion vectors established for one or more previous images.

88. The '609 Patent Family has been cited by 64 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '609 Patent Family as relevant prior art:

- Canon Inc.
- Xaxis Holdings, Inc.
- Samsung Electronics Co., Ltd.
- Electronics and Telecommunications Research Institute

- Broadcom Limited
- Sony Corporation
- Rakuten, Inc.
- Elan Microelectronics Corp.
- Garmin Ltd.
- State University System of Florida
- Ricoh Company Ltd.
- Intel Corporation
- Novatek Microelectronics Corp.
- Pearl River Hydraulic Research Institute

U.S. PATENT NO. 7,982,799

89. U.S. Patent No. 7,982,799 entitled, *Method And Device For Interpolation Of An Image Information Value For Pixel Of An Interline*, was filed on December 29, 2006, and claims priority to December 30, 2005. The '799 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,233 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '799 Patent. A true and correct copy of the '799 Patent is attached hereto as Exhibit 9.

90. The '799 Patent discloses novel methods and systems for interpolating an image information value for a pixel of an interline situated between two original image lines in an image.

91. The inventions disclosed in the '799 Patent reduce or prevent ambiguities in the determination of an optimal image direction by adding a single direction values of several adjacent pixels.

92. The '799 Patent discloses a method for interpolation of an image information value for a pixel of an interline that includes selecting from a number of image directions, to each of which a direction quality value is assigned, a direction of interpolation by comparing the direction quality values.

93. The '799 Patent discloses a method for interpolation of an image information value for a pixel of an interline that includes determining the image information value being interpolated

in dependence on image information values assigned to pixels lying adjacent to the pixel being interpolated in the direction of interpolation.

94. The '799 Patent discloses a method for interpolation of an image information value for a pixel of an interline that includes ascertaining a direction quality value for an image direction by selecting a pixel group having at least two pixels.

95. The '799 Patent discloses a method for interpolation of an image information value for a pixel of an interline that includes ascertaining a direction quality value for an image direction by determining a single direction quality value for each pixel of the pixel group, the single direction quality value being dependent on image information values assigned to image regions lying adjacent to the particular pixel of the group in the image direction.

96. The '799 Patent discloses a method for interpolation of an image information value for a pixel of an interline that includes ascertaining a direction quality value for an image direction by creating the direction quality value as a function of the single direction quality values of the pixel group.

97. The '799 Patent Family has been cited by several patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '799 Patent Family as relevant prior art: NEC Corporation; Intel Corporation; Qualcomm Inc.; ***MediaTek, Inc.;*** and Zoran Corporation.

U.S. PATENT NO. 8,073,054

98. U.S. Patent No. 8,073,054 entitled, *Unit For And Method Of Estimating A Current Motion Vector*, was filed on December 12, 2002, and claims priority to January 17, 2002. The '054 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,162 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '054 Patent. A true and correct copy of the '054 Patent is attached hereto as Exhibit 10.

99. The ‘054 Patent discloses novel methods and apparatuses for estimating a current motion vector for a group of pixels of an image.

100. The inventions disclosed in the ‘054 Patent enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

101. The ‘054 Patent discloses a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

102. The ‘054 Patent discloses a motion estimation unit comprising a match error unit for calculating match errors of respective candidate motion vectors.

103. The ‘054 Patent discloses a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

104. The ‘054 Patent discloses a motion estimation unit that calculates the further candidate motion vector on the basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different.

105. The ‘054 Patent discloses a motion estimation unit that arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and

the first motion vector.

106. The '054 Patent Family has been cited by 14 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '054 Patent Family as relevant prior art:

- Canon Inc.
- Huawei Technologies, Ltd.
- Imagination Technologies Ltd.
- ***MediaTek Inc.***
- Panasonic Corp.
- Samsung Electronics Co., Ltd.
- Siemens Healthcare GmbH
- Tencent Technology (Shenzhen) Co., Ltd.

U.S. PATENT NO. 8,135,073

107. U.S. Patent No. 8,135,073 entitled, *Enhancing Video Images Depending on Prior Image Enhancements*, was filed on December 12, 2003, and claims priority to December 19, 2002. The '073 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1,799 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '073 Patent. A true and correct copy of the '073 Patent is attached hereto as Exhibit 11.

108. The '073 Patent discloses novel methods and systems for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

109. The inventions disclosed in the '073 Patent reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

110. Accordingly, the technologies disclosed in the '073 Patent enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

111. The ‘073 Patent discloses a video decoder comprising an input for receiving a video stream containing encoded frame-based video information including an encoded first frame and an encoded second frame.

112. The ‘073 Patent discloses a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame.

113. The ‘073 Patent discloses a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers the motion vectors for the second frame.

114. The ‘073 Patent discloses a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

115. The ‘073 Patent Family has been cited by 36 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the ‘073 Patent Family as relevant prior art:

- Canon Inc.
- Microsoft Corporation
- International Business Machines Corporation
- Qualcomm Inc.
- Digital Fountain Incorporated
- Samsung Electronics Co., Ltd.
- SK Planet Co. Ltd.

U.S. PATENT NO. 8,189,105

116. U.S. Patent No. 8,189,105 entitled, *Systems and Methods of Motion and Edge Adaptive Processing Including Motion Compensation Features*, was filed on October 17, 2007. The '105 Patent is subject to a 35 U.S.C. § 154(b) term extension of 1258 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '105 Patent. A true and correct copy of the '105 Patent is attached hereto as Exhibit 12.

117. The '105 Patent discloses novel systems and methods for processing pixel information based on received motion and edge data.

118. The '105 Patent further discloses the use of a blending component (implemented by hardware, software, firmware, combinations thereof, etc.) that implements interpolating intensity of the pixel to equal to the first intensity estimate if motion reliability data is below a threshold.

119. The '105 Patent in one embodiment teaches using segmentation to average four contiguous pixels into one averaged pixel segment during motion detection.

120. The '105 Patent Family has been cited by 46 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '105 Patent Family as relevant prior art:

- Flextronics Ap, LLC
- Qingdao Hisense Electronics Co., Ltd.
- Hon Hai Precision Industry Co., Ltd.
- Intel Corporation
- Sony Corporation
- Fujitsu Corporation
- Himax Media Solutions, Inc.
- Ati Technologies Ulc
- Sharp Kabushiki Kaisha
- Xerox Corporation

U.S. PATENT NO. 8,311,112

121. U.S. Patent No. 8,311,112 entitled, *System And Method For Video Compression Using Predictive Coding*, was filed on December 31, 2008. The '112 Patent is subject to a 35 U.S.C. § 154(b) term extension of 847 days. Dynamic Data is the owner by assignment of all right, title, and interest in the '112 Patent. A true and correct copy of the '112 Patent is attached hereto as Exhibit 13.

122. The '112 Patent discloses novel methods and systems for video compression.

123. The '112 Patent discloses novel technologies for video compression that perform predictive coding on a macroblock of a video frame such that a set of pixels of the macroblock is coded using some of the pixels from the same video frame as reference pixels and the rest of the macroblock is coded using reference pixels from at least one other video frame.

124. The '112 Patent discloses a system for video compression comprising an intra-frame coding unit configured to perform predictive coding on a set of pixels of a macroblock of pixels using a first group of reference pixels, the macroblock of pixels and the first group of reference pixels being from a video frame.

125. The '112 Patent discloses a system for video compression comprising an inter-frame coding unit configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels, the second group of reference pixels being from at least one other video frame.

126. The '112 Patent Family has been cited by 10 patents and patent applications as relevant prior art. Specifically, patents issued to the following companies have cited the '112 Patent Family as relevant prior art:

- British Broadcasting Corporation
- Google LLC

- Megachips Corp.
- Olympus Corp.
- Samsung Electronics Co., Ltd.
- Sony Corporation
- Toshiba Corporation

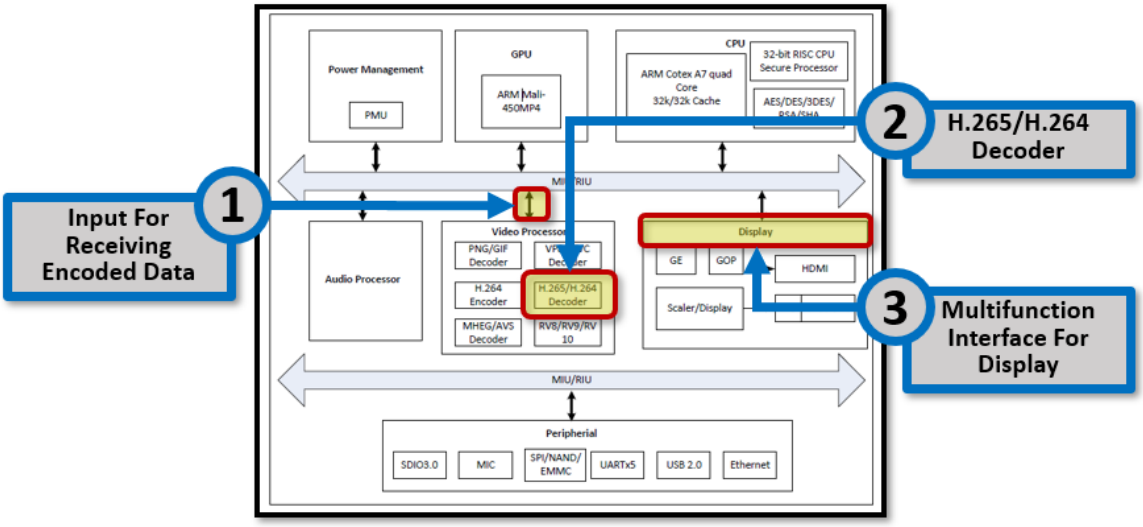
COUNT I
INFRINGEMENT OF U.S. PATENT NO. 6,639,944

127. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

128. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for sub-pixel accurate motion vector estimation and motion-compensated interpolation or prediction.

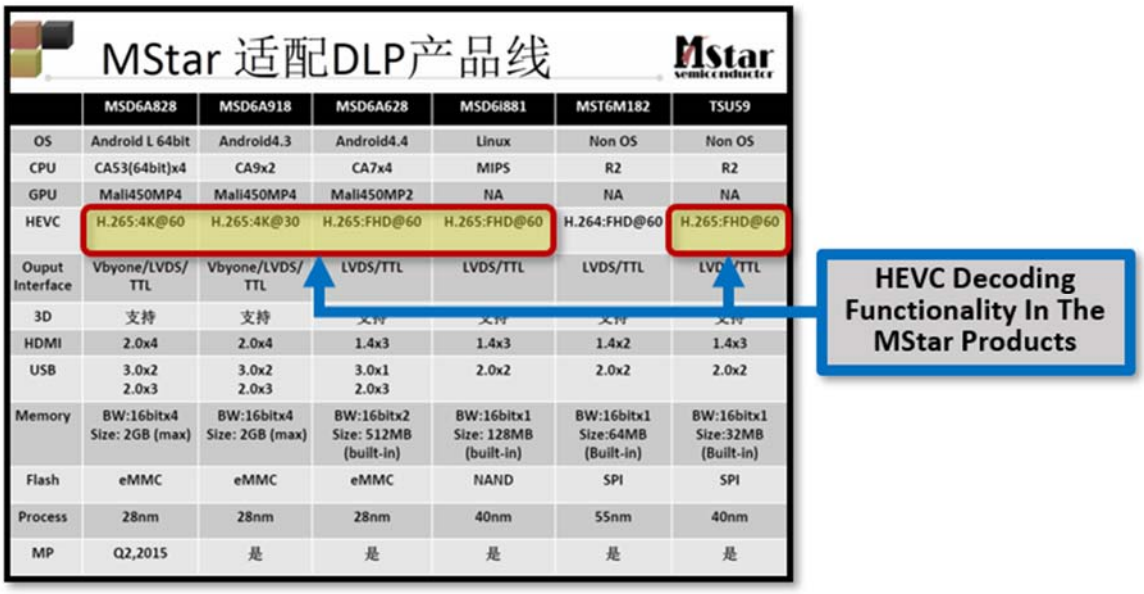
129. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that contain sub-pixel accurate motion vector functionality, including but not limited to MStar System on Chip ("SoC") Products, including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MediaTek '944 Product(s)").

130. The MediaTek '944 Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

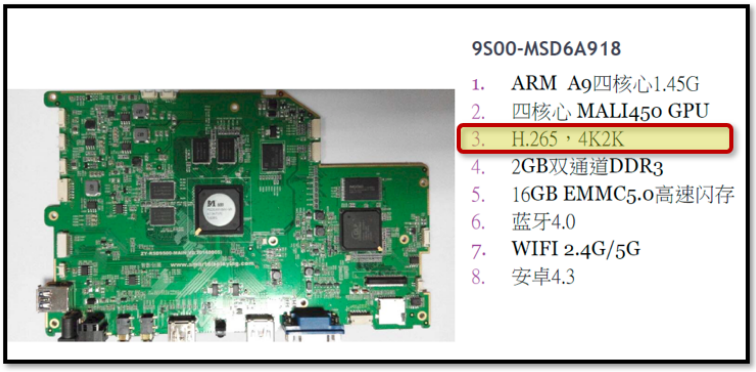
131. Documentation regarding the MediaTek '944 Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MediaTek '944 Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



	MSD6A828	MSD6A918	MSD6A628	MSD6i881	MST6M182	TSU59
OS	Android L 64bit	Android4.3	Android4.4	Linux	Non OS	Non OS
CPU	CA53(64bit)x4	CA9x2	CA7x4	MIPS	R2	R2
GPU	Mali450MP4	Mali450MP4	Mali450MP2	NA	NA	NA
HEVC	H.265:4K@60	H.265:4K@30	H.265:FHD@60	H.265:FHD@60	H.264:FHD@60	H.265:FHD@60
Ouput Interface	Vbyone/LVDS/ TTL	Vbyone/LVDS/ TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL
3D	支持	支持	支持	支持	支持	支持
HDMI	2.0x4	2.0x4	1.4x3	1.4x3	1.4x2	1.4x3
USB	3.0x2 2.0x3	3.0x2 2.0x3	3.0x1 2.0x3	2.0x2	2.0x2	2.0x2
Memory	BW:16bitx4 Size: 2GB (max)	BW:16bitx4 Size: 2GB (max)	BW:16bitx2 Size: 512MB (built-in)	BW:16bitx1 Size: 128MB (built-in)	BW:16bitx1 Size:64MB (Built-in)	BW:16bitx1 Size:32MB (Built-in)
Flash	eMMC	eMMC	eMMC	NAND	SPI	SPI
Process	28nm	28nm	28nm	40nm	55nm	40nm
MP	Q2,2015	是	是	是	是	是

MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

132. The MediaTek '944 Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MediaTek '944 Products that contain a decoder that conforms to the H.265 standard.



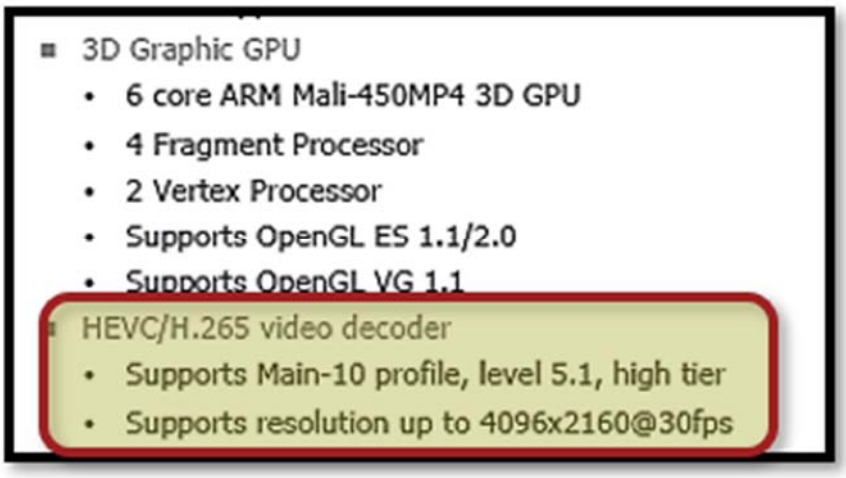
Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product Contains A Decoder Complaint With The H.265 Standard).

133. Datasheets from MediaTek also establish that the accused MediaTek '944 Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states "all in one 的SOC 芯片，芯片主要功能规格参数如下： 支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60."[27]

[27] *Translated Text*: "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."

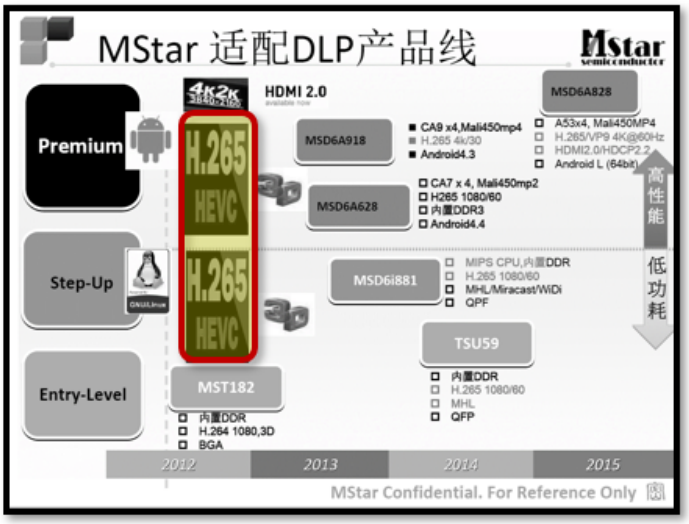
MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

134. Similarly, the datasheet for the MSO9280MC Product identifies that it contains an HEVC H.265 decoder.



MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added).

135. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MediaTek '944 Products.



MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

136. Documentation from MediaTek customers such as TCL that incorporate the accused MediaTek '944 Products into devices such as televisions also identifies that the accused chips contain an H.265 decoder.

类别	项目	L55H8800-CUD
输入和输出	ATV/DTV(DVB-C/DTMB) (PAL D/K I B/G)	✓
	HDMI (480i/p,576i/p,720p up to1080i/p,4K2K,with HDCP)	3 路，HDMI2 与 MHL 复用 支持 4K2K@30Hz 支持 H.265 格式
	VGA	无
	VGA/DVI audio	与 YPbPr 共用
	YPbPr (可支持 480i 到 1080p)	无
	SPDIF output	与AVout共用

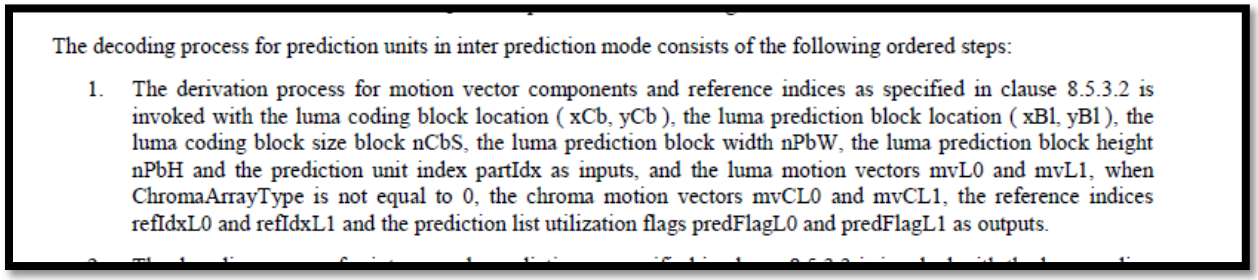
TCL PRODUCT BRIEF: MS918 机芯手册V1.0 at 35 (March 18, 2015) (annotation added) (showing that the MS918 chip from MStar contains a H.265 compliant decoder).

137. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '944 Products in regular business operations.

138. The MediaTek '944 Products perform a method of generating an intermediate image using sub-pixel accurate motion vectors having vector components that may have non-

integer values, from first and second images having a given mutual temporal distance, the intermediate image being at a fractional distance from said first image, said fractional distance being a fraction of said given mutual temporal distance.

139. The MediaTek '944 Products comply with the HEVC standard, which requires determining motion vectors assigned to individual image regions of an image.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

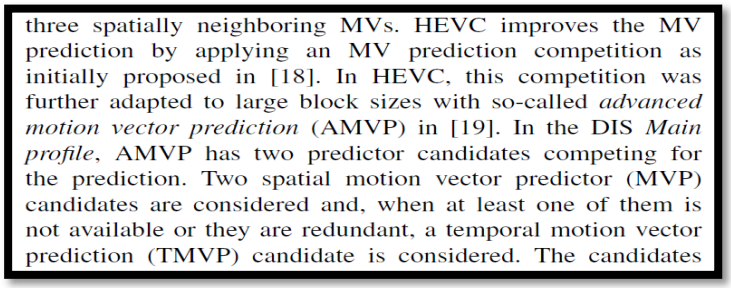
140. The MediaTek '944 Products perform a method that includes deriving first and second vectors from said sub-pixel accurate motion vectors.

141. The MediaTek '944 Products perform a method that includes generating an intermediate image by combining first positions in a first image shifted over first vectors and second positions in said second image shifted over second vectors.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess, *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

142. The MediaTek '944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by multiplying the vector components of the sub-pixel accurate motion vectors by a fraction to obtain fractional vector components.



three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC,* IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. *22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

143. In AMVP, the motion vector selection process is composed of two steps wherein the candidate motion vectors are constructed into an index and then the motion vectors are compared. "In AMVP, the motion vector selection process is composed by two steps in encoder implementation. The first step is the motion vector candidate set construction process and the second step is the best motion vector selection step. In the first step, the motion vector candidate set is organized by selecting the motion vectors spatially and temporally." Gwo-Long Li, Chuen-Ching Wang, and Kuang-Hung Chiang, *An Efficient Motion Vector Prediction Method for Avoiding AMVP Data Dependency For HEVC*, 2014 IEEE INTERNATIONAL CONFERENCE ON ACOUSTIC, SPEECH AND SIGNAL PROCESSING (ICASSP) at 7412-13 (2014).

144. The MediaTek '944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by rounding the fractional vector components to obtain vector components of the first vectors, which have only integer vector components.

> Using a translational motion model, the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy could be of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, i.e. motion vectors and reference indices, are further referred to as motion data.

Benjamin Bross, *Inter-Picture Prediction In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 114 (September 2014) (emphasis added).

145. The MediaTek '944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by subtracting the first vector from the candidate vector to obtain the second vector, whereby the second vectors have vector components that, depending on the candidate vector and the fraction, may have non-integer values.

146. The MediaTek '944 Products contain functionality for motion compensation where two or more motion vectors can be applied. Further, one or two motion vectors can be applied to the image processing process. The application of the motion vectors leads to uni-predictive or bi-predictive coding, respectively, where bi-predictive coding uses an averaged result of two predictions to form the final prediction.

Summary

Recommendation ITU-T H.265 | International Standard ISO/IEC 23008-2 represents an evolution of the existing video coding Recommendations (ITU-T H.261, ITU-T H.262, ITU-T H.263 and ITU-T H.264) and was developed in response to the growing need for higher compression of moving pictures for various applications such as Internet streaming, communication, videoconferencing, digital storage media and television broadcasting. It is also designed to enable the use of the coded video representation in a flexible manner for a wide variety of network environments. The use of this Recommendation | International Standard allows motion video to be manipulated as a form of computer data and to be stored on various storage media, transmitted and received over existing and future networks and distributed on existing and future broadcasting channels.

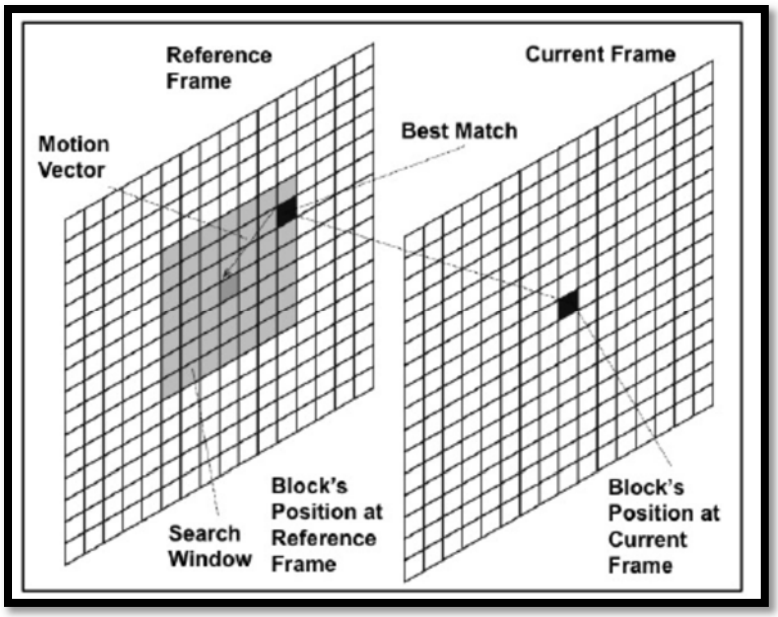
Series H: Audiovisual and Multimedia Systems- Infrastructure of Audiovisual Services – Coding of Moving Video, INTERNATIONAL TELECOMMUNICATIONS UNIONS - TU-T H.265, V.5 at I (February 2018).

147. The following excerpt from a book describes that the motion estimation is done through PU matching method and that the MV represents the displacement between the current PU in the current frame and the matching PU in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, High Efficiency Video Coding (HEVC) at 347 (September 2014) (emphasis added).

148. The following exemplary drawings reflect that the corresponding image segment of a reference picture is co-located with the current image segment of a current picture.



R.C. LINS, *et al., A Faster Pixel-Decimation Method for Block Motion Estimation in H.264/AVC*, PUBLISHED IN TEND. MAT. APL. COMPUT., VOL. 15, NO. 1 at 120 (2014), *available at*: http://www.scielo.br/scielo.php?script=sci_arttext&pid=S2179-84512014000100010.

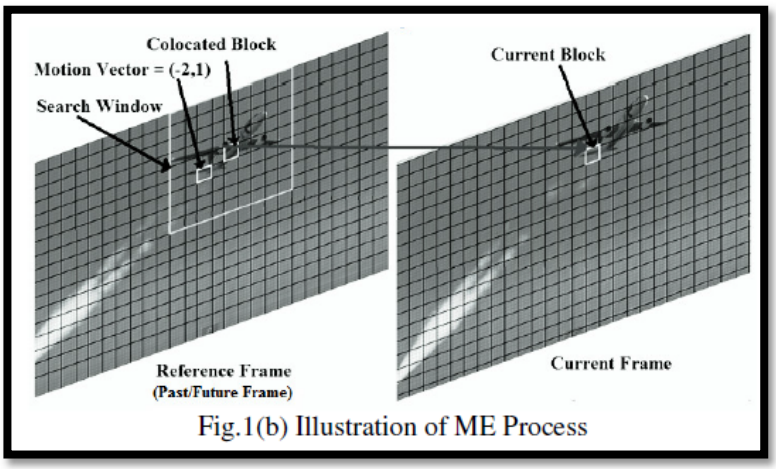


Fig.1(b) Illustration of ME Process

Purnachand Nalluri, *et al., Fast Motion Estimation Algorithm for HEVC Video Encoder*, published in 9TH CONFERENCE ON TELECOMMUNICATIONS, Vol. 1 at 1 (May 2013) (attached hereto as Exhibit_ZL 5), *available at*: https://www.it.pt/Publications/PaperConference/14332

149. For AMVP mode with motion estimation, the main goal of the motion estimation is to find the best matching block of each current PU and determine the real MV which represents the motion translation in the successive frame. The MV difference between the optimal AMVP candidate and the real MV derived from the motion estimation is encoded and transmitted together with other information, e.g., the optimal AMVP and reference frame indexes. The motion estimation is conducted in two stages, the integer motion estimation (IME) at integer pixel accuracy and the fractional motion estimation (FME) at subpixel accuracy. According to the "High Efficiency Video Coding (HEVC) Test Model 16 (HM 16) Improved Encoder Description Update 9" approved by JCT-VC, the best candidate MVP selected from the AMVP candidate list is used as an initial search center of the IME, which indicates that the search center of the IME is offset from the co-located block within the reference frame by the best candidate MVP.

150. Therefore, when the MediaTek '944 Products processes the video data using AMVP mode based on the IME, the co-located block within the reference frame of the current PU corresponds to the selected image segment, and the best candidate MVP corresponds to the offset

vector within the reference frame from the co-located block of the current PU (i.e., the selected image segment) to the search center.

> To derive the motion vector(s) for each PU, a block matching algorithm is performed in the HM encoder. For AMVP, find the best candidate MV predictor for each ref_idx and ref_pic_list using xEstimateMvPredAMVP(), called from predInterSearch(). The default search range for the first search in the HM encoder is 96 integer pixels, however the CTC [3] uses a value of 64. A search window is defined according to the search range, relative to the **best candidate MV predictor**. Firstly an integer-pel search is performed, followed by a fractional-pel refinement search.

The Joint Collaborative Team on Video Coding (JCT-VC), *High Efficiency Video Coding (HEVC) Test Model 16 (HM 16) Improved Encoder Description Update 9*, ISO/IEC JTC1/SC29/WG11 N17047 at 43 (July 2017) (emphasis added), *available at*: https://mpeg.chiariglione.org/standards/mpeg-h/high-efficiency-video-coding/n17047-high-efficiency-video-coding-hevc-test-model-16.

151. By complying with the HEVC standard, the MediaTek '944 Products necessarily infringe the '944 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '944 patent, including but not limited to claim 2 of the '944 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '944 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

152. The MediaTek '944 Products perform a method that includes deriving first and second vectors from said sub-pixel accurate motion vectors.

153. The MediaTek ‘944 Products perform a method that includes generating an intermediate image by combining first positions in a first image shifted over first vectors and second positions in said second image shifted over second vectors.

154. The MediaTek ‘944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by multiplying the vector components of the sub-pixel accurate motion vectors by a fraction to obtain fractional vector components.

155. The MediaTek ‘944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by rounding the fractional vector components to obtain vector components of the first vectors, which have only integer vector components.

156. The MediaTek ‘944 Products perform a method that includes deriving first and second vectors from sub-pixel accurate motion vectors by subtracting the first vector from the candidate vector to obtain the second vector, whereby the second vectors have vector components that, depending on the candidate vector and the fraction, may have non-integer values.

157. The MediaTek ’944 Products are available to businesses and individuals throughout the United States.

158. The MediaTek ’944 Products are provided to businesses and individuals located in the State of Delaware.

159. By making, using, testing, offering for sale, and/or selling products and services for sub-pixel accurate motion vector estimation and motion-compensated interpolation or prediction, including but not limited to the MediaTek ’944 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘944 patent, including at least claim 2 pursuant to 35 U.S.C. § 271(a).

160. MediaTek also indirectly infringes the '944 patent by actively inducing infringement under 35 USC § 271(b).

161. MediaTek has had knowledge of the '944 patent since at least service of the initial Complaint in this matter, MediaTek knew of the '944 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '944 patent based on prior communications that identified the '944 patent to MediaTek as early as six years prior to the filing of the initial Complaint in this matter.

162. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '944 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '944 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '944 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '944 Products that have the capability of operating in a manner that infringe one or more of the claims of the '944 patent, including at least claim 2, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '944 Products to utilize the products in a manner that directly infringe one or more claims of the '944 patent.[28] By providing instruction and training to customers and end-users on how to use the MediaTek '944 Products in a manner that directly infringes one or more claims of the '944 patent, including at least claim 2, MediaTek specifically intended to induce

[28] *See, e.g.*, *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); MSD6180 SOC DATASHEET (2016); MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" (December 18, 2014).

infringement of the '944 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '944 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '944 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '944 patent, knowing that such use constitutes infringement of the '944 patent.

163. The '944 patent is well-known within the industry as demonstrated by multiple citations to the '944 patent in published patents and patent applications assigned to technology companies and academic institutions.

164. MediaTek is utilizing the technology claimed in the '944 patent without paying a reasonable royalty. MediaTek is infringing the '944 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

165. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '944 patent. As a result of MediaTek's infringement of the '944 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

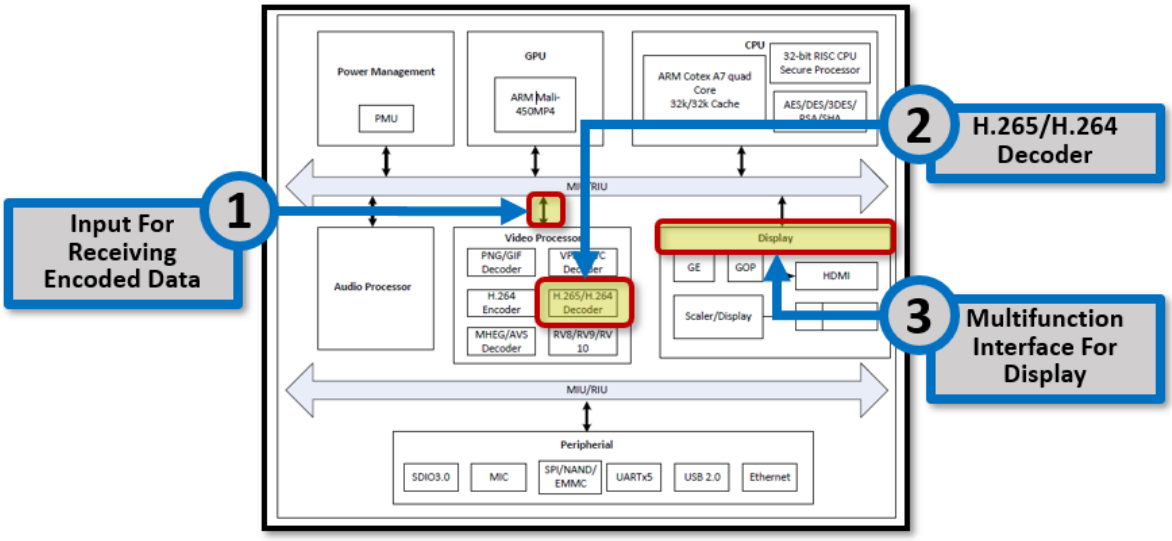
COUNT II
INFRINGEMENT OF U.S. PATENT NO. 6,760,376

166. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

167. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion compensated upconversion in a video image that uses motion

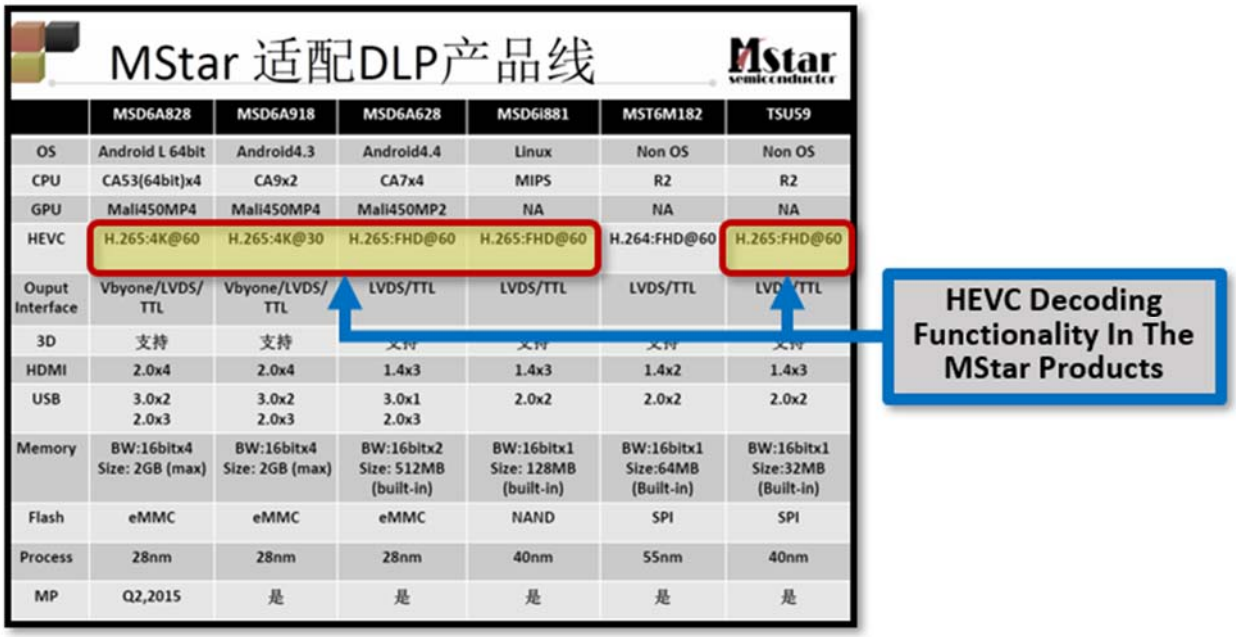
compensation to generate an interpolated video field using motion vectors, including but not limited to MStar System on Chip ("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MediaTek '376 Product(s)").

168. The MediaTek '376 Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

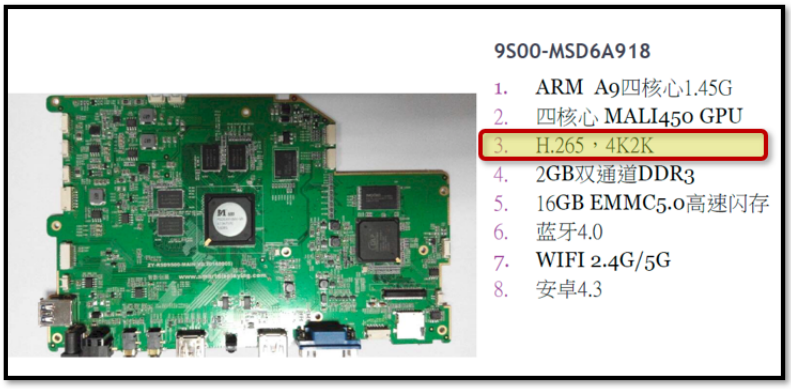
169. Documentation regarding the MediaTek '376 Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MediaTek '376 Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



	MSD6A828	MSD6A918	MSD6A628	MSD6i881	MST6M182	TSU59
OS	Android L 64bit	Android4.3	Android4.4	Linux	Non OS	Non OS
CPU	CA53(64bit)x4	CA9x2	CA7x4	MIPS	R2	R2
GPU	Mali450MP4	Mali450MP4	Mali450MP2	NA	NA	NA
HEVC	H.265:4K@60	H.265:4K@30	H.265:FHD@60	H.265:FHD@60	H.264:FHD@60	H.265:FHD@60
Ouput Interface	Vbyone/LVDS/ TTL	Vbyone/LVDS/ TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL
3D	支持	支持	支持	支持	支持	支持
HDMI	2.0x4	2.0x4	1.4x3	1.4x3	1.4x2	1.4x3
USB	3.0x2 2.0x3	3.0x2 2.0x3	3.0x1 2.0x3	2.0x2	2.0x2	2.0x2
Memory	BW:16bitx4 Size: 2GB (max)	BW:16bitx4 Size: 2GB (max)	BW:16bitx2 Size: 512MB (built-in)	BW:16bitx1 Size: 128MB (built-in)	BW:16bitx1 Size:64MB (Built-in)	BW:16bitx1 Size:32MB (Built-in)
Flash	eMMC	eMMC	eMMC	NAND	SPI	SPI
Process	28nm	28nm	28nm	40nm	55nm	40nm
MP	Q2,2015	是	是	是	是	是

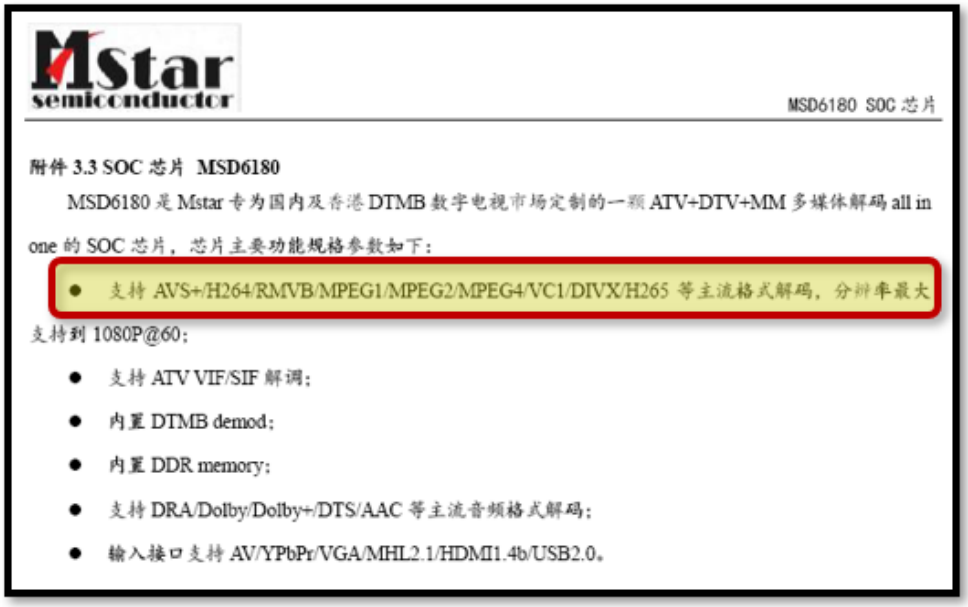
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

170. The MediaTek '376 Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MediaTek '376 Products that contain a decoder that conforms to the H.265 standard.



Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product Contains A Decoder Complaint With The H.265 Standard).

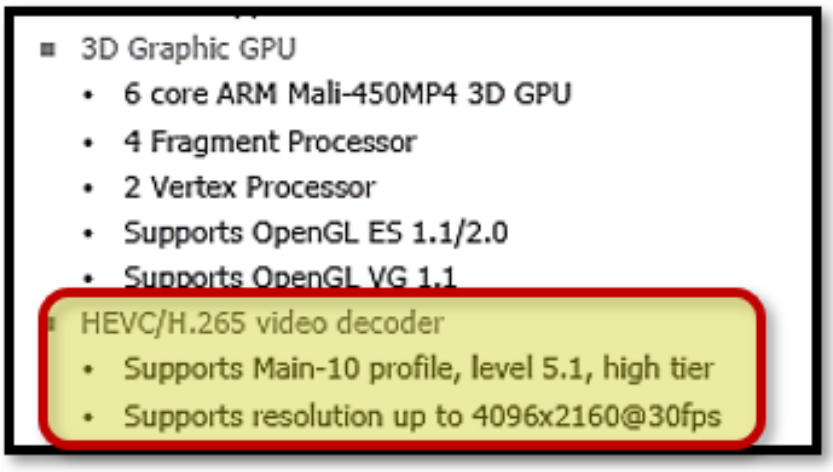
171. Datasheets from MediaTek also establish that the accused MediaTek '376 Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states: "all in one 的SOC 芯片，芯片主要功能规格参数如下： 支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60."[29]



MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

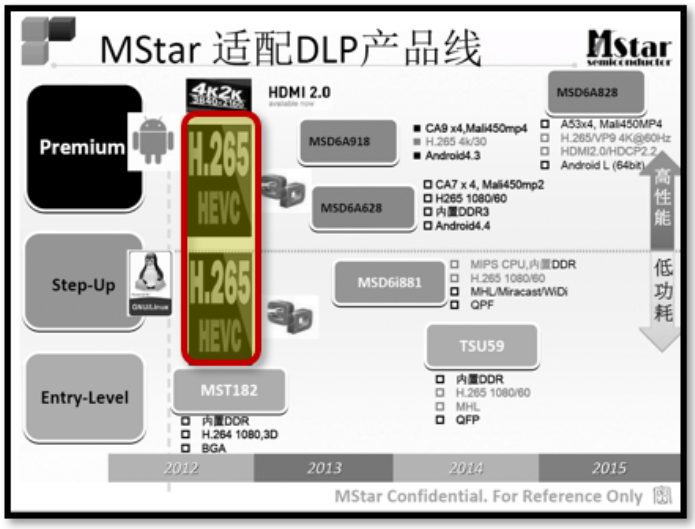
172. Similarly, the datasheet for the MSO9280MC Product identifies that it contains a HEVC H.265 decoder.

[29] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."



MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added).

173. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MediaTek '376 Products.



MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

174. Documentation from MediaTek customers such as TCL that incorporate the accused MediaTek '376 Products into devices such as televisions also identifies the accused chips contain an H.265 decoder.

类别	项目	L55H8800-CUD
输入和输出	ATV/DTV(DVB-C/DTMB) (PAL D/K I B/G)	✓
	HDMI (480i/p,576i/p,720p up to1080i/p,4K2K,with HDCP)	3 路，HDMI2 与 MHL 复用 支持 4K2K@30Hz 支持 H.265 格式
	VGA	无
	VGA/DVI audio	与 YPbPr 共用
	YPbPr (可支持 480i 到 1080p)	无
	SPDIF output	与AVout共用

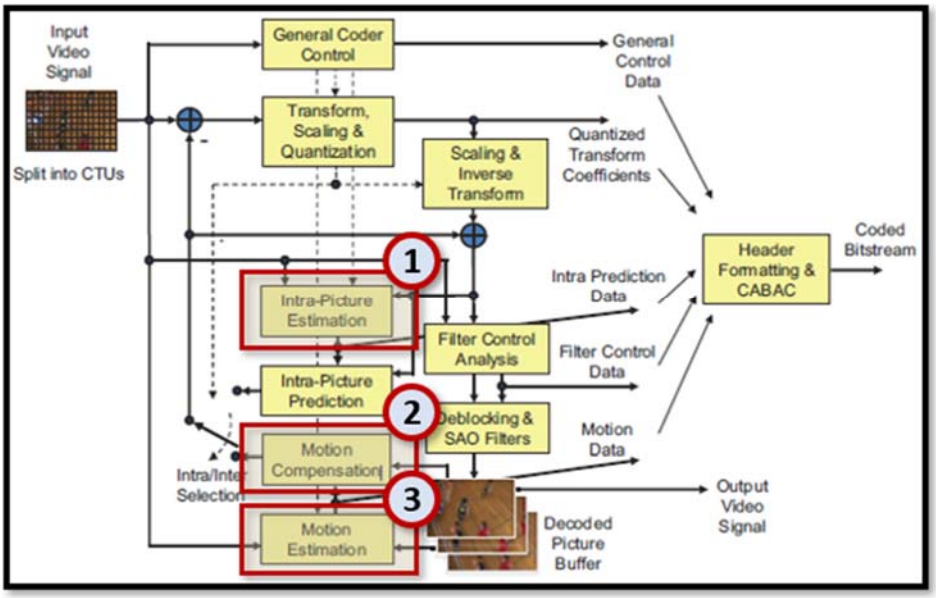
TCL PRODUCT BRIEF: MS918 机芯手册V1.0 at 35 (March 18, 2015) (annotation added) (showing that the MS918 chip from MStar contains a H.265 compliant decoder).

175. One or more MediaTek subsidiaries and/or affiliates use the MediaTek ’376 Products in regular business operations.

176. One or more of the MediaTek ‘376 Products include technology for motion compensated upconversion in a video image that uses motion compensation to generate an interpolated video field using motion vectors.

177. One or more of the MediaTek ’376 Products use upconversion units to generate an interpolated field using motion vectors to in the process of performing motion compensation.

178. The MediaTek ‘376 Products use upconversion units within an image retrieved from memory. The frames are then processed using both motion compensation and motion estimation. The motion compensation functionality used by the MediaTek ‘376 Products include quarter-sample precision for the motion vectors and 7-tap or 8-tap filters that are used for interpolation of fractional-sample positions.



Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, VOL. 7, NO. 6 at 1002 (December 2013) (emphasis added) (the annotations showing (1) intra-picture prediction, (2) motion compensation, and (3) motion estimation).

179. The MediaTek '376 Products calculate a correlation value from the values of causal neighbor pixels of a generated field and from the values of corresponding neighbor pixels of a next field.

> It can be seen from Fig. 5.4b that only motion vectors from spatial neighboring blocks to the left and above the current block are considered as spatial MVP candidates. This can be explained by the fact that the blocks to the right and below the current block are not yet decoded and hence, their motion data is not available. Since the co-located picture is a reference picture which is already decoded, it is possible to also consider motion data from the block at the same position, from blocks to the right of the co-located block or from the blocks below**.** In HEVC, the block to the bottom right and at the center of the current block have been determined to be the most suitable to provide a good temporal motion vector predictor (TMVP).

Benjamin Bross, *et al., Inter-picture prediction in HEVC,* in HIGH EFFICIENCY VIDEO CODING (HEVC) at 119 (2014) (emphasis added).

180. The MediaTek '376 Products compare the correlation value with a threshold value.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

181. The MediaTek '376 Products set the value of a pixel to be created within the generated field to be equal to the value of a corresponding pixel of the next field if the correlation value is less than the threshold value.

182. MediaTek has directly infringed and continues to directly infringe the '376 patent by, among other things, making, using, offering for sale, and/or selling technology for motion compensated upconversion in a video image that uses motion compensation to generate an interpolated video field using motion vectors, including but not limited to the MediaTek '376 Products.

183. By complying with the HEVC standard, the MediaTek products – such as the MediaTek '376 Products – necessarily infringe the '376 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '376 patent, including but not limited to claim 4 of the '376 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '376 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

184. The MediaTek ‘376 Products perform a method of motion compensation for use in a video image upconversion unit of the type that uses motion compensation to generate an interpolated field using motion vectors.

185. The MediaTek ‘376 Products perform a method of motion compensation that includes calculating a correlation value from the values of causal neighbor pixels of a generated field and from the values of corresponding neighbor pixels of a next field.

186. The MediaTek ‘376 Products perform a method of motion compensation that includes comparing the correlation value with a threshold value.

187. The MediaTek ‘376 Products perform a method of motion compensation that includes setting the value of a pixel to be created within the generated field to be equal to the value of a corresponding pixel of the next field if the correlation value is less than the threshold value.

188. The MediaTek ’376 Products are available to businesses and individuals throughout the United States.

189. The MediaTek ’376 Products are provided to businesses and individuals located in the State of Delaware.

190. By making, using, testing, offering for sale, and/or selling products and services for motion compensated upconversion in a video image that uses motion compensation to generate an interpolated video field using motion vectors, including but not limited to the MediaTek ’376 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘376 patent, including at least claim 4 pursuant to 35 U.S.C. § 271(a).

191. MediaTek has also indirectly infringed the ‘376 patent by actively inducing infringement under 35 USC § 271(b).

192. MediaTek has had knowledge of the '376 patent since at least service of the initial Complaint in this matter, MediaTek knew of the '376 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '376 patent based on prior communications that identified the '376 patent to MediaTek as early as six years prior to the filing of the initial Complaint in this matter.

193. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '376 Products in regular business operations.

194. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '376 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '376 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '376 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '376 Products that have the capability of operating in a manner that infringe one or more of the claims of the '376 patent, including at least claim 4, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '376 Products to utilize the products in a manner that directly infringe one or more claims of the '376 patent.[30] By providing instruction and training to customers and end-users on how to use the MediaTek '376 Products in a manner that directly infringes one or more claims of the '376 patent, including at least claim 4, MediaTek specifically intended to induce

[30] *See, e.g.*, *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); MSD6180 SOC DATASHEET (2016); MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" (December 18, 2014).

infringement of the '376 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '376 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '376 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '376 patent, knowing that such use constitutes infringement of the '376 patent.

195. The '376 patent is well-known within the industry as demonstrated by multiple citations to the '376 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '376 patent without paying a reasonable royalty. MediaTek is infringing the '376 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

196. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '376 patent. As a result of MediaTek's infringement of the '376 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

COUNT III
INFRINGEMENT OF U.S. PATENT NO. 6,774,918

197. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

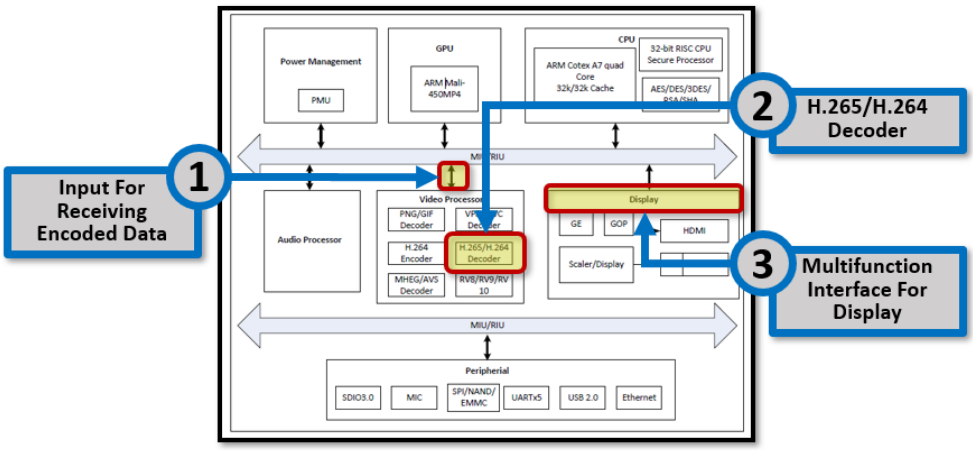
198. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for image processing.

199. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek devices that contain H.265 decoding functionality, the infringing MediaTek products include but are not limited to: MediaTek Automotive Products (MediaTek Autus I20 (MT2712)); MediaTek Mobile Products (MediaTek Helio A11, MediaTek Helio P10, MediaTek Helio P18, MediaTek Helio P20, MediaTek Helio P22, MediaTek Helio P23, MediaTek Helio P25, MediaTek Helio P30, MediaTek Helio P60, MediaTek Helio P70, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, MediaTek MT6732, MediaTek MT6735, MediaTek MT6738, MediaTek MT6739, MediaTek MT6750, MediaTek MT6752, and MediaTek MT6753); MediaTek Digital TV Products (MediaTek MT5582, MediaTek MT5596, and MediaTek MT5597); MediaTek Home Products (MediaTek MT8581, MediaTek MT8685, and MediaTek MT8693); and MediaTek Tablet Products (MediaTek MT8163V/A, MediaTek MT8163V/B, MediaTek MT8167A, MediaTek MT8167B, MediaTek MT8173, MediaTek MT8176, MediaTek MT8735B, MediaTek MT8735D, MediaTek MT8735M, MediaTek MT8735P, MediaTek MT8783, and MediaTek MT8785) (collectively, the "MediaTek Products").

200. MediaTek designs, makes, sells, offers to sell, imports, and/or uses products that contain HEVC decoding technology, including but not limited to the MStar System on Chip ("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MStar Product(s)").

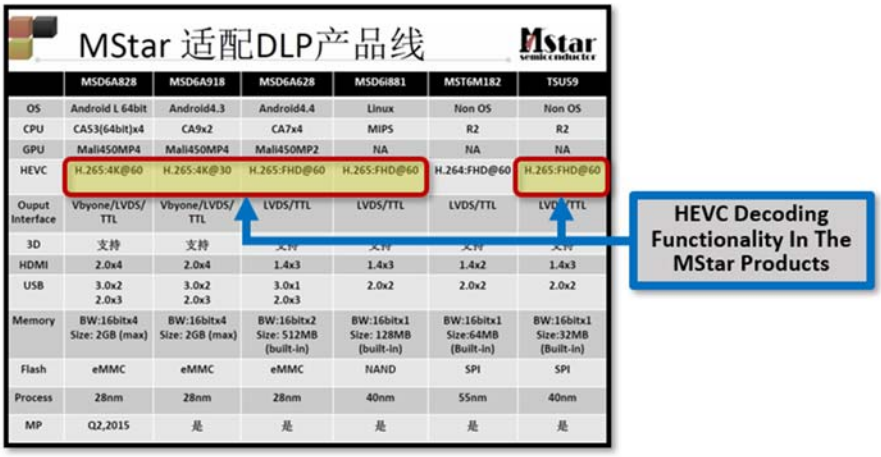
201. The MediaTek Products and MStar Products (collectively, the "MediaTek '918 Product(s)") directly infringe the '918 patent.

202. The MStar Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

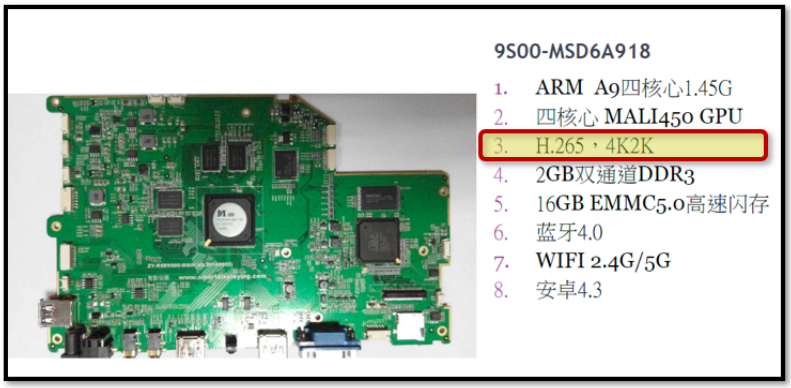
203. Documentation regarding the MStar Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MStar Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



	MSD6A828	MSD6A918	MSD6A628	MSD6i881	MST6M182	TSU59
OS	Android L 64bit	Android4.3	Android4.4	Linux	Non OS	Non OS
CPU	CA53(64bit)x4	CA9x2	CA7x4	MIPS	R2	R2
GPU	Mali450MP4	Mali450MP4	Mali450MP2	NA	NA	NA
HEVC	H.265:4K@60	H.265:4K@30	H.265:FHD@60	H.265:FHD@60	H.264:FHD@60	H.265:FHD@60
Ouput Interface	Vbyone/LVDS/ TTL	Vbyone/LVDS/ TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL
3D	支持	支持	支持	支持	支持	支持
HDMI	2.0x4	2.0x4	1.4x3	1.4x3	1.4x2	1.4x3
USB	3.0x2 2.0x3	3.0x2 2.0x3	3.0x1 2.0x3	2.0x2	2.0x2	2.0x2
Memory	BW:16bitx4 Size: 2GB (max)	BW:16bitx4 Size: 2GB (max)	BW:16bitx2 Size: 512MB (built-in)	BW:16bitx1 Size: 128MB (built-in)	BW:16bitx1 Size:64MB (Built-in)	BW:16bitx1 Size:32MB (Built-in)
Flash	eMMC	eMMC	eMMC	NAND	SPI	SPI
Process	28nm	28nm	28nm	40nm	55nm	40nm
MP	Q2,2015	是	是	是	是	是

MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

204. The MStar Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MStar Products that contain a decoder that conforms to the H.265 standard.



Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product contains a decoder compliant with the H.265 standard).

205. Datasheets from MediaTek also establish that the accused MStar Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states:

"all in one 的SOC 芯片，芯片主要功能规格参数如下：支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60"[31]


MSD6180 SOC 芯片

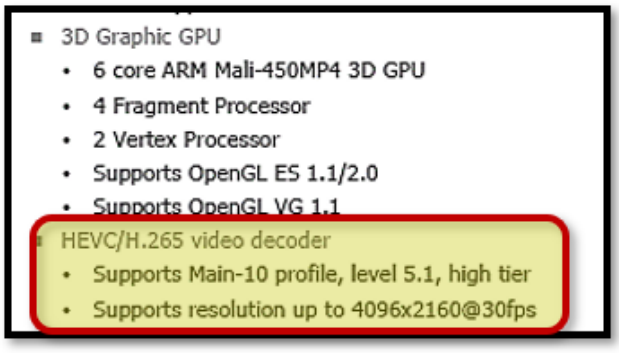
附件 3.3 SOC 芯片 MSD6180

MSD6180 是 Mstar 专为国内及香港 DTMB 数字电视市场定制的一颗 ATV+DTV+MM 多媒体解码 all in one 的 SOC 芯片，芯片主要功能规格参数如下：

- 支持 AVS+/H264/RMVB/MPEG1/MPEG2/MPEG4/VC1/DIVX/H265 等主流格式解码，分辨率最大支持到 1080P@60；
- 支持 ATV VIF/SIF 解调；
- 内置 DTMB demod；
- 内置 DDR memory；
- 支持 DRA/Dolby/Dolby+/DTS/AAC 等主流音频格式解码；
- 输入接口支持 AV/YPbPr/VGA/MHL2.1/HDMI1.4b/USB2.0。

MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

206. Similarly, the MediaTek datasheet for the MSO9280MC Product identifies that it contains an HEVC H.265 decoder.


3D Graphic GPU

- 6 core ARM Mali-450MP4 3D GPU
- 4 Fragment Processor
- 2 Vertex Processor
- Supports OpenGL ES 1.1/2.0
- Supports OpenGL VG 1.1

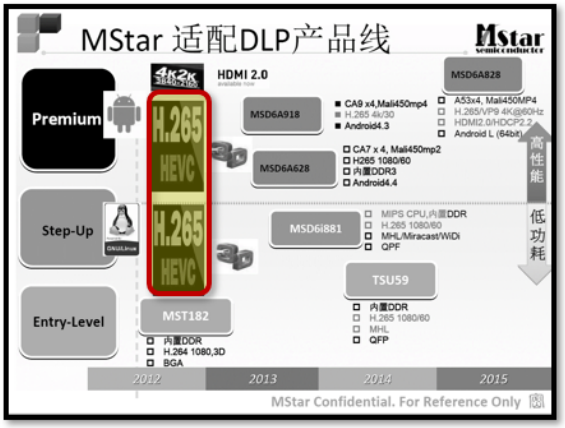
HEVC/H.265 video decoder

- Supports Main-10 profile, level 5.1, high tier
- Supports resolution up to 4096x2160@30fps

MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added).

[31] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."

207. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MStar Products.



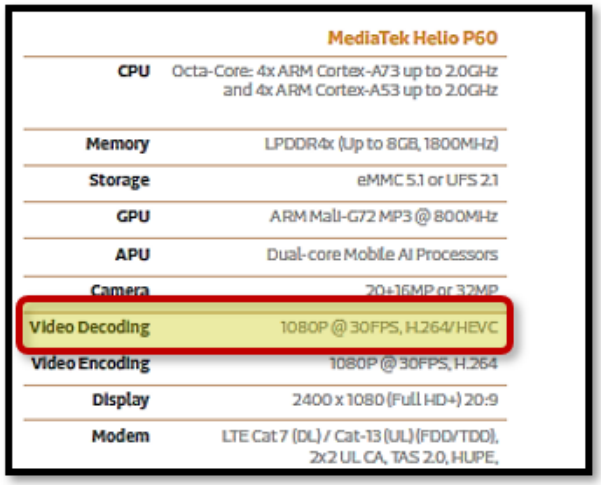
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

208. Documentation from MediaTek customers such as TCL that incorporate the accused MStar Products into devices such as televisions also identifies the accused MStar Products as containing an H.265 decoder.

类别	项目	L55H8800-CUD
输入和输出	ATV/DTV(DVB-C/DTMB) (PAL D/K I B/G)	✓
	HDMI (480i/p,576i/p,720p up to1080i/p,4K2K,with HDCP)	3 路，HDMI2 与 MHL 复用 支持 4K2K@30Hz 支持 H.265 格式
	VGA	无
	VGA/DVI audio	与 YPbPr 共用
	YPbPr (可支持 480i 到 1080p)	无
	SPDIF output	与AVout共用

TCL PRODUCT BRIEF: MS918 机芯手册V1.0 at 35 (March 18, 2015) (annotation added) (showing that the MS918 chip from MStar contains a H.265 compliant decoder).

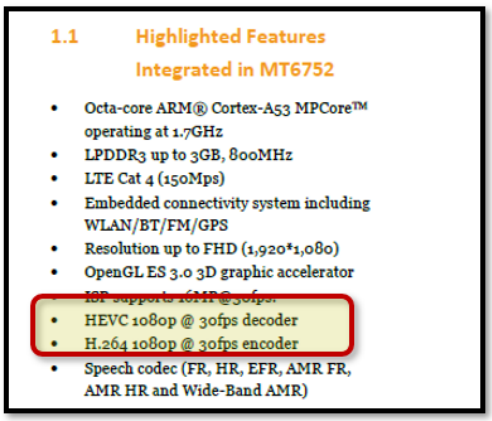
209. MediaTek's datasheets identify that the MediaTek Products (*e.g.*, MediaTek Helio P60) contain a video decoder that complies with the H.265 standard.



	MediaTek Helio P60
CPU	Octa-Core: 4x ARM Cortex-A73 up to 2.0GHz and 4x ARM Cortex-A53 up to 2.0GHz
Memory	LPDDR4x (Up to 8GB, 1800MHz)
Storage	eMMC 5.1 or UFS 2.1
GPU	ARM Mali-G72 MP3 @ 800MHz
APU	Dual-core Mobile AI Processors
Camera	20+16MP or 32MP
Video Decoding	1080P @ 30FPS, H.264/HEVC
Video Encoding	1080P @ 30FPS, H.264
Display	2400 x 1080 (Full HD+) 20:9
Modem	LTE Cat 7 (DL) / Cat-13 (UL) (FDD/TDD), 2x2 UL CA, TAS 2.0, HUPE,

MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 at 2 (2018) (annotation added).

210. Technical briefs from MediaTek similarly identify the accused MediaTek products as containing a decoder that complies with the HEVC standard.

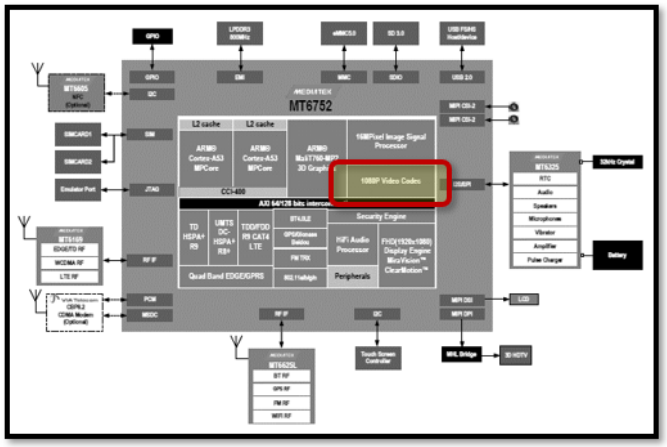


1.1 Highlighted Features Integrated in MT6752

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.7GHz
- LPDDR3 up to 3GB, 800MHz
- LTE Cat 4 (150Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

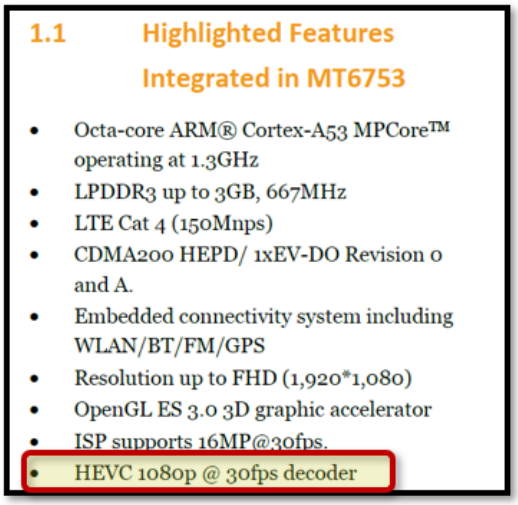
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (June 10, 2014) (annotation added) ("The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.").

211. MediaTek documentation relating to the accused MediaTek Products (*e.g.*, MT6752) describe the chips as a "brand-new generation smart phone SoC integrating MediaTek LTE modem, Octa-core ARM® Cortex-A53 MPCoreTM, 3D graphics and high-definition 1080p video decoder."



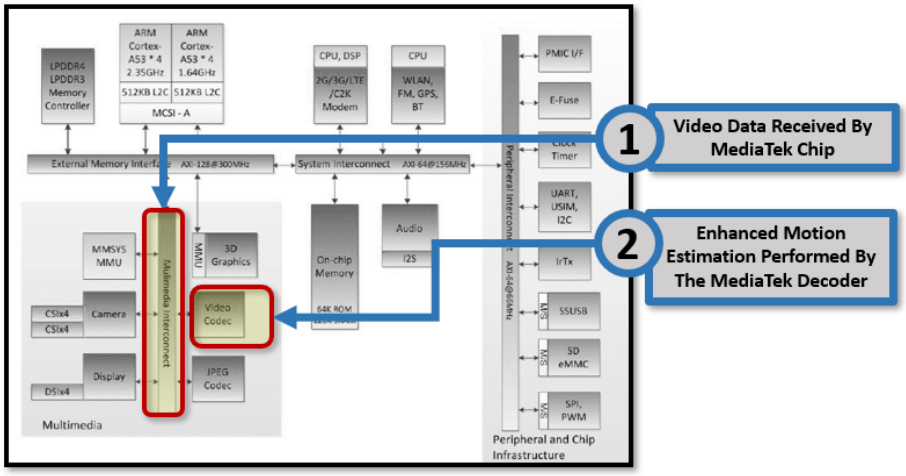
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 15 (June 10, 2014) (annotation showing the HEVC video decoder).

212. MediaTek documentation for the accused products identifies products such as the MT6753 Application Processor contains a video decoder that complies with the HEVC standard.



MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (November 27, 2014) ("The chip integrates Octa-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.").

213. MediaTek documentation shows the interconnects that connect the video decoding engine to the rest of the application processor. For example, MediaTek documentation for the MT6757 chip (i.e., the Helio P20 chip) shows connections to the video codec engine.



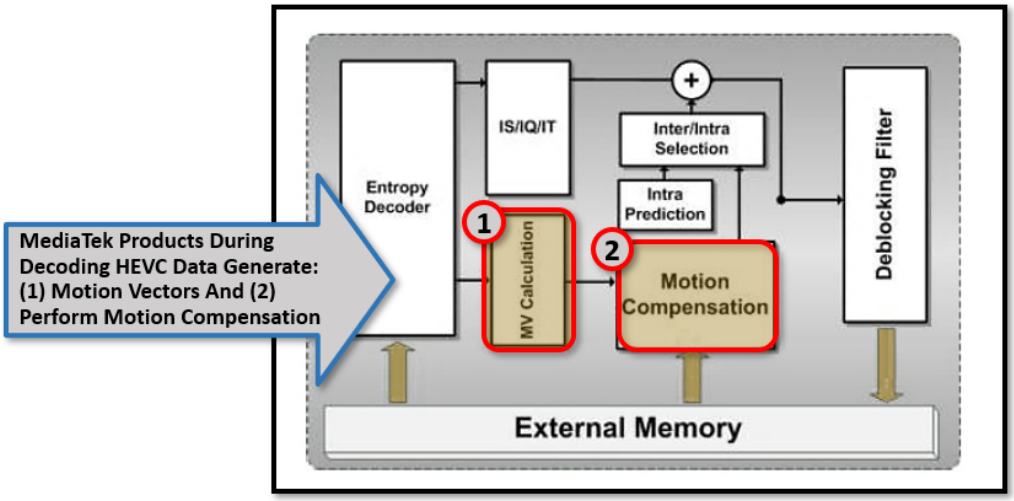
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 18 (June 20, 2016) (annotations added).

214. MediaTek technical documentation establishes the accused products (e.g., the MT6757 application processor) include an HEVC compliant decoder.

> The application processor, an Octa-core ARM® Cortex-A53 MPCoreTM equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

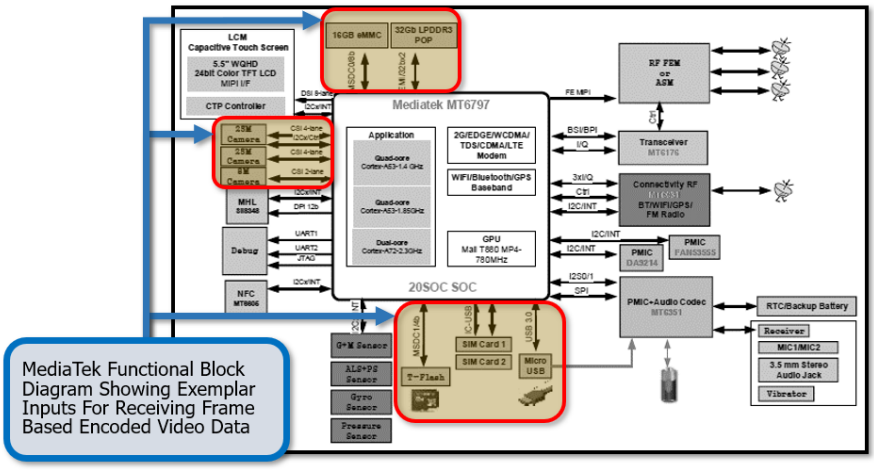
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 7 (June 20, 2016) (emphasis added) (describing that the MediaTek product includes a decoder for "HEVC 4K @ 30fps").

215. The architecture and core blocks of HEVC decoder ("VDEC") are shown in the below diagram including the following functional components: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra prediction, Motion Compensation, and De-Blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is sent to the display stage.



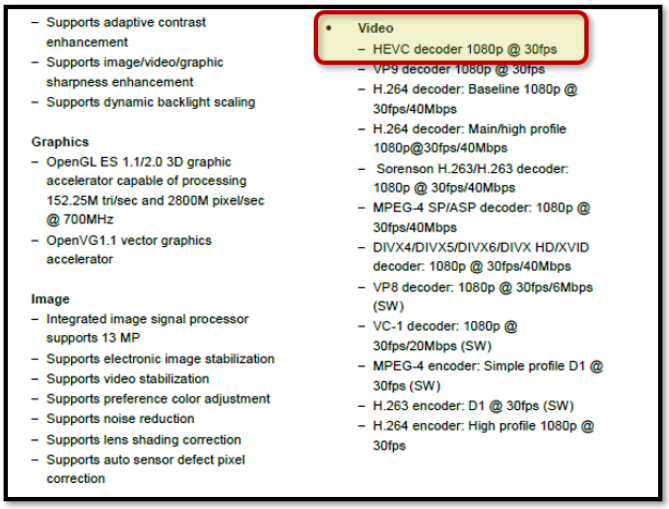
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 276 (July 19, 2016) (annotations added)

216. The accused MediaTek '918 Products receive HEVC encoded data through a variety of inputs. The below excerpt from MediaTek's technical documentation identifies the inputs for receiving HEVC encoded video data as part of the decoding process.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 12 (July 19, 2016) (annotations added) (showing a high-level functional block diagram of the MT6797 product).

217. MediaTek documentation similarly identifies that the MediaTek '918 Products contain an "HEVC decoder" as shown in the below excerpt from a MediaTek Technical Brief for the MT6592 Octa-Core Smartphone Application Processor.



- Supports adaptive contrast enhancement
- Supports image/video/graphic sharpness enhancement
- Supports dynamic backlight scaling

Graphics
- OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 152.25M tri/sec and 2800M pixel/sec @ 700MHz
- OpenVG1.1 vector graphics accelerator

Image
- Integrated image signal processor supports 13 MP
- Supports electronic image stabilization
- Supports video stabilization
- Supports preference color adjustment
- Supports noise reduction
- Supports lens shading correction
- Supports auto sensor defect pixel correction

- **Video**
  - HEVC decoder 1080p @ 30fps
  - VP9 decoder 1080p @ 30fps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p@30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - VP8 decoder: 1080p @ 30fps/6Mbps (SW)
  - VC-1 decoder: 1080p @ 30fps/20Mbps (SW)
  - MPEG-4 encoder: Simple profile D1 @ 30fps (SW)
  - H.263 encoder: D1 @ 30fps (SW)
  - H.264 encoder: High profile 1080p @ 30fps

MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 8 and 11 (July 6, 2013) (annotation added) ("Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6592 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.7GHz Octa-core ARM® Cortex-A7 MPCoreTM, 3D graphics and high-definition 1080p video decoder.").

218. The MediaTek '918 Products contain functionality for downloading on-screen display (OSD) data for generating an image on a display device. Specifically, the MediaTek Products have an input for receiving frame-based encoded video information. The MediaTek Products receive frame-based encoded video information in the form of video data that is encoded in the High Efficiency Video Coding (HEVC/H.265) format set by the ITU-T Video Coding Experts Group.

219. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '918 Products – necessarily infringe the '918 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '918 patent, including but not limited to claim 18. High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '918 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and

descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

220. The MediaTek '918 Products receive a bitstream in which the data is segmented into Network Abstraction Layer ("NAL") Units. NAL Units are segments of data that can include video data and overlay data (such as captions and overlay images). The MediaTek Products support the receipt of VCL and non-VCL NAL units. The VCL NAL units contain the data that represents the values of the samples in the video pictures, and the non-VCL NAL units contain any associated additional information such as parameter sets or overlay data.

> HEVC uses a NAL unit based bitstream structure. A coded bitstream is partitioned into NAL units which, when conveyed over lossy packet networks, should be smaller than the maximum transfer unit (MTU) size. Each NAL unit consists of a NAL unit header followed by the NAL unit payload. There are two conceptual classes of NAL units. Video coding layer (VCL) NAL units containing coded sample data, e.g., coded slice NAL units, whereas non-VCL NAL units that contain metadata typically belonging to more than one coded picture, or where the association with a single coded picture would be meaningless, such as parameter set NAL units, or where the information is not needed by the decoding process, such as SEI NAL units.

Rickard Sjöberg, et al., *Overview of HEVC High-Level Syntax and Reference Picture Management,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1859 (December 2012) (emphasis added).

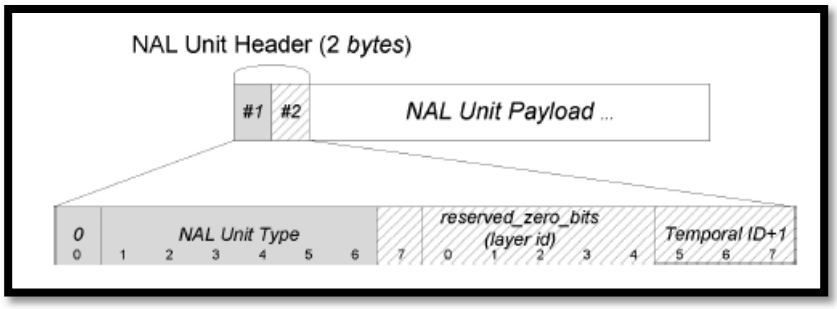
221. The VCL NAL Units contain segments of data which are used to generate an image (*e.g.*, HEVC image) on a display device. Each VCL NAL Unit comprises a discrete number of bites which make up a segment. The following excerpt from the HEVC specification describes the NAL unit as being a segment with a "demarcation" setting forth where the segment ends and begins:

> NumBytesInNalUnit specifies the size of the NAL unit in bytes. This value is required for decoding of the NAL unit. Some form of demarcation of NAL unit boundaries is necessary to enable inference of NumBytesInNalUnit. One such

> demarcation method is specified in Annex B for the byte stream format. Other methods of demarcation may be specified outside of this Specification.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.2.1 (February 2018) (emphasis added).

222. VCL NAL Units comprise discrete video data that ends. It is between the receipt of VCL NAL Units that the overlay data (Non-VCL NAL Unit) data is received by the MediaTek Products.



Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, VOL.* 22, NO. 12 at 1875 (December 2012).

223. The HEVC bitstream structure is comprised of discreet data. In the gaps between the receipt by the MediaTek '918 Products of VCL NAL Units, Non-VCL NAL Units are received by the MediaTek Products' decoder.

> An HEVC bitstream consists of a number of access units, each including coded data associated with a picture that has a distinct capturing or presentation time. Each access unit is divided into NAL units, including one or more VCL NAL units (i.e., coded slice NAL units) and zero or more non-VCL NAL units, e.g., parameter set NAL units or supplemental enhancement information (SEI) NAL units. Each NAL unit includes an NAL unit header and an NAL unit payload. Information in the NAL unit header can be (conveniently) accessed by media gateways, also known as media aware network elements (MANEs), for intelligent, media aware operations on the stream, such as stream adaptation.

Thomas Schierl, Miska M. Hannuksela, Ye-Kui Wang, and Stephan Wenger, System Layer Integration of High Efficiency Video Coding, *IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, VOL.* 22, NO. 12 at 1873 (December 2012).

224. Non-VCL NAL unit types include data such as supplemental enhancement information that is used to create overlays for display on the device.

Table 2.2 The 32 HEVC non-VCL NAL unit types

Non-VCL NAL unit types			
Parameter sets	32	VPS_NUT	Video parameter set
	33	SPS_NUT	Sequence parameter set
	34	PPS_NUT	Picture parameter set
Delimiters	35	AUD_NUT	Access unit delimiter
	36	EOS_NUT	End of sequence
	37	EOB_NUT	End of bitstream
Filler data	38	FD_NUT	Filler data
Supplemental enhancement information (SEI)	39	PREFIX_SEI_NUT	
	40	SUFFIX_SEI_NUT	
Reserved	41–47	RSV	
Unspecified	48–63	UNSPEC	

Gary J. Sullivan, et al., HIGH EFFICIENCY VIDEO CODING (HEVC) at 29 (September 2014).

225. Non-VCL NAL Units include supplemental enhancement information ("SEI") messages. The SEI data that is received contains overlay information that can be combined with the image data that has already been received.

sei_message( ) {	Descriptor
payloadType = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadType += 255	
}	
last_payload_type_byte	u(8)
payloadType += last_payload_type_byte	
payloadSize = 0	
while(next_bits(8) == 0xFF) {	
ff_byte /* equal to 0xFF */	f(8)
payloadSize += 255	
}	
last_payload_size_byte	u(8)
payloadSize += last_payload_size_byte	
sei_payload(payloadType, payloadSize)	
}	

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 7.3.5 (February 2018).

226. The MediaTek '918 Products combine the VCL NAL Unit and Non-VCL NAL Unit information to create images that contain overlay information.

> The NAL units are decoded by the decoder to produce the decoded pictures that are output from the decoder. Both the encoder and decoder store pictures in a decoded picture buffer (DPB). This buffer is mainly used for storing pictures so that previously coded pictures can be used to generate prediction signals to use when coding other pictures. These stored pictures are called reference pictures. . . . There are two classes of NAL units in HEVC—video coding layer (VCL) NAL units and non-VCL NAL units. Each VCL NAL unit carries one slice segment of coded picture data while the non-VCL NAL units contain control information that

> typically relates to multiple coded pictures. One coded picture, together with the non-VCL NAL units that are associated with the coded picture, is called an HEVC access unit.

Gary J. Sullivan, et al., HIGH EFFICIENCY VIDEO CODING (HEVC) at 14-15 (September 2014) (emphasis added).

227. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '918 Products in regular business operations.

228. The MediaTek '918 Products are available to businesses and individuals throughout the United States.

229. The MediaTek '918 Products are provided to businesses and individuals located in the State of Delaware.

230. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the MediaTek '918 Products, MediaTek has injured Dynamic Data and is liable for directly infringing one or more claims of the '918 patent, including at least claim 18, pursuant to 35 U.S.C. § 271(a).

231. MediaTek also indirectly infringes the '918 patent by actively inducing infringement under 35 U.S.C. § 271(b).

232. MediaTek has had knowledge of the '918 patent since at least service of this First Amended Complaint, and MediaTek knew of the '918 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '918 Patent based on prior communications that identified the '918 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

233. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '918 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause

infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '918 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '918 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '918 Products that have the capability of operating in a manner that infringe one or more of the claims of the '918 patent, including at least claim 18, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '918 Products to utilize the products in a manner that directly infringe one or more claims of the '918 patent.[32] By providing instruction and training to customers and end-users on how to use the MediaTek '918 Products in a manner that directly infringes one or more claims of the '918 patent, including at least claim 18, MediaTek specifically intended to induce infringement of the '918 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '918 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '918 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '918 patent, knowing that such use constitutes infringement of the '918 patent.

[32] *See, e.g.*, *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 (June 20, 2016); MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (November 27, 2014); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (June 10, 2014); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 (2018); *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); and MSD6180 SOC DATASHEET (2016).

234. The '918 patent is well-known within the industry as demonstrated by multiple citations to the '918 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '918 patent without paying a reasonable royalty. MediaTek is infringing the '918 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

235. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '918 patent.

236. As a result of MediaTek's infringement of the '918 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

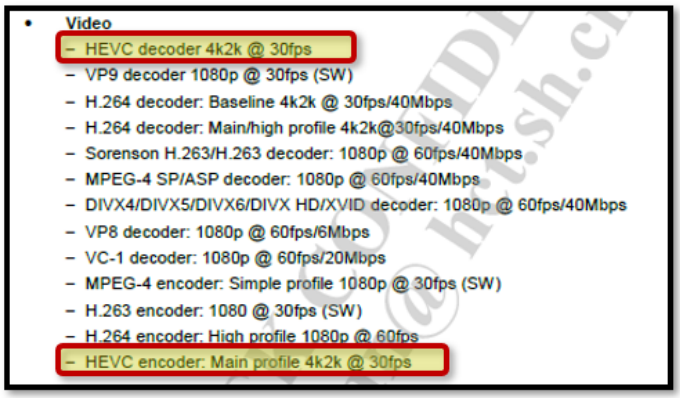
COUNT IV
INFRINGEMENT OF U.S. PATENT NO. 6,996,175

237. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

238. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for recursive motion vector estimation.

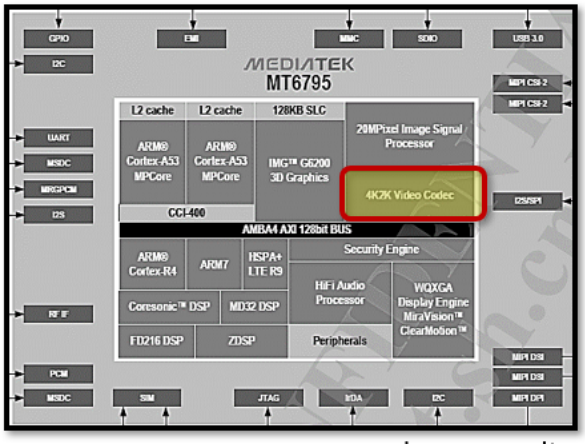
239. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '175 Product(s)").

240. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 (i.e., the Helio X10) Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.



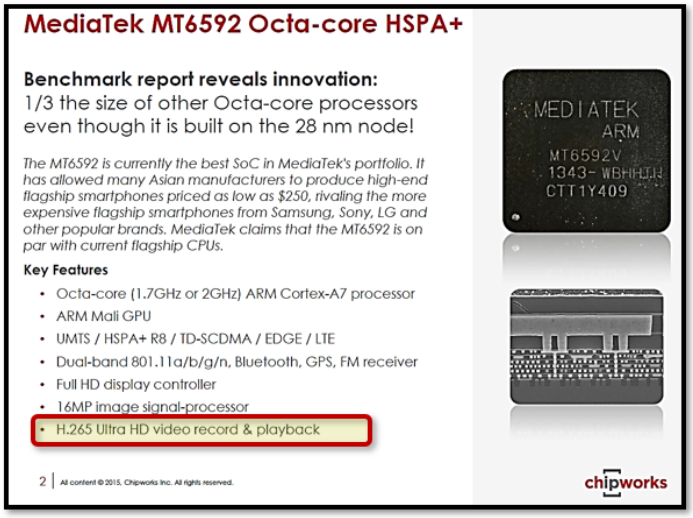
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 (August 27, 2014) (annotations added).

241. The following documentation from MediaTek shows an exemplar of the accused devices (e.g., MT6795) and in a functional diagram of the chip identifies the location of the HEVC "Video Codecs."



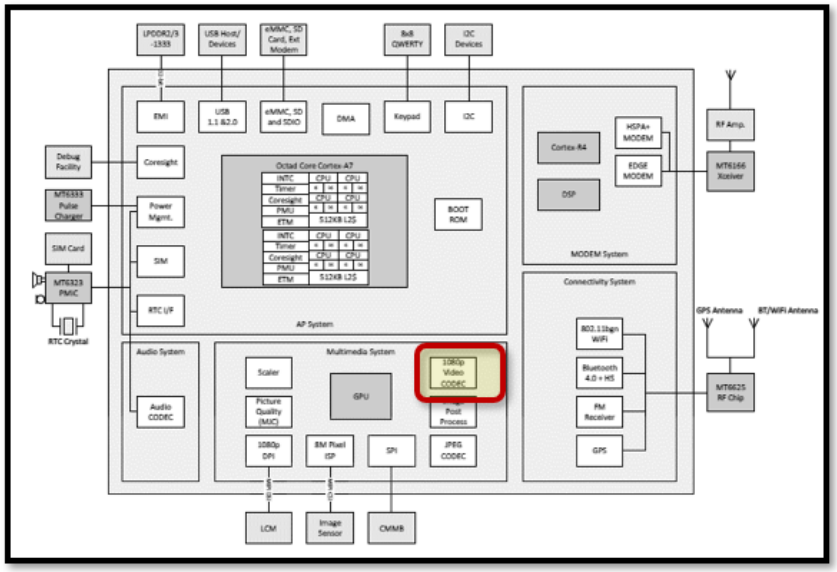
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 12 (August 27, 2014) (annotation added).

242. Analysis of the accused MediaTek '175 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

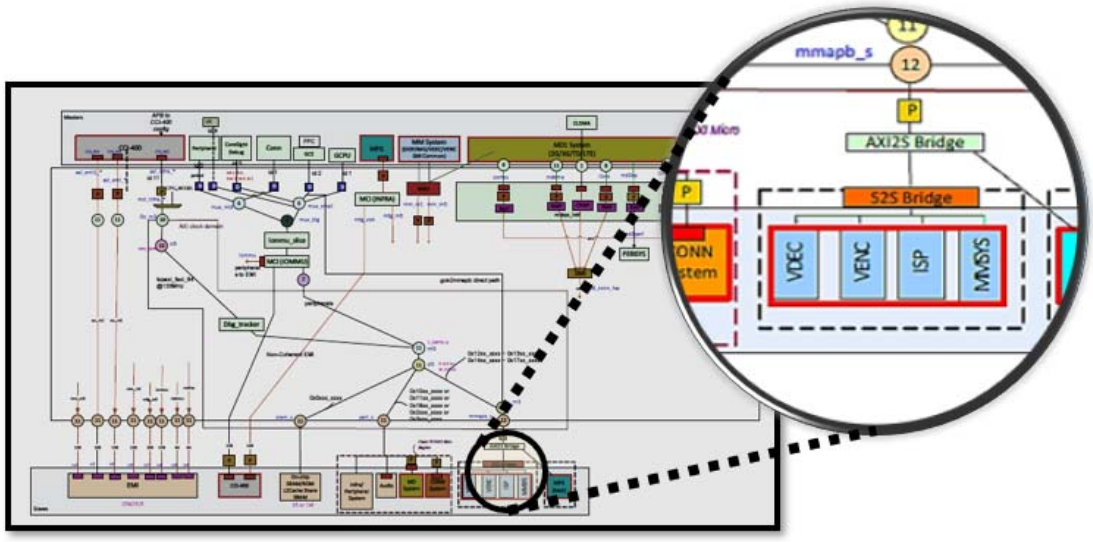
243. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (annotation added) (block diagram of the MT6592 Product showing the Video Codec for HEVC decoding that is part of the chip's multimedia system).

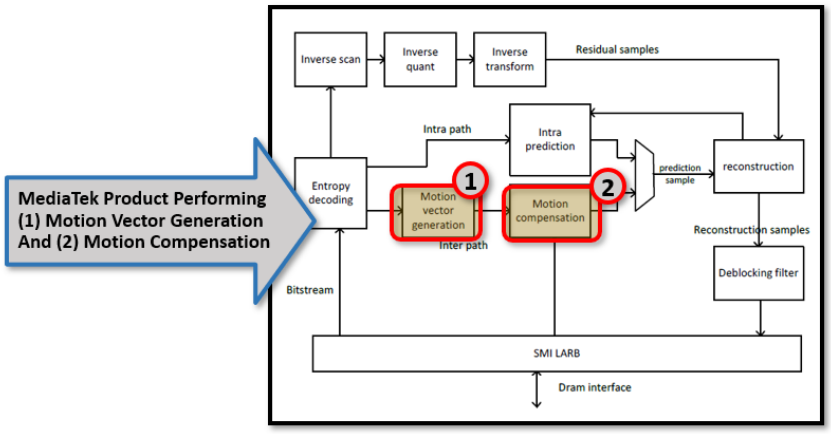
244. MediaTek documentation also establishes the accused MediaTek '175 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019).

245. MediaTek documentation also establishes that the accused MediaTek '175 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



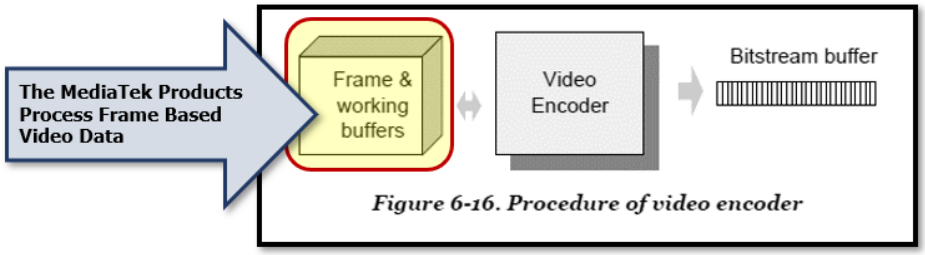
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

246. MediaTek documentation describes the encoding process used by the accused MediaTek '175 Products. For example, the below process diagram from MediaTek shows the MediaTek '175 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



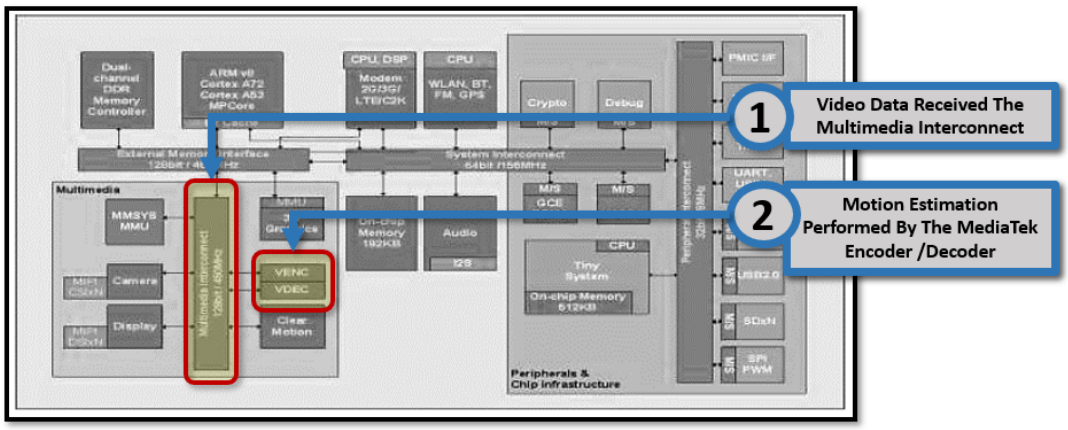
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

247. The video encoder in the accused MediaTek '175 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

248. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

249. The MediaTek '175 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '175 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

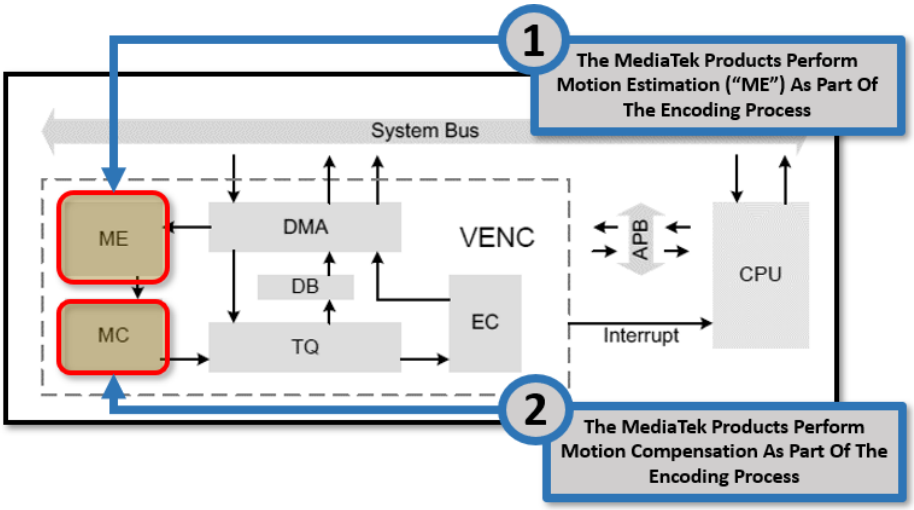
> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

250. The accused MediaTek '175 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC.

This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

251. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

252. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '175 Products in regular business operations.

253. One or more of the MediaTek '175 Products include technology for generating for a block a plurality of candidate vectors from stored vectors.

254. By complying with the HEVC standard, MediaTek's devices – such as the MediaTek '175 Products – necessarily infringe the '175 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '175 patent, including but not limited to claim 1. *High Efficiency Video Coding*, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265

(February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '175 patent: "3.110 Prediction Unit Definition;" "6.3.2 Block and quadtree structures;" "6.3.3 Spatial or component-wise partitioning;" "6.4.2 Derivation process for prediction block availability;" "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

255. One or more of the MediaTek '175 Products include technology for selecting one of these candidate vectors (that was generated from a stored vector) to generate a selected vector.

> Spatial Candidates
>
> As already mentioned, two spatial MVP candidates A and B are derived from five spatially neighboring blocks which are shown in Fig. 5.4b. The locations of the spatial candidate blocks are the same for both AMVP and inter-prediction block merging that will be presented in Sect. 5.2.2.

Gary Sullivan, *et al*., HIGH EFFICIENCY VIDEO CODING (HEVC) ALGORITHMS AND ARCHITECTURES at 117 (2014) (emphasis added).

256. One or more of the MediaTek '175 Products include technology for generating a plurality of test vectors from the selected vector.

> The entire ME process is made up of three coarse-to-fine procedures, namely, MV prediction, integer-pixel ME and fractional-pixel ME. First, MV prediction predicts the start search position for the following motion search by utilizing the neighboring motion information. In HEVC, Advanced Motion Vector Prediction (AMVP), a new and effective technology that predicts the starting search position by referencing the motion vector (MV) information of spatial and temporal motion vector candidates, is adopted, which derives several most probable candidates based on data from adjacent PBs and the reference picture. The displacement between the starting search position and the current coding PU is called a predictive motion vector (PMV). HEVC also introduces a merge mode to derive the motion information from spatially or temporally neighboring blocks [1].

Yongfei Zhang, Chao Zhang, and Rui Fan, *Fast Motion Estimation in HEVC Inter Coding: An Overview of Recent Advances*, PROCEEDINGS, APSIPA ANNUAL SUMMIT AND CONFERENCE 2018 at 1 (November 2018) (emphasis added).

257. One or more of the MediaTek '175 Products include technology for selecting one of the test vectors to generate an output vector.

258. Specifically, the HEVC standard arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process diagram below (see the red box).

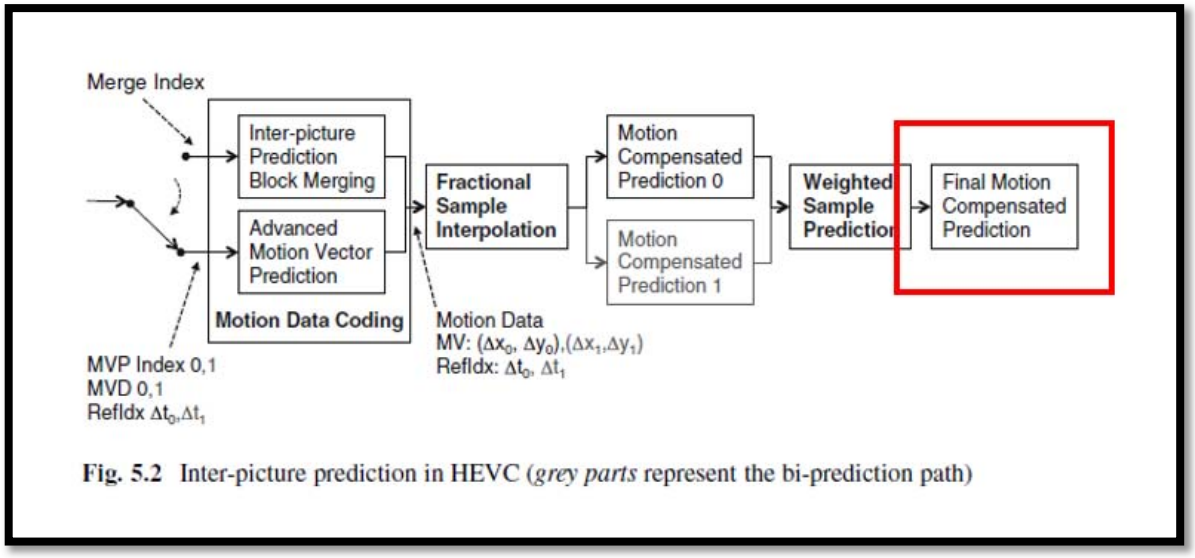


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al.*, HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

259. One or more of the MediaTek '175 Products comprise functionality wherein blocks in a picture are further divided into a plurality of blocks.

260. One or more of the MediaTek '175 Products comprises functionality wherein the vectors generated in the recursive estimation process are generated based on a difference between the output vector and the selected vector.

> It can be seen from Fig. 5.4b that only motion vectors from spatial neighboring blocks to the left and above the current block are considered as spatial MVP candidates. This can be explained by the fact that the blocks to the right and below the current block are not yet decoded and hence, their motion data is not available. Since the co-located picture is a reference picture which is already decoded, it is possible to also consider motion data from the block at the same position, from

> blocks to the right of the co-located block or from the blocks below**.** In HEVC, the block to the bottom right and at the center of the current block have been determined to be the most suitable to provide a good temporal motion vector predictor (TMVP).

Benjamin Bross, *et al., Inter-picture prediction in HEVC,* in HIGH EFFICIENCY VIDEO CODING (HEVC) at 119 (2014) (emphasis added).

261. One or more of the MediaTek '175 Products include technology for storing the output vector as one of the stored vectors for possible use in a next block.

262. MediaTek has directly infringed and continues to directly infringe the '175 patent by, among other things, making, using, offering for sale, and/or selling technology for recursive motion vector estimation, including but not limited to the MediaTek '175 Products.

263. The MediaTek '175 Products are available to businesses and individuals throughout the United States.

264. The MediaTek '175 Products are provided to businesses and individuals located in the State of Delaware.

265. By making, using, testing, offering for sale, and/or selling products and services for recursive motion vector estimation, including but not limited to the MediaTek '175 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '175 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

266. MediaTek also indirectly infringes the '175 patent by actively inducing infringement under 35 USC § 271(b).

267. MediaTek has had knowledge of the '175 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '175 patent and knew of its infringement, including by way of this lawsuit.

268. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '175 Products and had knowledge that the inducing acts would cause

infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '175 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '175 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '175 Products that have the capability of operating in a manner that infringe one or more of the claims of the '175 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '175 Products to utilize the products in a manner that directly infringe one or more claims of the '175 patent.[33] By providing instruction and training to customers and end-users on how to use the MediaTek '175 Products in a manner that directly infringes one or more claims of the '175 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '175 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '175 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '175 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '175 patent, knowing that such use constitutes infringement of the '175 patent.

269. The '175 patent is well-known within the industry as demonstrated by multiple citations to the '175 patent in published patents and patent applications assigned to technology

[33] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

companies and academic institutions. MediaTek is utilizing the technology claimed in the '175 patent without paying a reasonable royalty. MediaTek is infringing the '175 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

270. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '175 patent.

271. As a result of MediaTek's infringement of the '175 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

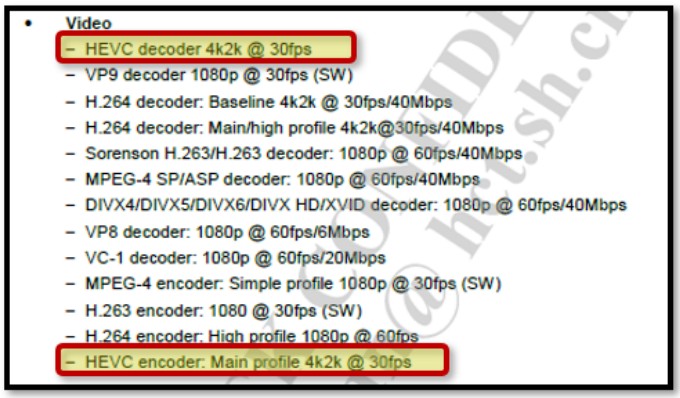
COUNT V
INFRINGEMENT OF U.S. PATENT NO. 6,996,177

272. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

273. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for motion estimation.

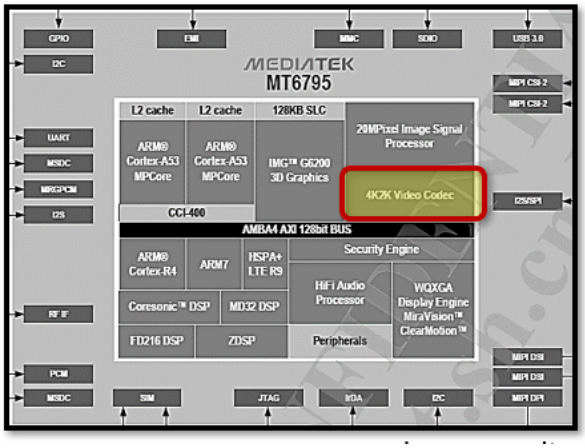
274. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '177 Product(s)").

275. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.



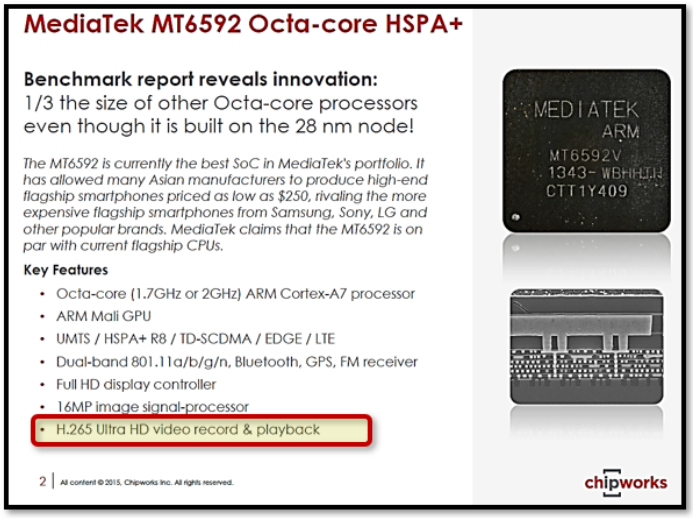
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 (August 27, 2014) (annotations added).

276. The following documentation from MediaTek shows an exemplar of the accused devices (e.g., MT6795) and in a functional diagram of the chip identifies the location of the HEVC "Video Codecs."



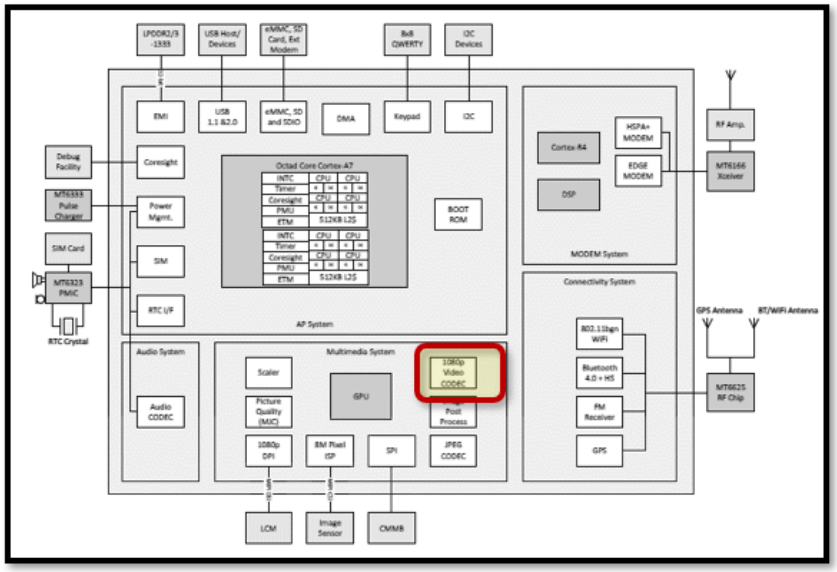
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 12 (August 27, 2014) (annotation added).

277. Analysis of the accused MediaTek '177 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

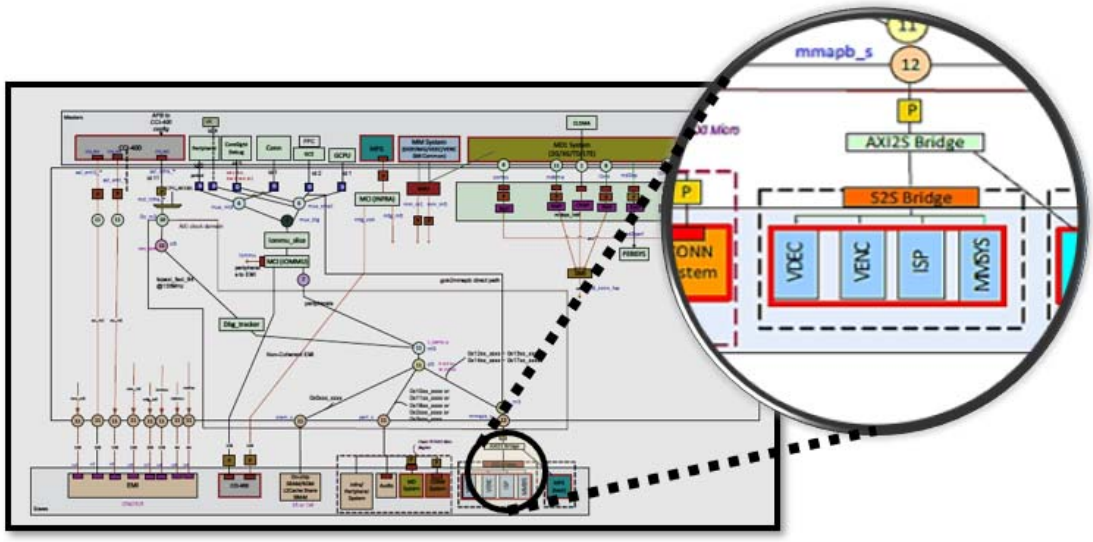
278. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (annotation added) (block diagram of the MT6592 Product showing the Video Codec for HEVC decoding that is part of the chip's multimedia system).

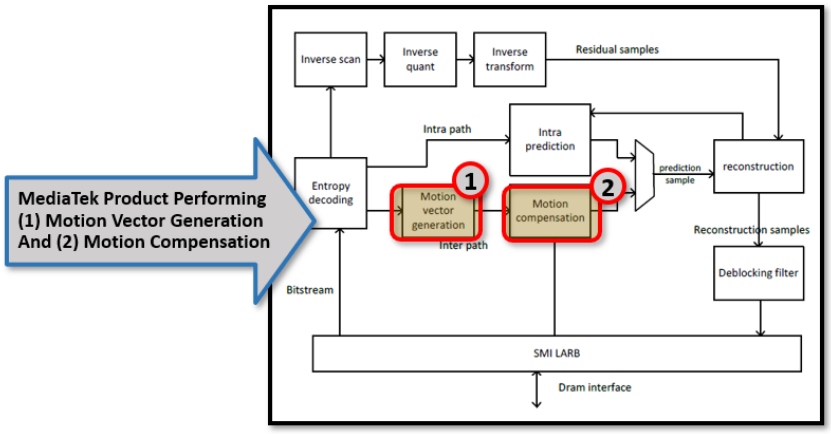
279. MediaTek documentation also establishes the accused MediaTek '177 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019).

280. MediaTek documentation also establishes that the accused MediaTek '177 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



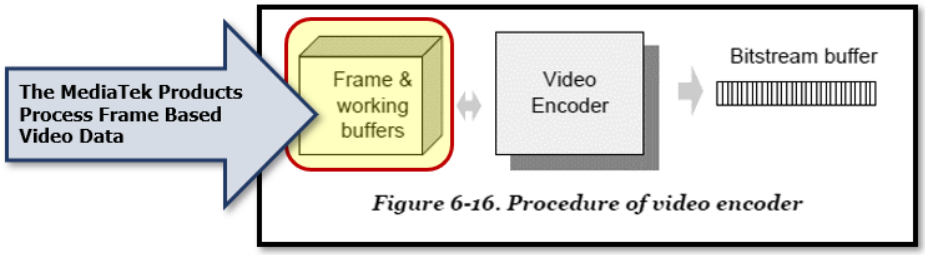
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

281. MediaTek documentation describes the encoding process used by the accused MediaTek '177 Products. For example, the below process diagram from MediaTek shows the MediaTek '177 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



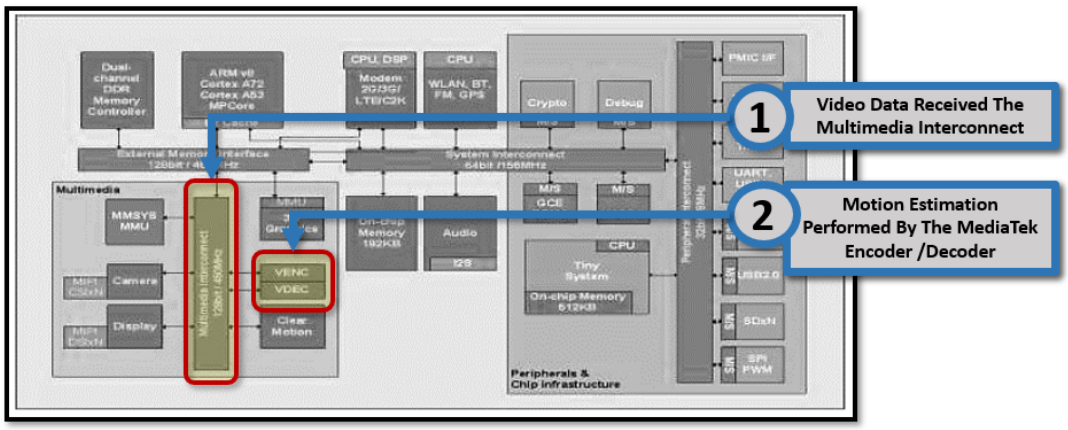
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

282. The video encoder in the accused MediaTek '177 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

283. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

284. The MediaTek '177 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '177 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

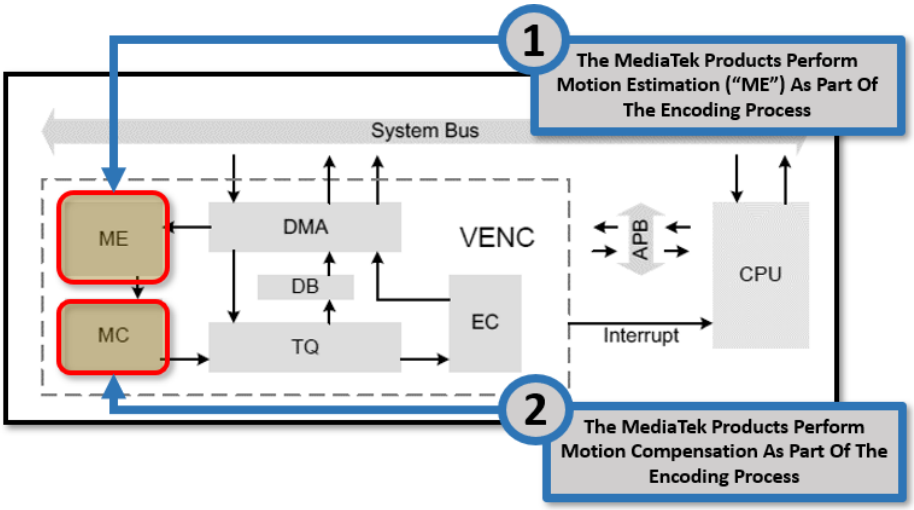
> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

285. The accused MediaTek '177 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC.

This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

286. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

287. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '177 Products in regular business operations.

288. One or more of the MediaTek '177 Products include technology for motion estimation and motion-compensated picture signal processing.

289. The MediaTek '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to the determine block-based motion vectors.

290. The MediaTek '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center.

291. Documentation from MediaTek provides additional evidence that the MediaTek '177 products contain H.265 encoding.

292. The MediaTek '177 Products use a Prediction Unit matching method wherein the motion vector represents the displacement between the current Prediction Unit in the current frame and the matching Prediction Unit in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

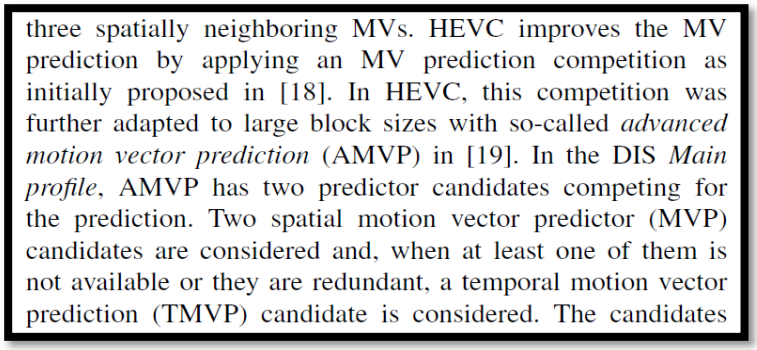
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

293. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '177 Products – necessarily infringe the '177 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '177 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '177 patent: "7.3.4 Scaling list data syntax;" 7.3.6.1 General slice segment header syntax;" "7.3.6.3 Weighted prediction parameters syntax;" "7.3.8.14 Delta QP syntax;" "7.4.4 Profile, tier and level semantics;" and "7.4.7.3 Weighted prediction parameters semantics."

294. One or more of the MediaTek '177 Products include technology for motion estimation and motion-compensated picture signal processing.

295. One or more of the MediaTek '177 Products include technology for estimating a current motion vector for a group of pixels of an image.

296. The MediaTek '177 Products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The MediaTek '177 Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.



three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

297. The MediaTek '177 Products utilize a motion vector selection process wherein the candidate motion vectors are constructed into an index and then the motion vectors are compared. "In AMVP, the motion vector selection process is composed by two steps in encoder implementation. The first step is the motion vector candidate set construction process and the second step is the best motion vector selection step. In the first step, the motion vector candidate set is organized by selecting the motion vectors spatially and temporally." Gwo-Long Li, Chuen-Ching Wang, and Kuang-Hung Chiang, *An Efficient Motion Vector Prediction Method for Avoiding AMVP Data Dependency For HEVC*, 2014 IEEE INTERNATIONAL CONFERENCE ON ACOUSTIC, SPEECH AND SIGNAL PROCESSING (ICASSP) at 13 (2014).

298. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '177 Products in regular business operations.

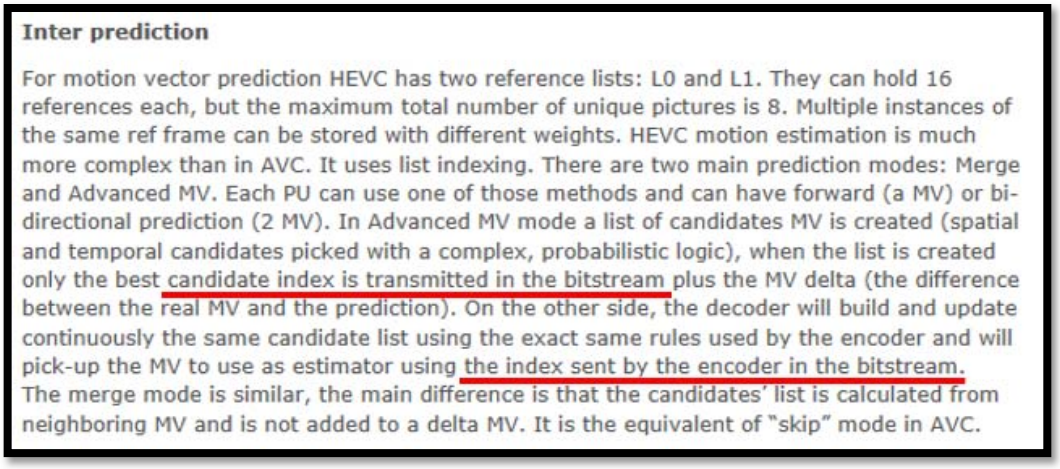
299. The MediaTek '177 Products are available to businesses and individuals throughout the United States.

300. The MediaTek '177 Products are provided to businesses and individuals located in the State of Delaware.

301. The HEVC Standard provides details regarding what would be required for a compliant HEVC encoder—e.g., the standard uses terms such as "encoding," "coding," "compressing," and other similar terms to describe the encoding process.

302. The MediaTek '177 Products use a block-based motion vector estimation process that compares a plurality of candidate vectors to determine block-based motion vectors. The MediaTek '177 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image.

303. The MediaTek '177 Products determine at least a most frequently occurring block-based motion vector. The MediaTek '177 Products contain functionality wherein the motion vector prediction performed includes the ability to transmit in the bitstream the candidate index of motion vectors. Documentation of the encoding process states that the encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

304. Any implementation of the HEVC standard would infringe the '177 patent as every possible implementation of the standard requires: compliant devices to carry out a global motion vector estimation process using the most frequently occurring block-based motion vectors. This process of vector candidate selection allows the MediaTek '177 Products to obtain a global motion vector. Specifically, the HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, if there are two spatial motion vectors that are identical, that is determined to be the most frequently occurring block-based motion vector and the frequently occurring spatial motion vector and temporal motion vector candidate are used to generate the global motion vector. "In HEVC, this competition was further adapted to large block sizes with so-called advanced motion vector prediction (AMVP). In the DIS Main profile, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered." Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for*

Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22 No. 12 (December 2012).

305. The MediaTek '177 Products apply a global motion vector as a candidate vector to the block-based motion vector estimation process. Specially, the MediaTek '177 Products calculate the global motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process diagram below (as shown in the below figure) and applied to the block-based motion vector estimation process.

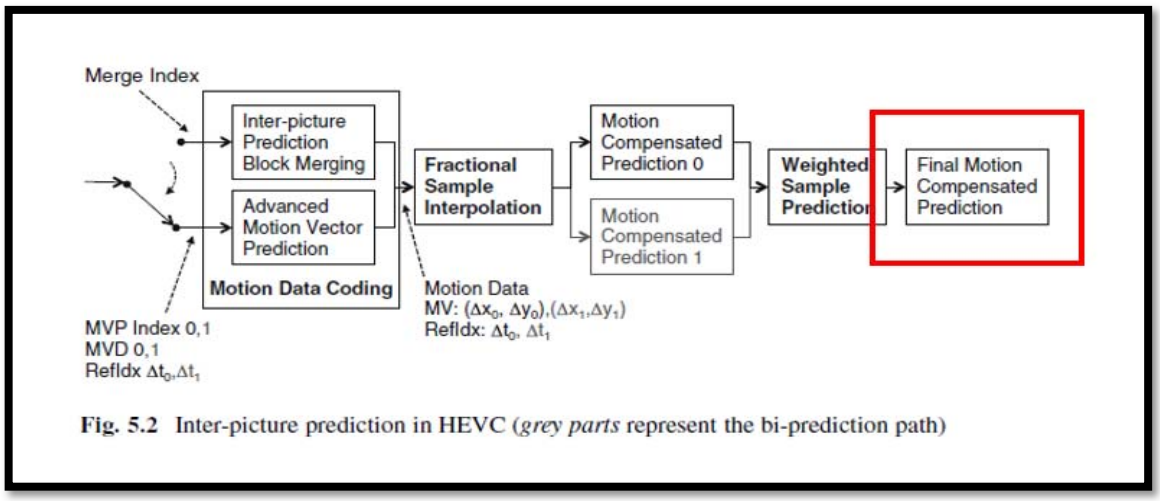


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

306. Further, the MediaTek '177 Products enable AMVP wherein several of the most probable candidate vectors based on data from adjacent prediction blocks are used to create a global estimation vector and that vector is applied to the block-based motion estimation functionality.

> Motion vector signaling: Advanced motion vector prediction (AMVP) is used, including derivation of several most probable candidates based on data from adjacent PBs and the reference picture. A "merge" mode for MV coding can be also used, allowing the inheritance of MVs from neighboring PBs. Moreover,

> compared to H.264/MPEG-4 AVC, improved "skipped" and "direct" motion inference are also specified.

Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, PRE-PUBLICATION DRAFT, TO APPEAR IN IEEE TRANS. ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY at 3 (December 2012) (emphasis added).

307. MediaTek has directly infringed and continues to directly infringe the '177 patent by, among other things, making, using, offering for sale, and/or selling products and services for motion estimation and motion-compensated picture signal processing.

308. The MediaTek '177 Products comprise methods and devices for motion estimation and motion-compensated picture signal processing.

309. The MediaTek '177 Products incorporate a motion vector estimation method and device that carries out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors.

310. The MediaTek '177 Products determine at least a most frequently occurring block-based motion vector.

311. The MediaTek '177 Products carry out a global motion vector estimation process using at least the most frequently occurring block-based motion vector to obtain a global motion vector.

312. The MediaTek '177 Products applies the global motion vector as a candidate vector to the block-based motion vector estimation process.

313. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the MediaTek '177 Products, MediaTek has injured Dynamic Data and is liable for directly infringing one or more claims of the '177 patent, including at least claim 1, pursuant to 35 U.S.C. § 271(a).

314. MediaTek also indirectly infringes the '177 patent by actively inducing infringement under 35 U.S.C. § 271(b).

315. MediaTek has had knowledge of the '177 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '177 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '177 Patent based on prior communications that identified the '177 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

316. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '177 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '177 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '177 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '177 Products that have the capability of operating in a manner that infringe one or more of the claims of the '177 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '177 Products to utilize the products in a manner that directly infringe one or more claims of the '177 patent.[34] By providing instruction and training to customers and end-users on how to use the MediaTek '177 Products in a manner that directly infringes one or more claims of the '177 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '177 patent. MediaTek engaged in such inducement to promote the sales of

[34] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

the MediaTek '177 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '177 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '177 patent, knowing that such use constitutes infringement of the '177 patent.

317. The '177 patent is well-known within the industry as demonstrated by multiple citations to the '177 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '177 patent without paying a reasonable royalty. MediaTek is infringing the '177 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

318. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '177 patent.

319. As a result of MediaTek's infringement of the '177 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

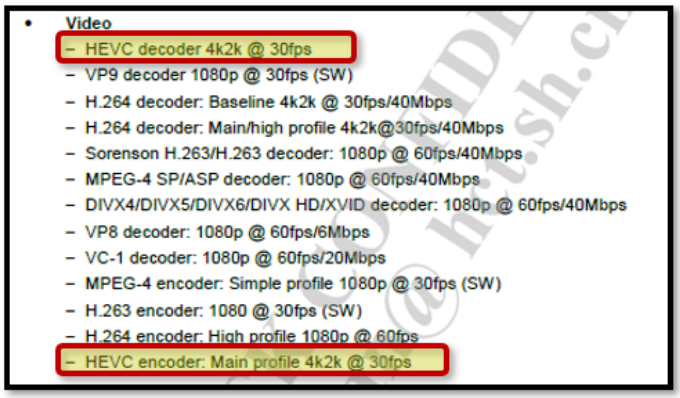
COUNT VI
INFRINGEMENT OF U.S. PATENT NO. 7,010,039

320. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

321. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for detecting motion.

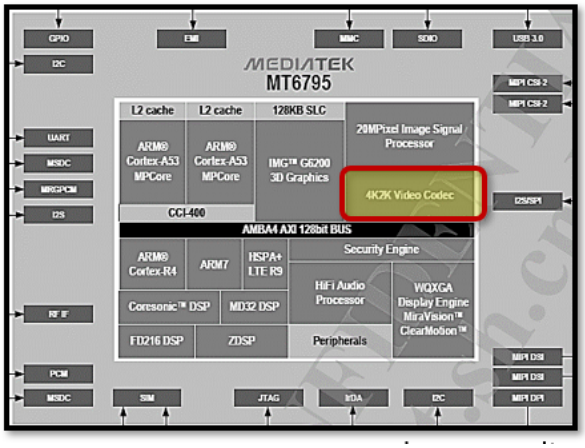
322. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '039 Product(s)").

323. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.



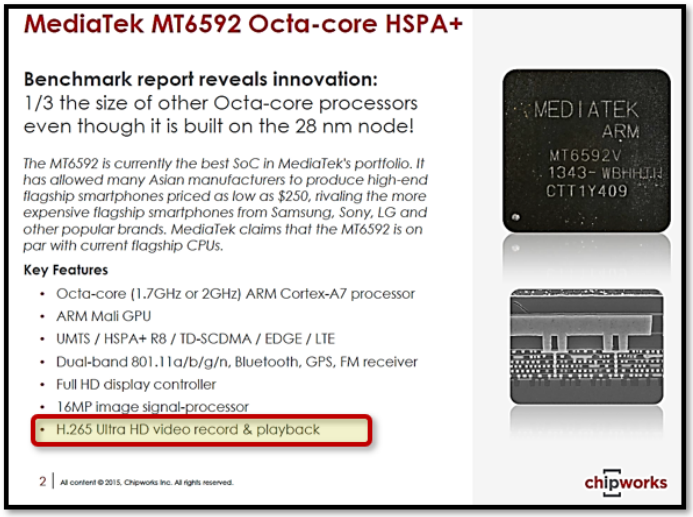
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 (August 27, 2014) (annotations added).

324. The following documentation from MediaTek shows an exemplar of the accused devices (e.g., MT6795) and in a functional diagram of the chip identifies the location of the HEVC "Video Codecs."



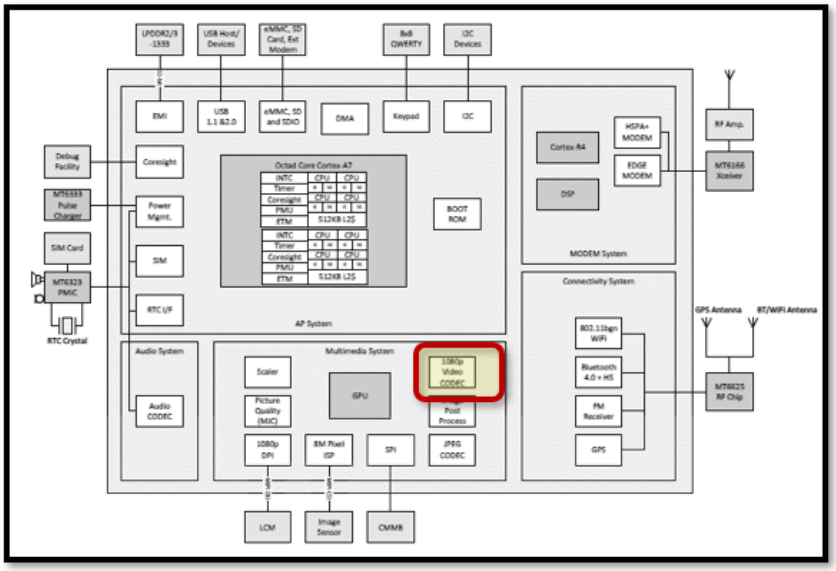
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 12 (August 27, 2014) (annotation added).

325. Analysis of the accused MediaTek '039 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

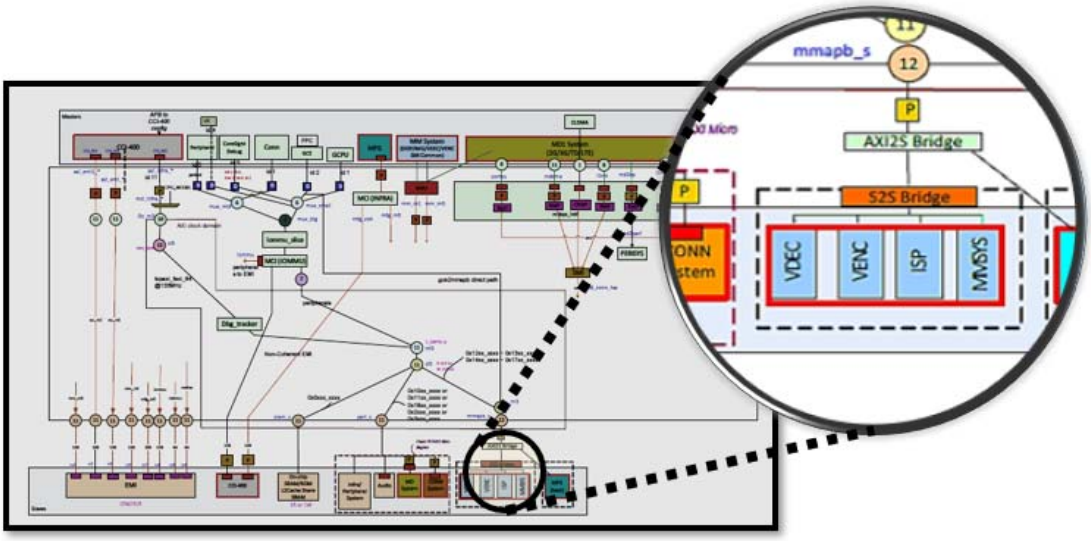
326. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (annotation added) (block diagram of the MT6592 Product showing the Video Codec for HEVC decoding that is part of the chip's multimedia system).

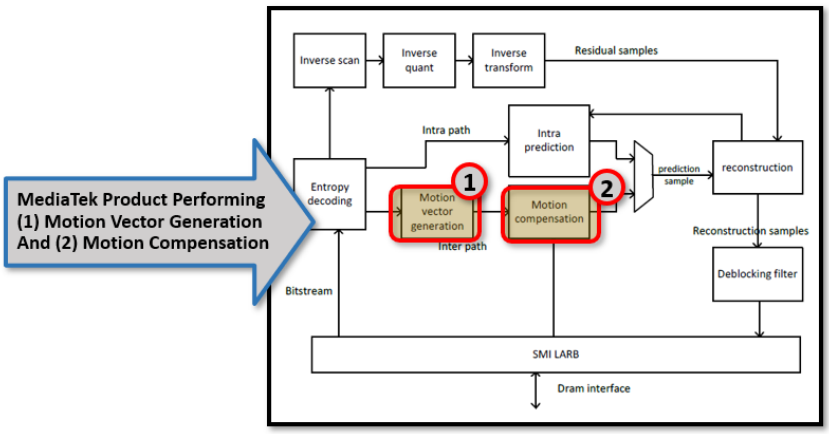
327. MediaTek documentation also establishes the accused MediaTek '039 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019).

328. MediaTek documentation also establishes that the accused MediaTek '039 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



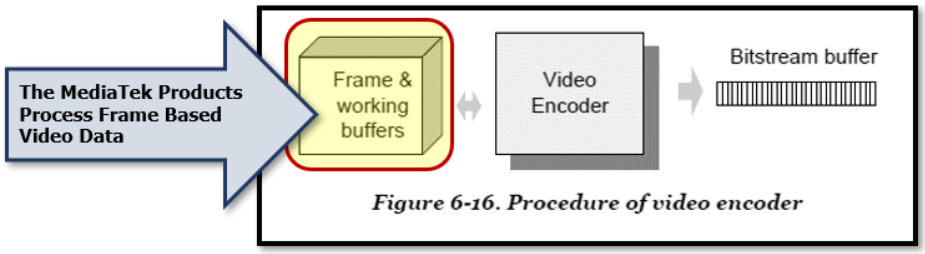
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

329. MediaTek documentation describes the encoding process used by the accused MediaTek '039 Products. For example, the below process diagram from MediaTek shows the MediaTek '039 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



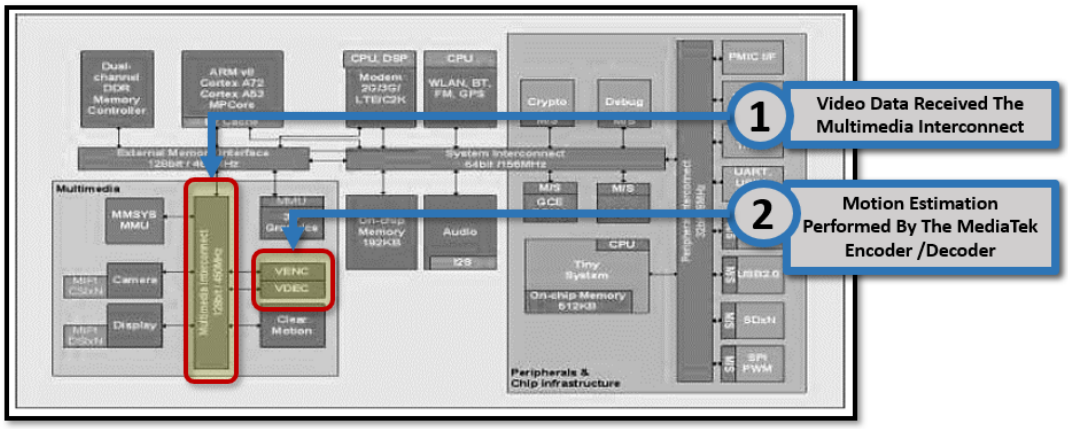
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

330. The video encoder in the accused MediaTek '039 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

331. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

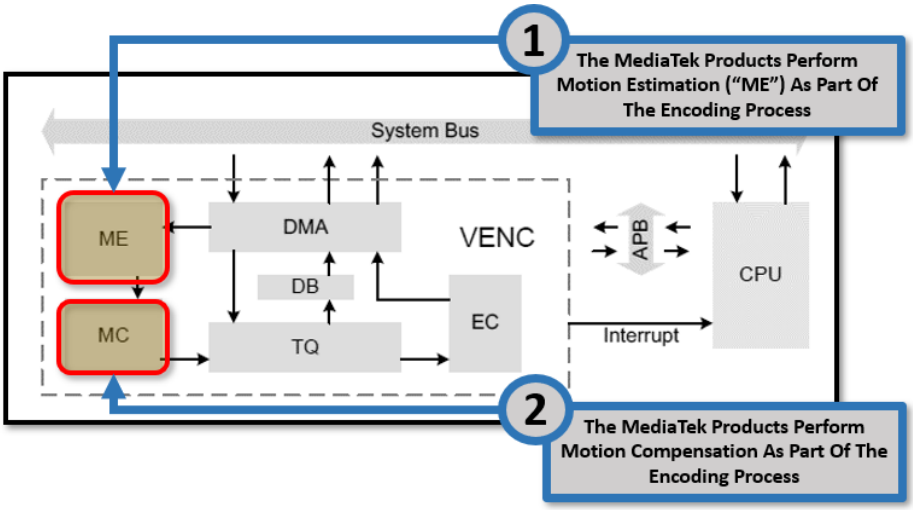
332. The MediaTek '039 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '039 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

333. The accused MediaTek '039 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC. This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

334. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

335. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '039 Products in regular business operations.

336. The MediaTek '039 Products contain functionality wherein a criterion function for candidate vectors is optimized. The criterion function depends on data obtained from the previous and next images in the video data stream. The optimizing is carried out at a temporal intermediate position in non-covered and covered areas. The following excerpts explain how HEVC is a form of encoding video information using a temporal intermediate position between previous and next images.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess. *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016)

> HEVC features both low- and high-level methods for dependency removal which can be used to leverage multi-core processors [13]. Only the three high-level mechanisms slices, tiles and WPP are of interest for this work. It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC's basic processing unit. CTUs have a maximum size of 64×64 luma pixels and are recursively split into square-shaped Coding Units (CUs), which contain Prediction Units (PUs) and Transform Units (TUs) [14].

Stefan Radicke, *et al*., *Many-Core HEVC Encoding Based on Wavefront Parallel Processing and GPU -accelerated Motion Estimation*, E-BUSINESS AND TELECOMMUNICATIONS: 11TH INTERNATIONAL JOINT CONFERENCE at 296 (2015) ("HEVC feature both low- and high-level methods for dependency removal which can be used to leverage multi-core processors. . . It is important to note that all of them subdivide individual video frames based on CTUs which are HEVC' basic processing unit.").

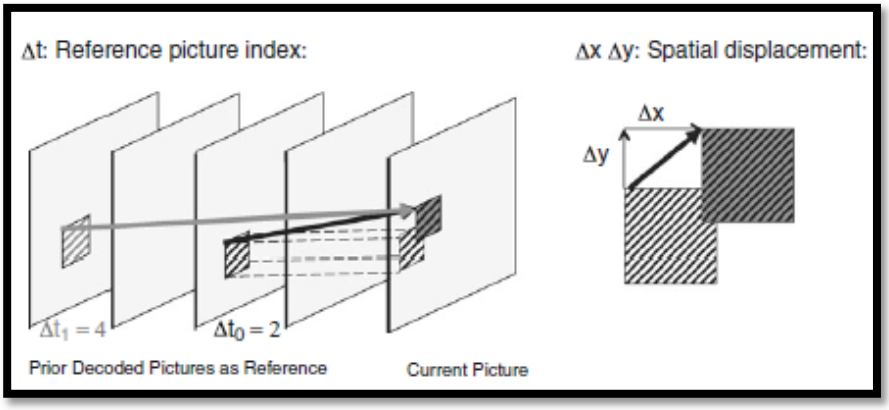
337. The MediaTek '039 Products receive encoded video data that is encoded using inter-frame coding. The encoded video stream received by the MediaTek Products are coded using its predecessor frame and subsequent frame. Inter-prediction used in the encoded video data received by the MediaTek Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit ***temporal statistical dependences,*** intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

338. The encoded video stream received by the MediaTek Products are encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a

predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



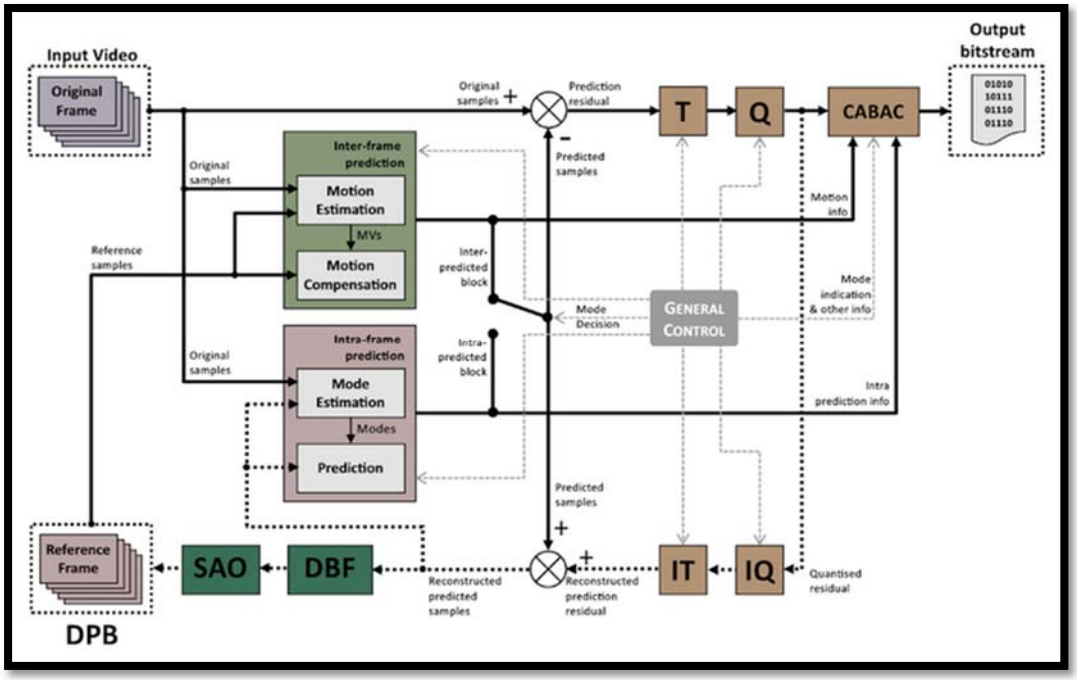
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

339. The following excerpt from an article describing the architecture of the encoded video stream received by the MediaTek '039 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . or two reference frames (bi-prediction) to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

340. The following diagram shows how the MediaTek '039 Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across frames.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

341. The MediaTek '039 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the MediaTek Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list.

These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

342. The MediaTek '039 Products optimize the selection of candidate vectors by calculation a temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas. Specifically, the encoding process for video data received by the MediaTek Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

343. The "Overview of Design Characteristics" in the HEVC specification describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."

> compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 0.7 (April 2015) (annotation added).

344. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '039 Products – necessarily infringe the '039 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '039 patent, including but not limited to claim 13. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to

MediaTek's infringement of the '039 patent: "5.3 Logical operators;" "5.10 Variables, syntax elements and tables;" "5.11 Text description of logical operations;" "7.2 Specification of syntax functions and descriptors;" "7.3.1 NAL unit syntax;" "7.3.2 Raw byte sequence payloads, trailing bits and byte alignment syntax;" "7.3.5 Supplemental enhancement information message syntax;" "7.4.2 NAL unit semantics;" and "7.4.6 Supplemental enhancement information message semantics."

345. The MediaTek '039 Products are available to businesses and individuals throughout the United States.

346. The MediaTek '039 Products are provided to businesses and individuals located in the State of Delaware.

347. MediaTek has directly infringed and continues to directly infringe the '039 patent by, among other things, making, using, offering for sale, and/or selling technology for detecting motion, including but not limited to the MediaTek '039 Products.

348. The MediaTek '039 Products detect motion at a temporal intermediate position between previous and next images.

349. The MediaTek '039 Products carry out the optimization at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

350. The MediaTek '039 Products detect motion at a temporal intermediate position between previous and next images.

351. The MediaTek '039 Products utilize a criterion function for candidate vectors that is optimized.

352. The MediaTek ‘039 Products utilize a criterion function that depends on data from both previous and next images and in which the optimizing is carried out at the temporal intermediate position in non-covering and non-uncovering areas, characterized in that the optimizing is carried out at the temporal position of the next image in covering areas and at the temporal position of the previous image in uncovering areas.

353. By making, using, testing, offering for sale, and/or selling products and services, including but not limited to the MediaTek ‘039 Products, MediaTek has injured Dynamic Data and is liable for directly infringing one or more claims of the ‘039 patent, including at least claim 13, pursuant to 35 U.S.C. § 271(a).

354. MediaTek also indirectly infringes the ‘039 patent by actively inducing infringement under 35 U.S.C. § 271(b).

355. MediaTek has had knowledge of the ‘039 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the ‘039 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the ‘039 Patent based on prior communications that identified the ‘039 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

356. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek ‘039 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the ‘039 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the ‘039 patent and with the knowledge that the induced acts would constitute infringement. For

example, MediaTek provides the MediaTek '039 Products that have the capability of operating in a manner that infringe one or more of the claims of the '039 patent, including at least claim 13, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '039 Products to utilize the products in a manner that directly infringe one or more claims of the '039 patent.[35] By providing instruction and training to customers and end-users on how to use the MediaTek '039 Products in a manner that directly infringes one or more claims of the '039 patent, including at least claim 13, MediaTek specifically intended to induce infringement of the '039 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '039 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '039 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '039 patent, knowing that such use constitutes infringement of the '039 patent.

357. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '039 patent.

358. As a result of MediaTek's infringement of the '039 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

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[35] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

COUNT VII
INFRINGEMENT OF U.S. PATENT NO. 7,894,529

359. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

360. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for determining motion vectors that are each assigned to individual image regions.

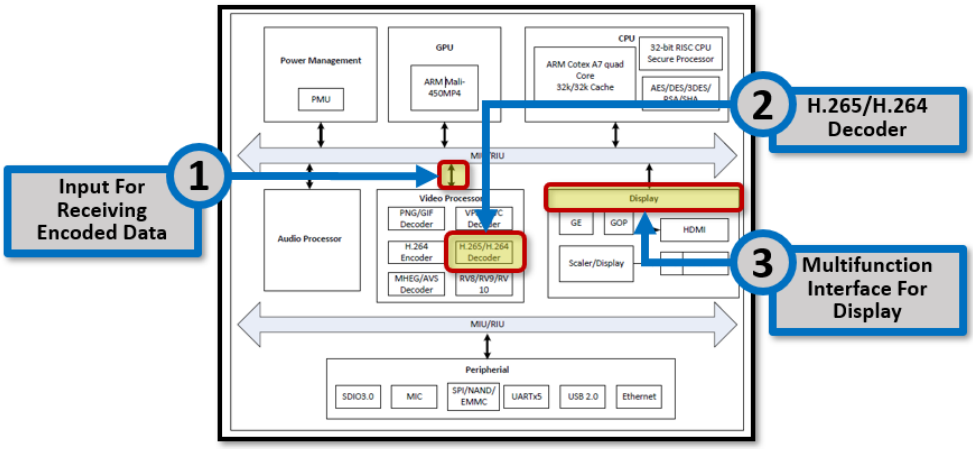
361. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek devices that contain H.265 decoding functionality including but not limited to: MediaTek Automotive Products (MediaTek Autus I20 (MT2712)); MediaTek Mobile Products (MediaTek Helio A11, MediaTek Helio P10, MediaTek Helio P18, MediaTek Helio P20, MediaTek Helio P22, MediaTek Helio P23, MediaTek Helio P25, MediaTek Helio P30, MediaTek Helio P60, MediaTek Helio P70, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, MediaTek MT6732, MediaTek MT6735, MediaTek MT6738, MediaTek MT6739, MediaTek MT6750, MediaTek MT6752, and MediaTek MT6753); MediaTek Digital TV Products (MediaTek MT5582, MediaTek MT5596, and MediaTek MT5597); MediaTek Home Products (MediaTek MT8581, MediaTek MT8685, and MediaTek MT8693); and MediaTek Tablet Products (MediaTek MT8163V/A, MediaTek MT8163V/B, MediaTek MT8167A, MediaTek MT8167B, MediaTek MT8173, MediaTek MT8176, MediaTek MT8735B, MediaTek MT8735D, MediaTek MT8735M, MediaTek MT8735P, MediaTek MT8783, and MediaTek MT8785) (collectively, the "MediaTek Products").

362. MediaTek designs, makes, sells, offers to sell, imports, and/or uses products that contain HEVC decoding technology, including but not limited to the MStar System on Chip

("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MStar Product(s)").

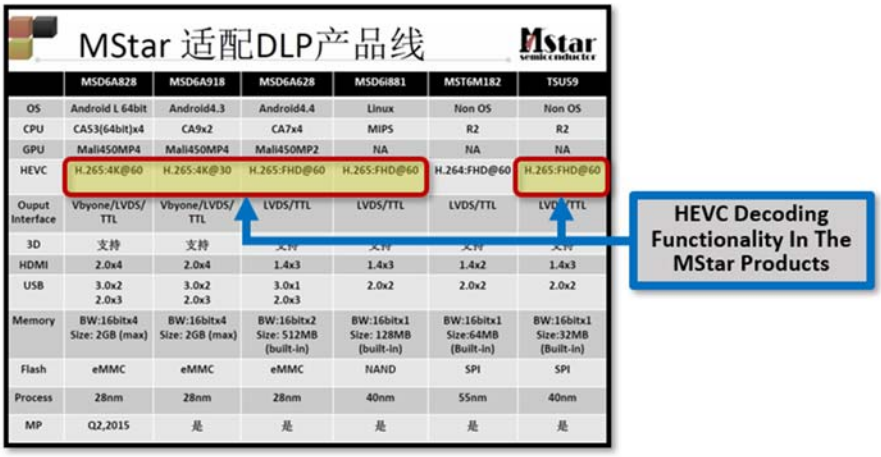
363. The MediaTek Products and MStar Products (collectively, the "MediaTek '529 Product(s)") directly infringe the '529 patent.

364. The MStar Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

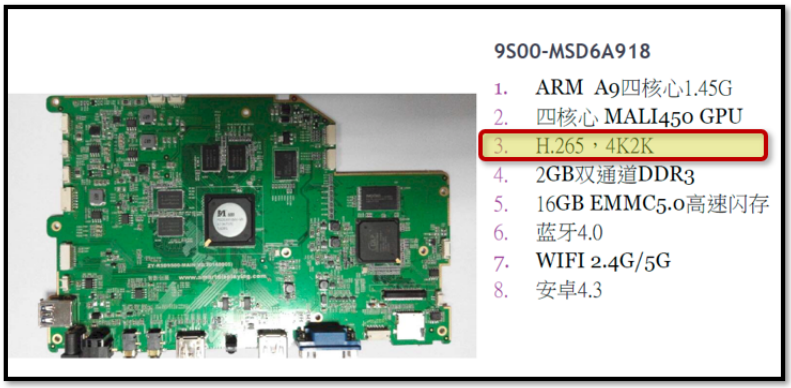
365. Documentation regarding the MStar Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MStar Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



	MSD6A828	MSD6A918	MSD6A628	MSD6I881	MST6M182	TSU59
OS	Android L 64bit	Android4.3	Android4.4	Linux	Non OS	Non OS
CPU	CA53(64bit)x4	CA9x2	CA7x4	MIPS	R2	R2
GPU	Mali450MP4	Mali450MP4	Mali450MP2	NA	NA	NA
HEVC	H.265:4K@60	H.265:4K@30	H.265:FHD@60	H.265:FHD@60	H.264:FHD@60	H.265:FHD@60
Ouput Interface	Vbyone/LVDS/ TTL	Vbyone/LVDS/ TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL
3D	支持	支持	支持	支持	支持	支持
HDMI	2.0x4	2.0x4	1.4x3	1.4x3	1.4x2	1.4x3
USB	3.0x2 2.0x3	3.0x2 2.0x3	3.0x1 2.0x3	2.0x2	2.0x2	2.0x2
Memory	BW:16bitx4 Size: 2GB (max)	BW:16bitx4 Size: 2GB (max)	BW:16bitx2 Size: 512MB (built-in)	BW:16bitx1 Size: 128MB (built-in)	BW:16bitx1 Size:64MB (Built-in)	BW:16bitx1 Size:32MB (Built-in)
Flash	eMMC	eMMC	eMMC	NAND	SPI	SPI
Process	28nm	28nm	28nm	40nm	55nm	40nm
MP	Q2,2015	是	是	是	是	是

MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

366. The MStar Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MStar Products that contain a decoder that conforms to the H.265 standard.



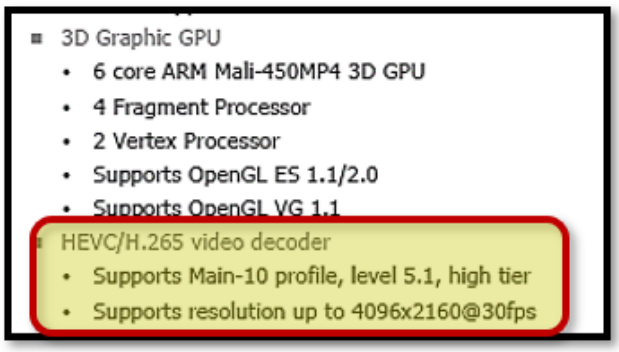
Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product contains a decoder compliant with the H.265 standard).

367. Datasheets from MediaTek also establish that the accused MStar Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states:

"all in one 的SOC 芯片，芯片主要功能规格参数如下： 支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60"[36]

MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

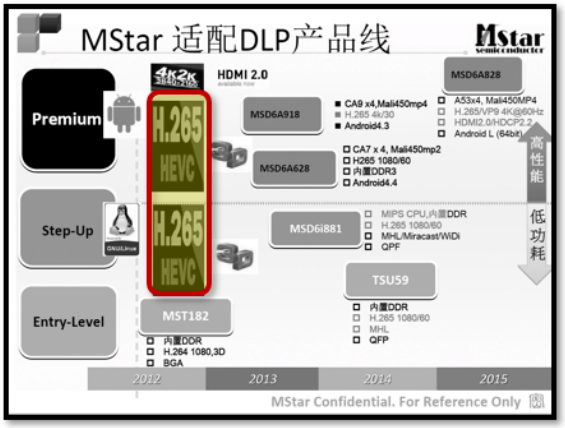
368. Similarly, the MediaTek datasheet for the MSO9280MC Product identifies that it contains an HEVC H.265 decoder.



MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added).

[36] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."

369. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MStar Products.



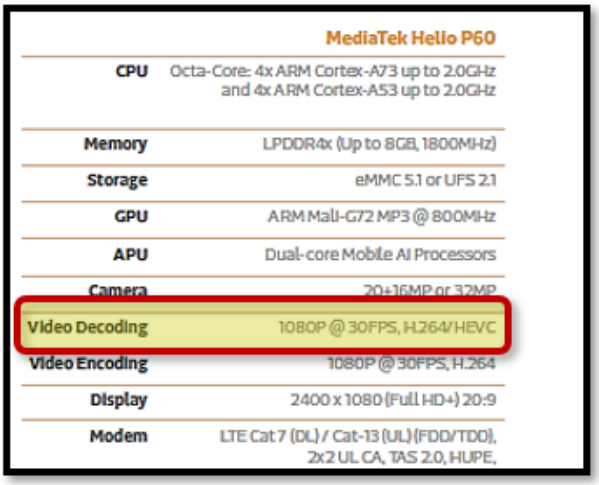
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

370. Documentation from MediaTek customers such as TCL that incorporate the accused MStar Products into devices such as televisions also identifies the accused MStar Products as containing an H.265 decoder.

类别	项目	L55H8800-CUD
输入和输出	ATV/DTV(DVB-C/DTMB) (PAL D/K I B/G)	✓
	HDMI (480i/p,576i/p,720p up to1080i/p,4K2K,with HDCP)	3 路，HDMI2 与 MHL 复用 支持 4K2K@30Hz 支持 H.265 格式
	VGA	无
	VGA/DVI audio	与 YPbPr 共用
	YPbPr (可支持 480i 到 1080p)	无
	SPDIF output	与AVout共用

TCL PRODUCT BRIEF: MS918 机芯手册V1.0 at 35 (March 18, 2015) (annotation added) (showing that the MS918 chip from MStar contains a H.265 compliant decoder).

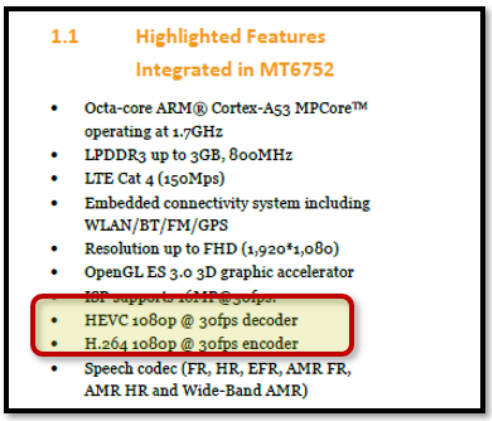
371. MediaTek's datasheets identify that the MediaTek Products (*e.g.*, MediaTek Helio P60) contain a video decoder that complies with the H.265 standard.



	MediaTek Helio P60
CPU	Octa-Core: 4x ARM Cortex-A73 up to 2.0GHz and 4x ARM Cortex-A53 up to 2.0GHz
Memory	LPDDR4x (Up to 8GB, 1800MHz)
Storage	eMMC 5.1 or UFS 2.1
GPU	ARM Mali-G72 MP3 @ 800MHz
APU	Dual-core Mobile AI Processors
Camera	20+16MP or 32MP
Video Decoding	1080P @ 30FPS, H.264/HEVC
Video Encoding	1080P @ 30FPS, H.264
Display	2400 x 1080 (Full HD+) 20:9
Modem	LTE Cat 7 (DL) / Cat-13 (UL) (FDD/TDD), 2x2 UL CA, TAS 2.0, HUPE,

MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 at 2 (2018) (annotation added).

372. Technical briefs from MediaTek similarly identify the accused MediaTek products as containing a decoder that complies with the HEVC standard.

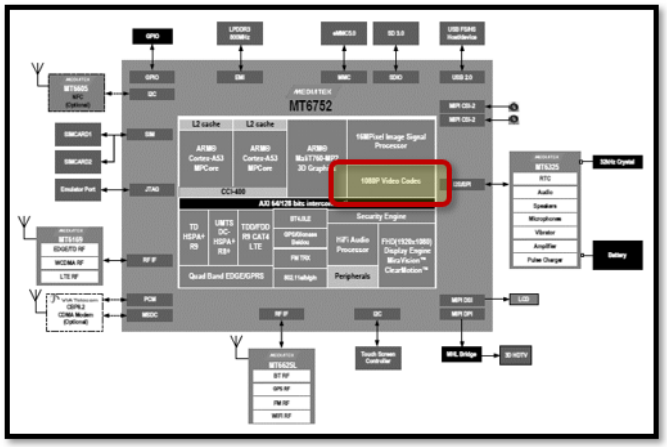


1.1 Highlighted Features Integrated in MT6752

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.7GHz
- LPDDR3 up to 3GB, 800MHz
- LTE Cat 4 (150Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

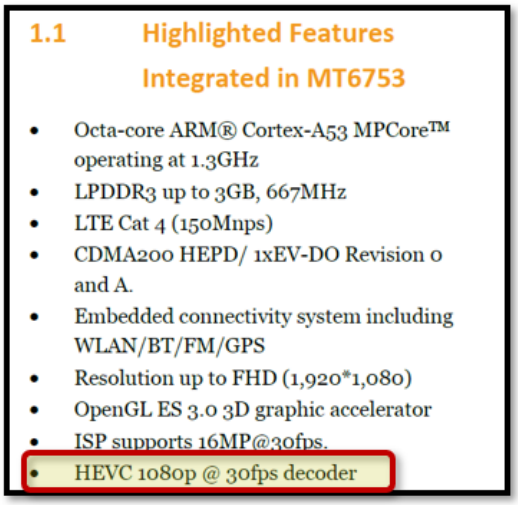
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (June 10, 2014) (annotation added) ("The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.").

373. MediaTek documentation relating to the accused MediaTek Products (*e.g.*, MT6752) describe the chips as a "brand-new generation smart phone SoC integrating MediaTek LTE modem, Octa-core ARM® Cortex-A53 MPCoreTM, 3D graphics and high-definition 1080p video decoder."



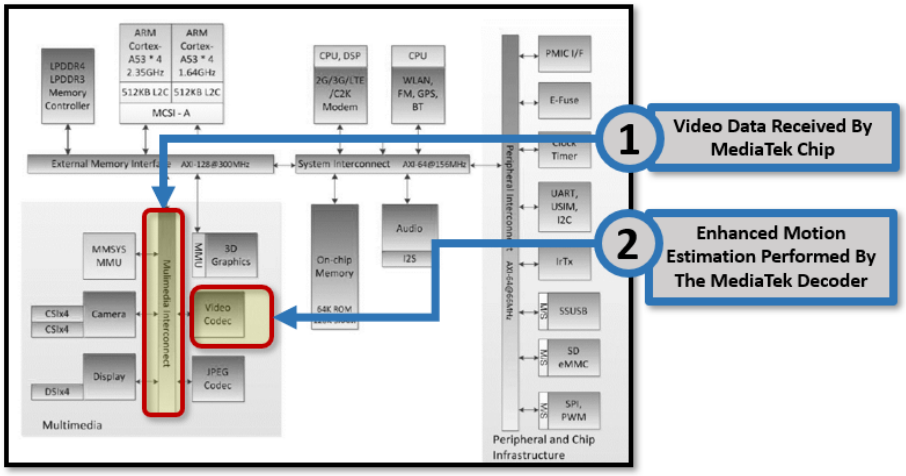
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 15 (June 10, 2014) (annotation showing the HEVC video decoder).

374. MediaTek documentation for the accused products identifies products such as the MT6753 Application Processor contains a video decoder that complies with the HEVC standard.



MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (November 27, 2014) ("The chip integrates Octa-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.").

375. MediaTek documentation shows the interconnects that connect the video decoding engine to the rest of the application processor. For example, MediaTek documentation for the MT6757 chip (i.e., the Helio P20 chip) shows connections to the video codec engine.



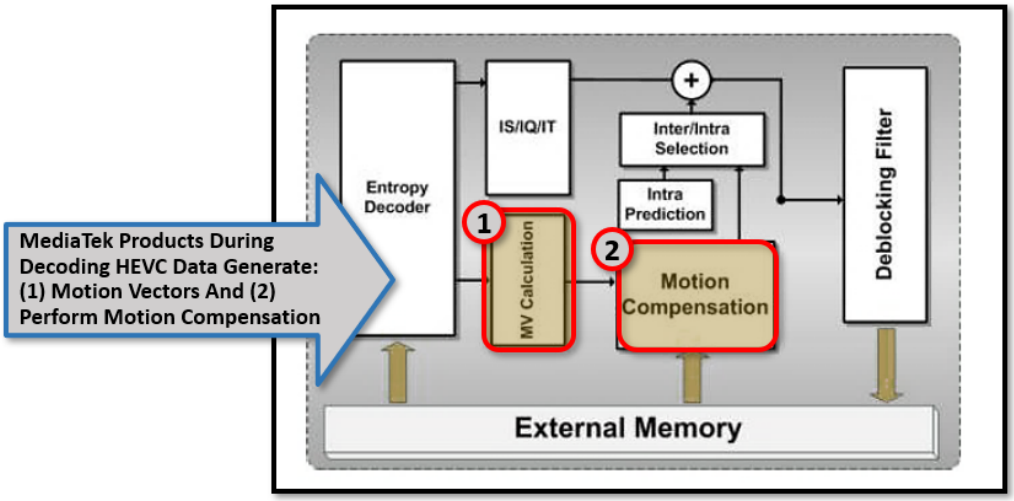
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 18 (June 20, 2016) (annotations added).

376. MediaTek technical documentation establishes the accused products (e.g., the MT6757 application processor) include an HEVC compliant decoder.

> The application processor, an Octa-core ARM® Cortex-A53 MPCoreTM equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

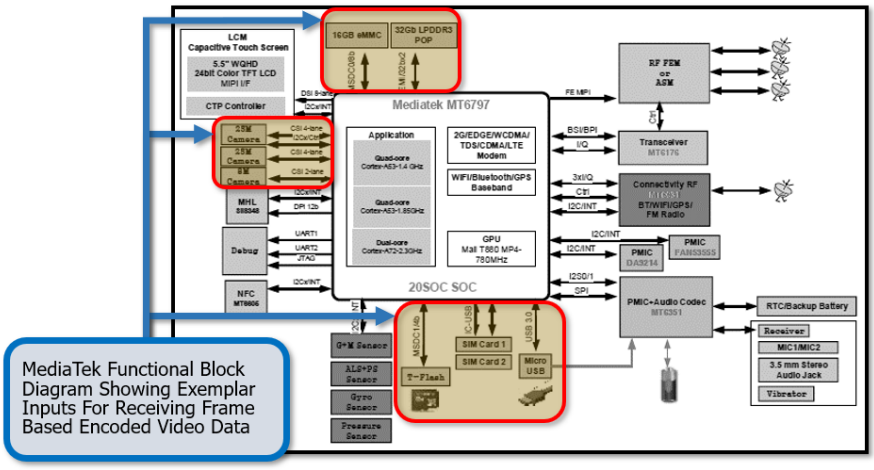
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 7 (June 20, 2016) (emphasis added) (describing that the MediaTek product includes a decoder for "HEVC 4K @ 30fps").

377. The architecture and core blocks of HEVC decoder ("VDEC") are shown in the below diagram including the following functional components: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra prediction, Motion Compensation, and De-Blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is sent to the display stage.



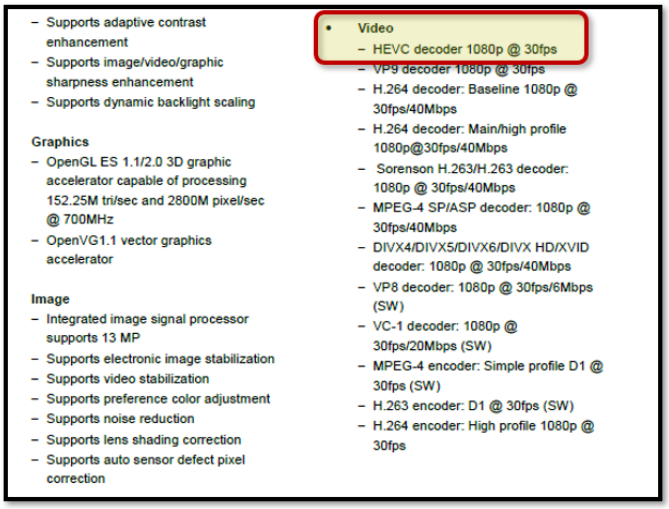
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 276 (July 19, 2016) (annotations added)

378. The accused MediaTek '529 Products receive HEVC encoded data through a variety of inputs. The below excerpt from MediaTek's technical documentation identifies the inputs for receiving HEVC encoded video data as part of the decoding process.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 12 (July 19, 2016) (annotations added) (showing a high-level functional block diagram of the MT6797 product).

379. MediaTek documentation similarly identifies that the MediaTek '529 Products contain an "HEVC decoder" as shown in the below excerpt from a MediaTek Technical Brief for the MT6592 Octa-Core Smartphone Application Processor.



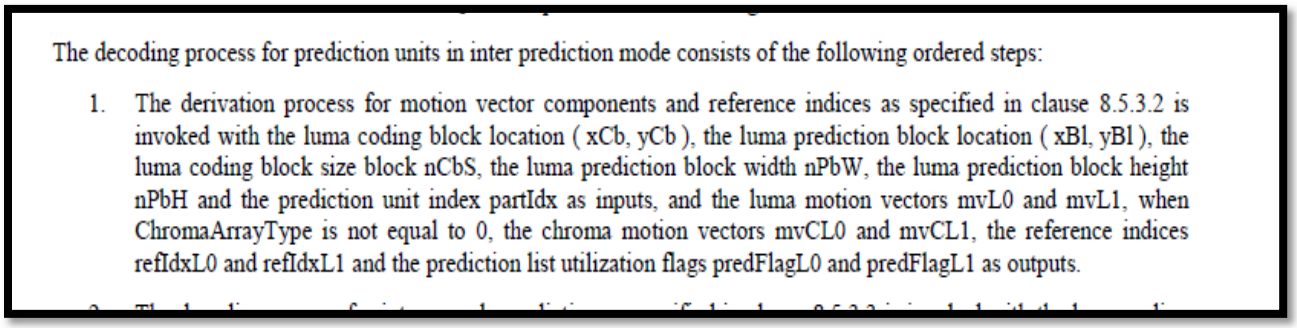
MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 8 and 11 (July 6, 2013) (annotation added) ("Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6592 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.7GHz Octa-core ARM® Cortex-A7 MPCoreTM, 3D graphics and high-definition 1080p video decoder.").

380. The MediaTek '529 Products incorporate a decoding unit for decoding the frame of the received video data. The decoding utilizes a second frame recovery unit that is a decoding motion vector. Specifically, the encoding and decoding process for video data received by the MediaTek '529 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

381. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '529 Products – necessarily infringe the '529 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the '529 patent, including but not limited to claim 1. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018). The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '529 patent: "3.110 Prediction Unit Definition;" "6.3.2 Block and quadtree structures;" "6.3.3 Spatial or component-wise partitioning;" "6.4.2 Derivation process for prediction block availability;" "7.3.8.5 Coding unit syntax;" "7.3.8.6 Prediction unit syntax;"

"8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process."

382. The MediaTek '529 Products comply with the HEVC standard, which requires determining motion vectors assigned to individual image regions of an image.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

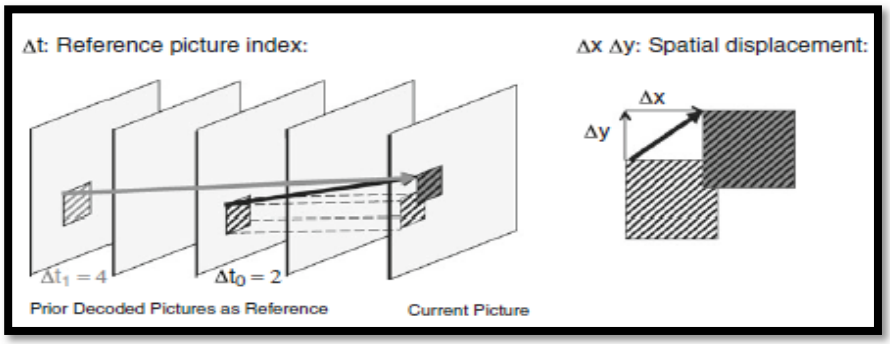
1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § 8.5.3.1 (February 2018).

383. MediaTek has directly infringed and continues to directly infringe the '529 patent by, among other things, making, using, offering for sale, and/or selling technology for implementing a motion estimation technique that assigns at least one motion vector to each of the image blocks and generating a modification motion vector for at least the first image block.

384. The encoded video stream received by the MediaTek '529 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each

block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

385. The MediaTek '529 Products perform the step of selecting a second image block where the motion vector that is assigned to the first image block passes. Specifically, the MediaTek '529 Products, in the use of inter-picture prediction, look at two or more blocks in different frames wherein the vector passes through both the first and second image block. The following excerpts from documentation relating the video estimation technique used by the MediaTek '529 Products explains how HEVC uses motion estimation to determine a temporal intermediate position between two images wherein two image blocks are selected that have a motion vector passing in both the first and second image block.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess, *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

386. The MediaTek '529 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the MediaTek '529 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the MediaTek '529 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., Vol. 22, No. 12, p. 1654 (December 2012) (emphasis added).

387. The following excerpt from an article describing the architecture of the video stream received by the MediaTek '529 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

388. Any implementation of the HEVC standard infringes the '529 patent as every possible implementation of the standard requires: determining at least a second image block through which the motion vector assigned to the first image block at least partially passes; generating the modified motion vector as a function of a motion vector assigned to at least the

second image block; and assigning the modified motion vector as the motion vector to the first image block. Further, the functionality of the motion estimation process in HEVC uses "motion vector[s]: A two-dimensional vector used for *inter prediction* that provides an offset from the coordinates in the decoded picture to the coordinates in a reference picture," as defined in definition 3.83 of the *ITU-T H.265 Series H: Audiovisual and Multimedia Systems* (2018) (emphasis added); *see also, e.g.,* Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1650 (December 2012) ("The encoder and decoder generate identical inter picture prediction signals by applying motion compensation (MC) using the MV and mode decision data.").

389. The motion estimation done by the MediaTek '529 Products is done through a PU matching method where the motion vector represents the displacement between the current PU in the current frame and the matching PU in the reference frame.

> Motion estimation compares the current prediction unit (PU) with the spatially neighboring PUs in the reference frames, and chooses the one with the least difference to the current PU. The displacement between the current PU and the matching PU in the reference frames is signaled using a motion vector.

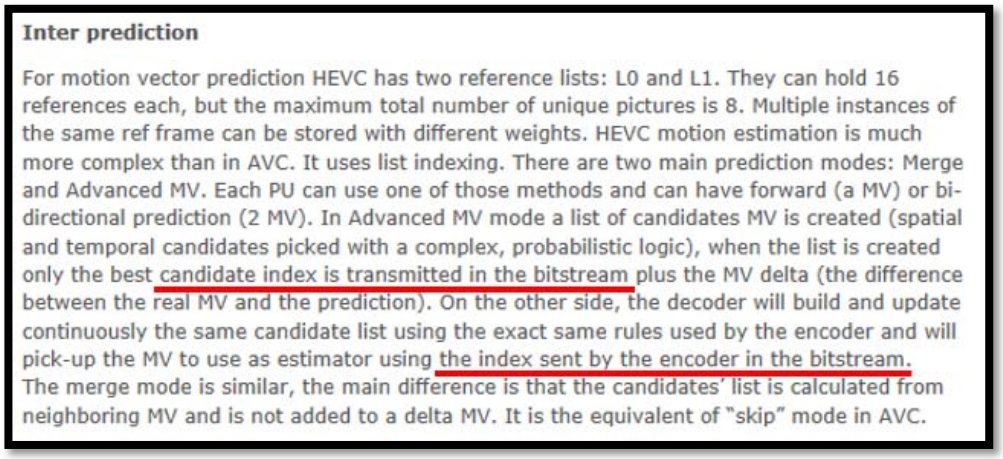
Sung-Fang Tsai, *et al., Encoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 347 (September 2014) (emphasis added).

390. The MediaTek '529 Products perform the step of assigning the modified motion vector as the motion vector to the first image block. Specifically, the MediaTek '529 Products, through the use of AMVP and Merge Mode, select the modified motion vector and assign it to a first block. The displacement between the current prediction unit and the matching prediction unit in the second image (reference image) is signaled using a motion vector. Further, the MediaTek '529 Products take the modified motion vector "computed from corresponding regions of previously decoded pictures" and transmit the residual.

> A block-wise prediction residual is computed from corresponding regions of previously decoded pictures (inter-picture motion compensated prediction) or neighboring previously decoded samples from the same picture (intra-picture spatial prediction). The residual is then processed by a block transform, and the transform coefficients are quantized and entropy coded. Side information data such as motion vectors and mode switching parameters are also encoded and transmitted.

Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, Vol. 7, No. 6 at 1002 (December 2013) (emphasis added).

391. The MediaTek '529 Products transmit into the bitstream the candidate index of motion vectors. HEVC documentation states that the coding process will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

392. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '529 Products in regular business operations.

393. MediaTek has directly infringed and continues to directly infringe the '529 Patent by, among other things, making, using, offering for sale, and/or selling technology for determining motion vectors that are each assigned to individual image regions, including but not limited to the MediaTek '529 Products.

394. One or more of the MediaTek '529 Products include technology for determining motion vectors that are each assigned to individual image regions.

395. One or more of the MediaTek ‘529 Products enable an increase in the resolution of video and image signals during the motion estimation process.

396. One or more of the MediaTek ‘529 Products perform a method for determining motion vectors which are assigned to individual image regions of an image.

397. One or more of the MediaTek ‘529 Products perform a method wherein an image is subdivided into a number of image blocks, and a motion estimation technique is implemented to assign at least one motion vector to each of the image blocks where a modified motion vector is generated for at least a first image block.

398. One or more of the MediaTek ‘529 Products perform a method that determines at least a second image block through which the motion vector assigned to the first image block at least partially passes.

399. One or more of the MediaTek ‘529 Products perform a method that generates the modified motion vector as a function of a motion vector assigned to at least the second image block.

400. One or more of the MediaTek ‘529 Products perform a method that assigns the modified motion vector as the motion vector to the first image block.

401. The MediaTek ‘529 Products are available to businesses and individuals throughout the United States.

402. The MediaTek ‘529 Products are provided to businesses and individuals located in the State of Delaware.

403. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the MediaTek ‘529 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for

directly infringing one or more claims of the '529 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

404. MediaTek also indirectly infringes the '529 patent by actively inducing infringement under 35 U.S.C. § 271(b).

405. MediaTek has had knowledge of the '529 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '529 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '529 Patent based on prior communications that identified the '529 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

406. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '529 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '529 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '529 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '529 Products that have the capability of operating in a manner that infringe one or more of the claims of the '529 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '529 Products to utilize the products in a manner that directly infringe one or more claims of the '529 patent.[37] By providing instruction and training to customers and end-

[37] *See, e.g.*, *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); MT6757

users on how to use the MediaTek '529 Products in a manner that directly infringes one or more claims of the '529 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '529 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '529 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '529 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '529 patent, knowing that such use constitutes infringement of the '529 patent.

407. The '529 patent is well-known within the industry as demonstrated by multiple citations to the '529 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '529 patent without paying a reasonable royalty. MediaTek is infringing the '529 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

408. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '529 patent.

409. As a result of MediaTek's infringement of the '529 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 (June 20, 2016); MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (November 27, 2014); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (June 10, 2014); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 (2018); *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); and MSD6180 SOC DATASHEET (2016).

COUNT VIII
INFRINGEMENT OF U.S. PATENT NO. 7,929,609

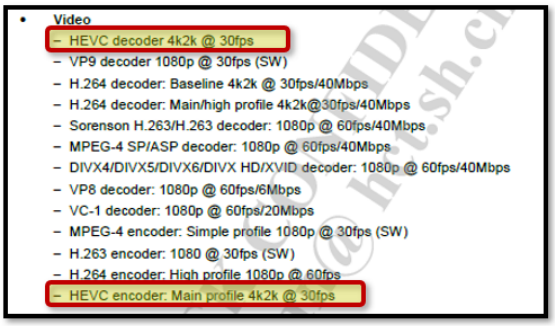
410. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

411. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for compensation and estimation of motion in video images.

412. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek devices that contain H.265 video compression functionality,

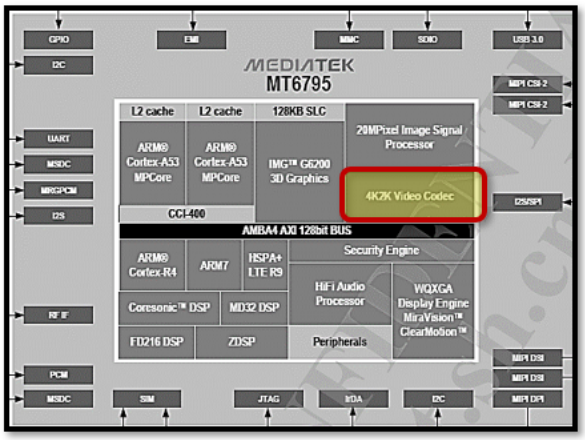
413. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '609 Product(s)").

414. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.



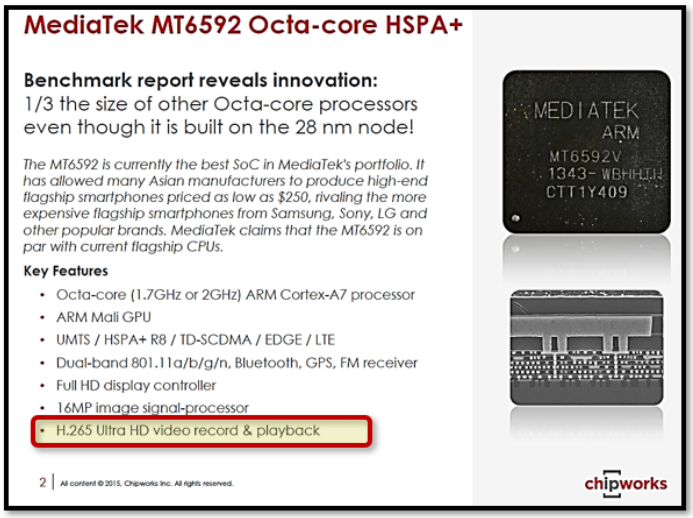
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 (August 27, 2014) (annotations added).

415. The following documentation from MediaTek shows an exemplar of the accused devices (e.g., MT6795) and in a functional diagram of the chip identifies the location of the HEVC "Video Codecs."



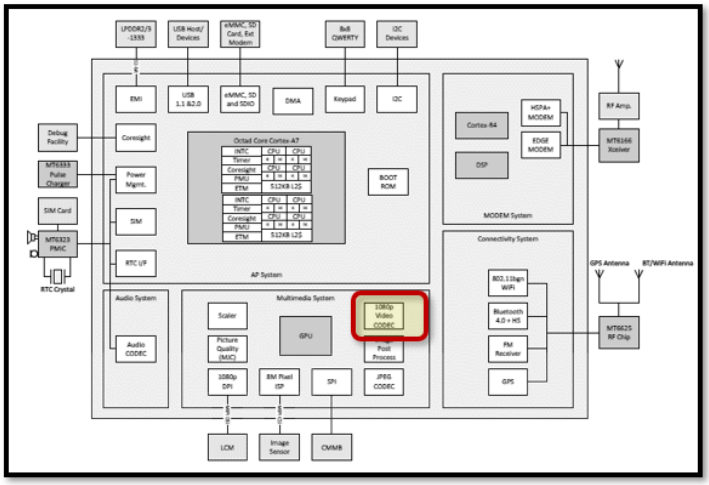
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 12 (August 27, 2014) (annotation added).

416. Analysis of the accused MediaTek '609 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

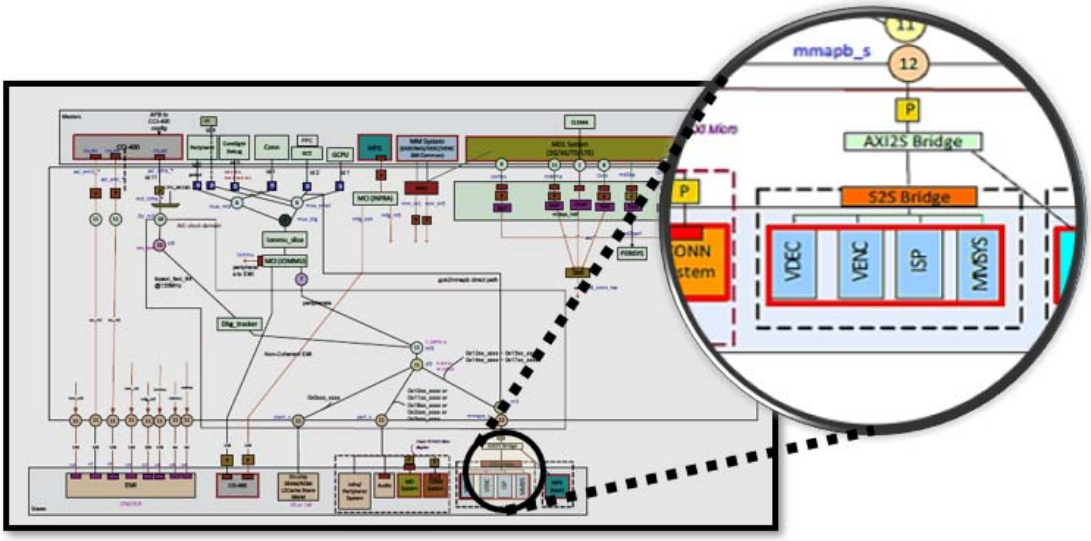
417. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (annotation added) (block diagram of the MT6592 Product showing the Video Codec for HEVC decoding that is part of the chip's multimedia system).

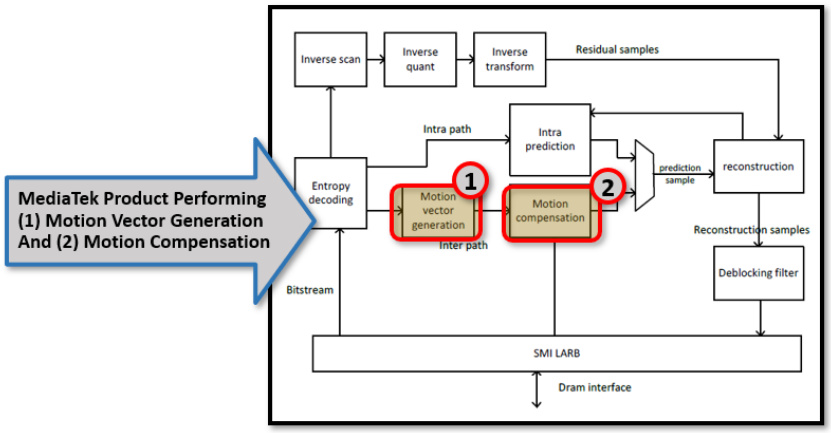
418. MediaTek documentation also establishes the accused MediaTek '609 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019).

419. MediaTek documentation also establishes that the accused MediaTek '609 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



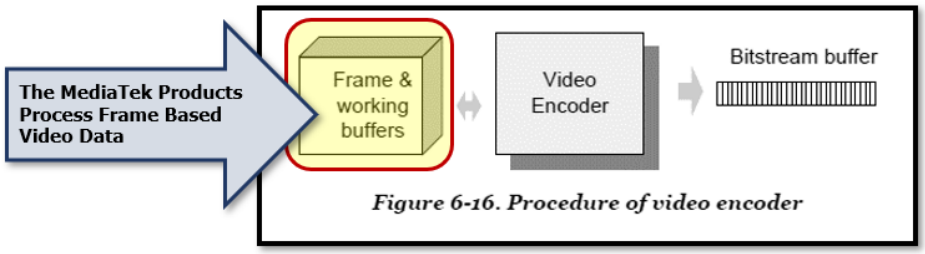
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

420. MediaTek documentation describes the encoding process used by the accused MediaTek '609 Products. For example, the below process diagram from MediaTek shows the MediaTek '609 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



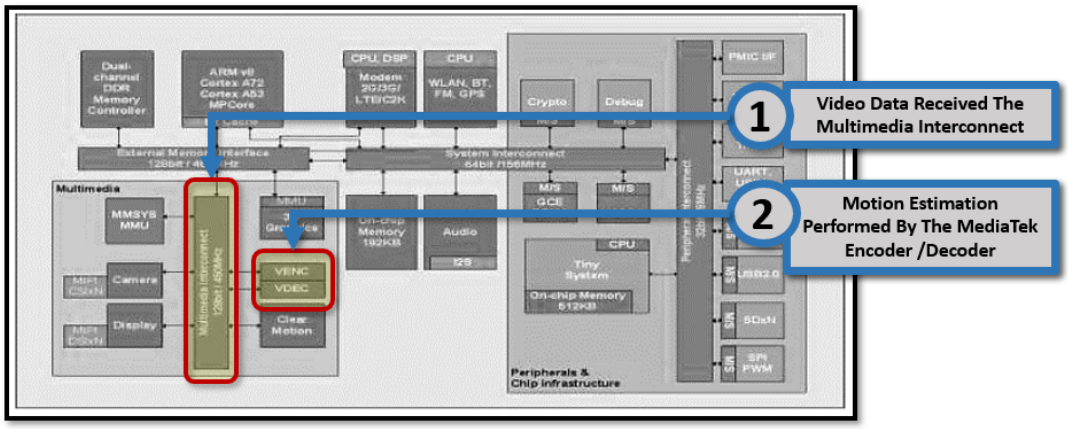
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

421. The video encoder in the accused MediaTek '609 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

422. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

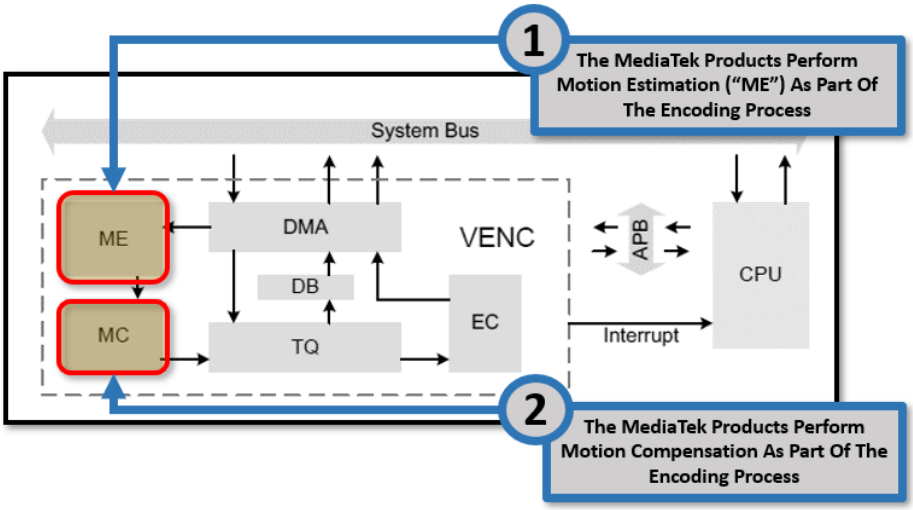
423. The MediaTek '609 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '609 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

424. The accused MediaTek '609 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC. This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

425. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



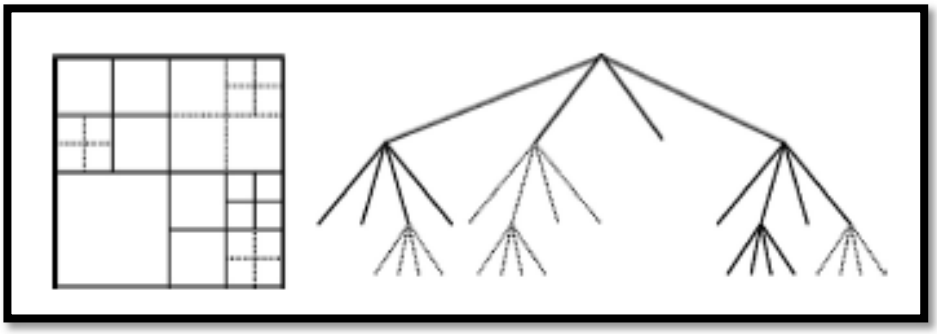
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

426. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '609 Products in regular business operations.

427. The functionality of the encoding process used by the MediaTek '609 Products use "motion vector[s]: A two-dimensional vector used for *inter prediction* that provides an offset from the coordinates in the decoded picture to the coordinates in a reference picture," as defined in definition 3.83 of the *ITU-T H.265 Series H: Audiovisual and Multimedia Systems* (2018) (emphasis added); *see also, e.g.,* Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1650 (December 2012) ("The encoding process for inter picture prediction consists of choosing motion data comprising the selected reference picture and motion vector (MV) to be applied for predicting the samples of each block. The encoder and decoder generate identical inter picture prediction signals by applying motion compensation (MC) using the MV and mode decision data.").

428. The MediaTek '609 Products further select the selected image selection area based on a range of possible motion vectors in the selected image search area. Further, the search area

of the selected image segment has a center. Specifically, the MediaTek '609 Products contain functionality for selecting a coding unit. The coding unit comprises a selected image segment. The below diagram shows that the MediaTek '609 Products select a content unit (e.g., selected image segment).



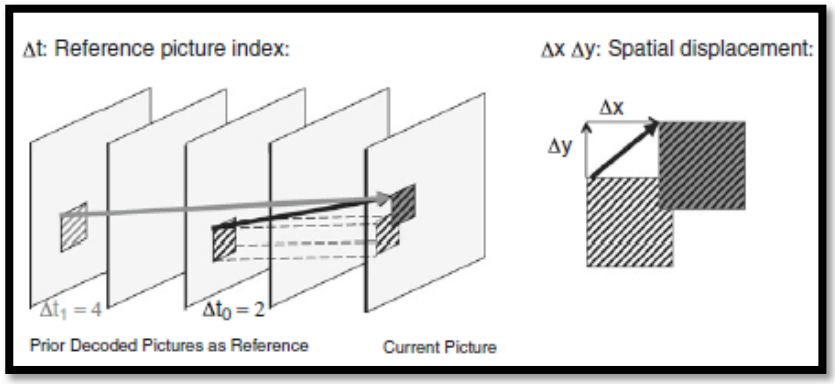
Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1656 (December 2012).

429. The MediaTek '609 Products enable the selection of a selected image segment of a given image corresponding to an image segment of a first video image. The selected image segment has a center and a search area is defined around the image segment. Specifically, the MediaTek '609 Products encode video data using inter-frame coding. Specifically, video data is encoded using a predecessor frame. Inter-prediction used in the encoding of video data allows a transform block to span across multiple prediction blocks for inter picture-predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences**,** intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1652 (December 2012) (emphasis added).

430. The video data processed by the MediaTek '609 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

431. The following excerpt from an article describing the architecture of the video stream encoded by the MediaTek '609 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

432. The MediaTek '609 Products comprise a system for retrieving image motion data related to the search area. Specifically, the MediaTek '609 Products retrieve data relating to the motion search area. The data, which includes the motion vector index, is sent from the encoder and retrieved by the decoder.

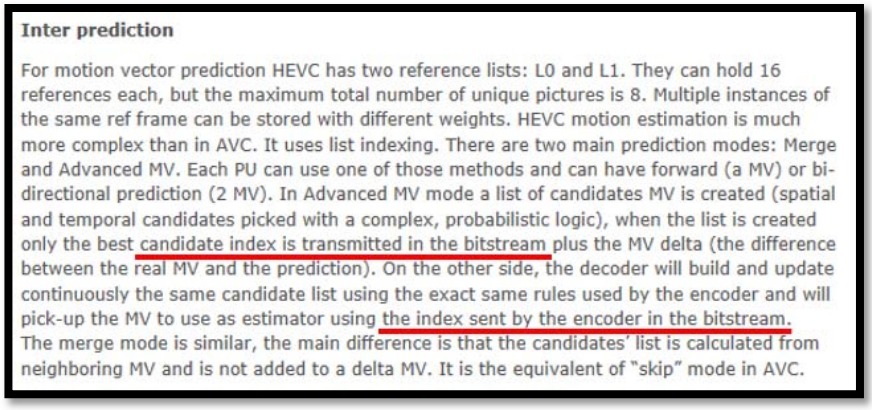
> Since inter-picture prediction typically compensates for the motion of real-world objects between pictures of a video sequence, it is also referred to as motion-compensated prediction. While intra-picture prediction exploits the spatial redundancy between neighboring blocks inside a picture, motion-compensated prediction utilizes the large amount of temporal redundancy between pictures. In either case, the resulting prediction error, which is formed by taking the difference between the original block and its prediction, is transmitted using transform coding, which exploits the spatial redundancy inside a block and consists of a decorrelating linear transform, scalar quantization of the transform coefficients and entropy coding of the resulting transform coefficient levels.

Heiko Schwarz, Thomas Schierl, Detlev Marpe, *Block Structures and Parallelism Features in HEVC*, in HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 49 (September 2014) (emphasis added).

> For each CU, a prediction mode is signaled inside the bitstream. The prediction mode indicates whether the CU is coded using intra-picture prediction or motion-compensated prediction. If intra-picture prediction is chosen, one of the 35 supported spatial intra prediction modes has to be selected for the luma CB and signaled inside the bitstream. If the CU has the minimum CU size specified in the sequence parameter set, the luma CB can also be decomposed into four equallysized square subblocks, in which case a separate intra prediction mode is transmitted for each of these subblocks.

Id. at 59 (emphasis added).

433. Further, the MediaTek '609 Products contain functionality wherein the motion vector prediction performed includes the ability to transmit in the bitstream the candidate index of motion vectors. Documentation of the encoding process states that the encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

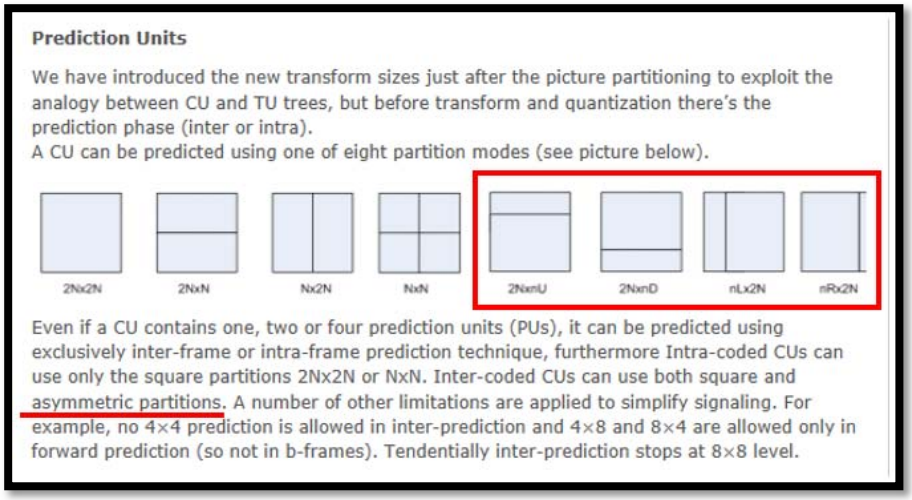
434. The MediaTek '609 Products comprise a system for specifying that the center of the search area is offset from the center of the image section. Specifically, the MediaTek '609 Products, when selecting a temporal candidate for HEVC encoding, default to the right bottom position just outside of the collocated prediction unit.

> It can be seen from Fig. 5.4b that only motion vectors from spatial neighboring blocks to the left and above the current block are considered as spatial MVP candidates. This can be explained by the fact that the blocks to the right and below the current block are not yet decoded and hence, their motion data is not available. Since the co-located picture is a reference picture which is already decoded, it is possible to also consider motion data from the block at the same position, from blocks to the right of the co-located block or from the blocks below**.** In HEVC, the block to the bottom right and at the center of the current block have been determined to be the most suitable to provide a good temporal motion vector predictor (TMVP).

Benjamin Bross, *et al., Inter-picture prediction in HEVC,* in HIGH EFFICIENCY VIDEO CODING (HEVC) at 119 (2014) (emphasis added).

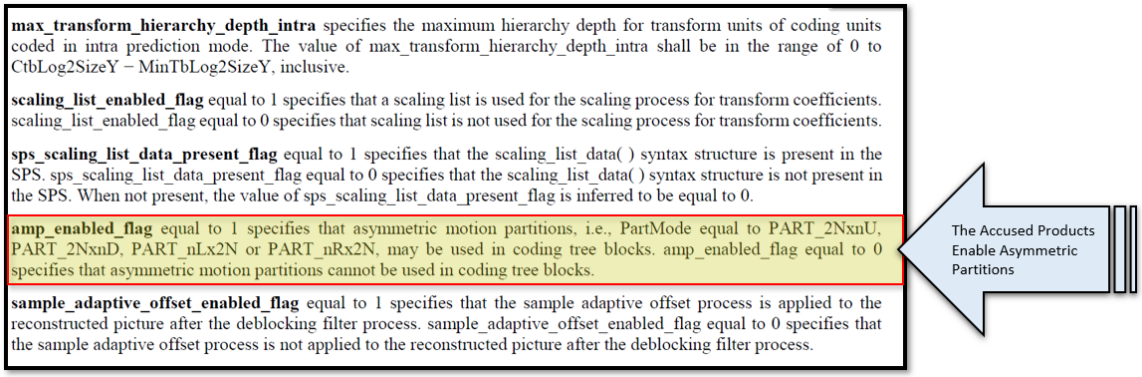
435. Descriptions of the HEVC encoding process, which are implemented by the MediaTek '609 Products state "for the temporal candidate, the right bottom position just outside of the collocated PU of the reference picture is used if it is available. Otherwise, the center position is used instead." Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1660 (December 2012) (emphasis added).

436. The MediaTek '609 Products encode video data such that a predetermined search area (S) center is offset from the center of the image segment. The predetermined search area is called a partition and there are eight different partition modes in the H.265 standard, these partition modes are shown in the figure below. The last four partition modes are asymmetric, meaning their center is offset from the overall CU center.



Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

437. The figure below shows the syntax as well as the instructions for enabling the asymmetric partitions within the H.265 standard as implemented by the MediaTek '609 Products.



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at 76 (February 2018) (annotation added).

438. One or more of the MediaTek '609 Products include technology for compensation and estimation of motion in video images.

439. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '609 Products – necessarily infringe the '609 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '609 patent, including but not limited to claim 1 of the '609 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '609 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

440. The MediaTek '609 Products comply with the HEVC standard, which requires estimating and/or compensating motion in video images.

441. MediaTek has directly infringed and continues to directly infringe the '609 patent by, among other things, making, using, offering for sale, and/or selling technology for compensation and estimation of motion in video images, including but not limited to the MediaTek '609 Products.

442. The MediaTek '609 Products improve video signal processing functionality used in motion compensated prediction in encoding and compressing of digital video signals, motion compensated filtering in noise reduction, motion compensated interpolation in video format

conversion, and motion compensated de-interlacing of interlaced video signals, among other video processing functionalities.

443. The MediaTek ‘609 Products enable a method of estimating or compensating motion in video images that includes using a video processor to select an image segment of a given video image.

444. The MediaTek ‘609 Products enable a method of estimating or compensating motion in video images that includes using the video processor to define an asymmetric search area surrounding the image segment based on ranges of possible motion vectors for the image segment.

445. The MediaTek ‘609 Products enable a method of estimating or compensating motion in video images that includes using the video processor to retrieve image data related to the asymmetric search area.

446. The MediaTek ‘609 Products enable a method of estimating or compensating motion in video images that includes a video processor that defines the asymmetric search area to have a center offset from a center of the image segment, the offset thereby defining asymmetry of the asymmetric search area, and statistically determines from an average vector of motion vectors established for one or more previous images.

447. The MediaTek ‘609 Products are available to businesses and individuals throughout the United States.

448. The MediaTek ‘609 Products are provided to businesses and individuals located in the State of Delaware.

449. By making, using, testing, offering for sale, and/or selling products and services for compensation and estimation of motion in video images, including but not limited to the MediaTek

‘609 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘609 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

450. MediaTek also indirectly infringes the ‘609 patent by actively inducing infringement under 35 U.S.C. § 271(b).

451. MediaTek has had knowledge of the ‘609 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the ‘609 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the ‘609 Patent based on prior communications that identified the ‘609 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

452. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek ‘609 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the ‘609 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the ‘609 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek ‘609 Products that have the capability of operating in a manner that infringe one or more of the claims of the ‘609 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek ‘609 Products to utilize the products in a manner that directly infringe one

or more claims of the '609 patent.[38] By providing instruction and training to customers and end-users on how to use the MediaTek '609 Products in a manner that directly infringes one or more claims of the '609 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '609 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '609 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '609 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '609 patent, knowing that such use constitutes infringement of the '609 patent.

453. The '609 patent is well-known within the industry as demonstrated by multiple citations to the '609 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '609 patent without paying a reasonable royalty. MediaTek is infringing the '609 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

454. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '609 patent.

455. As a result of MediaTek's infringement of the '609 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for

[38] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

COUNT IX
INFRINGEMENT OF U.S. PATENT NO. 7,982,799

456. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

457. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for interpolating an image information value for a pixel of an interline situated between two original image lines in an image.

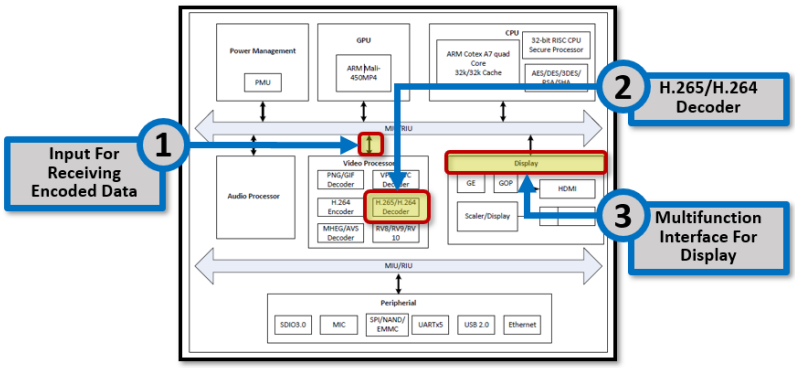
458. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that contain functionality for interpolating image information capable of decoding video data in compliance with the H.265 standard, including but not limited to the infringing MediaTek products include: MediaTek Automotive Products (MediaTek Autus I20 (MT2712)); MediaTek Mobile Products (MediaTek Helio A11, MediaTek Helio P10, MediaTek Helio P18, MediaTek Helio P20, MediaTek Helio P22, MediaTek Helio P23, MediaTek Helio P25, MediaTek Helio P30, MediaTek Helio P60, MediaTek Helio P70, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, MediaTek MT6732, MediaTek MT6735, MediaTek MT6738, MediaTek MT6739, MediaTek MT6750, MediaTek MT6752, and MediaTek MT6753); MediaTek Digital TV Products (MediaTek MT5582, MediaTek MT5596, and MediaTek MT5597); MediaTek Home Products (MediaTek MT8581, MediaTek MT8685, and MediaTek MT8693); and MediaTek Tablet Products (MediaTek MT8163V/A, MediaTek MT8163V/B, MediaTek MT8167A, MediaTek MT8167B, MediaTek MT8173, MediaTek MT8176, MediaTek

MT8735B, MediaTek MT8735D, MediaTek MT8735M, MediaTek MT8735P, MediaTek MT8783, and MediaTek MT8785) (collectively, the "MediaTek Products").

459. MediaTek designs, makes, sells, offers to sell, imports, and/or uses products that contain HEVC decoding technology, including but not limited to the MStar System on Chip ("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MStar Product(s)").

460. The MediaTek Products and MStar Products (collectively, the "MediaTek '799 Product(s)") directly infringe the '799 patent.

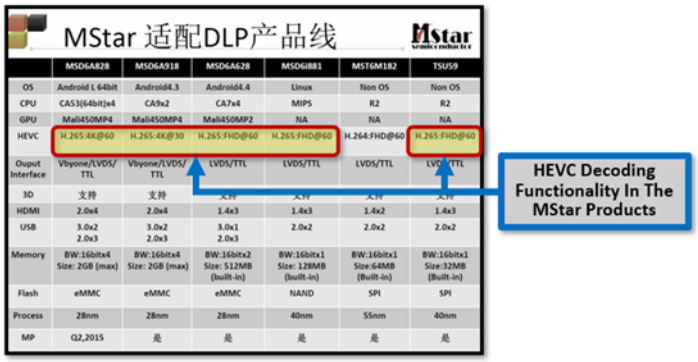
461. The MStar Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

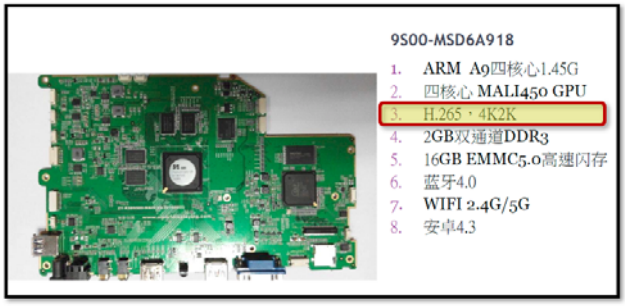
462. Documentation regarding the MStar Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows

that the accused MStar Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

463. The MStar Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MStar Products that contain a decoder that conforms to the H.265 standard.



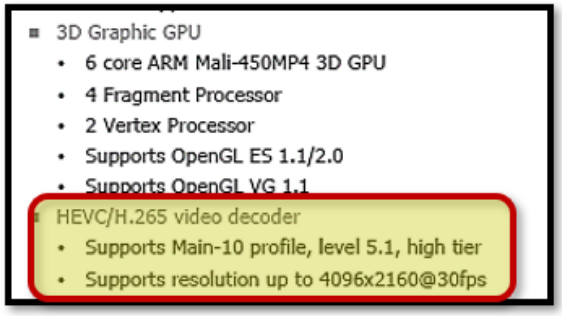
Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product contains a decoder compliant with the H.265 standard).

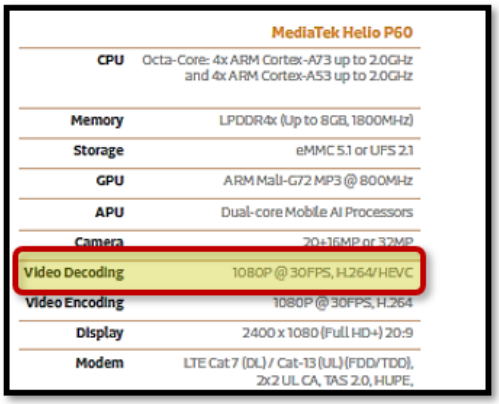
464. Datasheets from MediaTek also establish that the accused MStar Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states:

"all in one 的SOC 芯片, 芯片主要功能规格参数如下: 支持AVS+/ H264/ RMVB/ MPEG l/ MPEG2/ MPEG4NC l/ DIVX/ H265 等主流格式解码，分辨率最大支持到1 080P@60"[39]

MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

465. Similarly, the MediaTek datasheets for the MSO9280MC and MediaTek Helio P60 Products identifies that they contain HEVC H.265 decoders.

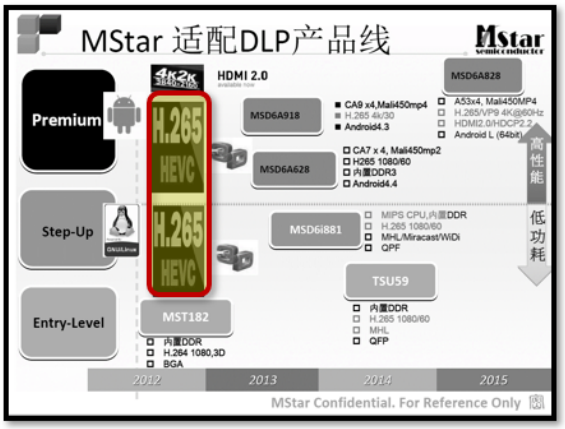




MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 at 2 (2018) (annotation added).

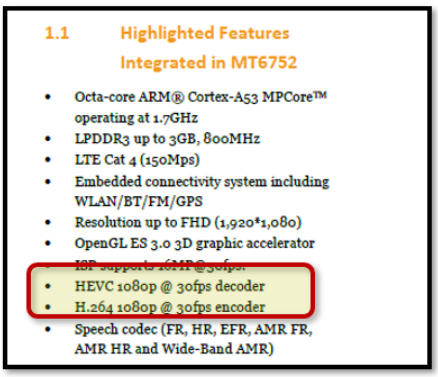
466. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MStar Products.

[39] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."



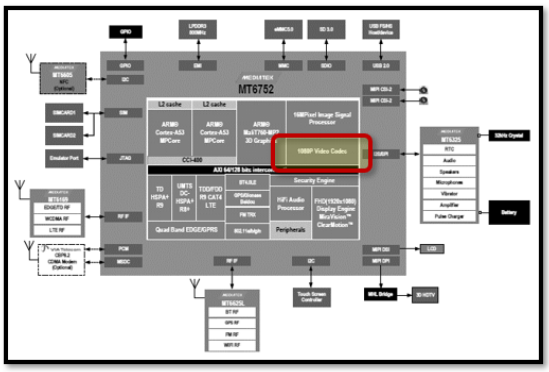
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

467. Technical briefs from MediaTek similarly identify the accused MediaTek products as containing a decoder that complies with the HEVC standard.



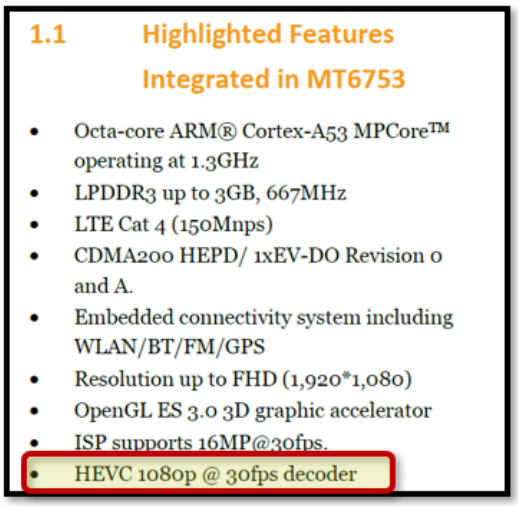
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (June 10, 2014) (annotation added) ("The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.").

468. MediaTek documentation relating to the accused MediaTek Products (*e.g.*, MT6752) describe the chips as a "brand-new generation smart phone SoC integrating MediaTek LTE modem, Octa-core ARM® Cortex-A53 MPCoreTM, 3D graphics and high-definition 1080p video decoder."



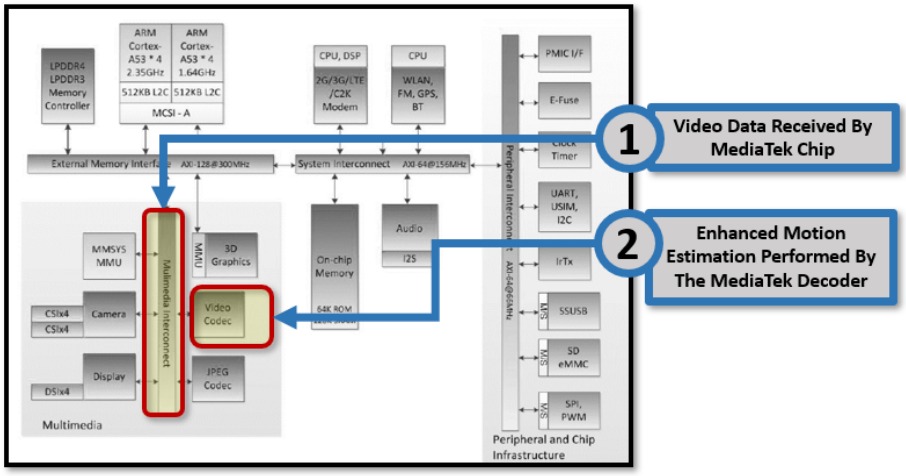
MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 15 (June 10, 2014) (annotation showing the HEVC video decoder).

469. MediaTek documentation for the accused products identifies products such as the MT6753 Application Processor contains a video decoder that complies with the HEVC standard.



MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (November 27, 2014) ("The chip integrates Octa-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.").

470. MediaTek documentation shows the interconnects that connect the video decoding engine to the rest of the application processor. For example, MediaTek documentation for the MT6757 chip (i.e., the Helio P20 chip) shows connections to the video codec engine.



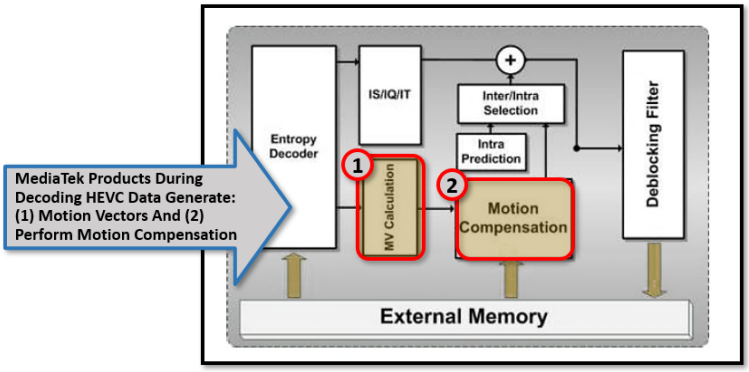
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 18 (June 20, 2016) (annotations added).

471. MediaTek technical documentation establishes the accused products (e.g., the MT6757 application processor) include an HEVC compliant decoder.

> The application processor, an Octa-core ARM® Cortex-A53 MPCoreTM equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

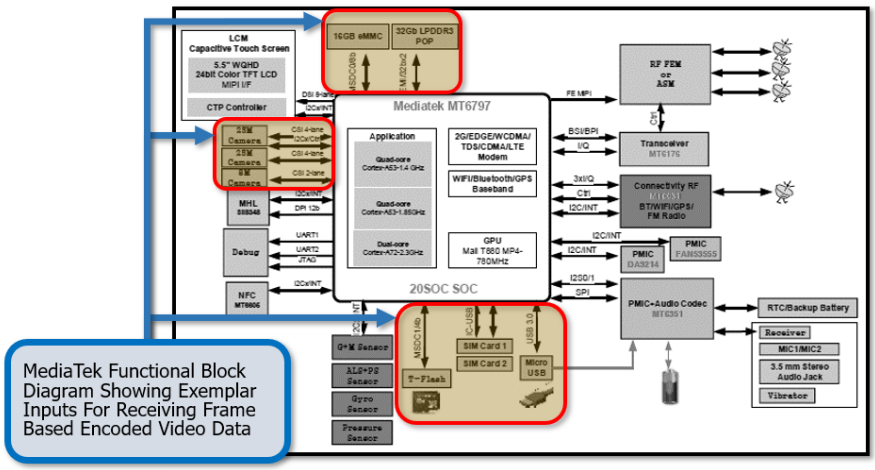
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 7 (June 20, 2016) (emphasis added) (describing that the MediaTek product includes a decoder for "HEVC 4K @ 30fps").

472. The architecture and core blocks of HEVC decoder ("VDEC") are shown in the below diagram including the following functional components: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra prediction, Motion Compensation, and De-Blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is sent to the display stage.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 276 (July 19, 2016) (annotations added)

473. The accused MediaTek '799 Products receive HEVC encoded data through a variety of inputs. The below excerpt from MediaTek's technical documentation identifies the inputs for receiving HEVC encoded video data as part of the decoding process.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 12 (July 19, 2016) (annotations added) (showing a high-level functional block diagram of the MT6797 product).

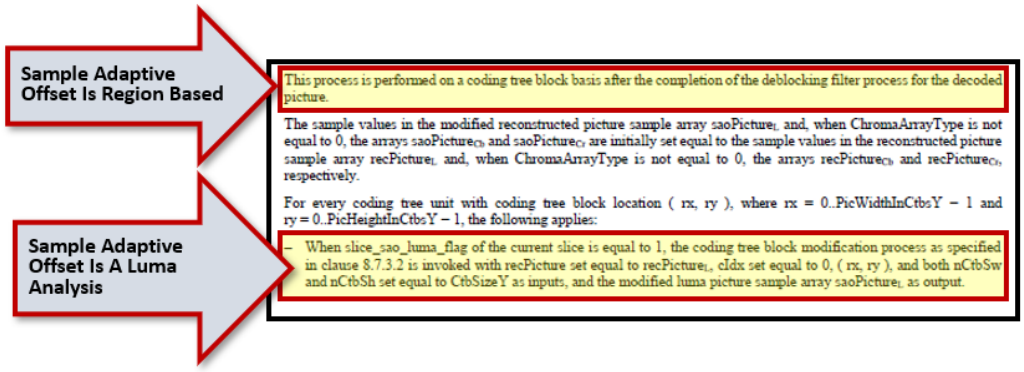
474. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '799 Products – necessarily infringe the '799 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '799 patent, including but not limited to claim 1 of the '799 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING

VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '799 patent: "8.6.7 Picture construction process prior to in-loop filter process;" "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process;" "F.8.7 In-loop filter process;" "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" and "8.5.3 Decoding process for prediction units in inter prediction mode.").

475. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '799 Products in regular business operations.

476. One or more of the MediaTek '799 Products contain functionality for a direction quality value for an image direction.

477. One or more of the MediaTek '799 Products include technology selecting from a number of image directions, to each of which a direction quality value is assigned, a direction of interpolation by comparing these direction quality values.



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 AT § 8.7.3.1 (April 2015) (annotations added).

478. MediaTek has directly infringed and continues to directly infringe the '799 patent by, among other things, making, using, offering for sale, and/or selling technology for interpolating an image information value for a pixel of an interline situated between two original image lines in an image, including but not limited to the MediaTek '799 Products.

> Using a translational motion model, the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx; Δy could be of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, i.e. motion vectors and reference indices, are further referred to as motion data.

Benjamin Bross, *Inter-Picture Prediction In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 114 (September 2014) (emphasis added).

479. One or more of the MediaTek '799 Products reduce or prevent ambiguities in the determination of an optimal image direction by adding a single direction values of several adjacent pixels.

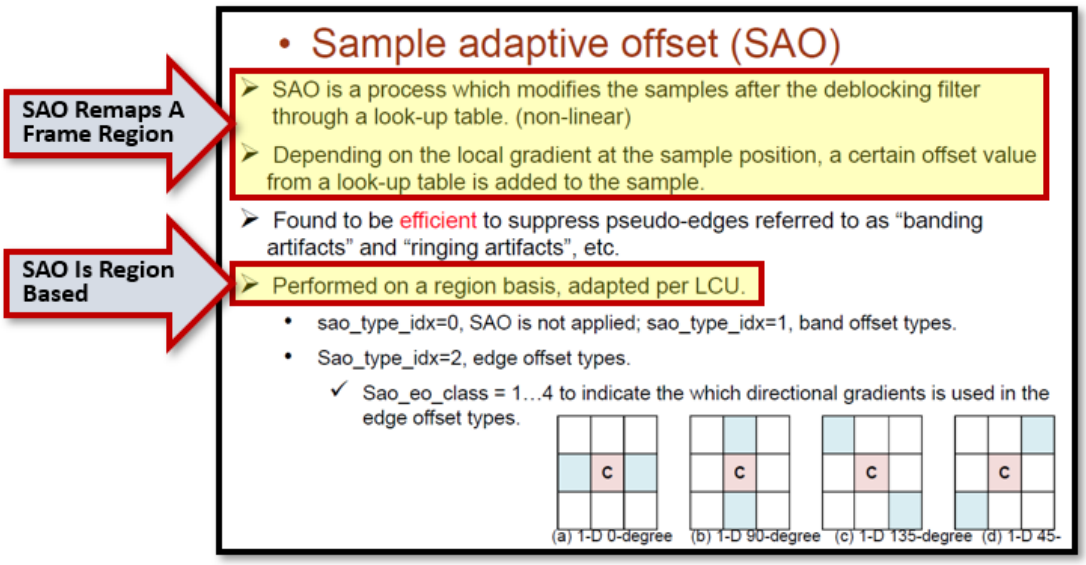
480. The MediaTek '799 Products contain functionality for determining the image information value being interposed in dependence on image information values assigned to pixels lying adjacent to the pixel being interpolated (in the direction of interpolation).

481. One or more of the MediaTek '799 Products contain functionality for selecting a pixel group with two or more pixels as part of ascertaining a directional quality value.

> SAO classifies each pixel into one of four bands or one of four edge types and adds an offset to it. For band offsets, the band of each pixel depends on its value and the position of the four bands. For edge offsets, the edge of each pixel depends on the whether its value is larger or smaller than two of its neighbors. The selection between band offsets and edge offsets, position of bands, choice of neighbors for edge offsets, and values of the offsets are signaled at the CTU level for luma and chroma separately.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 335 (September 2014) (emphasis added).

482. One or more of the MediaTek '799 Products enable a method for interpolation of an image information value for a pixel of an interline that includes selecting from a number of image directions, to each of which a direction quality value is assigned, a direction of interpolation by comparing the direction quality values. "[A]fter the deblocking filter through a look-up table . . . [and applying] a certain offset value from a look-up-table is added to the sample."[40]



Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013) (annotations added).

483. One or more of the MediaTek '799 Products enable a method for interpolation of an image information value for a pixel of an interline that includes determining the image information value being interpolated in dependence on image information values assigned to pixels lying adjacent to the pixel being interpolated in the direction of interpolation.

484. One or more of the MediaTek '799 Products enable a method for interpolation of an image information value for a pixel of an interline that includes ascertaining a direction quality

[40] Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013).

value for an image direction by determining a single direction quality value for each pixel of the pixel group, the single direction quality value being dependent on image information values assigned to image regions lying adjacent to the particular pixel of the group in the image direction.

> The second in-loop filter, SAO, is applied to the output of the deblocking filter and further improves the quality of the decoded picture by attenuating ringing artifacts and changes in sample intensity of some areas of a picture. The most important advantage of the in-loop filters is improved subjective quality of reconstructed pictures. In addition, using the filters in the decoding loop also increases the quality of the reference pictures and hence also the compression efficiency.

Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 171 (September 2014) (annotations added).

485. The MediaTek '799 Products are available to businesses and individuals throughout the United States.

486. The MediaTek '799 Products are provided to businesses and individuals located in the State of Delaware.

487. By making, using, testing, offering for sale, and/or selling products and services for interpolating an image information value for a pixel of an interline situated between two original image lines in an image, including but not limited to the MediaTek '799 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '799 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

488. MediaTek also indirectly infringes the '799 patent by actively inducing infringement under 35 USC § 271(b).

489. MediaTek has had knowledge of the '799 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '799 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of

the '799 Patent based on prior communications that identified the '799 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

490. MediaTek had knowledge of the '799 patent from at least September 17, 2009 onward based on MediaTek's U.S. Patent App. No. 2009/0231486A1 (the "'486 Application"). The '486 Application was assigned to MediaTek, Inc. and during the prosecution of the '486 Application the United States Patent and Trademark Office identified U.S. Patent App. No. 2007/0153124 A1 as relevant prior art to the '486 Application. The patent application identified by the United States Patent Office to MediaTek would later issue as the '799 patent.

491. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '799 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '799 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '799 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '799 Products that have the capability of operating in a manner that infringe one or more of the claims of the '799 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '799 Products to utilize the products in a manner that directly infringe one or more claims of the '799 patent.[41] By providing instruction and training to customers and end-

[41] *See, e.g.*, *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 (June 20, 2016); MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (November 27, 2014); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF

users on how to use the MediaTek '799 Products in a manner that directly infringes one or more claims of the '799 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '799 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '799 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '799 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '799 patent, knowing that such use constitutes infringement of the '799 patent.

492. The '799 patent is well-known within the industry as demonstrated by multiple citations to the '799 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '799 patent without paying a reasonable royalty. MediaTek is infringing the '799 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

493. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '799 patent.

494. As a result of MediaTek's infringement of the '799 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

(June 10, 2014); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 (2018); *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); and MSD6180 SOC DATASHEET (2016).

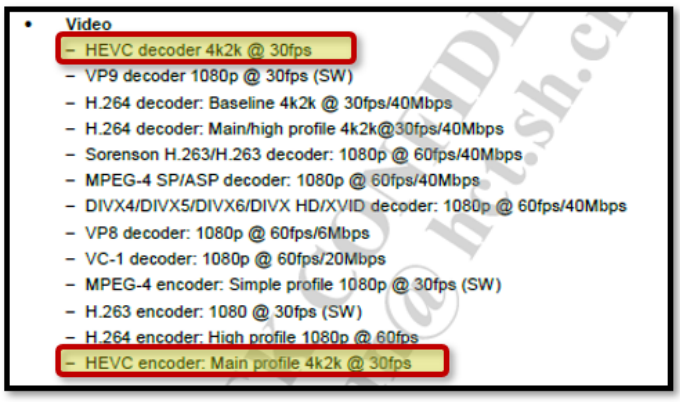
COUNT X
INFRINGEMENT OF U.S. PATENT NO. 8,073,054

495. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

496. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for estimating a current motion vector for a group of pixels of an image.

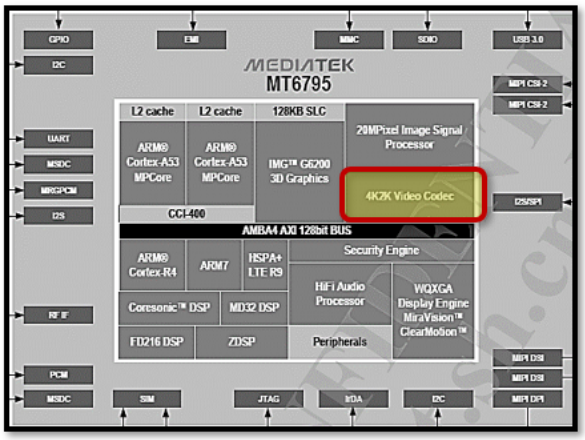
497. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '054 Product(s)").

498. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.



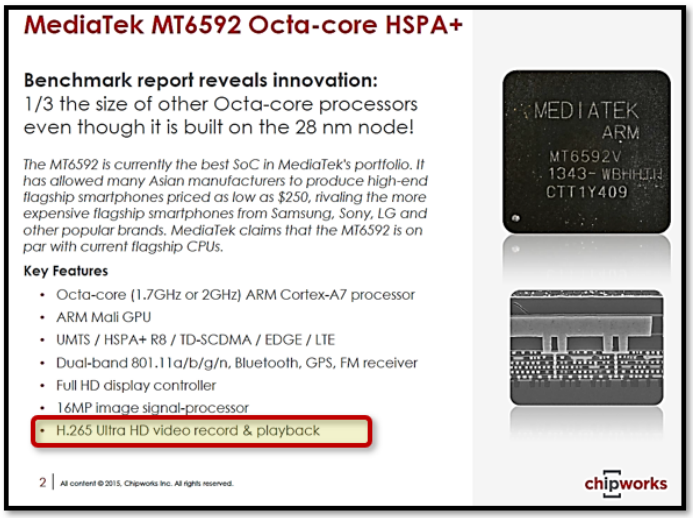
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 (August 27, 2014) (annotations added).

499. The following documentation from MediaTek shows an exemplar of the accused devices (e.g., MT6795) and in a functional diagram of the chip identifies the location of the HEVC "Video Codecs."



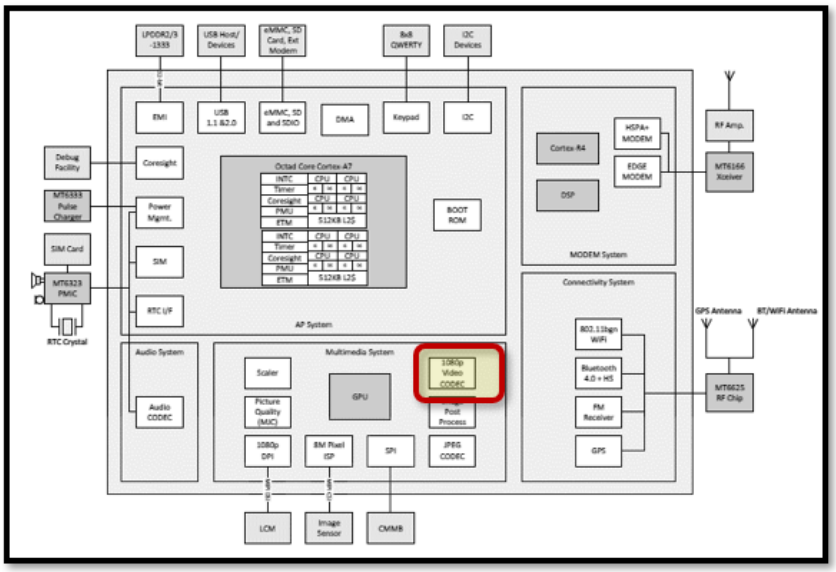
MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 12 (August 27, 2014) (annotation added).

500. Analysis of the accused MediaTek '054 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

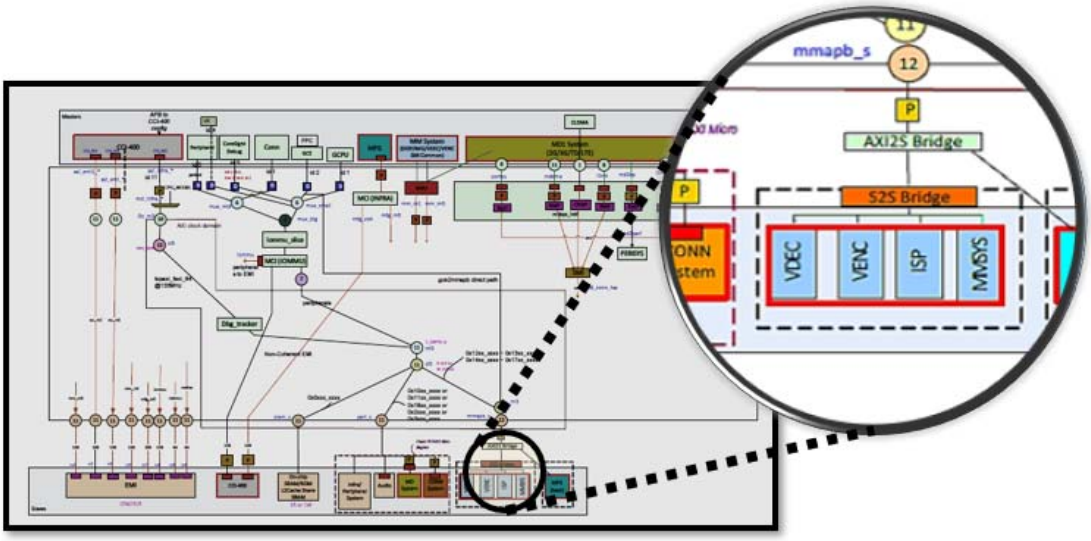
501. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (annotation added) (block diagram of the MT6592 Product showing the Video Codec for HEVC decoding that is part of the chip's multimedia system).

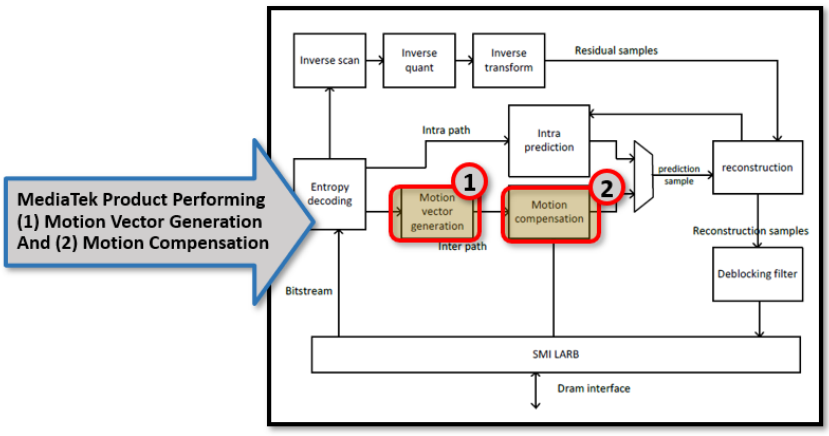
502. MediaTek documentation also establishes the accused MediaTek '054 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019).

503. MediaTek documentation also establishes that the accused MediaTek '054 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



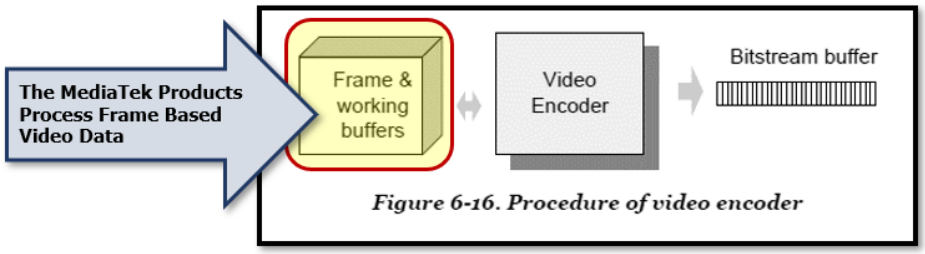
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

504. MediaTek documentation describes the encoding process used by the accused MediaTek '054 Products. For example, the below process diagram from MediaTek shows the MediaTek '054 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



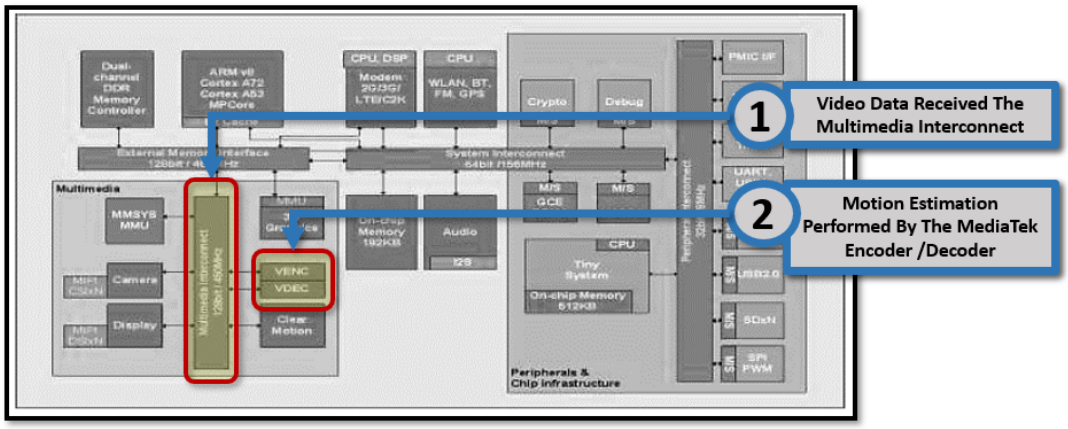
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

505. The video encoder in the accused MediaTek '054 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

506. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

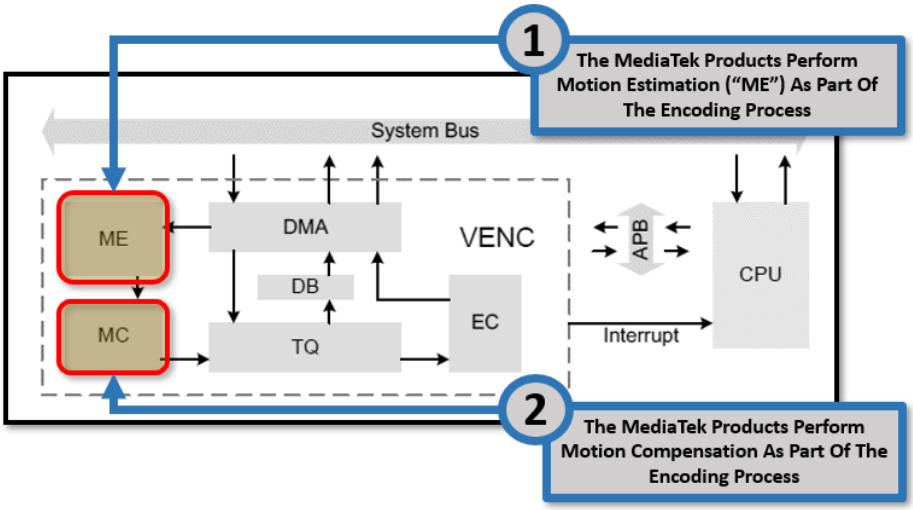
507. The MediaTek '054 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '054 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

508. The accused MediaTek '054 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC. This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

509. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

510. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '054 Products in regular business operations.

511. MediaTek documentation cited in the proceeding paragraphs shows that the MediaTek '054 Products perform a motion vector estimation method. Specifically, the MediaTek '054 Products perform the method of encoding video content using High Efficiency Video Coding ("HEVC").

512. The MediaTek '054 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the MediaTek Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by MediaTek Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

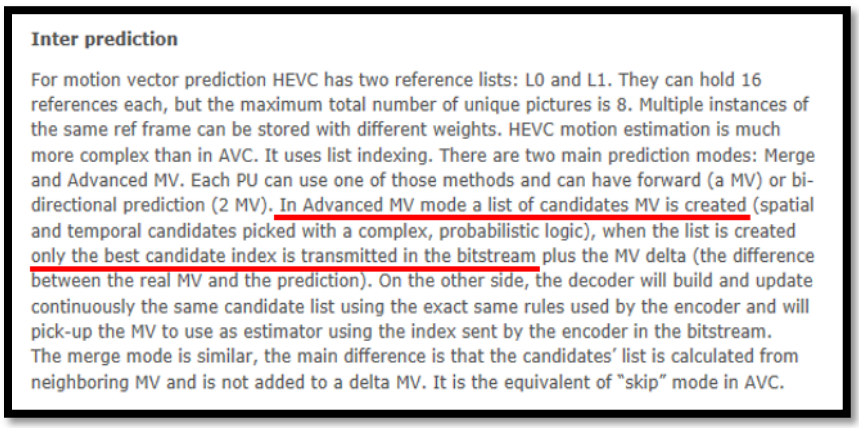
513. The MediaTek '054 Products contain a video encoder that selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment has an image segment center.

514. One or more of the MediaTek ‘054 Products include technology for estimating a current motion vector for a group of pixels of an image

515. MediaTek has directly infringed and continues to directly infringe the ‘054 patent by, among other things, making, using, offering for sale, and/or selling technology for estimating a current motion vector for a group of pixels of an image, including but not limited to the MediaTek ‘054 Products.

516. By complying with the HEVC standard, MediaTek’s devices – such as the MediaTek ‘054 Products – necessarily infringe the ‘054 patent. Mandatory sections of the HEVC standard require the elements required by certain claims of the ‘054 patent, including but not limited to claim 1. High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek’s infringement of the ‘054 patent: “7.3.4 Scaling list data syntax;” 7.3.6.1 General slice segment header syntax;” “7.3.6.3 Weighted prediction parameters syntax;” “7.3.8.14 Delta QP syntax;” “7.4.4 Profile, tier and level semantics;” and “7.4.7.3 Weighted prediction parameters semantics.”

517. The MediaTek ‘054 Products comprise functionality for generating a set of candidate motion vectors for a grouping of pixels (prediction unit). The HEVC standard generates a set of candidate motion vectors for the group of pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors. After the candidate motion vectors are generated, only the best candidate index is transmitted.



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

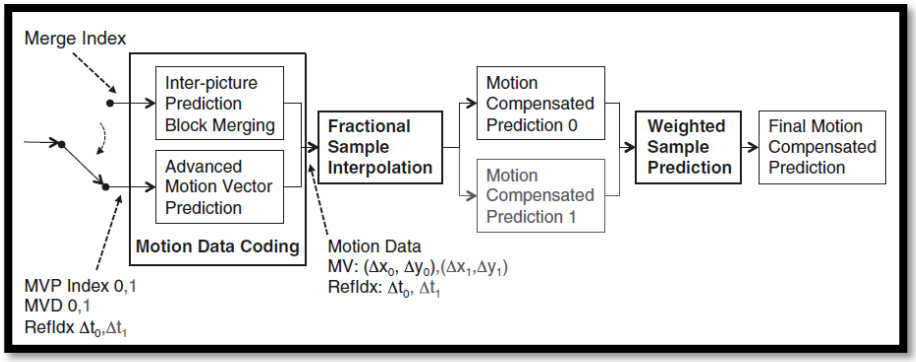
Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

518. One or more of the MediaTek '054 Products enable motion estimation with a relatively fast convergence in finding the appropriate motion vectors of the motion vector fields by adding a further candidate motion vector to the set of candidate motion vectors.

> HEVC introduces a so-called merge mode, which sets all motion parameters of an inter picture predicted block equal to the parameters of a merge candidate [6]. The merge mode and the motion vector prediction process optionally allow a picture to reuse motion vectors of prior pictures for motion vector coding,

Frank Bossen, *et al*., *HEVC Complexity and Implementation Analysis,* IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY VOL. 22 NO. 12 at 1686 (December (2012).

519. The following block diagram illustrates the form of encoded video data received by the MediaTek '054 Products. Specifically, the encoded video data received by the MediaTek '054 Products is encoded using inter-picture prediction where the motion data of a block is correlated with neighboring blocks. To exploit this correlation, motion data is not directly coded in the bitstream, but predictively coded based on neighboring motion data. Further, the MediaTek '054 Products receive data that is encoded using advanced motion vector prediction where the best predictor for each motion block is signaled to the decoder. In addition, inter-prediction block merging derives all motion data of a block from the neighboring blocks.



Benjamin Bross, *et al*., *Inter-Picture Prediction in HEVC,* In HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (2014).

520. The MediaTek '054 Products carry out a block-based motion vector estimation process that involves comparing a plurality of candidate vectors to determine block-based motion vectors. The MediaTek '054 Products generate two predictor candidate motion vectors (a spatial motion vector and temporal motion vector). The first predictor candidate motion vector is drawn from a list of spatial motion vector candidates.

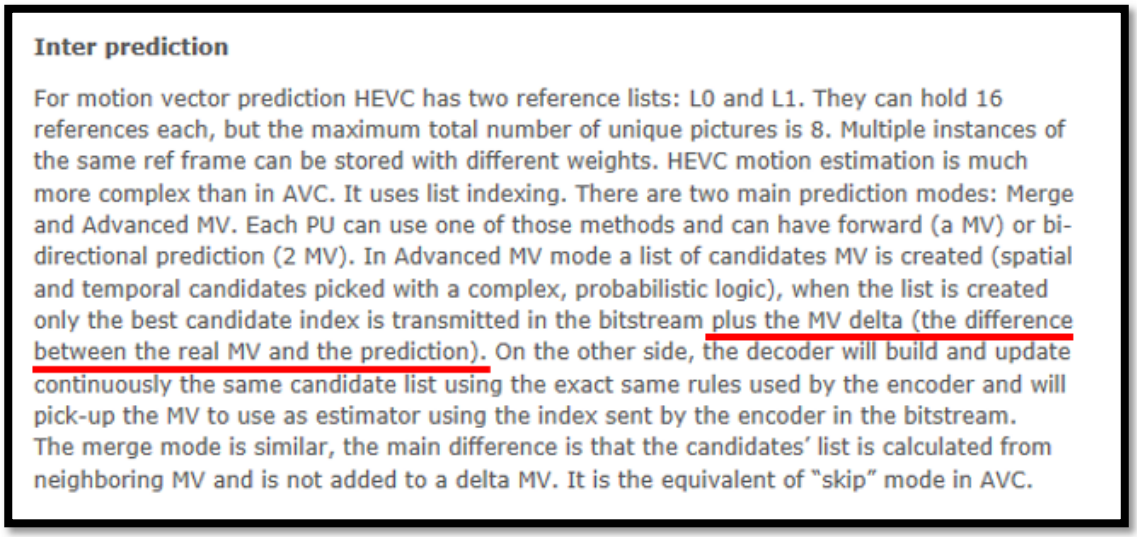
three spatially neighboring MVs. HEVC improves the MV prediction by applying an MV prediction competition as initially proposed in [18]. In HEVC, this competition was further adapted to large block sizes with so-called *advanced motion vector prediction* (AMVP) in [19]. In the DIS *Main profile*, AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered. The candidates

Philipp Helle, Simon Oudin, Benjamin Bross, Detlev Marpe, M. Oguz Bici, Kemal Ugur, Joel Jung, Gordon Clare, and Thomas Wiegand, *Block Merging for Quadtree-Based Partitioning in HEVC, IEEE TRANS. CIR. AND SYS. FOR VIDEO TECHNOLOGY, Vol. 22* No. 12 (December 2012) ("AMVP has two predictor candidates competing for the prediction. Two spatial motion vector predictor (MVP) candidates are considered and, when at least one of them is not available or they are redundant, a temporal motion vector prediction (TMVP) candidate is considered.").

521. One or more of the MediaTek '054 Products include a motion estimation unit comprising a generating unit for generating a set of candidate motion vectors for the group of

pixels, with the candidate motion vectors being extracted from a set of previously estimated motion vectors.

522. The MediaTek '054 Products contain functionality for generating match errors of the respective candidate motion vectors. The HEVC standard calculates match errors of respective candidate motion vectors. The match errors are referred to as the MV delta. The MV delta is the difference between the real MV and the candidate prediction.



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

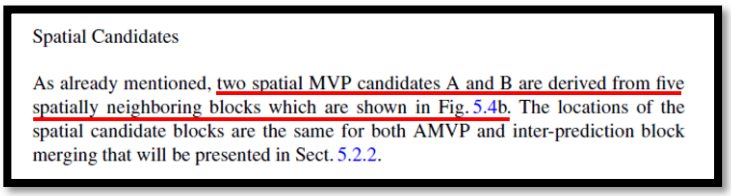
Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

523. Any implementation of the HEVC standard would infringe the '054 patent as every implementation of the standard requires the elements in one or more claims of the '054 patent, including but not limited to claim 1, by way of example: a match error unit for calculating match errors of respective candidate motion vectors and calculating the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

524. One or more of the MediaTek '054 Products include a motion estimation unit comprising a selector for selecting the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the

motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors.

525. The MediaTek '054 Products select the current motion vector from the candidate motion vectors by comparing the match errors of the respective candidate motion vectors, characterized in that the motion estimation unit is arranged to add a further candidate motion vector to the set of candidate motion vectors by calculating the further candidate motion vector on the basis of a first motion vector and a second motion vector, both belonging to the set of previously estimated motion vectors. The first motion vector is labeled 'A' and the second motion vector is labeled 'B.'

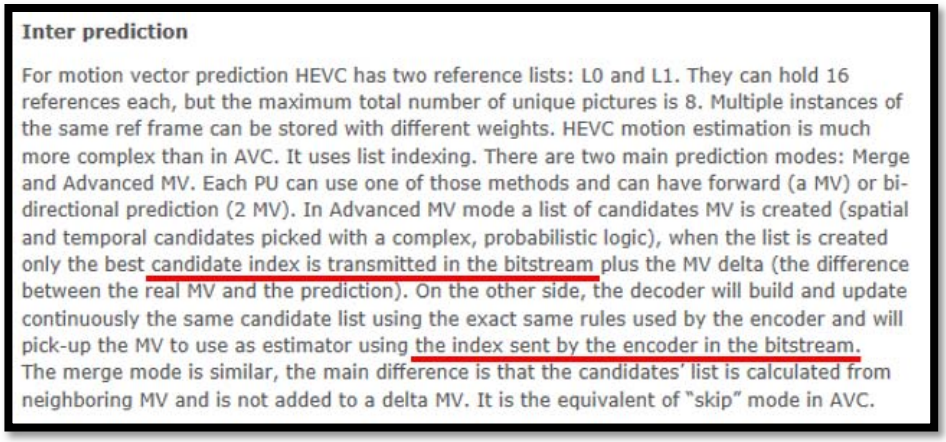


Spatial Candidates

As already mentioned, two spatial MVP candidates A and B are derived from five spatially neighboring blocks which are shown in Fig. 5.4b. The locations of the spatial candidate blocks are the same for both AMVP and inter-prediction block merging that will be presented in Sect. 5.2.2.

Gary Sullivan, *et al*., HIGH EFFICIENCY VIDEO CODING (HEVC) ALGORITHMS AND ARCHITECTURES at 117 (2014) (emphasis added).

526. Further, the MediaTek '054 Products perform motion vector "competition / weighted sample prediction" by comparing the match errors of the candidate motion vectors. The match errors generated by the MediaTek '054 Products comprise the difference value between the second motion vector and the first motion vector. Documentation of the encoding process states that the encoder will "pick up the MV [motion vector] to use as an estimator using the index sent by the encoder in the bitstream."



Inter prediction

For motion vector prediction HEVC has two reference lists: L0 and L1. They can hold 16 references each, but the maximum total number of unique pictures is 8. Multiple instances of the same ref frame can be stored with different weights. HEVC motion estimation is much more complex than in AVC. It uses list indexing. There are two main prediction modes: Merge and Advanced MV. Each PU can use one of those methods and can have forward (a MV) or bi-directional prediction (2 MV). In Advanced MV mode a list of candidates MV is created (spatial and temporal candidates picked with a complex, probabilistic logic), when the list is created only the best candidate index is transmitted in the bitstream plus the MV delta (the difference between the real MV and the prediction). On the other side, the decoder will build and update continuously the same candidate list using the exact same rules used by the encoder and will pick-up the MV to use as estimator using the index sent by the encoder in the bitstream. The merge mode is similar, the main difference is that the candidates' list is calculated from neighboring MV and is not added to a delta MV. It is the equivalent of "skip" mode in AVC.

Fabio Sonnati, *H.265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

527. The MediaTek '054 Products calculate the square of the difference between two corresponding pixels of the spatial position of the candidate block where the motion vector is located and the spatial position where the reference motion vector is located. As a result, this value is used to assess the similarity, or the matching degree, of a candidate block. Thus, in order to obtain the best matching vector, the MediaTek '054 Products apply a penalty value to every candidate block with a different motion vector (*MVx, MVy*) within the search window defined by the search range in the reference frame. Finally, a candidate block with the minimum penalty value will be denoted as the best matching block and used to calculate the best motion vector from the candidate motion vectors. The below excerpt from an article discussing the selection of a best motion vector describes that the selection of a motion vector is based on the position of the motion vector.

> The entire ME process is made up of three coarse-to-fine procedures, namely, MV prediction, integer-pixel ME and fractional-pixel ME. First, MV prediction predicts the start search position for the following motion search by utilizing the neighboring motion information. In HEVC, Advanced Motion Vector Prediction (AMVP), a new and effective technology that predicts the starting search position by referencing the motion vector (MV) information of spatial and temporal motion vector candidates, is adopted, which derives several most probable candidates based on data from adjacent PBs and the reference picture. The displacement between the starting search position and the current coding PU is called a predictive motion vector (PMV). HEVC also introduces a merge mode to derive the motion information from spatially or temporally neighboring blocks [1].

Yongfei Zhang, Chao Zhang, and Rui Fan, *Fast Motion Estimation in HEVC Inter Coding: An Overview of Recent Advances*, PROCEEDINGS, APSIPA ANNUAL SUMMIT AND CONFERENCE 2018 at 1 (November 2018) (emphasis added).

528. One or more of the MediaTek '054 Products include a motion estimation unit that calculates the further candidate motion vector on the basis of the first motion vector and the second motion vector, with the first motion vector belonging to a first forward motion vector field and the second motion vector belonging to a second forward motion vector field, with the first forward motion vector field and the second forward motion vector field being different. Specifically, the HEVC standard arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector. The further candidate motion vector is calculated at the end of the process (see the red box in the below diagram).

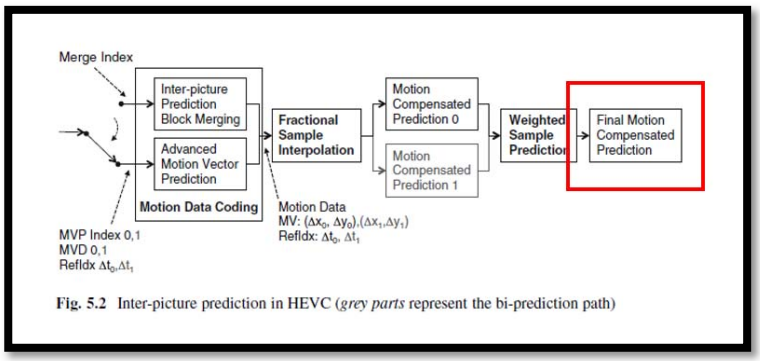


Fig. 5.2 Inter-picture prediction in HEVC (*grey parts* represent the bi-prediction path)

Gary J. Sullivan, *et al*., HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 115 (September 2014) (emphasis added).

529. One or more of the MediaTek ‘054 Products include a motion estimation unit that arranges to calculate the further candidate motion vector by calculating a difference between the second motion vector and the first motion vector.

530. The MediaTek ‘054 Products are available to businesses and individuals throughout the United States.

531. The MediaTek ‘054 Products are provided to businesses and individuals located in the State of Delaware.

532. By making, using, testing, offering for sale, and/or selling products and services for estimating a current motion vector for a group of pixels of an image, including but not limited to the MediaTek ‘054 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the ‘054 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

533. MediaTek also indirectly infringes the ‘054 patent by actively inducing infringement under 35 U.S.C. § 271(b).

534. MediaTek has had knowledge of the ‘054 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the ‘054 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the ‘054 Patent based on prior communications that identified the ‘054 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

535. MediaTek had knowledge of the ‘054 patent from at least May 15, 2012 onward based on MediaTek’s U.S. Patent No. 8,179,984 (the “‘984 Patent”). The ‘984 Patent was assigned to MediaTek, Inc. and during the prosecution of the ‘’984 Patent MediaTek identified the ‘054 patent family as relevant prior art to the ‘984 Patent.

536. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '054 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '054 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '054 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '054 Products that have the capability of operating in a manner that infringe one or more of the claims of the '054 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '054 Products to utilize the products in a manner that directly infringe one or more claims of the '054 patent.[42] By providing instruction and training to customers and end-users on how to use the MediaTek '054 Products in a manner that directly infringes one or more claims of the '054 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '054 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '054 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '054 patent. Accordingly, MediaTek has induced and continues to induce users of the accused

[42] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

products to use the accused products in their ordinary and customary way to infringe the '054 patent, knowing that such use constitutes infringement of the '054 patent.

537. The '054 patent is well-known within the industry as demonstrated by multiple citations to the '054 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '054 patent without paying a reasonable royalty. MediaTek is infringing the '054 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

538. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '054 patent.

539. As a result of MediaTek's infringement of the '054 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

COUNT XI
INFRINGEMENT OF U.S. PATENT NO. 8,135,073

540. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

541. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

542. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek devices that contain a decoder that is compliant with the HEVC standard, including but not limited to: MediaTek Automotive Products (MediaTek Autus I20 (MT2712)); MediaTek Mobile Products

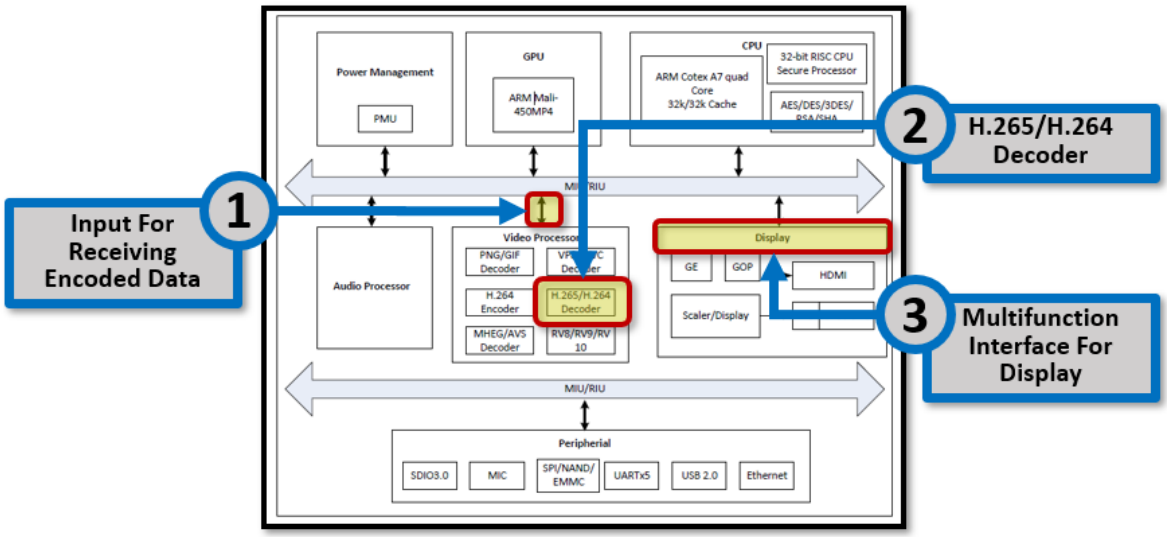
(MediaTek Helio A11, MediaTek Helio P10, MediaTek Helio P18, MediaTek Helio P20, MediaTek Helio P22, MediaTek Helio P23, MediaTek Helio P25, MediaTek Helio P30, MediaTek Helio P60, MediaTek Helio P70, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, MediaTek MT6732, MediaTek MT6735, MediaTek MT6738, MediaTek MT6739, MediaTek MT6750, MediaTek MT6752, and MediaTek MT6753); MediaTek Digital TV Products (MediaTek MT5582, MediaTek MT5596, and MediaTek MT5597); MediaTek Home Products (MediaTek MT8581, MediaTek MT8685, and MediaTek MT8693); and MediaTek Tablet Products (MediaTek MT8163V/A, MediaTek MT8163V/B, MediaTek MT8167A, MediaTek MT8167B, MediaTek MT8173, MediaTek MT8176, MediaTek MT8735B, MediaTek MT8735D, MediaTek MT8735M, MediaTek MT8735P, MediaTek MT8783, and MediaTek MT8785) (collectively, the "MediaTek Products").

543. MediaTek designs, makes, sells, offers to sell, imports, and/or uses products that contain HEVC decoding technology, including but not limited to the MStar System on Chip ("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MStar Product(s)").

544. The MediaTek Products and MStar Products (collectively, the "MediaTek '073 Product(s)") directly infringe the '073 patent.

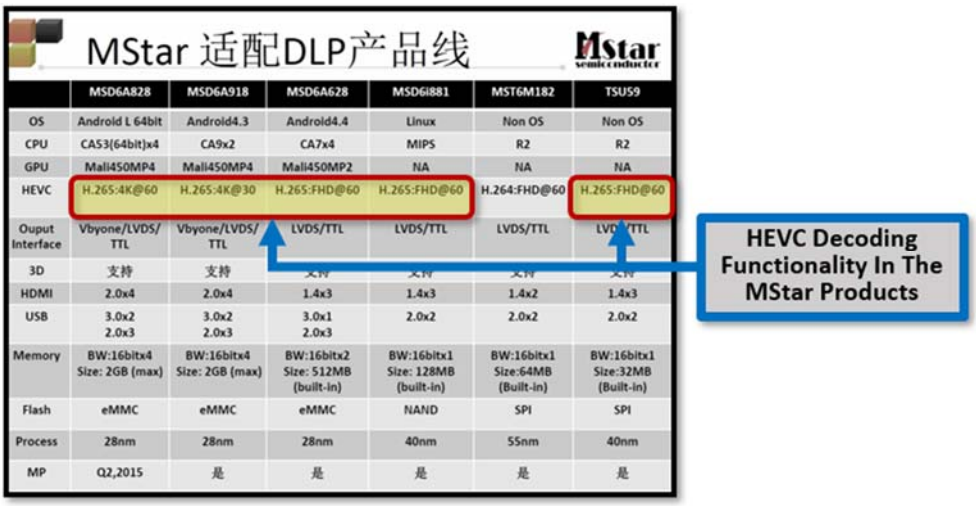
545. The MStar Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for

processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

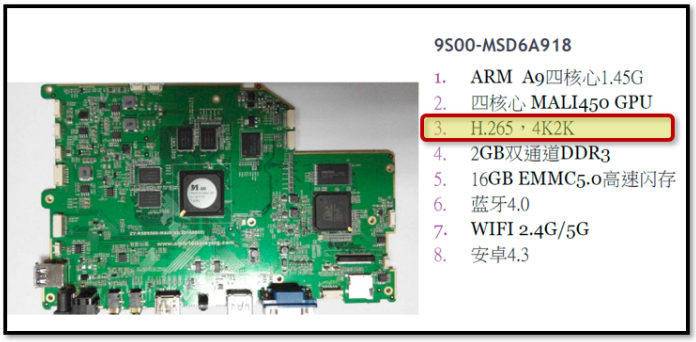
546. Documentation regarding the MStar Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MStar Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



	MSD6A828	MSD6A918	MSD6A628	MSD6i881	MST6M182	TSUS9
OS	Android L 64bit	Android4.3	Android4.4	Linux	Non OS	Non OS
CPU	CA53(64bit)x4	CA9x2	CA7x4	MIPS	R2	R2
GPU	Mali450MP4	Mali450MP4	Mali450MP2	NA	NA	NA
HEVC	H.265:4K@60	H.265:4K@30	H.265:FHD@60	H.265:FHD@60	H.264:FHD@60	H.265:FHD@60
Ouput Interface	Vbyone/LVDS/ TTL	Vbyone/LVDS/ TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL	LVDS/TTL
3D	支持	支持				
HDMI	2.0x4	2.0x4	1.4x3	1.4x3	1.4x2	1.4x3
USB	3.0x2 2.0x3	3.0x2 2.0x3	3.0x1 2.0x3	2.0x2	2.0x2	2.0x2
Memory	BW:16bitx4 Size: 2GB (max)	BW:16bitx4 Size: 2GB (max)	BW:16bitx2 Size: 512MB (built-in)	BW:16bitx1 Size: 128MB (built-in)	BW:16bitx1 Size:64MB (Built-in)	BW:16bitx1 Size:32MB (Built-in)
Flash	eMMC	eMMC	eMMC	NAND	SPI	SPI
Process	28nm	28nm	28nm	40nm	55nm	40nm
MP	Q2,2015	是	是	是	是	是

MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

547. The MStar Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. The following excerpt from a presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MStar Products that contain a decoder that conforms to the H.265 standard.



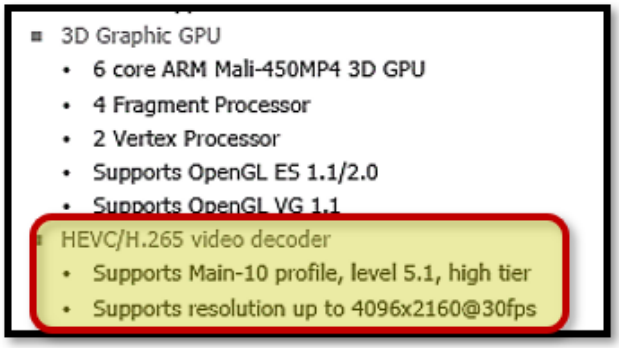
Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (annotation added) (showing that the MSD6A918 Product contains a decoder compliant with the H.265 standard).

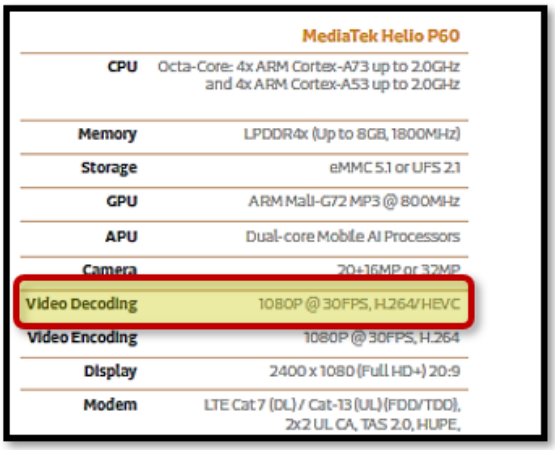
548. Datasheets from MediaTek also establish that the accused MStar Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states:

"all in one 的SOC 芯片, 芯片主要功能规格参数如下: 支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60"[43]

MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

549. Similarly, the MediaTek datasheets for the MSO9280MC and Helio P60 products identifies that they contain an HEVC H.265 decoder.

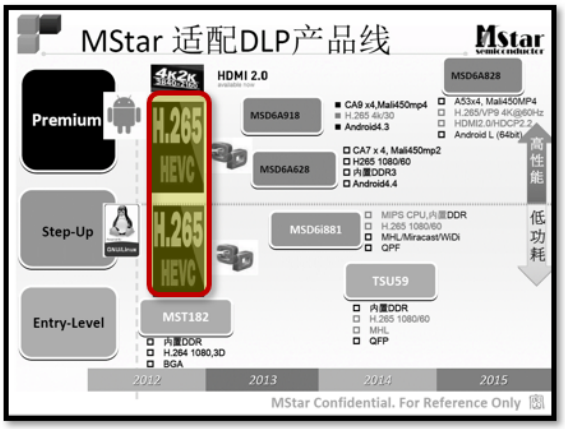




MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added)=; MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 at 2 (2018) (annotation added).

550. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MStar Products.

[43] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."



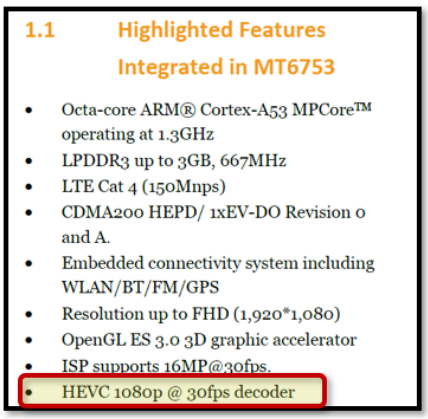
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

551. Documentation from MediaTek customers such as TCL that incorporate the accused MStar Products into devices such as televisions also identifies the accused MStar Products as containing an H.265 decoder.

类别	项目	L55H8800-CUD
输入和输出	ATV/DTV(DVB-C/DTMB) (PAL D/K I B/G)	✓
	HDMI (480i/p,576i/p,720p up to1080i/p,4K2K,with HDCP)	3 路，HDMI2 与 MHL 复用 支持 4K2K@30Hz 支持 H.265 格式
	VGA	无
	VGA/DVI audio	与 YPbPr 共用
	YPbPr (可支持 480i 到 1080p)	无
	SPDIF output	与AVout共用

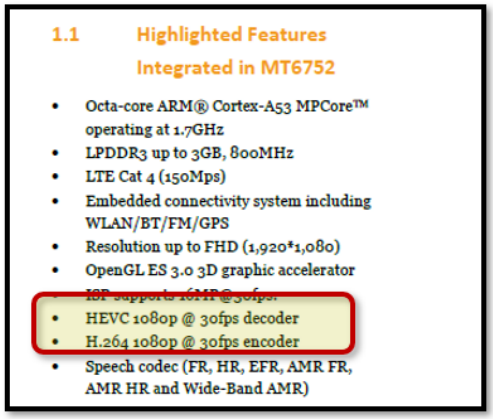
TCL PRODUCT BRIEF: MS918 机芯手册V1.0 at 35 (March 18, 2015) (annotation added) (showing that the MS918 chip from MStar contains a H.265 compliant decoder).

552. Technical briefs from MediaTek similarly identify the accused MediaTek products as containing a decoder that complies with the HEVC standard. For example, the MT6753 and MT6752 Application Processors contains a video decoder that complies with the HE VC standard.



1.1 Highlighted Features Integrated in MT6753

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.3GHz
- LPDDR3 up to 3GB, 667MHz
- LTE Cat 4 (150Mnps)
- CDMA200 HEPD/ 1xEV-DO Revision 0 and A.
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder

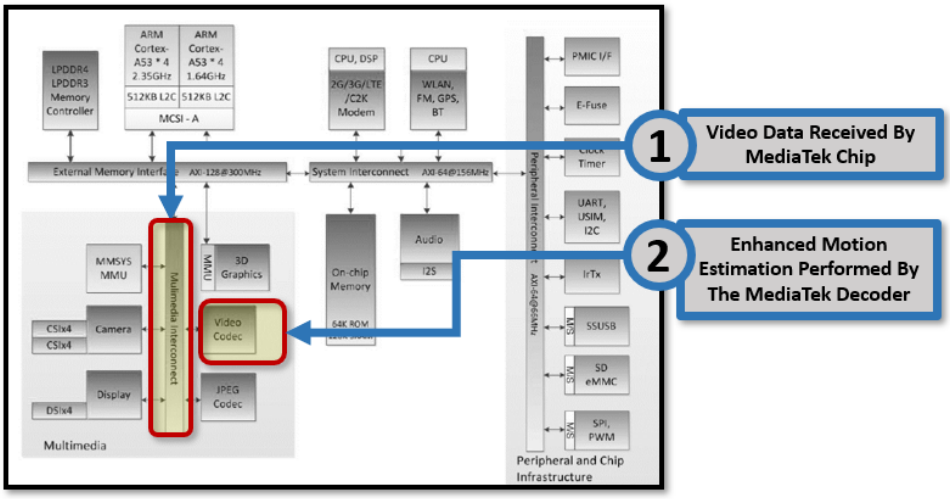


1.1 Highlighted Features Integrated in MT6752

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.7GHz
- LPDDR3 up to 3GB, 800MHz
- LTE Cat 4 (150Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (November 27, 2014) ("The chip integrates Octa-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards."); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (June 10, 2014) (annotation added) ("The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.").

553. MediaTek documentation shows the interconnects that connect the video decoding engine to the rest of the application processor. For example, MediaTek documentation for the MT6757 chip (i.e., the Helio P20 chip) shows connections to the video codec engine.



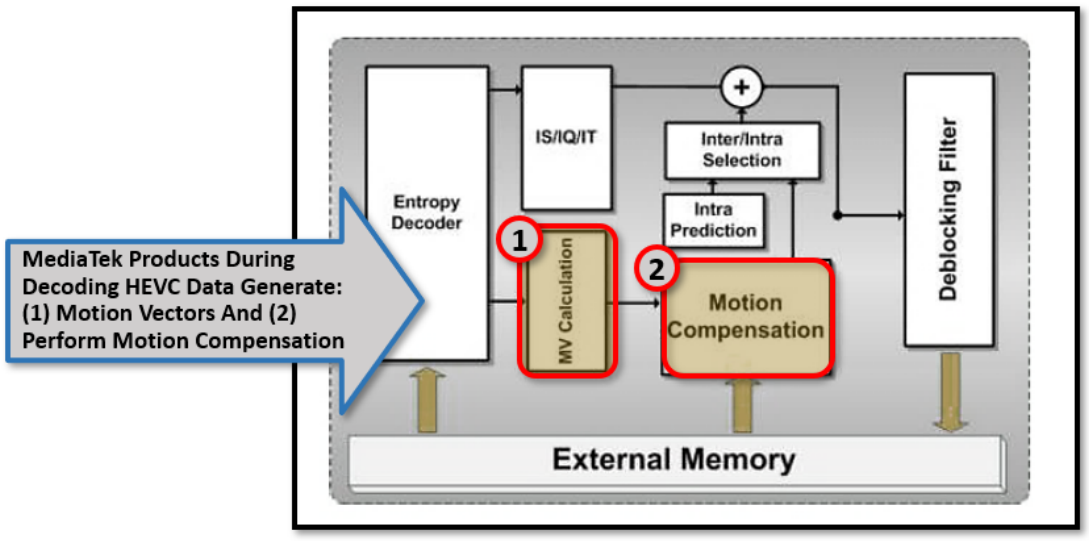
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 18 (June 20, 2016) (annotations added).

554. MediaTek technical documentation establishes the accused products (e.g., the MT6757 application processor) include an HEVC compliant decoder.

> All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

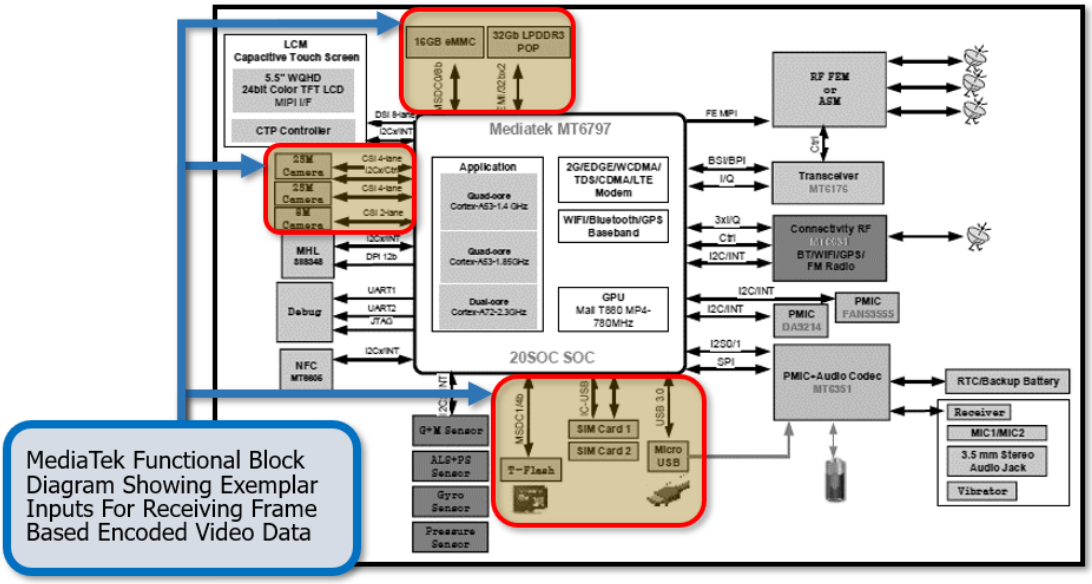
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 7 (June 20, 2016) (emphasis added) (describing that the MediaTek product includes a decoder for "HEVC 4K @ 30fps").

555. The architecture and core blocks of HEVC decoder ("VDEC") are shown in the below diagram including the following functional components: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra prediction, Motion Compensation, and De-Blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is sent to the display stage.



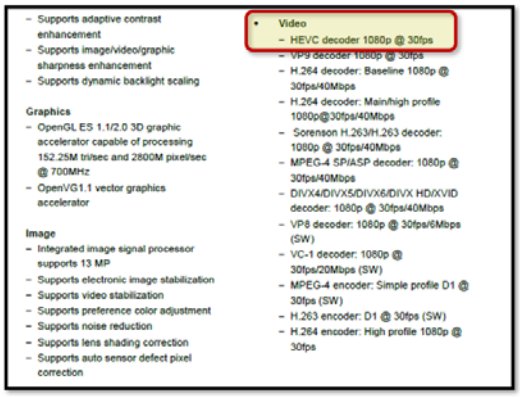
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 276 (July 19, 2016) (annotations added)

556. The accused MediaTek '073 Products receive HEVC encoded data through a variety of inputs. The below excerpt from MediaTek's technical documentation identifies the inputs for receiving HEVC encoded video data as part of the decoding process.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 12 (July 19, 2016) (annotations added) (showing a high-level functional block diagram of the MT6797 product).

557. MediaTek documentation similarly identifies that the MediaTek '073 Products contain an "HEVC decoder" as shown in the below excerpt from a MediaTek Technical Brief for the MT6592 Octa-Core Smartphone Application Processor.



MT6592 Octa-Core Smartphone Application Processor Technical Brief, MEDIATEK DOCUMENTATION at 8 and 11 (July 6, 2013) (annotation added) ("Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6592 is the brand-new generation smart phone SoC integrating MediaTek HSPA R8 modem, 1.7GHz Octa-core ARM® Cortex-A7 MPCoreTM, 3D graphics and high-definition 1080p video decoder.").

558. MediaTek documentation states that the MediaTek '073 Products are compliant with the HEVC standard as shown in the following excerpts.

559. The MediaTek ‘073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the MediaTek ‘073 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by MediaTek ‘073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

560. The MediaTek ‘073 Products comprise a video decoder for decoding video images. Specifically, the MediaTek ‘073 Products contain functionality for video decoding through H.265/High Efficiency Video Coding (“HEVC”) decoding.

561. The MediaTek ‘073 Products contain a processor for decoding the received encoded frame-based encoded video data. Further, the MediaTek ‘073 Products apply a remapping policy to the first frame of decoded video data using a region-based luma analysis. As part of the decoding process performed by MediaTek ‘073 Products, a reference picture (first frame) is decoded and two in-loop filters (deblocking and a sample adaptive offset) are applied to the reference picture.

562. The MediaTek ‘073 Products have an input for receiving frame-based encoded video information. Specifically, the MediaTek ‘073 Products receive frame-based encoded video information in the form of video data that is encoded in the High

563. The MediaTek ‘073 Products include inputs for receiving and decoding HEVC video data

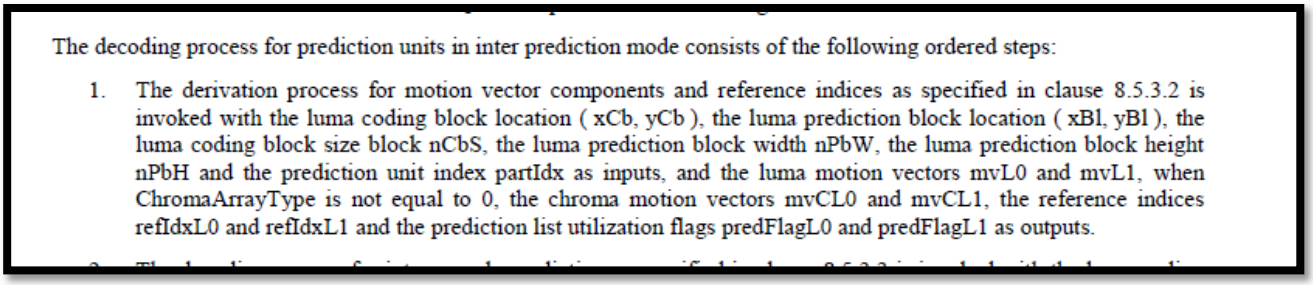
564. The MediaTek ‘073 Products incorporate a decoding unit for decoding the frame of the received video data. The encoding and decoding process for video data received by the

MediaTek '073 Products use inter-picture prediction wherein motion data comprises the selection of a reference frame and motion vectors to be applied in predicting the samples of each block.

565. One or more of the MediaTek '073 Products include technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation.

566. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '073 Products – necessarily infringe the '073 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '073 patent, including but not limited to claim 14 of the '073 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND Multimedia SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '073 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

567. The MediaTek '073 Products comply with the HEVC standard, which requires that motion vectors are recovered from the second frame in the video stream.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

568. MediaTek has directly infringed and continues to directly infringe the '073 patent by, among other things, making, using, offering for sale, and/or selling technology for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the MediaTek '073 Products. The following excerpt explains how HEVC is a form of frame-based encoded video information.

> One way of achieving high video compression is to predict pixel values for a frame based on prior and succeeding pictures in the video. Like its predecessors, H.265 features the ability to predict pixel values between pictures, and in particular, to specify in which order pictures are coded and which pictures are predicted from which. The coding order is specified for Groups Of Pictures (GOP), where a number of pictures are grouped together and predicted from each other in a specified order. The pictures available to predict from, called reference pictures, are specified for every individual picture.

Johan Bartelmess. *Compression Efficiency of Different Picture Coding Structures in High Efficiency Video Coding (HEVC),* UPTEC STS 16006 at 4 (March 2016) (emphasis added).

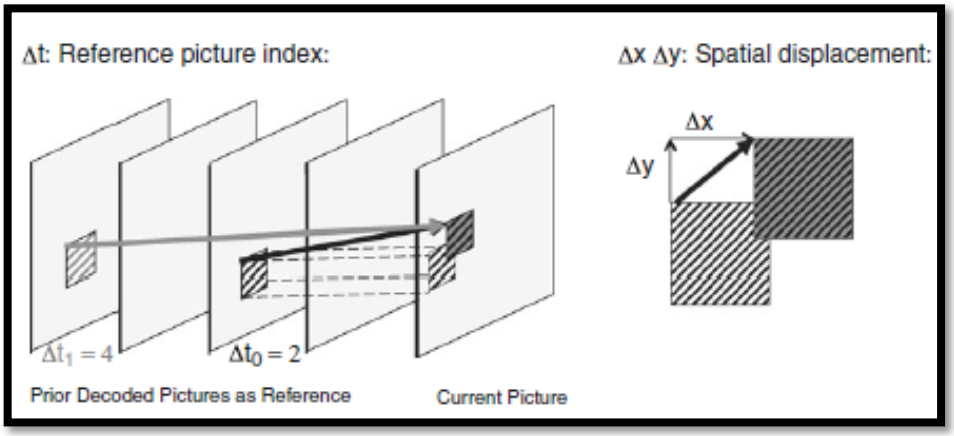
569. The MediaTek '073 Products receive encoded video data that is encoded using inter-frame coding. Specifically, the encoded video stream received by the MediaTek '073 Products is coded using its predecessor frame. Inter-prediction used in the encoded video data received by the MediaTek '073 Products allows a transform block to span across multiple prediction blocks for inter-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical

> dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

570. The encoded video stream received by the MediaTek '073 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, a video picture is divided into rectangular blocks. Assuming homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



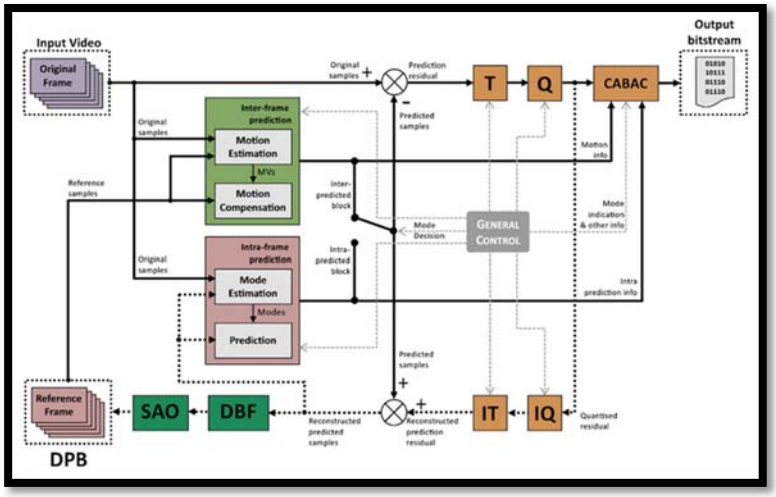
Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

571. The following excerpt from an article describing the architecture of the encoded video stream received by the MediaTek '073 Products describes the functionality wherein the second encoded frame of the video data is dependent on the encoding of a first frame. "HEVC inter prediction uses motion vectors pointing to one reference frame . . . to predict a block of pixels."

> HEVC inter prediction uses motion vectors pointing to one reference frame (uni-prediction) or two reference frames (bi-prediction) to predict a block of pixels. The size of the predicted block, called Prediction Unit (PU), is determined by the Coding Unit (CU) size and its partitioning mode. For example, a 32×32 CU with 2N×N partitioning is split into two PUs of size 32×16, or a 16×16 CU with nL×2N partitioning is split into 4×16 and 12×16 PUs.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) (September 2014).

572. The following diagram shows how the MediaTek Products receive video data encoded using inter-frame prediction. Specifically, interframe prediction generates a motion vector based on the motion estimation across a first and second frame.



Guilherme Corrêa, *et al.*, COMPLEXITY-AWARE HIGH EFFICIENCY VIDEO CODING at 16 (2015).

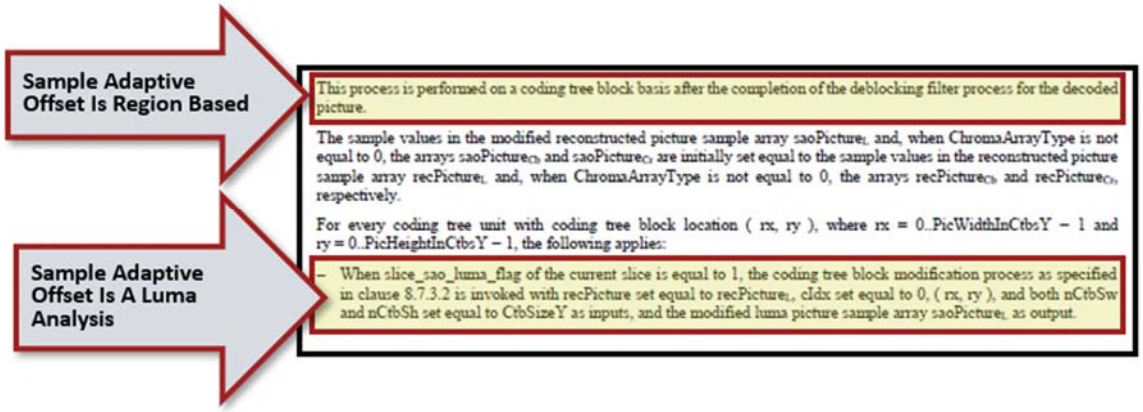
573. One or more of the MediaTek '073 Products reduce the processing capacity required for providing video enhancements to video processing through re-mapping of previous frames for subsequent frames.

574. Any implementation of the HEVC standard would infringe the '073 patent as every possible implementation of the standard requires: receiving a video stream containing encoded frame based video information (including both an encoded first frame and an encoded second frame); the encoded second frame that is received depends on the encoding of the first frame, the

encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame; the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame; decoding the video stream by recovering the motion vectors in the second stream; and determining a re-mapping strategy for the video enhancement of the decoded first frame using a region-based analysis where the first frame is remapped using a remapping strategy and at least one region of the second frame is remapped depending on the re-mapping strategy for corresponding regions of the first frame.

575. The MediaTek '073 Products' use of sample adaptive offset is a region-based luma analysis that is applied to the decoded first frame (reference picture). "The SAO reduces sample distortion by first classifying the samples in the region into multiple categories with as selected classifier and adding a specific offset to each sample depending on its category. The classifier index and the offsets for each region are signaled in the bitstream." Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 185 (September 2014) (emphasis added).

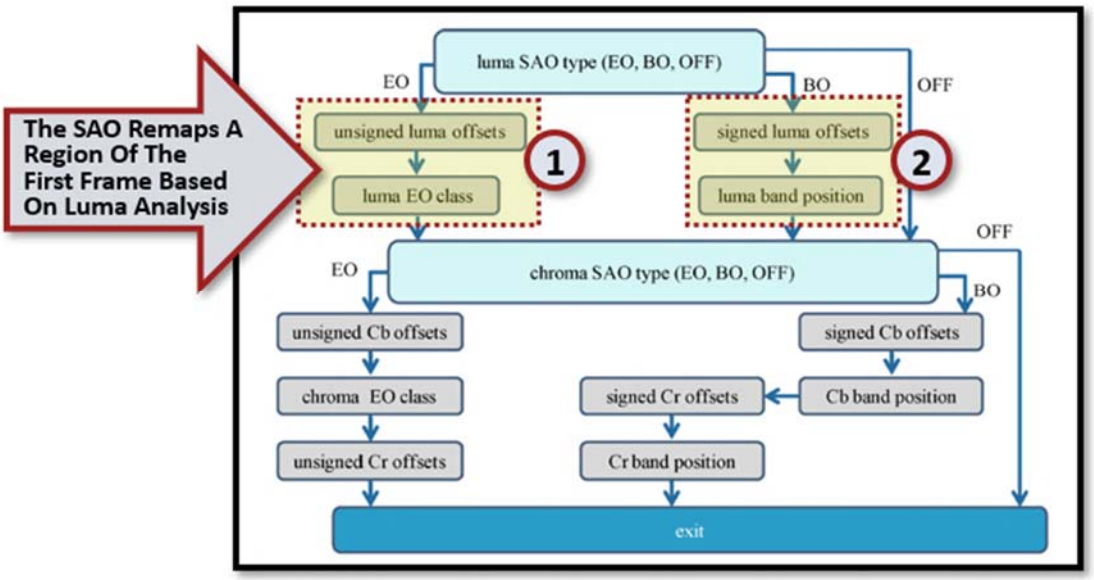
576. Further, the HEVC documentation requires that the application of a sample adaptive offset be region based (*e.g.*, applied to a coding block) ("This process is performed on a coding block basis after the completion for the deblocking filter process for the decoded picture").



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.7.3.1 (April 2015) (annotations added).

577. The MediaTek '073 Products contain functionality wherein a decoder applies sample adaptive offset to a decoded reference frame (first frame). Further, the MediaTek '073 Products apply the sample adaptive offset functions to remap a portion of the region based on luminance values (luma). "SAO can be applied to not only luma but also chroma." Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 at 1765 (December 2012).

578. The MediaTek '073 Products apply the sample adaptive offset to a coding tree unit (region in the first frame), a luminance analysis is performed using two luminance analysis techniques: Edge Offset ("EO") and Band Offset ("BO"). Edge Offset "uses four 1-D directional patterns for sample classification: horizontal, vertical, 135° diagonal, and 45° diagonal." Chih-Ming Fu, *et al.*, Sample Adaptive Offset in the HEVC Standard, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1757 (December 2012). Band Offset "implies one offset is added to all samples of the same band. The sample value range is equally divided into 32 bands." *Id*. at 1757. The below diagram shows that the MediaTek '073 Products use different sample adaptive offsets in a region of the first frame in conducting a luminance analysis.



Chih-Ming Fu, *et al.*, *Sample Adaptive Offset in the HEVC Standard*, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 22, NO. 12 AT 1759 (December 2012) (annotations added showing (1) edge offset and (2) band offset luma analysis).

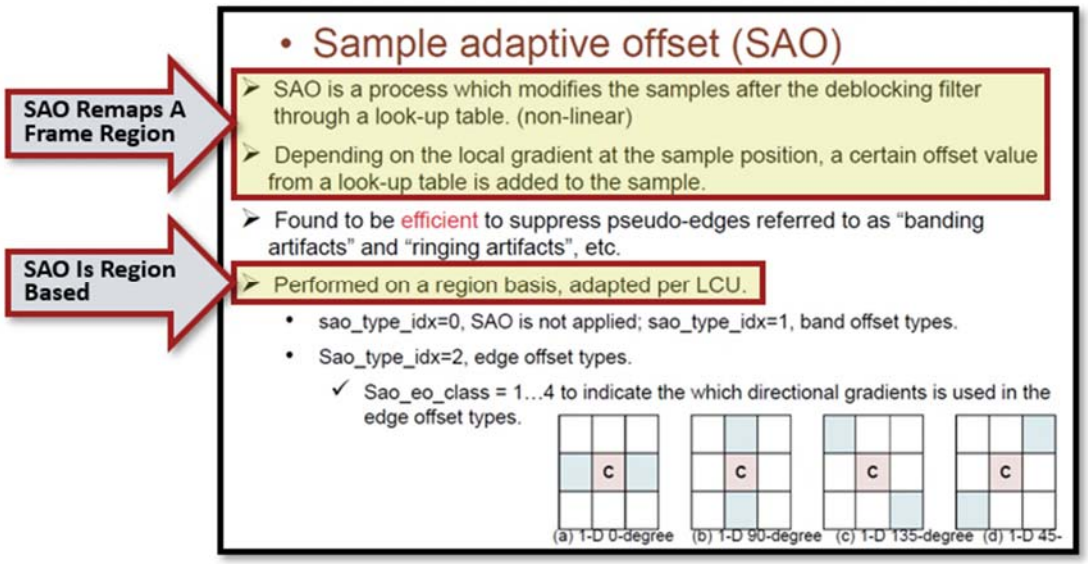
579. Further, HEVC documentation makes clear that the application of the standard adaptive offset remapping policy is based on a luminance analysis. The below shows that slices of a region have a standard adaptive offset applied based on a "luma flag."

if(sample_adaptive_offset_enabled_flag) {	
slice_sao_luma_flag	u(1)
if(ChromaArrayType != 0)	
slice_sao_chroma_flag	u(1)

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § F.7.3.6.1 (April 2015) ("sample_adaptive_offset_enabled_flag equal to 1 specifies that the sample adaptive offset process is applied to the reconstructed picture after the deblocking filter process.").

580. Commentary on the use of sample adaptive offset functionality in decoding HEVC video further confirms that the use of Sample Adaptive Offset (such as that implemented by the MediaTek '073 Products) is region based and remaps pixel values in a region of a frame by

modifying pixels based on an offset value. "[A]fter the deblocking filter through a look-up table . . . [and applying] a certain offset value from a look-up-table is added to the sample."[44]



Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013) (annotations added).

581. When the MediaTek '073 Products decode a second frame, the application of the remapping policy (sample adaptive offset) will be determined based on the application of sample adaptive offset to the first frame (reference picture). Thus, the application of the remapping policy (sample adaptive offset) to the first frame has the effect of increasing the quality of the reference picture such that the second frame might no longer require the application of sample adaptive offset (remapping policy).[45]

> The second in-loop filter, SAO, is applied to the output of the deblocking filter and further improves the quality of the decoded picture by attenuating ringing artifacts and changes in sample intensity of some areas of a picture. The most important advantage of the in-loop filters is improved subjective quality of reconstructed

[44] Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 43 (October 2013).
[45] Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) at 171 (September 2014) ("HEVC defines two in-loop filters, deblocking and sample adaptive offset (SAO), which significantly improve the subjective quality of decoded video sequences as well as compression efficiency by increasing the quality of the reconstructed/ reference pictures.").

> pictures. In addition, using the filters in the decoding loop also increases the quality of the reference pictures and hence also the compression efficiency.

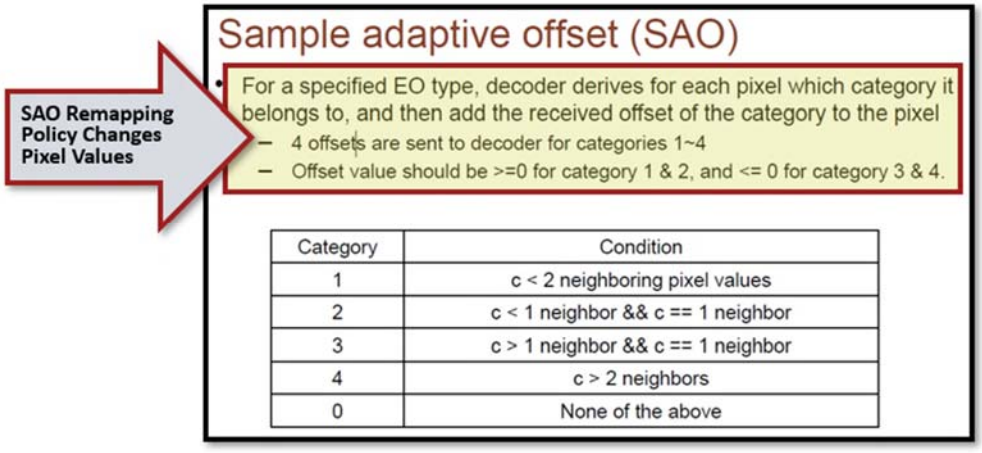
Andrey Norkin, Chih-Ming Fu, Yu-Wen Huang, and Shawmin Lei, *In-Loop Filters In HEVC*, IN HIGH EFFICIENCY VIDEO CODING (HEVC) (Vivienne Sze, Madhukar Budagavi, and Gary J. Sullivan (Editors)) at 171 (September 2014) (annotations added).

582. Sample adaptive offset as implemented by the MediaTek '073 Products is a policy that remaps the values of pixels. If sample adaptive offset is applied to a reference frame, regions in a second frame might not require the application of the remapping policy as the reference frame that was used to generate the second frame was of a better quality.

> SAO classifies each pixel into one of four bands or one of four edge types and adds an offset to it. For band offsets, the band of each pixel depends on its value and the position of the four bands. For edge offsets, the edge of each pixel depends on the whether its value is larger or smaller than two of its neighbors. The selection between band offsets and edge offsets, position of bands, choice of neighbors for edge offsets, and values of the offsets are signaled at the CTU level for luma and chroma separately.

Mehul Tikekar, *et al., Decoder Hardware Architecture for HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 335 (September 2014).

583. The following excerpt from a presentation describing HEVC decoding provides details on how the application of sample adaptive offset remaps pixel values by adding an offset to the pixel value based on a luma analysis.

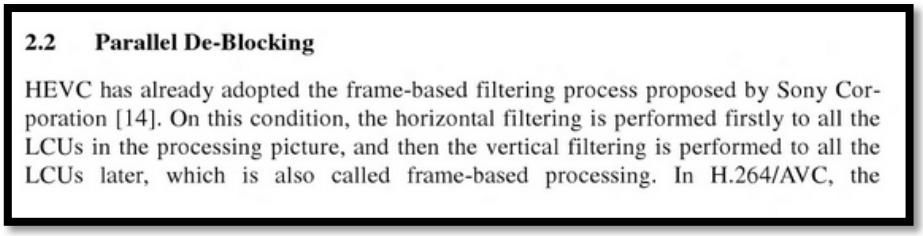


Oscar C. Au, HIGH EFFICIENCY VIDEO CODING (HEVC) PRESENTATION at 44 (October 2013) (annotation added).

584. The MediaTek ‘073 Products receive encoded video data wherein the second frame includes a region encoding a motion vector difference in position between the region corresponding to the second frame indicating the first frame, the motion vector defines a region between the frame and the second frame corresponding to the first region the correspondence relationship. Specifically, the encoded video data received by the MediaTek ‘073 Products use a translational motion model wherein the position of the block in a previously decoded picture is indicated by a motion vector: Δx; Δy where Δx specifies the horizontal and Δy the vertical displacement relative to the position of the current block. The motion vectors: Δx and Δy are of fractional sample accuracy to more accurately capture the movement of the underlying object. Interpolation is applied on the reference pictures to derive the prediction signal when the corresponding motion vector has fractional sample accuracy. The previously decoded picture is referred to as the reference picture and indicated by a reference index Δt to a reference picture list. These translational motion model parameters, *i.e.*, motion vectors and reference indices, are further referred to as motion data.

585. One or more of the MediaTek ‘073 Products enable the provision of enhanced video pictures with minimal additional hardware costs for the components required to successfully process the video data.

586. One or more of the MediaTek ‘073 Products include an input for receiving a video stream containing encoded frame-based video information including an encoded first frame and an encoded second frame.

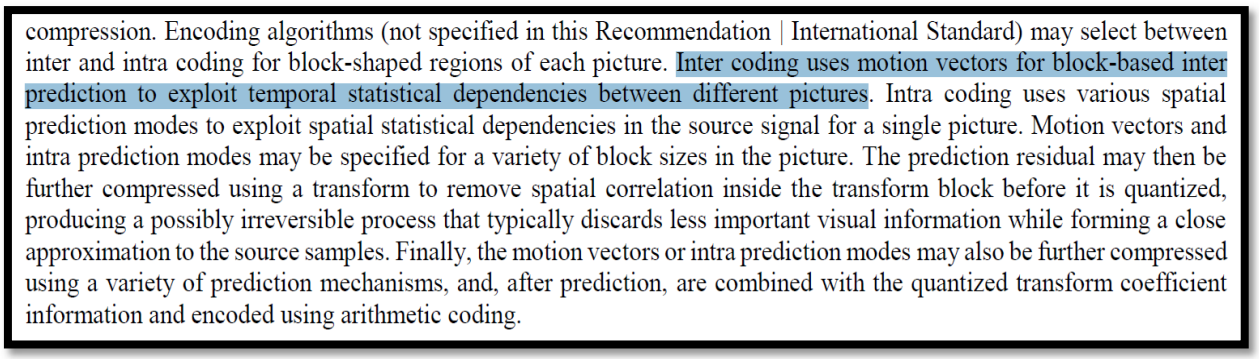


2.2 Parallel De-Blocking

HEVC has already adopted the frame-based filtering process proposed by Sony Corporation [14]. On this condition, the horizontal filtering is performed firstly to all the LCUs in the processing picture, and then the vertical filtering is performed to all the LCUs later, which is also called frame-based processing. In H.264/AVC, the

Ming-Ting Sun, *et al*., *Advances in Multimedia Information Processing*, PCM 2012: 13TH PACIFIC-RIM CONFERENCE ON MULTIMEDIA PROCEEDINGS VOLUME 7674 at 274 (December 4-6, 2012) ("HEVC has already adopted the frame-based filtering process proposed by Sony Corporation.").

587. One or more of the MediaTek '073 Products include a video decoder comprising an input for receiving video information wherein the encoding of the second frame depends on the encoding of the first frame, the encoding of the second frame includes motion vectors indicating differences in positions between regions of the second frame and corresponding regions of the first frame, the motion vectors define correspondence between regions of the second frame and corresponding regions of the first frame. The Overview of Design Characteristics in the HEVC Standard describes the use of "motion vectors for block-based inter prediction to exploit temporal statistical dependencies between frames."

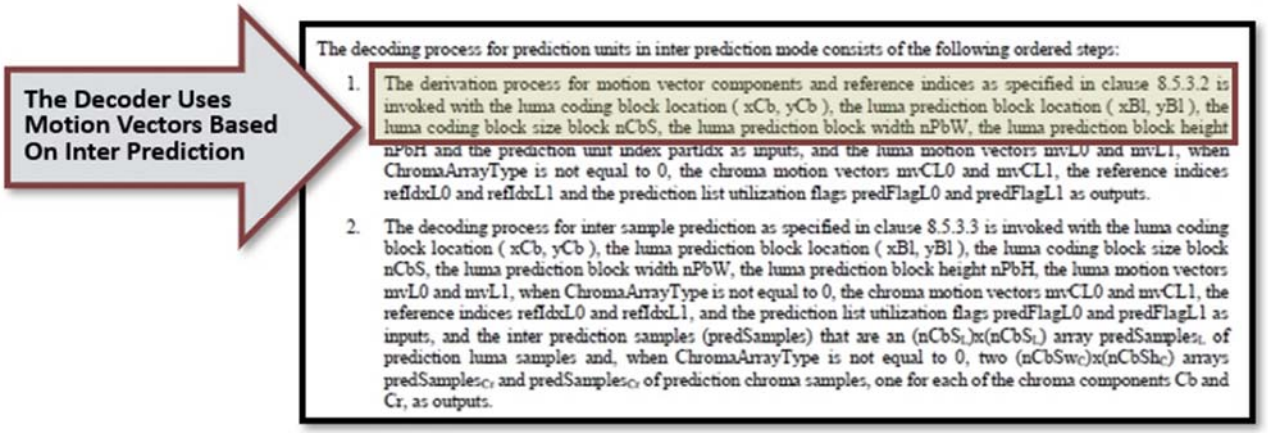


compression. Encoding algorithms (not specified in this Recommendation | International Standard) may select between inter and intra coding for block-shaped regions of each picture. Inter coding uses motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra coding uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. Motion vectors and intra prediction modes may be specified for a variety of block sizes in the picture. The prediction residual may then be further compressed using a transform to remove spatial correlation inside the transform block before it is quantized, producing a possibly irreversible process that typically discards less important visual information while forming a close approximation to the source samples. Finally, the motion vectors or intra prediction modes may also be further compressed using a variety of prediction mechanisms, and, after prediction, are combined with the quantized transform coefficient information and encoded using arithmetic coding.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 0.7 (April 2015) (annotation added).

588. One or more of the MediaTek '073 Products include a video decoder comprising a decoding unit for decoding the frames, wherein the decoding unit recovers the motion vectors for

the second frame. Further, HEVC documentation shows that "motion vectors are used during the decoding process for prediction units in inter prediction mode."



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (April 2015) (annotation added).

589. One or more of the MediaTek '073 Products include a video decoder comprising a processing component configured to determine a re-mapping strategy for video enhancement of the decoded first frame using a region-based analysis, re-map the first frame using the re-mapping strategy, and re-map one or more regions of the second frame depending on the re-mapping strategy for corresponding regions of the first frame.

590. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '073 Products in regular business operations.

591. The MediaTek '073 Products are available to businesses and individuals throughout the United States.

592. The MediaTek '073 Products are provided to businesses and individuals located in the State of Delaware.

593. By making, using, testing, offering for sale, and/or selling products and services for enhancing subsequent images of a video stream in which frames are encoded based on previous

frames using prediction and motion estimation, including but not limited to the MediaTek '073 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '073 patent, including at least claim 14 pursuant to 35 U.S.C. § 271(a).

594. MediaTek also indirectly infringes the '073 patent by actively inducing infringement under 35 U.S.C. § 271(b).

595. MediaTek has had knowledge of the '073 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '073 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '073 Patent based on prior communications that identified the '073 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

596. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '073 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '073 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '073 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '073 Products that have the capability of operating in a manner that infringe one or more of the claims of the '073 patent, including at least claim 14, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '073 Products to utilize the products in a manner that directly infringe one

or more claims of the '073 patent.[46] By providing instruction and training to customers and end-users on how to use the MediaTek '073 Products in a manner that directly infringes one or more claims of the '073 patent, including at least claim 14, MediaTek specifically intended to induce infringement of the '073 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '073 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '073 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '073 patent, knowing that such use constitutes infringement of the '073 patent.

597. The '073 patent is well-known within the industry as demonstrated by multiple citations to the '073 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '073 patent without paying a reasonable royalty. MediaTek is infringing the '073 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

598. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '073 patent.

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[46] *See, e.g.*, *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 (June 20, 2016); MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (November 27, 2014); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (June 10, 2014); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 (2018); *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); and MSD6180 SOC DATASHEET (2016).

599. As a result of MediaTek's infringement of the '073 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

COUNT XII
INFRINGEMENT OF U.S. PATENT NO. 8,189,105

600. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

601. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for processing pixel information based on received motion and edge data.

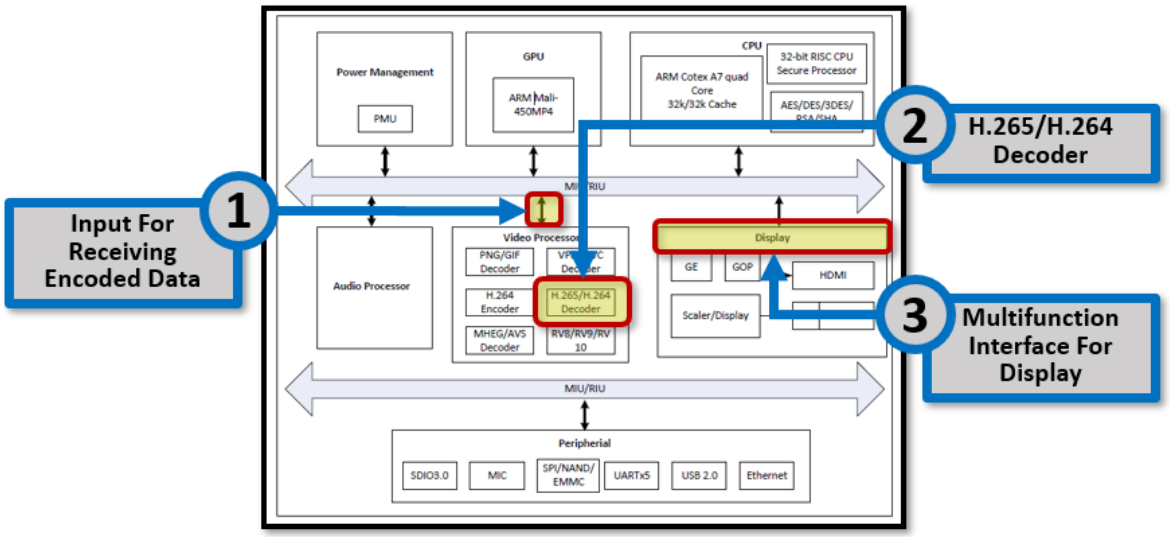
602. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek graphic processors containing H.265/High Efficiency Video Coding ("HEVC") processing functionality, including but not limited to: MediaTek Automotive Products (MediaTek Autus I20 (MT2712)); MediaTek Mobile Products (MediaTek Helio A11, MediaTek Helio P10, MediaTek Helio P18, MediaTek Helio P20, MediaTek Helio P22, MediaTek Helio P23, MediaTek Helio P25, MediaTek Helio P30, MediaTek Helio P60, MediaTek Helio P70, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, MediaTek MT6732, MediaTek MT6735, MediaTek MT6738, MediaTek MT6739, MediaTek MT6750, MediaTek MT6752, and MediaTek MT6753); MediaTek Digital TV Products (MediaTek MT5582, MediaTek MT5596, and MediaTek MT5597); MediaTek Home Products (MediaTek MT8581, MediaTek MT8685, and MediaTek MT8693); and MediaTek Tablet Products (MediaTek MT8163V/A, MediaTek MT8163V/B, MediaTek MT8167A, MediaTek MT8167B, MediaTek MT8173, MediaTek

MT8176, MediaTek MT8735B, MediaTek MT8735D, MediaTek MT8735M, MediaTek MT8735P, MediaTek MT8783, and MediaTek MT8785) (collectively, the "MediaTek Products").

603. MediaTek designs, makes, sells, offers to sell, imports, and/or uses products that contain HEVC decoding technology, including but not limited to the MStar System on Chip ("SoC") Products including the following model numbers: MSD3Z173, MSD3Z171, MSD6180, MSD6A918, MSO9280, MSD3Z173, MSO9380, MSD6i881, MSD6A628, MSD6A828, MSD6488E, MSD3553, MSD6486, MSD6A338, MSD6A638, and MSD6A938 (collectively, the "MStar Product(s)").

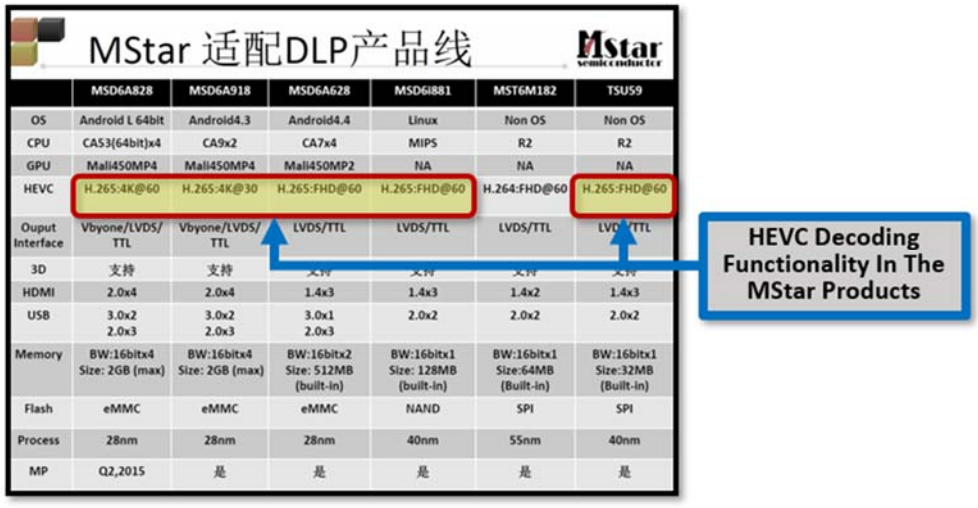
604. The MediaTek Products and MStar Products (collectively, the "MediaTek '105 Product(s)") directly infringe the '105 patent.

605. The MStar Products comprise an input for receiving encoded data and a decoder that is compliant with the H.265 standard. The below excerpt from MediaTek documentation shows a block diagram with annotations identifying: (1) inputs for receiving encoded data for processing; (2) the H.265 compliant decoder; and (3) the interface used for display of the decoded video data.



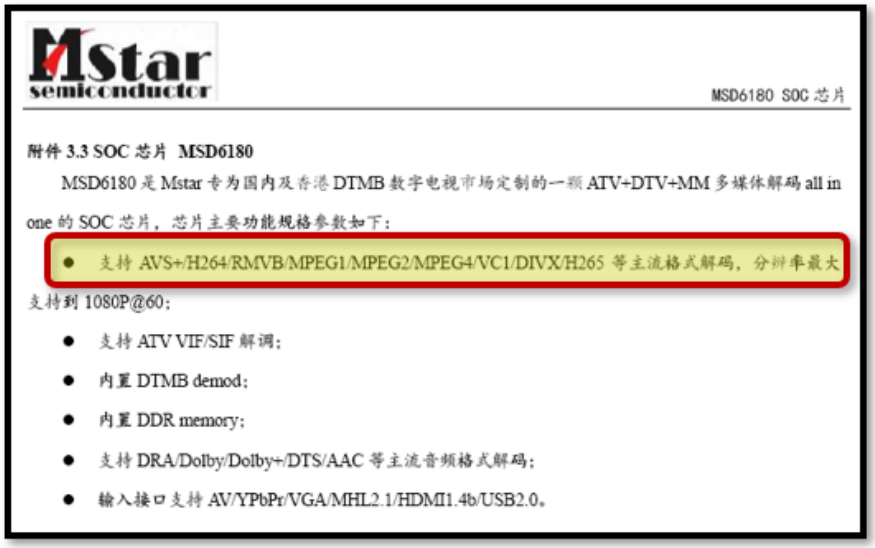
MSO9280MC Smart Set-Top Box Controller for IP.DRM Applications, MSTAR PRODUCT BRIEF VERSION 3.0 at 4 (August 4, 2015) (annotations added).

606. Documentation regarding the MStar Products identifies that they contain decoding functionality that is compliant with the H.265 standard. For example, the below excerpt shows that the accused MStar Products include decoders for the display of the following types of encoded video data: H.265:4K@60, H.265:4K@30, and H.265:FHD@60.



MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 12 (December 18, 2014) (annotations added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

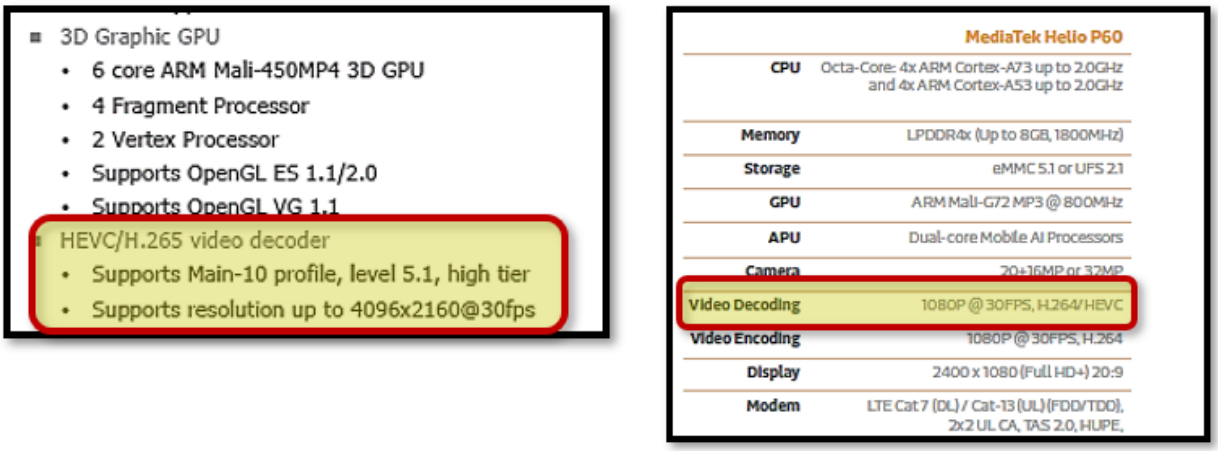
607. The MStar Products include circuitry for receiving frame-based video data that is encoded in compliance with the H.265 standard. A 2015 presentation on the MStar 9S00-MSD6A918 shows the circuit board for one of the MStar Products that contain a decoder that conforms to the H.265 standard. *See* Jack Cheng, SMART DISPLAY PRESENTATION ON MSD6A918 at 5 (2015) (describing that the MSD6A918 Product contains a decoder compliant with the H.265 standard). Datasheets from MediaTek also establish that the accused MStar Products comply with the H.265 standard. The below excerpt from the MSD6180 SOC Datasheet states: "all in one 的 SOC 芯片，芯片主要功能规格参数如下: 支持AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 等主流格式解码，分辨率最大支持到1 080P@60"[47]



MSD6180 SOC DATASHEET at 1 (2016) (annotation added) (showing that the MStar MSD6180 product contains a H.265 compliant decoder).

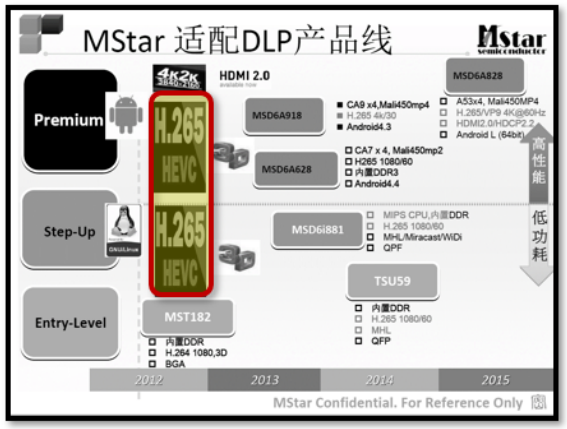
608. Similarly, the MediaTek datasheets for the MSO9280MC and Helio P60 products identifies that they contain an HEVC H.265 decoder.

[47] *Translated Text* "All in one SOC chip, the main functional specifications of the chip are as follows: Supports AVS+/H264/RMVB/MPEG l/MPEG2/MPEG4NC l/DIVX/H265 and other mainstream formats for decoding with maximum resolution Support to 1 080P@60."



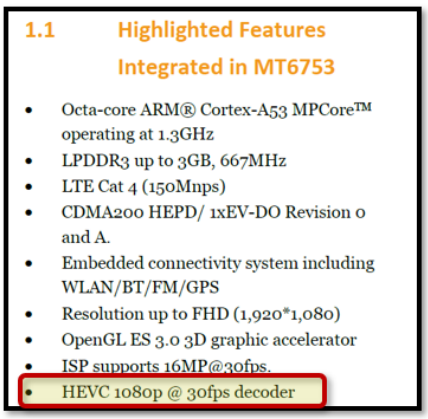
MSO9280MC Smart Set-Top Box Controller For IP/DRM Application, MSTAR PRODUCT BRIEF VERSION 3.0 at 1 (August 4, 2015) (annotation added); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 at 2 (2018) (annotation added).

609. A MediaTek presentation regarding its upcoming product release identifies that H.265 decoding functionality is incorporated into the accused MStar Products.



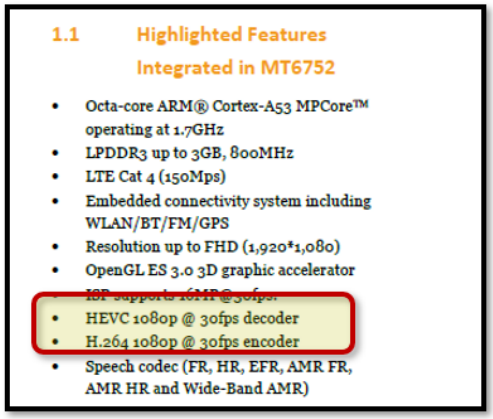
MSTAR PRESENTATION TITLED "DLP无屏显示新市场及竞争优势" at 11 (December 18, 2014) (annotation added) (showing that H.265 decoding functionality is incorporated into the accused MStar Products).

610. Technical briefs from MediaTek similarly identify the accused MediaTek products as containing a decoder that complies with the HEVC standard. For example, the MT6753 and MT6752 Application Processors contains a video decoder that complies with the HE VC standard.



1.1 Highlighted Features Integrated in MT6753

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.3GHz
- LPDDR3 up to 3GB, 667MHz
- LTE Cat 4 (150Mnps)
- CDMA200 HEPD/ 1xEV-DO Revision 0 and A.
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder

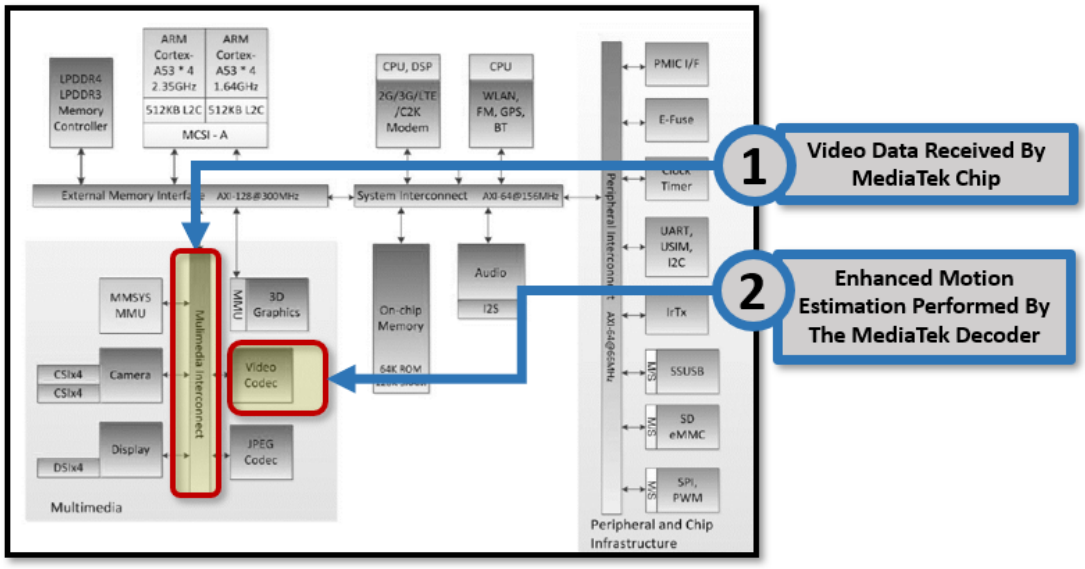


1.1 Highlighted Features Integrated in MT6752

- Octa-core ARM® Cortex-A53 MPCore™ operating at 1.7GHz
- LPDDR3 up to 3GB, 800MHz
- LTE Cat 4 (150Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (November 27, 2014) ("The chip integrates Octa-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards."); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF at 6 (June 10, 2014) (annotation added) ("The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.").

611. MediaTek documentation shows the interconnects that connect the video decoding engine to the rest of the application processor. For example, MediaTek documentation for the MT6757 chip (i.e., the Helio P20 chip) shows connections to the video codec engine.



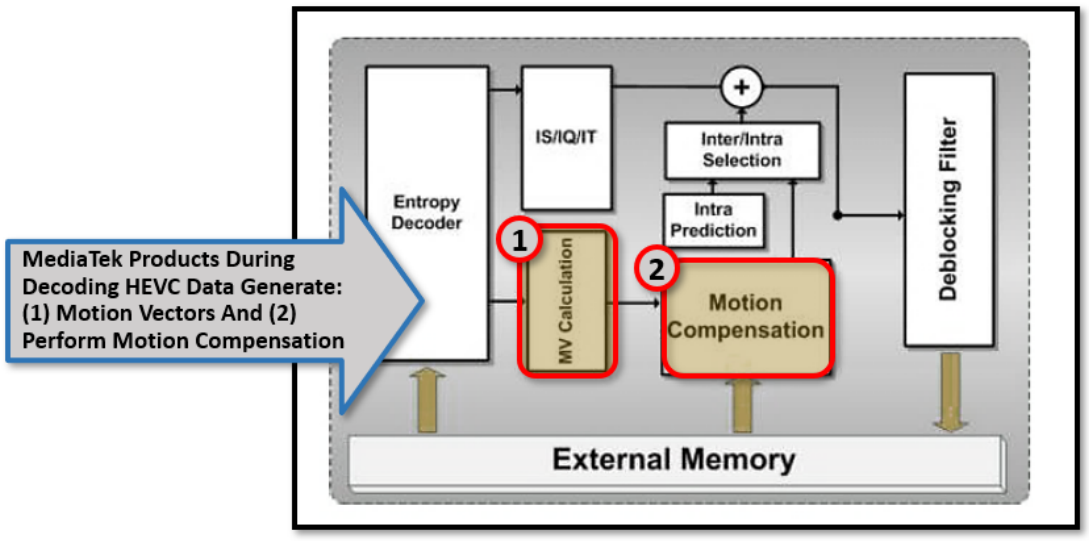
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 18 (June 20, 2016) (annotations added).

612. MediaTek technical documentation establishes the accused products (e.g., the MT6757 application processor) include an HEVC compliant decoder.

> All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

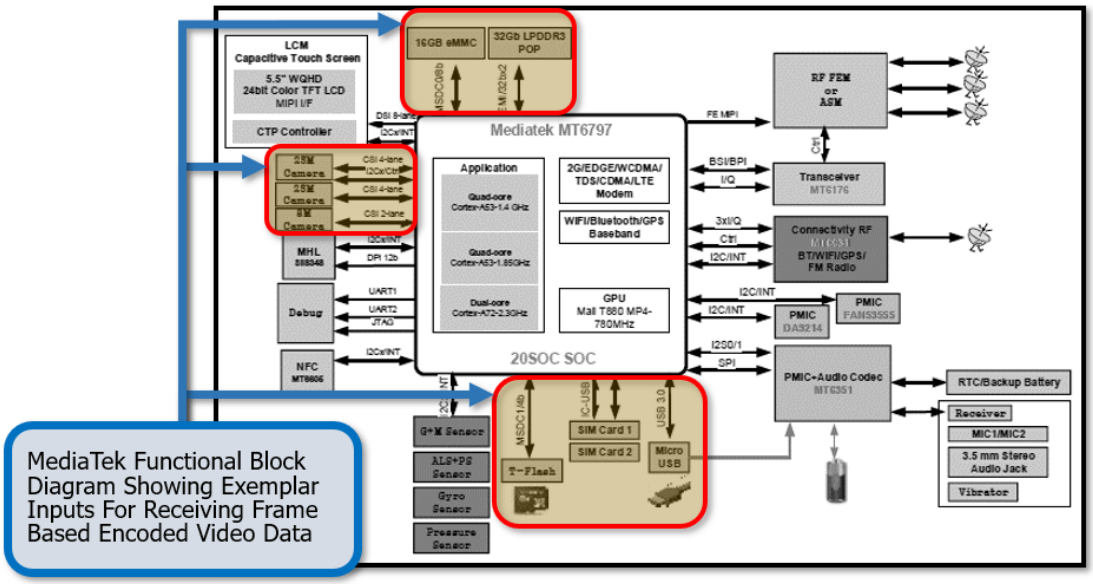
MT6757 LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 at 7 (June 20, 2016) (emphasis added) (describing that the MediaTek product includes a decoder for "HEVC 4K @ 30fps").

613. The architecture and core blocks of HEVC decoder ("VDEC") are shown in the below diagram including the following functional components: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra prediction, Motion Compensation, and De-Blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video is sent to the display stage.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 276 (July 19, 2016) (annotations added)

614. The accused MediaTek '105 Products receive HEVC encoded data through a variety of inputs. The below excerpt from MediaTek's technical documentation identifies the inputs for receiving HEVC encoded video data as part of the decoding process.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 12 (July 19, 2016) (annotations added) (showing a high-level functional block diagram of the MT6797 product).

615. MediaTek documentation states that the MediaTek '105 Products are compliant with the HEVC standard as shown in the above excerpted MediaTek documents.

616. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '105 Products in regular business operations.

617. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '105 Products – necessarily infringe the '105 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '105 patent, including but not limited to claim 1 of the '105 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '105 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking

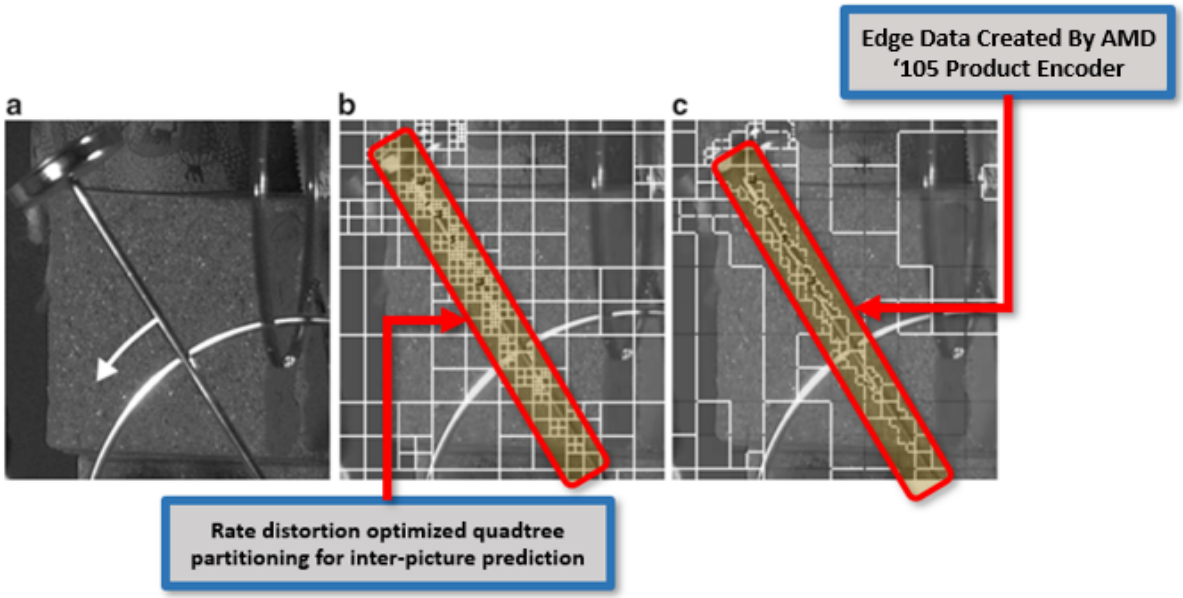
filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

618. The MediaTek '105 Products comply with the HEVC standard, which requires processing edge data from edge-adaptive interpolation processing.

619. The MediaTek '105 Products use two types of prediction methods for processing pixel information when encoding and decoding video data in HEVC format: inter prediction and intra prediction. Inter prediction utilizes motion vectors for block-based inter prediction to exploit temporal statistical dependencies between different pictures. Intra prediction uses various spatial prediction modes to exploit spatial statistical dependencies in the source signal for a single picture. The HEVC Specification (*e.g., High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) sets forth the standard that is followed by HEVC compliant devices such as the MediaTek '105 Products, and is relevant to both decoding and encoding that are performed pursuant to the HEVC standard. For instance, the MediaTek '105 Products perform a method for encoding a video signal comprised of pixels using motion vectors when performing encoding of H.265/HEVC video data.

620. During the encoding process, the MediaTek '105 products process pixel information based on edge data. The edge data is generated by the MediaTek '105 products using merge mode estimation. Specifically, the MediaTek '105 Products generate merge estimation regions which identify edge information within a video frame. The merge estimation regions are comprised of prediction units ("PU") that contain luma values. For example, in the below diagram PUs are shown. The encoding process then identifies along the edges of each prediction unit a

merge estimation region ("MER"). The MER regions thus identify the edges and the PU contains the intensity estimate for the pixels.



Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (annotations added).

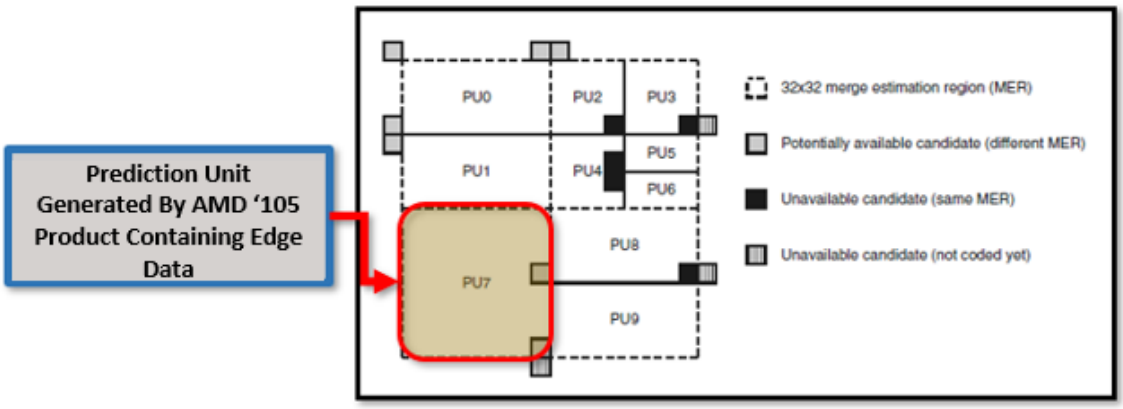
621. The MediaTek '105 Products in the process of encoding video content in HEVC format generate merge estimation regions generate edge data that include luma location and luma values which include a first intensity estimate. The HEVC standards describes this process as leading to the generation of luma motion vector mvL0 and mvL1.

> [T]he derivation process for luma motion vectors for merge mode as specified in clause I.8.5.3.2.7 is invoked with the luma location (xCb, yCb), the luma location (xPb, yPb), the variables nCbS, nPbW, nPbH, and the partition index partIdx as inputs, and the output being the luma motion vectors mvL0, mvL1, the reference indices refIdxL0, refIdxL1, the prediction list utilization flags predFlagL0 and predFlagL1, the flag ivMcFlag, the flag vspMcFlag, and the flag subPbMotionFlag.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.2.1 (February 2018) (emphasis added).

622. The MediaTek '105 Products perform the step of processing edge data from an edge adaptive interpolation process wherein the edge data includes a first intensity estimate of the pixel.

Specifically, the MediaTek '105 Products implement HEVC encoding which utilizes Parallel Merge Mode and Merge Estimation Regions (MER's) within the interpolation process to determine pixel edges. Parallel Merge Mode Estimation identifies the edge data within a prediction unit. The below diagram shows how video data is portioned into 10 prediction units and edge data is calculated and passed to the encoder.



Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 127 (September 2014) (annotations added).

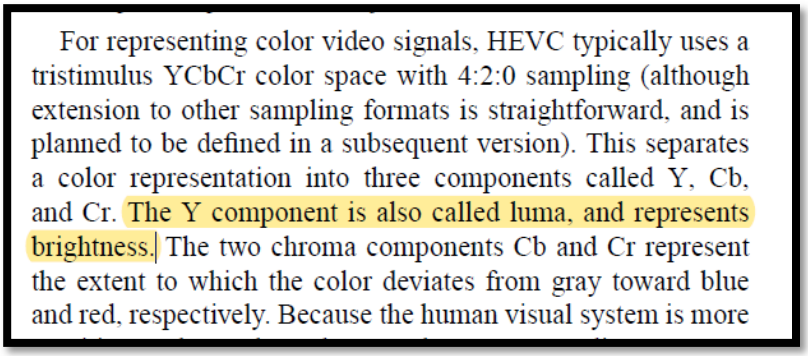
623. The merge estimation processes implemented by the MediaTek '105 Products is "adaptive." The below excerpt from documentation regarding the HEVC encoding process describes that the "merge estimation level is adaptive."

> In order to enable an encoder to trade-off parallelism and coding efficiency, the parallel merge estimation level is adaptive and signaled as `log2_parallel_merge_level_minus2` in the picture parameter set. The following MER sizes are allowed: 4×4 (no parallel merge estimation possible), 8×8, 16×16, 32×32 and 64×64. A higher degree of parallelization, enabled by a larger MER, excludes more potential candidates from the merge candidate list.

Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 128 (September 2014) (emphasis added).

624. The edge data that is processed from the edge adaptive interpolation process includes intensity estimates for pixels such as pixels in the merge estimation region. The intensity

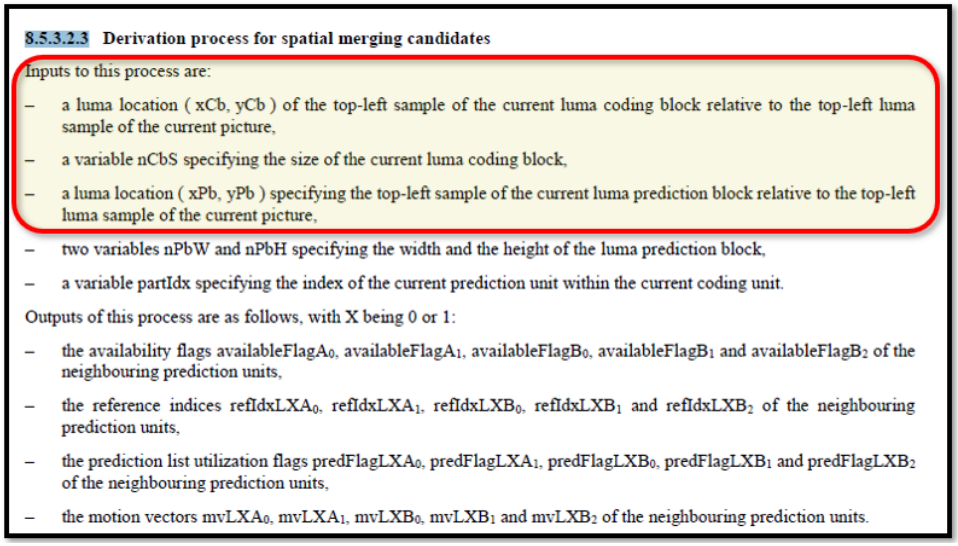
estimate or brightness estimate is referred to as "luma" in the encoding functionality implemented by the MediaTek '105 Products.



For representing color video signals, HEVC typically uses a tristimulus YCbCr color space with 4:2:0 sampling (although extension to other sampling formats is straightforward, and is planned to be defined in a subsequent version). This separates a color representation into three components called Y, Cb, and Cr. The Y component is also called luma, and represents brightness. The two chroma components Cb and Cr represent the extent to which the color deviates from gray toward blue and red, respectively. Because the human visual system is more

Gary J. Sullivan, Jens-Rainer Ohm, Woo-Jin Han, and Thomas Wiegand, Fellow, IEEE, *Overview of the High Efficiency Video Coding (HEVC) Standard*, published in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, Vol. 22, No. 12 at 1654 (December 2012) (emphasis added).

625. The motion estimation region ("MER") is an adaptive interpolation process in which the edges of images are calculated and include the intensity estimates of pixels by way of a luma value. The below excerpt from the HEVC specification describes how during the generation of merge estimation regions edge data includes luminosity values (intensity estimates) for pixels within a region.



8.5.3.2.3 Derivation process for spatial merging candidates

Inputs to this process are:

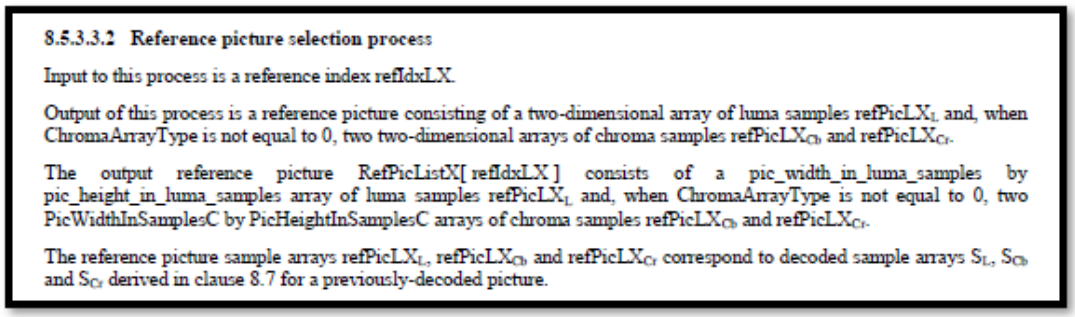
- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

Outputs of this process are as follows, with X being 0 or 1:

- the availability flags availableFlagA$_0$, availableFlagA$_1$, availableFlagB$_0$, availableFlagB$_1$ and availableFlagB$_2$ of the neighbouring prediction units,
- the reference indices refIdxLXA$_0$, refIdxLXA$_1$, refIdxLXB$_0$, refIdxLXB$_1$ and refIdxLXB$_2$ of the neighbouring prediction units,
- the prediction list utilization flags predFlagLXA$_0$, predFlagLXA$_1$, predFlagLXB$_0$, predFlagLXB$_1$ and predFlagLXB$_2$ of the neighbouring prediction units,
- the motion vectors mvLXA$_0$, mvLXA$_1$, mvLXB$_0$, mvLXB$_1$ and mvLXB$_2$ of the neighbouring prediction units.

High Efficiency Video Coding, Series H: Audiovisual And Multimedia Systems: Infrastructure Of Audiovisual Services – Coding Of Moving Video Rec. ITU-T H.265 at § I.8.5.2.3 (February 2018) (emphasis added).

626. The MediaTek '105 Products process motion data associated with motion compensation. The motion data processed by the MediaTek '105 Products include a first estimated motion vector of pixels within a reference frame prior to the current frame and a second estimated motion vector within the reference field after the current field. Specifically, the MediaTek '105 Products generate motion data in the form of a bi-directional prediction unit (PU) which has two motion vectors (referencing a prior frame and a subsequent frame in the sequence). The two motion vectors are combined to make a "bi-predictive merge candidate." One of the motion vectors is obtained from "reference picture list0" and the other motion vector is obtained from "reference picture list1."



8.5.3.3.2 Reference picture selection process

Input to this process is a reference index refIdxLX.

Output of this process is a reference picture consisting of a two-dimensional array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two two-dimensional arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The output reference picture RefPicListX[refIdxLX] consists of a pic_width_in_luma_samples by pic_height_in_luma_samples array of luma samples $refPicLX_L$ and, when ChromaArrayType is not equal to 0, two PicWidthInSamplesC by PicHeightInSamplesC arrays of chroma samples $refPicLX_{Cb}$ and $refPicLX_{Cr}$.

The reference picture sample arrays $refPicLX_L$, $refPicLX_{Cb}$ and $refPicLX_{Cr}$ correspond to decoded sample arrays S_L, S_{Cb} and S_{Cr} derived in clause 8.7 for a previously-decoded picture.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § I.8.5.3.3 (February 2018).

627. The reference pictures that are used to generate a motion vector comprise both the forward and prior reference pictures which are referred to in the HEVC encoding process implemented by the MediaTek '105 Products as "refPicLXcb" and "refPicLXcr." The following excerpt describing the implementation of the encoding process in the MediaTek '105 Products which use bi-predictive slices.

> Since a merge candidate comprises all motion data and the TMVP is only one motion vector, the derivation of the whole motion data only depends on the slice type. For bi-predictive slices, a TMVP is derived for each reference picture list. Depending on the availability of the TMVP for each list, the prediction type is set to bi-prediction or to the list for which the TMVP is available. All associated reference picture indices are set equal to zero. Consequently for uni-predictive slices, only the TMVP for list 0 is derived together with the reference picture index equal to zero.

Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added) (describing the use of bi-prediction in which motion data is derived from the forward and prior reference pictures in generating temporal arrays/vectors).

628. The MediaTek '105 Products' interpolation process contains bi-prediction functionality that computes a first estimated motion prediction and a second estimated motion prediction. The below excerpt from documentation of the encoding method used by the MediaTek '105 products describes that the encoding process includes functionality for generating a second intensity estimate for the pixel data and the edge data determined according to motion. In bi-prediction, the second estimate is defined as Δx_1, Δy_1, Δt_1.

In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014) (emphasis added).

629. In AMVP the system generates a temporal intermediate candidate based on bi-directional motion data. The "inter_pred_idc [x0] [y0] specifies whether list0, list1, or bi-prediction is used for the current prediction unit" according to the below referenced table. "The array indices x0, y0 specify the location (x0, y0) of the top-left luma sample of the considered prediction block relative to the top-left luma sample of the picture."

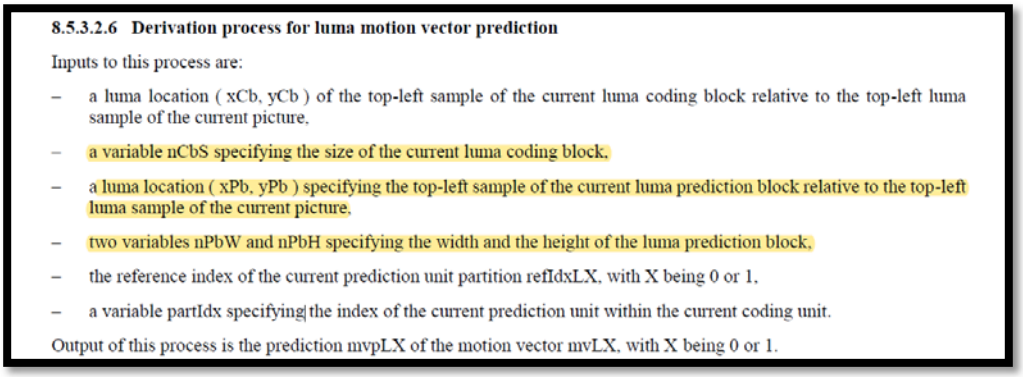
Table 7-11 – Name association to inter prediction mode

inter_pred_idc	Name of inter_pred_idc	
	(nPbW + nPbH) != 12	(nPbW + nPbH) == 12
0	PRED_L0	PRED_L0
1	PRED_L1	PRED_L1
2	PRED_BI	na

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 7.4.9.6 (February 2018).

630. The MediaTek '105 Products generate a second intensity estimate based on the edge data and the motion data. The edge data is combined with the temporal intermediate candidate to generate the temporal candidate. The prediction unit based on the first and second motion vector (motion data) is then combined with the edge data to generate a second intensity estimate. Once the reference picture for obtaining the co-located PU is selected then the position

of the co-located Pu will be selected among two candidate positions. A second intensity estimate is generated by using the bi-directional motion vectors and the edge data. The below excerpt from the HEVC specification describes that for a luma motion vector prediction the generation of a second intensity estimate is based on the motion data and the edge data. The edge data here is comprised by the luma location and luma prediction block information. Further, the luma motion vectors mvLO and mvL1 are combined with the edge data including luma location xCB yCB xBL and yBl to generate a second intensity estimate.



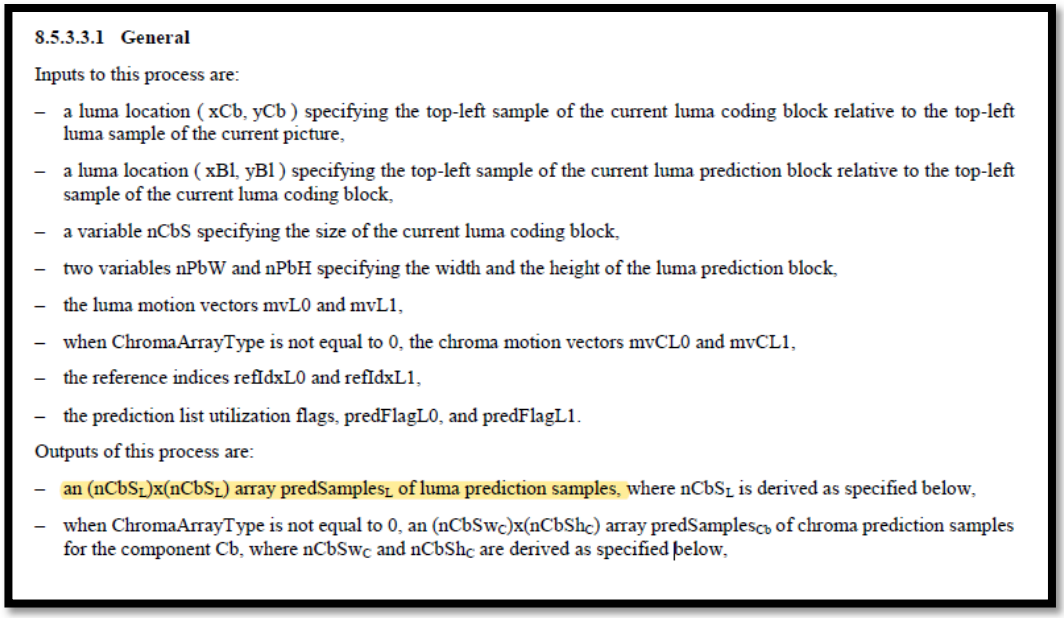
8.5.3.2.6 Derivation process for luma motion vector prediction

Inputs to this process are:

- a luma location (xCb, yCb) of the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a variable nCbS specifying the size of the current luma coding block,
- a luma location (xPb, yPb) specifying the top-left sample of the current luma prediction block relative to the top-left luma sample of the current picture,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the reference index of the current prediction unit partition refIdxLX, with X being 0 or 1,
- a variable partIdx specifying the index of the current prediction unit within the current coding unit.

Output of this process is the prediction mvpLX of the motion vector mvLX, with X being 0 or 1.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.2.6 (February 2018) (emphasis added).



8.5.3.3.1 General

Inputs to this process are:

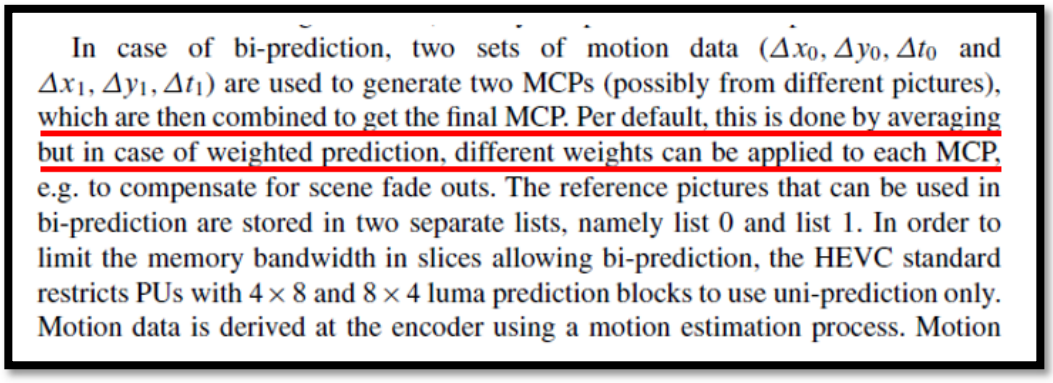
- a luma location (xCb, yCb) specifying the top-left sample of the current luma coding block relative to the top-left luma sample of the current picture,
- a luma location (xBl, yBl) specifying the top-left sample of the current luma prediction block relative to the top-left sample of the current luma coding block,
- a variable nCbS specifying the size of the current luma coding block,
- two variables nPbW and nPbH specifying the width and the height of the luma prediction block,
- the luma motion vectors mvL0 and mvL1,
- when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1,
- the reference indices refIdxL0 and refIdxL1,
- the prediction list utilization flags, predFlagL0, and predFlagL1.

Outputs of this process are:

- an ($nCbS_L$)x($nCbS_L$) array $predSamples_L$ of luma prediction samples, where $nCbS_L$ is derived as specified below,
- when ChromaArrayType is not equal to 0, an ($nCbSw_C$)x($nCbSh_C$) array $predSamples_{Cb}$ of chroma prediction samples for the component Cb, where $nCbSw_C$ and $nCbSh_C$ are derived as specified below,

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.1 (February 2018) (emphasis added).

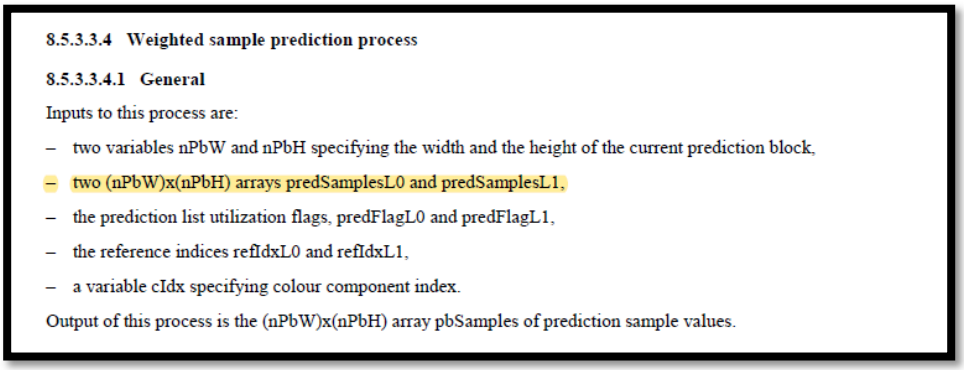
631. The MediaTek '105 Products perform a mixing process in which the final edge/motion data of a pixel is calculated based on a first intensity estimate, second intensity estimate, and motion reliability data. Specifically, the MediaTek '105 Products encode pixel data using bi-prediction wherein use two types of mixing functions: average mixing and weighted mixing.



In case of bi-prediction, two sets of motion data ($\Delta x_0, \Delta y_0, \Delta t_0$ and $\Delta x_1, \Delta y_1, \Delta t_1$) are used to generate two MCPs (possibly from different pictures), which are then combined to get the final MCP. Per default, this is done by averaging but in case of weighted prediction, different weights can be applied to each MCP, e.g. to compensate for scene fade outs. The reference pictures that can be used in bi-prediction are stored in two separate lists, namely list 0 and list 1. In order to limit the memory bandwidth in slices allowing bi-prediction, the HEVC standard restricts PUs with 4×8 and 8×4 luma prediction blocks to use uni-prediction only. Motion data is derived at the encoder using a motion estimation process. Motion

Benjamin Bross, et al., *Inter-Picture Prediction in HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 123 (September 2014) (emphasis added).

632. The HEVC standard includes functionality to perform a mixing process. In MERGE mode, an up-to five-entry MERGE candidate list is first constructed with four (MV, Refldx) pairs from spatial neighbor blocks and one (MV, Refldx) pair from temporal bottom-right or collocated neighbor block, where Refldx is the index of the reference picture that the MV pointed to. After that, the encoder decides to use which candidate (MV, Refldx) pair to encode current block and then encode the candidate index into bitstream. In MERGE mode, the selected (MV, Refldx) pair is directly used to encode current block, and no MVD information needs to be coded. The number of merge candidates could be configured at encoder, with up to five merge candidates."



8.5.3.3.4 Weighted sample prediction process

8.5.3.3.4.1 General

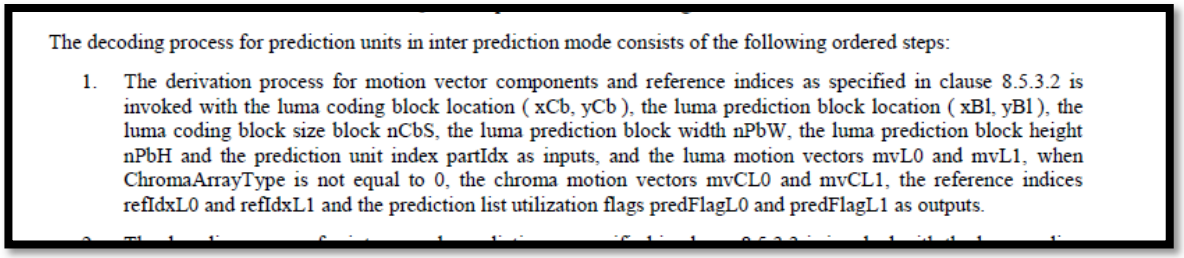
Inputs to this process are:

- two variables nPbW and nPbH specifying the width and the height of the current prediction block,
- two (nPbW)x(nPbH) arrays predSamplesL0 and predSamplesL1,
- the prediction list utilization flags, predFlagL0 and predFlagL1,
- the reference indices refIdxL0 and refIdxL1,
- a variable cIdx specifying colour component index.

Output of this process is the (nPbW)x(nPbH) array pbSamples of prediction sample values.

HIGH EFFICIENCY VIDEO CODING, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.3.4.1 (February 2018) (emphasis added).

633. The variables predFlagL0 and predFlagL1 are reliability values that are generated by the decoding process. The predFlagL0 and L1 values are prediction utilization values that are used to generate prediction utilization and reliability of the vectors.



The decoding process for prediction units in inter prediction mode consists of the following ordered steps:

1. The derivation process for motion vector components and reference indices as specified in clause 8.5.3.2 is invoked with the luma coding block location (xCb, yCb), the luma prediction block location (xBl, yBl), the luma coding block size block nCbS, the luma prediction block width nPbW, the luma prediction block height nPbH and the prediction unit index partIdx as inputs, and the luma motion vectors mvL0 and mvL1, when ChromaArrayType is not equal to 0, the chroma motion vectors mvCL0 and mvCL1, the reference indices refIdxL0 and refIdxL1 and the prediction list utilization flags predFlagL0 and predFlagL1 as outputs.

High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at § 8.5.3.1 (February 2018).

634. Any implementation of the HEVC standard would infringe the '105 patent as every possible implementation of the standard requires: processing edge data from edge-adaptive interpolation processing, including a first intensity estimate for the pixel as well as data pertaining to one or more pixels that neighbor the pixel; processing motion data associated with motion compensation processing, wherein the motion data includes a first estimated motion vector for a pixel in a reference field prior to the present field and a second estimated motion vector for a pixel in a reference field subsequent to the present field; determining a second intensity estimate for the pixel as a function of the edge data and the motion data; and performing a blending process wherein final edge/motion data of the pixel is calculated as a function of the first intensity estimate, the second intensity estimate, and motion reliability data characterizing reliability of the motion data.

635. The MediaTek '105 Products are available to businesses and individuals throughout the United States.

636. The MediaTek '105 Products are provided to businesses and individuals located in the State of Delaware.

637. By making, using, testing, offering for sale, and/or selling products and services for enhancing subsequent images of a video stream in which frames are encoded based on previous frames using prediction and motion estimation, including but not limited to the MediaTek '105

Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '105 patent, including at least claim 1 pursuant to 35 U.S.C. § 271(a).

638. MediaTek also indirectly infringes the '105 patent by actively inducing infringement under 35 U.S.C. § 271(b).

639. MediaTek has had knowledge of the '105 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '105 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '105 Patent based on prior communications that identified the '105 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

640. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '105 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '105 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '105 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '105 Products that have the capability of operating in a manner that infringe one or more of the claims of the '105 patent, including at least claim 1, and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '105 Products to utilize the products in a manner that directly infringe one or more claims of the '105 patent.[48] By providing instruction and training to customers and end-

[48] *See, e.g.*, *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); MT6757

users on how to use the MediaTek '105 Products in a manner that directly infringes one or more claims of the '105 patent, including at least claim 1, MediaTek specifically intended to induce infringement of the '105 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '105 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '105 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '105 patent, knowing that such use constitutes infringement of the '105 patent.

641. The '105 patent is well-known within the industry as demonstrated by multiple citations to the '105 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '105 patent without paying a reasonable royalty. MediaTek is infringing the '105 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

642. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '105 patent.

643. As a result of MediaTek's infringement of the '105 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

LTE-A SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF VERSION 1.3 (June 20, 2016); MEDIATEK MT6753 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (November 27, 2014); MEDIATEK MT6752 LTE SMARTPHONE APPLICATION PROCESSOR TECHNICAL BRIEF (June 10, 2014); MEDIATEK HELIO P60, MEDIATEK DATASHEET NO. PDFHP60PB A4 0218 (2018); *MSO9280MC Smart Set-Top Box Controller For IP/DRM Application*, MSTAR PRODUCT BRIEF VERSION 3.0 (August 4, 2015); and MSD6180 SOC DATASHEET (2016).

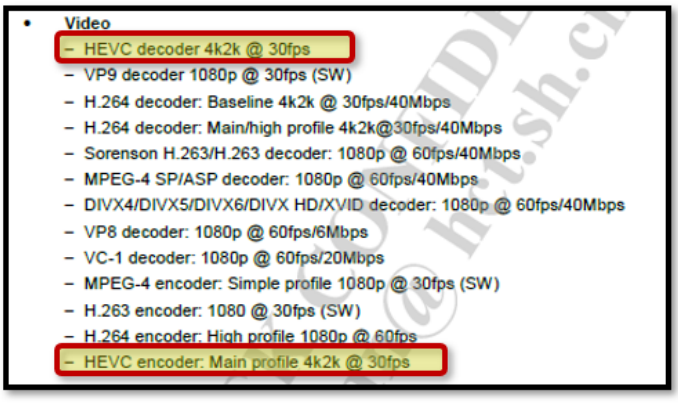
COUNT XIII
INFRINGEMENT OF U.S. PATENT NO. 8,311,112

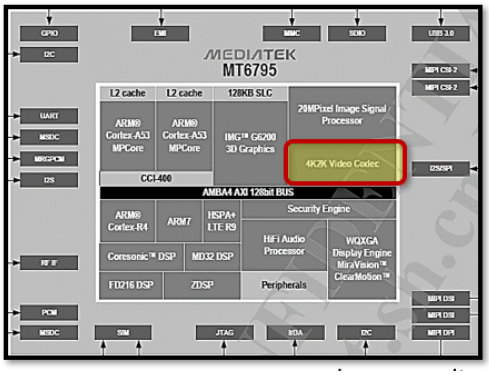
644. Dynamic Data references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

645. MediaTek designs, makes, uses, sells, and/or offers for sale in the United States products and/or services for video compression.

646. MediaTek designs, makes, sells, offers to sell, imports, and/or uses MediaTek products that comply with the H.265 standard, including but not limited to the following MediaTek Products that perform encoding pursuant to the H.265 standard: MediaTek Helio P30, MediaTek Helio X10, MediaTek Helio X20, MediaTek Helio X23, MediaTek Helio X25, MediaTek Helio X27, MediaTek Helio X30, MediaTek MT6592, MediaTek MT6595, and MediaTek MT8176 (collectively, the "MediaTek '112 Product(s)").

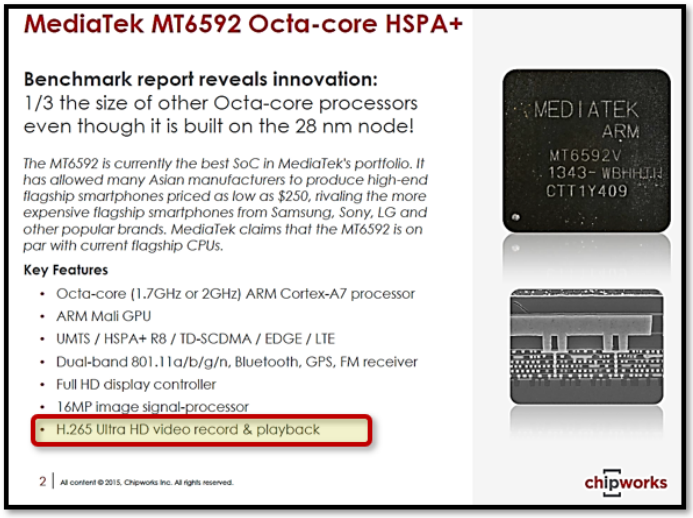
647. Documentation from MediaTek establishes that the accused devices contain an HEVC Decoder and HEVC Encoder. For example, the MT6795 Octa-Core Smartphone Application Processor Technical Brief identifies the product as containing both an HEVC encoder and decoder as shown in the below excerpt.





MT6795 Octa-Core Smartphone Application Processor Technical Brief, MEDIA TEK DOCUMENTATION 0.1 at 10 & 12 (August 27, 2014) (annotations added).

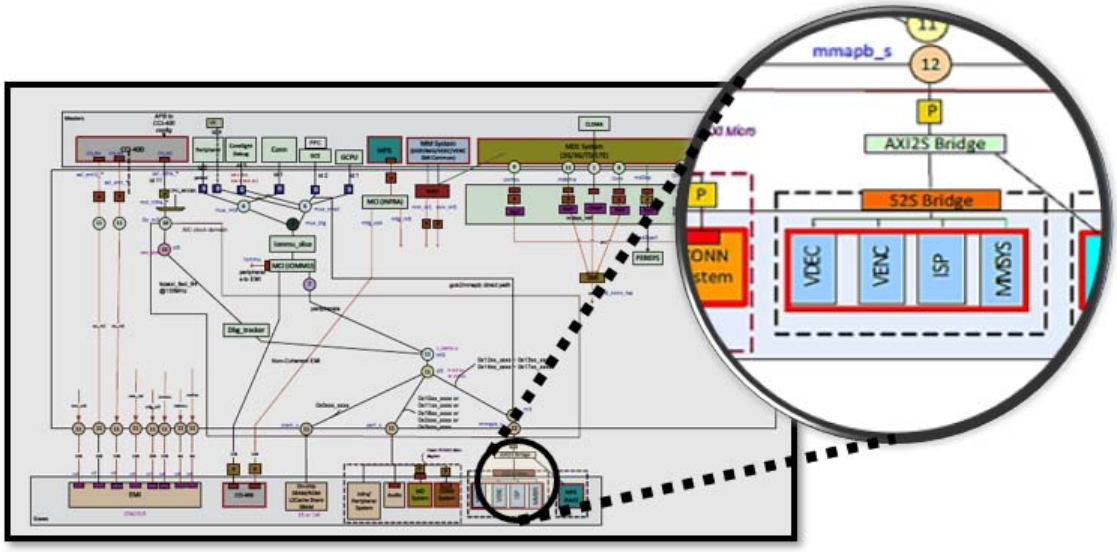
648. Analysis of the accused MediaTek '112 Products from ChipWorks identifies one of the key features in the MediaTek MT6592 Octa-Core Processor is "H.265 Ultra HD video record & Playback."



CHIPWORKS PRODUCT BRIEF: MEDIATEK MT6592 OCTA-CORE HSPA+ PLATFORM at 2 (February 2015) (annotation added).

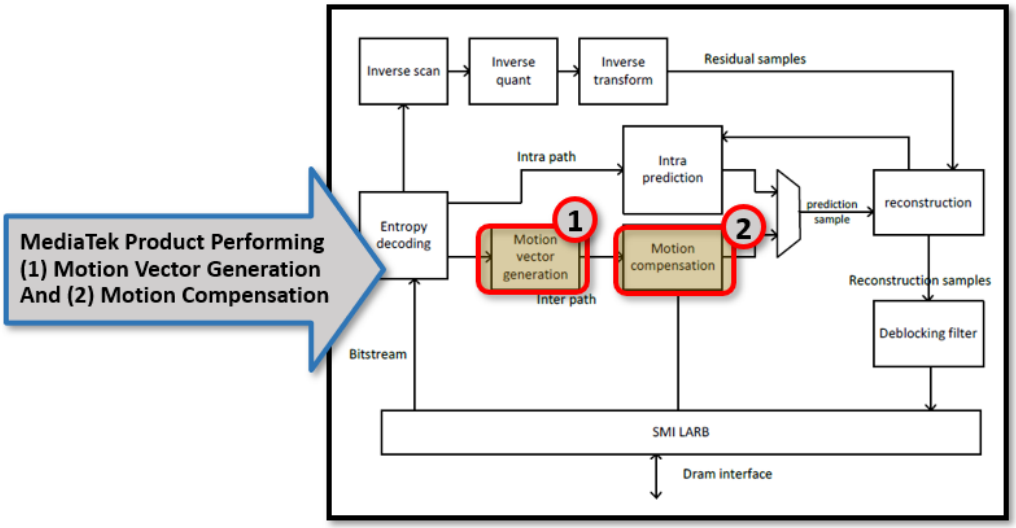
649. MediaTek documentation for the MT6592 Octa-Core Processor shows that the chip's multimedia system contains a video encoding function. *See MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION at 11 (July 6, 2013) (showing that the Video Codec for HEVC decoding is part of the chip's multimedia system).

650. MediaTek documentation also establishes the accused MediaTek '112 Products (e.g., MT6592) contains a graphics processing unit that supports HEVC encoding and decoding. *See MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592 (last visited February 2019). MediaTek documentation also establishes that the accused MediaTek '112 Products (*e.g.*, MT6797) contain a video decoder ("VDEC") and video encoder ("VENC") that is connected via the S25 and AXI2S bridge.



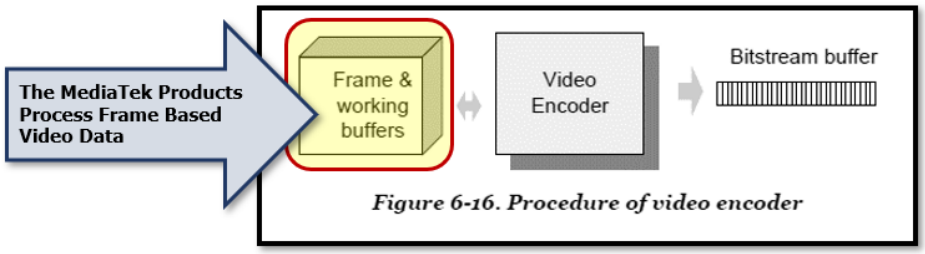
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 138 (July 19, 2016) (annotations added) (showing the AXI Fabric and Control Blocks and specifically identifying the VDEC (video decoder) and VENC (video encoder) that is connected via the S25 Bridge and AXI2S Bridge. The MT6797 chip is also referred to as the Helio X20 chip.).

651. MediaTek documentation describes the encoding process used by the accused MediaTek '112 Products. For example, the below process diagram from MediaTek shows the MediaTek '112 Products perform motion vector generation and motion compensation as part of the HEVC encoding of video data.



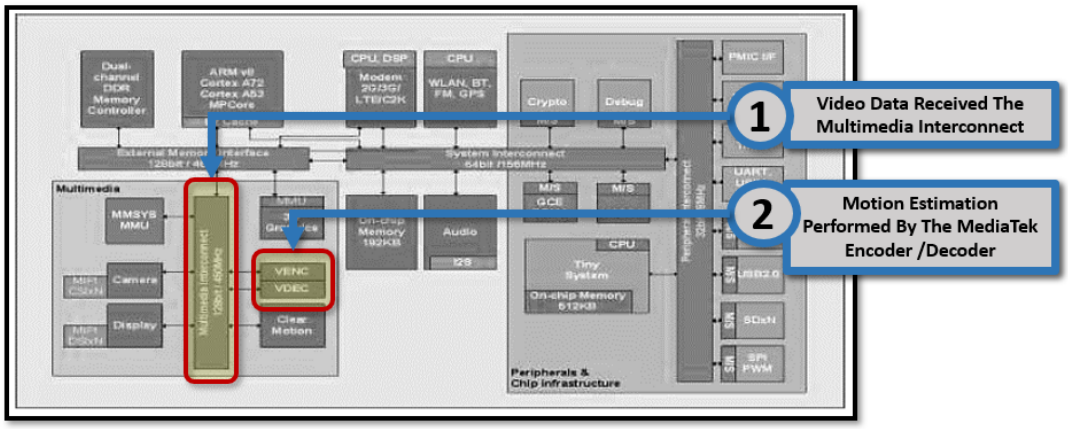
MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 278 (July 19, 2016) (annotations added).

652. The video encoder in the accused MediaTek '112 Products "takes DRAM as input, output, and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to output buffer. The driver software maintains all buffers and assign proper value to video encoder to allow hardware to work correctly." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016). This process is shown in the below diagram excerpted from MediaTek's documentation.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (annotation added).

653. MediaTek documentation shows the H.265 compliant VENC and VDEC receive video data via the multimedia interconnect and perform motion estimation on the received video data.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 23 (July 19, 2016) (annotations added) (showing the bus structure of the MediaTek MT6797 Product).

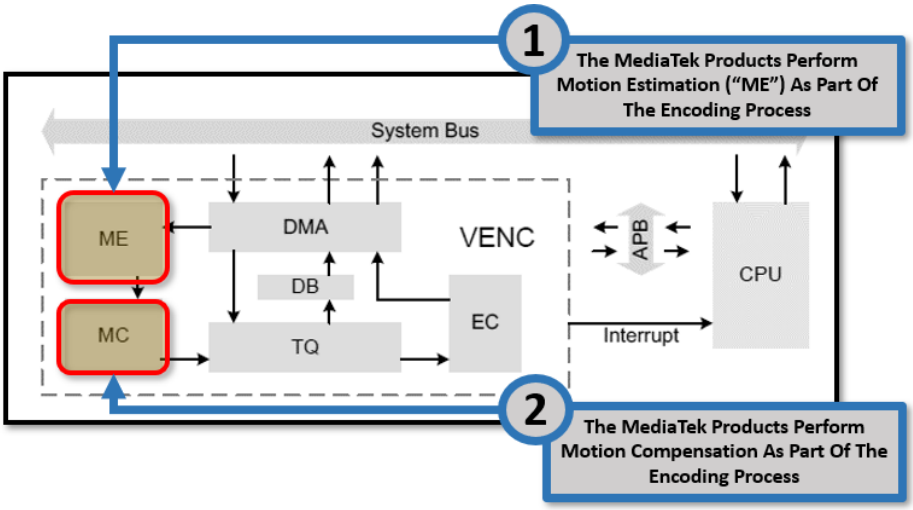
654. The MediaTek '112 Products conduct motion estimation as part of the video encoding process where motion estimation is used to decide motion vectors for later encoding. The MediaTek '112 Product conduct motion compensation as part of the video encoding process to give predicted pixel values. This process is described in the following excerpt from MediaTek's documentation.

> The video encoder is configured by software through APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME conducts motion estimation to decide motion vector for later encoding. MC conducts motion compensation to give predicted pixel values. TQ conducts transform and quantization operation and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB conducts de-blocking operation and allows DMA to store back the processed frame as the next frame's reference frame. EC conducts entropy encoding, and the coding can be variable length code, context based arithmetic code, or context based variable length code. The encoded bitstream will be written to memory by DMA.

MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284—85 (July 19, 2016) (emphasis added).

655. The accused MediaTek '112 Products contain an HEVC encoder and decoder. MediaTek documentation states that "[t]his design is main stream video encoder consisting of two video encoders: H.264, and HEVC. It is capable of encoding 1080P video at 60 frames per second (FPS) with promising superior video quality for H.264 and up to 2160P video at 30 FPS for HEVC. This IP supports various encoding methods that satisfy basic requirement of easy software controllability." MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 284 (July 19, 2016) (emphasis added).

656. The below excerpt from MediaTek documentation shows that as part of the HEVC encoding process performed by the MediaTek Video Encoder ("VENC") motion estimation and motion compensation are performed.



MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD at 285 (July 19, 2016) (annotations added).

657. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '112 Products in regular business operations.

658. The MediaTek '112 Products select the selected image selection area based on a range of possible motion vectors in the selected image search area. Further, the search area of the selected image segment has a center. Specifically, the MediaTek '112 Products contain functionality for selecting a coding unit. The coding unit comprises a selected image segment.

659. The H.265/HEVC encoding performed by the MediaTek '112 Products enables the selection of an image segment of a given image corresponding to an image segment of a first video image. The selected image segment has a center and a search area is defined around the image segment.

660. The MediaTek '112 Products contain an image processing unit that receives, at a minimum, two frames of a video from memory. These frames are then processed by the video compensation unit of the MediaTek Products. Further, the MediaTek Products contain an encoder for motion estimation. "[T]he encoder needs to perform motion estimation, which is one of the

most computationally expensive operations in the encoder, and complexity is reduced by allowing less candidates."[49]

661. The MediaTek '112 Products perform encoding using motion compensation, specifically, inter-picture prediction wherein the MediaTek Product makes use of the temporal correlation between pictures in order to derive a motion-compensated prediction for a block of image samples. Each image is divided into blocks (prediction units) and the MediaTek '112 Product compares the prediction unit in a first image with the spatially neighboring prediction units in a second image (reference image). The displacement between the current prediction unit and the matching prediction unit in the second image (reference image) is signaled using a motion vector.

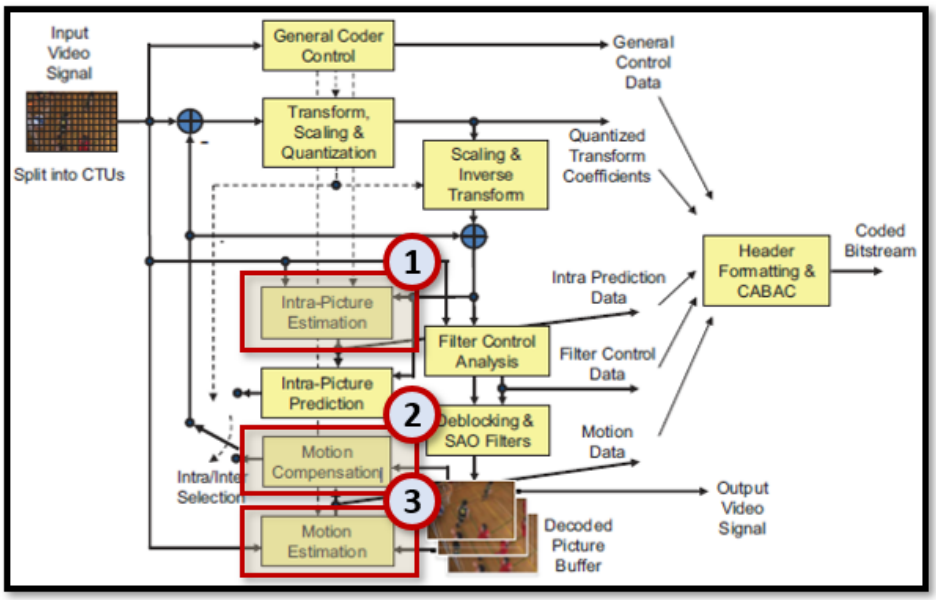
662. The MediaTek '112 Products contain functionality wherein during the motion estimation process the block size used for prediction units can range from 4 × 8/8 × 4 to 64 × 64.

> A block-wise prediction residual is computed from corresponding regions of previously decoded pictures (inter-picture motion compensated prediction) or neighboring previously decoded samples from the same picture (intra-picture spatial prediction). The residual is then processed by a block transform, and the transform coefficients are quantized and entropy coded. Side information data such as motion vectors and mode switching parameters are also encoded and transmitted.

Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, Vol. 7, No. 6 at 1002 (December 2013) (emphasis added).

663. The MediaTek '112 Products use intra-picture estimation between blocks (prediction units) within an image retrieved from memory. The frames are then processed using both motion compensation and motion estimation. The motion compensation functionality used by the MediaTek Products include quarter-sample precision for the motion vectors and 7-tap or 8-tap filters that are used for interpolation of fractional-sample positions.

[49] Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, PRE-PUBLICATION DRAFT, TO APPEAR IN IEEE TRANS. ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY at 13 (December 2012) (emphasis added).



Standardized Extensions of High Efficiency Video Coding (HEVC), IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, VOL. 7, NO. 6 at 1002 (December 2013) (emphasis added) (the annotations showing (1) intra-picture prediction, (2) motion compensation, and (3) motion estimation).

664. The MediaTek '112 Products contain functionality for motion compensation where two or more motion vectors can be applied. Further, one or two motion vectors can be applied to the image processing process. The application of the motion vectors leads to uni-predictive or bi-predictive coding, respectively, where bi-predictive coding uses an averaged result of two predictions to form the final prediction.

Summary

Recommendation ITU-T H.265 | International Standard ISO/IEC 23008-2 represents an evolution of the existing video coding Recommendations (ITU-T H.261, ITU-T H.262, ITU-T H.263 and ITU-T H.264) and was developed in response to the growing need for higher compression of moving pictures for various applications such as Internet streaming, communication, videoconferencing, digital storage media and television broadcasting. It is also designed to enable the use of the coded video representation in a flexible manner for a wide variety of network environments. The use of this Recommendation | International Standard allows motion video to be manipulated as a form of computer data and to be stored on various storage media, transmitted and received over existing and future networks and distributed on existing and future broadcasting channels.

Series H: Audiovisual and Multimedia Systems- Infrastructure of Audiovisual Services – Coding of Moving Video, INTERNATIONAL TELECOMMUNICATIONS UNIONS - TU-T H.265, V.5 at I (February 2018).

665. The MediaTek '112 Products comprise a system wherein an intra-frame coding unit is configured to perform predictive coding on a set of pixels of a macroblock of pixels. Further,

the predictive coding functionality uses a first group of reference pixels and a macroblock of pixels from the video frame. Specifically, the MediaTek Products, when selecting a temporal candidate for HEVC intra-frame encoding, default to the right bottom position just outside of the collocated prediction unit.

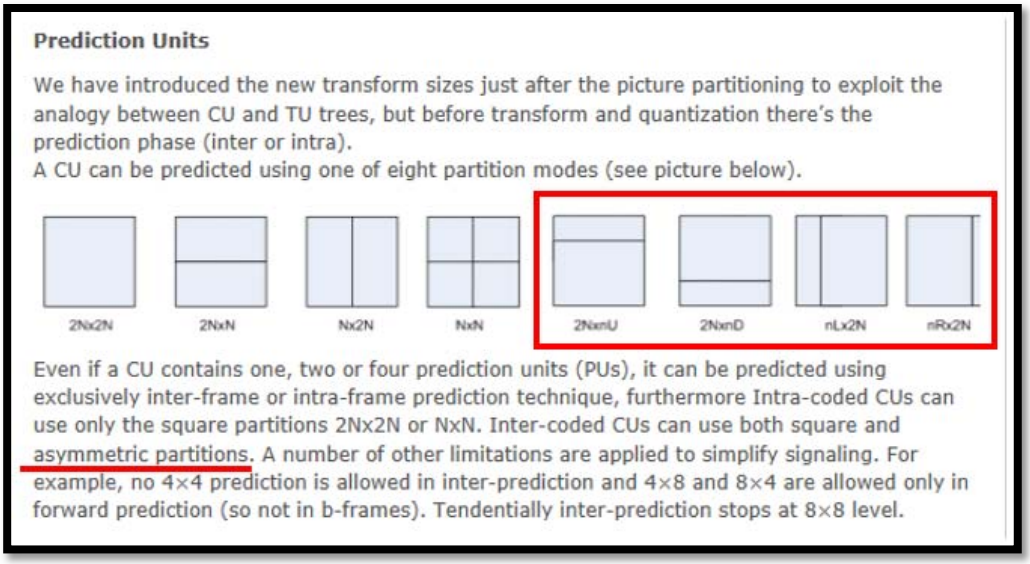
> It can be seen from Fig. 5.4b that only motion vectors from spatial neighboring blocks to the left and above the current block are considered as spatial MVP candidates. This can be explained by the fact that the blocks to the right and below the current block are not yet decoded and hence, their motion data is not available. Since the co-located picture is a reference picture which is already decoded, it is possible to also consider motion data from the block at the same position, from blocks to the right of the co-located block or from the blocks below**.** In HEVC, the block to the bottom right and at the center of the current block have been determined to be the most suitable to provide a good temporal motion vector predictor (TMVP).

Benjamin Bross, *et al., Inter-picture prediction in HEVC,* in HIGH EFFICIENCY VIDEO CODING (HEVC) at 119 (2014) (emphasis added);

666. Descriptions of the HEVC encoding process, which are implemented by the MediaTek '112 Products, state "for the temporal candidate, the right bottom position just outside of the collocated PU of the reference picture is used if it is available. Otherwise, the center position is used instead." Gary J. Sullivan, *et al.*, *Overview of the High Efficiency Video Coding (HEVC) Standard*, IEEE TRANS. ON CIRCUIT AND SYSTEMS FOR VIDEO TECHNOLOGY at 13 (December 2012).

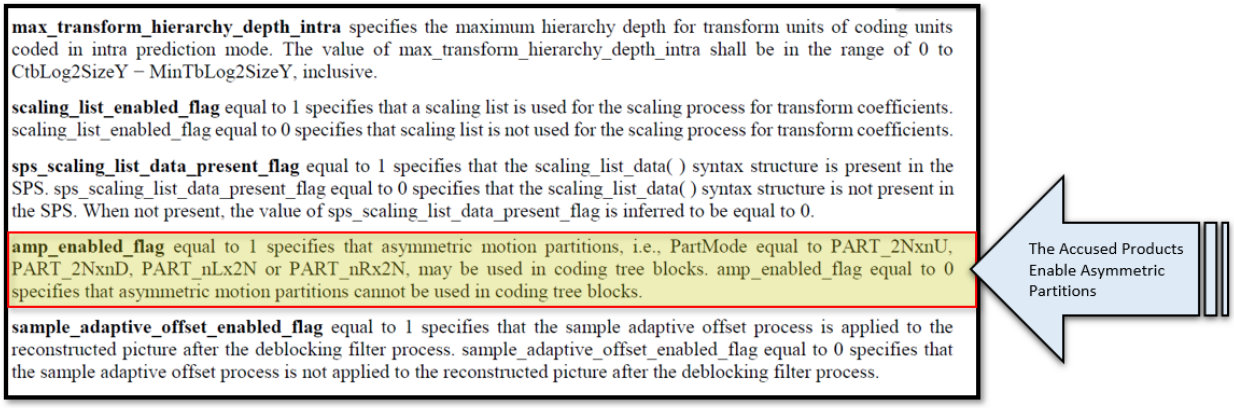
667. The MediaTek video encoder in the MediaTek '112 Products selects an image segment of a second video image corresponding to an image segment of a first video image. The image segment further has an image segment center.

668. The MediaTek '112 Products encode video data such that a predetermined search area (S) center is offset from the center of the image segment. The predetermined search area is called a partition and there are eight different partition modes in the H.265 standard, these partition modes are shown in the figure below. The last four partition modes are asymmetric, meaning their center is offset from the overall CU center.



Fabio Sonnati, *H265 – Part I: Technical Overview,* VIDEO ENCODING & STREAMING TECHNOLOGIES WEBSITE (June 20, 2014) (emphasis added).

669. The figure below shows the syntax as well as the instructions for enabling the asymmetric partitions within the H.265 standard, which is used by the MediaTek '112 Products.



High Efficiency Video Coding, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 at 76 (April 2015) (annotation added).

670. The MediaTek '112 Products receive encoded video data that is encoded using intra-frame coding. Specifically, the encoded video stream received by the MediaTek '112 Products is coded using a reference group of pixels in the video frame. Intra-frame prediction used in the encoded video data received by the MediaTek '112 Products allows a transform block to

span across multiple prediction blocks for intra-frame-picture predicted coding units to maximize the potential coding efficiency benefits of the quadtree-structured transform block partitioning.

> The basic source-coding algorithm is a hybrid of interpicture prediction to exploit temporal statistical dependences, intrapicture prediction to exploit spatial statistical dependences, and transform coding of the prediction residual signals to further exploit spatial statistical dependences.

G. J. Sullivan, J.-R. Ohm, W.-J. Han, and T. Wiegand, *Overview of the High Efficiency Video Coding (HEVC) standard*, IEEE TRANS. CIRCUITS SYST. VIDEO TECHNOL., vol. 22, no. 12, p. 1654 (December 2012) (emphasis added).

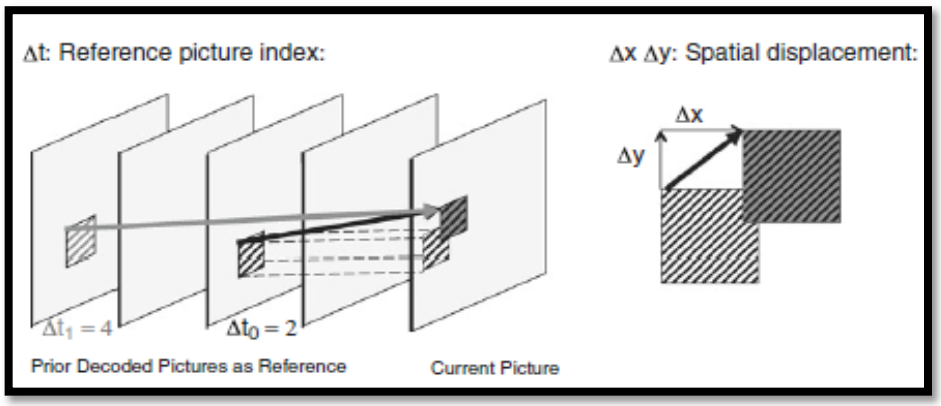
671. The MediaTek '112 Products comprise functionality for retrieving image motion data related to the search area. Specifically, the MediaTek '112 Products retrieve data relating to the motion search area. The data, which includes the motion vector index, is sent from the encoder and retrieved by the decoder.

> Since inter-picture prediction typically compensates for the motion of real-world objects between pictures of a video sequence, it is also referred to as motion-compensated prediction. While intra-picture prediction exploits the spatial redundancy between neighboring blocks inside a picture, motion-compensated prediction utilizes the large amount of temporal redundancy between pictures. In either case, the resulting prediction error, which is formed by taking the difference between the original block and its prediction, is transmitted using transform coding, which exploits the spatial redundancy inside a block and consists of a decorrelating linear transform, scalar quantization of the transform coefficients and entropy coding of the resulting transform coefficient levels.

Heiko Schwarz, Thomas Schierl, Detlev Marpe, *Block Structures and Parallelism Features in HEVC*, in HEVC, HIGH EFFICIENCY VIDEO CODING (HEVC) at 49 (September 2014) (emphasis added).

672. MediaTek '112 Products comprise an inter-frame coding unit that is configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels. The second group of reference pixels that are used to perform inter-frame coding are drawn from at least one other video frame. The image data processed by the MediaTek '112 Products is encoded using inter-picture prediction that makes use of the temporal correlation between pictures to derive a motion-compensated prediction (MCP) for a block of image samples. For this block-based motion compensated prediction, an image is divided into rectangular blocks. Assuming

homogeneous motion inside one block, and that moving objects are larger than one block, for each block, a corresponding block in a previously decoded picture can be found that serves as a predictor (a second image). Both the first and second images are retrieved by the MediaTek '112 Product from storage such as on chip memory. The general concept of inter-frame-based encoding using motion-compensated prediction based on a translational motion model is illustrated below.



Benjamin Bross, *Inter-Picture Prediction In HEVC*, HIGH EFFICIENCY VIDEO CODING (HEVC) at 114 (September 2014).

673. By complying with the HEVC standard, the MediaTek devices – such as the MediaTek '112 Products – necessarily infringe the '112 patent. The mandatory sections of the HEVC standard require the elements required by certain claims of the '112 patent, including but not limited to claim 11 of the '112 patent. *High Efficiency Video Coding*, SERIES H: AUDIOVISUAL AND MULTIMEDIA SYSTEMS: INFRASTRUCTURE OF AUDIOVISUAL SERVICES – CODING OF MOVING VIDEO REC. ITU-T H.265 (February 2018) (The following sections of the HEVC Standard are relevant to MediaTek's infringement of the '112 patent: "8.3.2 Decoding process for reference picture set;" "8.5.4 Decoding process for the residual signal of coding units coded in inter prediction mode;" "8.6 Scaling, transformation and array construction process prior to deblocking filter process;" "8.5.2 Inter prediction process;" "8.5.3 Decoding process for prediction units in

inter prediction mode;" and "8.7.2 Deblocking filter process;" "8.7.3 Sample adaptive offset process.").

674. One or more MediaTek subsidiaries and/or affiliates use the MediaTek '112 Products in regular business operations.

675. One or more of the MediaTek '112 Products include technology for video compression.

676. MediaTek has directly infringed and continues to directly infringe the '112 patent by, among other things, making, using, offering for sale, and/or selling technology for video compression, including but not limited to the MediaTek '112 Products.

677. One or more of the MediaTek '112 Products perform predictive coding on a macroblock of a video frame such that a set of pixels of the macroblock is coded using some of the pixels from the same video frame as reference pixels and the rest of the macroblock is coded using reference pixels from at least one other video frame.

678. One or more of the MediaTek '112 Products include a system for video compression comprising an intra-frame coding unit configured to perform predictive coding on a set of pixels of a macroblock of pixels using a first group of reference pixels, the macroblock of pixels and the first group of reference pixels being from a video frame.

679. One or more of the MediaTek '112 Products include a system for video compression comprising an inter-frame coding unit configured to perform predictive coding on the rest of the macroblock of pixels using a second group of reference pixels, the second group of reference pixels being from at least one other video frame.

680. The MediaTek '112 Products are available to businesses and individuals throughout the United States.

681. The MediaTek '112 Products are provided to businesses and individuals located in the State of Delaware.

682. By making, using, testing, offering for sale, and/or selling products and services for interpolating a pixel during the interlacing of a video signal, including but not limited to the MediaTek '112 Products, MediaTek has injured Dynamic Data and is liable to the Plaintiff for directly infringing one or more claims of the '112 patent, including at least claim 11 pursuant to 35 U.S.C. § 271(a).

683. MediaTek also indirectly infringes the '112 patent by actively inducing infringement under 35 U.S.C. § 271(b).

684. MediaTek has had knowledge of the '112 patent since at least service of this First Amended Complaint or shortly thereafter, and MediaTek knew of the '112 patent and knew of its infringement, including by way of this lawsuit. Alternatively, MediaTek has had knowledge of the '112 Patent based on prior communications that identified the '112 Patent to MediaTek as early as six years prior to the filing of this First Amended Complaint.

685. MediaTek intended to induce patent infringement by third-party customers and users of the MediaTek '112 Products and had knowledge that the inducing acts would cause infringement or was willfully blind to the possibility that its inducing acts would cause infringement. MediaTek specifically intended and was aware that the normal and customary use of the accused products would infringe the '112 patent. MediaTek performed the acts that constitute induced infringement, and would induce actual infringement, with knowledge of the '112 patent and with the knowledge that the induced acts would constitute infringement. For example, MediaTek provides the MediaTek '112 Products that have the capability of operating in a manner that infringe one or more of the claims of the '112 patent, including at least claim 11,

and MediaTek further provides documentation and training materials that cause customers and end users of the MediaTek '112 Products to utilize the products in a manner that directly infringe one or more claims of the '112 patent.[50] By providing instruction and training to customers and end-users on how to use the MediaTek '112 Products in a manner that directly infringes one or more claims of the '112 patent, including at least claim 11, MediaTek specifically intended to induce infringement of the '112 patent. MediaTek engaged in such inducement to promote the sales of the MediaTek '112 Products, e.g., through MediaTek user manuals, product support, marketing materials, and training materials to actively induce the users of the accused products to infringe the '112 patent. Accordingly, MediaTek has induced and continues to induce users of the accused products to use the accused products in their ordinary and customary way to infringe the '112 patent, knowing that such use constitutes infringement of the '112 patent.

686. The '112 patent is well-known within the industry as demonstrated by multiple citations to the '112 patent in published patents and patent applications assigned to technology companies and academic institutions. MediaTek is utilizing the technology claimed in the '112 patent without paying a reasonable royalty. MediaTek is infringing the '112 patent in a manner best described as willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate.

687. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '112 patent.

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[50] *See, e.g.*, MEDIATEK MT6797 LTE-A SMARTPHONE APPLICATION PROCESSOR FUNCTIONAL SPECIFICATION FOR DEVELOPMENT BOARD (July 19, 2016); *MT6592 Octa-Core Smartphone Application Processor Technical Brief,* MEDIATEK DOCUMENTATION (July 6, 2013); *MT6795 Octa-Core Smartphone Application Processor Technical Brief*, MEDIA TEK DOCUMENTATION 0.1 (August 27, 2014); and *MediaTek MS6592 Specifications,* MEDIATEK WEBSITE, *available at*: https://www.mediatek.com/products/smartphones/mt6592.

688. As a result of MediaTek's infringement of the '112 patent, Dynamic Data has suffered monetary damages, and seeks recovery in an amount adequate to compensate for MediaTek's infringement, but in no event less than a reasonable royalty for the use made of the invention by MediaTek together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Dynamic Data respectfully requests that this Court enter:

A. A judgment in favor of Dynamic Data that MediaTek has infringed, either literally and/or under the doctrine of equivalents, the '944, '376, '918, '175, '177, '039, '529, '609, '799, '054, '073, '105, and '112 Patents;

B. An award of damages resulting from MediaTek's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order finding that MediaTek's infringement was willful, wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate within the meaning of 35 U.S.C. § 284 and awarding to Dynamic Data enhanced damages.

D. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Dynamic Data its reasonable attorneys' fees against MediaTek.

E. Any and all other relief to which Dynamic Data may show themselves to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Dynamic Data Technologies, LLC requests a trial by jury of any issues so triable by right.

Dated: March 6, 2019

BAYARD, P.A.

/s/ Stephen B. Brauerman
Stephen B. Brauerman (#4952)
600 N. King Street, Suite 400
P.O. Box 25130
Wilmington, Delaware 19801
(302) 655-5000
sbrauerman@bayardlaw.com

Attorneys for Plaintiff
Dynamic Data Technologies, LLC

OF COUNSEL:

Dorian S. Berger
Daniel P. Hipskind
Eric B. Hanson
BERGER & HIPSKIND LLP
9538 Brighton Way, Ste. 320
Beverly Hills, CA 90210
(323) 886-3430
dsb@bergerhipskind.com
dph@bergerhipskind.com
ebh@bergerhipskind.com