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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

INTEL CORPORATION, Plaintiff, v. TELA INNOVATIONS, INC., Defendant.	CASE NO. 18-cv-02848-WHO **SECOND AMENDED COMPLAINT FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT AND UNENFORCEABILITY** **DEMAND FOR JURY TRIAL** Judge: Hon. William H. Orrick

Plaintiff INTEL CORPORATION ("Intel"), for its Second Amended Complaint against Defendant TELA INNOVATIONS, INC. ("Tela") seeking declaratory judgment of non-infringement and/or unenforceability as to the following patents owned by Tela: U.S. Patent Nos. 7,943,966; 7,948,012; 8,030,689; 8,258,552; 9,425,272; 9,443,947; 7,446,352; 10,141,334; 10,141,335; 10,186,523 (collectively, the "Patents-in-Suit"), as well as bringing claims for breach of contract, correction of inventorship, fraud, and violation of California Business and Professions Code § 17200 et seq., hereby alleges as follows:

NATURE OF THE ACTION

1. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 et. seq. and the Declaratory Judgment Act, 28 U.S.C. §§ 2201-2202, seeking a declaratory judgment of: (i) non-infringement of the Patents-in-Suit; (ii) unenforceability of certain of the Patents-in-Suit due to inequitable conduct and/or patent misuse; (iii) a bar to asserting infringement of certain of the Patents-in-Suit due to equitable estoppel; (iv) non-infringement of certain of the Patents-in-Suit due to a bar from asserting infringement of any Patent-in-Suit having a proper priority date within the term of the May 9, 2007 Covenant Not To Sue ("CNTS") between Intel and Tela; (v) correction of inventorship of the Patents-in-Suit pursuant to 35 U.S.C. § 256; (vi) non-infringement of the Patents-in-Suit due to Intel being licensed by an omitted inventor, Professor Lawrence T. Pileggi; (vii) lack of standing to assert the Patents-in-Suit; and for such other relief as the Court deems just and proper. Intel further brings claims against Tela for breach of the CNTS, fraud, and violation of California Business and Professions Code § 17200 et seq.

2. Intel requests this declaratory judgment and other relief because: (i) Tela is asserting its patents in bad faith because Tela knows that Intel does not infringe the Patents-in-Suit; (ii) inequitable conduct during prosecution and patent misuse render certain of the Patents-in-Suit unenforceable; (iii) Tela is barred from asserting infringement against Intel with respect to certain of the Patents-in-Suit due to equitable estoppel; (iv) Tela is barred from asserting infringement of the

Patents-in-Suit to the extent they have a proper priority date within the term of Intel and Tela's CNTS; (v) Tela breached the CNTS between Intel and Tela; (vi) the inventorship of the Patents-in-Suit requires correction; (vii) Tela is barred from asserting infringement of the Patents-in-Suit because Intel is licensed by Professor Pileggi; (viii) Tela lacks standing to assert the Patents-in-Suit; and (ix) Tela has engaged and continues to engage in unlawful, unfair, and fraudulent business acts.

THE PARTIES

3. Plaintiff Intel is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95054.

4. On information and belief, Defendant Tela is a privately held corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 475 Alberto Way, Suite 120, Los Gatos, CA 95032.

JURISDICTION AND VENUE

5. This Court has exclusive subject matter jurisdiction over this action pursuant to federal question jurisdiction, 28 U.S.C. §§ 1331 and 1338(a), the Declaratory Judgment Act, 28 U.S.C. §§ 2201-2202, and the Patent Laws of the United States, 35 U.S.C. § 1 et seq. This Court has subject matter jurisdiction over the breach of contract, fraud, and violation of California Business and Professions Code § 17200 et seq. claims pursuant to supplemental jurisdiction, 28 U.S.C. § 1367(a).

6. An actual and justiciable controversy exists between Intel and Tela as to the alleged infringement and enforceability of the claims of the Patents-in-Suit.

7. This Court has subject matter jurisdiction over this action based on a real and immediate controversy between Intel and Tela regarding whether various Intel processors and/or process nodes infringe certain Tela patents, whether those Tela patents are unenforceable, whether Intel is licensed to those Tela patents, whether Tela has standing to assert those patents, and whether

Tela is barred from asserting infringement of those Tela patents based on Intel and Tela's CNTS. As described in more detail below, this controversy arises out of Tela's infringement assertions and licensing demands to Intel between the first half of 2014 to April 2016 with respect to Intel's 22nm and 14nm FinFET-based products, in which Tela broadly alleges that its patents cover technologies implemented by Intel's products, as well as infringement claims that Tela has brought against Intel since December 2018.

8. This Court has subject matter jurisdiction over the breach of contract, fraud, and violation of California Business and Professions Code § 17200 et seq. claims based on their being so related to the claims brought herein over which the Court has original jurisdiction that they form part of the same case or controversy under Article III of the United States Constitution.

9. This Court has personal jurisdiction over Tela because Tela has its principal place of business in this district and conducts substantial business in this district.

10. Venue is proper in this Court under 28 U.S.C. § 1391 because Tela has its principal place of business in this district and is subject to personal jurisdiction in this district.

FACTUAL BACKGROUND

The Patents-in-Suit

11. U.S. Patent No. 7,943,966 ("the '966 Patent") is entitled "Integrated Circuit And Associated Layout With Gate Electrode Level Portion Including At Least Two Complimentary Transistor Forming Linear Conductive Segments And At Least One Non-Gate Linear Conductive Segment," and bears an issuance date of May 17, 2011. The '966 Patent bears a filing date of September 16, 2009. The '966 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '966 Patent is attached hereto as Exhibit 1.

12. U.S. Patent No. 7,948,012 ("the '012 Patent") is entitled "Semiconductor Device Having 1965 NM Gate Electrode Level Region Including At Least Four Active Linear Conductive Segments And At Least One Non-Gate Linear Conductive Segment," and bears an issuance date of May 24, 2011. The '012 Patent bears a filing date of September 16, 2009. The '012 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '012 Patent is attached hereto as Exhibit 2.

13. U.S. Patent No. 8,030,689 ("the '689 Patent") is entitled "Integrated Circuit Device And Associated Layout Including Separated Diffusion Regions Of Different Type Each Having Four Gate Electrodes With Each Of Two Complementary Gate Electrode Pairs Formed From Respective Linear Conductive Segment," and bears an issuance date of October 4, 2011. The '689 Patent bears a filing date of September 18, 2009. The '689 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '689 Patent is attached hereto as Exhibit 3.

14. U.S. Patent No. 8,258,552 ("the '552 Patent") is entitled "Semiconductor Device Including At Least Six Transistor Forming Linear Shapes With At Least Two Transistor Forming Linear Shapes Having Offset Ends," and bears an issuance date of September 4, 2012. The '552 Patent bears a filing date of October 1, 2009. The '552 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '552 Patent is attached hereto as Exhibit 4.

15. U.S. Patent No. 9,425,272 ("the '272 Patent") is entitled "Semiconductor Chip Including Integrated Circuit Including Four Transistors Of First Transistor Type And Four Transistors Of Second Transistor Type With Electrical Connections Between Various Transistors And Methods For Manufacturing The Same," and bears an issuance date of August 23, 2016. The '272 Patent bears a filing date of June 4, 2015. The '272 Patent lists Scott T. Becker and Michael C. Smayling as the

inventors and Tela as the sole assignee. A true and correct copy of the '272 Patent is attached hereto as Exhibit 5.

16. U.S. Patent No. 9,443,947 ("the '947 Patent") is entitled "Semiconductor Chip Including Region Having Integrated Circuit Transistor Gate Electrodes Formed By Various Conductive Structure Of Specified Shape And Position And Method For Manufacturing The Same," and bears an issuance date of September 13, 2016. The '947 Patent bears a filing date of May 13, 2015. The '947 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '947 Patent is attached hereto as Exhibit 6.

17. U.S. Patent No. 7,446,352 ("the '352 Patent") is entitled "Dynamic Array Architecture," and bears an issuance date of November 4, 2008. The '352 Patent bears a filing date of March 7, 2007. The '352 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '352 Patent is attached hereto as Exhibit 7.

18. U.S. Patent No. 10,141,334 ("the '334 Patent") is entitled "Semiconductor Chip Including Region Having Rectangular-Shaped Gate Structures And First-Metal Structures," and bears an issuance date of November 27, 2018. The '334 Patent bears a filing date of August 28, 2017. The '334 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '334 Patent is attached hereto as Exhibit 8.

19. U.S. Patent No. 10,141,335 ("the '335 Patent") is entitled "Semiconductor Chip Including Region Having Rectangular-Shaped Gate Structures And First Metal Structures," and bears an issuance date of November 27, 2018. The '335 Patent bears a filing date of September 6, 2017. The '335 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '335 Patent is attached hereto as Exhibit 9.

20. U.S. Patent No. 10,186,523 ("the '523 Patent") is entitled "Semiconductor Chip Having Region Including Gate Electrode Features Formed In Part From Rectangular Layout Shapes On Gate Horizontal Grid And First-Metal Structures Formed In Part From Rectangular Layout Shapes On At Least Eight First-Metal Gridlines Of First-Metal Vertical Grid," and bears an issuance date of January 22, 2019. The '523 Patent bears a filing date of August 31, 2018. The '523 Patent lists Scott T. Becker and Michael C. Smayling as the inventors and Tela as the sole assignee. A true and correct copy of the '523 Patent is attached hereto as Exhibit 10.

21. Intel is an investor in Tela. Tela approached Intel in December 2005 regarding investing in Tela. Intel finalized its investment in Tela in May 2007. As part of that investment, Intel and Tela entered into a CNTS on May 9, 2007, that covers Tela patents claiming priority during the term of the CNTS. The CNTS between Intel and Tela is still in effect.

22. The Patents-in-Suit purport to claim priority to a provisional application (U.S. Patent Application No. 60/781,288) filed on March 9, 2006 ("The 2006 Provisional"). Intel disagrees with Tela's purported claim of priority to The 2006 Provisional for the Patents-in-Suit. As discussed in Count X below, all but one of the Patents-in-Suit are only entitled to priority dates after May 9, 2007, and thus are covered by the CNTS.

23. Tela claims to be the owner of each of the Patents-in-Suit. Tela further claims to be the owner of over 200 issued and pending U.S. patents. Intel reserves all rights to amend this Second Amended Complaint to seek a declaratory judgment of non-infringement, invalidity, and/or unenforceability of, and/or a license to, these or any other U.S. patent owned by Tela.

Intel Has a Long History of Innovation in the Semiconductor Industry

24. Intel has been a pioneer in the semiconductor industry since the 1970s.

25. Intel has introduced generation after generation of cutting-edge microprocessors, memory products and related chips that have been the benchmark for high performance computers.

26. A key area of Intel's research and development has been development of fabrication techniques that make its products possible, including development of gridded semiconductor layout technology. This technology involves placing various features of a semiconductor device in a grid-like pattern to achieve design efficiencies.

Intel Invented the Accused Technology Before the Patents-in-Suit

27. Intel conducted extensive research and development of gridded layout techniques for high resolution lithography, and documented this technology in its 45nm design rules by May 2004.

28. Intel's invention and documentation of this gridded layout technology in its 45nm design rules occurred almost two years before Tela filed The 2006 Provisional on March 9, 2006.

29. Intel's invention and documentation of this gridded layout technology in its 45nm design rules occurred over a year before Tela was founded in 2005.

30. Intel's invention and documentation of this gridded layout technology in its 45nm design rules occurred over a year before Tela approached Intel in late 2005 about investing in Tela.

31. Intel developed GDSII layout files for its 45nm SRAM test chip by June 2005.

32. Intel taped-out its 45nm SRAM test chip by August 2005.

33. Intel publicly announced its working 45nm SRAM test chip by January 25, 2006.

34. Intel's 45nm design rules were used by Intel for implementation into products on the 45nm process node, and such products, including Intel's 45nm Penryn product, were commercially available by at least November 2007.

35. In March 2013, Tela brought an ITC action against several handset manufacturers (Motorola, Nokia, LG, HTC, and Pantech) alleging infringement of several Tela patents, including two of the Patents-in-Suit (the '689 Patent and the '552 Patent) and other patents in the same family of patents ("ITC Action").

36. In May 2013, the respondent handset manufacturers in the ITC Action issued a subpoena to Intel requesting technical documents and a deposition relating to several Intel products, including the 45nm Penryn product and 45nm SRAM test chip, for use as prior art to Tela's patents.

37. In July 2013, Intel produced GDSII files and design rule documents on a standalone computer for review by outside counsel and experts for the respondents and Tela in the ITC Action.

38. In July 2013, Intel provided in the ITC Action a 30(b)(6) deposition regarding Intel's 45nm SRAM test chip and 45nm Penryn product.

39. A hearing in the ITC Action was held between February 24 and March 7, 2014.

40. Intel's 30(b)(6) deponent testified at the hearing in the ITC Action on March 4, 2014 regarding Intel's 45nm SRAM test chip and 45nm Penryn product.

41. The respondents in the ITC Action argued that Tela's patents were invalid under 35 U.S.C. § 102(g) because of Intel's earlier development of gridded layout technology via its 45nm process technology.

42. In response to the respondents' 102(g) argument, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer. Tela also took the position that Tela's patents were valid over Intel's 45nm prior art because Tela's patents required strictly one-dimensional conductive structures in the gate layer and were different from Intel's gridded layout technology with two-dimensional conductive structures.

43. The technology behind Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents is still used in Intel's accused process nodes.

44. Tela settled the ITC Action with a subset of the handset manufacturers in May 2014 and with the remainder of the handset manufacturers in July 2014. The ITC Action was terminated before the Administrative Law Judge issued an Initial Determination on the merits of the case.

Intel's Response to Tela's Accusations of Infringement

45. In the first half of 2014, Tela notified Intel that certain Tela patents purportedly not covered by the CNTS read on Intel's products. Tela indicated that it wanted to discuss with Intel the licensing of Tela's patents that allegedly were not covered by the CNTS. In August 2014, Tela sent Intel lists of the Tela patents and applications in question, which included the '966, '012, '689, '552, and '352 Patents, and offered to schedule a meeting for Tela to present claim charts to Intel.

46. In October 2014, Tela informed Intel via telephone conversation that Tela was reverse engineering Intel products to establish evidence of Intel's alleged use of technology covered by Tela's 1D gridded layout patent family.

47. On January 22, 2015, Tela informed Intel that it was working on claim charts and would be ready to meet to provide and discuss the claim charts in the next few weeks. Tela stated, on January 27, 2015, that its reverse-engineering efforts and claim charts were nearly complete and that its analysis purportedly determined alleged infringement of Tela's 1D gridded layout patent family by Intel's 22nm and 14nm FinFET-based products. Tela reiterated its request for a meeting to present claim charts to Intel. Tela also asserted that it was pursuing licensing assertions against the entire semiconductor industry and had limited manpower for its discussions with Intel, but noted that Intel remained an important target for Tela.

48. Intel was surprised when Tela informed Intel of its belief that Intel products practice Tela's patents. Intel immediately investigated in detail Tela's beliefs when Tela first raised them with Intel. Intel confirmed the dates and specifics of Intel's designs and production runs in Intel design rules documents, chip layout files, semiconductor fabrication process flow, and in the design and manufacture of Intel's 45nm SRAM test chip through to the 45nm Penryn CPU.

49. Intel verified the design, development and production dates for its 45nm process and products as part of its investigation in response to Tela coming forward in 2014 with its belief that

Intel products practice Tela's patents. Intel determined that it independently developed the specific "gridded" semiconductor layout technology at issue long before Tela applied for its patents.

50. Intel was also surprised that Tela attempted to apply its one-dimensional layout patents to Intel's earlier-developed structures that Tela previously claimed in the ITC Action were two-dimensional and thus do not infringe Tela's patents. Regardless, because Intel's technology used in its commercial products since at least 2007—including use of the accused features at issue in Intel's 45nm, 22nm, and 14nm products—was developed by Intel well before any of Tela's patents were conceived, and before Tela was even created, Intel's products cannot be covered by Tela's patents. And Tela's attempts to apply those patents to Intel's products would render Tela's patents invalid because Intel's technology was developed by Intel first.

51. Tela and Intel scheduled a meeting for February 24, 2015, for Tela to provide and present its claim charts to Intel.

52. On February 10, 2015, Tela notified Intel that it had to postpone the meeting for the time being due to internal circumstances. Tela did not provide any claim charts to Intel at this time.

53. In March 2016, Tela informed Intel that it had not forgotten about its assertions against Intel and wanted to resume discussions; Tela apologized to Intel for the large gap in communication.

54. In April 2016, Tela asserted that it expected a licensing payment from Intel and specified a general numerical range for its demand. Tela also repeated its previous assertion that it would provide claim charts showing alleged infringement of its 1D gridded layout patent family by Intel's 22nm and 14nm FinFET-based products, and reiterated that Intel remained an important target for Tela. In that discussion, Intel explained that it did not need a license, including because the accused features in Intel's 22nm and 14nm products were developed (in connection with Intel's 45nm products) before Tela's 1D gridded layout family. Tela stated that it was aware of this issue but nevertheless planned to maintain its infringement accusations against Intel. Tela also stated that it was

pursuing assertion of claim limitations in later-issued patents within the 1D gridded layout patent family that Tela believed strengthened its infringement assertions against Intel's 22nm and 14nm products. Intel was aware of Tela's continuing prosecution efforts with respect to the 1D gridded layout patent family.

55. On May 25, 2016, Tela and Intel entered into a non-disclosure agreement ("NDA") pertaining to licensing discussions. The NDA was forward looking, and applied to discussions on or after May 25, 2016.

56. On December 19, 2018, Tela brought an ITC action against Intel and several of Intel's customers (Acer, Inc., Acer America Corporation, ASUSTeK Computer Inc., ASUS Computer International, Lenovo Group Ltd., Lenovo (United States) Inc., Micro-Star International Co., Ltd., and MSI Computer Corp.) alleging infringement of four of the Patents-in-Suit (the '966, '012, '334, and '335 Patents). On the same day, Tela brought counterclaims against Intel in this case asserting infringement of the '966, '012, '352, '334, and '335 Patents. On February 6, 2019, Tela filed an amended complaint in the ITC action asserting infringement of the '523 patent. On February 8, 2019, Tela amended its counterclaims in this action to assert infringement of the '523 Patent.

Tela Misappropriated the Core Technology of the Patents-in-Suit from Professor Lawrence Pileggi

57. Professor Lawrence T. Pileggi is the Tanoto Professor of Electrical and Computer Engineering at Carnegie Mellon University ("CMU"). Professor Pileggi received his Master's and Bachelor of Science degrees in Electrical Engineering from the University of Pittsburgh in 1983-1984, and his Ph.D. in Electrical and Computer Engineering from CMU in 1989. His research focuses on all aspects of modeling, design, and design methodologies for CMOS and post-CMOS technologies.

58. On May 27, 2004, Professor Pileggi founded Fabbrix Inc. ("Fabbrix") to pursue his research in regular fabric semiconductor layouts commercially. Fabbrix's technology focused on

solving challenges due to sub-wavelength lithography, *i.e.*, semiconductor feature sizes smaller than the wavelength of light used to create them. To address these challenges, Professor Pileggi's "regular fabric" technology utilized, among other things, simplified regular layout geometries with unidirectional gridded gate and metal layers.

59. Tela has provided Intel documentation indicating that Tela was founded in January 2005 by Scott Becker ("Becker"), Dhrumil Gandhi, and John Malecki.

60. On March 1, 2005, Professor Pileggi and a number of Fabbrix employees met with Becker at CMU to interview him for the position of Fabbrix CEO. Immediately before the meeting, Becker signed an NDA in which he agreed not to use Fabbrix confidential information for any purpose other than entering into a business relationship with Fabbrix. Becker was informed in detail about Fabbrix's technology at this meeting, including regular layout geometries with unidirectional gridded gate and metal layers.

61. Notwithstanding Tela's representations that it was founded in January 2005, Becker failed to tell anyone at the March 1, 2005 meeting that he was operating his own competing company at the time he interviewed for a CEO position at Fabbrix. During the March 1, 2005 meeting, Becker expressed that he was unfamiliar with 1D gridded layout technology. After the meeting, Becker did not join or enter into a business relationship with Fabbrix, but instead incorporated Tela and pursued the 1D gridded layout technology disclosed to him by Professor Pileggi and Fabbrix.

62. From April 2005 through June 2005, John Malecki ("Malecki") was acting CEO of Fabbrix. While Malecki was acting CEO, he had access to and learned in detail about confidential Fabbrix technology, including as it related to layout geometries with unidirectional gridded gate and metal layers, through Fabbrix material including presentations and layout diagrams, as well as discussions with Professor Pileggi and Fabbrix employees.

63. Malecki joined Tela in or around May 2005. Malecki did not inform anyone at Fabbrix that he had joined Tela while he continued to act as Fabbrix CEO and receive confidential details about Fabbrix technology through June 2005.

64. On June 1, 2005, Tela Innovations, Inc. was formally incorporated. The information regarding Professor Pileggi's 1D gridded layout technology that Becker and Malecki received from Fabbrix is reflected in the core of Tela's 1D gridded layout technology, which Becker and Malecki used as the foundation for Tela's business and the subsequent 1D gridded layout patent family.

65. On March 9, 2006, Becker and Smayling filed The 2006 Provisional to which the Patents-in-Suit claim priority. The 2006 Provisional describes a solution using "a grid pattern" where layers other than diffusion "should be rectangular in shape and fixed in one dimension." Becker and Smayling did not themselves invent these and other core ideas expressed in The 2006 Provisional, but instead misappropriated them from Professor Pileggi. For example, during the March 1, 2005 meeting, Professor Pileggi and Fabbrix disclosed to Becker a regular fabric layout with "all poly, M1 and contacts on grid," "fixed poly pitch," and "single orientation of CD [critical dimension] lines." *E.g.*, 90214DOC0001309 at 321, 327; 90214DOC0001362 at 379, 383. Similarly, other Fabbrix presentations to which Malecki had access disclose a gridded architecture where "Poly, Metal 1 and Metal 2 are unidirectional." *E.g.*, 90214DOC0001451 at 489, 483, 467; 90214DOC0001622 at 658, 652, 638.

66. Over the following years, Becker and Smayling filed applications for many patents claiming priority to The 2006 Provisional, including the Patents-in-Suit. These patent applications contain false representations from Becker and Smayling that they were the original inventors of the claimed subject matter, when in fact they had misappropriated the core of the claimed subject matter from Professor Pileggi. On information and belief, Becker and Smayling knowingly and intentionally

concealed these facts from the Patent Office so that they would be the only named inventors to the exclusion of Professor Pileggi.

In Order To Secure an Investment from Intel, Tela Knowingly and Intentionally Concealed from Intel that It Misappropriated Its Technology from Professor Pileggi

67. In December 2005, Tela approached Intel about Intel investing in Tela. Tela sent Intel a presentation that, among other things, described its "IP Protection Status," including "[f]uture patents" on "[d]ynamic array layout architecture." Intel understands that "[d]ynamic array layout architecture" referred to the 1D gridded architecture that became the subject of the 1D gridded patent family. Tela's presentation also noted that Fabbrix was a competitor, but failed to mention that Tela had misappropriated its core technology from Professor Pileggi.

68. In May 2006, Tela stated to Intel that its architecture used a gridded layout and directional constraints on all layers except diffusion, and that it had a patent pending on this technology. Neither Becker nor anyone else at Tela informed Intel that Tela had misappropriated this and related technology from Professor Pileggi. To the contrary, Tela represented to Intel that its technology was "clean."

69. In June 2006, Tela stated to Intel that one of the key attributes of its architecture was a highly structured and regular layout, which it illustrated as having unidirectional gridded gate and metal layers. Tela further stated that its architecture comprised layout design innovations. Tela failed to inform Intel that its purported "innovations" were misappropriated from Professor Pileggi.

70. In April 2007, Tela stated to Intel that it had a patent application pending on "[d]ynamic array architecture (1D architecture)." Tela further stated that "[w]e believe that patents are the backbone of our company."

71. The presentations and statements described above were provided by Becker to Intel employees including at least Shishpal Rawat.

72. Intel finalized its investment in Tela in May 2007. The associated Series B Stock Purchase Agreement contains the following provision:

> 2.25 ***Full Disclosure.*** The Company [Tela] has provided each Investor or their counsel with such information as it has deemed necessary to respond in all material respects to the Investor's request for information about the Company. Neither this Agreement, together with any exhibits or schedules attached hereto, nor any other agreement, document, certificate or written information furnished to the Investors or their counsel by or on behalf of the Company in connection with the transactions contemplated hereby contains any untrue statement of a material fact or omits to state a material fact necessary in order to make the statements contained herein not misleading in light of the circumstances under which they were made.

73. The Schedule of Exceptions to the Series B Stock Purchase Agreement states in the "Intellectual Property" section that Tela had a pending patent application on "Dynamic array architecture (1D architecture)." Tela failed to inform Intel that the core of this "1D architecture" was misappropriated from Professor Pileggi.

74. In connection with Intel's investment in Tela, Tela provided documents to Intel and made other written and verbal statements that were untrue and misleading in that they represented that Tela had independently developed its technology, including regular layout geometries with unidirectional gridded gate and metal layers, when in fact Tela misappropriated the core of its technology from Professor Pileggi. In deciding to invest in Tela, Intel relied on these documents and other written and verbal statements by Tela.

75. In a February 27, 2008 press release on Intel Capital's investment in Tela, Tela stated the following:

> About Tela Innovations
>
> Tela develops technology for addressing the challenge of scaling semiconductor design and manufacturing to next generation process geometries, such as 45nm and 32nm. Its solution uses gridded, straight line, one dimensional layout structures to provide a more efficient and reliable way to implement next generation chips.

76. Had Intel known that Tela's solution, including "gridded, straight line, one dimensional layout structures," was not independently developed by Tela—but was instead misappropriated by Becker and Malecki from Professor Pileggi—Intel would not have invested in Tela.

COUNT I

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 7,943,966)

77. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

78. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '966 Patent.

79. Intel's products, including at least its 22nm, 14nm, and 10nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '966 Patent, either literally or under the doctrine of equivalents. For example, independent claim 1 of the '966 Patent requires a "gate electrode level layout portion including a plurality of linear-shaped layout features placed to extend lengthwise in a first direction so as to extend parallel to each other." Independent claim 2 of the '966 Patent requires a "gate electrode level region [that] includes a plurality of linear conductive segments . . ., wherein the plurality of linear conductive segments are formed to have their lengths extend in a first direction in a parallel manner." Claims 1 and 2 are the only independent claims in the '966 Patent.

80. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents.

Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '966 Patent.

81. Tela has failed to properly accuse or provide claim charts in this case for Intel's 10nm products, and instead simply argues that "Intel's own publications show that its 10nm process shares similar gate features, dummy gates, and contact structures with its 14nm process." To the extent Tela is permitted to proceed with its infringement accusations against Intel's 10nm products, these products do not infringe any claims of the '966 Patent for the same reasons discussed above with respect to Intel's 22nm and 14nm products.

82. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '966 Patent.

COUNT II

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 7,948,012)

83. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

84. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '012 Patent.

85. Intel's products, including at least its 22nm, 14nm, and 10nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '012 Patent, either literally or under the doctrine of equivalents. For example, independent claim 1 of the '012 Patent requires a "gate electrode level layout portion including a plurality of linear-shaped layout features placed to extend lengthwise in a first direction so as to extend parallel to each other." Independent claim 2 of the '012 Patent requires a "gate electrode level region [that] includes a plurality of linear conductive segments . . ., wherein the plurality of linear conductive segments are formed to

have their lengths extend in a first direction in a parallel manner." Claims 1 and 2 are the only independent claims in the '012 Patent.

86. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents. Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '012 Patent.

87. Tela has failed to properly accuse or provide claim charts in this case for Intel's 10nm products, and instead simply argues that "Intel's own publications show that its 10nm process shares similar gate features, dummy gates, and contact structures with its 14nm process." To the extent Tela is permitted to proceed with its infringement accusations against Intel's 10nm products, these products do not infringe any claims of the '012 Patent for the same reasons discussed above with respect to Intel's 22nm and 14nm products.

88. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '012 Patent.

COUNT III

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,030,689)

89. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

90. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '689 Patent.

91. Intel's products, including at least the accused 22nm and 14nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '689 Patent, either literally or under the doctrine of equivalents. For example, independent claim 1 of the '689 Patent requires "gate electrode level layout shapes . . . formed from a first [and second] linear layout shape within the gate electrode level region layout." Independent claim 2 of the '689 Patent requires "a first [and second] linear conductive segment within the gate electrode level region." Claims 1 and 2 are the only independent claims in the '689 Patent.

92. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents. Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '689 Patent.

93. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '689 Patent.

COUNT IV

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,258,552)

94. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

95. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '552 Patent.

96. Intel's products, including at least the accused 22nm and 14nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '552 Patent,

either literally or under the doctrine of equivalents. For example, independent claims 1, 48 and 49 of the '552 Patent require "at least six linear shapes extending along a first direction in a gate layer region of the region of the semiconductor device." Claims 1, 48 and 49 are the only independent claims in the '552 Patent.

97. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents. Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '552 Patent.

98. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '552 Patent.

COUNT V

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 9,425,272)

99. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

100. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '272 Patent.

101. Intel's products, including at least the accused 22nm and 14nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '272 Patent, either literally or under the doctrine of equivalents. For example, independent claims 1 and 29 of the '272 Patent require that "the first [and second] edge of each of the at least eight conductive structures is substantially straight." Claims 1 and 29 are the only independent claims in the '272 Patent.

102. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents. Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '272 Patent.

103. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '272 Patent.

COUNT VI

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 9,443,947)

104. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

105. An actual and justiciable controversy exists between Intel and Tela concerning the non-infringement of the '947 Patent.

106. Intel's products, including at least the accused 22nm and 14nm products, have not infringed, and do not infringe, directly or indirectly, any valid and enforceable claim of the '947 Patent, either literally or under the doctrine of equivalents. For example, independent claims 1 and 29 of the '947 Patent require that "the first [and second] edge of each of the at least eight conductive structures is substantially straight." Claims 1 and 29 are the only independent claims in the '947 Patent.

107. As alleged above in Paragraph 42, Tela took the position in the ITC Action that Intel's 45nm products have two-dimensional conductive structures in the gate layer and were thus different from Tela's 1D gridded layout patents, which require one-dimensional conductive structures. Intel's accused 22nm and 14nm products use the same conductive structures in the gate layer as Intel's 45nm

products that Tela distinguished at the ITC as being two-dimensional and different from Tela's patents. Based on Tela's own arguments, Intel's accused 22nm and 14nm products do not infringe any of the claims of the '947 Patent.

108. Intel is entitled to a judgment from this Court that Intel has not infringed, and does not infringe, any valid and enforceable claim of the '947 Patent.

COUNT VII

(Declaratory Judgment of Unenforceability of U.S. Patent Nos. 9,425,272, 9,443,947, 10,141,334, and 10,141,335 Due to Inequitable Conduct)

109. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

110. An actual and justiciable controversy exists between Intel and Tela concerning the '272, '947, '334, and '335 Patents.

111. The '272, '947, '334, and '335 Patents, which Tela has asserted against Intel, are unenforceable due to inequitable conduct that occurred during the prosecution of the respective applications resulting in the issuance of these patents.

112. Becker and Smayling are named as alleged inventors on the face of each of the '272, '947, '334, and '335 Patents.

113. Upon information and belief, Becker is the President and CEO of Tela, and served in this role at Tela while the '272, '947, '334, and '335 Patents were being prosecuted.

114. Upon information and belief, Smayling was Senior Vice President of Product Technology at Tela while at least the '272 and '947 Patents were being prosecuted.

115. Kenneth D. Wright ("Wright") of the law firm Martine Penilla Group, LLP, on behalf of Tela, prosecuted the applications that issued as the '272, '947, '334, and '335 Patents.

116. In connection with prosecution of the '272 and '947 Patents, Becker and Smayling signed declarations vouching for the content of the applications, in which they acknowledged their

duty to disclose to the Patent Office information known to them to be material to patentability of the claims of the ’272 and ’947 Patents in accordance with 37 C.F.R. § 1.56.

117. Upon information and belief, Wright understood his duty to disclose to the Patent Office information known to him to be material to patentability of the claims of the ’272, ’947, ’334, and ’335 Patents in accordance with 37 C.F.R. § 1.56.

118. Upon information and belief, Wright also informed Becker and Smayling of their duty of disclosure to the Patent Office.

119. The application that resulted in the issuance of the ’272 Patent is U.S. Patent Application No. 14/731,316 (“the ’316 Application”).

120. The ’316 Application was filed on June 4, 2015, and issued on August 23, 2016, as the ’272 Patent.

121. The ’316 Application claims to be a continuation of U.S. Patent Application No. 13/774,919 (filed on February 22, 2013), which claims to be a continuation of U.S. Patent Application No. 12/572,225 (filed on October 1, 2009, and issued as U.S. Patent No 8,436,400), which claims to be a continuation of U.S. Patent Application No. 12/212,562 (filed on September 17, 2008, and issued as U.S. Patent No. 7,842,975), which claims to be a continuation of U.S. Patent Application No. 11/683,402 (filed on March 7, 2007, and issued as U.S. Patent No. 7,446,352).

122. The ’272 Patent, and each application in its chain, purport to claim priority to The 2006 Provisional application filed on March 9, 2006.

123. Each of Becker, Smayling, and Wright added new subject matter to the specification of the ’316 Application, and/or vouched for the ’316 Application containing such new matter, on June 4, 2015, when they filed that application (“June 2015 Specification”). That new subject matter includes the description of an embodiment contained in paragraph 0013 of the June 2015 Specification. A true and correct copy of the June 2015 Specification is attached hereto as Exhibit 11. The new

subject matter added to the June 2015 Specification corresponds to columns 5:22-7:30 of the '272 Patent.

124. The new subject matter described in paragraph 0013 of the June 2015 Specification, and the corresponding columns 5:22-7:30 of the '272 Patent, is incorporated into limitations of independent claims 1 and 29 of the '272 Patent, which are the only independent claims of the '272 Patent. The new subject matter includes, among other things, the following limitations: (i) "wherein the width of each of the at least eight conductive structures is less than 45 nanometers;" and (ii) "a first pitch that is less than or equal to about 193 nanometers."

125. The new subject matter that is incorporated into limitations of the independent claims of the '272 Patent (as noted in Paragraph 124 of this Complaint) was not described or disclosed in The 2006 Provisional to which the '272 Patent claims priority. A true and correct copy of The 2006 Provisional is attached hereto as Exhibit 12.

126. The new subject matter that is incorporated into limitations of the independent claims of the '272 Patent (as noted in Paragraph 124 of this Complaint) was disclosed for the first time on June 4, 2015, in the June 2015 Specification.

127. Because all independent (and thus all dependent) claims of the '272 Patent contain limitations that were disclosed in the specification no earlier than June 4, 2015, the '272 Patent is not entitled to claim a priority date earlier than June 4, 2015.

128. The Patent Office has confirmed that the new subject matter was not described or disclosed in The 2006 Provisional. For example, on August 28, 2017, Tela filed U.S. Patent Application No. 15/688,187 ("the '187 Application"). The '187 Application purported to claim priority to The 2006 Provisional. On April 12, 2018, the Examiner issued a Notice of Allowance. On May 15, 2018, Intel filed its original Complaint in this action (Dkt. 1). On May 25, 2018, Tela filed a Request for Continued Examination of the '187 Application, enclosing an Information Disclosure

Statement (IDS) including Intel's original Complaint. On May 31, 2018, in a telephone interview to discuss the IDS, the Examiner requested clarification of written description support for the following limitations: "wherein the width of each of the at least ten conductive structures is less than 45 nanometers" and "a first pitch that is less than or equal to about 193 nanometers." The Examiner suggested removing these limitations from the specification, but Tela did not agree.

129. On August 8, 2018, the Examiner issued a Corrected Notice of Allowability for the '187 Application, confirming that Tela was not in possession of gate widths less than 45 nanometers or gate pitch less than or equal to about 193 nanometers at the time the parent application was filed, and that Tela's priority claim was therefore improper.

> Applicants have described values of gate pitch and width that they were not in possession of the claimed invention at the time the parent case was filed. Specifically applicants have introduced an unclaimed values of gate pitch of less than or equal to about 193 nanometers and a width of less than or equal to about 45 nanometers, which has no antecedent basis in application 14/711,731. Since both values would have been new matter in application 14/711,731 the claim to priority as a continuation i[s] improper.

130. The Examiner explained that Tela's "newly introduced values"—*i.e.*, gate widths less than 45 nanometers and gate pitch less than or equal to about 193 nanometers—are "nowhere to be found in the parent application," and that the conditions of 35 U.S.C. 120 (Benefit of Earlier Filing Date in the United States) are therefore "clearly not met."

> It would be noted that the gate pitch and width created by newly introduced values is a most prominent design feature in the present application. … Applicants have offered no explanation for how one ordinary skill might recognize these values of application 14/711,731. Since these values are claimed in the present application and is nowhere to be found in the parent application, the conditions of 35 U.S.C. 120 are clearly not met.

131. On November 27, 2018, the '187 Application issued as the '334 Patent.

132. The portions of the '334 file history referenced in the preceding paragraphs are attached hereto at Exhibit 13.

133. Despite knowingly adding new subject matter to the June 2015 Specification, each of Becker, Smayling, and Wright filed the '316 Application as a direct continuation of a chain of prior

applications (which does not allow new matter), instead of filing it as a continuation-in-part (which allows new matter) and/or vouched for the application, which contained such misrepresentations. In particular, Becker submitted a declaration vouching for the '316 Application, which states that it is a continuation. Smayling submitted a declaration vouching for the '316 Application, which states that it is a continuation. Wright filed the '316 Application, which states that is a continuation. A true and correct copy of the Application Data Sheet for the '316 Application is attached hereto as Exhibit 14. (*See* Ex. 9 at 3, section entitled "Domestic Benefit/National Stage Information.")

134. Each of Becker, Smayling, and Wright did not disclose to the Patent Office during prosecution of the '272 Patent that they added new subject matter to the June 2015 Specification.

135. Upon information and belief, each of Becker, Smayling, and Wright filed the '316 Application as a direct continuation of a chain of prior applications, and/or vouched for such Application containing such misrepresentations, in order to attempt to claim the benefit of the priority date of The 2006 Provisional and avoid prior art.

136. Upon information and belief, each of Becker, Smayling, and Wright knowingly and deliberately failed to disclose to the Patent Office that they added new subject matter to the June 2015 Specification, and knowingly and deliberately made affirmative misrepresentations to the Patent Office that the '316 Application was a continuation of prior applications, rather than a continuation-in-part. Each of Becker, Smayling, and Wright's affirmative misrepresentations to the Patent Office constituted egregious misconduct and are thus material to patentability by their very nature, and upon information and belief, each of Becker, Smayling and Wright had knowledge of this materiality.

137. The wrongdoing by each of Becker, Smayling, and Wright is also material to the patentability of the '272 Patent because it impacts the priority date of the '272 Patent, which in turn impacts the prior art that can be considered by the Patent Office in assessing the validity of the '272 Patent. Based on the true priority date of no earlier than June 4, 2015 for the '272 Patent, at least

Becker knew when he submitted a declaration vouching for the '316 Application, and at all times leading up to the issuance of the '272 Patent, that the '272 Patent was invalid based on at least Intel products that were publicly available before 2015, including at least the 22nm and 14nm Intel products Tela has accused of infringing its 1D gridded layout patents. Intel released its 22nm products by April 2012, and released its 14nm products by July 2014. Tela accused Intel's 22nm and 14nm products of infringing its 1D gridded in January 2015, which is before the June 4, 2015 filing date of the '316 Application, and at least Becker was involved in discussions relating to Tela's accusations against Intel and was therefore knowledgeable about the materiality of his failure to disclose. None of Becker, Smayling, or Wright disclosed Intel's 22nm and 14nm products, or Tela's accusations against these products, to the Patent Office during prosecution of the '272 Patent.

138. Upon information and belief, each of Becker, Smayling, and Wright acted with specific intent to deceive the Patent Office because they: (i) knowingly and deliberately added new subject matter to the June 2015 Specification and/or participated in adding such new subject matter; (ii) knowingly and deliberately failed to disclose to the Patent Office that they added new subject matter to the June 2015 Specification; and (iii) knowingly and deliberately filed the '316 Application as a continuation of prior applications, rather than a continuation-in-part, and/or submitted declarations vouching for the application, which contained these statements—all in order to allow Tela to improperly claim priority for the '272 Patent all the way back to The 2006 Provisional to avoid material prior art and to avoid having the '272 Patent encompassed by the CNTS between Tela and Intel. Becker, Smayling, and Wright's specific intent to deceive the Patent Office is the single most reasonable inference to be drawn from Becker, Smayling and Wright's actions.

139. The '272 Patent is unenforceable due to inequitable conduct during the prosecution of the '272 Patent.

140. The application that resulted in the issuance of the '947 Patent is U.S. Patent Application No. 14/711,731 ("the '731 Application").

141. The '731 Application was filed on May 13, 2015, and issued on September 13, 2016, as the '947 Patent.

142. The '731 Application claims to be a continuation of U.S. Patent Application No. 13/774,919 (filed on February 22, 2013), which claims to be a continuation of U.S. Patent Application No. 12/572,225 (filed on October 1, 2009, and issued as U.S. Patent No 8,436,400), which claims to be a continuation of U.S. Patent Application No. 12/212,562 (filed on September 17, 2008, and issued as U.S. Patent No. 7,842,975), which claims to be a continuation of U.S. Patent Application No. 11/683,402 (filed on March 7, 2007, and issued as U.S. Patent No. 7,446,352).

143. The application that resulted in the issuance of the '334 Patent is the '187 Application.

144. The '187 Application was filed on August 28, 2017, and issued on November 27, 2018, as the '334 Patent.

145. The '187 Application claims to be a continuation of U.S. Patent Application No. 15/263,282 (filed on September 12, 2016), which claims to be a continuation of the '731 Application, which claims to be a continuation of U.S. Patent Application No. 13/774,919 (filed on February 22, 2013), which claims to be a continuation of U.S. Patent Application No. 12/572,225 (filed on October 1, 2009, and issued as U.S. Patent No 8,436,400), which claims to be a continuation of U.S. Patent Application No. 12/212,562 (filed on September 17, 2008, and issued as U.S. Patent No. 7,842,975), which claims to be a continuation of U.S. Patent Application No. 11/683,402 (filed on March 7, 2007, and issued as U.S. Patent No. 7,446,352).

146. The application that resulted in the issuance of the '335 Patent is U.S. Patent Application No. 15/696,651 ("the '651 Application").

147. The ’651 Application was filed on September 6, 2017, and issued on November 27, 2018, as the ’335 Patent.

148. The ’651 Application claims to be a continuation of U.S. Patent Application No. 15/263,282 (filed on September 12, 2016), which claims to be a continuation of the ’731 Application, which claims to be a continuation of U.S. Patent Application No. 13/774,919 (filed on February 22, 2013), which claims to be a continuation of U.S. Patent Application No. 12/572,225 (filed on October 1, 2009, and issued as U.S. Patent No 8,436,400), which claims to be a continuation of U.S. Patent Application No. 12/212,562 (filed on September 17, 2008, and issued as U.S. Patent No. 7,842,975), which claims to be a continuation of U.S. Patent Application No. 11/683,402 (filed on March 7, 2007, and issued as U.S. Patent No. 7,446,352).

149. The ’947, ’334, and ’335 Patents, and each application in their chains, purport to claim priority to The 2006 Provisional filed on March 9, 2006.

150. Each of Becker, Smayling, and Wright added new subject matter to the specification of the ’731 Application, and/or vouched for the ’731 Application containing such new matter, on May 13, 2015, when they filed that application (“May 2015 Specification”). The new subject matter includes the description of an embodiment contained in paragraph 0013 of the May 2015 Specification. A true and correct copy of the May 2015 Specification is attached hereto as Exhibit 15. The new subject matter added to the May 2015 Specification corresponds to columns 5:24-6:67 of the ’947 Patent; columns 5:49-7:24 of the ’334 Patent; and columns 5:49-7:24 of the ’335 Patent.

151. The new subject matter described in paragraph 0013 of the May 2015 Specification, and the corresponding columns 5:24-6:67 of the ’947 Patent, is incorporated into limitations of independent claims 1 and 29 of the ’947 Patent, which are the only independent claims of the ’947 Patent. The new subject matter includes, among other things, the following limitations: (i) “wherein

the width of each of the at least eight conductive structures is less than 45 nanometers;" and (ii) "a first pitch that is less than or equal to about 193 nanometers."

152. The new subject matter is also described in columns 5:49-7:24 of the '334 Patent and incorporated into independent claims 1, 29, 30, which are the only independent claims of the '334 Patent. The new subject matter includes, among other things, the following limitations: (i) "each gate structure in the region having a substantially rectangular shape with a width of less than or equal to about 45 nanometers;" and (ii) "a gate pitch of less than or equal to about 193 nanometers."

153. The new subject matter is also described in columns 5:49-7:24 of the '335 Patent and incorporated into independent claims 1, 29, 30, which are the only independent claims of the '335 Patent. The new subject matter includes, among other things, the following limitations: (i) "each of the gate structures having a width of less than or equal to about 45 nanometers;" and (ii) "a gate pitch of less than or equal to about 193 nanometers."

154. The new subject matter that is incorporated into limitations of the independent claims of the '947, '334, and '335 Patents (as noted in Paragraphs 151 through 153 of this Complaint) was not described or disclosed in The 2006 Provisional to which these patents claim priority.

155. The new subject matter that is incorporated into limitations of the independent claims of the '947, '334, and '335 Patents (as noted in Paragraphs 151 through 153 of this Complaint) was disclosed for the first time on May 13, 2015, in the May 2015 Specification.

156. The Examiner has confirmed that the new subject matter was not described or disclosed in The 2006 Provisional, as discussed above in Paragraphs 128 through 132.

157. Because all independent (and thus all dependent) claims of the '947, '334, and '335 Patents contain limitations that were disclosed in the specification no earlier than May 13, 2015, the '947, '334, and '335 Patents are not entitled to claim a priority date earlier than May 13, 2015.

158. Despite knowingly adding new subject matter to the May 2015 Specification, each of Becker, Smayling, and Wright filed the '731 Application as a direct continuation of a chain of prior applications (which does not allow new matter), instead of filing it as a continuation-in-part (which allows new matter). Becker and Smayling each vouched for the '731 Application, which contained such misrepresentations. In particular, Becker and Smayling each submitted a declaration for the '731 Application, stating that it is a continuation. Likewise, Wright filed the '187 and '651 Applications with declarations from Becker and Smayling stating that they are continuations. True and correct copies of the Application Data Sheets for the '731, '187, and '651 Applications are attached hereto as Exhibits 16, 17, and 18, respectively. (*See* Ex. 16 at 3; Ex. 17 at 3; Ex. 18 at 3, section entitled "Domestic Benefit/National Stage Information.")

159. Each of Becker, Smayling, and Wright did not disclose to the Patent Office during prosecution of the '947, '334, or '335 Patents that they added new subject matter to the May 2015 Specification.

160. Upon information and belief, each of Becker, Smayling, and Wright filed the '731 Application as a direct continuation of a chain of prior applications, and/or vouched for such Application containing such misrepresentations, in order to attempt to claim the benefit of the priority date of The 2006 Provisional and avoid prior art. Likewise, Wright filed the '187 and '651 Applications with declarations from Becker and Smayling stating that they are continuations, which upon information and belief was done in order to attempt to claim the benefit of the priority date of The 2006 Provisional and avoid prior art.

161. Upon information and belief, each of Becker, Smayling, and Wright knowingly and deliberately failed to disclose to the Patent Office that they added new subject matter to the May 2015 Specification, and knowingly and deliberately made affirmative misrepresentations to the Patent Office that the '731 Application was a continuation of prior applications, rather than a continuation-

in-part. Upon information and belief, Becker and Wright further knowingly and deliberately made affirmative misrepresentations to the Patent Office that the '187 and '651 Applications were continuations of prior applications, rather than continuations-in-part. Each of Becker, Smayling, and Wright's affirmative misrepresentations to the Patent Office constituted egregious misconduct and are thus material to patentability by their very nature, and each of Becker, Smayling and Wright had knowledge of this materiality.

162. The wrongdoing by each of Becker, Smayling, and Wright is also material to the patentability of the '947, '334, and '335 Patents because it impacts the priority date of each patent, which in turn impacts the prior art that can be considered by the Patent Office in assessing the validity of these patents. Based on the true priority date of no earlier than May 13, 2015 for the '947, '334, and '335 Patents, at least Becker knew when he submitted a declaration vouching for the '731 Application and May 2015 Specification, and at all times leading up to the issuance of the '947, '334, and '335 Patents, that these patents were invalid based on at least Intel products that were publicly available before 2015, including at least the 22nm and 14nm Intel products Tela has accused of infringing its 1D gridded layout patents. Intel released its 22nm products by April 2012, and released its 14nm products by September 2014. Tela accused Intel's 22nm and 14nm products of infringing its 1D gridded in January 2015, which is before the May 13, 2015 filing date of the '731 Application, and at least Becker was involved in discussions relating to Tela's accusations against Intel and was therefore knowledgeable about the materiality of his failure to disclose. None of Becker, Smayling, or Wright disclosed Intel's 22nm and 14nm products, or Tela's accusations against these products, to the Patent Office during prosecution of the '947, '334, or '335 Patents.

163. Upon information and belief, each of Becker, Smayling, and Wright acted with specific intent to deceive the Patent Office because they: (i) knowingly and deliberately added new subject matter to the May 2015 Specification and/or participated in adding such new subject matter; (ii)

knowingly and deliberately failed to disclose to the Patent Office that they added new subject matter to the May 2015 Specification; and (iii) knowingly and deliberately filed the '731, '187, and '651 Applications as continuations of prior applications, rather than continuations-in-part and/or submitted declarations vouching for the '731 Application and May 2015 Specification, which contained these statements—all in order to allow Tela to improperly claim priority for the '947, '334, and '335 Patents, all the way back to The 2006 Provisional to avoid material prior art and to avoid having the '947, '334, and '335 Patents encompassed by the CNTS between Tela and Intel. Becker, Smayling, and Wright's specific intent to deceive the Patent Office is the single most reasonable inference to be drawn from Becker, Smayling, and Wright's actions.

164. The '947, '334, and '335 Patents are unenforceable due to inequitable conduct during the prosecution of these patents.

165. Intel is entitled to a judgment from this Court that the '272, '947, '334, and '335 Patents are unenforceable due to inequitable conduct that occurred during the prosecution of these patents.

COUNT VIII

(Declaratory Judgment of Unenforceability of U.S. Patent Nos. 9,425,272, 9,443,947, 10,141,334, and 10,141,335 Due to Patent Misuse)

166. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference the allegations in Paragraphs 109 through 165 above, with respect to inequitable conduct, as though fully set forth herein.

167. An actual and justiciable controversy exists between Intel and Tela concerning the '272, '947, '334, and '335 Patents, which Tela has asserted against Intel, are unenforceable due to Tela's patent misuse.

168. As discussed above in Paragraphs 109 through 165, each of Becker, Smayling, and Wright, on behalf of Tela, made material misrepresentations to the Patent Office with the specific intent to deceive the Patent Office in connection with the '272, '947, '334, and '335 Patents.

169. Based on the true priority dates of no earlier than June 4, 2015, for the ’272 Patent, and no earlier than May 13, 2015, for the ’947, ’334, and ’335 Patents, Tela knew that the ’272, ’947, ’334, and ’335 Patents were invalid based on at least Intel products that were publicly available before 2015, including at least the 22nm and 14nm Intel products Tela has accused of infringing its patents. Intel released its 22nm products by April 2012, and released its 14nm products by September 2014. Despite knowing that the ’272, ’947, ’334, and ’335 Patents were invalid and had been procured via inequitable conduct, Tela attempted to solicit licenses to its 1D gridded portfolio, which includes the ’272, ’947, ’334, and ’335 Patents, from the entire logic industry, including Intel. Tela had already licensed Intel competitors Qualcomm and TSMC in 2014, licensed Samsung in 2016, and was actively pursuing licenses from the rest of the industry and on information and belief continues to do so.

170. Based on the true priority dates of no earlier than June 4, 2015, for the ’272 Patent, and no earlier than May 13, 2015, for the ’947, ’334, and ’335 Patents, Tela also knew that the ’272, ’947, ’334, and ’335 Patents were covered under the May 9, 2007, CNTS between Intel and Tela.

171. Despite knowing that the ’272, ’947, ’334, and ’335 Patents were invalid and/or covered by the May 9, 2007, CNTS, and, thus, that the ’272, ’947, ’334, and ’335 Patents could not properly be asserted against Intel, Tela continued to assert these patents against Intel in bad faith. Tela’s bad faith assertion of these patents impermissibly broadens the scope of its patent grant with anticompetitive effect by asserting patents against Intel that Tela knew were covered by its non-assertion agreement (CNTS) with Intel and/or invalid based on Intel’s own products, in an attempt to negatively impact Intel’s role in the market. Tela’s assertion of knowingly invalid patents, which also had been procured via inequitable conduct, against other players in the market also harms the market as a whole.

172. Intel is entitled to a judgment from this Court that the ’272, ’947, ’334, and ’335 Patents are unenforceable due to Tela’s patent misuse.

COUNT IX

(Declaratory Judgment of No Infringement Due to Equitable Estoppel)

173. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

174. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

175. Tela should be barred from asserting infringement against Intel with respect to the '966, '012, '689, '552, and '352 Patents due to equitable estoppel.

176. Tela and Intel began talks regarding Intel's business investment in Tela by December 2005. Those interactions culminated in Intel's investment in Tela in May 2007.

177. Intel publicly announced its working 45nm SRAM test chip by January 25, 2006. Intel also publicly discussed its 45nm process in various articles and technical conferences, including presentation of an Intel paper by Clair Webb entitled "Layout Rule Trends and Affect Upon CPU Design" at a February 19, 2006, SPIE conference in San Jose, California. Intel's 45nm Penryn product was commercially released by November 2007. Upon information and belief, Tela was aware of Intel's well-publicized gridded layout technology. Intel continued to invest in implementing and marketing that technology after November 2007 and through Tela's accusation of infringement and demand for a license in 2014, including in connection with Intel's 22nm and 14nm products.

178. Tela's first patent in the patent family to which the Patents-in-Suit belong, the '352 Patent, issued on November 4, 2008. Tela's second patent in the patent family to which the Patents-in-Suit belong, U.S. Patent No. 7,842,975 ("the '975 Patent") issued on November 30, 2010.

179. Three of the Patents-in-Suit, namely the '966, '012, and '689 Patents, issued in 2011.

180. One of the Patents-in-Suit, namely the '552 Patent, issued in 2012.

181. Intel's 22nm products, which Tela has accused of infringing the Patents-in-Suit, were released by April 2012. Intel invested money and time over the course of several years prior to this release date in developing its 22nm products and related technologies. Intel also continued to invest in implementing and marketing that technology and subsequent technologies after April 2012 leading up to Tela's accusation of infringement and demand for a license in 2014.

182. Intel's work on each of its process nodes and corresponding products is well-publicized.

183. Tela approached Intel in 2014 about licensing patents Tela claimed were not covered by the CNTS.

184. Despite Tela having a business relationship with Intel since 2007, being aware of Intel's gridded layout technology, and having issued patents in the patent family to which the Patents-in-Suit belong since November 2008, Tela remained silent and took no action to approach Intel until almost six years after the '352 patent issued in 2008, three years after the '966, '012, and '689 Patents issued in 2011, and two years after the '552 Patent issued in 2012.

185. Tela's misleading conduct, through silence and inaction with respect to Intel, in view of the relationship and facts noted above, led Intel to reasonably believe that Tela did not intend to enforce the Patents-in-Suit against Intel.

186. Intel relied on Tela's misleading conduct with respect to the Patents-in-Suit and continued to develop and invest in its technology.

187. Based on its reliance, Intel would be materially prejudiced if Tela were permitted to proceed with its allegation of infringement after years of silence and inaction. The prejudice to Intel includes, but is not limited to, Intel's investment (in terms of expense, time, and resources) in the research, development, and marketing of its technology.

188. Intel is entitled to a judgment from this Court that Tela should be barred from asserting infringement against Intel with respect to the ’966, ’012, ’689, ’552, and ’352 Patents due to equitable estoppel.

COUNT X

(Declaratory Judgment of No Infringement Based on Covenant Not To Sue)

189. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

190. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

191. The CNTS between Intel and Tela, which was signed on May 9, 2007, covers Tela patents that claim priority during the term of the CNTS. Thus, the CNTS covers Tela patents with priority dates after May 9, 2007. The CNTS is still in effect.

192. The correct priority dates for the ’966, ’012, ’689, ’552, ’272, ’947, ’334, ’335, and ’523 patents are after May 9, 2007, because none of Tela’s patent applications filed prior to May 9, 2007, provides adequate written description to support Tela’s purported claims of priority before May 9, 2007. For example, as discussed above in Paragraphs 109 through 165, the earliest priority date to which the ’272 Patent is entitled is June 4, 2015, and the earliest priority date to which the ’947, ’334, and ’335 Patents are entitled is May 13, 2015. In addition, each of the ’966, ’012, ’689, ’552, and ’523 Patents are entitled to priority dates after May 9, 2007 because the claims of these patents include language directed to gate electrode levels that “include” linear (or substantially rectangular) features, but the purported priority applications before May 9, 2007 in the chain of each of these patents do not contain such broad language and instead require that “in each layer other than the diffusion region layer 203, ***only*** linear-shaped layout features are allowed.” This restrictive language in the priority applications before May 9, 2007 does not provide adequate support for the broader claim language in

the ’966, ’012, ’689, ’552, and ’523 Patents. Thus, the ’966, 012, ’689, ’552, and ’523 Patents are not entitled to priority before May 9, 2007. Accordingly, the ’966, ’012, ’689, ’552, ’272, ’947, ’334, ’335, and ’523 patents are covered by the CNTS and Tela cannot assert infringement of such patents against Intel with respect to products, processes or methods covered by the CNTS.

193. Intel is entitled to a judgment from this Court that Tela is barred from asserting against Intel infringement of any Patents-in-Suit that have priority dates after May 9, 2007, and, thus, are covered by the CNTS with respect to products, processes or methods covered by the CNTS.

COUNT XI

(Breach of Contract)

194. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

195. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

196. The CNTS between Intel and Tela is a valid and enforceable contract.

197. The CNTS between Intel and Tela was signed on May 9, 2007. Intel has performed under the CNTS, and it is still in effect. Under the CNTS, Tela agreed not to assert against Intel any Tela patent claiming priority during the term of the CNTS.

198. The correct priority dates for the ’966, ’012, ’689, ’552, ’272, ’947, ’334, ’335, and ’523 patents are after May 9, 2007. Accordingly, these patents are covered by the CNTS.

199. Tela breached the CNTS by filing counterclaims in this action and filing an ITC action against Intel asserting infringement of the ’966, ’012, ’334, ’335, and ’523 Patents.

200. Tela’s breach of the CNTS has caused and will continue to cause Intel to suffer substantial damages and irreparable harm for which there is no adequate remedy at law. For example, Intel has suffered damages from Tela’s breach of the CNTS by being forced to incur expenses

defending itself against Tela's wrongful assertion of patents that are covered by the CNTS. If Tela is permitted to maintain its infringement assertions and/or institute new actions based on patents covered by the CNTS, Intel will continue to incur expenses for which damages are not an adequate remedy at law. For example, Tela has brought an ITC action against Intel and several of Intel's customers alleging infringement of patents covered by the CNTS, as detailed in Paragraph 56. If Tela were allowed to maintain its current actions and/or institute new actions in breach of the CNTS, Intel's only remedy would be to sue Tela repeatedly. Intel could incur significant costs in bringing such lawsuits—costs it would not necessarily be able to recover. The prospect of repetitious litigation to hold Tela repeatedly accountable for ongoing and new breaches of the CNTS would cause Intel irreparable harm.

201. Intel is entitled to all monetary damages permitted under applicable law, including but not limited to attorneys' fees and costs, and any other relief that the Court deems just. In addition to monetary damages, Intel is entitled to specific performance of the CNTS, as well as injunctive relief (including but not limited to a temporary restraining order, preliminary injunction, and permanent injunction) prohibiting Tela from instituting or maintaining any litigation barred by the CNTS.

COUNT XII

(Correction of Inventorship)

202. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein.

203. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

204. As discussed in Paragraphs 57 through 66 above, Becker and Malecki wrongfully misappropriated numerous aspects of Professor Pileggi's technology, including those relating to regular layout geometries with unidirectional gridded gate and metal layers. Subsequently, Becker

and Smayling used Professor Pileggi's technology as the core of the claimed subject matter of the Patents-in-Suit.

205. Professor Pileggi thereby contributed in a significant manner to the conception of the Patents-in-Suit. Professor Pileggi's contributions were part of a collaboration and concerted effort in connection with the March 1, 2005 meeting with Becker, where the confidential details of Professor Pileggi's technology were discussed, as well as the months Malecki spent as acting CEO of Fabbrix working closely with Fabbrix, including Professor Pileggi and his technology.

206. Professor Pileggi's technology reflects a contribution to the Patents-in-Suit that is not insignificant in quality. For example, Professor Pileggi's technology applies regular layout geometries with unidirectional gridded gate and metal layers to form regular cells and fabrics. The 2006 Provisional places central emphasis on a solution using "a grid pattern" where layers other than diffusion "should be rectangular in shape and fixed in one dimension." This concept is reflected in the core of the claimed subject matter of the Patents-in-Suit, the claims of which recite:

- '966 Patent: "a gate electrode level layout portion … including a plurality of linear-shaped layout features"; "first interconnect linear conductive structures formed to extend in a linear manner in the first direction"
- '012 Patent: "a gate electrode level layout portion … including a plurality of linear-shaped layout features"; "first interconnect linear[] conductive structures formed to extend in a linear manner in the first direction"
- '689 Patent: "linear layout shape[s] within the gate electrode level region layout"; "a first linear interconnect conductive segment formed to extend lengthwise in the first direction"
- '552 Patent: "at least six linear shapes … in a gate layer region"; "wherein the interconnect layer region includes a second linear interconnect shape … positioned next to and spaced apart from the first linear interconnect shape"

- ’272 Patent: “some of the at least eight conductive structures forming at least one transistor gate electrode … the first edge [and second edge] of each of the at least eight conductive structures is substantially straight”; “the first edge [and second edge] of the first interconnect conductive structure is substantially straight”
- ’947 Patent: “some of the at least eight conductive structures forming at least one transistor gate electrode … the first edge [and second edge] of each of the at least eight conductive structures is substantially straight”; “the first edge [and second edge] of the first interconnect conductive structure is substantially straight”
- ’352 Patent: “linear gate electrode tracks having multiple linear gate electrode segments adjacently defined thereover in an end-to-end manner”; “a plurality of linear conductor tracks defined to extend over the substrate portion in a single common direction within a given interconnect layer”
- ’334 Patent: “the gate structures positioned in accordance with a gate horizontal grid … each gate structure in the region having a substantially rectangular shape”; “first-metal structures positioned in accordance with a first-metal vertical grid … each first-metal structure in the region having a substantially rectangular shape”
- ’335 Patent: “the gate structure layout shapes positioned in accordance with a gate horizontal grid … each gate structure layout shape having a substantially rectangular shape”; “first-metal structure layout shapes positioned in accordance with a first-metal vertical grid … each first-metal structure layout shape having a substantially rectangular shape”
- ’523 Patent: “each gate electrode feature layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise”; “each first-metal structure layout shape in the region having a substantially rectangular shape and positioned to extend lengthwise”

207. Either Professor Pileggi's contributions did more than merely explain to Becker and Smayling well-known concepts and/or the current state of the art; or the subject matter of the asserted patents was well-known in the prior art, rendering them anticipated and/or obvious (*see* Intel's Counterclaims, First through Sixth Counterclaims). At the time of Professor Pileggi's contributions in March through June 2005, and still when The 2006 Provisional was filed in March 2006, Fabbrix had not publicly revealed details behind its technology relating to regular layout geometries with unidirectional gridded gate and metal layers and their application to regular cells and fabrics. For example, U.S. Patent No. 7,278,118, on which Professor Pileggi is a named inventor, was not published until May 25, 2006.

208. For the above reasons, Professor Pileggi is an inventor of the Patents-in-Suit and must be named as such for the Patents-in-Suit not to be invalid under 35 U.S.C. § 102(f).

209. Intel has standing to bring this claim at least because Tela has accused it of infringing the Patents-in-Suit, and Intel has suffered and will continue to suffer injury in fact if Tela is permitted to maintain its accusations despite Intel being licensed by an inventor of the Patents-in-Suit who has not consented to join suit against Intel. Intel has been forced to incur and continues to incur legal costs in pursuing this claim to clear the cloud of uncertainty created by Tela's assertions of patents to which Intel is licensed.

210. Pursuant to 35 U.S.C. § 256, Intel is entitled to a judgment that Professor Pileggi is an inventor of the Patents-in-Suit and an order instructing the Patent Office to correct the Patents-in-Suit to properly include Professor Pileggi as an inventor.

COUNT XIII

(Declaratory Judgment of Unenforceability of the Patents-in-Suit Due to Inequitable Conduct)

211. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference the allegations in Paragraphs 202 through 210 above, with respect to correction of inventorship, as though fully set forth herein.

212. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

213. The Patents-in-Suit are unenforceable due to inequitable conduct that occurred during the prosecution of their respective applications resulting in the issuance of the Patents-in-Suit.

214. Becker and Smayling are named as alleged inventors on the face of each of the Patents-in-Suit and the 2006 Provisional to which they claim priority.

215. In connection with prosecution of the Patents-in-Suit, Becker signed a declaration vouching for the content of the applications, in which he acknowledged his duty to disclose to the Patent Office information known to him to be material to patentability of the claims of the Patents-in-Suit in accordance with 37 C.F.R. § 1.56.

216. This duty of disclosure includes disclosing the true inventors of the subject matter claimed in the Patents-in-Suit. Inventorship is material to patentability under 37 C.F.R. § 1.56.

217. As discussed in Paragraphs 202 through 210 above, Professor Pileggi is an inventor of the Patents-in-Suit. Despite knowing of Professor Pileggi's contributions to the Patents-in-Suit, Becker breached his duty of disclosure by improperly omitting Professor Pileggi as an inventor and failing to disclose Professor Pileggi's contributions to the Patents-in-Suit.

218. Upon information and belief, Becker acted with specific intent to deceive the Patent Office by knowingly and deliberately (i) failing to list Pileggi as a co-inventor in order for Tela to improperly claim ownership of the Patents-in-Suit; (ii) failing to disclose the interactions between Becker, Malecki, and Fabbrix, the information that Becker and Malecki received from Fabbrix, and

the contributions of Professor Pileggi; and (iii) inaccurately representing the claim limitations of the Patents-in-Suit as Becker and Smayling's own work.

219. These facts would have been material to a reasonable examiner's consideration of inventorship. The Patent Office would not have issued the Patents-in-Suit had the Patent Office known about Pileggi's contributions to the Patents-in-Suit. Becker knew this, and his misrepresentations to the Patent Office constitute egregious misconduct and are thus material to patentability by their very nature.

220. But for Becker's conduct described above, the Patent Office would not have issued the Patents-in-Suit.

221. Intel is entitled to a judgment from this Court that the Patents-in-Suit are unenforceable due to inequitable conduct that occurred during their prosecution.

COUNT XIV

(Declaratory Judgment of No Infringement Based on License)

222. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference the allegations in Paragraphs 202 through 210 above, with respect to correction of inventorship, and Paragraphs 211 through 221 above, with respect to inequitable conduct, as though fully set forth herein.

223. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

224. Pursuant to 35 U.S.C. § 256, Intel is entitled to a judgment that Professor Pileggi is an inventor of the Patents-in-Suit and an order instructing the Patent Office to correct the Patents-in-Suit to properly reflect Professor Pileggi as an inventor of the technology claimed in the Patents-in-Suit.

225. Intel does not need a license to the Patents-in-Suit because it does not use them, and instead uses its own semiconductor layout technology that it developed before the Patents-in-Suit were

conceived. Nonetheless, to resolve Tela's allegations in an expeditious and reasonable manner for all parties concerned, Intel entered into a license agreement with Professor Pileggi, an inventor of the Patents-in-Suit, effective February 4, 2019. This license agreement covers the Patents-in-Suit, and licenses Intel under the Patents-in-Suit to make, have made, use, and sell products that would otherwise infringe the Patents-in-Suit. As an inventor who has not assigned his patent rights to any other party, Professor Pileggi has the right to grant Intel this license.

226. Intel is entitled to a judgment from this Court that Tela is barred from asserting against Intel infringement of any Patent-in-Suit to the extent such alleged infringement is covered by Professor Pileggi's license to Intel.

COUNT XV

(Declaratory Judgment of Tela's Lack of Standing to Assert the Patents-in-Suit)

227. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference the allegations in Paragraphs 202 through 210 above, with respect to correction of inventorship, and Paragraphs 211 through 221 above, with respect to inequitable conduct, as though fully set forth herein.

228. An actual and justiciable controversy exists between Intel and Tela concerning the Patents-in-Suit.

229. As discussed in Paragraphs 202 through 210 above, Professor Pileggi is an inventor of the Patents-in-Suit and must be named as such for the Patents-in-Suit not to be invalid under 35 U.S.C. § 102(f).

230. Intel has standing to bring this claim at least because Tela has accused it of infringing the Patents-in-Suit, and Intel has suffered and will continue to suffer injury in fact if Tela is permitted to maintain its accusations despite Intel being licensed by an inventor of the Patents-in-Suit who has not consented to join suit against Intel. Intel has been forced to incur and continues to incur legal costs

in pursuing this DJ action to clear the cloud of uncertainty created by Tela's assertions of patents that it lacks standing to assert.

231. Professor Pileggi is an inventor of the Patents-in-Suit and retains his ownership interest in the Patents-in-Suit, yet has not consented to join Tela in a suit asserting the Patents-in-Suit. For at least that reason, Intel is entitled to a judicial determination and declaration that Tela lacks standing to assert the Patents-in-Suit.

COUNT XVI

(Fraud)

232. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference the allegations in Paragraphs 202 through 210 above, with respect to correction of inventorship, and Paragraphs 211 through 221 above, with respect to inequitable conduct, as though fully set forth herein.

233. As discussed in Paragraphs 67 through 76 above, Tela falsely represented to Intel that it had independently developed its 1D gridded technology; falsely represented that its intellectual property was "clean"; and concealed and failed to disclose that Becker and Malecki had in fact misappropriated the core of Tela's 1D gridded technology from Professor Pileggi.

234. Tela had knowledge of falsity (scienter). On information and belief, Becker (Tela's CEO) and Malecki knew that they had wrongfully misappropriated Professor Pileggi's technology, knew that Tela did not itself develop that technology, knew that Professor Pileggi was a rightful inventor of Tela's 1D gridded family, and nonetheless knowingly and intentionally concealed these facts from Intel via affirmative misrepresentations and nondisclosure.

235. On information and belief, Tela had intent to defraud Intel and induce Intel's reliance. For example, with the aim of securing an investment from Intel, Tela represented to Intel that it had a patent application pending on "[d]ynamic array architecture (1D architecture)," and further

represented that "[w]e believe that patents are the backbone of our company," while failing to disclose to Intel that the technology it was attempting to patent was in fact invented by another. On information and belief, Tela intentionally misrepresented the origin of its 1D gridded technology in order to induce investment from Intel, knowing that had it told the truth, Intel would not have invested in Tela.

236. Intel justifiably relied on Tela's misrepresentations in deciding to invest in Tela. Had Intel known that Tela did not independently develop its core 1D gridded technology, but instead misappropriated it from another, Intel would not have invested in Tela. Intel's reliance on Tela's misrepresentations was justified at least because in connection with the "Full Disclosure" clause of the stock purchase agreement, Tela expressly agreed that it had not provided any untrue statement of material fact or omitted to state a material fact, as discussed in Paragraph 72 above.

237. As a direct and proximate result of Tela fraudulently inducing Intel into investing in Tela, Intel has suffered damages in an amount to be proved at trial. For example, Intel would not have invested in Tela absent Tela's fraud. Further, because Becker and Smayling did not have the experience or history of innovation in 1D gridded technology that Tela touted, Tela's commercial business failed, and the technological and financial value of Intel's investment in Tela was materially reduced.

COUNT XVII

(Violation of California Business and Professions Code § 17200 et seq. (the "UCL"))

238. Intel incorporates by reference the allegations in Paragraphs 1 through 76 above as though fully set forth herein. Intel also incorporates by reference as though fully set forth herein the allegations in Paragraphs 166 through 172, with respect to patent misuse; Paragraphs 189 through 193, with respect to no infringement based on covenant not to sue; Paragraphs 202 through 210, with respect to correction of inventorship; Paragraphs 109 through 165 and 211 through 221, with respect to inequitable conduct; and Paragraphs 232 through 237, with respect to fraud.

239. Tela engaged in fraudulent business acts or practices in violation of the UCL. As set forth above in Paragraphs 232 through 237, Tela deceived and fraudulently induced Intel into investing in Tela by falsely representing to Intel that it had independently developed its 1D gridded technology, when in fact it took that technology from Professor Pileggi. Tela thereby committed fraud and deceit in connection with California Civil Code §§ 1572, 1573, 1709, and 1710; and breached section 2.25 ("Full Disclosure") of the Series B Stock Purchase Agreement at least by failing to disclose to Intel that Tela took the core of its 1D gridded technology from Professor Pileggi. Tela's actions constitute unlawful and unfair business acts or practices under the UCL. Tela has wrongfully asserted its 1D gridded patent portfolio against Intel and other companies within similar sectors of commerce in bad faith, and falsely claimed to members of the public, including potential licensees of the 1D gridded family, that Tela is the rightful owner of the 1D gridded family. Tela did this knowing that its purported rights in the 1D gridded family were wrongfully obtained (as discussed in Paragraphs 211 through 221); that inventorship of the Patents-in-Suit needs to be corrected (as discussed in Paragraphs 202 through 210); and that patents in the 1D gridded family including the '272, '947, '334, and '335 Patents are unenforceable due to inequitable conduct during prosecution (as discussed in Paragraphs 109 through 165 and Paragraphs 211 through 221) and patent misuse (as discussed in Paragraphs 166 through 172).

240. Intel has suffered injury in fact and lost money as a result of Tela's actions at least because Intel would not have invested in Tela absent Tela's fraud and deceit. Further, because Becker and Smayling did not have the experience or history of innovation in 1D gridded technology that Tela touted, Tela's commercial business failed, and the technological and financial value of Intel's investment in Tela was materially diminished. Intel has further suffered injury in fact and lost money by being forced to incur costs in responding to Tela's wrongful conduct, including its bad-faith allegations of patent infringement.

241. Tela's unlawful, unfair, and fraudulent business will continue as long as Tela wrongfully retains rights to the 1D gridded patent portfolio, and therefore presents a continuing threat to the public, Intel, and Intel's customers.

242. Intel is entitled to restitution and an injunction prohibiting Tela from enforcing or receiving any further benefit from the Patents-in-Suit.

PRAYER FOR RELIEF

WHEREFORE, Intel prays for the following judgment and relief:

A. A declaration that Intel has not infringed, and does not infringe, either directly or indirectly, any valid and enforceable claim of the Patents-in-Suit, either literally or under the doctrine of equivalents;

B. A declaration that the Patents-in-Suit are unenforceable;

C. A declaration that Tela is barred from asserting infringement against Intel with respect to the '966, '012, '689, '552, and '352 Patents due to equitable estoppel;

D. A declaration that Intel has not infringed, and does not infringe, the Patents-in-Suit that have priority dates after May 9, 2007 and are covered by the CNTS with respect to products, processes or methods covered by the CNTS;

E. A declaration that Professor Larry Pileggi is an inventor of the Patents-in-Suit and an order to correct the inventorship of the Patents-in-Suit accordingly pursuant to 35 U.S.C. § 256;

F. A declaration that Intel does not infringe the Patents-in-Suit because Intel is licensed by Professor Pileggi;

G. A declaration that Tela lacks standing to assert the Patents-in-Suit;

H. An award of damages to compensate Intel for Tela's breach of the CNTS in an amount to be proven at trial, as well as prejudgment and post-judgment interest;

I. An award of damages to compensate Intel for Tela's fraudulent acts in an amount to be proven at trial, as well as prejudgment and post-judgment interest;

J. An award of restitution for Tela's unlawful, unfair, and/or fraudulent business practices in an amount to be proven at trial, as well as prejudgment and post-judgment interest;

K. An award of exemplary damages pursuant to Cal. Civil Code § 3294 for Tela's fraudulent acts in an amount to be proven at trial, as well as prejudgment and post-judgment interest;

L. An injunction against Tela and its officers, agents, servants, employees, and those persons in active concert or participation with them who receive actual notice of this judgment from directly or indirectly asserting infringement or instituting any action for infringement of the Patents-in-Suit against Intel or any of its customers or suppliers;

M. An order declaring that Intel is the prevailing party and that this case is an exceptional case under 35 U.S.C. § 285, and awarding Intel its costs, expenses, and reasonable attorneys' fees under 35 U.S.C. § 285 and all other applicable statutes, rules and common law, including this Court's inherent authority; and

N. Any other equitable and/or legal relief that this Court may deem just and proper.

JURY TRIAL DEMAND

Pursuant to Federal Rule of Civil Procedure 38, Intel hereby demands a trial by jury on all issues and claims so triable.

DATED: March 15, 2019

Respectfully submitted,

/s/Todd M. Friedman

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