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7 ALTAIR LOGIX LLC, a Texas limited liability corporation

8 **UNITED STATES DISTRICT COURT**
9 **NORTHERN DISTRICT OF CALIFORNIA**

10 **SAN FRANCISCO DIVISION**

11 **ALTAIR LOGIX LLC,**
12 Plaintiff,
13 v.
14 **ADVANTECH CORPORATION,**
15 Defendant.

PATENT

Case No. _____

**ORIGINAL COMPLAINT FOR
PATENT INFRINGEMENT
AGAINST ADVANTECH
CORPORATION**

DEMAND FOR JURY TRIAL

16 Plaintiff Altair Logix LLC files this Original Complaint for Patent Infringement against
17 Advantech Corporation, and would respectfully show the Court as follows:

18 **I. THE PARTIES**

19 1. Plaintiff Altair Logix LLC (“Altair Logix” or “Plaintiff”) is a Texas limited
20 liability company with its principal place of business at 15922 Eldorado Pkwy, Suite 500 #1513,
21 Frisco, TX 75035.

22 2. On information and belief, Defendant Advantech Corporation (“Defendant”) is a
23 corporation organized and existing under the laws of California, with a place of business at 380
24 Fairview Way, Milpitas, CA 95035.
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II. JURISDICTION AND VENUE

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2 3. This action arises under the patent laws of the United States, Title 35 of the
3 United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§
4 1331 and 1338(a).

5
6 4. On information and belief, Defendant is subject to this Court’s specific and
7 general personal jurisdiction, pursuant to due process and the California Long-Arm Statute, due
8 at least to its business in this forum, including at least a portion of the infringements alleged
9 herein. Furthermore, Defendant is subject to this Court’s specific and general personal
10 jurisdiction because Defendant is a California corporation and it has a place of business within
11 this District.

12 5. Without limitation, on information and belief, within this State and this District,
13 Defendant has used the patented inventions thereby committing, and continuing to commit, acts
14 of patent infringement alleged herein. In addition, on information and belief, Defendant has
15 derived revenues from its infringing acts occurring within California and the Northern District of
16 California. Further, on information and belief, Defendant is subject to the Court’s general
17 jurisdiction, including from regularly doing or soliciting business, engaging in other persistent
18 courses of conduct, and deriving substantial revenue from goods and services provided to
19 persons or entities in California and the Northern District of California. Further, on information
20 and belief, Defendant is subject to the Court’s personal jurisdiction at least due to its sale of
21 products and/or services within California and the Northern District of California. Defendant has
22 committed such purposeful acts and/or transactions in California and the Northern District of
23 California such that it reasonably should know and expect that it could be haled into this Court as
24 a consequence of such activity.
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1 (Ex. A at col. 1:32-38). The object of the invention is to provide a new method and apparatus for
2 implementing systems on silicon or other chip material which will enable the user a means for
3 achieving the performance of fixed-function implementations at a lower cost. (*Id.* at col. 2:64 –
4 col. 3:1).

5
6 13. The most common method of implementing various functions on an integrated
7 circuit is by specifically designing the function or functions to be performed by placing on
8 silicon an interconnected group of digital circuits in a non-modifiable manner (hard-wired or
9 fixed function implementation). (*Id.* at col. 1:42-47). These circuits are designed to provide the
10 fastest possible operation of the circuit in the least amount of silicon area. (*Id.* at col. 1:47-49).
11 In general, these circuits are made up of an interconnection of various amounts of random-access
12 memory and logic circuits. (*Id.* at col. 1:49-51). Complex systems on silicon are broken up into
13 separate blocks and each block is designed separately to only perform the function that it was
14 intended to do. (*Id.* at col. 1:51-54). Each block has to be individually tested and validated, and
15 then the whole system has to be tested to make sure that the constituent parts work together. (*Id.*
16 at col. 1:54-56). This process is becoming increasingly complex as we move into future
17 generations of single-chip system implementations. (*Id.* at col. 1:57-59). Systems implemented
18 in this way generally tend to be the highest performing systems since each block in the system
19 has been individually tuned to provide the expected level of performance. (*Id.* at col. 1:59-62).
20 This method of implementation may be the smallest (cheapest in terms of silicon area) method
21 when compared to three other distinct ways of implementing such systems. (*Id.* at col. 1:62-65).
22 Each of the other three have their problems and generally do not tend to be the most cost-
23 effective solution. (*Id.* at col. 1:65-67).

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26 14. The first way is implemented in software using a microprocessor and associated
27 computing system, which can be used to functionally implement any system. (*Id.* at col. 2:1-2).
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1 However, such systems would not be able to deliver real-time performance in a cost-effective
2 manner for the class of applications that was described above. (*Id.* at col. 2:3-5). Their use is
3 best for modeling the subsequent hard-wired/fixed-function system before considerable design
4 effort is put into the system design. (*Id.* at col. 2:5-8).

5
6 15. The second way of implementing such systems is by using an ordinary digital
7 signal processor (DSP). (*Id.* at col. 2:9-10). This class of computing machines is useful for real-
8 time processing of certain speech, audio, video and image processing problems and in certain
9 control functions. (*Id.* at col. 2:10-13). However, they are not cost-effective when it comes to
10 performing certain real time tasks which do not have a high degree of parallelism in them or
11 tasks that require multiple parallel threads of operation such as three-dimensional graphics. (*Id.*
12 at col. 2:13-17).

13
14 16. The third way of implementing such systems is by using field programmable gate
15 arrays (FPGA). (*Id.* at col. 2:18-19). These devices are made up of a two-dimensional array of
16 fine grained logic and storage elements which can be connected together in the field by
17 downloading a configuration stream which essentially routes signals between these elements.
18 (*Id.* at col. 2:19-23). This routing of the data is performed by pass-transistor logic. (*Id.* at col.
19 2:24-25). FPGAs are by far the most flexible of the three methods mentioned. (*Id.* at col. 2:25-
20 26). The problem with trying to implement complex real-time systems with FPGAs is that
21 although there is a greater flexibility for optimizing the silicon usage in such devices, the
22 designer has to trade it off for increase in cost and decrease in performance. (*Id.* at col. 2:26-30).
23 The performance may (in some cases) be increased considerably at a significant cost, but still
24 would not match the performance of hard-wired fixed function devices. (*Id.* at col. 2:30-33).
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1 17. These three ways do not reduce the cost or increase the performance over fixed-
2 function systems. (*Id.* at col. 2:35-37). In terms of performance, fixed-function systems still
3 outperform the three ways for the same cost. (*Id.* at col. 2:37-39).

4 18. The three systems can theoretically reduce cost by removing redundancy from the
5 system. (*Id.* at col. 2:40-41). Redundancy is removed by re-using computational blocks and
6 memory. (*Id.* at col. 2:41-42). The only problem is that these systems themselves are
7 increasingly complex, and therefore, their computational density when compared with fixed-
8 function devices is very high. (*Id.* at col. 2:42-45).

9 19. Most systems on silicon are built up of complex blocks of functions that have
10 varying data bandwidth and computational requirements. (*Id.* at col. 2:46-48). As data and
11 control information moves through the system, the processing bandwidth varies enormously.
12 (*Id.* at col. 2:48-50). Regardless of the fact that the bandwidth varies, fixed-function systems
13 have logic blocks that exhibit a “temporal redundancy” that can be exploited to drastically reduce
14 the cost of the system. (*Id.* at col. 2:50-53). This is true, because in fixed function
15 implementations all possible functional requirements of the necessary data processing must be
16 implemented on the silicon regardless of the final application of the device or the nature of the
17 data to be processed. (*Id.* at col. 2:53-57). Therefore, if a fixed function device must adaptively
18 process data, then it must commit silicon resources to process all possible flavors of the data.
19 (*Id.* at col. 2:58-60). Furthermore, state-variable storage in all fixed function systems are
20 implemented using area inefficient storage elements such as latches and flip-flops. (*Id.* at col.
21 2:60-63).

22 20. The inventors therefore sought to provide a new apparatus for implementing
23 systems on a chip that will enable the user to achieve performance of fixed-function
24 implementation at a lower cost. (*Id.* at col. 2:64 – col. 3:1). The lower cost is achieved by
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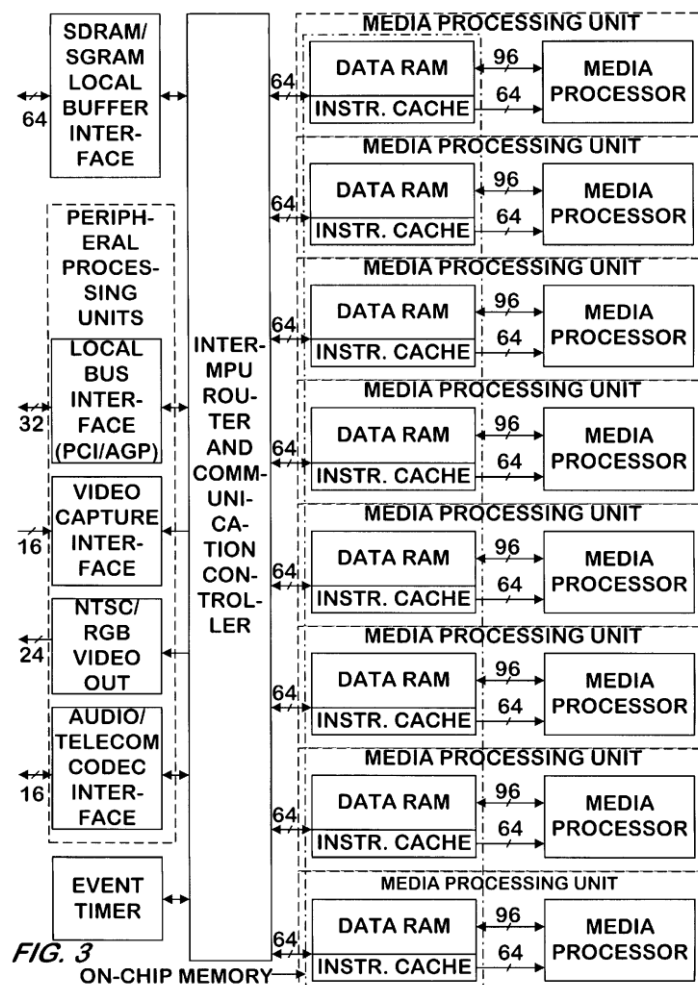
1 removing redundancy from the system. (*Id.* at col. 3:1-2). The redundancy is removed by re-
2 using groups of computational and storage elements in different configurations. (*Id.* at col. 3:2-
3 4). The cost is further reduced by employing only static or dynamic ram as a means for holding
4 the state of the system. (*Id.* at col. 3:4-6). This invention provides a way for effectively adapting
5 the configuration of the circuit to varying input data and processing requirements. (*Id.* at col. 3:6-
6 8). All of this reconfiguration can take place dynamically in run-time without any degradation of
7 performance over fixed-function implementations. (*Id.* at col. 3:8-11).

9 21. The present invention is therefore an apparatus for adaptively dynamically
10 reconfiguring groups of computations and storage elements in run-time to process multiple
11 separate streams of data and control at varying rates. (*Id.* at col. 3:14-18). The '434 patent refers
12 to the aggregate of the dynamically reconfigurable computational and storage elements as a
13 "media processing unit."

14 22. The claimed apparatus has addressable memory for storing data and a plurality of
15 instructions that can be provided through a plurality of inputs/outputs that is couple to the
16 input/output of a plurality of media processing units. (*Id.* at col. 55:21-30). The media
17 processing unit comprises a multiplier, an arithmetic unit, and arithmetic logic unit and a bit
18 manipulation unit. (*Id.* at col. 55:31 – col. 56:20). The '434 patent provides examples to explain
19 each of the parts of the media processing unit. (*Id.* at col. 16:27-61 (multiplier and adder); *Id.* at
20 col. 16:62 – col. 17:1-9 (arithmetic logic unit); and *Id.* at col. 17:10 – col. 17:43 (bit
21 manipulation unit)). Each of the parts has a data input coupled to the media processing unit
22 input/output, an instruction input coupled to the mediate processing unit input/output, and a data
23 output coupled to the mediate processing unit input/output. (*Id.* at col. 55:31 – col. 56:20).
24 Furthermore, the arithmetic logic unit must be capable of operating concurrently with either the
25 multiplier and arithmetic unit. (*Id.* at col. 56:6-12). And the bit manipulation unit must be
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1 capable of operating concurrently with the arithmetic logic unit and at least either the multiplier
 2 or the arithmetic unit. (*Id.* at col. 56:13-20). Each of the plurality of media processing units
 3 must be capable of performing an operating simultaneously with the performance of other
 4 operations by other media processing units. (*Id.* at col. 56:21-24). An operation comprises the
 5 media processing unit receiving an instruction and data from memory, processing the data
 6 responsive to the instruction to produce a result, and providing the result to the media processor
 7 input/output. (*Id.* at col. 56:26-33).

9 23. An exemplary block diagram of the claimed systems is shown in Figure 3 of the
 10 '434 patent:



1 (*Id.* at Fig. 3). Exemplary architecture and coding for the apparatus is disclosed in the ‘599
2 patent. (*E.g.*, *Id.* at col. 16:15 – col. 52:20; Figs. 9 – 106).

3 24. As further demonstrated by the prosecution history of the ‘434 patent, the claimed
4 invention in the ‘434 patent was unconventional. Claim 1 of the ‘434 patent was an originally
5 filed claim that issued without any amendment. There was no rejection in the prosecution
6 history contending that claim 1 was anticipated by any prior art.
7

8 25. A key element behind the invention is one of reconfigurability and reusability.
9 (*Id.* at col. 13:26-27). Each apparatus is therefore made up of very high-speed core elements that
10 on a pipelined basis can be configured to form a more complex function. (*Id.* at col. 13:27-30).
11 This leads to a lower gate count, thereby giving a smaller die size and ultimately a lower cost.
12 (*Id.* at col. 13:30-31). Since the apparatuses are virtually identical to each other, writing software
13 becomes very easy. (*Id.* at col. 13:32-33). The RISC-like nature of each of the media processing
14 units also allows for a consistent hardware platform for simple operating system and driver
15 development. (*Id.* at col. 13:33-36). Any one of the media processing units can take on a
16 supervisory role and act as a central controller if necessary. (*Id.* at col. 13:36-37). This can be
17 very useful in set top applications where a controlling CPU may not be necessary, further
18 reducing system cost. (*Id.* at col. 13:37-40). The claimed apparatus is therefore an
19 unconventional way of implementing processors that can achieve the performance of fixed-
20 function implementations at a lower cost. (*Id.* at col. 2:64 – col. 3:11).
21

22 26. **Direct Infringement.** Upon information and belief, Defendant has been directly
23 infringing claims of the ‘434 patent in California and the Northern District of California, and
24 elsewhere in the United States, by making, using, selling, and/or offering for sale an apparatus
25 for processing data for media processing that satisfies each and every limitation of at least claim
26 1, including without limitation the DMS-BA16 tablet (“Accused Instrumentality”). (*E.g.*,
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1 https://www.advantech.com/products/medical_computing_system/dms-ba16/mod_64aa1566-
 2 [169c-483d-97c8-c2c22c163fc3;](https://www.advantech.com/products/medical-computing-) <https://www.advantech.com/products/medical-computing->
 3 [platforms/sub_medical_computing_platforms;](https://www.advantech.com/products/medical-) [computing-system/sub_medical_computing_system;](https://www.advantech.com/products/medical-

 4 <a href=) [and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-](https://www.nxp.com/products/processors-

 5 <a href=)
 6 [processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-](https://www.nxp.com/products/processors-)
 7 [core:i.MX6Q\).](https://www.nxp.com/products/processors-)

9 27. The Accused Instrumentality comprises an addressable memory (*e.g.*, memory
 10 system of the Accused Instrumentality) for storing the data, and a plurality of instructions, and
 11 having a plurality of input/outputs, each said input/output for providing and receiving at least one
 12 selected from the data and the instructions. As shown below, the Accused Instrumentality
 13 comprises a memory system which is coupled to multicore ARM processors through multiple
 14 internal inputs/outputs. The memory system provides instructions and stored data for processing
 15 and receives processed data.

- 17 ▼ Memory
 - 18 ■ DDR
 - 19 ■ 2x32 LP-DDR2, 1x64 DDR3 / LV-DDR3
 - 20 ■ NAND
 - 21 ■ SLC/MLC, 40-bit ECC, ONFI2.2, DDR

22 ▶ Connectivity

23 ▶ Display

24 ▶ Advanced Power Management

25 ▶ Security

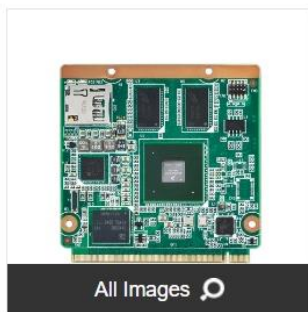
26 ▶ Package and Temperature

(E.g., <https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q>).

28. The Accused Instrumentality comprises a plurality of media processing units (e.g., ARM cortex A9 Dual/Quad Core processors), each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs. As shown below, the Accused Instrumentality comprises ARM cortex A9 Dual/Quad Core processors, each processor comprises a NEON media coprocessor and acts as a media processing unit. The ARM processors are coupled to the memory system. The processors receive instructions and data from the memory system by multiple internal inputs and provides processed data to the memory system by multiple internal outputs.

DMS-BA16

Freescale™ ARM Cortex-A9 i.MX6 Qseven V2.0 Module



- Freescale ARM Cortex-A9 i.MX6 Dual/Quad Core 1 GHz high performance processor
- Up to 2GB Onboard DDR3 Memory; Up to 32GB Onboard eMMC NAND Flash
- Supports OpenGL ES 2.0 and OpenVG 1.1
- HDMI, 24-bit LVDS
- 1x UART, 2x I2C, 8x GPIO, 4x Host USB 2.0 port, 1x USB OTG port, 1x micro SD (SDHC), 1x SDIO, 1x SATA II, 1x 10/100/1000 Mbps Ethernet, 1x PCIe X1 Gen1

Datasheet (PDF)

Technical Documents

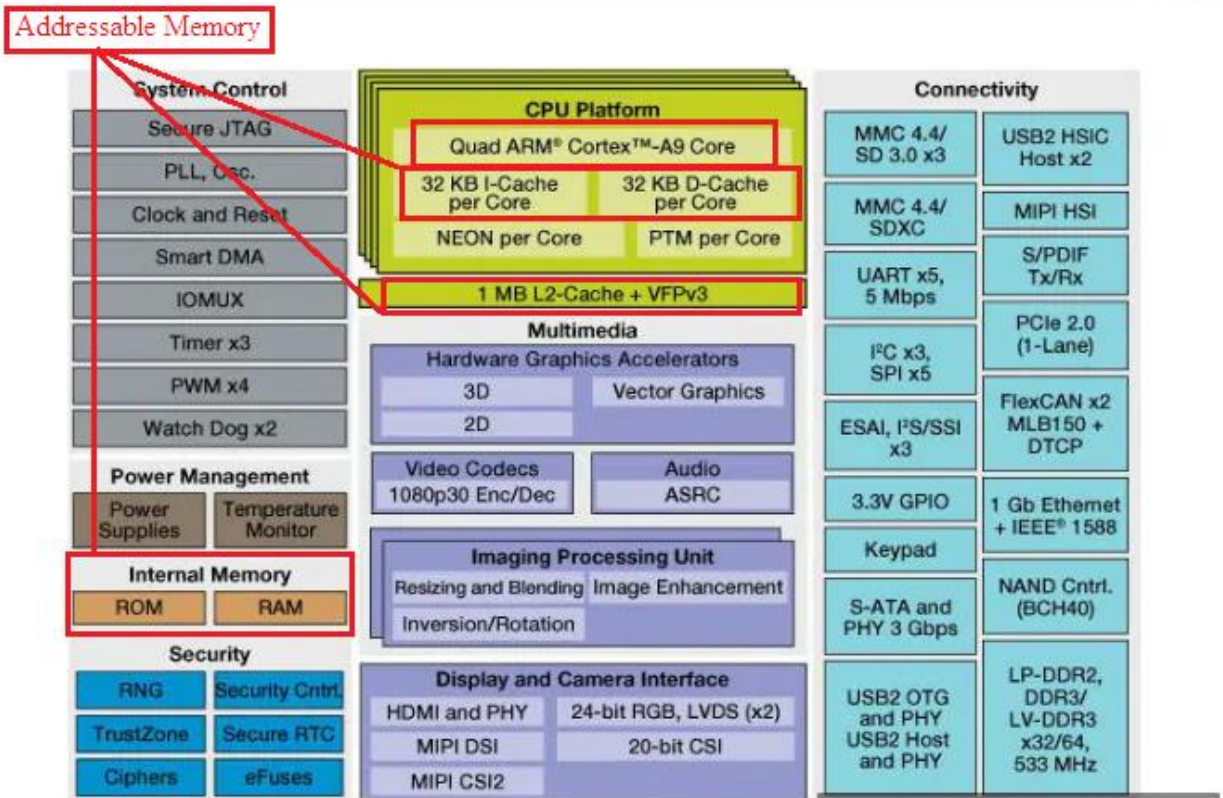
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All Images

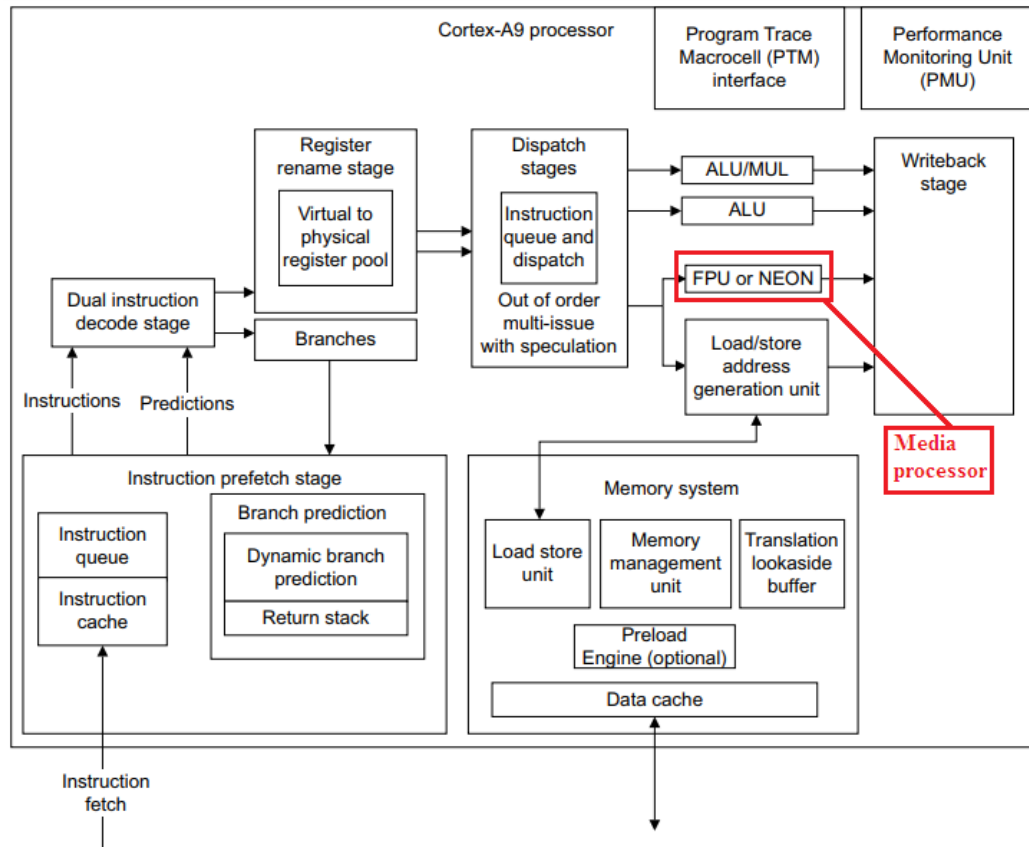
Advantech DMS-BA16 Qseven module is designed with Freescale ARM Cortex-A9 i.MX6 dual-core/Quad-core processor for faster and more robust applications. With up to 2GB memory and 32GB eMMC NAND flash, it offers optimized performance with ultra-low power consumption. DMS-BA16... More

(e.g., https://www.advantech.com/products/medical_computing_system/dms-ba16/mod_64aa1566-169c-483d-97c8-c2c22c163fc3).

i.MX 6Quad Multimedia Applications Processor Block Diagram



(e.g., <https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q>).



(E.g.,

http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388f/DDI0388F_cortex_a9_r2p2_trm.pdf

).

Background

The NEON subsystem is an advanced SIMD (Single Instruction, Multiple Data) processing unit. This means that it can apply a single type of instruction to many pieces of data at one time in parallel. This is extremely helpful when it comes to media processing such as audio/video filters and codecs.

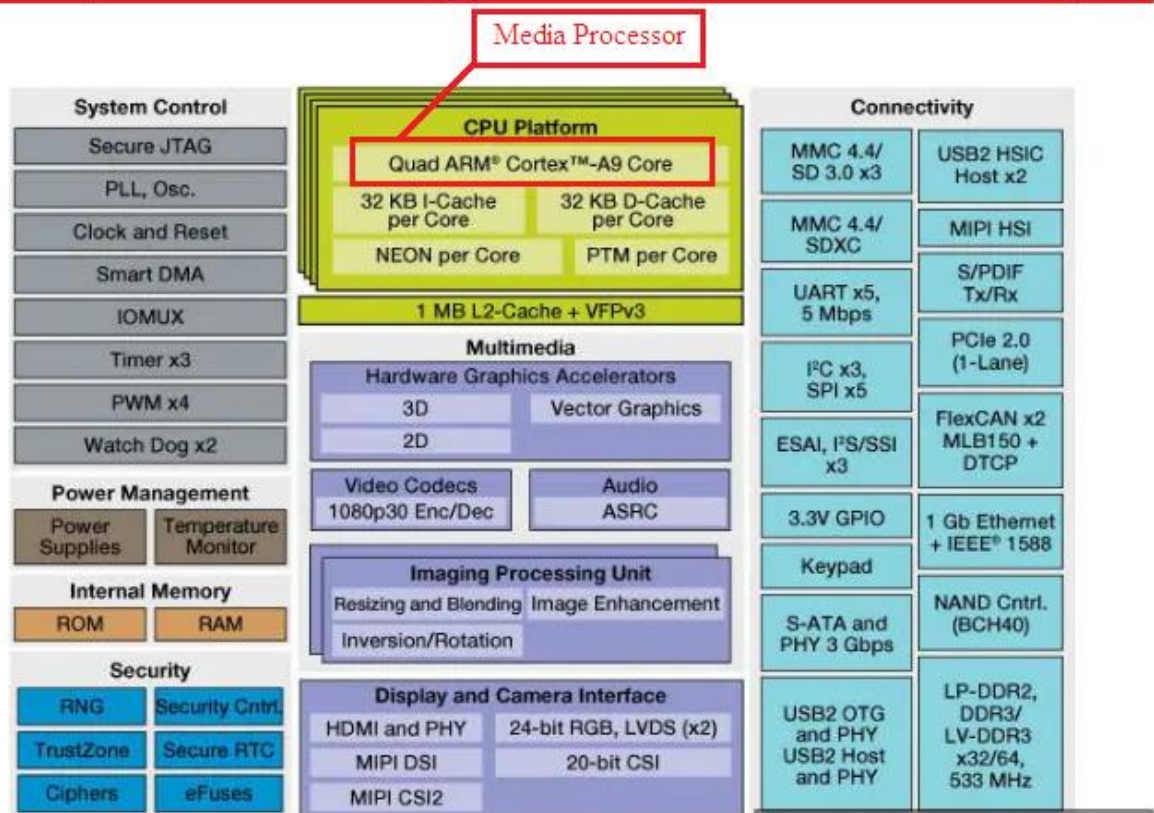
The NEON system is NOT the floating point unit of the ARM processor. There is separate FPU known as the VFP system. They use the same register space but this is taken care of by the compiler/kernel. There are a few differences between the NEON and VFP systems such as: NEON does not support double-precision floating point numbers, NEON only works on vectors and does not support advanced operations such as square root and divide.

(e.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

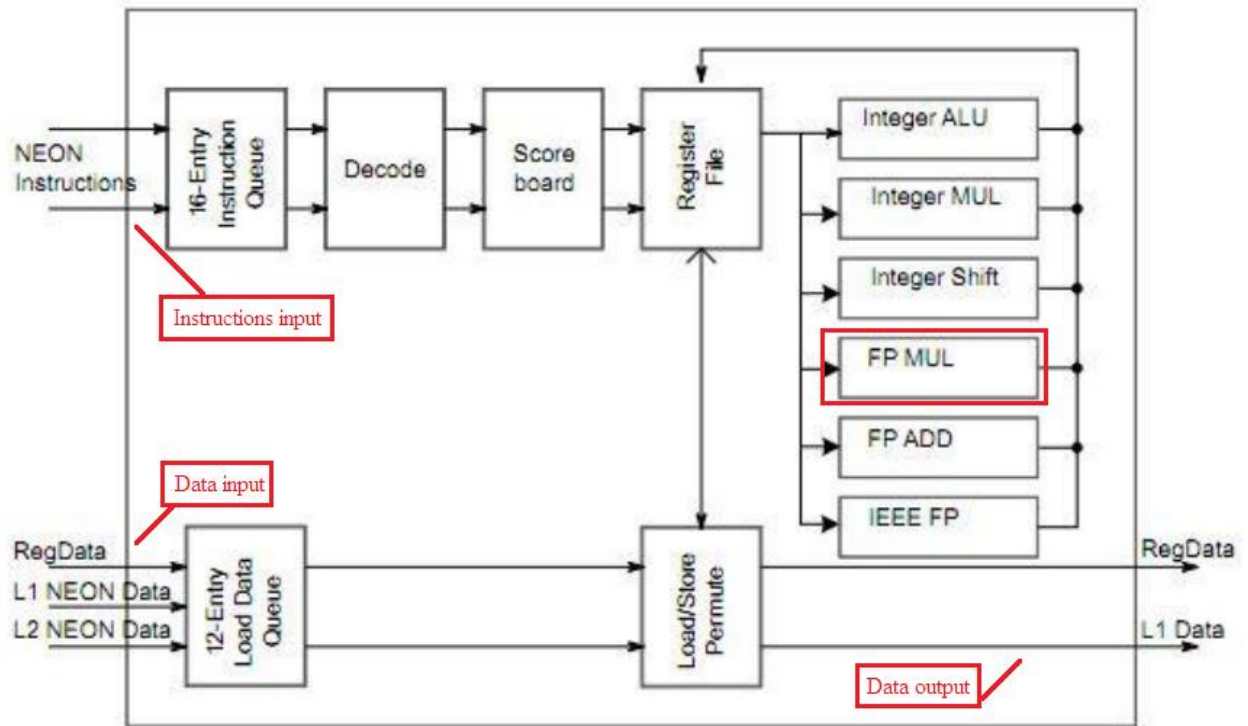
29. The Accused Instrumentality comprises media processors with each processor comprising a multiplier (e.g., an Integer MUL or FP MUL) having a data input coupled to the

1 media processing unit input/output, an instruction input coupled to the media processing unit
 2 input/output, and a data output coupled to the media processing unit input/output. As shown
 3 below, the Accused Instrumentality comprises multiple ARM cortex-A9 Dual/Quad core
 4 processor, each processor comprises a NEON media coprocessor and acts as a media processing
 5 unit. NEON media coprocessor comprises a multiplier which is coupled to the inputs/outputs of
 6 the processor. Upon information and belief, the multiplier comprises a data input, an instruction
 7 input, and a data output coupled to the input/output of the processor.

9 i.MX 6Quad Multimedia Applications Processor Block Diagram

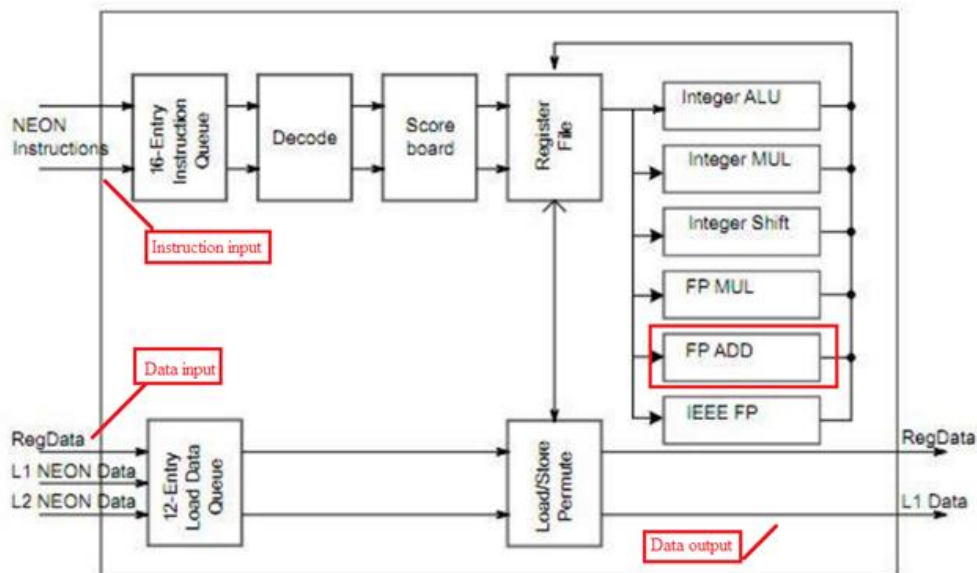


23 (e.g., [https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-](https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q)
 24 [mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-](https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q)
 25 [3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q](https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q)).



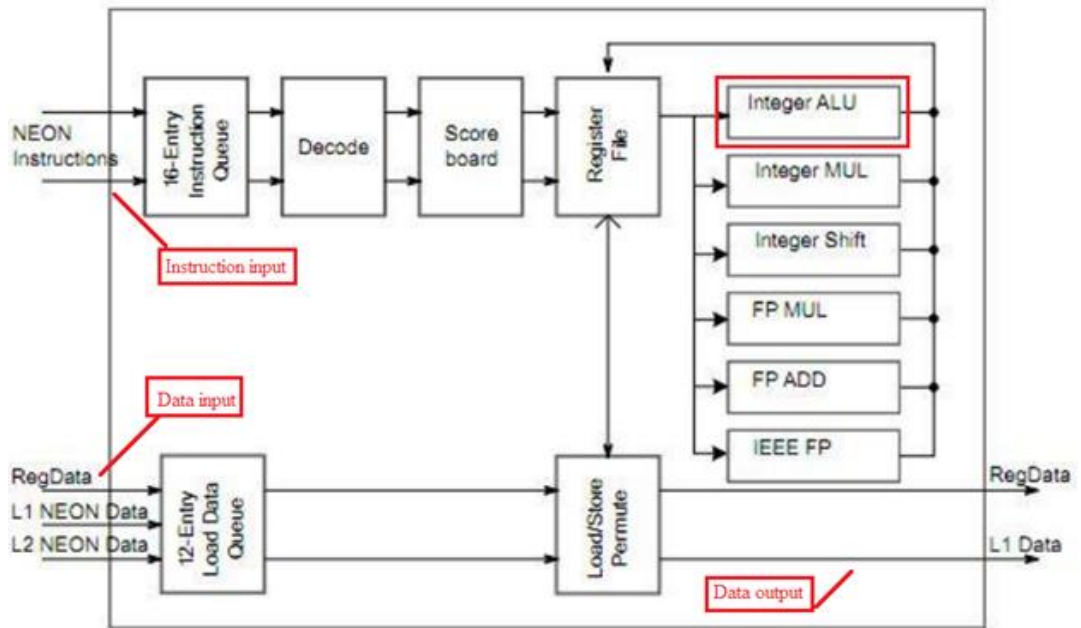
(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

30. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic unit (e.g., an FP ADD) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output. As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 Dual/Quad core processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor.



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

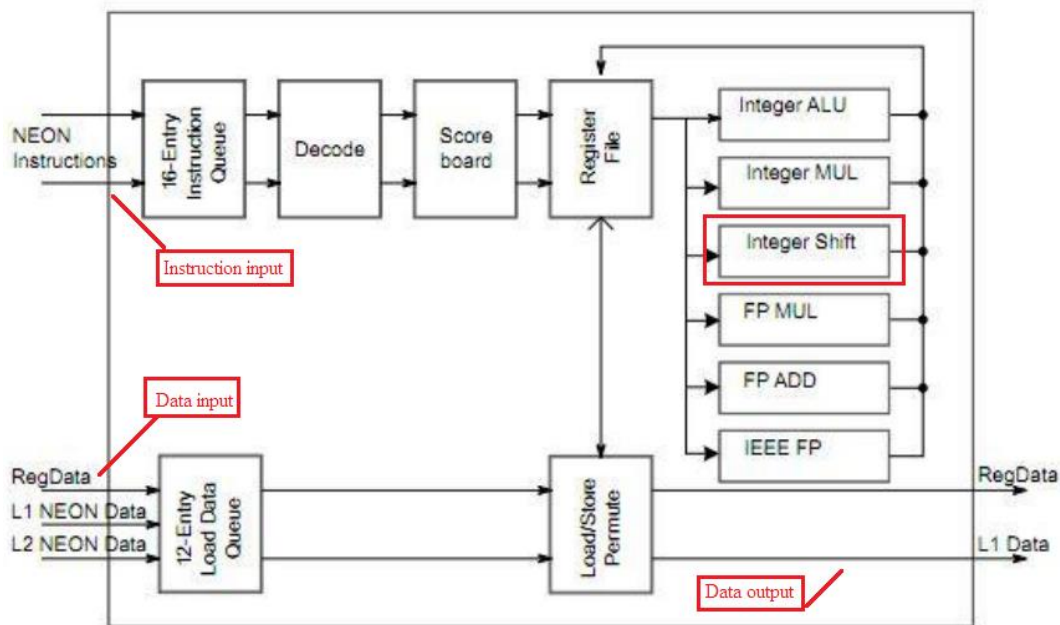
31. The Accused Instrumentality comprises media processors with each processor comprising an arithmetic logic unit (e.g., an ALU) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with at least one selected from the multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 Dual/Quad core processor, each processor comprises a NEON media coprocessor and acts as a media processing unit. NEON media coprocessor comprises an arithmetic logical unit which is coupled to the inputs/outputs of the processor. Upon information and belief, the arithmetic logical unit comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the arithmetic logical unit (e.g., the Integer ALU) is capable of operating concurrently with at least one selected from the multiplier (e.g., the Integer MUL or FP MUL) and arithmetic unit (e.g., the FP ADD).



(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

32. The Accused Instrumentality comprises media processors with each processor comprising a bit manipulation unit (e.g., an Integer Shift unit) having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with the arithmetic logic unit (e.g., an Integer ALU) and at least one selected from the multiplier (e.g., an Integer MUL or FP MUL) and arithmetic unit (e.g., a FP ADD). As shown below, the Accused Instrumentality comprises multiple ARM cortex-A9 Dual/Quad core processors, each processor comprising a NEON media coprocessor that acts as a media processing unit. The NEON media coprocessor comprises an integer shift unit (i.e., bit manipulation unit) which is coupled to the inputs/outputs of the processor. Upon information and belief, the integer shift unit (i.e., bit manipulation unit) comprises a data input, an instruction input, and a data output coupled to the input/output of the processor. Upon information and belief, the integer shift unit (i.e., bit manipulation unit) is capable of operating concurrently with

1 the arithmetic logic unit (e.g., the Integer ALU) and at least one selected from the multiplier
 2 (e.g., the Integer MUL or FP MUL) and arithmetic unit (e.g., the FP ADD).

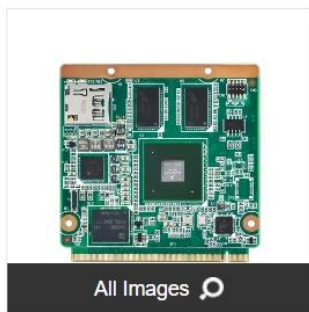


13
 14 (E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

15 33. The Accused Instrumentality comprises a plurality of media processors (e.g.,
 16 ARM cortex-A9 Dual/Quad core processors) for performing at least one operation,
 17 simultaneously with the performance of other operations by other media processing units (e.g.,
 18 other ARM cortex-A9 Dual/Quad core processors on the same chip).

19
 20 **DMS-BA16**

Freescale™ ARM Cortex-A9 i.MX6 Qseven V2.0 Module



- Freescale ARM Cortex-A9 i.MX6 Dual/Quad Core 1 GHz high performance processor
- Up to 2GB Onboard DDR3 Memory; Up to 32GB Onboard eMMC NAND Flash
- Supports OpenGL ES 2.0 and OpenVG 1.1
- HDMI, 24-bit LVDS
- 1x UART, 2x I2C, 8x GPIO, 4x Host USB 2.0 port, 1x USB OTG port, 1x micro SD (SDHC), 1x SDIO, 1x SATA II, 1x 10/100/1000 Mbps Ethernet, 1x PCIe X1 Gen1

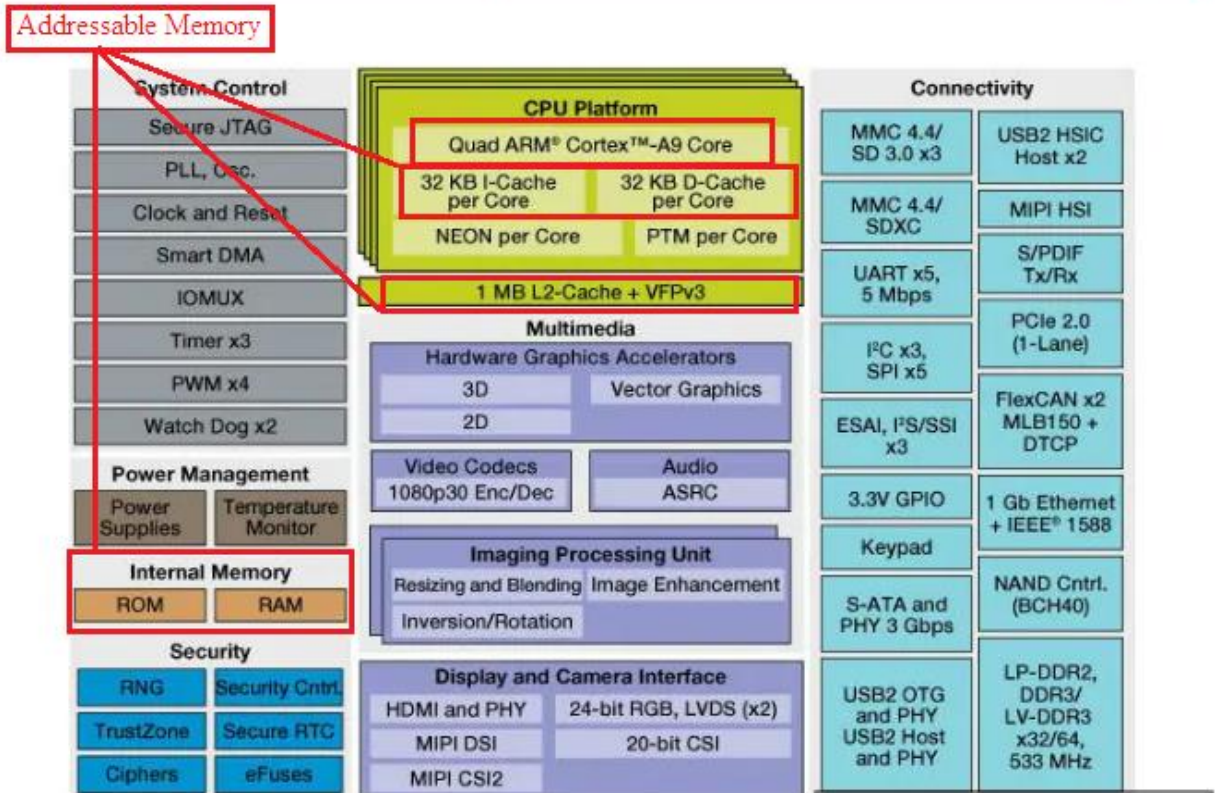
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Advantech DMS-BA16 Qseven module is designed with Freescale ARM Cortex-A9 i.MX6 dual-core/Quad-core processor for faster and more robust applications. With up to 2GB memory and 32GB eMMC NAND flash, it offers optimized performance with ultra-low power consumption. DMS-BA16... More

(e.g., https://www.advantech.com/products/medical_computing_system/dms-ba16/mod_64aa1566-169c-483d-97c8-c2c22c163fc3).

i.MX 6Quad Multimedia Applications Processor Block Diagram



(E.g., <https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q>).

Background

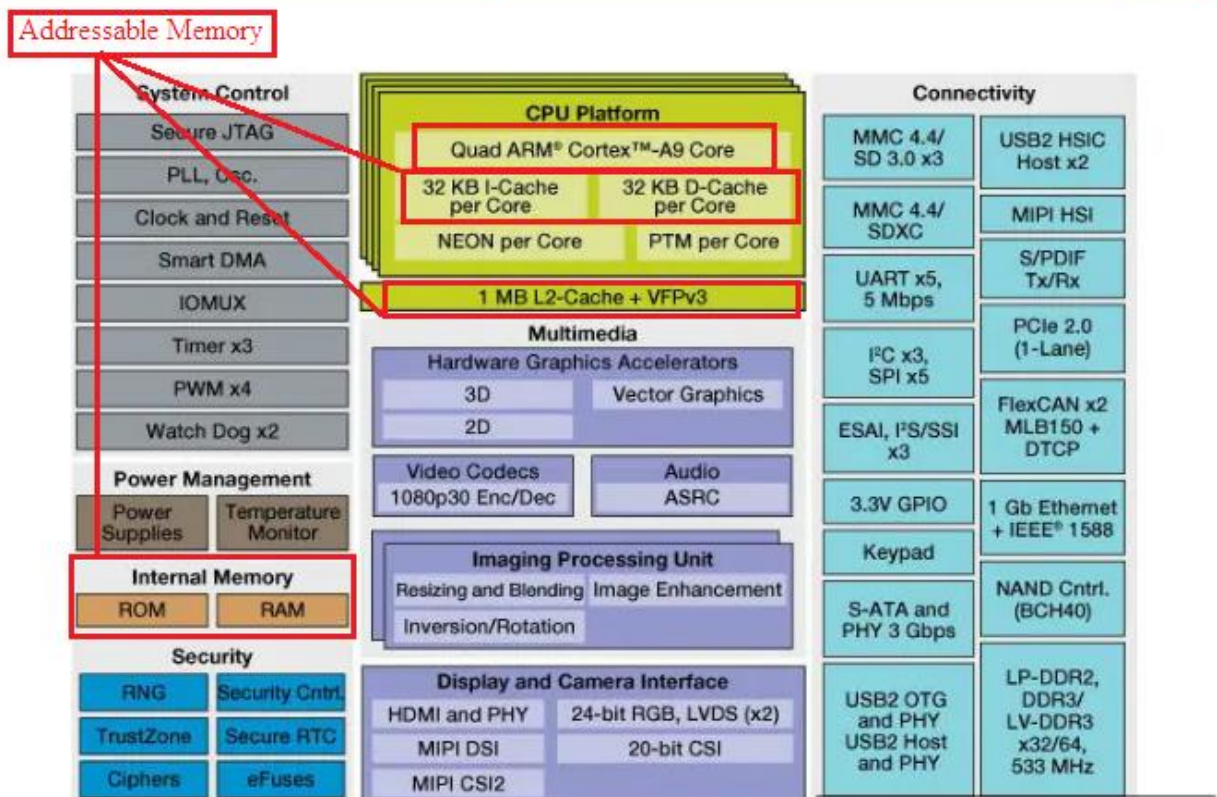
The NEON subsystem is an advanced SIMD (Single Instruction, Multiple Data) processing unit. This means that it can apply a single type of instruction to many pieces of data at one time in parallel. This is extremely helpful when it comes to media processing such as audio/video filters and codecs.

The NEON system is NOT the floating point unit of the ARM processor. There is separate FPU known as the VFP system. They use the same register space but this is taken care of by the compiler/kernel. There are a few differences between the NEON and VFP systems such as: NEON does not support double-precision floating point numbers, NEON only works on vectors and does not support advanced operations such as square root and divide.

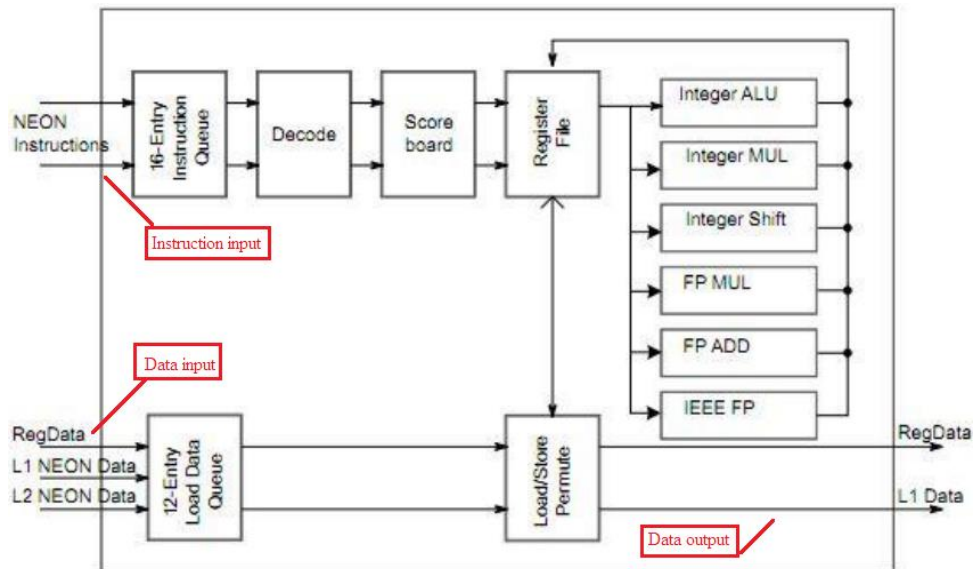
(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

34. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A9 Dual/Quad core processors), each processor receiving at the media processor input/output an instruction and data from the memory, and processing the data responsive to the instruction received to produce at least one result. As shown below, each ARM cortex-A9 Dual/Quad core media processor comprises a NEON media coprocessor which receives instructions and data from memory and processes the data responsive to the instruction received in order to produce a result.

i.MX 6Quad Multimedia Applications Processor Block Diagram



(E.g., <https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q>).

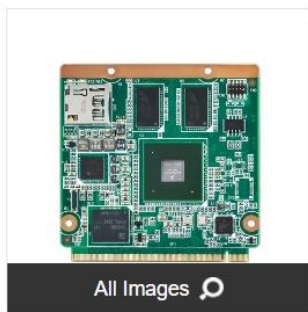


(E.g., <http://www.add.ece.ufl.edu/4924/docs/arm/ARM%20NEON%20Development.pdf>).

35. The Accused Instrumentality comprises a plurality of media processors (e.g., ARM cortex-A9 Dual/Quad core processors), each processor providing at least one of the at least one result at the media processor input/output. (*Supra* ¶34).

DMS-BA16

Freescale™ ARM Cortex-A9 i.MX6 Qseven V2.0 Module



- Freescale ARM Cortex-A9 i.MX6 Dual/Quad Core 1 GHz high performance processor
- Up to 2GB Onboard DDR3 Memory; Up to 32GB Onboard eMMC NAND Flash
- Supports OpenGL ES 2.0 and OpenVG 1.1
- HDMI, 24-bit LVDS
- 1x UART, 2x I2C, 8x GPIO, 4x Host USB 2.0 port, 1x USB OTG port, 1x micro SD (SDHC), 1x SDIO, 1x SATA II, 1x 10/100/1000 Mbps Ethernet, 1x PCIe X1 Gen1

Datasheet (PDF)

Technical Documents

Get Quote

Advantech DMS-BA16 Qseven module is designed with Freescale ARM Cortex-A9 i.MX6 dual-core/Quad-core processor for faster and more robust applications. With up to 2GB memory and 32GB eMMC NAND flash, it offers optimized performance with ultra-low power consumption. DMS-BA16... More

(E.g., https://www.advantech.com/products/medical_computing_system/dms-ba16/mod_64aa1566-169c-483d-97c8-c2c22c163fc3).

Overview

The i.MX 6 series of applications processors combines scalable platforms with broad levels of integration and power-efficient processing capabilities particularly suited to multimedia applications. The i.MX6 Quad processor features:

- Enhanced capabilities of high-tier portable applications by fulfilling MIPS needs of operations systems and games
- Multilevel memory system
- Smart speed technology that enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations
- Dynamic voltage and frequency scaling
- Powerful graphics acceleration
- Interface flexibility
- Integrated power management throughout the device
- Advanced hardware-enabled security

[Professional Services >](#)

(E.g., <https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-6-processors/i.mx-6quad-processors-high-performance-3d-graphics-hd-video-arm-cortex-a9-core:i.MX6Q>).

36. Plaintiff has been damaged as a result of Defendant's infringing conduct. Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '434 patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

37. On information and belief, Defendant has had at least constructive notice of the '434 patent by operation of law, and there are no marking requirements that have not been complied with.

Features

▶ CPU Complex

▼ Multimedia

- GPU 3D
 - Vivante GC2000
 - 200Mtri/s 1000Mpxl/s, OpenGL ES 3.0 and Halti, CL EP
- GPU 2D(Vector Graphics)
 - Vivante GC355
 - 300Mpxl/s, OpenVG 1.1
- GPU 2D(Composition)
 - Vivante GC320
 - 600Mpxl/s, BLIT
- Video Decode
 - 1080p 60 h.264
- Video Encode
 - 1080p30 H.264 BP/ Dual 720p encode
- Camera Interface
 - Types: 1x 20-bit parallel, MIPI-CSI2 (4 lanes), three simultaneous inputs

IV. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

- a. Judgment that one or more claims of United States Patent No. 6,289,434 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;
- b. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein, and an accounting of all infringements and damages not presented at trial;
- c. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein;
- d. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

March 27, 2019

By /s/Steven A. Nielsen

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Attorneys for Plaintiff Altair Logix LLC

JURY DEMAND

1
2 Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of
3 any issues so triable by right.
4

5 March 27, 2019

By /s/Steven A. Nielsen

6
7 OF COUNSEL:

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