IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	C.A. No. 6:19-cv-00255 **JURY TRIAL DEMANDED**

VLSI TECHNOLOGY LLC'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff VLSI Technology LLC ("VLSI"), by and through its undersigned counsel, pleads the following against Intel Corporation ("Intel") and alleges as follows:

THE PARTIES

1. Plaintiff VLSI is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of VLSI is Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801. The name of VLSI's registered agent at that address is The Corporation Trust Company.

2. VLSI is the assignee and owns all right, title, and interest to U.S. Patent Nos. 6,366,522 ("the '522 Patent") and 6,633,187 ("the '187 Patent") (collectively, the "Asserted Patents").

3. On information and belief, Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business in the Western District of Texas, including at 1300 S. Mopac Expressway, Austin, Texas 78746.[1]

JURISDICTION AND VENUE

4. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over Intel because Intel manufactures products that are and have been used, offered for sale, sold, and purchased in the Western District of Texas, and Intel has committed, and continues to commit, acts of infringement in the Western District of Texas, has conducted business in the Western District of Texas, and/or has engaged in continuous and systematic activities in the Western District of Texas.

6. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this judicial district because Intel maintains a regular and established place of business in this district and has committed acts of infringement within this judicial district giving rise to this action.

[1] https://www.intel.com/content/www/us/en/location/usa.html; https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html.

FIRST CLAIM

(Infringement of U.S. Patent No. 6,366,522)

7. VLSI re-alleges and incorporates herein by reference Paragraphs 1-6 of its Complaint.

8. The '522 Patent, entitled "Method and apparatus for controlling power consumption of an integrated circuit," was duly and lawfully issued on April 2, 2002. A true and correct copy of the '522 Patent is attached hereto as Exhibit 1.

9. The '522 Patent names Marcus W. May and Daniel Mulligan as co-inventors.

10. The '522 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '522 Patent, including the right to seek damages for past, current, and future infringement thereof.

11. The '522 Patent "relates generally to integrated circuits and more particularly to controlling power consumption by an integrated circuit." Ex. 1 at 1:6-8.

12. The '522 Patent explains, for example, that "a need exists for a method and apparatus that adjust[s] the system clock and/or the supply voltage based on the processing capabilities of an integrated circuit and the application being performed to conserve power." *Id.* at 1:45-48.

13. The '522 Patent further explains that it "provides a method and apparatus for controlling power consumption of an integrated circuit." *Id.* at 2:7-9.

14. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '522 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the

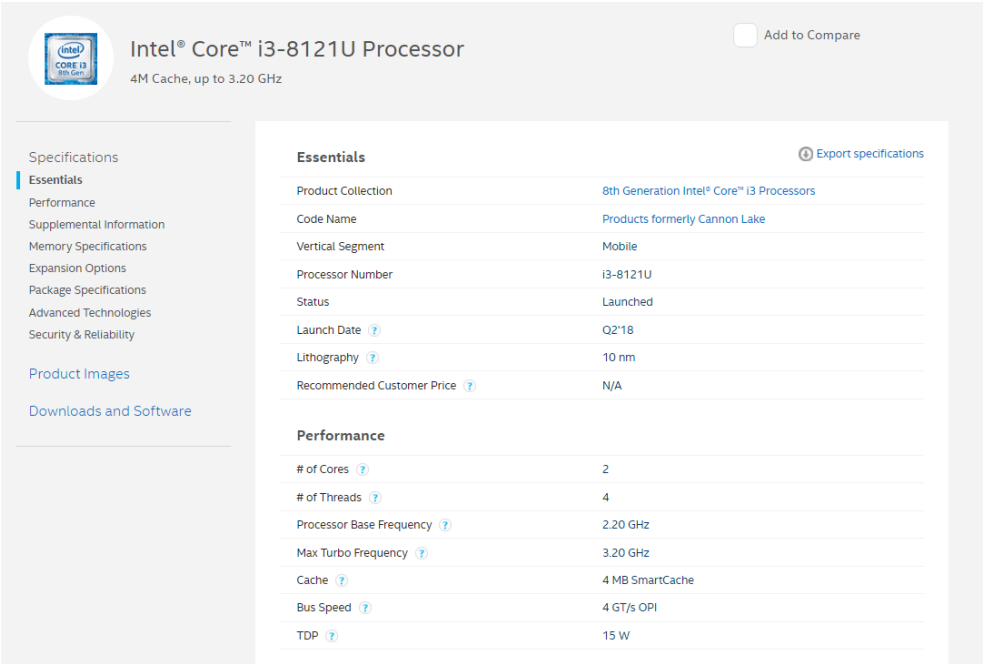
United States, without authority or license, Intel products that use "Speed Shift" technology with a fully integrated voltage regulator ("FIVR") in an infringing manner.

15. For example, the '522 accused products embody every limitation of at least claim 9 of the '522 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["9. A method for controlling power consumption of an integrated circuit, the method comprises the steps of:"]

16. Intel Cannon Lake processors are operated using a method of controlling power consumption of an integrated circuit.

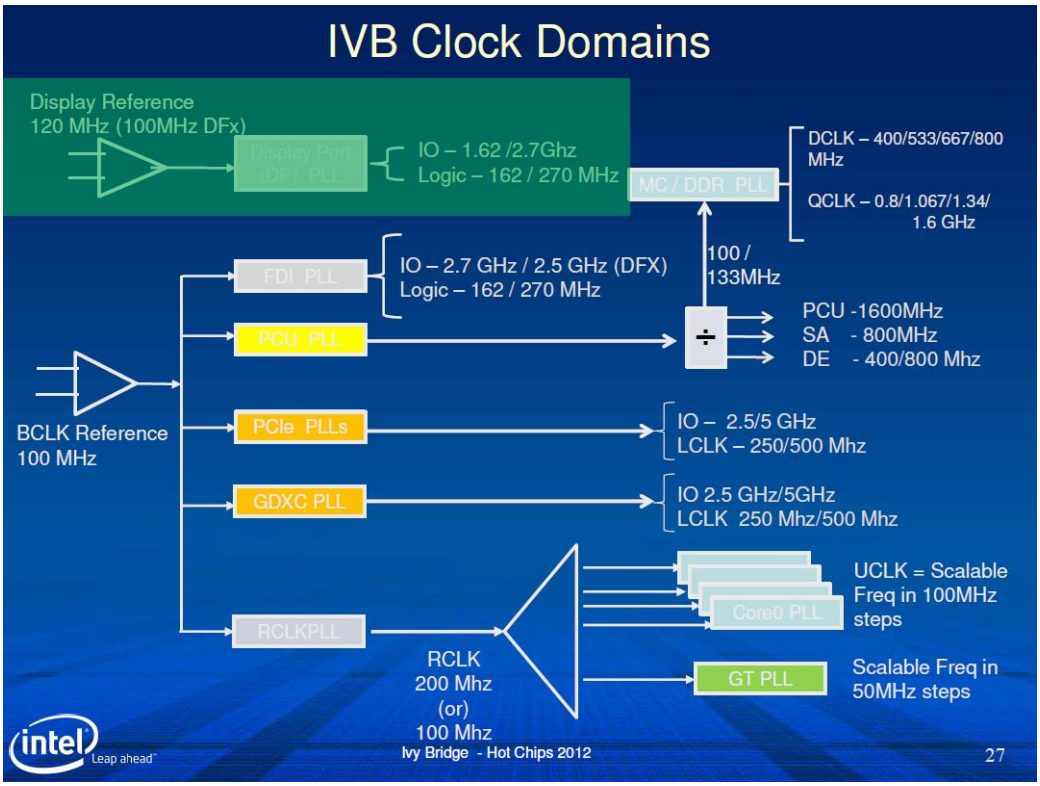
17. For example, Intel Cannon Lake processors include an integrated circuit. *See, e.g.*, https://ark.intel.com/products/136863/Intel-Core-i3-8121U-Processor-4M-Cache-up-to-3-20-GHz-?q=Core%20i3-8121U [hereinafter "ARK"]:



[“producing a system clock from a reference clock based on a system clock control signal;”]

18. Intel Cannon Lake processors are operated using a method that comprises producing a system clock from a reference clock based on a system clock control signal.

19. For example, the Intel power control architecture produces a number of controllably scalable system clocks, including core clocks, from a reference clock based on system clock control signals. *See, e.g.*, Power Management of the Third Generation Core Micro Architecture formerly codenamed Ivy Bridge [hereinafter “PM”] at 27:



20. On information and belief, these and the other pertinent portions of Intel’s Ivy Bridge generation (as well as the Sandy Bridge and 4th Generation Intel Core SoCs discussed below) were carried over to the Cannon Lake processor in a manner that is materially the same with respect to the infringement analysis presented in this example.

21. As a further example, reverse engineering of an Intel Cannon Lake processor also shows the production of a number of controllably scalable system clocks, including core clocks, from a reference clock based on system clock control signals:

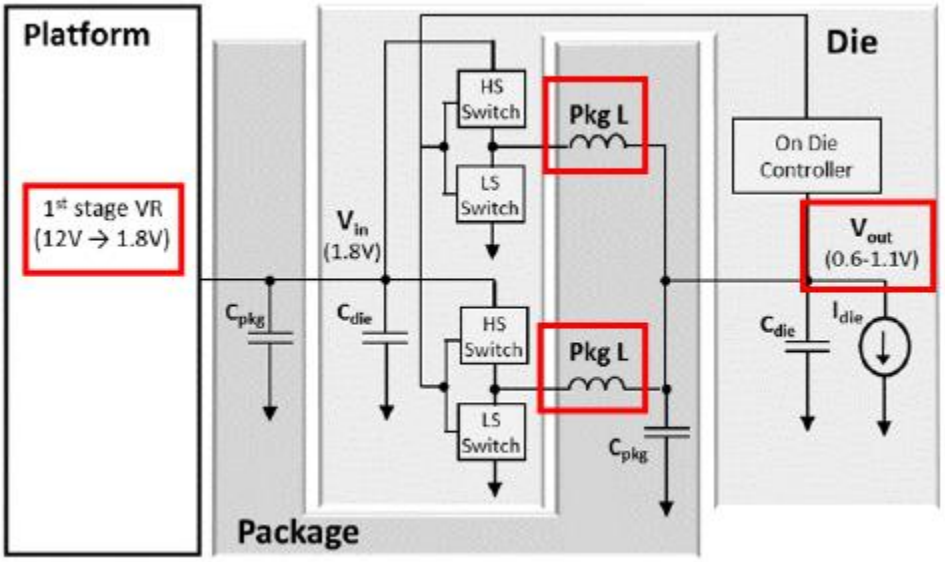
Processors Information	
Socket 1	ID = 0
Number of cores	2 (max 2)
Number of threads	4 (max 4)
Name	Intel Cannon Lake
Codename	Skylake
Specification	Intel(R) Core(TM) i3-8121U CPU @ 2.20GHz
Package (platform ID)	(0x7)
CPUID	6.6.3
Extended CPUID	6.66
Core Stepping	
TDP Limit	15.0 Watts
Tjmax	105.0 °C
Core Speed	3094.7 MHz
Multiplier x Bus Speed	31.0 x 99.8 MHz
Base frequency (cores)	99.8 MHz
Base frequency (ext.)	99.8 MHz
Stock frequency	2200 MHz
Max frequency	3200 MHz

[“regulating at least one supply from a power source and an inductance based on a power supply control signal; and”]

22. Intel Cannon Lake processors are operated using a method that comprises regulating at least one supply from a power source and an inductance based on a power supply control signal.

23. For example, on information and belief the FIVR on Intel Cannon Lake Processors regulates an output supply (*e.g.*, Vout) from a power source (*e.g.*, 1st stage VR) and an inductance (*e.g.*, Pkg L) based on power supply control signals. *See*, *e.g.*, “FIVR – Fully Integrated Voltage

Regulators on the 4th Generation Intel Core SoCs" [hereinafter "FIVR"] at 2:



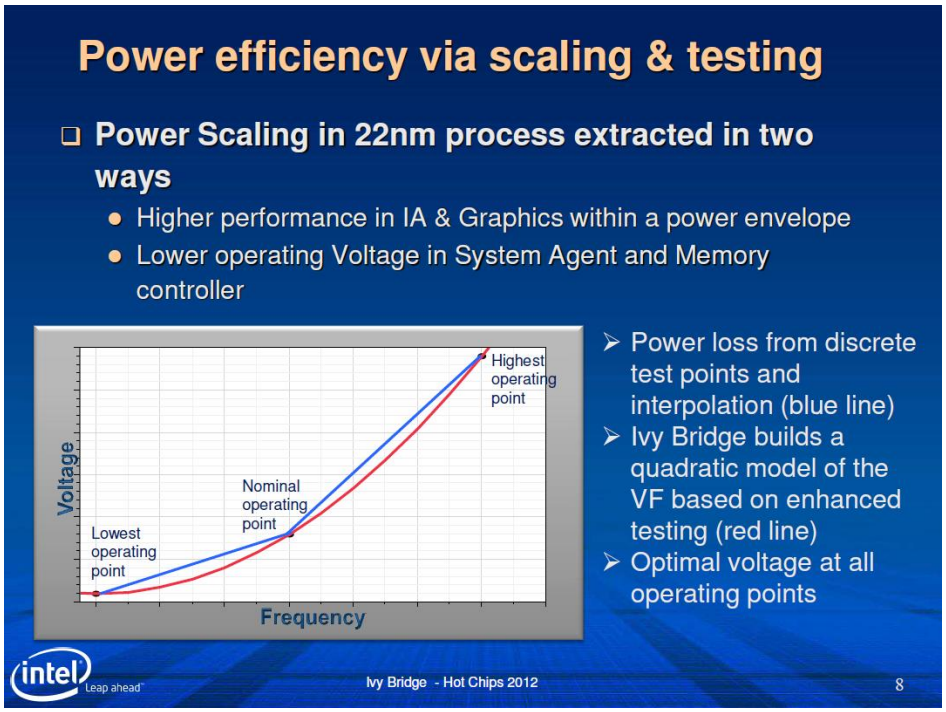
24. *See also, e.g.*, FIVR at 1: "Each FIVR is independently programmable to achieve optimal operation given the requirements of the domain it is powering. The settings are optimized by the Power Control Unit (PCU), which specifies the input voltage, output voltage, number of operating phases, and a variety of other settings to minimize the total power consumption of the die."

25. *See also, e.g.*, https://forums.anandtech.com/threads/fivr-returning-with-cannonlake.2484038/#lg=_xfUid-1-1549490270&slide=0 (discussing "FIVR at uncore for Cannonlake SoC" and "Cannonlake architecture … with FIVR").

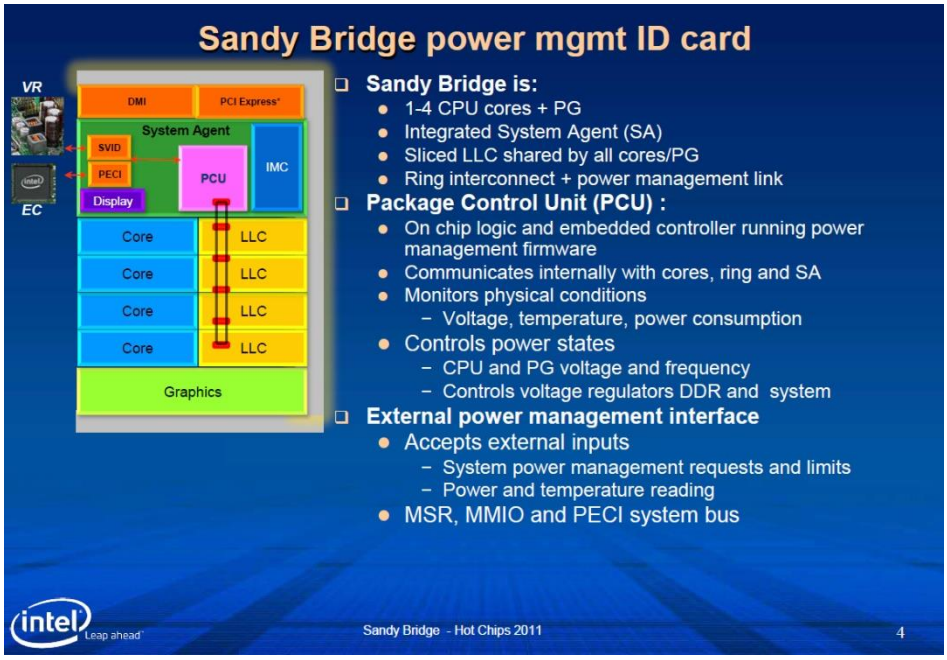
["producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and"]

26. Intel Cannon Lake processors are operated using a method that comprises producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine.

27. For example, the PCU produces power supply control signals based on a quadratic model of the VF requirements, a model that includes one or more processing transfer characteristics of the computation engine. *See*, *e.g.*, PM at 8:



28. *See also, e.g.*, "Power management architecture of the 2nd generation Intel Core microarchitecture, formerly codenamed Sandy Bridge" at 4:



29. Additionally, the PCU produces system clock control signals based on maximum frequencies, maximum turbo frequencies and TDP, additional processing transfer characteristics of the computational engine. *See, e.g.*, ARK:

Performance	
# of Cores	2
# of Threads	4
Processor Base Frequency	2.20 GHz
Max Turbo Frequency	3.20 GHz
Cache	4 MB SmartCache
Bus Speed	4 GT/s OPI
TDP	15 W

["processing requirements associated with processing at least a portion of an application by the computation engine."]

30. Intel Cannon Lake processors are operated using a method that comprises producing the system clock control signal and the power supply control signal based on processing

requirements associated with processing at least a portion of an application by the computation engine.

31. For example, the processor P-state, which includes an operating frequency and voltage, is set by the PCU and the Hardware-Controlled Performance State system based on processing requirements deemed appropriate for the applied workload. *See, e.g.*, Intel Software Developer's Manual [hereinafter "SDM"] at 3158-3159:

14.4 HARDWARE-CONTROLLED PERFORMANCE STATES (HWP)

Intel processors may contain support for Hardware-Controlled Performance States (HWP), which autonomously selects performance states while utilizing OS supplied performance guidance hints. The Enhanced Intel Speed-Step® Technology provides a means for the OS to control and monitor discrete frequency-based operating points via the IA32_PERF_CTL and IA32_PERF_STATUS MSRs.

In contrast, HWP is an implementation of the ACPI-defined Collaborative Processor Performance Control (CPPC), which specifies that the platform enumerates a continuous, abstract unit-less, performance value scale that is not tied to a specific performance state / frequency by definition. While the enumerated scale is roughly linear in terms of a delivered integer workload performance result, the OS is required to characterize the performance value range to comprehend the delivered performance for an applied workload.

When HWP is enabled, the processor autonomously selects performance states as deemed appropriate for the applied workload and with consideration of constraining hints that are programmed by the OS. These OS-provided hints include minimum and maximum performance limits, preference towards energy efficiency or performance, and the specification of a relevant workload history observation time window. The means for the OS to override HWP's autonomous selection of performance state with a specific desired performance target is also provided, however, the effective frequency delivered is subject to the result of energy efficiency and performance optimizations.

32. Reverse engineering analysis shows that Intel Cannon Lake processors include the HWP feature:

Processors Information	
Socket 1	ID = 0
Number of cores	2 (max 2)
Number of threads	4 (max 4)
Name	Intel Cannon Lake
Codename	Skylake
Specification	Intel(R) Core(TM) i3-8121U CPU @ 2.20GHz
Package (platform ID)	(0x7)
CPUID	6.6.3
Extended CPUID	6.66

[...]

IBRS	supported, disabled
IBPB	supported
STIBP	supported, disabled
RDCL_NO	no
IBRS_ALL	not supported
Turbo Mode	supported, enabled
Max non-turbo ratio	22x
Max turbo ratio	32x
Max efficiency ratio	4x
Speedshift	Autonomous

33. Intel has had knowledge of the '522 Patent and its infringement of the '522 Patent at least since the filing of the complaint in *VLSI Technology LLC v. Intel Corp.*, Civil Action No. 19-00426 (D. Del.) (filed Mar. 1, 2019) (the "Delaware Complaint") which asserted infringement by Intel of the '522 Patent, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the '522 Patent and its infringement of the '522 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals. For example, in *Intel Corp. v. Future Link Sys., LLC*, 268 F. Supp. 3d 605, 623 (D. Del. 2017) the court noted the patent owner's observation that "Intel's own engineers concede that they avoid reviewing other, non-Intel patents so as to avoid willfully infringing them." As a further example, former Intel employees, including Intel's long-time Chief Architect Robert Colwell, have admitted that this policy's purpose is to "avoid possible triple damages for 'willful infringement.'" As still another example, on information and belief, Intel has been sued for infringing patents previously assigned to NXP while this policy was in place, including for infringing a patent naming Marcus W. May (also an inventor on the '522 Patent) as an inventor. *See, e.g.*, *VLSI Technology LLC v. Intel Corp.*, Civil Action No. 18-0966-CFC (D. Del.). Yet despite this notice, Intel proceeded to infringe other patents on inventions developed in the same area by Mr. May. Under the

circumstances present here, including explicit notice having been provided of Intel's infringement of other NXP patents and NXP's competitive position with Intel in the marketplace, Intel knew or should have known of the high probability that NXP had patented other technologies, such as those to which the '522 Patent is directed, that Intel had included within its microprocessor products. Intel should have known that its conduct was infringing both prior to and following the filing of VLSI's Delaware Complaint.

34. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '522 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States (as used in this pleading, "customers" refers to both direct and indirect customers, including entities that distribute and resell the accused products, alone or as part of a system, and end users of such products and systems). For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '522 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '522 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

35. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '522 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed

invention of the ’522 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the ’522 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the ’522 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel’s customers directly infringe the ’522 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

36. As a result of Intel’s infringement of the ’522 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel’s wrongful acts in an amount subject to proof at trial.

37. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the ’522 Patent.

38. In addition, Intel’s infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

39. VLSI is informed and believes, and thereon alleges, that Intel’s infringement of the ’522 Patent has been and continues to be willful. As noted above, Intel has had knowledge of the ’522 Patent and its infringement of the ’522 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI’s patent rights. Thus, Intel’s infringing actions have been and continue to be consciously wrongful.

40. Based on the information alleged in this claim, as well as the information alleged in the Second Claim, *infra*, VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

SECOND CLAIM

(Infringement of U.S. Patent No. 6,633,187)

41. VLSI re-alleges and incorporates herein by reference Paragraphs 1-40 of its Complaint.

42. The '187 Patent, entitled "Method and apparatus for enabling a stand alone integrated circuit," was duly and lawfully issued October 14, 2003. A true and correct copy of the '187 Patent is attached hereto as Exhibit 2.

43. The '187 Patent names Michael R. May and Marcus W. May as inventors.

44. The '187 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '187 Patent, including the right to seek damages for past, current, and future infringement thereof.

45. The '187 Patent states that it "relates generally to integrated circuits and more particularly to enabling a stand-alone integrated circuit." Ex. 2 at 1:7-9.

46. The '187 Patent states that integrated circuits "include a large amount of circuitry in a very small area." *Id*. at 1:12-13. The '187 Patent further explains that when a "power converter is on-chip with the digital circuitry and the power converter requires a clock signal to produce a supply voltage, a difficulty arises in enabling such a stand-alone integrated circuit." *Id*. at 1:34-39. Thus, the patent explains, there was a need "for a method and apparatus for enabling a stand-alone integrated circuit that includes an on-chip power converter." *Id*. at 1:40-42.

47. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the ’187 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products containing an infringing fully integrated voltage regulator.

48. For example, the ’187 accused products embody every limitation of at least claim 1 of the ’187 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

[“1. A method for enabling a stand-alone integrated circuit (IC), the method comprises the steps of:”]

49. Intel Broadwell processors use a method for enabling a stand-alone integrated circuit.

50. For example, Intel Broadwell processors comprise a stand-alone integrated circuit that includes a FIVR. *See*, *e.g.*, 5th Generation Intel Core Processor Family Datasheet Vol. 1 [hereinafter “Datasheet”] at 80:

> **7.1 Integrated Voltage Regulator**
>
> A feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the processor has one main voltage rail (V_{CC}) and a voltage rail for the memory interface (V_{DDQ}) , compared to six voltage rails on previous processors. The V_{CC} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, system agent, and graphics. This integration allows the processor to better control on-die voltages to optimize between performance and power savings. The processor V_{CC} rail will remain a VID-based voltage with a loadline similar to the core voltage rail (also called V_{CC}) in previous processors.

[“a) establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;”]

51. Intel Broadwell processors use a method that comprises establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC.

52. For example, Broadwell processors initialize into an idle state that holds the cores in a reset condition, preventing them from running while a power source is operably coupled to the stand-alone IC until the correct power sequencing signals are received. *See*, *e.g.*, Datasheet at 77:

6.8 Power Sequencing Signals

Table 33. Power Sequencing Signals

Signal Name	Description	Direction / Buffer Type
PROCPWRGD	The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state.	I Asynchronous CMOS
VCCST_PWRGD	The processor requires this input signal to be a clean indication that the V_{CCST} and V_{DDQ} power supplies are stable and within specifications. This single must have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state."	I Asynchronous CMOS
PROC_DETECT#	**Processor Detect:** This signal is pulled down directly (0 Ohms) on the processor package to ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	—

[“b) receiving a power enable signal;”]

53. Intel Broadwell processors use a method that comprises receiving a power enable signal.

54. For example, Broadwell processors receive a power enable signal such as PROCPWRGD. *See, e.g.*, Datasheet at 77:

6.8 Power Sequencing Signals

Table 33. Power Sequencing Signals

Signal Name	Description	Direction / Buffer Type
PROCPWRGD	The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state.	I Asynchronous CMOS
VCCST_PWRGD	The processor requires this input signal to be a clean indication that the V_{CCST} and V_{DDQ} power supplies are stable and within specifications. This single must have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until the supplies come within specification. The signal must then transition monotonically to a high state."	I Asynchronous CMOS
PROC_DETECT#	**Processor Detect:** This signal is pulled down directly (0 Ohms) on the processor package to ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	–

["c) enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source, wherein the enabling includes:"]

55. Intel Broadwell processors use a method that comprises enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source.

56. For example, Broadwell processors are started in response to the power enable signals, including PROCPWRGD. The system's Power Control Unit (PCU) then turns on or off given "rails," or regions of the chip powered by a particular on-chip power converter. These on-chip power converters then provide the correct supply voltages.

57. *See, e.g.*, "FIVR – Fully Integrated Voltage Regulators on 4th Generation Intel Core SoCs" [hereinafter "FIVR"] at 4:

> *C. System Control*
>
> In order to minimize losses from FIVR, a modified version of the PCU [1] dynamically configures each FCM based on the current activity level of the domain. The PCU turns each rail on or off based on activity, and specifies an output voltage target to support the desired frequency. It also optimizes the settings discussed in section II.A for the anticipated operating conditions. These settings include the number of active phases (i.e. phase shedding to improve light load performance), the compensator settings (to maintain optimal transient response as the number of phases changes), and the timing of switch drivers (to ensure zero voltage switching at light loads). This allows each FIVR domain to operate at near peak efficiency across a wide range of load conditions from retention to Turbo. An example of the benefit this provides is shown in Section IV.A.

58. On information and belief, these and the other pertinent portions of the FIVR in 4th Generation Intel Core chips were carried over to the Broadwell processor in a manner that is materially the same with respect to the infringement analysis presented in this example.

["generating a clock signal;" and "generating power converter regulation signals based on the clock signal;"]

59. Intel Broadwell processors use a method that comprises generating a clock signal and generating power converter regulation signals based on the clock signal.

60. For example, the Frequency Control Module in each FIVR domain of the Intel Broadwell processor generates a clock signal using, *e.g.*, a "triangular waveform synthesizer" PLL

and generates power converter regulation signals, for instance, in a comparator based on this clock signal. *See, e.g.*, FIVR at 3:

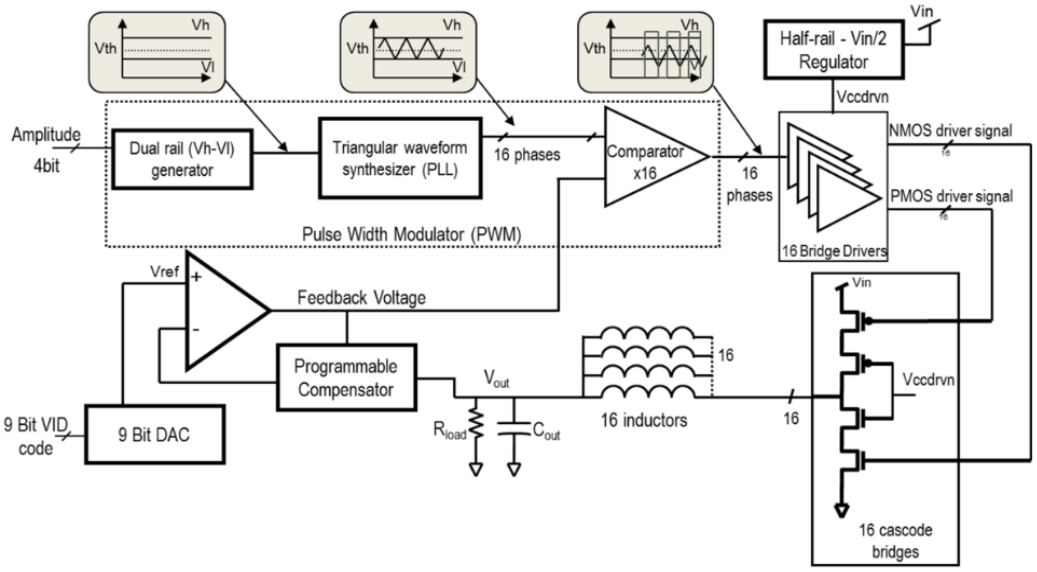


Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain

[“enabling a band-gap reference that is used in generating the power converter regulation signals; and”]

61. Intel Broadwell processors use a method that comprises enabling a band-gap reference that is used in generating the power converter regulation signals.

62. For example, Broadwell processors, which are manufactured in 14-nm CMOS technology, on information and belief use a band-gap reference (“BGREF”) in generating their power converter regulation signals by measuring “the digital VCC power-up.” *See, e.g.*, “An

Accurate Bandgap-Based Power-on-Detector in 14-nm CMOS Technology" [hereinafter "Bandgap"] at 1:

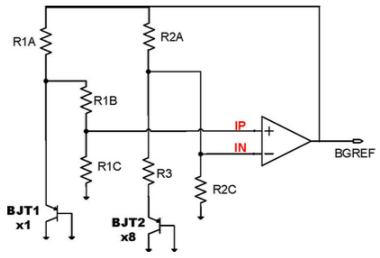
An Accurate Bandgap-Based Power-on-Detector in 14-nm CMOS Technology

Joseph Shor, *Senior Member, IEEE*, and Dror Zilberman

***Abstract*—A novel power-on-detector (POD) circuit is reported in 14-nm technology. This POD has a sigma accuracy of 12 mV, including process, voltage, and temperature variations with a power of 496 μW and an area of 0.02 mm^2. The POD uses an open-loop offset-cancelled bandgap-based circuit to achieve this high accuracy. It is also capable of detecting two operating voltages simultaneously and can measure the digital VCC power-up at supply levels lower than the diode voltage.**

***Index Terms*—Analog, bandgap reference (BGREF), micro-processors, power-on-detector (POD) circuit.**

I. Introduction



63. *See also, e.g.*, FIVR at 3:

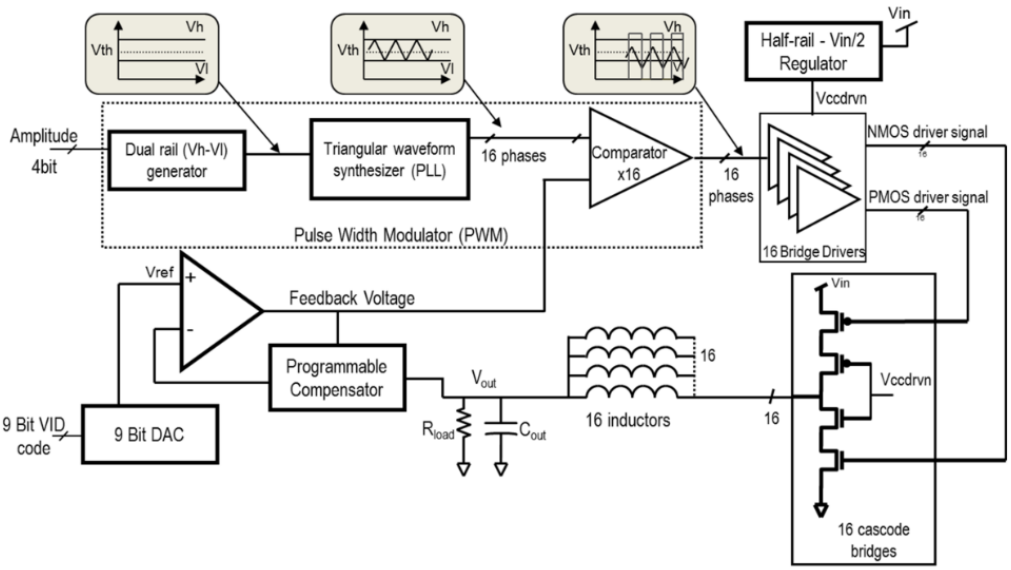


Figure 2. Simplified block diagram of the circuitry for a single representative FIVR domain

64. *See also, e.g.*, Bandgap at 4, stating that this circuit was produced "extensively in high-volume manufacturing."

[“d) when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.”]

65. Intel Broadwell processors use a method that comprises, when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.

66. For example, Broadwell processors use a “power-on detector” to enable functionality of the IC when the supply voltages have reached their steady state operating level. *See*, *e.g.*, Bandgap at 1:

> COMPUTER systems require power-on-detector (POD) circuits to determine that the supply voltages have reached the correct operating level [1]–[5]. This is especially true when memory elements are involved. In present microprocessors, there are usually multiple supply domains, both analog and digital, each of which can have its own operating point [6], [7]. The accuracy of the POD will determine the minimum VCC level of the microprocessor or system-on-chip, so this is an important parameter.

67. Intel has had knowledge of the ’187 Patent and its infringement of the ’187 Patent at least since the filing of the complaint in *VLSI Technology LLC v. Intel Corp.*, Civil Action No. 19-00426 (D. Del.) (filed Mar. 1, 2019) which asserted infringement by Intel of the ’187 Patent, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the ’187 Patent and its infringement of the ’187 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals, as already described above. As still another example, on information and belief, Intel has been sued for infringing patents previously assigned to NXP while this policy was in place, including for infringing a patent naming Marcus W. May (also an inventor on the ’187 Patent) as an inventor, as already explained above. Yet despite this notice, Intel proceeded to infringe other

patents on inventions developed in the same area by Mr. May. Under the circumstances present here, including explicit notice having been provided of Intel's infringement of other NXP patents and NXP's competitive position with Intel in the marketplace, Intel knew or should have known of the high probability that NXP had patented other technologies, such as those to which the '187 Patent is directed, that Intel had included within its microprocessor products. Intel should have known that its conduct was infringing both prior to and following the filing of VLSI's Delaware Complaint.

68. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '187 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '187 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '187 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

69. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '187 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '187 Patent both inside and outside the United States. For example, the above-

described products constitute a material part of the inventions of the '187 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '187 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel's customers directly infringe the '187 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

70. As a result of Intel's infringement of the '187 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

71. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '187 Patent.

72. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

73. VLSI is informed and believes, and thereon alleges, that Intel's infringement of the '187 Patent has been and continues to be willful. As noted above, Intel has had knowledge of the '187 Patent and its infringement of the '187 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

74. Based on the information alleged in this claim, as well as the information alleged in the First Claim, *supra*, VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, VLSI prays for judgment against Intel as follows:

A. That Intel has infringed, and unless enjoined will continue to infringe, each of the Asserted Patents;

B. That Intel has willfully infringed each of the Asserted Patents;

C. That Intel pay VLSI damages adequate to compensate VLSI for Intel's infringement of each of the Asserted Patents, together with interest and costs under 35 U.S.C. § 284;

D. That Intel be ordered to pay prejudgment and post-judgment interest on the damages assessed;

E. That Intel pay VLSI enhanced damages pursuant to 35 U.S.C. § 284;

F. That Intel be ordered to pay supplemental damages to VLSI, including interest, with an accounting, as needed;

G. That Intel be enjoined from infringing the Asserted Patents, or if its infringement is not enjoined, that Intel be ordered to pay ongoing royalties to VLSI for any post-judgment infringement of the Asserted Patents;

H. That this is an exceptional case under 35 U.S.C. § 285, and that Intel pay VLSI's attorneys' fees and costs in this action; and

I. That VLSI be awarded such other and further relief, including equitable relief, as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), VLSI hereby demands a trial by jury on all issues triable to a jury.

Dated: April 11, 2019

Respectfully submitted,

By: */s/J. Mark Mann*

J. Mark Mann
State Bar No. 12926150
mark@themannfirm.com
G. Blake Thompson
State Bar No. 24042033
blake@themannfirm.com
MANN | TINDEL | THOMPSON
300 W. Main Street
Henderson, TX 75652
Telephone: 903.657.8540
Fax: 903.657.6003

Andy Tindel (Texas Bar No. 20054500)
atindel@andytindel.com
MANN | TINDEL | THOMPSON
112 E. Line Street, Suite 304
Tyler, Texas 75702
Telephone: (903) 596-0900
Facsimile: (903) 596-0909

Craig D. Cherry (Texas Bar No. 24012419)
ccherry@haleyolson.com
HALEY & OLSON, P.C.
100 N. Ritchie Road, Suite 200
Waco, Texas 76701
Telephone: (254) 776-3336
Facsimile: (254) 776-6823

Attorneys for Plaintiff VLSI Technology LLC