IN THE UNITED STATES DISTRICT COURT
FOR THE SOUTHERN DISTRICT OF NEW YORK

JAMES B. GOODMAN,	*	
	*	**Civil Action No.**
Plaintiff,	*	
	*	**COMPLAINT FOR PATENT**
Vs.	*	**INFRINGEMENT**
	*	
NVIDIA CORPORATION	*	**DEMAND FOR JURY TRIAL**
	*	
	*	
Defendant.	*	
**********		**********

NOW COMES Plaintiff, JAMES B. GOODMAN ("Goodman" herein), through his attorney, and files this Complaint for Patent Infringement and Demand for Jury Trial against Nvidia Corporation ("Nvidia").

PARTIES

1. Goodman is an individual residing in the State of Texas.

2. On information and belief from the web site for Nvidia, Nvidia maintains a U.S. Corporate Headquarters located at 2788 San Tomas Expressway, Santa Clara, CA 955051.

3. On information and belief from the web site for Nvidia, Nvidia offers for sale; and sells products in this Federal Judicial District on its web site, and through many stores in New York, NY including Best Buy, Walmart, Staples Technologies Solutions, Micro Electronics Inc., and CompUSA (DealCentral LLC).

4. On information and belief, Nvidia has an active business and product development office located at 41 East 11th Street, Suite 61, New York, NY 10003.

5. On information and belief, Nvidia has substantial sales and business presence in this Federal Judicial District through Nvidia's sales online through the internet, and through local

stores; and Nvidia has a significant physical presence at least with its active office business and product development in this Federal Judicial District.

JURISDICTION AND VENUE

6. This is an action for patent infringement of United States Patent No. 6,243,315 (“ ‘315 Patent") pursuant to the laws of the United States of America as set forth in Title 35 Sections 271 and 281 of the United States Code. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. Sec. 1338(a) and 28 U.S.C. Sec. 1331. Venue is proper in this Federal Judicial District under 28 U.S.C. § 1400(b).

7. On information and belief, Nvidia is subject to this Court's specific and general personal jurisdiction, pursuant to due process and/or the New York Long Arm Statute, due to at least its business presence in this Federal Judicial District, including substantial infringing activities in this Federal Judicial District.

8. On information and belief, Nvidia, directly and/or through intermediaries, advertise at least through Nvidia’s web sites and other web sites, offers to sell, sold and/or distributed its products, and/or has induced the sale and use of infringing products in this Federal Judicial District. In addition, and on information and belief, Nvidia is subject to the Court's general jurisdiction, including from regularly doing business, or soliciting business, or engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to individuals and businesses in this Federal Judicial District.

9. Venue is proper in this Federal Judicial District because, on information and belief, Nvidia has committed substantial infringement of the ‘315 Patent in this Judicial District, and maintains at least one active business office in this Federal Judicial District.

BACKGROUND LITIGATION

10. On June 5, 2001, U.S. Patent No. 6,243,315 ("'315 Patent") entitled "Computer Memory System with a Low Power Mode" was duly and legally issued to James B. Goodman ("Goodman") as the sole patentee, the Plaintiff herein.

11. Goodman is the sole owner of the '315 Patent has standing to bring this action.

12. During a prior litigation (*Goodman v. Hewlett-Packard Co.*, Civil Action No. 4:16-CV-3195), Hewlett-Packard ("HP") petitioned the Patent Trial and Appeal Board ("PTAB") for an *Inter Partes* Review ("IPR") for claim 1 of the '315 Patent and other patent claims, and the Petition was granted. See IPR 2017-01994.

13. On March 9, 2019, the PTAB Decision found claim 1 of the '315 Patent patentable over the references cited by HP.

14. On the same day HP had its petition for an IPR granted, the PTAB granted the petitions against claim 1 and other patent claims of the '315 Patent filed by Samsung Electronics America, Inc. (IPR2017-02021), and by ASUS Computer International, Inc. (IPR2018-00047

15. The PTAB held a Hearing for all three petitions by HP, Samsung, and ASUS on the same day.

16. Under the PTAB Rules, the PTAB is required to issue a Decision within one year of a Hearing, but if there are two or more combined petitioners such as Samsung and ASUS, the PTAB can take 18 months to issue a Decision.

17. Goodman is still awaiting the Decision for the petitions from Samsung and ASUS; however, it is expected that the same claim construction stated by the PTAB for the HP petition as being the broadest reasonable construction for claim 1 of the '315 Patent will again be as

favorable to the Patent Owner, Goodman, as in the HP IPR, and it is reasonably expected that claim 1 of the '315 Patent will be found valid over the multitude of cited prior art.

18. This litigation is being brought in the reasonable anticipation of claim 1 of the '315 Patent being determined to be valid over the arguments of both Samsung and ASUS to start damages due to the continuing patent infringement by Nvidia of claim 1 of the '315 Patent.

19. This litigation is substantially different from prior patent infringement litigation based on the '315 Patent against companies making, offering for sale, and selling computers incorporating a DDR2, DDR3, and DDR4 memory products because this litigation is for a graphics cards including a graphic processing units ("GPU") and a GDDR5, and/or a GDDR5X, and/or a GDDR6 memory product.

20. The designation of the memory products as being "GDDR5", "GDDR5X", and "GDDR6" is due to the JEDEC Solid State Technology Association located at 3103 North 10th Street, Suite 240-S, Arlington, VA 22201 ("JEDEC").

21. JEDEC is a global leader in developing open standards for the microelectronics industry, and a broad range of range of technologies; and no memory product is permitted to use the designation "GDDR5", "GDDR5X", or "GDDR6" unless it complies with the corresponding industry standard established by JEDEC.

22. The JEDEC Standards corresponding to GDDR5, GDDR5X, and GDDR6 memory products are JESD212C, JESD232A, and JESD250B, respectively.

23. On information and belief, each GEFORCE GTX 1050, 1060, and 1070 graphic card from Nvidia includes a graphics processor unit ("GPU"), and a GDDR5 memory product.

24. On information and belief, each GEFORCE GTX 2560 graphic card from Nvidia includes a graphics processor unit ("GPU") and a GDDR5X memory product.

25. On information and belief, each GEFORCE GTX 1660 Ti, 2060, 2070, 2080, and 2080 Ti graphic card from Nvidia includes a graphics processor unit ("GPU") and a GDDR6 memory product.

26. On information and belief, each of the memory products identified as "GDDR5", "GDDR5X", and "GDDR6" above in ¶ ¶ ¶ 23, 24, and 25 includes a plurality of memory banks which corresponds to a plurality of memory devices literally, or at least under the doctrine of equivalents in claim 1 of the '315 Patent.

27. On information and belief, each of the Nvidia graphics cards identified above in ¶ ¶ ¶ 23, 24, and 25 includes controllers to detect activity in a memory device, and to enter and implement a low power down state according to claim 1 of the '315 Patent.

28. The following is a chart comparing the elements of claim 1 of the '315 Patent to the respective Nvidia graphics cards identified in ¶ 23 to provide notice of the infringement being asserted herein:

NOTICE OF INFRINGEMENT FOR CLAIM 1 OF THE '315 PATENT AND AN NVIDIA GRAPHICS CARD INCLUDING A GDDR5 MEMORY PRODUCT

CLAIM 1	**NVIDIA GRAPHICS CARD INCLUDING A GPU AND GDDR5 MEMORY PRODUCT (¶ 23)**
1. A memory system for use in a computer system, said memory system comprising:	EACH NVIDIA GRAPHICS CARD GEFORCE GTX 1050, 1060, AND 1070 IS A MEMORY SYSTEM. THE NVIDIA GRAPHICS CARD IS USED IN A COMPUTER SYSTEM. THE JESD212C SETS FORTH THE REQUIRED OPERATIONS AND TECHNICAL REQUIREMENTS OF THE GDDR5 MEMORY PRODUCT INCORPORATED INTO THE NVIDIA GRAPHICS CARD SO THAT IT IS APPROPRIATE TO COMPARE THE TECHNICAL ASPECTS IN JESD212C AS THOUGH IT WERE A COMPARISON OF THE TECHNICAL

	ASPECTS OF GDDR5 FOR A COMPARISON TO CLAIM 1. JESD212C AT P. 2, UNDER THE HEADING, "**NOTICE**" STATES: **"No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."** THIS CONFIRMS THAT ANALYZING THE JESD212C IS THE SAME AS ANALYZING THE GDDR5 MEMORY PRODUCT.
	THE SCOPE OF COVERAGE OF THE JESD212C IS COMPLETE FOR ALL KNOWN GDDR5 MEMORY PRODUCTS: P. 2, SEC. 2 STATES THAT THE FOLLOWING GDDR5 MEMORY PRODUCTS ARE COVERED BY THE JEDEC STANDARD IN JESD212C: **"512 Mb = 16 Mb x 32 (2 Mb x 32 x 8 banks) / 32 Mb x 16 (4 Mb x 16 x 8 banks)** **1 Gb = 32 Mb x 32 (2 Mb x 32 x 16 banks) / 64 Mb x 16 (4 Mb x 16 x 16 banks)** **2 Gb = 64 Mb x 32 (4 Mb x 32 x 16 banks) / 128 Mb x 16 (8 Mb x 16 x 16 banks)** **4 Gb = 128 Mb x 32 (8 Mb x 32 x 16 banks) / 256 Mb x 16 (16 Mb x 16 x 16 banks)** **8 Gb = 256 Mb x 32 (16 Mb x 32 x 16 banks) / 512 Mb x 16 (32 Mb x 16 x 16 bank"**
	THE UNIVERSAL APPLICATION OF THE JESD212C IS DISCLOSED AT P. 1, SEC. 1 FOR MEMORY COMPONENTS: **"This document defines the Graphics Double Data Rate 5 GDDR5) Synchronous Graphics Random Access Memory (SGRAM) standard, including features, functionality, package, and pin assignments. This scope may be expanded in future to also include other higher density devices. The purpose of this Standard is to define the minimum set of requirements for JEDEC standard compatible 512 Mb through 8 Gb x32 GDDR5 SGRAM devices. System designs**

	based on the required aspects of this standard will be supported by all GDDR5 SGRAM vendors providing JEDEC standard compatible devices."
a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and	JESD212C AT P. 108, SEC. 8.2 DISCLOSES THE LIMITED VOLTAGE RANGES FOR THE SGRAM. THE FACT THAT THE GDDR5 HAS AT LEAST TWO BANKS OF MEMORY (AS STATED IN JESD212C, P. 1) CONSTITUTES A PLURALITY OF MEMORY DEVICES DIRECTLY, OR UNDER THE DOCTRINE OF EQUIVALENTS. THE BANKS CAN BE OPERATED ON INDEPENDENTLY. SEE JESD212C AT PP. 60-61, AND 85-88.
capable of being placed in a self refresh mode;	JESD212C DISCLOSES SELF REFRESH CAPABILITY AT PP. 85-88, AND AT MANY OTHER PLACES. NOTE THAT AT P. 89, IT IS DISCLOSED: "**7.16 SELF-REFRESH** **Self-Refresh can be used to retain data in the device, even if the rest of the system is powered down. When in the Self-Refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command (see Figure) is initiated like a REFRESH command except that CKE_n is pulled HIGH. SELF REFRESH ENTRY is only allowed when all banks are precharged with tRP satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command have been pushed out (tRDSRE or tWRSRE). NOP commands are required until tCKSRE is met after the entering Self-Refresh. The PLL/DLL is automatically disabled upon entering Self-Refresh and is automatically enabled and reset upon exiting Self-Refresh. If the device enters Self-Refresh with the PLL/DLL disabled, it will exit Self-Refresh with the PLL/DLL disabled. Once the**

	SELF REFRESH ENTRY command is registered, CKE_n must be held HIGH to keep the device in Self-Refresh mode. When the device has entered the Self-Refresh mode, all external control signals, except CKE_n and RESET_n are "Don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFC, VREFD) must be at valid levels. The device initiates a minimum of one internal refresh within tCKE period once it enters Self-Refresh mode. The address, command, data and WCK pins are in ODT state, and the EDC pins drive a HIGH." JESD212C, AT P. 52, PARA. 6.9 SHOWS THAT REFRESH CAN BE DONE ON A PER-BANK. SEE ALSO P. 55, PARA. 7.1, THE TABLE ENTRY "PER-BANK REFRESH" AND NOTE 6.
said memory devices having address lines and control lines;	ADDRESS AND CONTROL LINES ARE NECESSARY FOR WRITING AND READING DATA IN THE MEMORY DEVICES. THE TECHNICAL DESCRIPTION OF THE SGRAM PORTION OF THE GDDR5 IS SET FORTH IN JEDEC STANDARDS JESD21-C, 1/97, AND JESD100-B, 12/99. JESDEC 212C DISCUSSES THE SIGNALS FOR THE GDDR5 IN MANY PLACES SUCH AS AT P. 12: "**4.1 ADDRESSING** **GDDR5 SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 6. The addresses should be provided to the device in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c. The use of GDDR5 addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned**

	for latching on the initial rising edge for faster decoding."
a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	A PORTION OF THE NVIDIA CARD IS RESPONSIBLE FOR THE OPERATION OF THE GDRR5 FOR SELF-REFRESH AS SHOWN IN JESD212C AT P.91, PARA. 7.16, FIG. 81, TOP TIMING GRAPH. THIS TIMING GRAPH SHOWS THAT WHEN THE CKE_n GOES FROM LOW TO HIGH, THE SELF-REFRESH COMMAND IS THEN REGISTERED AND NOP COMMANDS ARE REQUIRED UNTIL tCKSRE IS MET (CORRESPONDING TO tCPDED) ELECTRICALLY ISOLATING THE MEMORY DEVICES UNTIL ENTERING SELF-REFRESH MODE. AFTER THE ENTERING SELF-REFRESH. WHEN THE DEVICE HAS ENTERED THE SELF-REFRESH MODE, ALL EXTERNAL CONTROL SIGNALS, EXCEPT CKE_n AND RESET_n ARE "DON'T CARE". THE CLOCK IS INTERNALLY DISABLE DURING SELF-REFRESH OPERATION TO SAVE POWER. AFTER tCKSRE IS MET, CK_c AND CK_t ARE "DON'T CARE". THE OPERATION OF THE NOP IS DEFINED AT P. 57, PARA. 7.2 AND 7.3 AS: **"7.2 DESELECT (NOP)** **The DESELECT function (CS_n HIGH) prevents new commands from being executed by the device. The device is effectively deselected. Operations already in progress are not affected.** **7.3 NO OPERATION (NOP)** **The NO OPERATION (NOP) command is used to instruct the selected device to perform a NOP (CS_n LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected."** JESD212C AT P. 138 DISCLOSES: **"9.2 SIGNALS - Table 67**

	CKE_n Input Clock Enable: CKE_n LOW activates and CKE_n HIGH deactivates the internal clock, device input buffers, and output drivers. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained LOW throughout read and write accesses. The value of CKE_n latched at power-up with RESET_n going High determines the termination value of the address and command inputs." JESD212C P. 138, TABLE 67 BALL-OUT DESCRIPTION DISCLOSES TAKING CKE_n HIGH DEACTIVATES THE INTERNAL CLOCK, DEVICE INPUT BUFFERS, AND OUTPUT DRIVERS. TAKING CKE_n HIGH PROVIDES PRECHARGE POWER-DOWN AND SELF-REFRESH OR ACTIVE POWER-DOWN. JESD212C P. 92 TABLE 29 SHOWS CKE_n PIN BEING DRIVEN HIGH BY EXTERNAL CONTROLLER DURING SELF REFRESH. THE JESD212C AT P. 95, PARA. 7.19 SHOWS THAT FOR CKE_n IN SELF REFRESH, THE COMMAND IS "X" AND NOTE 1 DEFINES THIS CONDITION AS HAVING THE COMMAND DECODER DISABLED. THAT IS, NO RAS, CAS OR WE SIGNALS ARE GENERATED BY THE COMMAND DECODER TO GO TO THE MEMORY DEVICES. THUS, THE RAS, CAS, AND WE SIGNALS ARE ISOLATED FROM THE MEMORY DEVICES AT LEAST UNDER THE DOCTRINE OF EQUIVALENTS. THE JESD212C AT P. 89, PARA. 7.16 DESCRIBES THE SELF-REFRESH OPERATIONS, AND POINTS OUT IN THE THIRD PARAGRAPH THAT CKE_n IS AN EXTERNAL SIGNAL. THE CKE_n DOES NOT CONNECT TO THE MEMORY DEVICES.

a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system;	ON INFORMATION AND BELIEF, THE SELF-REFRESH STATE FOR THE GDDR5 IS A LOW POWER MODE. NOTE P. 89, PARA. 7.16, THIRD PARAGRAPH: "**7.16 SELF-REFRESH** **Self-Refresh can be used to retain data in the device, even if the rest of the system is powered down. When in the Self-Refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command (see Figure) is initiated like a REFRESH command except that CKE_n is pulled HIGH. SELF REFRESH ENTRY is only allowed when all banks are precharged with tRP satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command have been pushed out (tRDSRE or tWRSRE). NOP commands are required until tCKSRE is met after the entering Self-Refresh."** THE SELF REFRESH STARTS AFTER THERE ARE NO PENDING WRITING TO OR READING OUT OF THE MEMORY DEVICE. THE FIRST SENTENCE OF THE THIRD PARAGRAPH OF 7.16 STATES: **"The clock is internally disabled during the Self-Refresh operation to save power"**
wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	IT HAS BEEN SHOWN FROM JESD212C THAT DURING SELF-REFRESH, THE MEMORY DEVICES ARE ELECTRICLALY ISOLATED AND THAT THE MEMORY DEVICES ARE IN A LOW POWER MODE.

29. The following is a chart comparing the elements of claim 1 of the '315 Patent to the respective Nvidia graphics cards identified in ¶ 24 to provide notice of the infringement being asserted herein:

NOTICE OF INFRINGEMENT FOR CLAIM 1 OF THE '315 PATENT AND AN NVIDIA GRAPHICS CARD INCLUDING A GDDR5X MEMORY PRODUCT

CLAIM 1	**NVIDIA GRAPHICS CARD INCLUDING A GPU AND GDDR5X MEMORY PRODUCT (¶ 24)**
1. A memory system for use in a computer system, said memory system comprising:	THE NVIDIA GRAPHICS CARD GEFORCE GTX 2560 IS THE MEMORY SYSTEM. THE NVIDIA GRAPHICS CARD IS USED IN A COMPUTER SYSTEM. THE JESD232A SETS FORTH THE REQUIRED OPERATIONS AND TECHNICAL REQUIREMENTS OF THE GDDR5X MEMORY PRODUCT INCORPORATED INTO THE NVIDIA GRAPHICS CARD SO THAT IT IS APPROPRIATE TO COMPARE THE TECHNICAL ASPECTS IN JESD232A AS THOUGH IT WERE A COMPARISON OF THE TECHNICAL ASPECTS OF GDDR5X FOR A COMPARISON TO CLAIM 1. JESD232A AT P. 2, UNDER THE HEADING, "**NOTICE**" STATES: **"No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."** THIS CONFIRMS THAT ANALYZING THE JESD232A IS THE SAME AS ANALYZING THE GDDR5X MEMORY PRODUCT.
	THE SCOPE OF COVERAGE OF THE JESD232A IS COMPLETE FOR ALL KNOWN GDDR5X MEMORY PRODUCTS: P. 2, SEC. 2 STATES THAT THE FOLLOWING GDDR5X MEMORY PRODUCTS ARE COVERED BY THE JEDEC STANDARD IN JESD232A: "**4 Gb = 128 Mb x 32 (8 Mb x 32 x 16 banks)/256 Mb x 16 (16 Mb x 16 x 16 banks)** **6 Gb = 192 Mb x 32 (12 Mb x 32 x 16 banks)/384 Mb x 16 (24 Mb x 16 x 16 banks)8 Gb = 256 Mb x 32 (16 Mb x 32 x 16 banks)/512 Mb x 16 (32 Mb x 16 x 16 banks)**

	12 Gb = 384 Mb x 32 (24 Mb x 32 x 16 banks)/768 Mb x 16 (48 Mb x 16 x 16 banks) **16 Gb = 512 Mb x 32 (32 Mb x 32 x 16 banks)/ 1 Gb x 16 (64 Mb x 16 x 16 banks)**
	THE UNIVERSAL APPLICATION OF THE JESD232A IS DISCLOSED AT P. 1, SEC. 1 FOR MEMORY COMPONENTS: **"This document defines the GDDR5X SGRAM memory standard, including features, device operation, electrical characteristics, timings, signal pin assignments and package. The purpose of this standard is to define the minimum set of requirements for JEDEC standard compatible4 Gb through 16 Gb x32 GDDR5X SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5X SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5X standard such as AC timings were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics."**
a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and	JESD232A AT P. 112, SEC. 8.1 DISCLOSES THE LIMITED VOLTAGE RANGES FOR THE SGRAM. THE FACT THAT THE GDDR5X HAS AT LEAST TWO BANKS OF MEMORY, AS STATED IN JESD232A, P. 2, CONSTITUTES A PLURALITY OF MEMORY DEVICES DIRECTLY, OR UNDER THE DOCTRINE OF EQUIVALENTS. THE BANKS CAN BE OPERATED ON INDEPENDENTLY. SEE JESD232A AT PP. 69-70, AND 97-101.
capable of being placed in a self refresh mode;	JESD232A DISCLOSES SELF REFRESH CAPABILITY AT PP. 41, 64, 105 AND AT

	MANY OTHER PLACES. AT P. 101, IT IS DISCLOSED: "**7.12 SELF-REFRESH** **Self refresh can be used to retain data in the GDDR5X SGRAM, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command is like a REFRESH command except that CKE_n is pulled High. Automatic NOPs protects the memory devices from Self Refresh entering (initiation) through Self Refresh exiting.**" IN ADDITION: **"After the SELF REFRESH ENTRY command is registered, CKE_n must be held High to keep the device in self refresh mode. When the device has entered the self refresh mode, all external control signals except CKE_n and RESET_n are "Don't care". The user can halt the external CK and WCK clocks or change the external clock frequency tCKSRE after self refresh entry. The address, command, data, CK and WCK pins are in ODT state, and the EDC pins drive a High (or High-Z when the EDC High-Z bit is set). CK and WCK clocks are internally disabled during self refresh operation to save power."**
said memory devices having address lines and control lines;	ADDRESS AND CONTROL LINES GOING TO THE MEMORY DEVICES ARE NECESSARY FOR WRITING AND READING IN THE MEMORY DEVICES. THE TECHNICAL DESCRIPTION OF THE SGRAM PORTION OF THE GDDR5X IS SET FORTH IN JEDEC STANDARDS JESD21-C, 1/97, AND JESD100-B, 12/99. JESDEC 232A DISCUSSES THE SIGNALS FOR THE GDDR5X IN MANY PLACES SUCH AS: "**3.4 ADDRESSING** **GDDR5X SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 6. The addresses should be provided to the device in two parts; the first half is latched on the**

	rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c. The use of GDDR5X addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding."
a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	A PORTION OF THE NVIDIA CARD IS RESPONSIBLE FOR THE OPERATION OF THE GDRR5X FOR SELF-REFRESH AS SHOWN IN JESD232A AT P. 103, PARA. 7.12, FIG. 101, TOP TIMING GRAPH. THIS TIMING GRAPH SHOWS THAT WHEN THE CKE_n GOES FROM LOW TO HIGH, THE SELF-REFRESH COMMAND IS THEN REGISTERED AND NOP COMMANDS ARE REQUIRED UNTIL tCKSRE IS MET (CORRESPONDING TO tCPDED) ELECTRICALLY ISOLATING THE MEMORY DEVICES UNTIL ENTERING SELF-REFRESH MODE. AFTER THE ENTERING SELF-REFRESH. WHEN THE DEVICE HAS ENTERED THE SELF-REFRESH MODE, ALL EXTERNAL CONTROL SIGNALS, EXCEPT CKE_N AND RESET_N ARE "DON'T CARE". THE CLOCK IS INTERNALLY DISABLE DURING SELF-REFRESH OPERATION TO SAVE POWER. AFTER tCKSRE IS MET, CK_c AND CK_t ARE "DON'T CARE". THE OPERATION OF THE NOP IS DEFINED AT P. 65, PARA. 7.3 AS: **7.3 NO OPERATION (NOP)** **The NO OPERATION (NOP) command is used to instruct the device to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected."** JESD232A AT P. 137 DISCLOSES: **"9.1 SIGNAL DESCRIPTION Table 58**

	Clock Enable: CKE_n Low activates and CKE_n High deactivates the internal clock, device input buffers, and output drivers. Taking CKE_n High provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained Low throughout read and write accesses." JESD232A P. 137, TABLE 58 BALL-OUT DESCRIPTION DISCLOSES TAKING CKE_n HIGH DEACTIVATES THE INTERNAL CLOCK, DEVICE INPUT BUFFERS, AND OUTPUT DRIVERS. TAKING CKE_n HIGH PROVIDES PRECHARGE POWER-DOWN AND SELF-REFRESH OR ACTIVE POWER-DOWN. JESD232A P. 107 TABLE 33 SHOWS CKE_n PIN BEING DRIVEN HIGH BY EXTERNAL CONTROLLER DURING SELF REFRESH. THE JESD232A AT P. 108, PARA. 7.16 SHOWS THAT FOR CKE_n IN SELF REFRESH, THE COMMAND IS "X" AND NOTE 1 DEFINES THIS CONDITION AS HAVING THE COMMAND DECODER DISABLED. THAT IS, NO RAS, CAS OR WE SIGNALS ARE GENERATED BY THE COMMAND DECODER TO GO TO THE MEMORY DEVICES. THUS, THE RAS, CAS, AND WE SIGNALS ARE ISOLATED FROM THE MEMORY DEVICES AT LEAST UNDER THE DOCTRINE OF EQUIVALENTS. THE JESD232A AT P. 101-102, PARA. 7.12 DESCRIBES THE SELF-REFRESH OPERATIONS, AND POINTS OUT IN THE THIRD PARAGRAPH THAT CKE_n IS AN EXTERNAL SIGNAL. THE CKE_n DOES NOT CONNECT TO THE MEMORY DEVICES.
a memory access enable control device coupled to said control device and to said	ON INFORMATION AND BELIEF, THE SELF-REFRESH STATE FOR THE

control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system;	GDDR5X IS A LOW POWER MODE. NOTE P. 101, PARA. 7.11.2, FIRST PARAGRAPH: "**7.12 SELF-REFRESH** **After the SELF REFRESH ENTRY command is registered, CKE_n must be held High to keep the device in self refresh mode. When the device has entered the self refresh mode, all external control signals except CKE_n and RESET_n are "Don't care". The user can halt the external CK and WCK clocks or change the external clock frequency tCKSRE after self refresh entry. The address, command, data, CK and WCK pins are in ODT state, and the EDC pins drive a High (or High-Z when the EDC High-Z bit is set). CK and WCK clocks are internally disabled during self refresh operation to save power."** THE SELF REFRESH STARTS AFTER THERE ARE NO PENDING WRITING TO OR READING OUT OF THE MEMORY DEVICE. THE LAST SENTENCE STATES: **"The clock is internally disabled during the Self-Refresh operation to save power"**
wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	IT HAS BEEN SHOWN FROM JESD232A THAT DURING SELF-REFRESH, THE MEMORY DEVICES ARE ELECTRICLALY ISOLATED AND THAT THE MEMORY DEVICES ARE IN A LOW POWER MODE.

30. The following is a chart comparing the elements of claim 1 of the '315 Patent to the respective Nvidia graphics cards identified in ¶ 25 to provide notice of the infringement being asserted herein:

NOTICE OF INFRINGEMENT FOR CLAIM 1 OF THE '315 PATENT AND AN NVIDIA GRAPHICS CARD INCLUDING A GDDR6 MEMORY PRODUCT

CLAIM 1	**AN NVIDIA GPU INCORPORATING GDDR6 MEMORY PRODUCT (¶ 25)**
1. A memory system for use in a computer system, said memory system comprising:	EACH NVIDIA GRAPHICS CARD GEFORCE GTX 1660 Ti, 2060, 2070, 2080, AND 2080 TI GRAPHIC CARD IS A MEMORY SYSTEM. THE NVIDIA GRAPHICS CARD IS USED IN A COMPUTER SYSTEM. THE JESD250B SETS FORTH THE REQUIRED OPERATIONS AND TECHNICAL REQUIREMENTS OF THE GDDR6 MEMORY PRODUCT INCORPORATED INTO THE NVIDIA GRAPHICS CARD SO THAT IT IS APPROPRIATE TO COMPARE THE TECHNICAL ASPECTS IN JESD250B AS THOUGH IT WERE A COMPARISON OF THE TECHNICAL ASPECTS OF GDDR6 FOR A COMPARISON TO CLAIM 1. JESD250B AT P. 2, UNDER THE HEADING, "**NOTICE**" STATES: **"No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."** THIS CONFIRMS THAT ANALYZING THE JESD250B IS THE SAME AS ANALYZING THE GDDR6 MEMORY PRODUCT.
	NOTE THAT JESD250B AT P. 2, SEC. 2 STATES THAT THE FOLLOWING MEMORY PRODUCTS ARE COVERED BY THE JEDEC STANDARD IN JESD250B: **"8 Gb = 2 Channels 256Mb x 16 2 x (16Mb x 16 x 16 banks) / 2 Channels 512Mb x 8 2 x (32Mb x 8 x 16 banks)** **12 Gb = 2 Channels 384Mb x 16 2 x (24Mb x 16 x 16 banks) / 2 Channels 768Mb x 8 2 x (48Mb x 8 x 16 banks)** **16 Gb = 2 Channels 512Mb x 16 2 x (32Mb x 16 x 16 banks) / 2 Channels 1Gb x 8 2 x (64Mb x 8 x 16 banks)**

	24 Gb = 2 Channels 768Mb x 16 2 x (48Mb x 16 x 16 banks) / 2 Channels 1.5Gb x 8 2 x (96Mb x 8 x 16 banks) **32 Gb = 2 Channels 1Gb x 16 2 x (64Mb x 16 x 16 banks) / 2 Channels 2Gb x 8 2 x (128Mb x 8 x 16 banks)"**
a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode;	JESD250A AT P. 139, SEC. 8.1 FOR THE LIMITED VOLTAGE RANGES FOR THE SGRAM. THE FACT THAT THE GDDR6 HAS AT LEAST TWO BANKS OF MEMORY CONSTITUTES A PLURALITY OF MEMORY DEVICES DIRECTLY, OR UNDER THE DOCTRINE OF EQUIVALENTS. NOTE THAT THE BANKS CAN BE OPERATED ON INDEPENDENTLY. SEE JESD250B AT PP. 114-119. JESD250B DISCLOSES SELF REFRESH AT PP. 114-120.
said memory devices having address lines and control lines;	ADDRESS AND CONTROL LINES GOING TO THE MEMORY DEVICES ARE NECESSARY FOR WRITING AND READING DATA IN THE MEMORY DEVICES. THE TECHNICAL DESCRIPTION OF THE SGRAM IS SET FORTH IN JEDEC STANDARDS JESD21-C, 1/97, AND JESD100-B, 12/99. JESDEC 250B DISCUSSES THE SIGNALS FOR THE GDDR6 IN MANY PLACES SUCH AS P. 17: **"4.1 COMMAND and ADDRESSING GDDR6 SGRAMs use a double data rate command address scheme to reduce balls required on the device. The command and address is packetized on the 10 CA signals (CA[9:0]) over either single cycle or multi cycles depending on the command (see Command Truth Table). For single cycle commands the command and address data is provided to the device in two parts; the first half is latched on the rising edge of CK; the second half is latched on the falling edge of CK. An 11th CA signal (CA10) is reserved for higher densities.**

	GDDR6 addressing is defined for a single channel with devices having 2 channels/device."
a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	A PORTION OF THE NVIDIA CARD IS RESPONSIBLE FOR THE OPERATION OF THE GDDR6 FOR SELF-REFRESH AS SHOWN IN JESD250B AT P. 124, PARA. 7.18, FIG. 124, TOP TIMING GRAPH. THIS TIMING GRAPH SHOWS THAT WHEN THE CKE_n GOES FROM LOW TO HIGH, THE SELF-REFRESH COMMAND IS THEN REGISTERED AND NOP COMMANDS ARE REQUIRED UNTIL tCKSRE IS MET (CORRESPONDING TO tCPDED) ELECTRICALLY ISOLATING THE MEMORY DEVICES UNTIL ENTERING SELF-REFRESH MODE. AFTER THE ENTERING SELF-REFRESH. WHEN THE DEVICE HAS ENTERED THE SELF-REFRESH MODE, ALL EXTERNAL CONTROL SIGNALS, EXCEPT CKE_N AND RESET_N ARE "DON'T CARE". THE CLOCK IS INTERNALLY DISABLE DURING SELF-REFRESH OPERATION TO SAVE POWER. AFTER tCKSRE IS MET, CK_c AND CK_t ARE "DON'T CARE". THE OPERATION OF THE NOP IS DEFINED AT P. 76, PARA. 7.3 AS: **"7.3 NO OPERATION (NOP)** **The NO OPERATION (NOP) command is used to instruct the device to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. GDDR6 defines three encodings for the NOP command, and all three encodings perform the same NOP. NOP (2) and NOP (3) encodings are only allowed during CA Training."** THE JESD250A AT P. 130, PARA. 7.23 SHOWS THAT FOR CKE_n IN SELF REFRESH, THE COMMAND IS "X" AND NOTE 1 DEFINES THIS CONDITION AS

	HAVING THE COMMAND DECODER DISABLED. THAT IS, NO RAS, CAS OR WE SIGNALS ARE GENERATED BY THE COMMAND DECODER TO GO TO THE MEMORY DEVICES. THUS, THE RAS, CAS, AND WE SIGNALS ARE ISOLATED FROM THE MEMORY DEVICES AT LEAST UNDER THE DOCTRINE OF EQUIVALENTS. THE JESD250B AT P. 122, PARA. 7.18 DESCRIBES THE SELF-REFRESH OPERATIONS, AND POINTS OUT IN THE THIRD PARAGRAPH THAT CKE_n IS AN EXTERNAL SIGNAL. THE CKE_n DOES NOT CONNECT TO THE MEMORY DEVICES. JESD250B AT P. 172 DISCLOSES: **"9.2 SIGNALS Table 74** **Clock Enable: CKE_n LOW activates and CKE_n HIGH deactivates the internal clock, device input buffers, and output drivers excluding RESET_n, TDI, TDO, TMS and TCK. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained LOW throughout read and write accesses."** JESD250B P. 172, TABLE 74 BALL-OUT DESCRIPTION DISCLOSES TAKING CKE_n HIGH DEACTIVATES THE INTERNAL CLOCK, DEVICE INPUT BUFFERS, AND OUTPUT DRIVERS. TAKING CKE HIGH PROVIDES PRECHARGE POWER-DOWN AND SELF-REFRESH OR ACTIVE POWER-DOWN. NOTE THAT JESD250B P. 123 TABLE 43 SHOWS CKE_n PIN BEING DRIVEN HIGH BY EXTERNAL CONTROLLER DURING SELF REFRESH.
a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for	ON INFORMATION AND BELIEF, THE SELF-REFRESH STATE FOR THE GDDR6 IS A LOW POWER MODE. NOTE P. 122, PARA. 7.18, FIRST AND SECOND PARAGRAPHS:

initiating a low power mode for said memory system;	**"7.18 SELF REFRESH** **Self Refresh can be used to retain data in the device, even if the rest of the system is powered down. Self Refresh can also be used to retain data in only one channel while the other channel is in normal operation. The full power savings can only be achieved when both channels are in Self Refresh. When in the Self Refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command (see Figure 99) is initiated like a REFRESH command except that CKE_n is pulled HIGH.** **SELF REFRESH ENTRY is only allowed when all banks are precharged with tRP satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command has been pushed out (tRDSRE or tWRSRE). NOP commands are required until tCKSRE is met after the entering Self Refresh. The PLL/DLL is automatically disabled upon entering Self Refresh and is automatically enabled and reset upon exiting Self Refresh. If the device enters Self Refresh with the PLL/DLL disabled, it will exit Self Refresh with the PLL/DLL disabled."** THE SELF REFRESH STARTS AFTER THERE ARE NO PENDING WRITING TO OR READING OUT OF THE MEMORY DEVICE. THE FIRST SENTENCE OF THE FOURTH PARAGRAPH OF 7.18 STATES: **"The clock is internally disabled during the Self-Refresh operation to save power"**
wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	IT HAS BEEN SHOWN FROM JESD250bC THAT DURING SELF-REFRESH, THE MEMORY DEVICES ARE ELECTRICLALY ISOLATED AND THAT THE MEMORY DEVICES ARE IN A LOW POWER MODE.

COUNT ONE

31. Plaintiff Goodman repeats and incorporates herein the allegations stated in paragraphs 1 to 30 above.

32. All of the limitations of claim 1 of the ‘315 Patent are present literally and/or under the doctrine of equivalents in Nvidia GEFORCE GTX 1050, 1060, and 1070 manufactured, and/or offered for sale, and/or sold by Nvidia.

33. Nvidia is infringing claim 1 of the ‘315 Patent by its activities stated on ¶ 31 in this Federal Judicial District.

COUNT TWO

34. Plaintiff Goodman repeats and incorporates herein the allegations stated in paragraphs 1 to 30 above.

35. All of the limitations of claim 1 of the ‘315 Patent are present literally and/or under the doctrine of equivalents in Nvidia GEFORCE GTX 2560 manufactured, and/or offered for sale, and/or sold by Nvidia.

36. Nvidia is infringing claim 1 of the ‘315 Patent by its activities stated on ¶ 31 in this Federal Judicial District.

COUNT THREE

37. Plaintiff Goodman repeats and incorporates herein the allegations stated in paragraphs 1 to 30 above.

38. All of the limitations of claim 1 of the ‘315 Patent are present literally and/or under the doctrine of equivalents in Nvidia GEFORCE GTX 1660 Ti, 2060, 2070, and 2080 manufactured, and/or offered for sale, and/or sold by Nvidia.

39. Nvidia is infringing claim 1 of the '315 Patent by its activities stated on ¶ 31 in this Federal Judicial District.

JURY DEMAND

Pursuant to Fed. R. Civ. P. 38(b), Goodman hereby demands a jury trial as to all issues in this lawsuit.

PRAYER FOR RELEIF

THEREFORE, Goodman respectfully requests this to Court to:

a. Enter judgment for Goodman on Count One as to patent infringement either literally, and/or under the doctrine of equivalents;

b. Enter judgment for Goodman on Count Two as to patent infringement either literally, and/or under the doctrine of equivalents;

c. Enter judgment for Goodman on Count Three as to patent infringement either literally, and/or under the doctrine of equivalents;

d. order an accounting for Nvidia to determine damages to be paid to Goodman for patent infringement;

e. award Goodman interest;

f. award Goodman costs; and

g. award Goodman such other and further relief as this Court may deem just and equitable.

Date: May 21, 2019

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