**IN THE UNITED STATES DISTRICT COURT**
**FOR THE DISTRICT OF DELAWARE**

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| HOME SEMICONDUCTOR CORPORATION,<br><br>Plaintiff,<br><br>v.<br><br>SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC. and SAMSUNG AUSTIN SEMICONDUCTOR, LLC,<br><br>Defendants. | PUBLIC VERSION FILED: MAY 24, 2019<br><br>C.A. No. 13-2033-RGA<br><br>JURY TRIAL DEMANDED<br><br>[redacted] |

**PLAINTIFF'S SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff Home Semiconductor Corporation ("Plaintiff" or "Home Semiconductor") by and through its undersigned counsel, files this Plaintiff's Second Amended Complaint against Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC. (collectively, "Samsung").

**THE PARTIES**

1. Home Semiconductor is a Delaware corporation having its principal place of business at 3422 Old Capitol Trail, Suite 700, Wilmington, Delaware 19808-6192, U.S.A.

2. Upon information and belief, Samsung Electronics Co., Ltd. ("SEC") is a Korean corporation having its principal place of business at 250 2 Ka Taepyung, Ro Chung Ku, Seoul, Korea M5 100742. On information and belief, SEC is one of the world's largest electronics companies and it designs, manufactures, uses, sells, and offers to sell in, and imports into, the United States, a range of electronics products, including consumer electronics, mobile phones,

entertainment devices (such as TVs), and computer components, such as semiconductor chips, hard drives and other storage devices, such as the infringing DRAM and other devices at issue in this case. Additionally, SEC performs the infringing processes and uses at its facilities in the U.S. Upon information and belief, SEC is the parent company of an extremely complex and complicated ownership structure that includes numerous subsidiaries and related companies and has manufacturing and assembly plants and sales offices and affiliates in more than 80 countries, including Korea and the United States, and employs more than 300,000 workers.

3. Upon information and belief, Samsung Electronics America, Inc. ("SEA") is a New York corporation having its principal place of business at 85 Challenger Road, Ridgefield Park, New Jersey 07660. Upon information and belief, SEA is a wholly-owned subsidiary of SEC. Upon information and belief, SEA is a wholly-owned subsidiary of SEC and it manufactures, uses, sells, and offers to sell in, and imports into, the United States, a wide variety of consumer electronics products, a range of electronics products, including consumer electronics, mobile phones, entertainment devices (such as TVs), and computer components, such as semiconductor chips, hard drives and other storage devices, such as the infringing DRAM and other devices at issue in this case. Additionally, SEA performs the infringing processes and uses at its facilities in the U.S.

4. Upon information and belief, Samsung Semiconductor, Inc. ("SSI") is a California corporation having its principal place of business at 3655 North First Street, San Jose, California 95134 or 601 McCarthy Blvd., Milpitas, California 95035. Upon information and belief, SSI is a subsidiary of SEA and it manufactures, uses, sells, offers to sell in, and imports into, the United States a wide variety of consumer electronics products, including computer components and memory chips, such as the infringing DRAM and other devices at issue in this

case. Additionally, SSI performs the infringing processes and uses, at its facilities in San Jose, Austin and San Diego.

5. Upon information and belief, Samsung Austin Semiconductor, LLC. ("SAS") is a Delaware limited liability corporation having its principal place of business at 12100 Samsung Boulevard, Austin, Texas 78754. Upon information and belief, SAS is a wholly-owned subsidiary of SSI, is one of the Samsung manufacturing facilities and foundry operations in the U.S., and manufactures, uses, sells, and offers to sell in the United States a wide variety of electronics products, including computer components and memory chips, such as the infringing DRAM and other devices at issue in this case. Additionally, SAS performs the infringing processes and uses at its Austin, Texas facility.

6. Upon information and belief, Samsung has conducted and regularly conducts business within this District, has purposefully availed itself of the privileges of conducting business in this District, and has sought protection and benefit from the laws of the State of Delaware.

**JURISDICTION AND VENUE**

7. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.*, including but not limited to 35 U.S.C. §§ 271, 281, 283, 284, and 285. This Court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a).

8. This Court has personal jurisdiction over SEC. SEC is amenable to service of summons for this action. Furthermore, personal jurisdiction over SEC in this action comports with due process. SEC has conducted and regularly conducts business within the United States and this District. SEC has purposefully availed itself of the privileges of conducting business in

the United States, and more specifically in the State of Delaware and this District. SEC has sought protection and benefit from the laws of the State of Delaware by forming its United States affiliate in this District and/or by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

9. SEC – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale, and/or sells its products in the United States and this District. SEC has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SEC knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SEC has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from SEC's activities in this District.

10. This Court has personal jurisdiction over SEA. SEA is amenable to service of summons for this action. Furthermore, personal jurisdiction over SEA in this action comports with due process. SEA has conducted and regularly conducts business within the United States and this District. SEA has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SEA has sought protection and benefit from the laws of the State of Delaware by forming its United States affiliate in this District and/or by placing infringing products into the stream of

commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

11. SEA – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale, and/or sells its products in the United States and this District. SEA has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SEA knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SEA has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from SEA's activities in this District.

12. This Court has personal jurisdiction over SSI. SSI is amenable to service of summons for this action. Furthermore, personal jurisdiction over SSI in this action comports with due process. SSI has conducted and regularly conducts business within the United States and this District. SSI has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SSI has sought protection and benefit from the laws of the State of Delaware by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

13. SSI – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale, and/or sells its

products in the United States and this District. SSI has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SSI knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SSI has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from SSI's activities in this District.

14. This Court has personal jurisdiction over SAS. SAS is amenable to service of summons for this action. Furthermore, personal jurisdiction over SAS in this action comports with due process. SAS has conducted and regularly conducts business within the United States and this District. SAS has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SAS has sought protection and benefit from the laws of the State of Delaware by forming in this District and/or by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

15. SAS – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale, and/or sells its products in the United States and this District. SAS has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SAS knowingly and purposefully ships

infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SAS has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from SAS's activities in this District.

16. Venue is proper in this Court according to the venue provisions set forth by 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Samsung is subject to personal jurisdiction in this District, and therefore is deemed to reside in this District for purposes of venue. Upon information and belief, Samsung has committed acts within this District giving rise to this action and does business in this District, including but not limited to making sales in this District, providing service and support to its respective customers in this District and/or operating an interactive website, available to persons in this District that advertises, markets, and/or offers for sale infringing products.

**BACKGROUND**

17. U.S. Patent No. 5,452,261 titled "Serial Address Generator for Burst Memory" (the "'261 patent") was duly and legally issued by the U.S. Patent and Trademark Office on September 19, 1995, after full and fair examination. Jinyong Chung and Michael A. Murray are the inventors listed on the '261 patent. The '261 patent has been assigned to Plaintiff, and Plaintiff holds all rights, title, and interest in the '261 patent, including the right to collect and receive damages for past, present and future infringements. A true and correct copy of the '261 patent is attached as Exhibit A and made a part hereof.

18. U.S. Patent No. 6,146,997 titled "Method for Forming Self-Aligned Contact

Hole" (the "'997 patent") was duly and legally issued by the U.S. Patent and Trademark Office on November 14, 2000, after full and fair examination. Jacson Liu and Jing-Xian Huang are the inventors listed on the '997 patent. The '997 patent has been assigned to Plaintiff, and Plaintiff holds all rights, title, and interest in the '997 patent, including the right to collect and receive damages for past, present and future infringements. A true and correct copy of the '997 patent is attached as Exhibit B and made a part hereof.

19. Upon information and belief, Samsung makes, uses, offers to sell, and/or sells within, and/or imports into the United States products that incorporate the fundamental technologies covered by the '261 and '997 patents (collectively, the "patents-in-suit").

20. Upon information and belief, distributors purchase and have purchased Samsung's infringing products for sale or importation into the United States, including this District. Upon information and belief, consumers use and have used Samsung's infringing products in the United States, including this District.

**COUNT I**

**Patent Infringement of U.S. Patent No. 5,452,261**

21. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-20 as though fully set forth herein.

22. The '261 patent is valid and enforceable.

23. Samsung has never been licensed, either expressly or impliedly, under the '261 patent.

24. Upon information and belief, SEC, SEA, SSI, and SAS have been and are directly infringing under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, and/or indirectly infringing, by way of inducement with specific intent under 35 U.S.C. §

271(b), the '261 patent by making, using, offering to sell, and/or selling to manufacturers, distributors, customers and/or consumers (directly or through intermediaries and/or affiliates or subsidiaries) in this District and elsewhere within the United States and/or importing into the United States, or by inducing others to make, use, offer for sale, sell, and/or import into the United States, without authority, Samsung's dynamic random-access memories ("DRAMs") that include all of the limitations of one or more claims of the '261 patent, products containing Samsung's DRAMs that include all of the limitations of one or more claims of the '261 patent, and/or other products that include all of the limitations of one or more claims of the '261 patent. The accused products include but are not limited to Samsung DRAMs; and Samsung and non-Samsung branded smartphones, tablets, desktop PCs, notebook PCs, Chrome devices, Smart TVs, Blu-ray/DVD players, home theater systems, media players, cameras/camcorders, and printers that contain Samsung DRAMs.

25. Samsung DRAM has circuitry meeting every limitation of at least claims 1-5, 7-10, 12 and 14 of the '261 patent, as shown in Home's Infringement Contentions attached hereto as confidential Exhibit C.

26. Upon information and belief, distributors, customers and consumers that purchase Samsung's DRAMs that include all of the limitations of one or more claims of the '261 patent, products containing Samsung's DRAMs that include all of the limitations of one or more claims of the '261 patent, and/or other products made, sold or imported by Samsung that include all of the limitations of one or more claims of the '261 patent also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the '261 patent by using, offering to sell, and/or selling infringing products in this District and elsewhere in the United States.

27. Upon information and belief, Samsung had knowledge of the '261 patent and its

infringing conduct at least since October 24, 2013 when Samsung was formally placed on notice of its infringement. In any event, Samsung had knowledge of the '261 patent and its infringing conduct no later than the filing date of this Complaint.

28. Upon information and belief, since at least the above-mentioned date when Plaintiff formally placed Samsung on notice of its infringement, SEC, SEA, SSI, and SAS have actively induced, under 35 U.S.C. § 271(b), manufacturers, distributors, importers, customers and/or consumers to directly infringe one or more claims of the '261 patent. Since at least the notice provided on the above-mentioned date, SEC, SEA, SSI, and SAS do so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the '261 patent. Upon information and belief, SEC, SEA, SSI, and SAS intend to cause infringement by these manufacturers, distributors, importers, customers and/or consumers. SEC, SEA, SSI, and SAS have taken affirmative steps to induce infringement by, *inter alia*, creating advertisements that promote the infringing use of the infringing products, creating an established distribution channel for these products into and within the United States, manufacturing these products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States.

29. Upon information and belief, Samsung's acts of infringement of the '261 patent have been willful and intentional. Since at least the above-mentioned date of notice, Samsung has acted with an objectively high likelihood that its actions constitute infringement of the '261 patent by refusing to take a license and continuing to make and sell infringing products. The objectively-defined risk was either known or so obvious that it should have been known.

30. As a direct and proximate result of these acts of patent infringement, Samsung has encroached on the exclusive rights of Plaintiff to practice the '261 patent, for which Plaintiff is entitled to at least a reasonable royalty.

**COUNT II**

**Patent Infringement of U.S. Patent No. 6,146,997**

31. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-30 as though fully set forth herein.

32. The '997 patent is valid and enforceable.

33. Samsung has never been licensed, either expressly or impliedly, under the '997 patent.

34. Upon information and belief, SEC, SEA, SSI, and SAS have been and are directly infringing under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, and/or indirectly infringing, by way of inducement with specific intent under 35 U.S.C. § 271(b), the '997 patent by making, using, offering to sell, and/or selling to manufacturers, distributors, and/or consumers (directly or through intermediaries and/or affiliates or subsidiaries) in this District and elsewhere within the United States and/or importing into the United States, or by inducing others to make, use, offer for sale, sell, and/or import into the United States, without authority, Samsung's DRAMs that include all of the limitations of one or more claims of the '997 patent, Samsung's NAND flash memories that include all of the limitations of one or more claims of the '997 patent, Samsung's CPUs that include all of the limitations of one or more claims of the '997 patent, products containing Samsung's DRAMs, NAND flash memories and/or CPUs that include all of the limitations of one or more claims of the '997 patent, and/or other products that include all of the limitations of one or more claims of the '997 patent. The

accused products include but are not limited to Samsung DRAMs, internal and external NAND flash memories, and CPUs; and Samsung and non-Samsung branded smartphones, tablets, desktop PCs, notebook PCs, Chrome devices, Smart TVs, Blu-ray/DVD players, home theater systems, media players, cameras/camcorders, and printers that contain such DRAMs, NAND flash memories, and CPUs.

35. Upon information and belief, SEC, SEA, SSI, and SAS have been and are directly infringing the ’997 patent under 35 U.S.C. § 271(g) by, without authority, importing into the United States and/or offering to sell, selling, and/or using within the United States Samsung DRAMs, NAND flash memories, and CPUs and/or products containing Samsung DRAMs, NAND flash memories, and CPUs, where those Samsung DRAMs, NAND flash memories, and CPUs are made by a process practicing all of the limitations of one or more claims of the ’997 patent, either literally or under the doctrine of equivalents.

36. Samsung DRAMs, NAND flash memories, and CPUs are made by a process practicing every limitation of at least claims 2 and 9-14 of the ’997 patent, as shown Home’s Supplemental Infringement Contentions attached hereto as confidential Exhibit D.

37. Upon information and belief, distributors, customers and consumers that purchase Samsung’s DRAMs that include all of the limitations of one or more claims of the ’997 patent, Samsung’s NAND flash memories that include all of the limitations of one or more claims of the ’997 patent, Samsung’s CPUs that include all of the limitations of one or more claims of the ’997 patent, products containing Samsung’s DRAMs, NAND flash memories and/or CPUs that include all of the limitations of one or more claims of the ’997 patent, and/or other products made, sold or imported by Samsung that include all of the limitations of one or more claims of the ’997 patent also directly infringe, either literally or under the doctrine of equivalents, under

35 U.S.C. § 271(a), the ’997 patent by using, offering to sell, and/or selling infringing products in this District and elsewhere in the United States.

38. Upon information and belief, Samsung had knowledge of the ’997 patent and its infringing conduct at least since October 24, 2013 when Samsung was formally placed on notice of its infringement. In any event, Samsung had knowledge of the ’997 patent and its infringing conduct no later than the filing date of this Complaint.

39. Upon information and belief, since at least the above-mentioned date when Plaintiff formally placed Samsung on notice of its infringement, SEC, SEA, SSI, and SAS have actively induced, under 35 U.S.C. § 271(b), manufacturers, distributors, importers, customers and/or consumers to directly infringe one or more claims of the ’997 patent. Since at least the notice provided on the above-mentioned date, SEC, SEA, SSI, and SAS do so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the ’997 patent. Upon information and belief, SEC, SEA, SSI, and SAS intend to cause infringement by these manufacturers, distributors, importers, customers and/or consumers. SEC, SEA, SSI, and SAS have taken affirmative steps to induce its infringement by, *inter alia*, creating advertisements that promote the infringing use of the infringing products, creating an established distribution channel for these products into and within the United States, manufacturing these products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States.

40. Upon information and belief, Samsung’s acts of infringement of the ’997 patent have been willful and intentional. Since at least the above-mentioned date of notice, Samsung

has acted with an objectively high likelihood that its actions constitute infringement of the ’997 patent by refusing to take a license and continuing to make and sell infringing products. The objectively-defined risk was either known or so obvious that it should have been known.

41. As a direct and proximate result of these acts of patent infringement, Samsung has encroached on the exclusive rights of Plaintiff to practice the ’997 patent, for which Plaintiff is entitled to at least a reasonable royalty.

**CONCLUSION**

42. Plaintiff is entitled to recover from Samsung the damages sustained by Plaintiff as a result of Samsung’s wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

43. Plaintiff has incurred and will incur attorneys’ fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute create an exceptional case within the meaning of 35 U.S.C. § 285, and Plaintiff is entitled to recover its reasonable and necessary attorneys’ fees, costs, and expenses.

**JURY DEMAND**

44. Plaintiff hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

**PRAYER FOR RELIEF**

45. Plaintiff respectfully requests that the Court find in its favor and against Samsung, and that the Court grant Plaintiff the following relief:

A. A judgment that Samsung has infringed the patents-in-suit as alleged herein, directly and/or indirectly by way of inducing infringement of such patents;

B. A judgment for an accounting of all damages sustained by Plaintiff as a result of the acts of infringement by Samsung;

C. A judgment and order requiring Samsung to pay Plaintiff damages under 35 U.S.C. § 284, including up to treble damages for willful infringement as provided by 35 U.S.C. § 284, and any royalties determined to be appropriate;

D. A permanent injunction enjoining Samsung and its officers, directors, agents, servants, employees, affiliates, divisions, branches, subsidiaries, parents and all others acting in concert or privity with them from direct and/or indirect infringement of the patents-in-suit pursuant to 35 U.S.C. § 283;

E. A judgment and order requiring Samsung to pay Plaintiff pre-judgment and post-judgment interest on the damages awarded;

F. A judgment and order finding this to be an exceptional case and requiring Samsung to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. § 285; and

G. Such other and further relief as the Court deems just and equitable.

Respectfully submitted,

MCCARTER ENGLISH LLP

*/s/ Daniel M. Silver*

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*mting@tklg-llp.com*

*Counsel for Plaintiff*
HOME SEMICONDUCTOR CORPORATION

Dated: December ___, 2018

# Exhibit A

US005452261A

# United States Patent [19]

Chung et al.

[11] Patent Number: 5,452,261

[45] Date of Patent: Sep. 19, 1995

[54] **SERIAL ADDRESS GENERATOR FOR BURST MEMORY**

[75] Inventors: **Jinyong Chung**, Los Altos Hills, Calif.; **Michael A. Murray**, Bellevue, Wash.

[73] Assignee: **Mosel Vitelic Corporation**, San Jose, Calif.

[21] Appl. No.: **265,535**

[22] Filed: **Jun. 24, 1994**

[51] **Int. Cl.**[6] ..... **G11C 8/00**

[52] **U.S. Cl.** ..... **365/233**; 365/221; 365/236; 365/239; 365/230.06; 365/230.08

[58] **Field of Search** ..... 365/230.01, 230.06, 365/230.08, 230.09, 236, 239, 240, 221, 233

[56] **References Cited**

U.S. PATENT DOCUMENTS

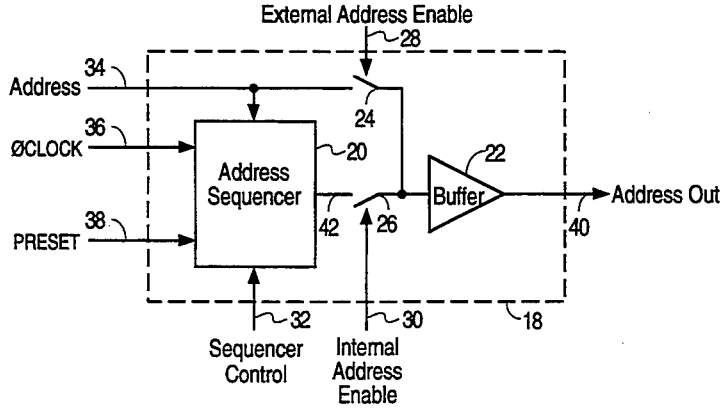
| | | | |
|---|---|---|---|
| 5,097,447 | 3/1992 | Ogawa | 365/230.09 X |
| 5,146,431 | 9/1992 | Eby | 365/236 X |
| 5,260,905 | 11/1993 | Mori | 365/230.09 X |

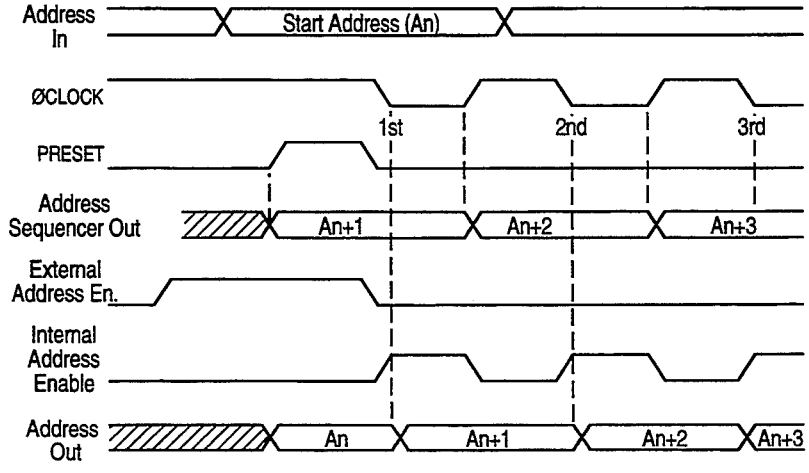
*Primary Examiner*—David C. Nelms
*Assistant Examiner*—Son Mai
*Attorney, Agent, or Firm*—Skjerven, Morrill, MacPherson, Franklin & Friel; Norman R. Klivans

[57] **ABSTRACT**

A serial address generator for a sequential (burst mode) random access memory generates a sequence of internally generated addresses for fast cycling. The start address is externally provided. Then, as the clock signals arrive, the subsequent addresses are generated in sequence by the address sequencer. The address sequencer is preset to the second address in the sequence following the start address. Simultaneously, the start address is connected by an external address enable switch to an output terminal of the address generator, bypassing the address sequencer. When the first clock signal arrives at the address sequencer, the address sequencer output is sampled by closing an internal address enable switch and opening the external address enable switch. Thus the internally generated addresses are provided immediately following the start address. The address sequencer thereby generates each address one clock cycle ahead of that in the prior art, and the output address is provided one half clock cycle ahead of that in the prior art.

**14 Claims, 16 Drawing Sheets**



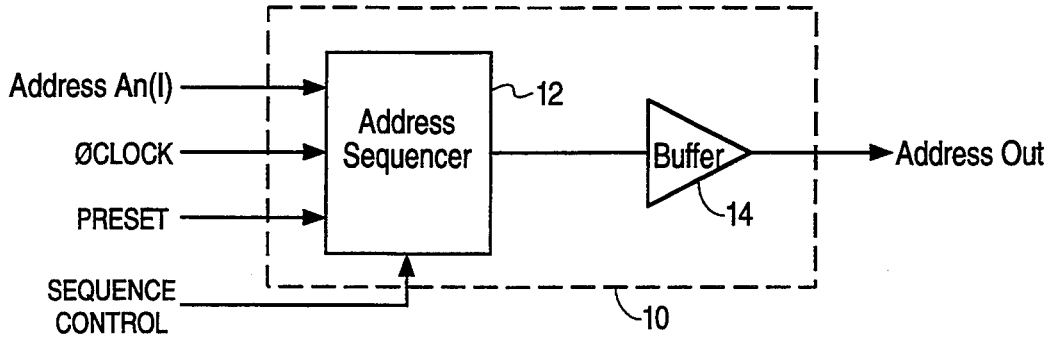



FIG. 1A
(PRIOR ART)

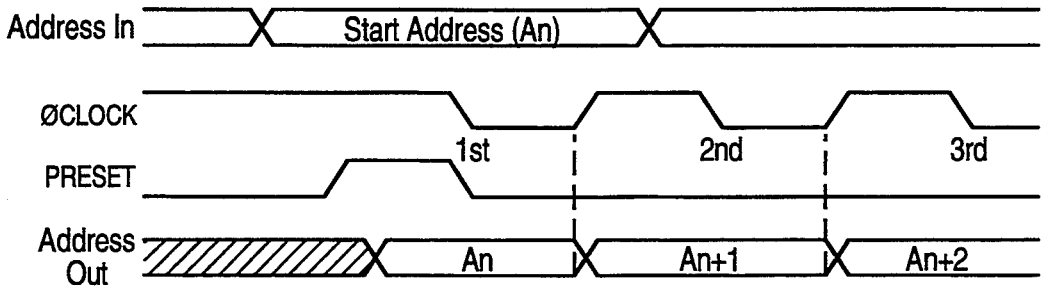



FIG. 2A
(PRIOR ART)

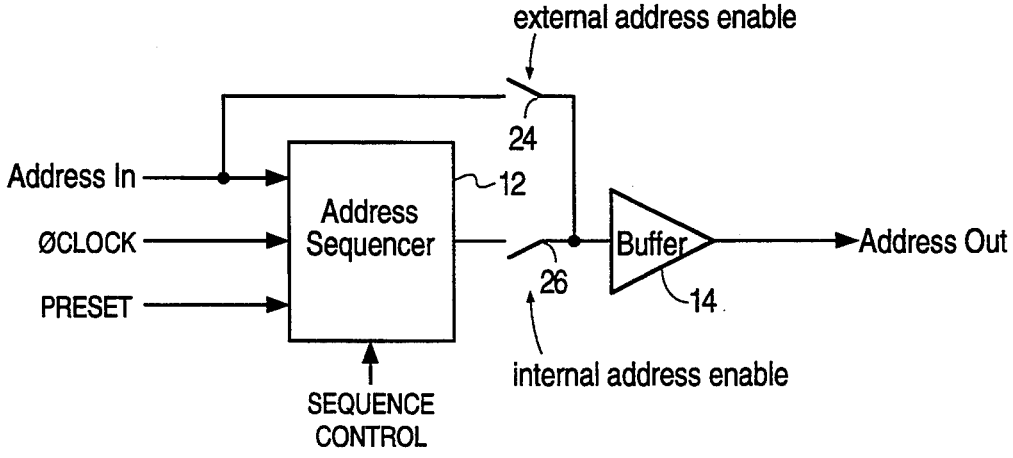



FIG. 1B
(PRIOR ART)

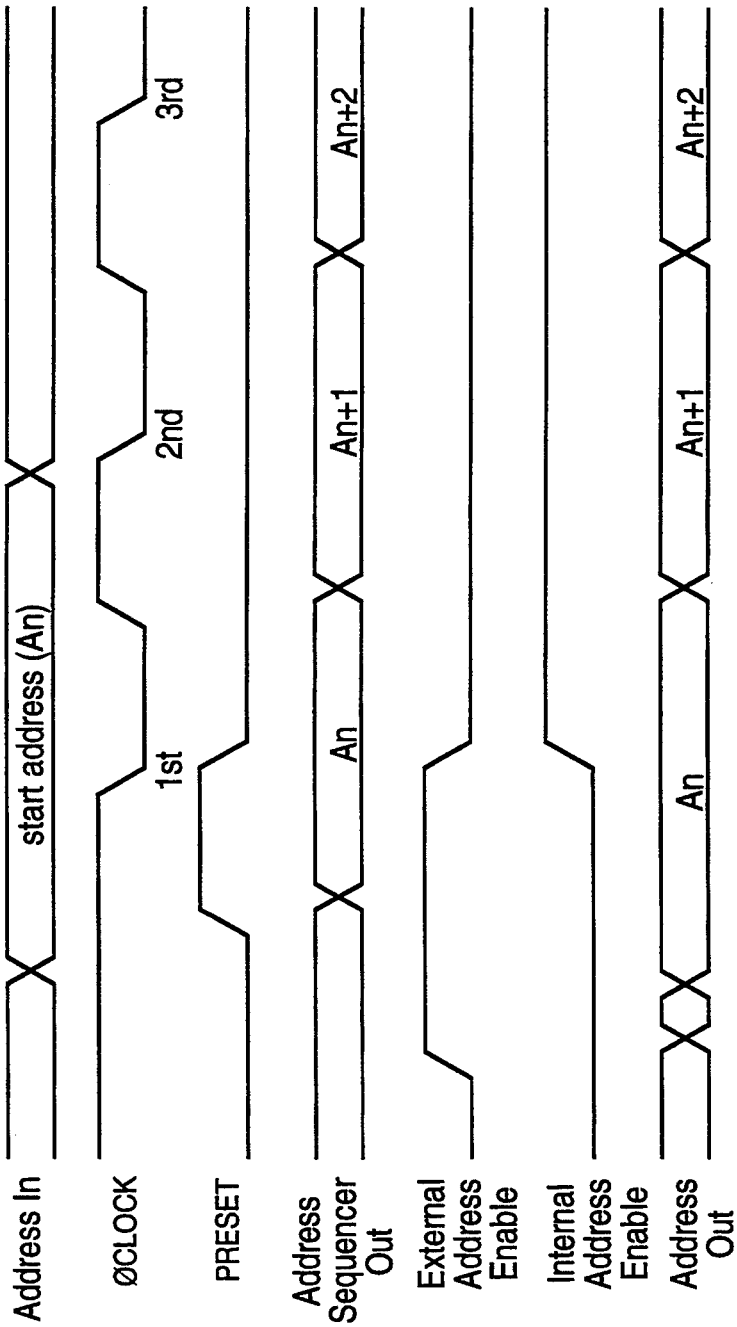



FIG. 2B
(PRIOR ART)

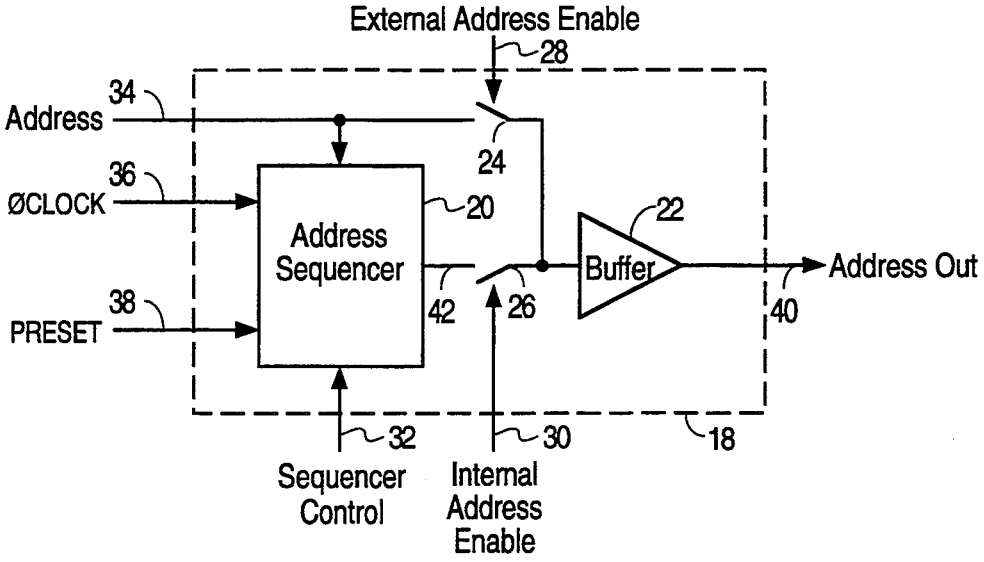

External Address Enable
28
34
Address
24
36
ØCLOCK
Address Sequencer
20
22
Buffer
Address Out
38
PRESET
42
26
40
32
30
18
Sequencer Control
Internal Address Enable

FIG. 3

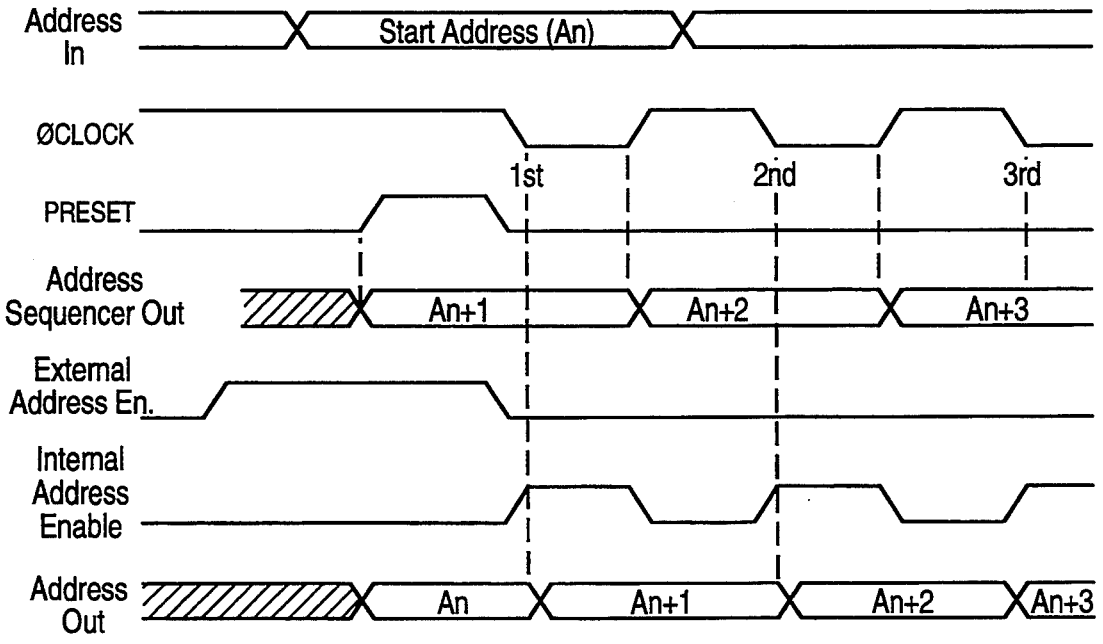

Address In
Start Address (An)
ØCLOCK
1st
2nd
3rd
PRESET
Address Sequencer Out
An+1
An+2
An+3
External Address En.
Internal Address Enable
Address Out
An
An+1
An+2
An+3

FIG. 4

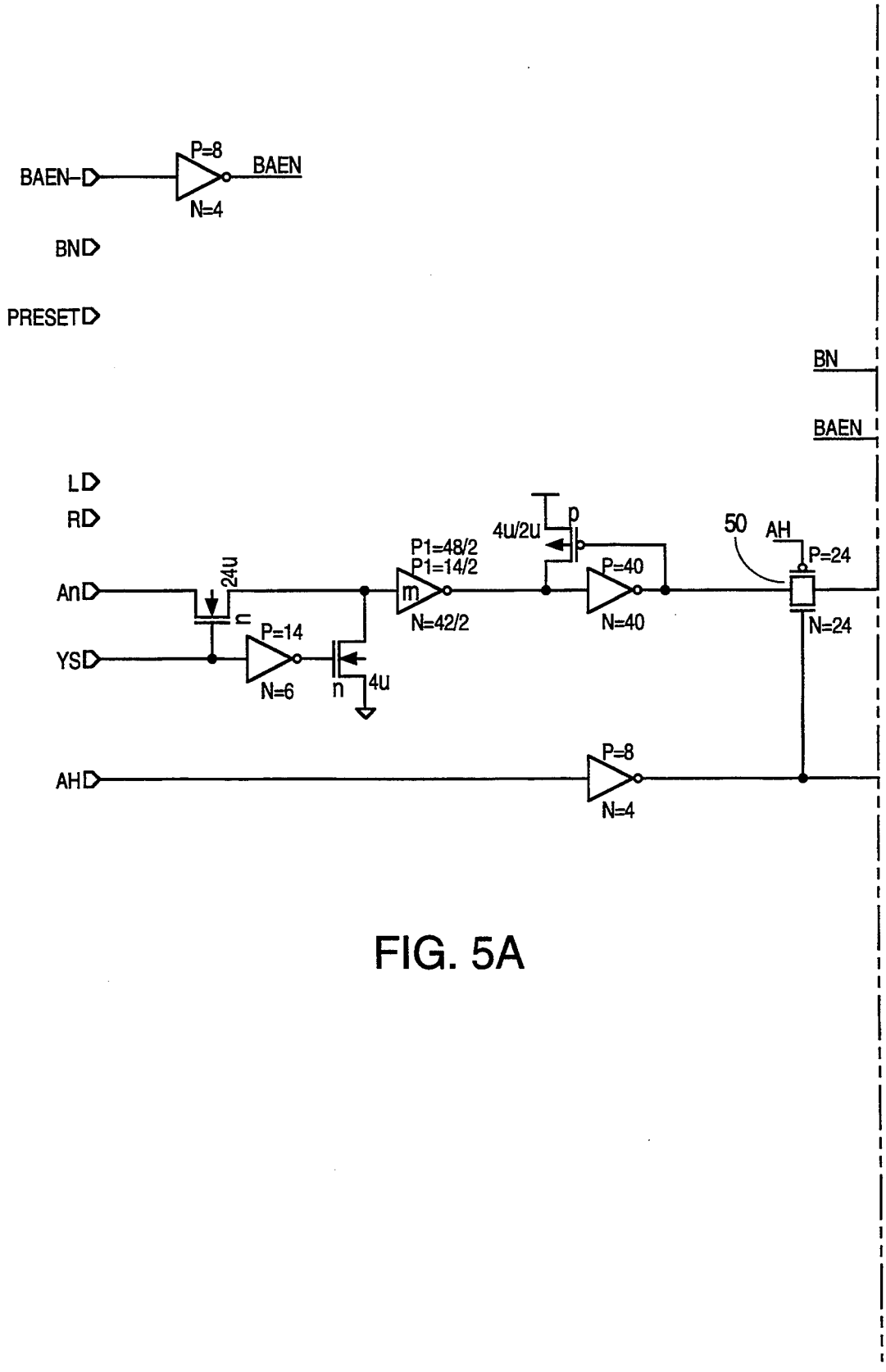

BAEN-
P=8
BAEN
N=4
BND
PRESETD
BN
BAEN
LD
RD
AnD
24u
n
P=14
YSD
N=6
n
4u
P1=48/2
P1=14/2
m
N=42/2
4u/2u
p
P=40
N=40
50
AH
P=24
N=24
AHD
P=8
N=4

FIG. 5A

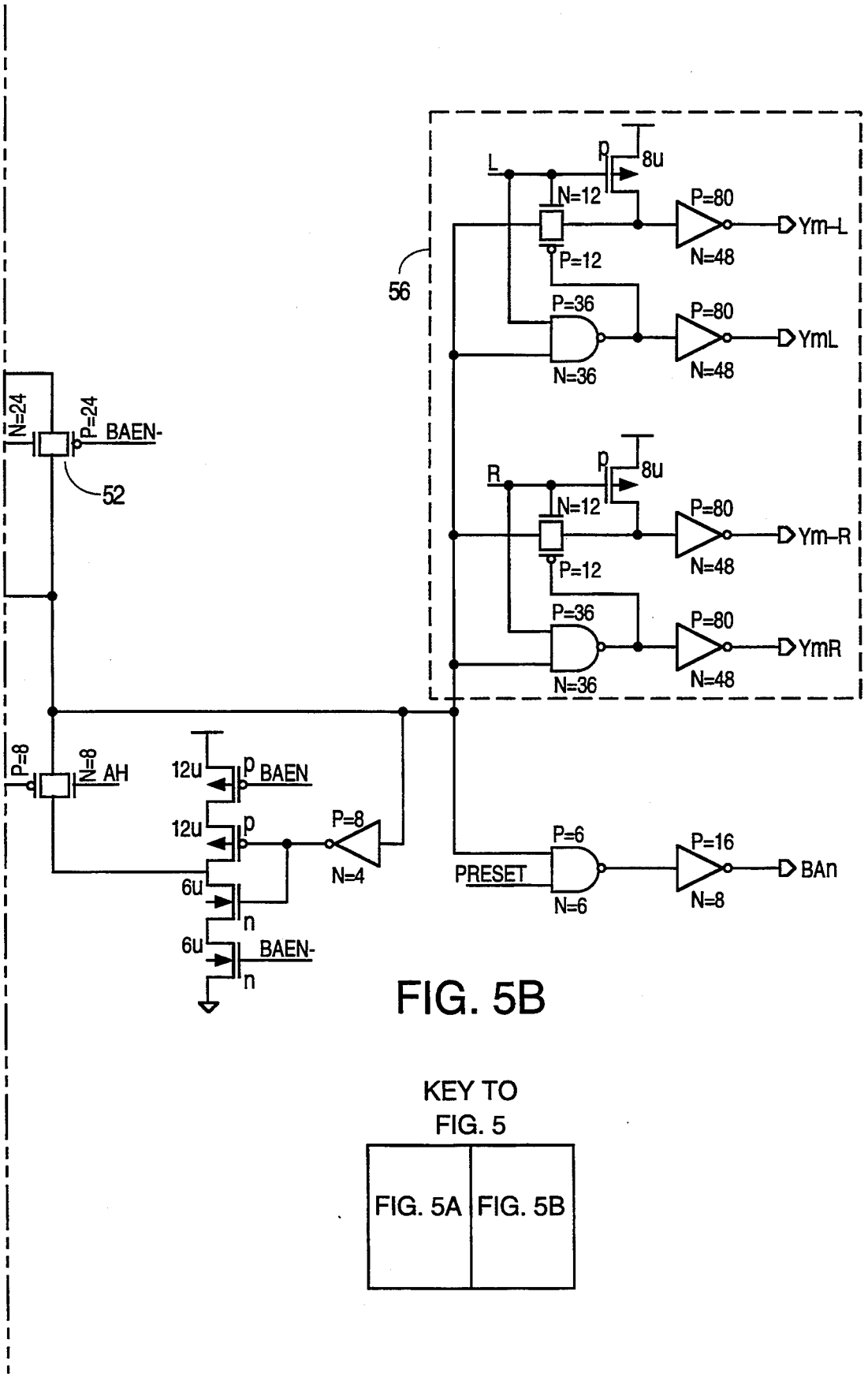



FIG. 5B

KEY TO
FIG. 5

| FIG. 5A | FIG. 5B |
|---|---|

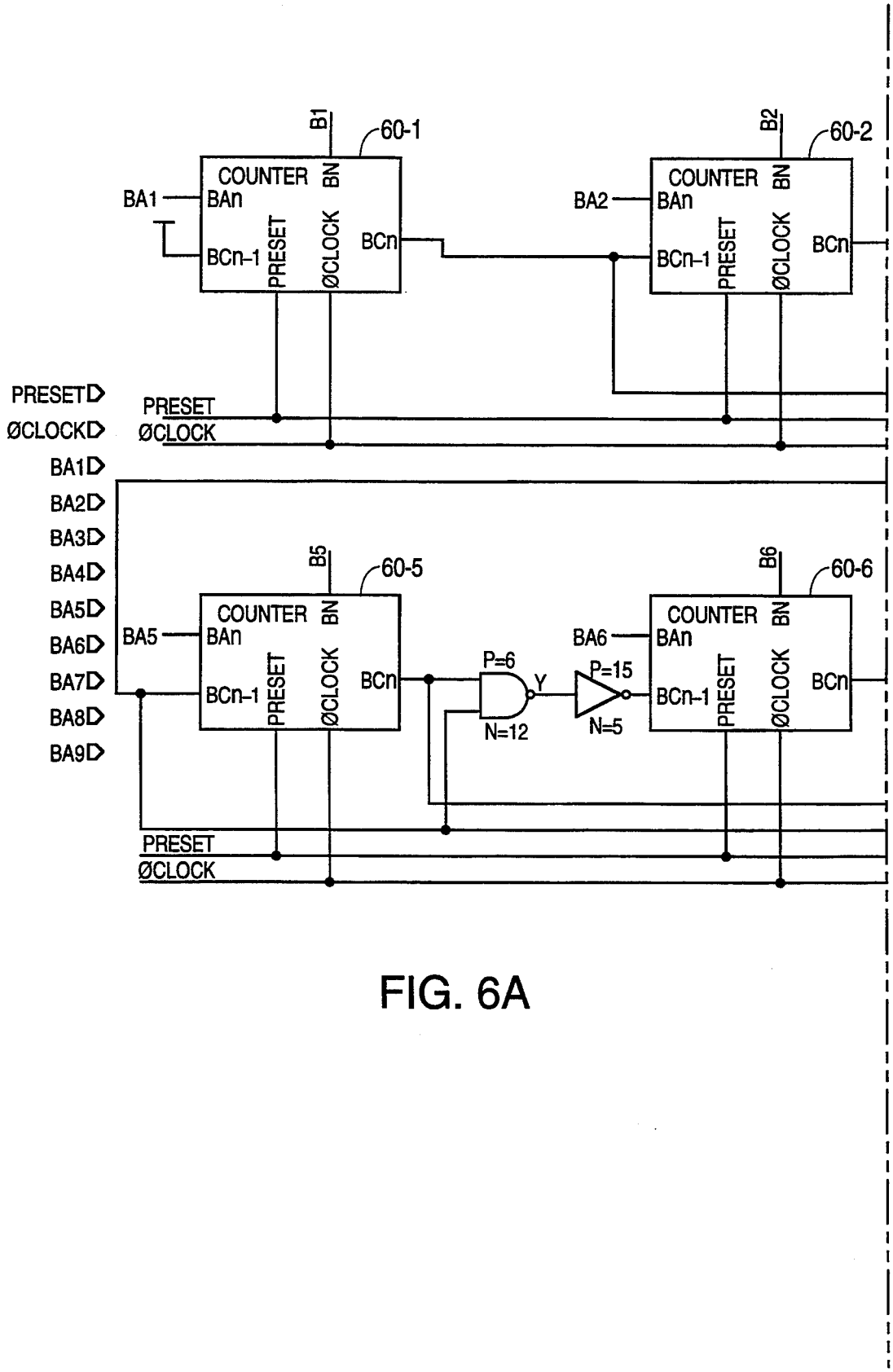

B1
60-1
COUNTER
BAn
BCn-1
PRESET
ØCLOCK
BN
BCn
BA1
B2
60-2
BA2
PRESETD
ØCLOCKD
BA1D
BA2D
BA3D
BA4D
BA5D
BA6D
BA7D
BA8D
BA9D
PRESET
ØCLOCK
B5
60-5
BA5
B6
60-6
BA6
P=6
N=12
Y
P=15
N=5

FIG. 6A

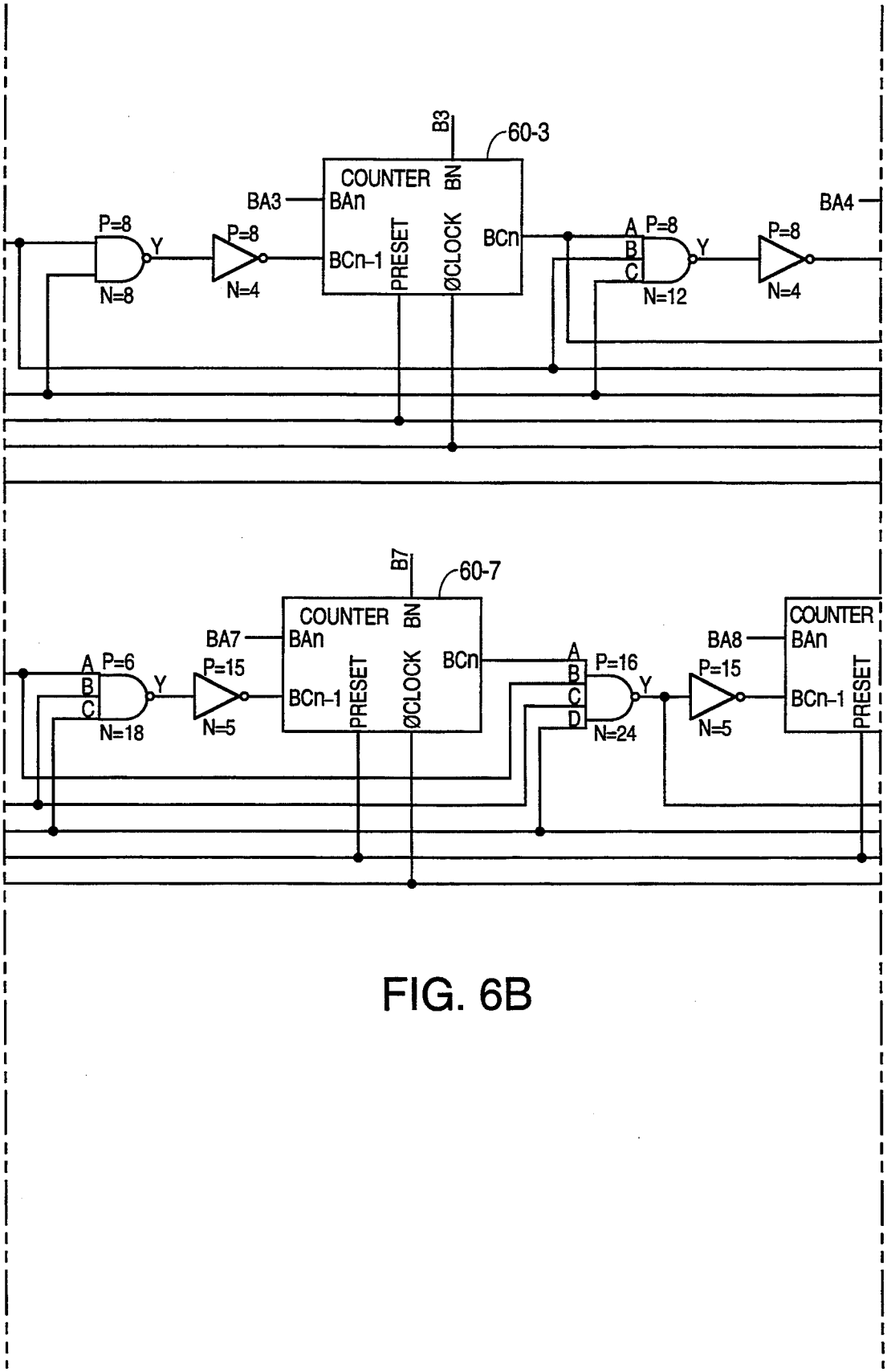

B3
60-3
COUNTER
BAn
BN
BA3
BCn-1
PRESET
ØCLOCK
BCn
BA4
P=8
Y
N=8
P=8
N=4
A
B
C
P=8
Y
N=12
P=8
N=4
B7
60-7
COUNTER
BAn
BN
BA7
BCn-1
PRESET
ØCLOCK
BCn
BA8
COUNTER
BAn
BCn-1
PRESET
A
B
C
P=6
Y
N=18
P=15
N=5
A
B
C
D
P=16
Y
N=24
P=15
N=5

FIG. 6B

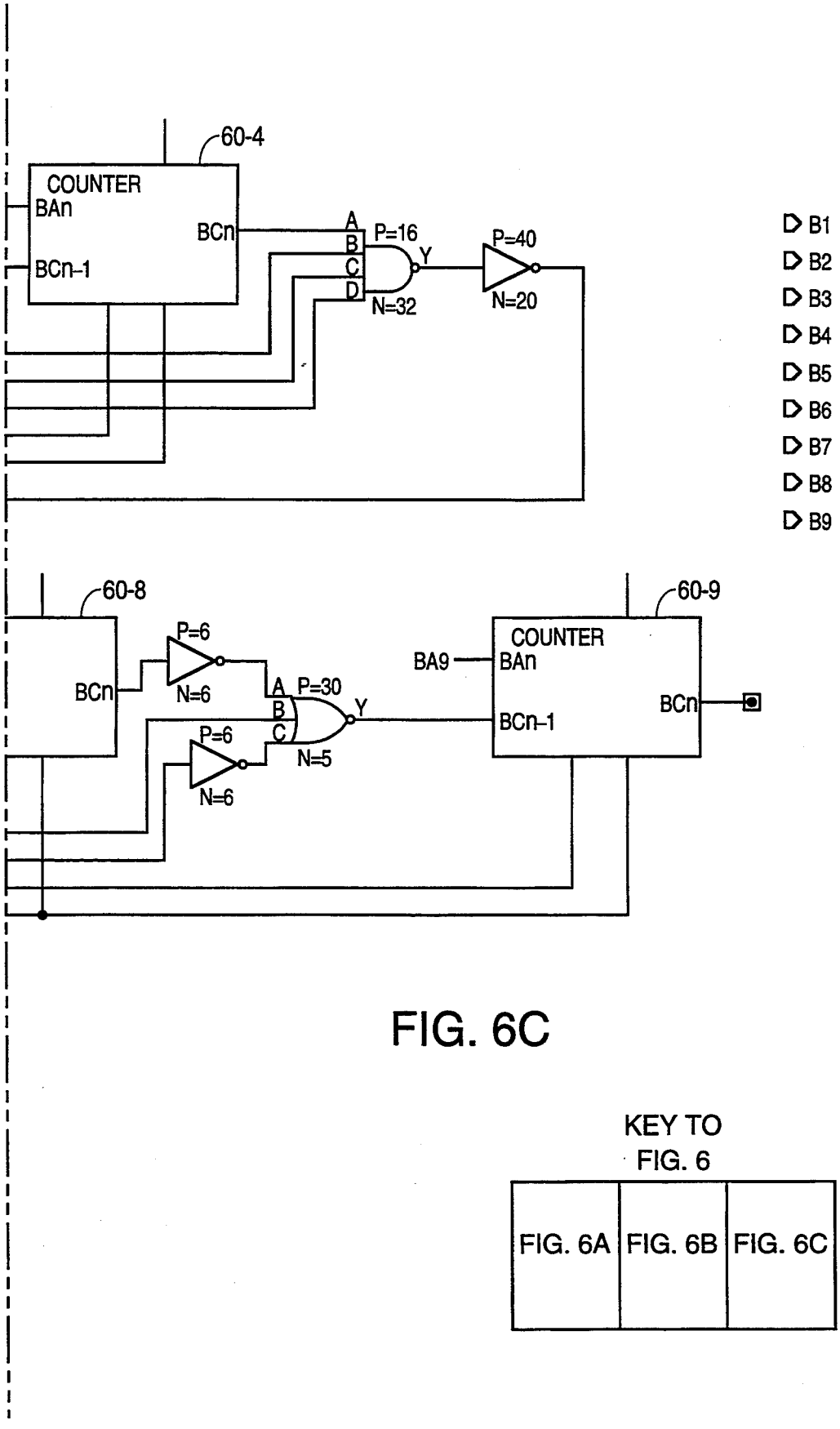



FIG. 6C

KEY TO
FIG. 6

| | | |
|---|---|---|
| FIG. 6A | FIG. 6B | FIG. 6C |

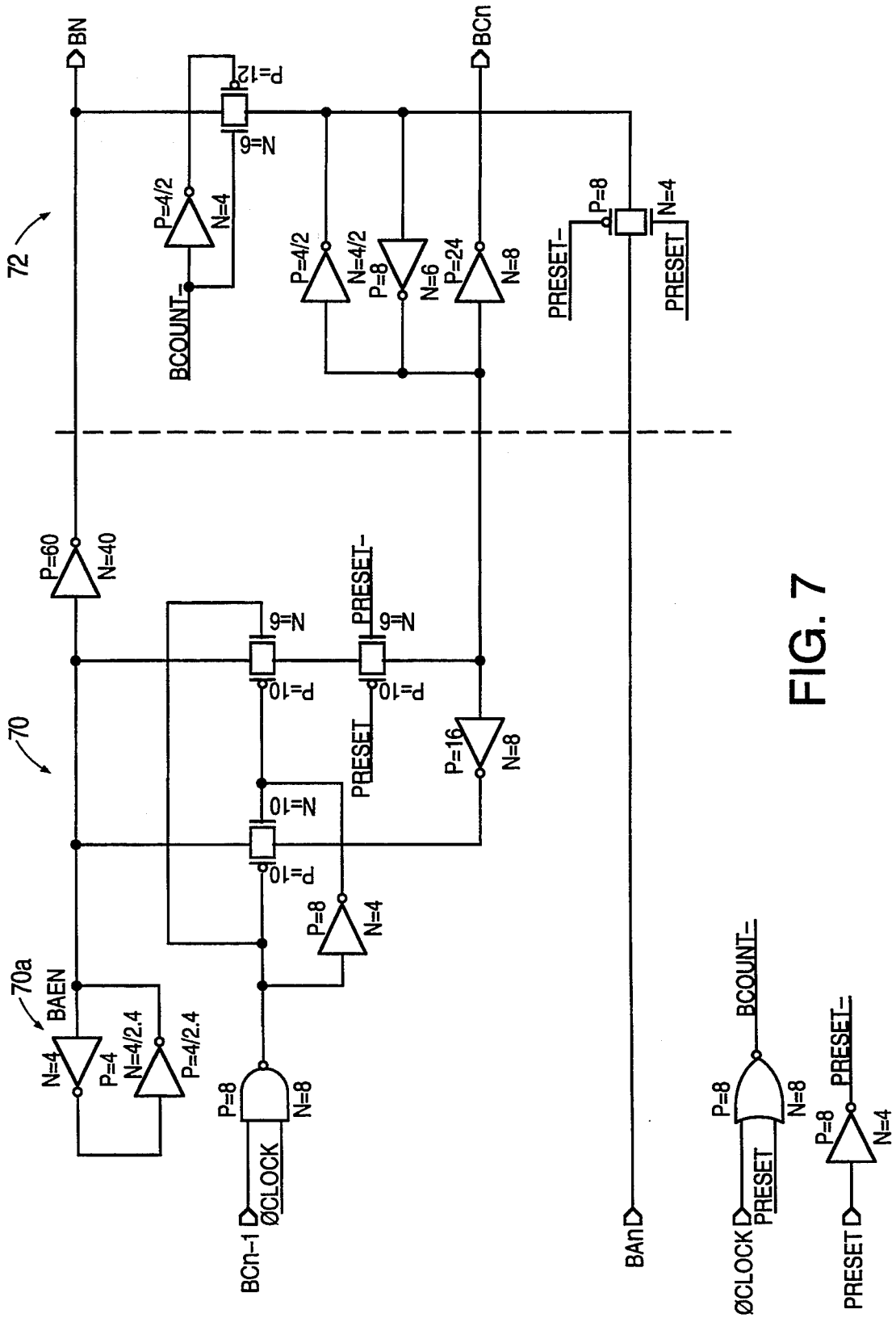

BN
BCn
72
P=12
N=6
P=4/2
N=4
BCOUNT-
P=4/2
N=4/2
P=8
N=6
P=24
N=8
PRESET-
P=8
N=4
PRESET
70
P=60
N=40
N=6
PRESET-
N=6
P=10
P=10
PRESET
P=16
N=8
N=10
P=10
P=8
N=4
70a
BAEN
N=4
P=4
N=4/2.4
P=4/2.4
P=8
N=8
BCn-1
ØCLOCK
BAnD
P=8
N=8
BCOUNT-
ØCLOCK
PRESET
P=8
N=4
PRESET-
PRESET

FIG. 7

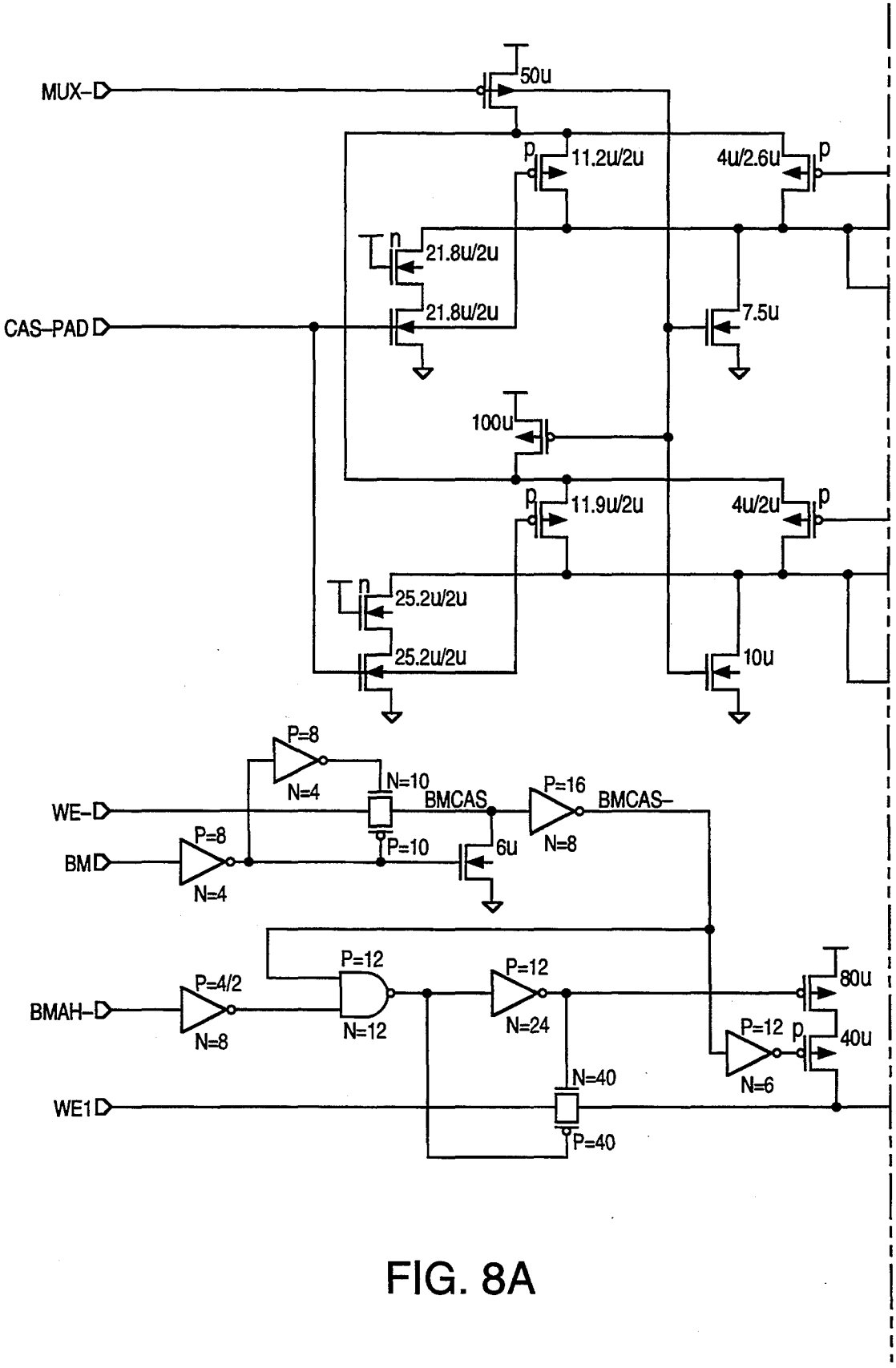

MUX–
50u
p
11.2u/2u
4u/2.6u
p
n
21.8u/2u
CAS–PAD
21.8u/2u
7.5u
100u
p
11.9u/2u
4u/2u
p
n
25.2u/2u
25.2u/2u
10u
P=8
N=4
N=10
WE–
BMCAS
P=16
BMCAS–
P=8
BM
P=10
6u
N=8
N=4
P=12
P=12
80u
P=4/2
BMAH–
N=12
N=24
P=12
p
40u
N=8
N=6
N=40
WE1
P=40

FIG. 8A

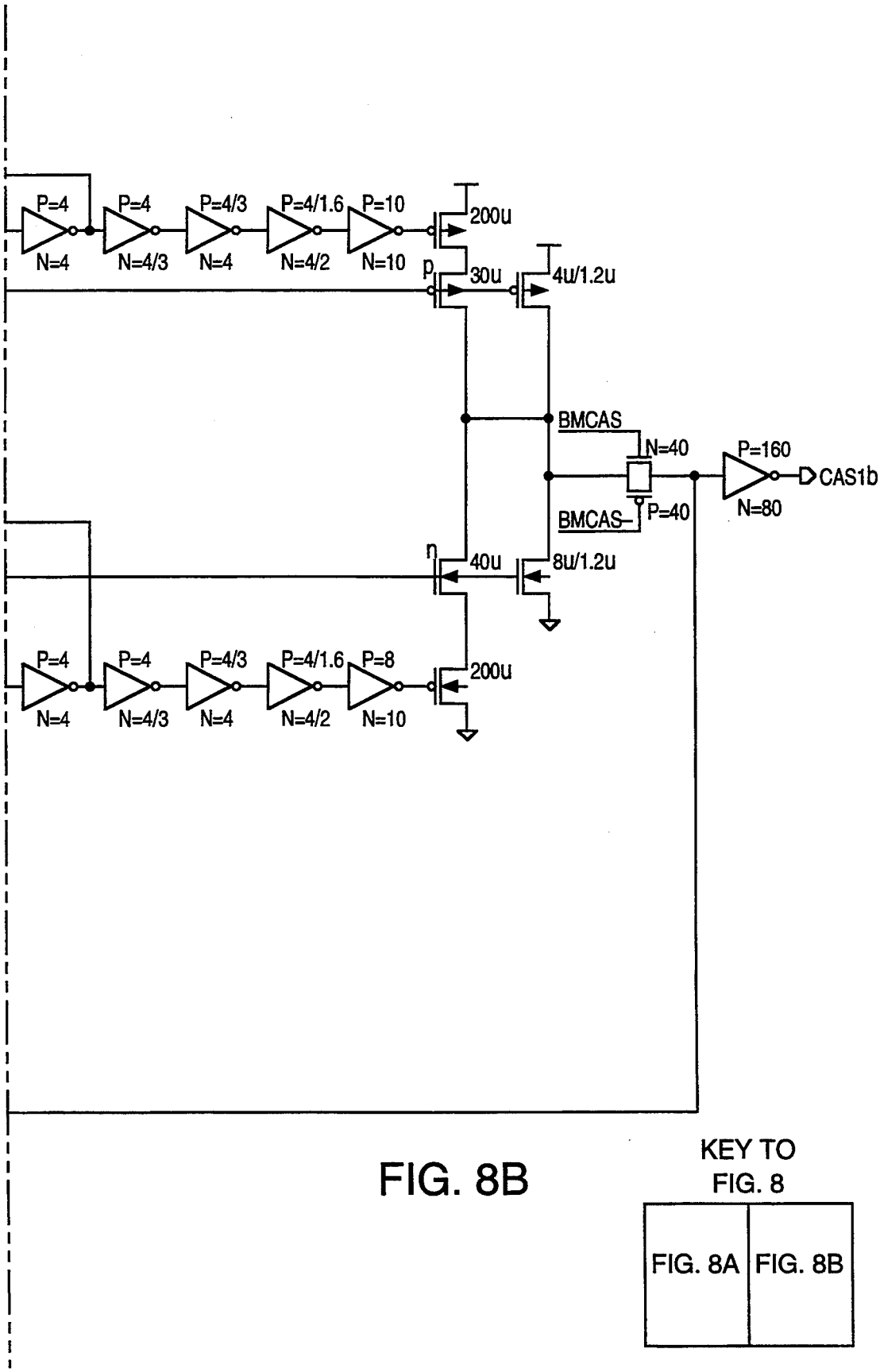



FIG. 8B

KEY TO FIG. 8

| FIG. 8A | FIG. 8B |
|---|---|

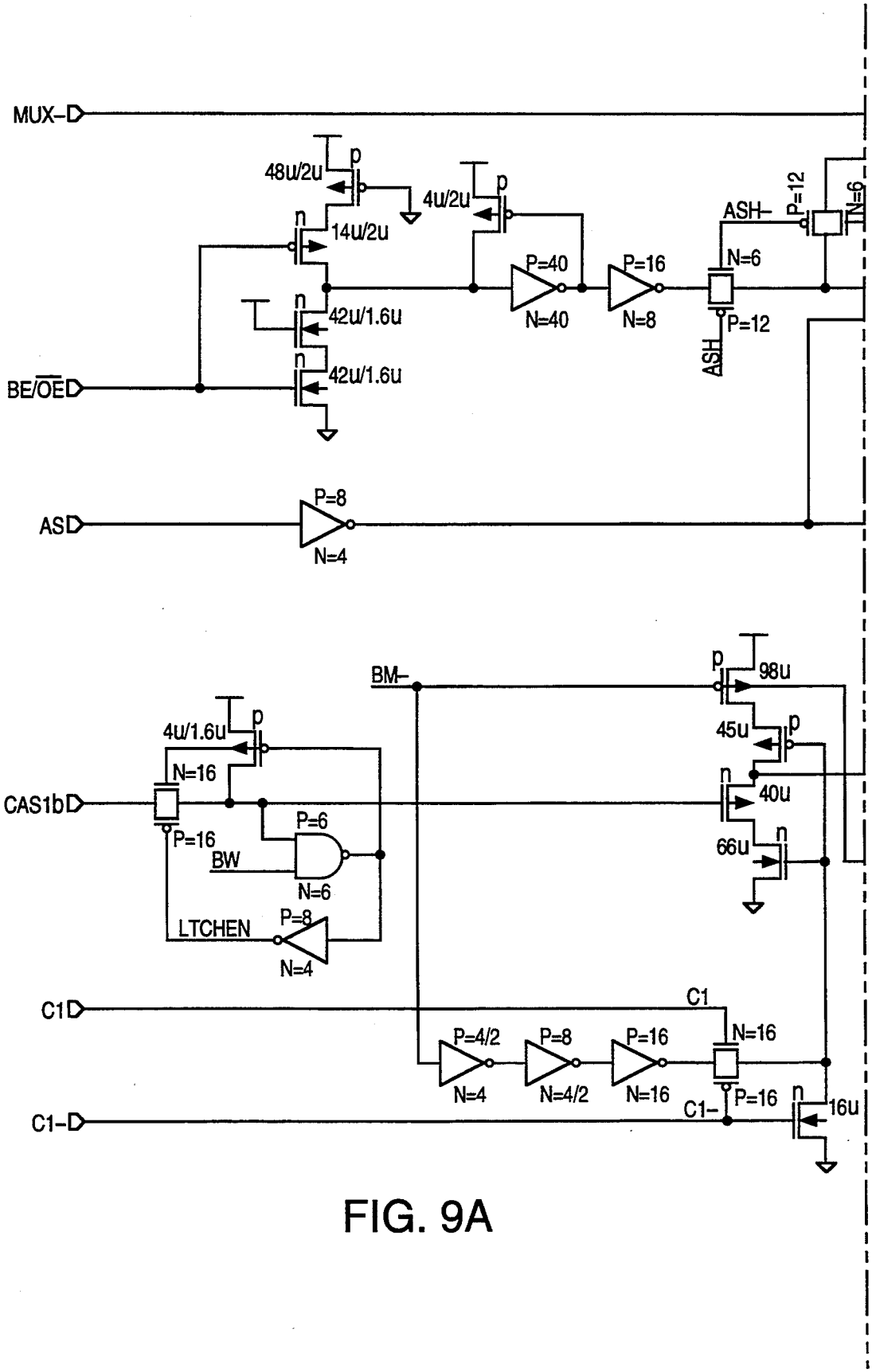

MUX–D
48u/2u
p
4u/2u
p
n
14u/2u
P=40
N=40
P=16
N=8
ASH–
P=12
N=6
P=12
ASH
n
42u/1.6u
n
42u/1.6u
BE/OED
ASD
P=8
N=4
BM–
p
98u
45u
p
n
40u
66u
n
4u/1.6u
p
N=16
P=16
CAS1bD
P=6
BW
N=6
LTCHEN
P=8
N=4
C1D
C1
P=4/2
N=4
P=8
N=4/2
P=16
N=16
N=16
C1–
P=16
n
16u
C1–D

FIG. 9A

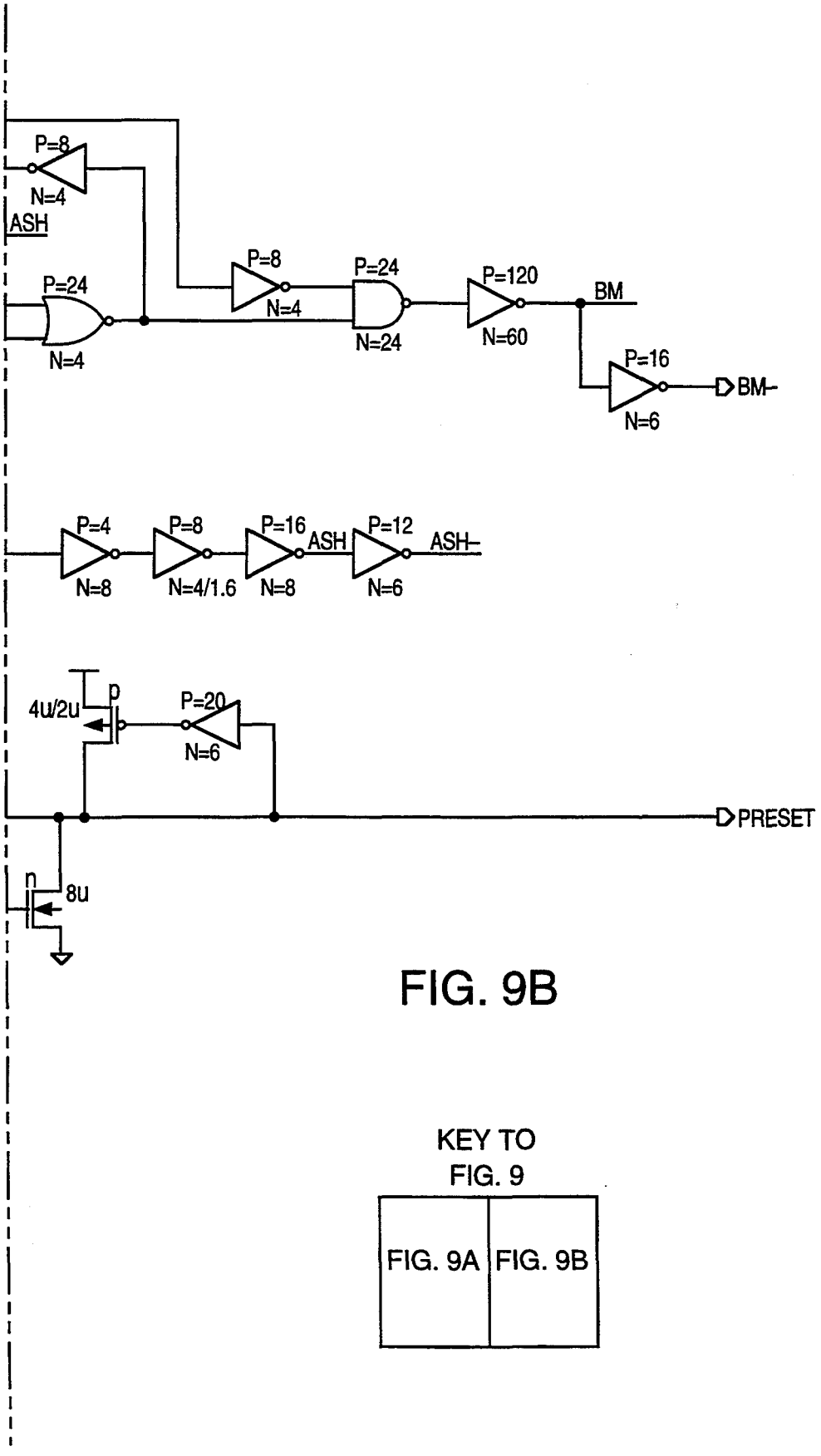



FIG. 9B

KEY TO
FIG. 9

| FIG. 9A | FIG. 9B |
|---|---|

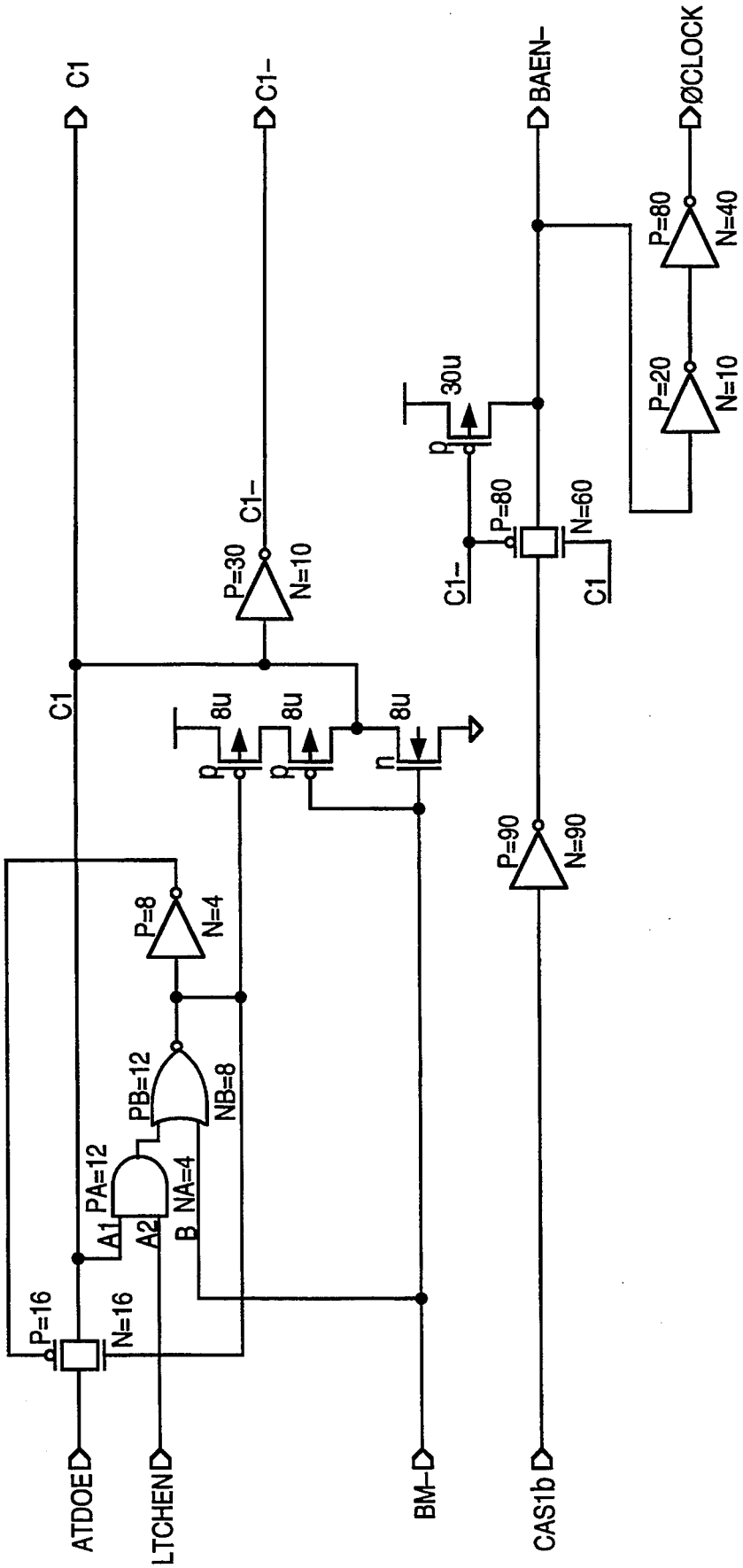

C1
C1-
BAEN-
ØCLOCK
P=80
N=40
P=20
N=10
30u
P=80
N=60
C1-
C1
P=30
N=10
C1
8u
8u
8u
P=90
N=90
P=8
N=4
PB=12
NB=8
PA=12
NA=4
A1
A2
B
P=16
N=16
ATDOE
LTCHEN
BM-
CAS1b

FIG. 10

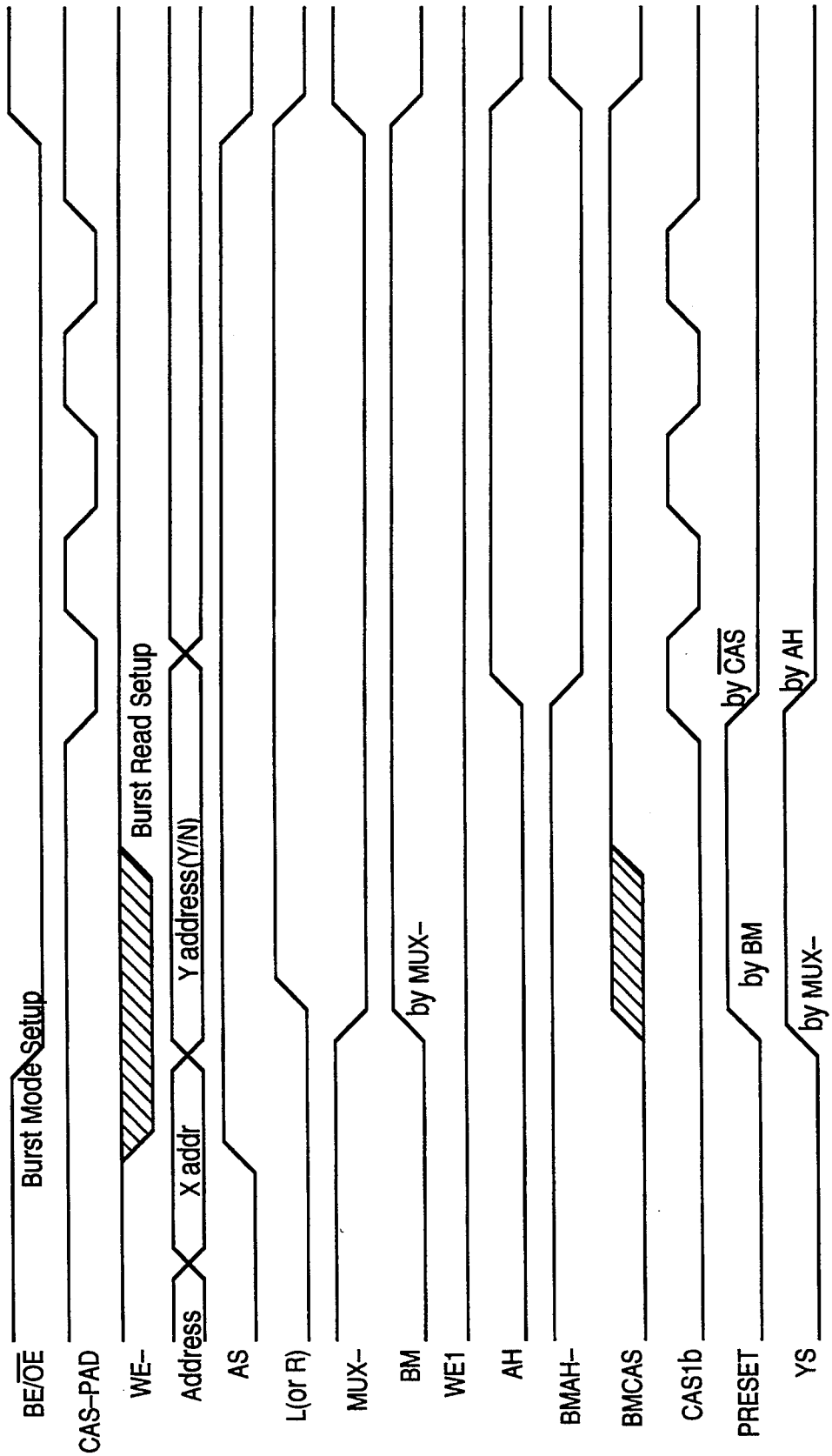

BE/OE
Burst Mode Setup
CAS-PAD
WE-
Burst Read Setup
Address
X addr
Y address(Y/N)
AS
L(or R)
MUX-
BM
by MUX-
WE1
AH
BMAH-
BMCAS
CAS1b
PRESET
by BM
by CAS
YS
by MUX-
by AH

FIG. 11A

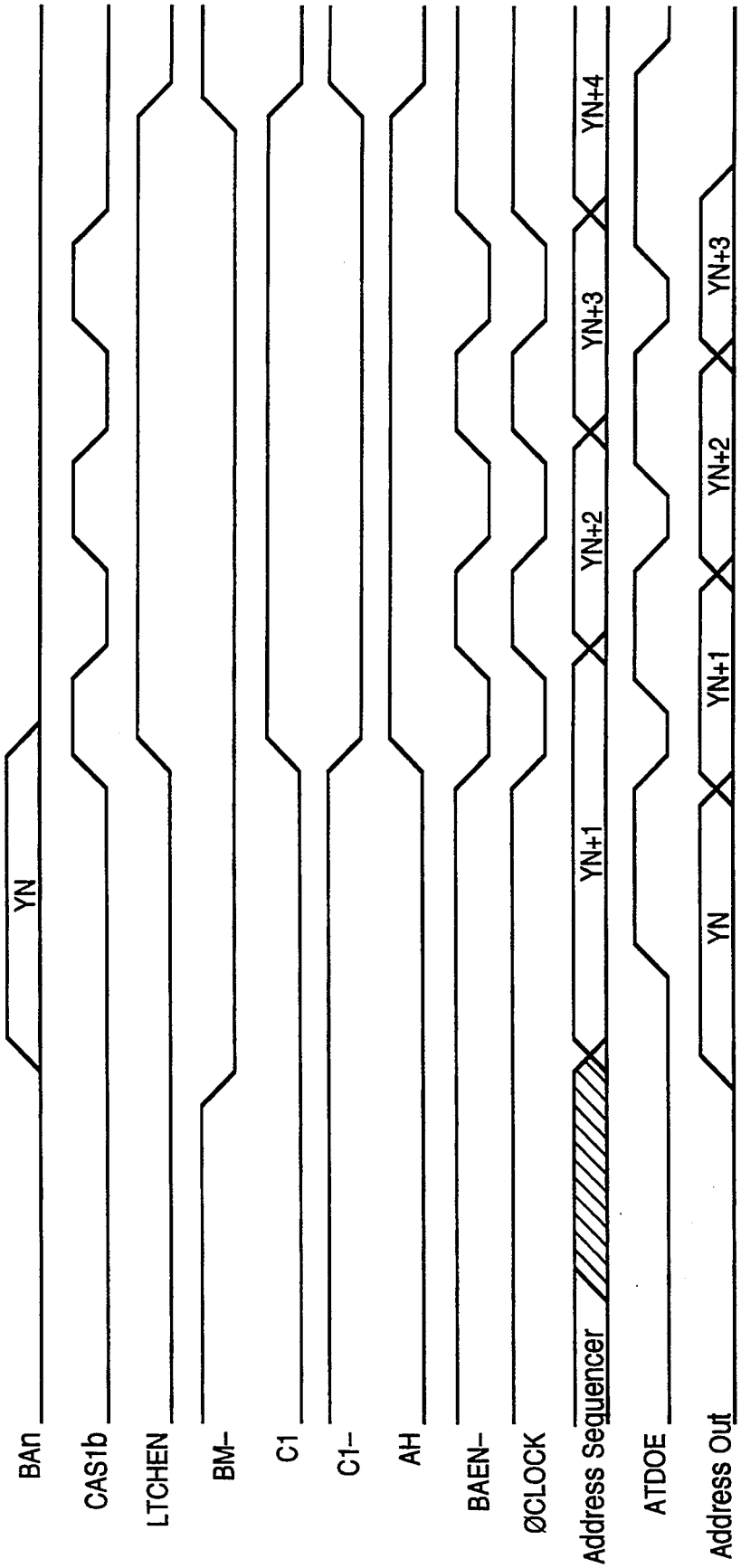

BAn
CAS1b
LTCHEN
BM–
C1
C1–
AH
BAEN–
ØCLOCK
Address Sequencer
ATDOE
Address Out
YN
YN+1
YN+2
YN+3
YN+4

FIG. 11B

# SERIAL ADDRESS GENERATOR FOR BURST MEMORY

## BACKGROUND OF THE INVENTION

1. Field of the Invention

This disclosure relates to random access memory and specifically to a serial address generator for a burst-type random access memory.

2. Description of the Prior Art

Video RAM (random access memory), synchronous RAM and burst RAM each require a sequence of internally generated addresses for faster cycling and prevention of the external address bus lines from fast switching to suppress switching noise in the system. Typically the start address of a particular address burst is provided from an external source (a host computer or a processor) and as subsequent clock signals arrive at the address generator, the following addresses in the burst are generated continuously in sequence for the duration of the burst. The prior art presets the address sequencer (typically a counter) to the externally provided start address ($A_n$) in response to a PRESET signal. The address sequencer output is updated with each $\phi_{clock}$ rising edge, and the outputs of the address generator are sequentially $A_n$, $A_{n+1}$, $A_{n+2}$, etc.

Such a prior art address generator is shown in FIG. 1A including address sequencer **12** outputting the sequence of addresses to an output buffer **14**. The three input signals to the address sequencer **12** are the input address signal (the start address $A_n$), the $\phi_{clock}$ signal, and the PRESET signal. Additionally, a sequence control signal controls whether the address sequencer **12** counts up or down. In most applications, upcounting is used, and this function is built in, rather than being a control function. The associated timing diagram is shown in FIG. 2A.

Typically the address sequencer **12** (counter) includes a master side and a slave side, each initially set to the start address $A_n$. It is to be understood that the device of FIG. 1A is a parallel device, where the start address $A_n$ is a multi-bit address provided by a plurality of lines, i.e. an address bus. The address out signal is also provided on a multi-line bus.

As seen in FIG. 2A, the first address out $A_n$ is output to buffer **14** when the Preset signal is applied, and kept until leading edge of $\phi_{clock}$ arrives. The second address out $A_{n+1}$ is output to buffer **14** at the trailing edge of $\phi_{clock}$ and the following addresses are updated at every trailing edge of the $\phi_{clock}$ signal.

The address generator of FIG. 1A functions adequately; however it is slower than desired. Faster operation is desirable to improve system performance such as needed in a typical burst DRAM (dynamic random access memory) chip. The FIG. 1A address generator delivers the first address late, due to the propagation delay through the counters inside the address sequencer. This means a shorter start address duration time.

To improve the start address delivery, in a second prior art address generator the start address is provided from the Address Input directly, instead of going through the counters. (See FIG. 1B, and corresponding timing diagram FIG. 2B).

Rather than providing the start address $A_n$ to the address sequencer as in FIG. 1A, the address sequencer **12** of FIG. 1B is bypassed before and during the preset period by means of external address enable switch **24** and internal address enable switch **26**, and the start address is provided directly to the output buffer via external address enable switch **24**. This (start) address $A_n$ is therefore available almost immediately as the address out at buffer **14**, without processing by the address sequencer **12**.

However, further performance improvement (i.e., higher speed) is desirable in terms of address output.



## SUMMARY OF THE INVENTION

In the above described prior art, the second address $A_{n+1}$ is delivered by the address sequencer to the output buffer at the time of the trailing edge of the first $\phi_{clock}$ cycle. In accordance with the invention, instead the second address $A_{n+1}$ is delivered to the output buffer at the leading edge of the $\phi_{clock}$ signal. Thus one half of a clock cycle is gained for each address burst.

After provision to the output buffer of the first address $A_n$ (which is externally supplied as in FIG. 1B) the external address line is disconnected from the output buffer by an external address enable switch, and an internal address enable switch which connects the address sequencer to the output buffer is closed, allowing the address sequencer to provide the subsequent internally generated address $A_{n+1}$ to the output buffer, also as in FIG. 1B. Then, during the time that the start address $A_n$ is being provided to the output buffer, the address sequencer operates to calculate the subsequent address $A_{n+1}$. The output addresses of each burst are thereby, each provided to the output buffer approximately $\frac{1}{2}$ of a clock cycle earlier than in the prior art of FIG. 1B.

The externally provided address and the address out both begin with the same address $A_n$ which is the initial address in the burst, while using the preset signal to advance the counting of the sequence by one count.

Therefore, the address sequencer is preset to address $A_{n+1}$ (the second address in the burst) following the externally provided start address $A_n$. When the first clock signal arrives at the address sequencer, the address sequencer output is sampled by enabling the internal address enable (second) switch and disabling the external address enable (first) switch. The address sequencer output is updated with each rising edge of the clock signal $\phi_{clock}$. Thereby the address sequencer generates each address one clock cycle ahead of the time that address would have been generated in the prior art, and the address output is supplied to the output buffer $\frac{1}{2}$ clock cycle ahead of the prior art (FIG. 2B) timing. As in the prior art, the address sequencer includes a master/slave counter. However, in accordance with the invention and in order to set the address sequencer initially to the second address $A_{n+1}$, the master side of the counter is initially set to value $A_n$, and the slave side of the counter is initially set to value $A_{n+1}$. This provides the desired incremental timing advantage over the prior art.

The present invention is applicable specifically to burst DRAM (dynamic RAM) operating in page mode, and is also applicable to other types of burst memory using sequential type addressing.

In accordance with the invention, operation of the address generator is the same as in the prior art except during the preset cycle. Thus the performance advantage is gained during the preset portion of the address burst. Since the addresses are output one-half cycle ahead of that provided in the prior art, this improves the

operational performance of the system in which the burst memory is installed.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A, 1B** show prior art address generators.

FIGS. **2A, 2B** show timing diagrams for the prior art address generators of respectively FIGS. **1A, 1B**.

FIG. **3** shows an address generator in accordance with the present invention.

FIG. **4** shows a timing diagram for the address generator of FIG. **3**.

FIG. **5** shows a schematic of the internal address enable switch, external address enable switch, and output buffer in accordance with the present invention.

FIG. **6** shows a counter in accordance with the present invention.

FIG. **7** shows detail of one cell of the counter of FIG. **6**.

FIGS. **8, 9,** and **10** show circuitry for generation of the timing signals for the address generator in accordance with the present invention.

FIGS. **11**(*a*) and **11**(*b*) show a timing diagram for an address generator in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

FIG. **3** shows in a block diagram serial address generator **18** in accordance with the invention. Address generator **18** includes address sequencer **20**, output buffer **22**, external address enable switch **24** (as in FIG. **1B**) actuated by an external address enable control signal **28**, and internal address enable switch **26** (as in FIG. **1B**) actuated by an internal address enable control signal **30**. Thus the serial address generator of FIG. **3** appears in the block diagram to be similar to the serial address generator of FIG. **1B**; the distinction is in the internal structure and operation of address sequencer **20**, which differs significantly from address sequencer **12** of FIGS. **1A** and **1B**.

Sequence control signal **32** (as in the prior art) determines whether address sequencer **20** is an up or down counter. Input signals on lines **34, 36** and **38** are conventional (as in the prior art). The output address ("address out") is provided on line **40**. This circuit, like that of FIGS. **1A** and **1B**, is a parallel device providing a multibit address. Hence address line **34**, the output from the address sequencer on line **42**, and the address out line **40** each represent multi-line busses with as many lines as there are address bits in the particular application.

FIG. **4** illustrates timing for the address generator of FIG. **3**, and specifically the timing for external address switch **24** and internal address switch **26** as controlled respectively by their control signals **28, 30** of FIG. **3**. Initially, external address enable switch **24** is closed (the external address enable control signal **28** is high) thus providing the externally provided address on line **34** directly to buffer **22**. After the initial address $A_n$ (which is externally provided) is provided to buffer **22**, the signal $\phi_{clock}$ goes low, and the external address enable control signal **28** goes low, then the internal address enable signal **30** goes high, closing switch **26**. At this time the address sequencer **20** has generated the second address $A_{n+1}$.

As seen in the timing diagram of FIG. **4**, generation of the second address $A_{n+1}$ overlaps with provision of the start address $A_n$. Thus within the first two $\phi_{clock}$ cycles, all of start address $A_n$ and second address $A_{n+1}$ are output to buffer **22**, in contrast to the prior art of FIG. **2B** in which only $1\frac{1}{2}$ addresses are outputted within the first two occurrences of clock cycles $\phi_{clock}$. This half-clock cycle advantage is the chief benefit of the present invention. Thus the generation of addresses ("Address sequencer out" in FIG. **4**) is one clock cycle ahead of that in the prior art, and there is also a half clock timing advantage in the output addresses ("Address out") in contrast to the prior art of FIG. **2B**.

In one embodiment the serial address generator of FIG. **3** is for use in a burst RAM operating in page mode, with the externally provided address being the first (start) address for each page. Therefore for example a RAM chip having 512 words per page requires nine bit addresses, i.e., $2^9=512$. Thus, the address sequencer is a nine-bit counter. The serial address generator in accordance with the invention is also be suitable for other (non-page mode) types of serially generated addresses, with the addition of conventional stop circuitry to terminate a burst of predetermined length.

It is to be appreciated that the serial address generator of FIG. **3** is used in place of conventional serial address generator of FIGS. **1A, 1B** as a portion typically of a RAM chip. The address out signal provided on line **40** is conventionally connected to an address decoder which selects the desired memory cell or cells to be written to or read from. (The remainder of the RAM chip is not illustrated herein as being conventional.)

FIGS. **5** through **10** show a detailed schematic of one embodiment of the present invention, corresponding to that shown in the block diagram of FIG. **3** except that the sequence control is not shown, due to only upcounting being available. In FIGS. **5** through **10** the small numbers adjacent each logic gate indicate the width (in micrometers) of each transistor gate of the logic gate. Thus, "P" indicates the width of a P channel transistor gate and "N" indicates the width of an N channel transistor gate. The gate length is equal for all transistors except where a two number notation is used i.e., "48/2" means the transistor gate width is 48 micrometers and the transistor gate length is 2 micrometers. The standard (default) transistor gate length is 1.2 micrometers, for this embodiment.

Table 1 shows the signal designations in the block diagram FIG. **3** and the corresponding signal designations in schematic FIGS. **5** to **10**, and in the corresponding timing diagram of FIGS. **11**(*a*), **11**(*b*). In Table 1 there is no schematic equivalent to the sequence control signal in FIG. **3**, since as explained above the circuit shown in the schematic of FIGS. **5** to **10** uses "up counting" only and does not have a down counting mode option.

TABLE 1

| CHIEF SIGNALS - EQUIVALENCES | | |
|---|---|---|
| BLOCK DIAGRAM - FIG. 3 | SCEMATIC - FIGS. 5-10 | TIMING CHART - FIG. 11 |
| Start address (An) | Same | Yn |
| PRESET | Same | Same |
| External Address | $A_n$ | Address |
| Internal Address | BN, (Burst Address N) | Address Sequencer |
| $\phi_{clock}$ | $\phi_{clock}$ signal generation sequence: CAS-PAD → CAS1$_b$ → BAEN- → $\phi_{clock}$ | $\phi_{clock}$ |
| Sequence | (up counting is inherent | |

TABLE 1-continued

| CHIEF SIGNALS - EQUIVALENCES | | |
|---|---|---|
| BLOCK DIAGRAM - FIG. 3 | SCEMATIC - FIGS. 5-10 | TIMING CHART - FIG. 11 |
| Control | so this control is not required) | |
| External Address Enable | AH (address HOLD) [functions as external address latching and disable at same time] | AH |
| Internal Address Enable | BAEN- (Burst Address Enable- ) | BAEN - |
| Address Out | $Y_m$-L, $Y_m$L, $Y_m$-R, $Y_m$R (two pairs per single address), | Address Out |
| (Not Shown) | $BC_n$ (Burst Counter Carry - Output) BCN-1 (Burst Counter Carry - Input) | |

Table 2 shows the externally provided input signals/-lines for the circuit of FIGS. **5** to **10**.

TABLE 2

| EXTERNALLY PROVIDED INPUTS | |
|---|---|
| NAME | DESCRIPTION |
| $A_n$ | External address |
| $V_{cc}$ | power |
| L | left decoder address enable |
| R | right decoder address enable |
| YS | column address power up |
| AS | Address Sense |
| CAS-PAD | Column Address Strobe input |
| MUX- | Row - column address multiplex |
| BE/OE | Burst enable/output enable input |
| AH | External address enable |
| ATDOE | Output enable control |
| WE- | Write Enable- |
| WE1 | Write Enable |

Table 3 shows the output signals for the circuit of FIGS. **5** to **10**.

TABLE 3

| EXTERNAL OUTPUT SIGNALS | |
|---|---|
| NAME | DESCRIPTION |
| $Y_{m-L}$ | left address bit inverted |
| $Y_{mL}$ | left address bit |
| $Y_{m-R}$ | right address bit inverted |
| $y_{mR}$ | right address bit |

Table 4 shows the internal signals for the circuit of FIGS. **5** to **10**.

TABLE 4

| NAME | DESCRIPTION |
|---|---|
| BAEN- | Internal address enable |
| BN | Internal address |
| $BA_n$ | Internal Start Address |
| BM | Burst mode |
| $BC_n$ | Counter carry output |
| $BC_n$-1 | Counter carry input |
| PRESET | Preset Timing |
| $CAS1_b$ | Timing |
| $\phi_{clock}$ | $\phi$ Clock Timing |

FIG. **5** corresponds most closely to the block diagram of FIG. **3**; however FIG. **5** is for a single address bit and hence shows only one of nine such identical circuits as would be used in FIG. **3**. These nine circuits are connected in parallel to provide a nine bit address output signal in this particular exemplary embodiment of the invention.

With reference to FIG. **5**, input signal An corresponds to the external Address $A_n$ on line **34** in FIG. **3**. Signal AH (address hold) functions as the external address latching and disable. This is the external address enable signal, controlling switch **50** in FIG. **5** which corresponds to switch **24** in FIG. **3**.

Similarly, the internal address supplied on line **42** of FIG. **3** is designated signal BN in FIG. **5**, and is provided as an input to switch **52** corresponding to switch **26** in FIG. **3**. Switch **52** is controlled by the internal address enable signal which in FIG. **5** is designated BAEN-. (The inverse of signal BAEN.) It is to be understood that the signal BN is provided from the counter portion of the address generator, described below.

Buffer **22** of FIG. **3** corresponds to the buffer circuitry **56** of FIG. **5**. The outputs of the buffer circuitry of FIG. **5** are designated as a "left" and "right" Y (column address) and the inverses thereof ($Y_{m-L}$, $Y_{mL}$, $Y_{m-R}$ and $Y_{mR}$). (Note there are two decoders, one for the left memory block and the other for the right memory block.) The output of buffer **56** corresponds to one bit of the address out signal of FIG. **3**.

The left and right (L, R) signals of FIG. **5** control the buffer **56** outputs, to provide address signals to left or right decoders respectively. Also provided is column address power up signal YS, which disables the input address pass when the chip is in the precharge state. The internal start address output by the circuit of FIG. **5** (designated $BA_n$) is an input to the associated counter cell, as described below.

FIG. **6** shows the counter (corresponding to the address sequencer **20** of FIG. **3**) providing a nine-bit count. The counter has nine identical cells **60-1**, **60-2**, . . . , **60-9** connected as shown. Each cell has as a first input the internal start address $BA_n$. The second cell input is the carry signal designated $BC_{n-1}$ from the prior cell. Each cell also receives a first timing signal PRESET, and a second timing signal $\phi_{clock}$. The output of each counter cell is an output address bit BN (which is the address out) which then goes to buffer **56** of FIG. **5**, and a second output $BC_n$ which is the carry value to the subsequent cell.

It is to be understood that the counter of FIG. **6** occurs only once in the address sequencer **20** and services all nine address buffer circuits, of which only one is shown in FIG. **5**.

FIG. **7** shows details of one of the cells of FIG. **6**. Signal $BC_{n-1}$ is the carry input signal, while signal $BA_n$ is the external address signal. The timing signals are $\phi_{clock}$ and PRESET (and their inverses). The cell output is the "real" address BN and a carry value $BC_n$ to the next cell. The cell of FIG. **7** includes conventionally a left-hand side which is the "slave" side **70** and a right hand side which is the "master" side **72** (indicated by the broken line). Thus, there are two latches **70***a*, **72***a* one for each side of the counter cell, with one latch at any one time updating its value while the second latch is holding the previously calculated data and transmitting it as output.

FIGS. **8**, **9** and **10** show circuitry for generating the timing signals for the serial address generator. The two externally provided timing signals are RAS and CAS-PAD. These in turn generate as shown the internal timing signals. The sequence is that the input clock signal CAS-PAD generates timing signal $CAS1_b$ which in turn generates signal BAEN- which in turn generates

signal $\phi_{clock}$. The $\phi_{clock}$ signal of FIG. **3** is shown in the timing diagram of FIGS. **11**(*a*), **11**(*b*).

FIG. **8** shows the circuitry which provides the timing signal $CAS1_b$ which is a timing signal for the above-described counter circuitry. Note that signal $CAS1_b$ is in part determined by the signal BM (burst mode) and by the signal WE1 which in this case is the burst write input signal.

FIGS. **11***a* and **11***b* show the timing for the signals of FIGS. **5** to **10**. The start address (designated $A_n$ in FIG. **3**) is designated $Y_N$ in the timing diagram of FIGS. **11***a* and **11***b*. The output signal of the counter is designated $Y_{N+1}$, $Y_{N+2}$, . . . in the timing diagram. It can be seen that when the clock signal AS goes high, and after a particular period, the PRESET signal goes high. In turn, the PRESET signal going low is determined by the signal CAS-PAD going low.

The overall clock speed of the chip in terms of address generation is determined by the signal CAS-PAD; in one embodiment this signal has a 15 nanosecond period, providing a 66 MHz operating speed.

It is to be understood that in a typical operation of the serial address generator, the associated memory array is considered to be an array of memory cells arranged in rows and columns. Each "page" is one row, with the first address on the page being that of the first memory cell in the column. Signal $BE/\overline{OE}$, (burst enable output enable) at the rising edge of AS determines whether one is to be in burst mode or in normal page mode. Signal $BE/\overline{OE}$ is determined by the host computer. The output of buffer **56** of the circuit of FIG. **5** is connected typically to a column predecoder for determining the particular column of a memory array to be addressed. A predecoder buffers the address signals prior to provision thereof to the decoder itself. The predecoder in this case saves power and increases operating speed, by serving as a buffer for the decoder proper.

The above description is illustrative and not limiting; further modifications will be apparent to one skilled in the art and are intended to be covered by the appended claims.

We claim:

**1**. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; and

an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator;

wherein the address sequencer includes means for incrementally timing the address sequencer to generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch.

**2**. The address generator of claim **1**, further comprising:

means for controlling the internal address enable switch; and

means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and

wherein during the duration the external address enable switch is closed, the address sequencer generates the second address in the sequence of addresses.

**3**. The address generator of claim **1**, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed.

**4**. The address generator of claim **1**, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator.

**5**. The address generator of claim **2**, further comprising means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses.

**6**. The address generator of claim **2**, further comprising means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address.

**7**. The address generator of claim **2**, wherein the address sequencer includes a counter having a master portion and a slave portion.

**8**. The address generator of claim **1**, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory.

**9**. An address generator for a random access memory, comprising:

means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address;

an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an output address immediately following the generation of the first address;

an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator;

an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for incrementally timing the address sequencer during a preset period to generate the second address at a same time that the first address is being provided from the external source.

**10**. A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of:

providing from an external source a first address in the sequence as an output address;

switching in the first address as an output address during a preset period;

then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; and

switching in the second address as an output address after the preset period.

**11**. The address generator of claim **2**, wherein the means for controlling the internal address enable switch

is a logical inversion of the signals provided to the clock input terminal.

12. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator;

an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series;

wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch.

13. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator;

an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; and

means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address;

wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch.

14. An address generator for a random access memory, comprising:

an address sequencer having a clock input terminal, a preset terminal, and an output terminal;

an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; and

an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator;

wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch, and

wherein the address sequencer includes a counter having a master portion and a slave portion.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION



PATENT NO. : 5,452,261
DATED : 09/19/95
INVENTOR(S) : Chung, Jinyong; Murray, Michael A.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Replace FIG. 7 with attached FIG. 7.

Signed and Sealed this

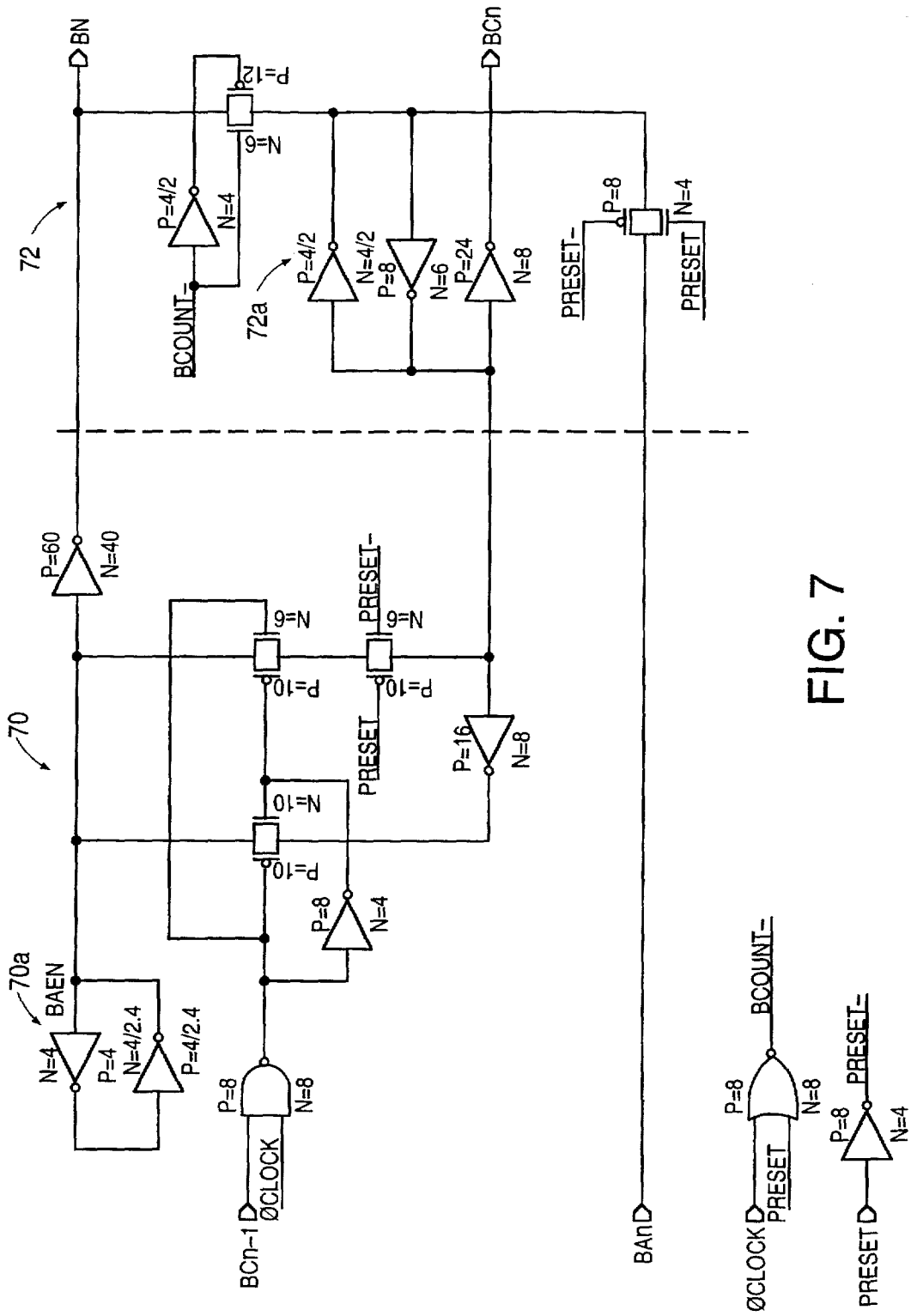
Sixteenth Day of March, 1999

*Attest:*

Q. TODD DICKINSON

*Attesting Officer*

*Acting Commissioner of Patents and Trademarks*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BCn
72
72a
70
70a
BAEN
BCOUNT-
PRESET-
PRESET
ØCLOCK
BCn-1
BAnD
P=12
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P=4/2
N=4
N=4/2
P=8
N=6
P=24
N=8
P=60
N=40
P=10
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FIG. 7

# Exhibit B

US006146997A

# United States Patent [19]

Liu et al.

[11] Patent Number: 6,146,997

[45] Date of Patent: Nov. 14, 2000

[54] **METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE**

[75] Inventors: **Jacson Liu**, Hsinchu Hsien; **Jing-Xian Huang**, Hsinchu, both of Taiwan

[73] Assignee: **Mosel Vitelic, Inc.**, Hsinchu, Taiwan

[21] Appl. No.: **09/407,268**

[22] Filed: **Sep. 29, 1999**

[30] **Foreign Application Priority Data**

May 11, 1999 [TW] Taiwan ..... 88107602

[51] **Int. Cl.**[7] ..... **H01L 21/4763**

[52] **U.S. Cl.** ..... **438/639**; 438/639; 438/253; 438/631; 438/626; 438/634; 257/336; 257/344; 257/346; 357/15; 357/59; 357/67

[58] **Field of Search** ..... 257/336, 344, 257/346; 357/59, 15, 67; 438/253, 631, 626, 634

[56] **References Cited**

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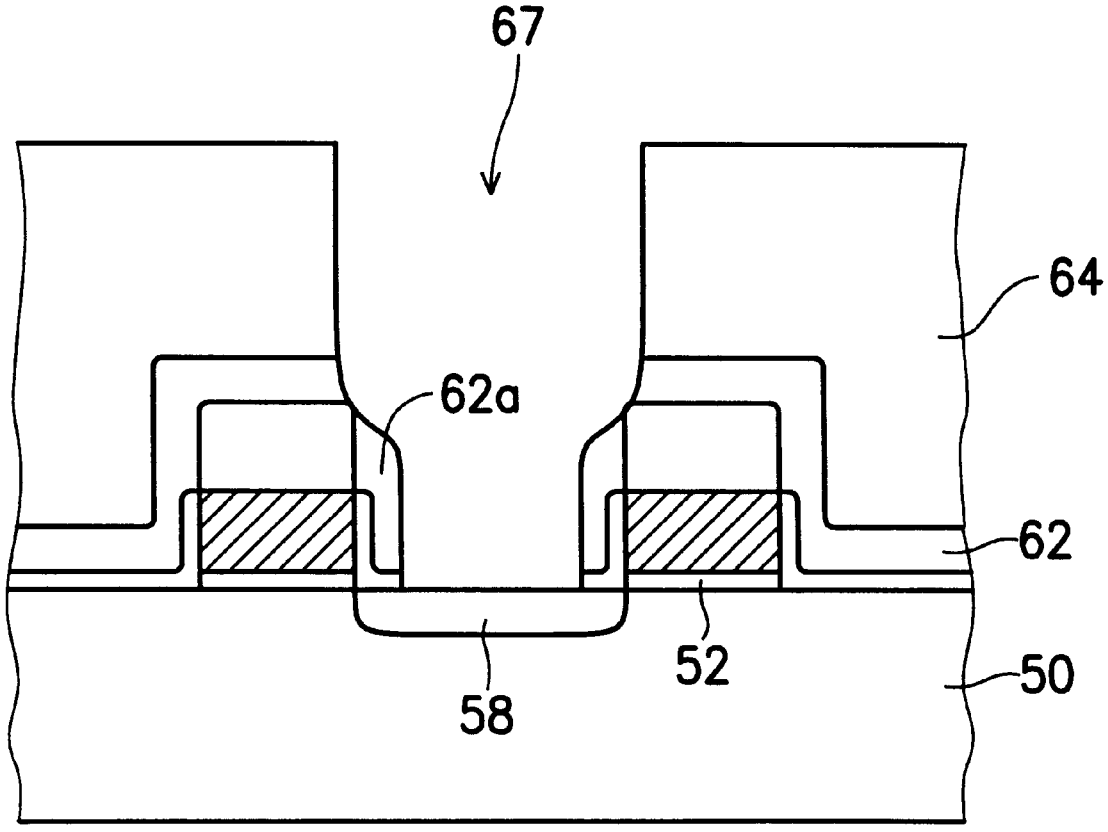
*Primary Examiner*—David Nelms
*Assistant Examiner*—Phuc Dang
*Attorney, Agent, or Firm*—Morrison & Foerster LLP

[57] **ABSTRACT**

A simplified method for forming a self-aligned contact hole is disclosed. The method comprises the steps of (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; (c) forming an insulating layer overlying the barrier layer; (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

**14 Claims, 5 Drawing Sheets**



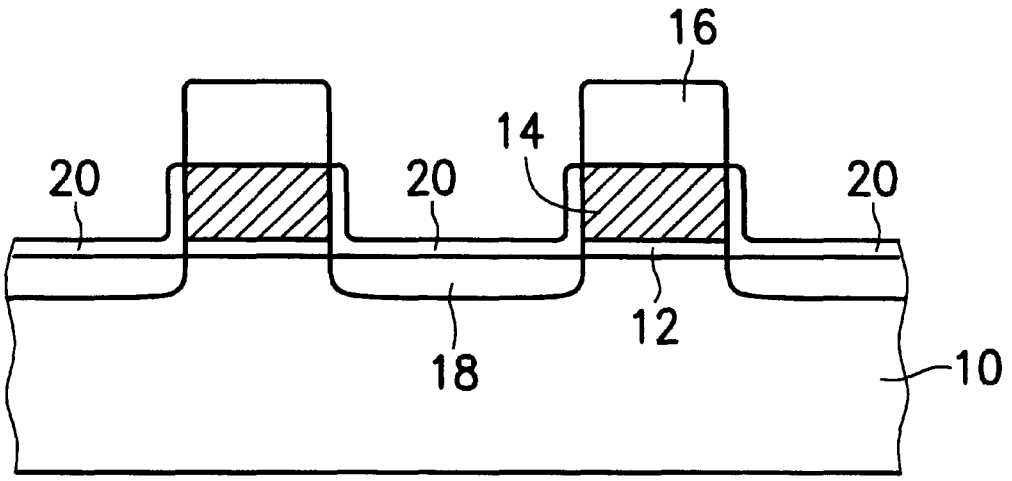



Fig. 1A (Prior Art)

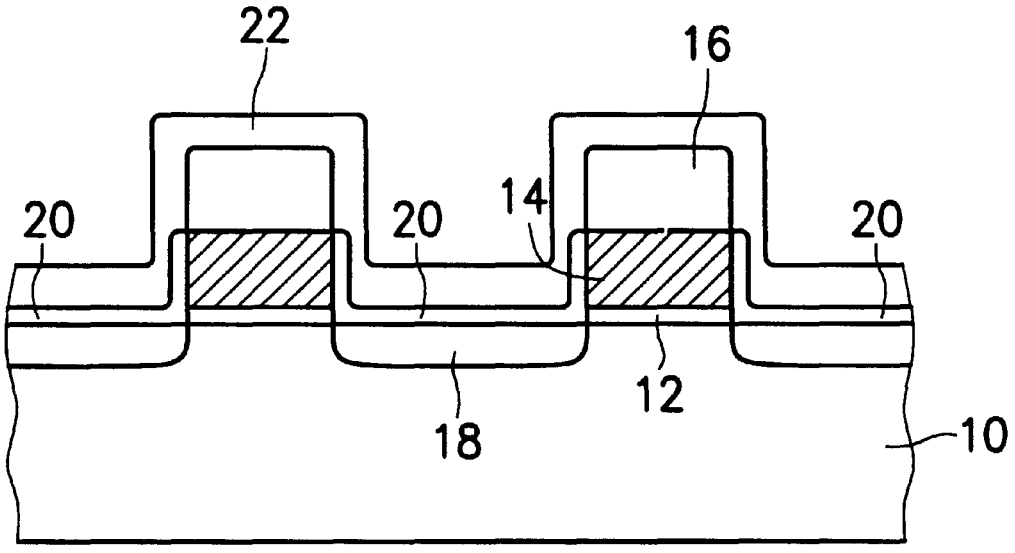



Fig. 1B (Prior Art)

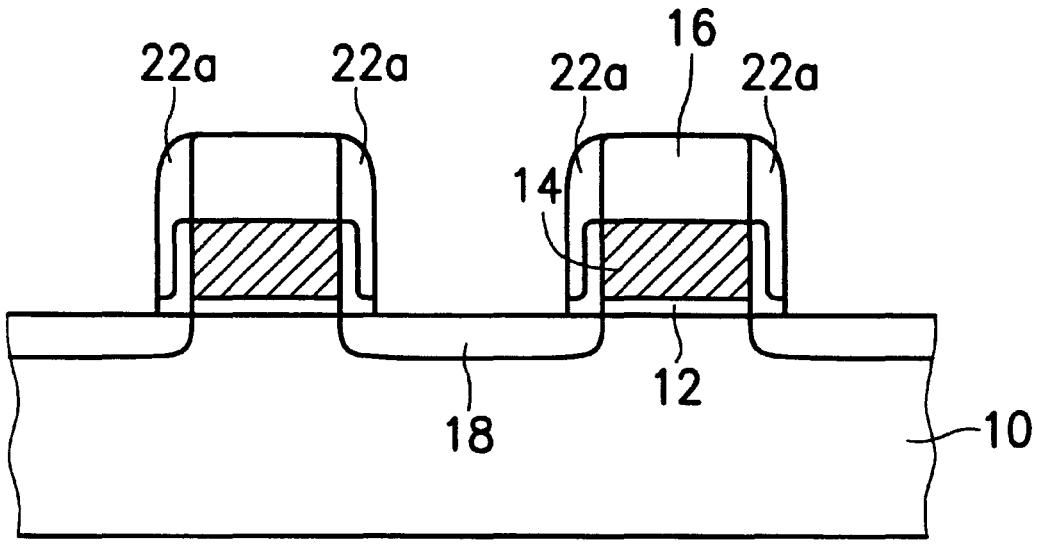



Fig. 1C (Prior Art)

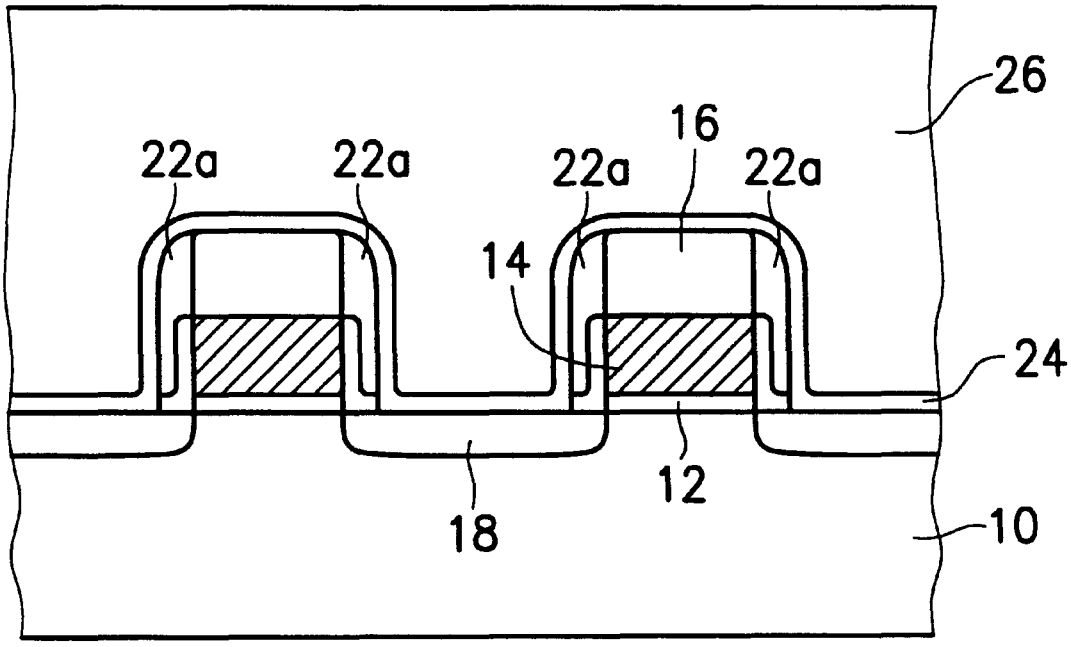



Fig. 1D (Prior Art)

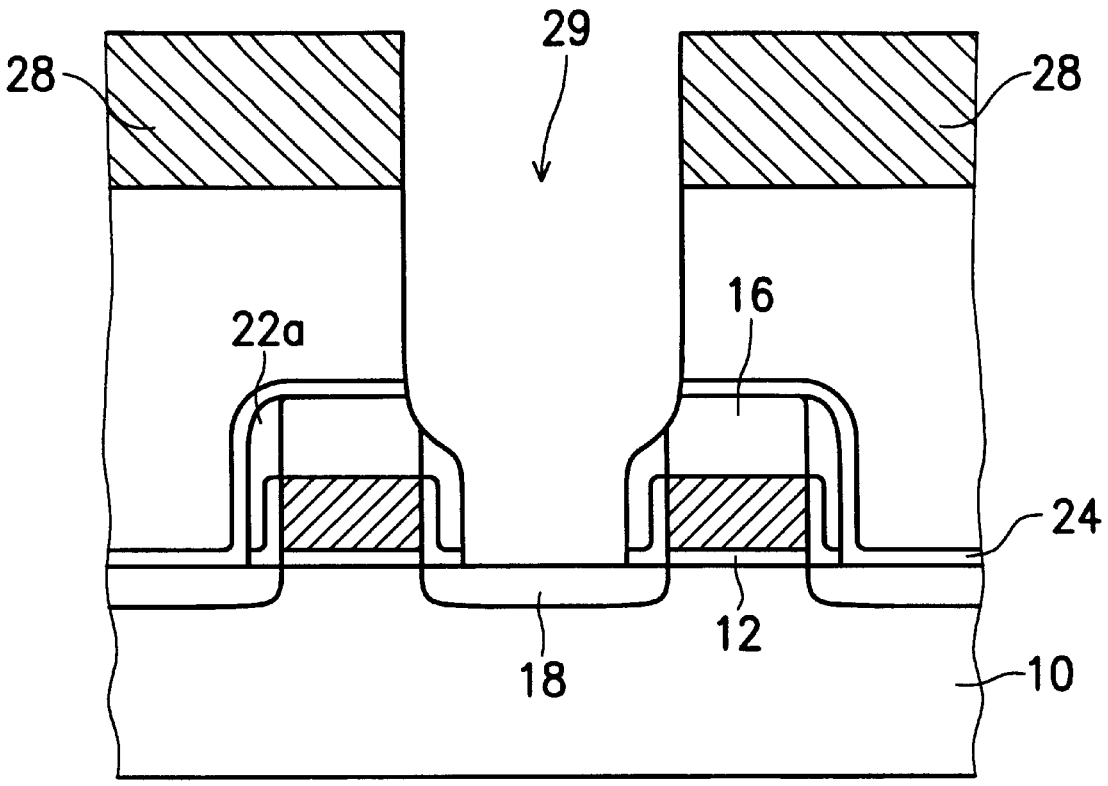



Fig. 1E (Prior Art)

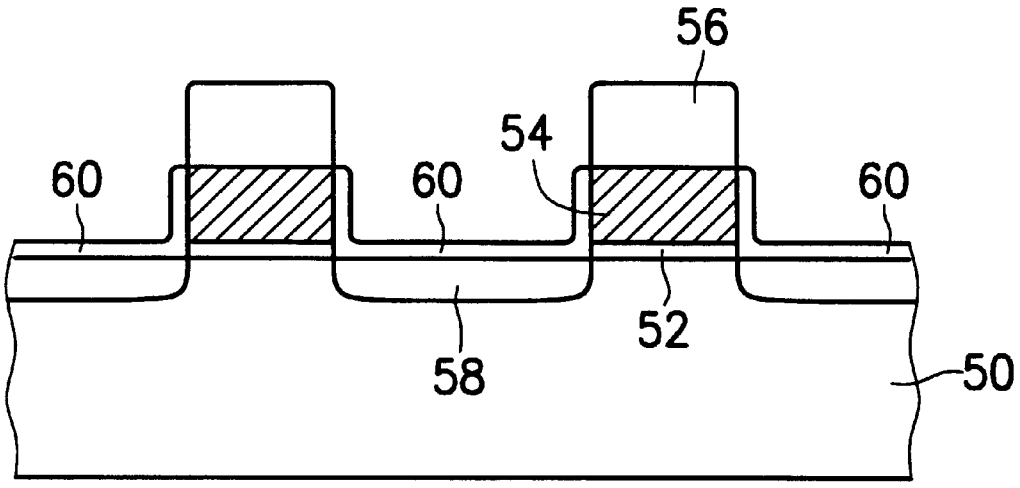



Fig. 2A

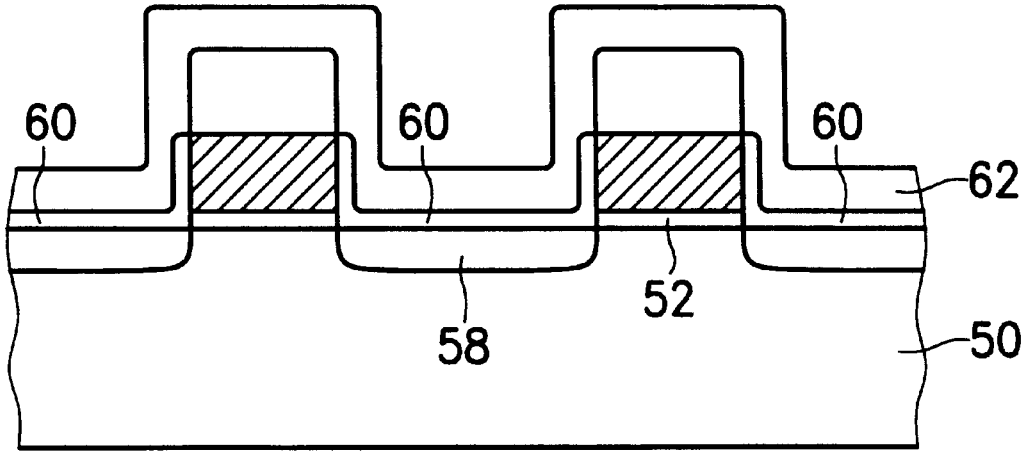



Fig. 2B

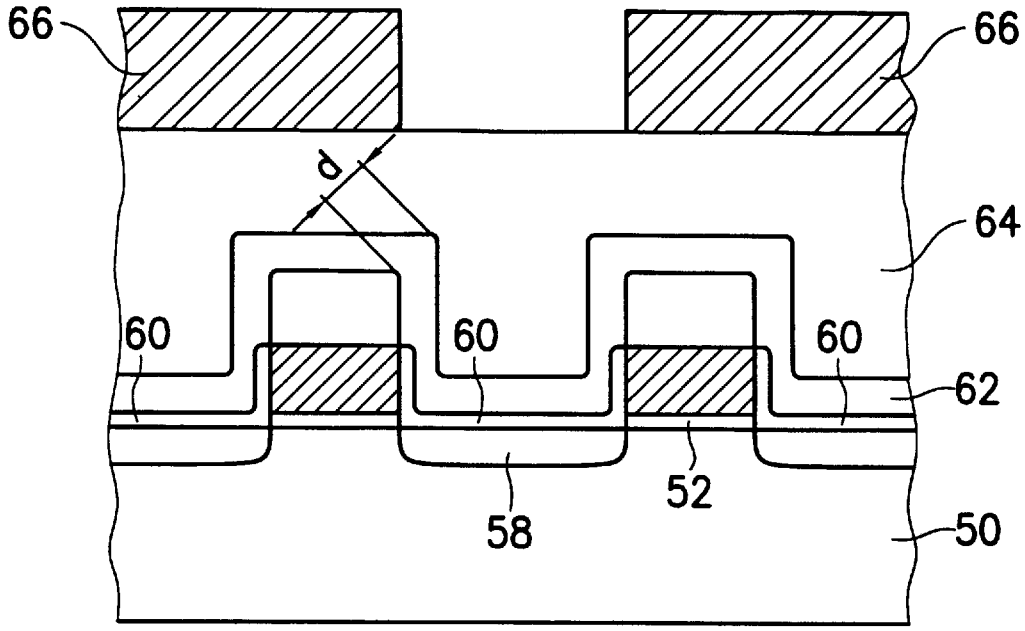



Fig. 2C

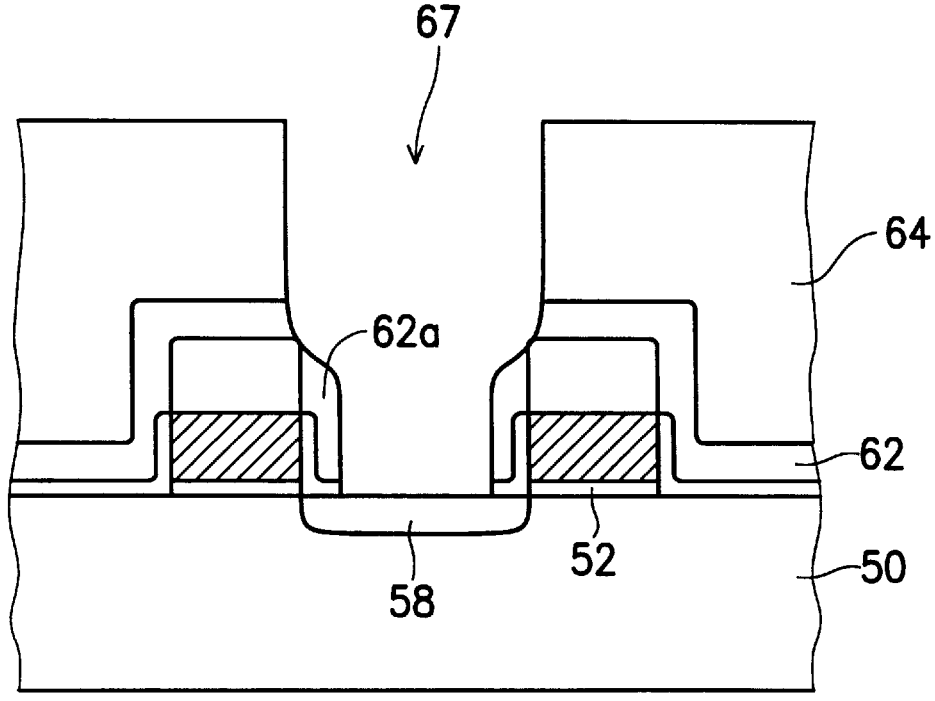



Fig. 2D

# METHOD FOR FORMING SELF-ALIGNED CONTACT HOLE

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to the fabrication of semiconductor devices, and more particularly to a simplified method for forming a self-aligned contact hole.

2. Description of the Related Arts

Self-alignment is a technique in which multiple levels of regions on the wafer are formed using a single mask, thereby eliminating the alignment tolerance required by additional masks. This powerful approach is being used more often as circuit sizes decrease. Self-aligned contacts are often used in memory cells where contacts are limited only by the spacers and field oxide bird's beak or a contact window landing pad. Therefore, the mask contact window can be oversized relative to the contact area underneath, and no contact borders are needed, resulting in significant space saving. Referring to FIGS. **1**A–**1**E, a conventional process of forming a self-aligned contact hole is illustrated in cross-sectional views. The process will be described as follows.

FIG. **1**A shows a semiconductor substrate **10** having two closely spaced field effect transistors with gate electrodes **14**, source/drain diffusion regions **18**, and gate oxides **12**. The gate electrodes **14**, commonly consisting of polysilicon and silicide, are capped with an insulator **16** of silicon nitride. Next, a thin oxide layer **20** is formed over the substrate surface and on the sidewalls of the gate electrode **14** by rapid thermal oxidation at about 800 to 1100° C.

Referring to FIG. **1**B, a conformal layer of silicon nitride **22** having a thickness of about 100 to 600 Å is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer **22** is anisotropically etched to form nitride spacers **22***a* on the sidewalls of the gate electrodes **22** and the cap layers **16**, as shown in FIG. **1**C. Then, the thin oxide layer on the substrate surface is removed by HF solution to expose the diffusion region **18**.

Referring to FIG. **1**D, a conformal layer of etch barrier material **24** is deposited over the diffusion region **18**, the cap layers **16**, and the sidewall spacers **22***a*. The barrier layer is typically a silicon nitride layer having a thickness of about 100 to 500 Å. A layer of insulator **26** is deposited over the substrate as inter-layer dielectric (ILD) and is preferably planarized. The insulating layer **26** may consist of one or more dielectric depositions of spin on glass (SOG), silicon oxide, borophosphosilicate (BPSG), and so on.

Referring to FIG. **1**E, using a photoresist mask **28**, a contact hole **29** is etched in the insulating layer **26** with the barrier layer **24** serving as an etch stop, which is finally removed to expose the diffusion region **18**. The etching of the insulating layer **26** is selective to the capping layers **16** and sidewall spacers **22***a* encapsulating the gate electrodes **14** so that the contact hole is self-aligning in nature.

The fabricating method described above, however, requires complicated processes. For example, two depositions of silicon nitride are required for forming the conformal layer **22** and the barrier layer **24**, respectively. Besides, the two layers are to be etched individually. The conformal nitride layer **22** is etched to form nitride spacers **22***a*, and the barrier layer **24** is etched to reveal the underlying diffusion region **18** after the contact hole etching. Thus, improvements are needed to eliminate process steps so as to reduce the manufacturing cost and to increase the throughput.



## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a simplified method for forming a self-aligned contact hole.

To accomplish the above objective, the present invention provides a method for forming a self-aligned contact hole. In this method, the conformal layer used for forming sidewall spacers of gate electrodes will not be etched until a contact opening is formed, such that the conformal layer can serve as an etch barrier that protects the diffusion region during the contact hole etching. Thus, there is no need for depositing another etch barrier layer. Furthermore, the etching for sidewall spacers can be thus incorporated into the contact hole etching, thereby eliminating process steps.

The present method for forming a self-aligned contact includes the steps of: (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; (c) forming an insulating layer overlying the barrier layer; (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

Other objects, features, and advantages of the present invention will become apparent from the following detailed description which makes reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A through **1**E are cross-sectional views illustrating the steps of a conventional method for fabricating a self-aligned contact hole; and

FIGS. **2**A through **2**D are cross-sectional views illustrating the steps for fabricating a self-aligned contact hole according to a preferred embodiment of the invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now in keeping with the objective of this invention, the method for fabricating a self-aligned contact hole is described in detail.

Referring to FIG. **2**A, two closely spaced field effect transistors with gate electrodes **54**, source/drain diffusion regions **58**, and gate oxides **52** are defined in a semiconductor substrate **50** using known processes. The gate electrodes **54**, preferably consisting of polysilicon and tungsten silicide, are capped with an insulator **56** of silicon nitride. The process details for forming such field effect transistors are well known and will not be described here. Next, a thin oxide layer **60** having a thickness of about 150 Å is formed over the substrate surface and on the sidewalls of the gate electrode **54** by rapid thermal oxidation at about 800 to 1100° C.

Referring to FIG. **2**B, a conformal layer of silicon nitride **62** is deposited over the substrate surface using low pressure chemical vapor deposition (LPCVD). The conformal silicon nitride layer **62**, as described earlier, acts as sidewall spacers of gate electrode **54** as well as an etch stop at contact hole etching. The conformal layer **62** preferably has a thickness of about 100 to 500 Å, and more preferably has a thickness of about 200 to 350 Å.

Referring to FIG. **2**C, a layer of insulator **64** is deposited over the substrate as inter-layer dielectric (ILD) and is preferably planarized. The insulating layer **64** may consist of one or more dielectric depositions of spin on glass (SOG), silicon oxide, borophosphosilicate (BPSG), and the like. It should be particularly noted that the process steps of anisotropically etching for sidewall spacers and depositing a barrier layer necessary in the conventional method are omitted here.

Referring to FIG. **2**D, using a photoresist mask **66**, a contact hole **67** is etched in the insulating layer **64** in a self-aligned manner. During this etch, the conformal nitride layer **62** serves as an etch barrier to protect the diffusion region **58** from being attacked by etching. Moreover, as depicted in FIG. **2**C, it provides extra thickness d to protect the gate electrode **54** when compared to that of the conventional method (see FIG. **1**C for reference). Next, the conformal nitride layer **62** underneath the opening is anisotropically etched to remove the portion over the diffusion region **58**. Simultaneously with this etch, nitride spacers **62***a* are formed on sidewalls of the gate electrode **54**. After removing the photoresist **66**, the thin oxide layer **60** is removed by HF solution to expose the diffusion region **58**, thereby completing the contact hole.

Thereafter, a conductive plug can be formed in the contact hole **67** to electrically connect to the diffusion region **58**. The conductive plug is preferably chosen from polysilicon, tungsten, molybdenum, aluminum alloys, copper alloys, and the like. It can be formed by overfilling the contact hole and removing the conductive material outside of the contact hole by etch back or chemical mechanical polishing.

According to a feature of the present invention, because the conformal nitride layer **62** is not etched until the contact opening is formed, it provides extra thickness d to protect the gate electrode **54** at the contact hole etching. Further, the same nitride layer is anisotropically etched to form sidewall spacers that prevent shorting between the gate electrode and the conductive plug.

The simplified method of the invention overall reduces one etch step and one deposition step as compared to the conventional method illustrated by FIGS. **1**A through **1**E. Accordingly, the manufacturing cost is reduced and the throughput is increased. Further, since the method of the present invention provides a better etch barrier at the contact hole etching, it is advantageous in process tolerance and reliability.

While the invention has been particularly shown and described with the reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

**1**. A method for forming a self-aligned contact hole, comprising the steps of:

(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon;

(b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;

(c) forming an insulating layer overlying the barrier layer;

(d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and



(e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode.

**2**. The method as claimed in claim **1**, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer.

**3**. The method as claimed in claim **1**, wherein said gate electrode comprises a capping layer of silicon nitride.

**4**. The method as claimed in claim **1**, wherein said barrier layer is a silicon nitride layer.

**5**. The method as claimed in claim **4**, wherein said barrier layer has a thickness between about 100 to 500 Å.

**6**. The method as claimed in claim **1**, wherein said insulating layer comprises a layer of borophosphosilicate glass.

**7**. The method as claimed in claim **1**, wherein step (c) comprises:

depositing an insulating layer overlying the barrier layer; and

planarizing the insulating layer.

**8**. The method as claimed in claim **1**, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region.

**9**. A method for forming a self-aligned contact hole, comprising the steps of:

(a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer;

(b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation;

(c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode;

(d) forming an insulating layer overlying the conformal layer of silicon nitride;

(e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop; and

(e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode.

**10**. The method as claimed in claim **9**, wherein said capping layer is a silicon nitride layer.

**11**. The method as claimed in claim **9**, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å.

**12**. The method as claimed in claim **9**, wherein said insulating layer comprises a layer of borophosphosilicate glass.

**13**. The method as claimed in claim **9**, wherein step (d) comprises:

depositing an insulating layer overlying the conformal layer of silicon nitride; and

planarizing the insulating layer.

**14**. The method as claimed in claim **9**, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region.

* * * * *

[redacted]

# EXHIBIT C

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer includes means for incrementally timing the address sequencer to generate a second | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 2** | |
| The address generator of claim 1, further comprising: | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for controlling the internal address enable switch; | [redacted] |
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| enable switch is closed, the address sequencer generates the second address in the sequence of addresses. | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 4** | |
| The address generator of claim 1, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |
| **Claim 5** | |
| The address generator of claim 2, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| further comprising means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | [redacted] |
| **Claim 6** | |
| The address generator of claim 2, further comprising means for providing clock signals | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address. | [redacted] |
| **Claim 7** | |
| The address generator of claim 2, wherein the address sequencer includes a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| counter having a master portion and a slave portion. | |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | [redacted] |
|---|---|
| **Claim 9** | |
| An address generator for a random access memory, comprising: | [redacted] |
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| provided as an out-put address immediately following the generation of the first address; | [redacted] |
| an internal address enable switch connected between an output terminal of the address sequencer and an output | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| means for incrementally timing the address sequencer during a preset period to generate the second address at a same time that | [redacted] |

[redacted]



| | | |
|---|---|---|
| the first address is being provided from the external source. | [redacted] | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 10** | |
| A method of generating a sequence of addresses for | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |
| switching in the first address as an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| output address during a preset period; | [redacted] |
| then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |
| switching in | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the second address as an output address after the preset period. | [redacted] |
| **Claim 12** | |
| An address generator for a random access memory, comprising: | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |
| an internal address enable switch connected between the output terminal of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the duration of the first address, the preset signal setting the address sequencer to the second address in the series; | |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 13** | |
| An address generator for a random access memory, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |
| an internal address enable switch connected between the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| only after the duration of the first address; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

| | |
|---|---|
| while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 14** | |
| An address generator for a random access memory, comprising: | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |
| an internal address enable switch connected | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

| | | |
|---|---|---|
| being supplied to the output terminal of the address generator by the external address enable switch, | [redacted] | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| wherein the address sequencer includes a counter having a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| master portion and a slave portion. | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| wherein the address sequencer includes means for incrementally timing the address sequencer to generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

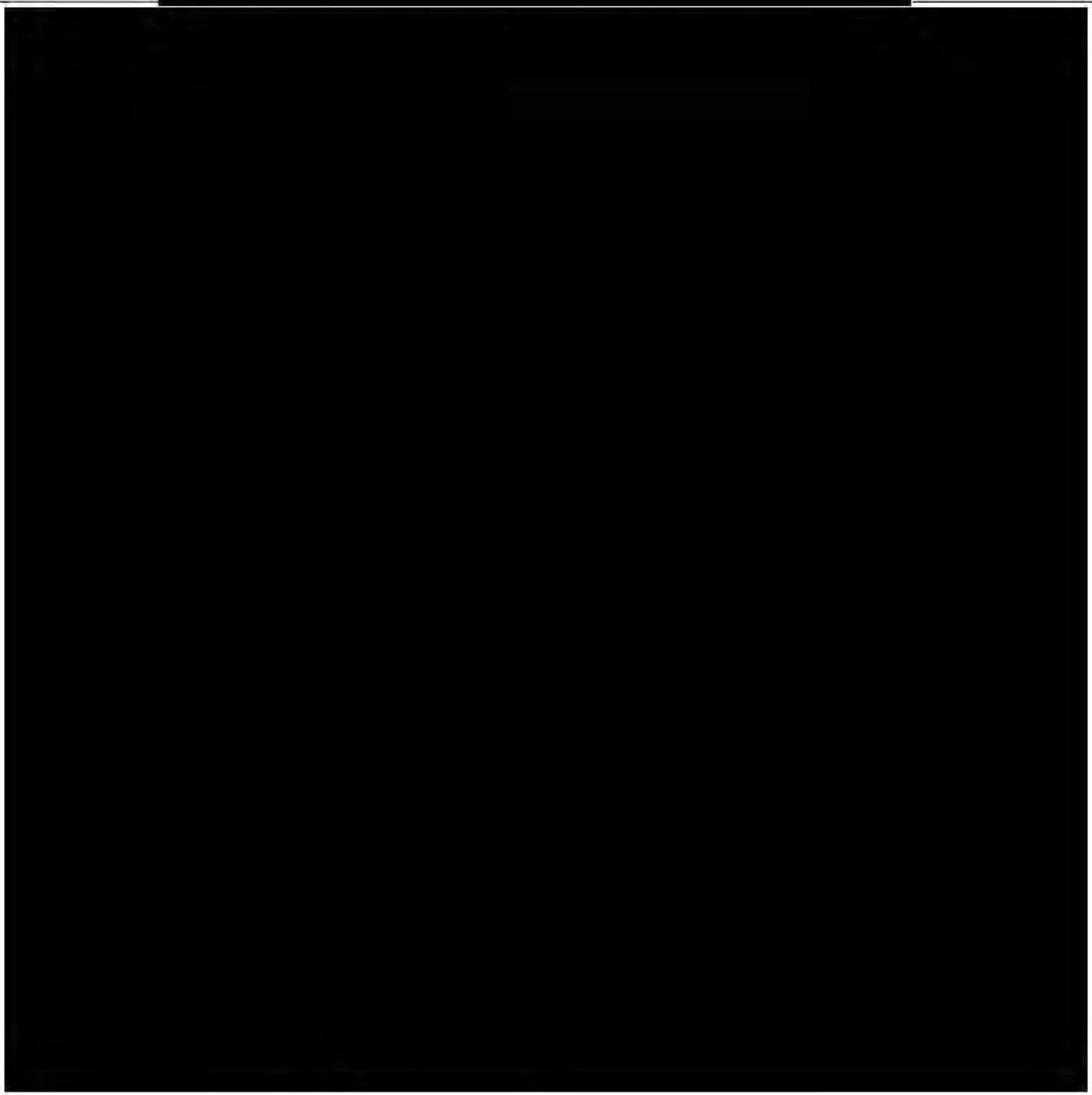
[redacted]

| Claim 2 | |
|---|---|
| The address generator of claim 1, further comprising: | |
| means for controlling the internal address enable switch; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]



[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address enable switch is closed, the address sequencer generates the second address in the sequence of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| addresses. | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 4 | |
|---|---|
| The address generator of claim 1, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| **Claim 5** | |
| The address generator of claim 2, further comprising means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | [redacted] |
| **Claim 6** | |
| The address generator of claim 2, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| further comprising means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| **Claim 7** | |
|---|---|
| The address generator of claim 2, wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| access memory. | [redacted] |
| **Claim 9** | |
| An address generator for | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| a random access memory, comprising: | [redacted] |
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

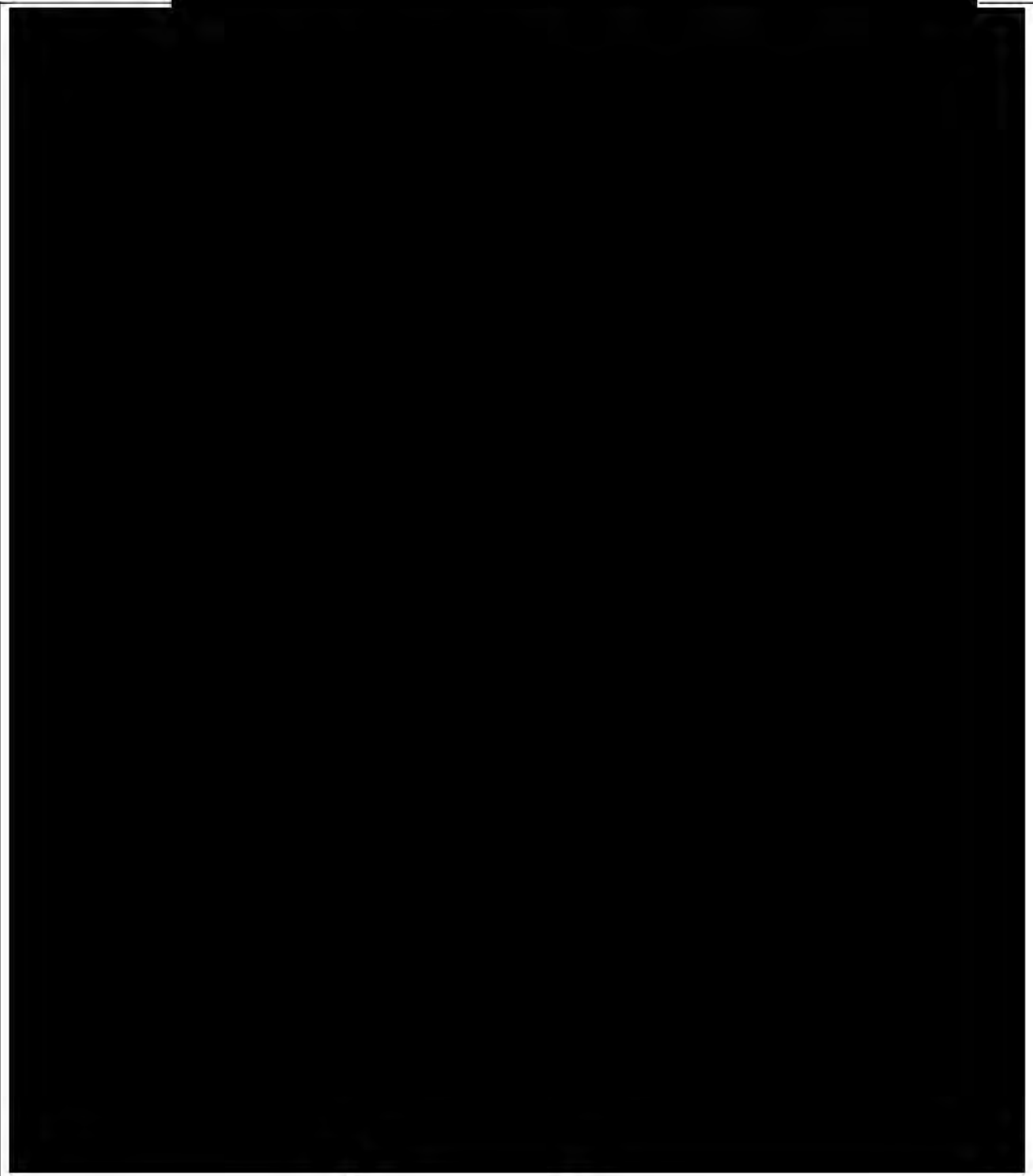
[redacted]

| | |
|---|---|
| an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an out-put address immediately following the generation of the first address; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]



[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for incrementally timing the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequencer during a preset period to generate the second address at a same time that the first address is being provided from the external source. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| **Claim 10** | |
| A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| switching in the first address as an output address during a preset period; | [redacted] |
| then, providing | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

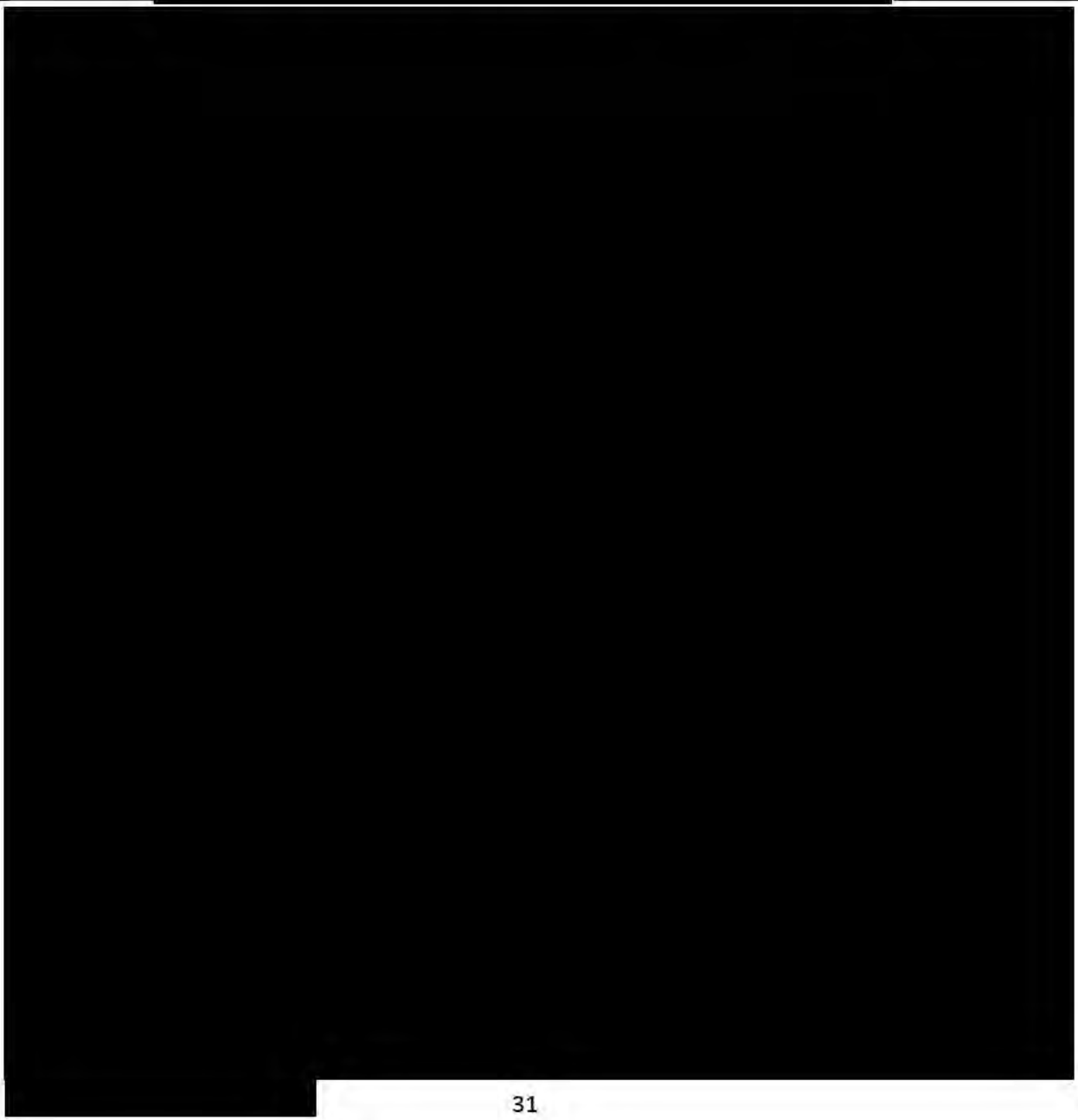
[redacted]

| | |
|---|---|
| from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]





[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

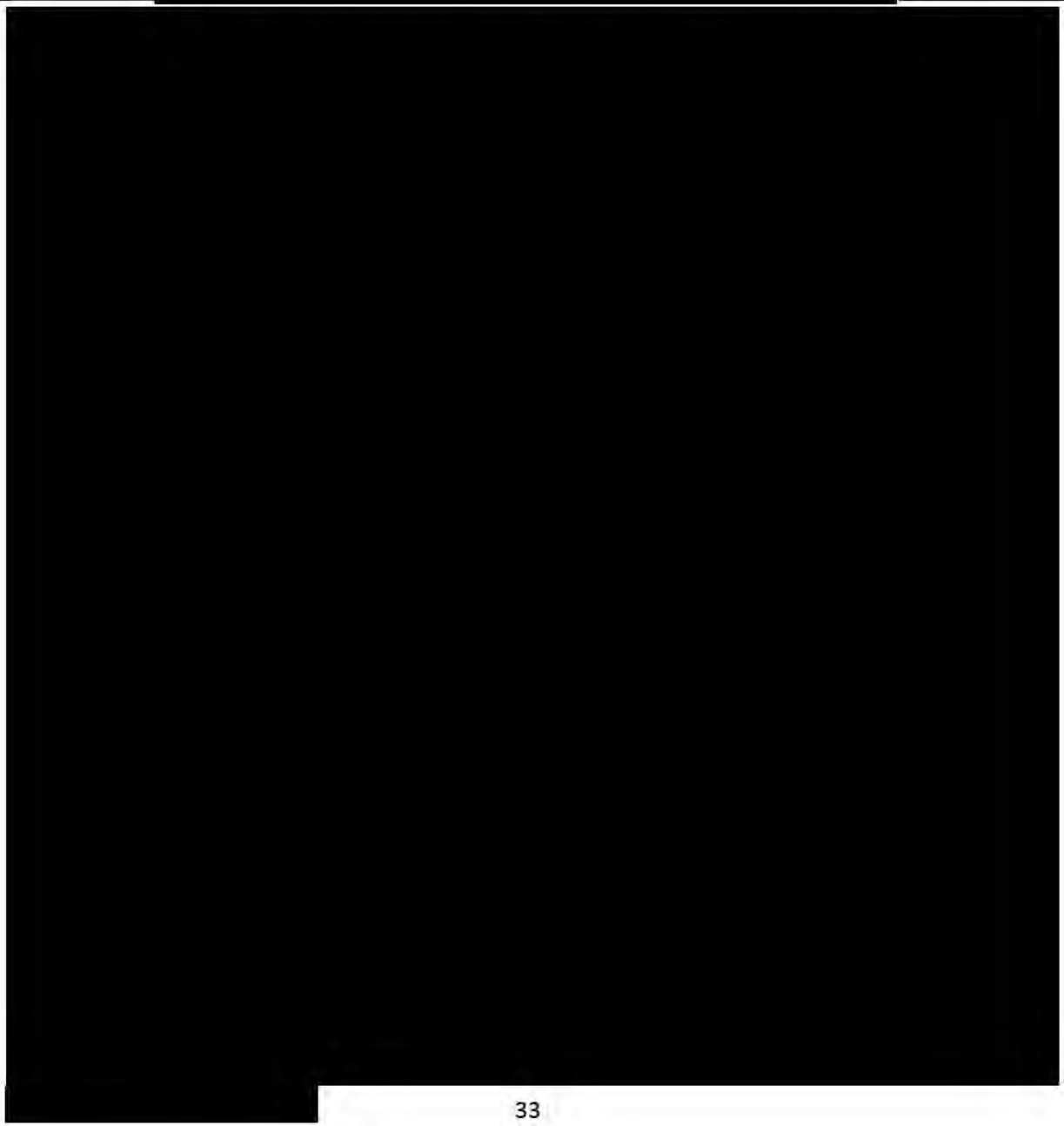
[redacted]

| | |
|---|---|
| switching in the second address as an output address after the preset period. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]





[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 12 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing a preset signal of a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 13 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing clock signals of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

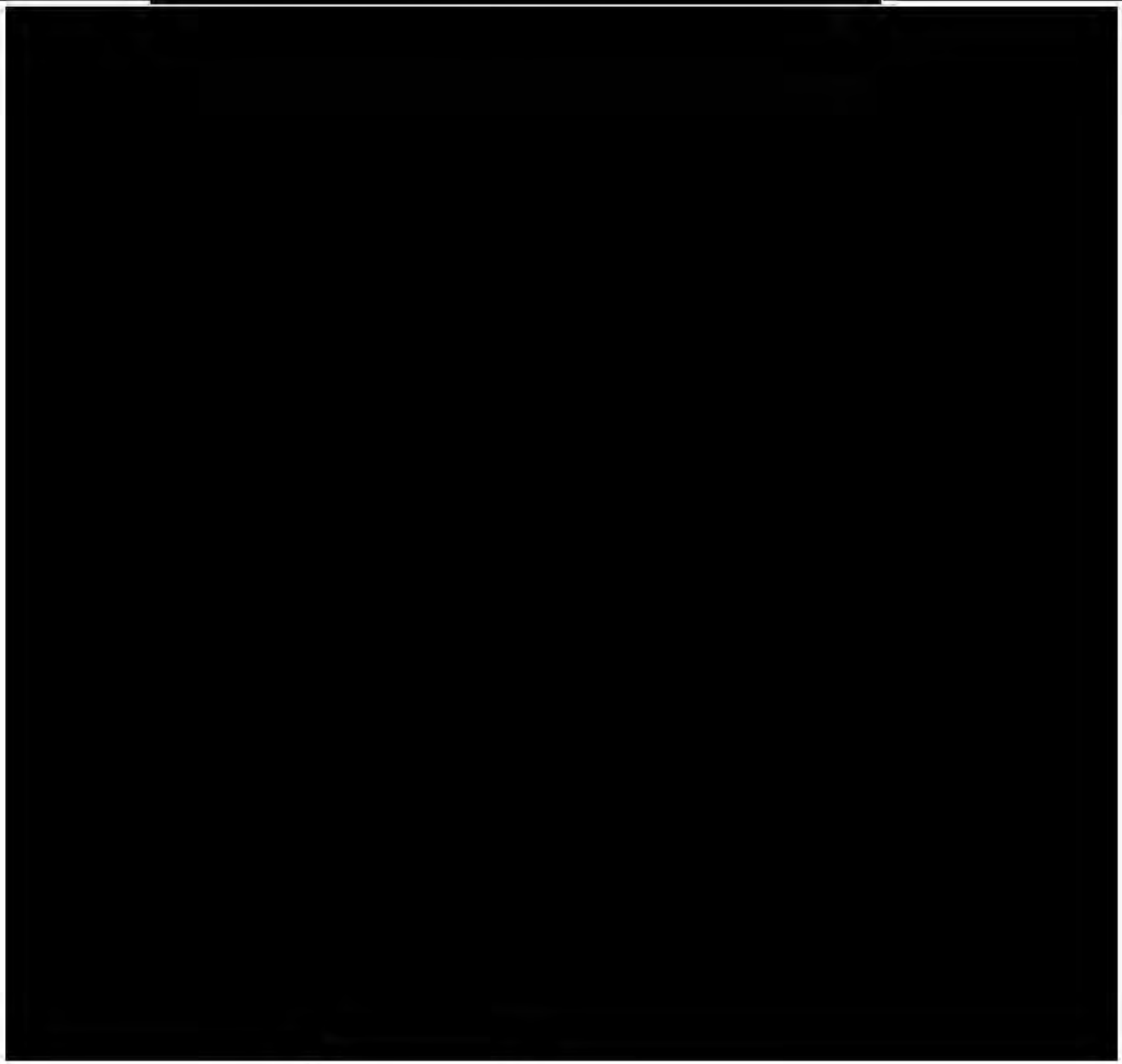
[redacted]

| Claim 14 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]



[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an external address enable switch connected between an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer includes means for incrementally timing the address sequencer to generate a second address in a sequence of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 2** | |
| The address | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator of claim 1, further comprising: | |
| means for controlling the internal address enable switch; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address enable switch is closed, the address sequencer | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generates the second address in the sequence of addresses. | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | [redacted] |
|---|---|
| **Claim 4** | |
| The address generator of claim 1, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |
| **Claim 5** | |
| The address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| generator of claim 2, further comprising means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | [redacted] |
| **Claim 6** | |
| The address generator of claim 2, further comprising means for | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| **Claim 7** | |
|---|---|
| The address generator of claim 2, wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| access memory. | [redacted] |
| **Claim 9** | |
| An address generator for a random access memory, comprising: | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |
| an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| out-put address immediately following the generation of the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for incrementally timing the address sequencer during a preset period to generate | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| the second address at a same time that the first address is being provided from the external source. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| **Claim 10** | |
| A method of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generating a sequence of addresses for addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |
| switching in the first address as an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| output address during a preset period; | [redacted] |
| then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| switching in the second address as an output address after the preset period. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

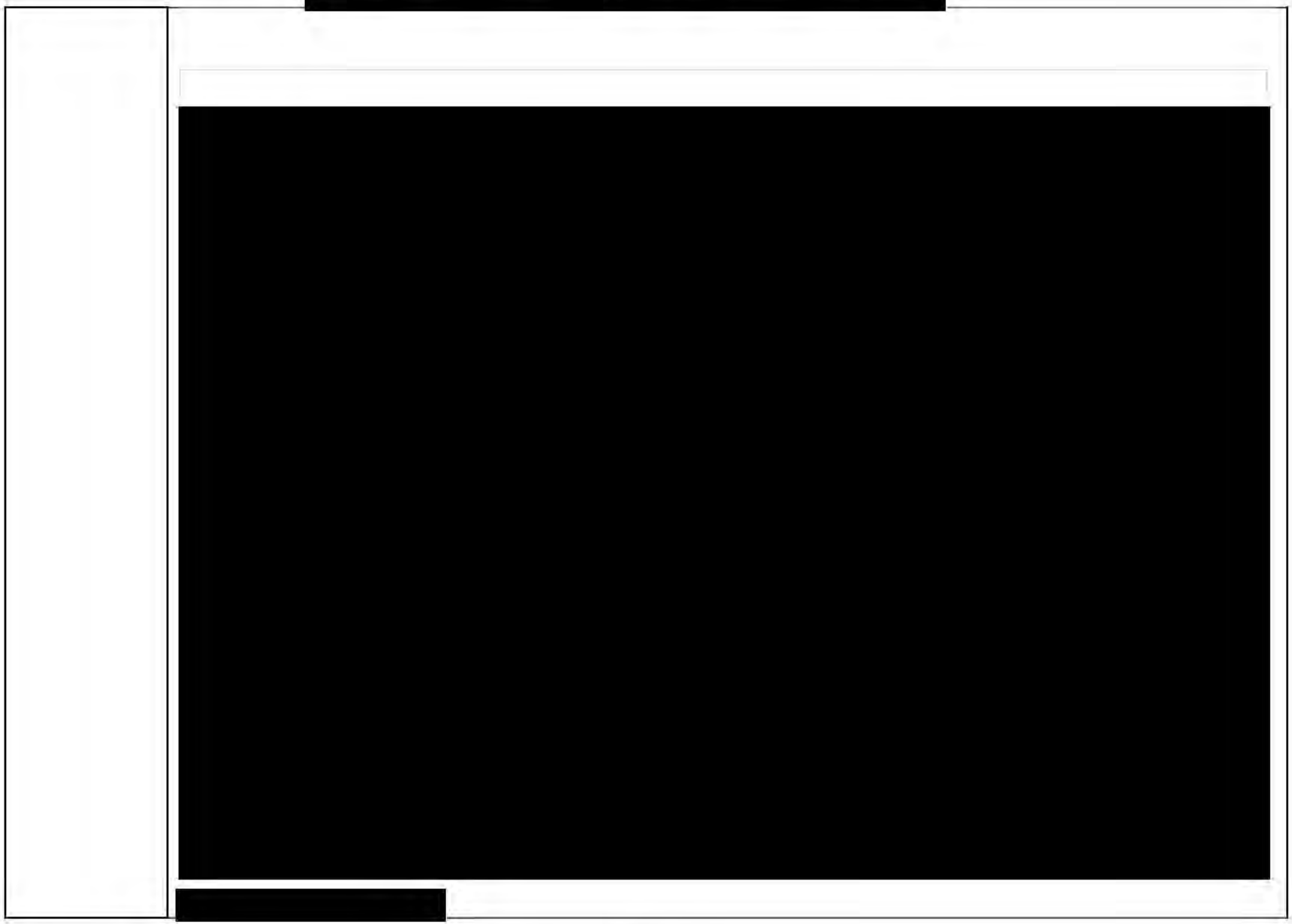
[redacted]

| | |
|---|---|
| **Claim 12** | |
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]



[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an external address enable switch connected between an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address, the preset signal setting the address sequencer to the second address in the series; | |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| **Claim 13** | |
| An address generator for | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

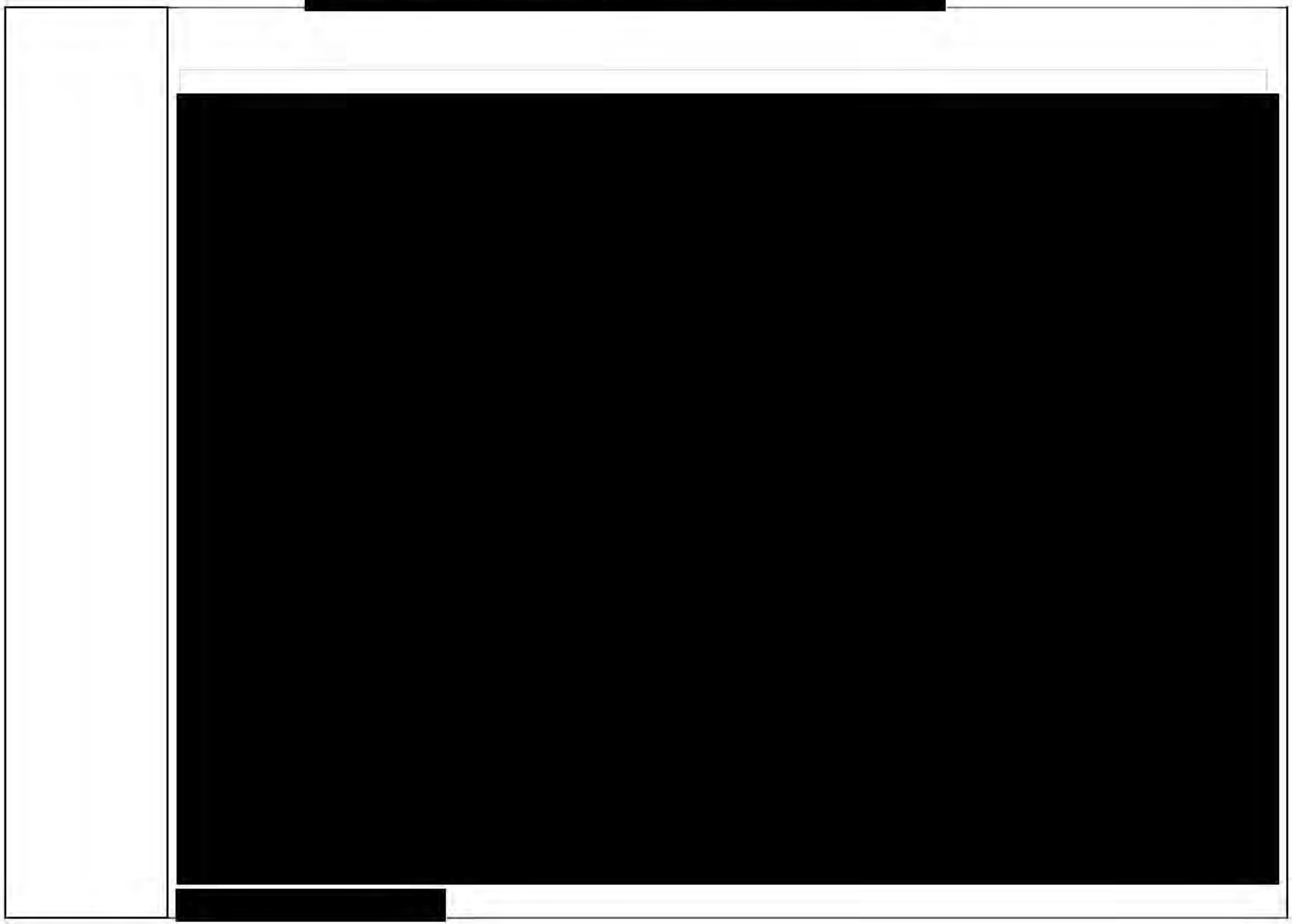
[redacted]

| | |
|---|---|
| a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]



[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an external address enable switch connected between an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring only after the duration of | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| **Claim 14** | |
| An address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an external address enable switch connected between an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the output terminal of the address generator by the external address enable switch, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| wherein the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequencer includes a counter having a master portion and a slave portion. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| wherein the address sequencer includes means for incrementally timing the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address sequencer to generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | [redacted] |
|---|---|
| **Claim 2** | |
| The address generator of claim 1, further comprising: | |
| means for controlling the internal address enable switch; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address enable switch is closed, the address sequencer generates the second address in the sequence of | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

| | |
|---|---|
| addresses. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |
| **Claim 4** | |
| The address generator of claim 1, further | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |
| **Claim 5** | |
| The address generator of claim 2, further comprising means for providing a preset signal of a predetermined duration and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | |
| **Claim 6** | |
| The address generator of claim 2, further comprising means for providing clock signals of predetermined level to the clock input terminal, a first of the clock signals occurring | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| only after the duration of the first address. | |
| **Claim 7** | |
| The address generator of claim 2, wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address is a first address of a page of the random access memory. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 9** | |
| An address generator for a random access memory, comprising: | [redacted] |
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an out-put address immediately following the generation of the first address; | [redacted] |
| an internal address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for incrementally timing the address sequencer during a preset period | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| to generate the second address at a same time that the first address is being provided from the external source. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | [redacted] |
|---|---|
| **Claim 10** | |
| A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| switching in the first address as an output address during a preset period; | [redacted] |
| then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| switching in the second address as an output address after the preset period. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 12** | |
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| means for providing a preset signal of a predetermined duration and level to the | [redacted] |

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**HOME SEMICONDUCTOR CLAIM CHART**
**EXHIBIT 23 - PATENT NO. 5,452,261 - ALL LPDDR2 DRAM**

| | |
|---|---|
| preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| **Claim 13** | |
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing clock signals of predetermined level to the clock input | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| terminal, a first of the clock signals occurring only after the duration of the first address; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 14** | |
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between the output terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| wherein the address sequencer generates a second address in a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch, | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| an internal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer includes means for incrementally timing the address sequencer to | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 2 | |
|---|---|
| The address generator of claim 1, further comprising: | |
| means for controlling the internal address enable switch; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address enable switch is closed, the address sequencer generates the second address in the | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| sequence of addresses. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| **Claim 4** | |
|---|---|
| The address generator of claim 1, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |
| **Claim 5** | |
| The address generator of claim 2, further comprising means for providing a preset signal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | [redacted] |
| **Claim 6** | |
| The address generator of claim 2, further comprising means for providing clock signals of predetermined level to the clock input terminal, a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| first of the clock signals occurring only after the duration of the first address. | |
| **Claim 7** | |
| The address generator of claim 2, wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the externally generated address is a first address of a page of the random access memory. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 9** | |
| An address generator for a random access memory, comprising: | [redacted] |
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an address sequencer for generating the subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an out-put address immediately following the generation of the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for incrementally timing the address sequencer during a preset period to generate the second ad- | [redacted] |

[redacted]



[redacted]

| | |
|---|---|
| dress at a same time that the first address is being provided from the external source. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | [redacted] |
|---|---|
| **Claim 10** | |
| A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| switching in the first address as an output address during a preset period; | [redacted] |
| then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| switching in | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| the second address as an output address after the preset period. | [redacted] |
| **Claim 12** | |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| | [redacted] |
| an internal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator and the output terminal of the address generator; | [redacted] |
| means for providing a preset signal of a predetermined duration and level to the preset terminal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 13 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator and the output terminal of the address generator; | [redacted] |
| means for providing clock signals of predetermined level to the clock input terminal, a first of the | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| clock signals occurring only after the duration of the first address; | |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 14 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch connected between an address input terminal of the address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| while a first address is being supplied to the output terminal of the address generator by the external address enable switch, | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 1 | [redacted] |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer includes means for incrementally | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| timing the address sequencer to generate a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 2 | |
|---|---|
| The address generator of claim 1, further comprising: | |
| means for controlling the internal address enable switch; | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| means for controlling the external address enable switch, wherein the means for controlling the external address enable switch closes the external address enable switch for a duration of the first address of the sequence of addresses, and wherein during the duration the external address enable switch is closed, the address sequencer generates the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| second address in the sequence of addresses. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |
| **Claim 3** | |
| The address generator of claim 1, wherein the second address is output to the output terminal of the address sequencer only when the internal address enable switch is closed. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | [redacted] |
|---|---|
| **Claim 4** | |
| The address generator of claim 1, further comprising a buffer serially connected between the output terminal of the address sequencer and the output terminal of the address generator. | [redacted] |
| **Claim 5** | |
| The address generator of claim 2, further comprising | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the sequence of addresses. | [redacted] |
| **Claim 6** | |
| The address generator of claim 2, further comprising means for providing clock signals of predetermined | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| level to the clock input terminal, a first of the clock signals occurring only after the duration of the first address. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| **Claim 7** | |
|---|---|
| The address generator of claim 2, wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |
| **Claim 8** | |
| The address generator of claim 1, further comprising means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| access memory. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| **Claim 9** | |
| An address generator for a random access memory, comprising: | [redacted] |
| means for providing a first address in a sequence of addresses, the first address being provided from an external source as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an address sequencer for generating the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| subsequent addresses in the sequence of addresses, a second address in the sequence being provided as an out-put address immediately following the generation of the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| an internal address enable switch connected between an output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an external address enable switch connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for incrementally | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| timing the address sequencer during a preset period to generate the second address at a same time that the first address is being provided from the external source. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 10 | |
|---|---|
| A method of generating a sequence of addresses for addressing a random access memory, comprising the steps of: | [redacted] |
| providing from an external source a first address in the sequence as an output address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| switching in the first address as an output address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| during a preset period; | [redacted] |
| then, providing from an address sequencer a second address in the sequence as an output address, the second address being generated by incremental timing during at least a part of a duration of the step of providing the first address; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| switching in the second address as an output address after the preset period. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| | [redacted] |
| **Claim 12** | |
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing a preset signal of a predetermined duration and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series; | [redacted] |
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| enable switch. | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 13 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| means for providing clock signals of predetermined level to the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| clock input terminal, a first of the clock signals occurring only after the duration of the first address; | [redacted] |

[redacted]

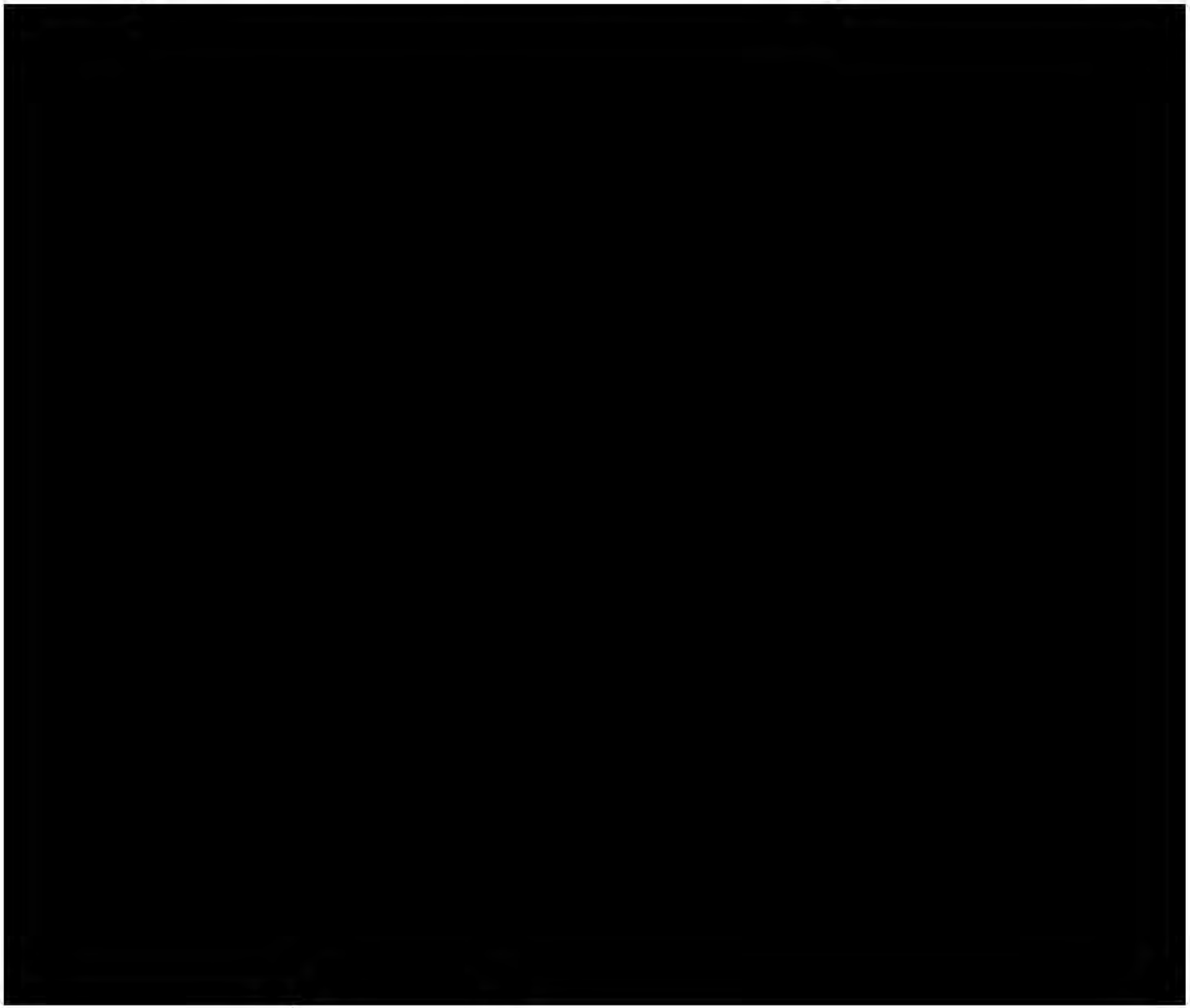
**HOME SEMICONDUCTOR CLAIM CHART**

| | |
|---|---|
| wherein the address sequencer generates a second address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]



[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim 14 | |
|---|---|
| An address generator for a random access memory, comprising: | [redacted] |
| an address sequencer having a clock input terminal, a preset terminal, and an output terminal; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| an internal address enable switch connected between the output terminal of the address sequencer and an output terminal of the address generator; | [redacted] |
| an external address enable switch | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| connected between an address input terminal of the address generator and the output terminal of the address generator; | [redacted] |
| wherein the address sequencer generates a second | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

| | |
|---|---|
| address in a sequence of addresses while a first address is being supplied to the output terminal of the address generator by the external address enable switch, | [redacted] |

[redacted]

HOME SEMICONDUCTOR CLAIM CHART

[redacted]



[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| | |
|---|---|
| wherein the address sequencer includes a counter having a master portion and a slave portion. | [redacted] |

[redacted]

# EXHIBIT D

[redacted]

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| sidewalls of the gate electrode; | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) etching an opening through the insulating layer self-aligned and borderless to | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| the diffusion region by using the silicon nitride layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode. | [redacted] |
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and<br>planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |
| (d) etching an opening | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| prior to forming the barrier layer. | [redacted] |
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| nitride on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **12.** The method as claimed in claim 9, wherein said insulating layer comprises a layer of borophosphosilicate glass. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | |
|---|---|
| electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) etching an opening through the insulating layer | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| nitride on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **12.** The method as claimed in claim 9, wherein said insulating layer comprises a layer of borophosphosilicate glass. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |
| (d) etching an opening | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | |
|---|---|
| prior to forming the barrier layer. | [redacted] |
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| nitride on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **12.** The method as claimed in claim 9, wherein said insulating layer comprises a layer of borophosphosilicate glass. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |
| (c) forming a conformal layer of silicon nitride overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| etch stop; and | [redacted] |
| (e) anisotropically etching the silicon nitride layer | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon nitride on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| **Claim** | [redacted] |
|---|---|
| | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and<br>planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |
| (b) forming a conformal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |
| (b) forming a conformal | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (c) forming an insulating layer overlying the barrier | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| layer; | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| the barrier layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |
| (b) forming a conformal layer of etch barrier material | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| the barrier layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
| --- | --- |
| diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |
| **2.** The method as claimed in claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **9.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon, said gate electrode comprising a capping layer; | [redacted] |
| (b) forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation; | [redacted] |
| (c) forming a conformal layer of silicon nitride | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |
| (d) forming an insulating layer overlying the conformal layer of silicon nitride; | [redacted] |
| (e) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the silicon nitride layer as an etch stop; and | [redacted] |
| (f) anisotropically etching the silicon nitride layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of silicon | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| nitride on the sidewall of the gate electrode. | [redacted] |
| **10.** The method as claimed in claim 9, wherein said capping layer is a silicon nitride layer. | [redacted] |
| **11**. The method as claimed in claim 9, wherein said conformal layer of silicon nitride has a thickness between about 100 to 500 Å. | [redacted] |
| **13.** The method as claimed in claim 9, wherein step (d) comprises: | |
| depositing an insulating layer overlying the conformal layer of silicon nitride; and<br>planarizing the insulating layer. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **14.** The method as claimed in claim 9, further comprising forming a conductive plug in said opening to electrically connect to the diffusion region. | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| **1.** A method for forming a self-aligned contact hole, comprising the steps of: | [redacted] |
| (a) providing a semiconductor substrate having a gate electrode and a diffusion region thereon; | [redacted] |
| (b) forming a conformal layer of etch barrier material overlying the substrate surface including the diffusion region and the upper surface and the sidewalls of the gate electrode; | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| (c) forming an insulating layer overlying the barrier layer; | [redacted] |
| (d) etching an opening through the insulating layer self-aligned and borderless to the diffusion region by using the barrier layer as an etch stop; and | [redacted] |
| (e) anisotropically etching the barrier layer underneath the opening, thereby exposing the diffusion region and simultaneously forming a spacer of the etch barrier material on the sidewall of the gate electrode. | [redacted] |
| **2.** The method as claimed in | [redacted] |

[redacted]

**HOME SEMICONDUCTOR CLAIM CHART**

[redacted]

| Claim | [redacted] |
|---|---|
| claim 1, further comprising a step of forming an oxide layer over the diffusion region and on the sidewalls of the gate electrode by thermal oxidation prior to forming the barrier layer. | [redacted] |