Jon A. Birmingham (CA SBN 271034)
FITCH, EVEN, TABIN & FLANNERY LLP
21700 Oxnard Street, Suite 1740
Woodland Hills, California 91367
Telephone: (818) 715-7025
Facsimile: (818) 715-7033
Email: jbirmi@fitcheven.com

Timothy P. Maloney (*admitted pro hac vice*)
tpmalo@fitcheven.com
Joseph F. Marinelli (*admitted pro hac vice*)
jmarinelli@fitcheven.com
David A. Gosse (*admitted pro hac vice*)
dgosse@fitcheven.com
FITCH, EVEN, TABIN & FLANNERY LLP
120 South LaSalle Street, Suite 2100
Chicago, Illinois 60603
Telephone: (312) 577-7000
Facsimile: (312) 577-7007

Attorneys for Plaintiff,
LONE STAR SILICON INNOVATIONS LLC

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

LONE STAR SILICON INNOVATIONS LLC, Plaintiff, v. UNITED MICROELECTRONICS CORPORATION, UMC GROUP (USA), and ADVANCED MICRO DEVICES, INC., Defendants.	Case No.: 3:17-cv-04033-WHA **FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT** DEMAND FOR JURY TRIAL

Plaintiff, Lone Star Silicon Innovations LLC ("Lone Star"), complains against Defendants United Microelectronics Corporation ("UMC"), UMC Group (USA) ("UMC-USA") (collectively, "the UMC Defendants") and Advanced Micro Devices, Inc. ("AMD") (together,"Defendants") as follows:

NATURE OF ACTION

1. This is an action for patent infringement of United States Patent Nos. 5,973,372, and 6,388,330 (collectively, the "Patents in Suit") under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.*

THE PARTIES

2. Plaintiff Lone Star is a corporation organized and existing under the laws of the State of Texas with its principal place of business at 8105 Rasor Blvd., Suite 210, Plano, TX 75024. Lone Star is in the business of licensing patented technology. Lone Star is the assignee of the Patents in Suit.

3. Defendant UMC is a corporation organized under the laws of Taiwan, with its principal place of business at No. 3 Li-Hsin Road II, Hsinchu Science Park, Hsinchu City, Taiwan, Republic of China. Defendant UMC conducts business in and is doing business in California and in this District and elsewhere in the United States, including, without limitation, using, promoting, offering to sell, importing, and/or selling integrated circuit devices that embody and/or are made using the patented technology, and enabling end-user purchasers to use such devices in this District.

4. Defendant UMC-USA is a corporation organized under the laws of the State of California, with its principal place of business at 488 Deguigne Drive, Sunnyvale, CA 94085. UMC-USA's registered agent for service of process in the State of California is Megan Su, 488 Deguigne Dr., Sunnyvale, California 94085. On information and belief, UMC-USA is a wholly-owned subsidiary of UMC, and is responsible for all sales of UMC's integrated circuit devices in North America. Defendant UMC-USA conducts business in and is doing business in California and in this District and elsewhere in the United States, including, without limitation, using, promoting, offering to sell, importing, and/or selling integrated circuit devices and/or devices that incorporate memory devices that embody the patented technology, and enabling end-user purchasers to use such devices in this District.

5. Upon information and belief, UMC controls and is the majority owner of UMC-USA, and

the UMC Defendants are joint tortfeasors with one another with respect to the matters alleged herein.

6. Advanced Micro Devices, Inc. ("AMD") is a corporation organized and existing under the law of the State of Delaware, and maintains its principal place of business at One AMD Place, Sunnyvale, California 94085.

7. As alleged in more detail below, AMD previously transferred rights in the Patents in Suit to Lone Star pursuant to a Patent Transfer Agreement effective August 4, 2016, which was amended on or about November 23, 2016, a copy of which is attached as Exhibit 1 (collectively "the Patent Transfer Agreement"). The rights transferred to Lone Star included "all rights to pursue damages, injunctive relief and other remedies for past, current and future infringement of" the Patents in Suit. The Court previously held that Lone Star lacked sufficient rights to bring suit against the UMC Defendants without AMD, and dismissed the action without prejudice. (Dkt. No. 80, January 20, 2018 Order). Limestone appealed the decision of the Court to Federal Circuit, arguing that it had all substantial rights to the Patent-in-Suit, and, alternatively, that if it did not that it did not have all substantial rights to the Patents in Suit then it should be allowed join AMD. The Federal Circuit held that Lone Star did not have all substantial rights under the Patents in Suit and that some of the substantial rights were held by AMD. *Lone Star Silicon Innovations LLC v. Nanya Tech. Corp et al.*, 925 F.3d 1225, 1229–34 (Fed. Cir. 2019). The Federal Circuit vacated the decision of the Court to dismiss this action, and remanded the case with instructions that Lone Star be permitted an opportunity to join AMD under Fed. R. Civ. P. 19(a). *Id.* at 1236–1239. The Federal Circuit instructed the Court to consider whether AMD's joinder is feasible and, "[i]f so, then AMD must be joined— involuntarily if need be." *Id.* at 1236.

8. In view of the rulings of this Court and of the Federal Circuit that AMD holds some substantial rights in the Patents in Suit, AMD should be joined as a required party to this action. AMD has an implied legal obligation to Lone Star to allow its name to be used as joined co-plaintiff in order to assure that Lone Star can enforce the rights granted to Lone Star under the Patent Transfer Agreement. Lone Star requested that AMD join this action as a plaintiff, but AMD declined that request and has refused to voluntarily join as a plaintiff. Joining AMD is feasible because AMD is subject to service of process and to personal jurisdiction in this Court, and such joinder would not divest the Court of subject

matter jurisdiction and would not make venue improper.

9. Rule 19(a)(2) permits joining AMD as a defendant or as an involuntary plaintiff. Under the "primary purpose" test applied in the Ninth Circuit, a district court should align those parties whose interests coincide respecting the primary matter in dispute. Realignment of AMD as a plaintiff is appropriate because the primary matter in dispute is infringement and validity of the Patents in Suit and Lone Star's request for infringement damages. The interests of AMD and Lone Star coincide with respect to the primary matter in dispute because AMD is the original owner of the Patents in Suit, is a party to the Patent Transfer Agreement, and has a contingent financial interest in any recovery.

JURISDICTION AND VENUE

10. On October 7, 2016, Lone Star initiated this action against the UMC Defendants under the Patent Laws of the United States, Title 35 of the United States Code in the District Court for the Eastern District of Texas. On February 28, 2017, the UMC Defendants moved to transfer venue to this District. Case 2:16-cv-01216-JRG-RSP, Docket No. 16. On May 22, 2017, the Supreme Court decided *TC Heartland LLC v. Kraft Foods Group Brands LLC*, 137 S.Ct. 1514 (2017). On June 19, 2017, in light of the *TC Heartland* decision, Lone Star conceded to transfer the action to this District. On July 14, 2017, the District Court for the Eastern District of Texas transferred the action to this District. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

11. UMC-USA is subject to personal jurisdiction in this Court because it has an established place of business in this District. On information and belief, the UMC Defendants are also subject to this Court's specific and general personal jurisdiction pursuant to due process and/or the California Long Arm Statute, due at least to their substantial business conducted in this forum, directly and/or through intermediaries, including (i) having solicited business in the State of California, having transacted business within the State of California, and having attempted to derive financial benefit from residents of the State of California, including benefits directly related to the instant patent infringement causes of action set forth herein; (ii) having placed their products and services into the stream of commerce throughout the United States and having been actively engaged in transacting business in California and in this District; and (iii) either alone or in conjunction with others, having committed acts of infringement within

California and in this District. On information and belief, the UMC Defendants, directly and/or through intermediaries, have advertised (including through websites), offered to sell, sold and/or distributed infringing products, and/or have induced the sale and use of infringing products in the United States and in California. The UMC Defendants have, directly or through their distribution network, purposefully and voluntarily placed such products in the stream of commerce knowing and expecting them to be purchased and used by consumers in California and in this District. Each UMC Defendant has either committed direct infringement in California or committed indirect infringement based on acts of direct infringement in California and from UMC-USA's location in Sunnyvale, California. Further, on information and belief, the UMC Defendants are subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to individuals in California and in this District.

12. On information and belief, the UMC Defendants do one or more of the following with integrated circuit devices and/or devices that incorporate such devices that they manufacture: (a) import these devices into the United States for sale to consumers, including consumers in California; (b) sell them or offer them for sale in the United States, including to customers in California; and (c) sell them to customers who incorporate them into products that such customers import, sell or offer for sale in the United States, including in California.

13. AMD is subject to personal jurisdiction in this Court because it has an established place of business in this District. On information and belief, AMD is also subject to this Court's specific and general personal jurisdiction pursuant to due process and/or the California Long Arm Statute, due at least to its substantial business conducted in this forum, directly and/or through intermediaries, including (a) having solicited business in the State of California, having transacted business within the State of California, and having attempted to derive financial benefit from residents of the State of California; (b) having placed its products and services into the stream of commerce throughout the United States and having been actively engaged in transacting business in California and in this District; and (c) having consented to jurisdiction and venue in the United States District Court for the Northern District of

California with respect to all civil actions or other legal proceedings directly arising between the Lone Stare and AMD under the Patent Transfer Agreement.

14. Venue lies in this District pursuant to 28 U.S.C. §§ 1391 and 1400. Defendant UMC-USA is subject to personal jurisdiction in this District, has a regular and established place of business within this District, resides in this District, and has committed acts of infringement within this District. Defendant UMC-USA maintains and operates at least one facility within this District. In addition, venue is proper in this District for Defendant UMC pursuant to 28 U.S.C. § 1391(c)(3) because it is not resident in the United States, and therefore may be sued in any federal judicial district. Venue is proper in this District as to AMD under 28 U.S.C. §§ 1391 and 1400 because it is subject to personal jurisdiction in this District and resides in this District.

THE PATENTS IN SUIT

15. On October 26, 1999, U.S. Patent No. 5,973,372 ("the '372 patent"), entitled "Silicided Shallow Junction Transistor Formation And Structure With High And Low Breakdown Voltages," a copy of which is attached hereto as Exhibit 2, was duly and legally issued. The '372 patent issued from U.S. patent application Serial Number 08/986,283 filed December 6, 1997, and discloses and relates to the design of and processes for fabricating semiconductor devices.

16. In an assignment recorded in the United States Patent Office Reel/Frame 009316/0047 on July 16, 1998, the inventors of the inventions contained in the '372 patent assigned all right, title, and interest in the '372 patent and all inventions contained therein to AMD. An assignment recorded in the United States Patent Office on August 5, 2016, Reel/Frame 039597/0957, indicates that AMD assigned "all of [its] entire right, title and interest in and to" the '372 patent to Lone Star, including all rights "in and to causes of actions and enforcement rights" and "all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of" the '372 patent. The assignment of the '372 patent from AMD to Lone Star was made subject to the terms and conditions of the Patent Transfer Agreement (which was inadvertently referenced as a Confidential Purchase and Sale Agreement in the recorded assignment document). Lone Star has the right to sue the UMC Defendants for infringement and

collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement of the '372 patent.

17. The validity of the '372 patent was challenged before the United States Patents and Trademark Office in an *inter partes* review proceeding numbered IPR2017-01513. *Inter partes* review of the '372 patent was denied.

18. On May 14, 2002, U.S. Patent No. 6,388,330 ("the '330 patent"), entitled "Low Dielectric Constant Etch Stop Layers In Integrated Circuit Interconnects," a copy of which is attached hereto as Exhibit 3, was duly and legally issued. The '330 patent issued from U.S. patent application Serial Number 09/776,012 filed February 1, 2001, and discloses and relates to the design of and processes for fabricating semiconductor devices.

19. In an assignment recorded in the United States Patent Office on February 2, 2001, Reel/Frame 011530/0755, the inventors of the inventions contained in the '330 patent assigned all right, title, and interest in the '330 patent and all inventions contained therein to AMD. An assignment recorded in the United States Patent Office on August 5, 2016, Reel/Frame 039597/0957, indicates that AMD assigned "all of [its] entire right, title and interest in and to" the '330 patent to Lone Star, including all rights "in and to causes of actions and enforcement rights" and "all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of" the '330 patent. The assignment of the '330 patent from AMD to Lone Star was made subject to the terms and conditions of the Patent Transfer Agreement (which was inadvertently referenced as a Confidential Purchase and Sale Agreement in the recorded assignment document). Lone Star has the right to sue the UMC Defendants for infringement and collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement of the '330 patent.

20. The validity of the '330 patent was challenged before the United States Patents and Trademark Office in *inter partes* review proceedings numbered: IPR2017-01566, IPR2017-01869, IPR2018-00062, and IPR2018-00087. Each of those *inter partes* review proceedings were instituted and each proceeded to a final written decision except IPR2018-00087 which was terminated prior to entry of a final written decision. In IPR2017-01566, claims 1, 2, 5–7, and 10 were found to be invalid. Lone Star

has appealed that decision to the Federal Circuit (Appeal No. 19-1669) with respect to claim 2. In IPR2017-01869 claims 1, 4–6, 9, and 10 were found to be invalid. In IPR2018-00062 claims 1, 5, 6, and 10 were found to be invalid. In both IPR2017-01869 and IPR2018-00062, claim 2 was not shown to be invalid. Nanya has appealed the Board's final written decision in IPR2018-00062, with respect to claim 2, to the Federal Circuit (Appeal No. 19-2030). The Board's final written decision in IPR2017-01869, with respect to claim 2, was not appealed.

LONE STAR'S STANDING TO BRING THIS LAWSUIT

21. Lone Star and AMD have standing to bring this action because together they possess all substantial rights to the Patents in Suit.

22. The Patent Transfer Agreement refers interchangeably to "Listed Patents" (see Exhibit A thereof) and "Assigned Patents" (see Exhibit B thereof). The Patents in Suit are included among the Listed Patents and the Assigned Patents. The Patent Transfer Agreement includes a representation that AMD, or one of its Affiliates, has good and marketable title to each Listed Patent, "including all rights, title, and interest in each such Listed Patent and the right to sue for past, present and future infringement thereof," and is the original assignee of the Listed Patents. (Ex. 1, §§ 6.1(b)(i) and (ii).) The Patent Transfer Agreement purports to assign to Lone Star "all right, title and interest in, to and under the Assigned Patents" including "any and all legal rights entitled by [AMD] and all rights of AMD to sue for past, present and future infringement of any and all of the Assigned Patents." (Ex. 1, § 2.1.) The Patent Transfer Agreement also states that AMD assigned to Lone Star "all right, title and interest in, to and under all causes of action and enforcement rights, whether known, unknown, currently pending, filed, or otherwise, for the Assigned Patents, including all rights to pursue damages, injunctive relief and other remedies for past, current and future infringement of the Assigned Patents." (Ex. 1, § 2.2.) Lone Star also received all rights "to collect royalties under such Assigned Patents, to prosecute all existing Assigned Patents worldwide, to apply for additional Assigned Patents worldwide and to have Assigned Patents issue in the name of Lone Star." (Ex. 1, § 2.1.)

23. As consideration for assigning the Assigned Patents to Lone Star, AMD is entitled to deferred compensation in the form of "Contingent Payments" based on any proceeds generated by Lone Star's patent enforcement and licensing efforts. (Ex. 1 at § 5.1.)

24. Pursuant to the Patent Transfer Agreement and as part of the consideration provided to AMD, Lone Star contractually granted a non-exclusive license back to AMD, effective as of the Effective Date. The rights granted to AMD include, inter alia, the right to make, offer for sale and sell AMD products covered by the Assigned Patents. (Ex. 1, § 4.1.)

25. The Patent Transfer Agreement acknowledges that the Assigned Patents are subject to certain pre-existing rights previously extended directly or indirectly by AMD to certain third parties, and reflects the parties' commitment to respect those rights. These are defined as "Existing Encumbrances," which may include, for example, pre-existing patent licenses, covenants not to sue, releases for past infringement granted by AMD, and pre-existing commitments relating to AMD's activities in standardization activities or patent pool activities. (Ex. 1, § 1.) Lone Star acknowledged that the Assigned Patents are subject to these Existing Encumbrances, and "commit[ted] to comply with such Existing Encumbrances. . . ." (Ex. 1, § 2.3.)

26. The Patent Transfer Agreement includes a list of "Unlicensed Third Party Entities" that are "not authorized or otherwise granted any rights (other than potentially by an implied license running with [AMD's] Licensed Products) by AMD to the Assigned Patents to use, develop, copy, modify, import, make and have made, offer for sale, sell, lease, import, export, distribute, demonstrate, display, transfer and/or otherwise exploit or dispose of a product or service by the Unlicensed Third Party Entity." (Ex. 1, § 1 and Exhibit E.) AMD further represented and warranted that to its knowledge, none of the Unlicensed Third Party Entities have been granted any rights under the Assigned Patents by AMD or its Affiliates. (Ex. 1, § 6.1(b)(vii).) The UMC Defendants each qualify as an Unlicensed Third Party Entity.

27. As additional consideration, Lone Star further contractually agreed to provide notice to AMD in the event that Lone Star decided not to pay a renewal, annuity, or maintenance fee on any Assigned Patent, and to assign such patent back to AMD or AMD's chosen designee upon AMD's request. (Ex. 1, § 3.4.) This clause of the Patent Transfer Agreement is of no legal or practical effect on the

Assigned Patents because, as of the Effective Date, all maintenance fees had already been paid for the full remaining life of the patents.

28. For the purpose of protecting AMD's interest in Contingent Payments, Lone Star also agreed that it would not transfer its ownership of any Assigned Patents unless all such patents are transferred collectively, the proposed assignee agrees in writing (with copy to AMD) to be bound by the Patent Transfer Agreement as Lone Star's successor-in-interest, and AMD provides its written consent to the transfer, "which shall not be unreasonably withheld." (Ex. 1, § 2.6.)

29. The Federal Circuit confirmed that the Patent Transfer Agreement gave Lone Star constitutional standing to bring this suit. *Lone Star Silicon Innovations LLC*, 925 F.3d 1225 at 1235. As such, Lone Star holds the status of an exclusive licensee of the Patents in Suit for the purpose of standing and has standing to bring this action against the UMC Defendants with AMD joined as a co-plaintiff. As the transferor of substantial exclusionary rights in the Patents in Suit to Lone Star and the holder of a contractual financial interest in the damages relief sought herein and of other contractual warranties and covenants extended by Lone Star, AMD has been joined to assure that principles of prudential standing are satisfied to enable Lone Star to secure the relief sought herein. As alleged above, AMD must be joined as a co-party because such joinder is feasible.

THE UMC DEFENDANTS' INFRINGING PRODUCTS AND METHODS

30. UMC is in the business of manufacturing semiconductors or integrated circuits for others. Using its own processes and techniques, UMC makes chips to the design specifications of customers in industries such as communications, and consumer and computer products, with a focus on high growth, large volume applications, including for networking, telecommunications, internet, multimedia, and personal electronic devices. UMC publicly represents itself as one of the world's largest independent semiconductor foundries and a leader in semiconductor manufacturing process technologies. UMC's customers include fabless design companies, which design, develop, and distribute semiconductor products but do not maintain internal manufacturing capacity, and integrated device manufacturers, which have their own manufacturing as well as design, development, sales, and distribution. UMC owns or

controls and operates semiconductor fabrication facilities in Taiwan, Singapore, and China. UMC's sales in the U.S. and North America are made through its wholly-owned subsidiary UMC-USA.

31. The UMC Defendants make, use, sell, offer for sale, and/or import into the United States integrated circuit devices for use in devices such as field programmable gate array ("FPGA") devices, system on chip ("SoC") devices, wireless communications modems, application processors, cellular baseband processors, and other products incorporating such devices. The UMC Defendants' integrated circuit products are utilized in devices such as mobile phones, tablets, personal computers, wearable electronics, industrial and automotive systems, high-speed networking gear, and other commercial and consumer applications. The UMC Defendants primarily supply their semiconductor devices in wafer form, knowing and intending that they are further configured into finished semiconductor products that have been assembled and tested. The UMC Defendants' customers include integrated device manufacturers, such as Intel and STMicroelectronics, and fabless design companies, such as Xilinx, Broadcom, MediaTek, Realtek, Qualcomm, and Novatek.

32. The UMC Defendants have continued to develop and enhance their process technologies to enable the manufacture of semiconductor devices with smaller geometries, allowing the production of more integrated circuit dice per wafer. The UMC Defendants market and promote their 40-nanometer process node technology as supporting high performance and low power requirements of many customers who have engaged with the UMC Defendants for the design and high volume production of integrated circuits based on the 40nm process technology. The UMC Defendants have represented that their 40nm process node utilizes techniques such as immersion lithography, ultra shallow junction transistor design, mobility enhancement techniques, and ultra low-k dielectrics for maximum power and performance optimization. The UMC Defendants' 40nm process consists of a low power platform adapted for low power and low leakage design requirements for mobile and consumer applications, and a generic platform that is optimized for a broad range of consumer and high-speed applications.

33. The UMC Defendants have also implemented 28nm process technologies for applications that require the highest performance with the lowest power leakage. Their 28nm process technology platform includes the UMC 28nm High Performance Low Power (28HLP) process, which utilizes poly

SiON technologies. The UMC Defendants market the 28HLP process for portable applications and consumer electronics such as mobile phones, wireless ICs, and TVs. The UMC Defendants have also implemented high-k/metal gate stack technologies within their 28nm process node. The UMC Defendants provide their 28HPCU process for a broad range of devices such as application processors, cellular baseband processors, and other integrated circuits for applications such as WLAN, tablet computers, FPGAs, and networking gear. The UMC Defendants' 28HPCU+ process technology offers improved transistor performance, and their 28uLP process offers lower core Vcc for ultra low power system on chip devices and other integrated circuits for applications such as wearable consumer devices, Internet of Things, and automotive systems.

34. Despite not having a license to the '372 or '330 patents, the UMC Defendants' integrated circuit products made using their 40nm and 28nm process node technologies adopt the designs claimed in these patents.

FIRST CAUSE OF ACTION – INFRINGEMENT OF THE '372 PATENT

35. Plaintiff hereby repeats and re-alleges the allegations contained in paragraphs 1 to 34, as if fully set forth herein.

36. The UMC Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have in the past and continue to directly infringe the '372 patent, including at least claims 1, 4, 5 and 6, pursuant to 35 U.S.C. § 271(a) by using, selling, offering to sell, and/or importing integrated circuit devices that embody the inventions claimed in the '372 patent, within the United States and within this District. In violation of the '372 patent, for example, the UMC Defendants' accused integrated circuit devices include: an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made comprising: a single crystalline silicon substrate with a upper surface region; a shallow junction for each of the source and drain of the transistor underlying said upper surface of the silicon substrate; a metal silicide layer having a lower surface disposed adjacent the shallow junction of each of the source and drain in the silicon substrate and above said upper surface of the silicon substrate; and an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the

shallow junction of each of the source and drain, whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each of the source and the drain.

37. The UMC Defendants have been and are engaged in one or more of these direct infringing activities related to their integrated circuit devices having transistors and related structures manufactured using their 40nm process node, a representative example being the integrated circuit devices manufactured for Xilinx for resale as the Xilinx XC6VLX130 Virtex-6 FPGA products. The UMC Defendants' integrated circuit devices having transistors and related structures manufactured using their 28nm HLP, 28nm HPCU, 28nm HPCU+ and 28nm uLP process nodes are also infringing, a representative example being the integrated circuit devices manufactured for Qualcomm for resale as the Qualcomm MDM9625M LTE Modem.

38. On information and belief, integrated circuit devices made using any of the 40nm, 28nm HLP, 28nm HPCU, 28nm HPCU+ and 28nm uLP process nodes infringe at least claims 1, 4 and 6 of the '372 patent, and integrated circuit devices made using any of the 40nm and the 28nm HLP process nodes infringe at least claim 5 of the '372 patent. Such infringing integrated circuits are referred to hereinafter as "the '372 Accused Products."

39. The UMC Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have been and are now indirectly infringing the '372 patent, including at least claims 1, 4, 5 and 6, pursuant to 35 U.S.C. § 271(b) by actively inducing acts of direct infringement performed by others. The UMC Defendants have actual notice of the '372 patent and the infringement alleged herein at least upon the service of the original Complaint in this action. Upon information and belief, the UMC Defendants have numerous lawyers and other active agents of the UMC Defendants and of its owned and controlled subsidiaries who regularly review patents and published patent applications relevant to technology in the fields of the Patents in Suit, specifically including patents directed to integrated circuit devices issued to competitors such as AMD, the original assignee of the '372 patent. Upon information and belief, the UMC Defendants have been issued over 4,470 patents, including over 200 patents prosecuted in the USPTO in the same classifications as the '372 patent, giving the UMC Defendants intimate knowledge of the art in fields relevant to this civil action. The UMC Defendants have had

previous actual notice of the '372 patent prior to the filing of the original Complaint in this action at least through its efforts to patent related technologies. The '372 patent is listed on the face of U.S. Patent No. 6,221,767 ("the '767 patent") issued to the UMC Defendants on April 24, 2001, indicating that it was among the references cited against and considered by the USPTO and the UMC Defendants during prosecution of '767 patent. Accordingly, the UMC Defendants have had actual notice of the '372 patent since at least the issue date of the '767 patent. The timing, circumstances and extent of the UMC Defendants obtaining actual knowledge of the '372 patent prior to the commencement of this lawsuit will be confirmed during discovery.

40. Upon gaining knowledge of the '372 patent, it was, or became, apparent to the UMC Defendants that the manufacture, sale, importing, offer for sale and use of their '372 Accused Products results in infringement of the '372 patent. Upon information and belief, the UMC Defendants have continued and will continue to engage in activities constituting inducement of infringement, notwithstanding their knowledge, or willful blindness thereto, that the activities they induce result in infringement of the '372 patent.

41. The '372 Accused Products are intended for integration into products known to be sold widely in the United States. The UMC Defendants make integrated circuit devices that embody the inventions claimed in the '372 patent, and those devices infringe when they are imported into, or sold, used, or offered for sale in, the United States. The UMC Defendants indirectly infringe by inducing customers (including fabless design companies and integrated semiconductor device manufacturers) and other downstream parties (such as makers of mobile devices, desktop computers and other devices) to import products that incorporate integrated circuit devices embodying inventions claimed in the '372 patent, or to sell or use such products, or offer them for sale, in the United States. For example, the UMC Defendants induce fabless design companies, integrated semiconductor device manufacturers, importers, resellers, and others who purchase or otherwise obtain devices manufactured at the UMC Defendant's overseas facilities to import devices embodying inventions recited in claims of the '372 patent, or to sell or use such devices, or offer them for sale in the United States without authority.

42. The UMC Defendants encourage customers, resellers or others to import into the United States and sell and use in the United States the '372 Accused Products embodying inventions claimed in the '372 patent with knowledge and the specific intent to cause the acts of direct infringement performed by these third parties. On information and belief, after the UMC Defendants obtained knowledge of the '372 patent, the '372 Accused Products have been and will continue to be imported into the United States and sold in large volumes by themselves and by others, such as customers, distributors, and resellers. The UMC Defendants work closely with their customers in the process of finalizing circuit designs and planning for the preparation of masks to be used in the manufacturing process, so that these aspects of the manufacturing process are optimized for the UMC Defendants' process technologies and equipment. The UMC Defendants also offer their customers outsourced semiconductor assembly and test services. The UMC Defendants are aware that the '372 Accused Products are integral components of the products incorporating them, that the infringing integrated circuits are built into the products and cannot be removed or disabled by a purchaser of the products containing the infringing integrated circuit devices, such that the UMC Defendants' customers will infringe one or more claims of the '372 patent by incorporating such integrated circuit devices in other products, and that subsequent importation, sale, and use of such products in the United States would be a direct infringement of the '372 patent. Therefore, the UMC Defendants are aware that their customers will infringe one or more claims of the '372 patent by selling, offering for sale, importing, and/or using the products supplied by the UMC Defendants.

43. The UMC Defendants directly benefit from and actively and knowingly encourage customers', resellers', and users' importation of these products into the United States and sale and use within the United States. The UMC Defendants actively encourage customers, resellers, and downstream users to import, use, and sell in the United States the '372 Accused Products that they manufacture and supply, including through advertising, marketing, and sales activities directed at United States sales. On information and belief, the UMC Defendants are aware of the size and importance of the United States market for customers of their products, and also distribute or supply these products intended for importation, use, and sale in the United States. The UMC Defendants routinely market their infringing integrated circuit products to third parties for inclusion in products that are sold to customers in the United

States. Defendant UMC-USA provides a direct sales outlet for these products in the United States. The UMC Defendants' marketing efforts show that they have specifically intended to and have induced direct infringement in the United States.

44. The UMC Defendants have engaged and will continue to engage in additional activities to specifically target the United States market for the '372 Accused Products and actively induce manufacturers, importers, resellers, customers, and end users to directly infringe one or more claims of the '372 patent in the United States. For example, the UMC Defendants have showcased their semiconductor manufacturing capabilities and process technologies at least through written materials distributed in the United States and through the www.umc.com website in an effort to showcase their process technology, manufacturing, testing, packaging, and market applications, and to encourage customers to engage the UMC Defendants to produce integrated circuits for inclusion in the customers' devices and products. These materials target fabless design companies and integrated semiconductor device manufacturers and generally companies that make, use, offer to sell, sell, or import in the United States products that use integrated circuit devices such as those made by the UMC Defendants. The UMC Defendants derive significant revenue by selling the '372 Accused Products to third parties who directly infringe the '372 patent in the United States.

45. The UMC Defendants' extensive sales and marketing efforts, sales volume, and partnerships all evidence their intent to induce companies to infringe one or more claims of the '372 patent by, using, offering to sell, selling, or importing products that incorporate the '372 Accused Products, in the United States. The UMC Defendants have had specific intent to induce infringement or have been willfully blind to the direct infringement they are inducing.

46. Upon information and belief, the UMC Defendants have continued and will continue to engage in activities constituting contributory infringement of the '372 patent, including at least claims 1, 4, 5 and 6 pursuant to 35 U.S.C. § 271(c). The UMC Defendants contributorily infringe with knowledge that the '372 Accused Products, or the use thereof, infringe the '372 patent. The UMC Defendants knowingly and intentionally contributed to the direct infringement of the '372 patent by others by supplying these integrated circuit devices that embody a material part of the claimed invention of the '372

patent, which are known by the UMC Defendants to be specially made or adapted for use in an infringing manner. For example, and without limitation, the '372 Accused Products are used in various end products, such as computers, networking gear, and mobile telephones. The '372 Accused Products are not staple articles or commodities of commerce suitable for non-infringing use and are especially made for or adapted for use in infringing the '372 patent. There are no substantial uses of the '372 Accused Products that do not infringe the '372 patent. By contributing a material part of the infringing computing products sold, offered for sale, imported, and used by their customers, resellers and users, the UMC Defendants have been and are now indirectly infringing the '372 patent under 35 U.S.C. § 271(c).

47. The UMC Defendants' direct and indirect infringement of the '372 patent has injured Lone Star, and Lone Star is entitled to recover damages adequate to compensate for such infringement pursuant to 35 U.S.C. § 284. Unless they cease their infringing activities, the UMC Defendants will continue to injure Lone Star by infringing the '372 patent.

48. On information and belief, The UMC Defendants acted egregiously and with willful misconduct in that their actions constituted direct or indirect infringement of a valid patent, and this was either known or so obvious that the UMC Defendants should have known about it. The UMC Defendants continue to infringe the '372 patent by making, using, selling, offering for sale, and importing in the United States the '372 Accused Products, and to induce the direct infringement of others performing these acts, or they have acted at least in reckless disregard of Lone Star's patent rights. On information and belief, the UMC Defendants will continue their infringement notwithstanding actual knowledge of the '372 patent and without a good faith basis to believe that their activities do not infringe any valid claim of the '372 patent. All infringement of the '372 patent following the UMC Defendants' knowledge of the '372 patent is willful and Lone Star is entitled to treble damages and attorneys' fees and costs incurred in this action under 35 U.S.C. §§ 284 and 285.

SECOND CAUSE OF ACTION – INFRINGEMENT OF THE '330 PATENT

49. Plaintiff hereby repeats and re-alleges the allegations contained in paragraphs 1 to 34, as if fully set forth herein.

50. The UMC Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have in the past and continue to directly infringe the '330 patent, including at least claim 2, pursuant to 35 U.S.C. § 271(a) by using, selling, offering to sell, and/or importing integrated circuit devices that embody the inventions claimed in the '330 patent, within the United States and within this District. In violation of the '330 patent, for example, the UMC Defendants' accused integrated circuit devices include: (a) a semiconductor substrate having a semiconductor device provided thereon; (b) a first dielectric layer formed over the semiconductor substrate having a first opening provided therein; (c) a first conductor core filling the first opening and connected to the semiconductor device; (d) an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5; (e) a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core; and (f) a second conductor core filling the second opening and connected to the first conductor core. The UMC Defendants further directly infringe the '330 patent because, for example, their accused integrated circuit devices include: (g) an etch stop layer that is a multilayer structure.

51. The UMC Defendants have been and are engaged in one or more of these direct infringing activities related to their integrated circuit devices manufactured using their 40nm process node, a representative example being the integrated circuit devices manufactured for Xilinx for resale as the Xilinx XC6VLX130 Virtex-6 FPGA products. The UMC Defendants' integrated circuit devices manufactured using their 28nm HLP, 28nm HPCU, 28nm HPCU+ and 28nm uLP process nodes are also infringing, a representative example being the integrated circuit devices manufactured for Qualcomm for resale as the Qualcomm MDM9625M LTE Modem. On information and belief, integrated circuit devices made using any of the 40nm, 28nm HLP, 28nm HPCU, 28nm HPCU+ and 28nm uLP process nodes infringe at least claim 2 of the '330 patent. Such infringing integrated circuits are referred to hereinafter as "the '330 Accused Products."

52. The UMC Defendants, directly and/or through their subsidiaries, affiliates, agents, and/or business partners, have been and are now indirectly infringing the '330 patent, including at least claim 2, pursuant to 35 U.S.C. § 271(b) by actively inducing acts of direct infringement performed by others. The

UMC Defendants have actual notice of the '330 patent and the infringement alleged herein at least upon the service of the original Complaint in this action. Upon information and belief, the UMC Defendants has numerous lawyers and other active agents of the UMC Defendants and of its owned and controlled subsidiaries who regularly review patents and published patent applications relevant to technology in the fields of the Patents in Suit, specifically including patents directed to semiconductor memory devices issued to competitors such as AMD, the original assignee of the '330 patent. Upon information and belief, the UMC Defendants have been issued over 4,470 patents, including over 103 patents prosecuted in the USPTO in the same classifications as the '330 patent, giving the UMC Defendants intimate knowledge of the art in fields relevant to this civil action. The UMC Defendants have had previous actual notice of the '330 patent prior to the filing of this Complaint at least through its efforts to patent related technologies. The timing, circumstances, and extent of the UMC Defendants obtaining actual knowledge of the '330 patent prior to the commencement of this lawsuit will be confirmed during discovery.

53. Upon gaining knowledge of the '330 patent, it was, or became, apparent to the UMC Defendants that the manufacture, sale, importing, offer for sale, and use of their '330 Accused Products results in infringement of the '330 patent. Upon information and belief, the UMC Defendants have continued and will continue to engage in activities constituting inducement of infringement, notwithstanding their knowledge, or willful blindness thereto, that the activities they induce result in infringement of the '330 patent.

54. The '330 Accused Products are intended for integration into products known to be sold widely in the United States. The UMC Defendants make integrated circuit devices that embody the inventions claimed in the '330 patent, and these devices infringe when they are imported into, or sold, used, or offered for sale in, the United States. The UMC Defendants indirectly infringe by inducing customers (including fabless design companies and integrated semiconductor device manufacturers) and other downstream parties (such as makers of mobile devices, desktop computers and other devices) to import products that incorporate integrated circuit devices embodying inventions claimed in the '330 patent, or to sell or use such products, or offer them for sale, in the United States. For example, the UMC Defendants induce fabless design companies, integrated semiconductor device manufacturers, importers,

resellers, and others who purchase or otherwise obtain devices manufactured at the UMC Defendant's overseas facilities to import devices embodying inventions recited in the asserted claim of the '330 patent, or to sell or use such devices, or offer them for sale in the United States without authority.

55. The UMC Defendants encourage customers, resellers, or others to import into the United States and sell and use in the United States the '330 Accused Products embodying inventions claimed in the '330 patent with knowledge and the specific intent to cause the acts of direct infringement performed by these third parties. On information and belief, after the UMC Defendants obtained knowledge of the '330 patent, the '330 Accused Products have been and will continue to be imported into the United States and sold in large volumes by them and by others, such as customers, distributors, and resellers. The UMC Defendants work closely with their customers in the process of finalizing circuit designs and planning for the preparation of masks to be used in the manufacturing process, so that these aspects of the manufacturing process are optimized for the UMC Defendants' process technologies and equipment. The UMC Defendants also offer their customers outsourced semiconductor assembly and test services. The UMC Defendants are aware that the '330 Accused Products are integral components of the products incorporating them, that the infringing integrated circuits are built into the products and cannot be removed or disabled by a purchaser of the products containing the infringing integrated circuit devices, such that the UMC Defendants' customers will infringe the asserted claim of the '330 patent by incorporating such integrated circuit devices in other products, and that subsequent importation, sale and use of such products in the United States would be a direct infringement of the '330 patent. Therefore, the UMC Defendants are aware that their customers will infringe the asserted claim of the '330 patent by selling, offering for sale, importing, and/or using the products supplied by the UMC Defendants.

56. The UMC Defendants directly benefit from and actively and knowingly encourage customers', resellers', and users' importation of these products into the United States and sale and use within the United States. The UMC Defendants actively encourage customers, resellers, and downstream users to import, use, and sell in the United States the '330 Accused Products that they manufacture and supply, including through advertising, marketing, and sales activities directed at United States sales. On information and belief, the UMC Defendants are aware of the size and importance of the United States

market for customers of their products, and also distribute or supply these products intended for importation, use, and sale in the United States. The UMC Defendants routinely market their infringing integrated circuit products to third parties for inclusion in products that are sold to customers in the United States. Defendant UMC-USA provides a direct sales outlet for these products in the United States. The UMC Defendants' marketing efforts show that they have specifically intended to and have induced direct infringement in the United States.

57. The UMC Defendants have engaged and will continue to engage in additional activities to specifically target the United States market for the '330 Accused Products and actively induce manufacturers, importers, resellers, customers, and end users to directly infringe the asserted claim of the '330 patent in the United States. For example, the UMC Defendants have showcased their semiconductor manufacturing capabilities and process technologies at least through written materials distributed in the United States and through the www.umc.com website in an effort to showcase their process technology, manufacturing, testing, packaging, and market applications, and to encourage customers to engage the UMC Defendants to produce integrated circuits for inclusion in the customers' devices and products. These materials target fabless design companies and integrated semiconductor device manufacturers and generally companies that make, use, offer to sell, sell, or import in the United States products that use integrated circuit devices such as those made by the UMC Defendants. The UMC Defendants derive significant revenue by selling the '330 Accused Products to third parties who directly infringe the '330 patent in the United States.

58. The UMC Defendants' extensive sales and marketing efforts, sales volume, and partnerships all evidence their intent to induce companies to infringe the asserted claim of the '330 patent by, using, offering to sell, selling, or importing products that incorporate the '330 Accused Products, in the United States. The UMC Defendants have had specific intent to induce infringement or have been willfully blind to the direct infringement they are inducing.

59. Upon information and belief, the UMC Defendants have continued and will continue to engage in activities constituting contributory infringement of the '330 patent, including at least claim 2, pursuant to 35 U.S.C. § 271(c). The UMC Defendants contributorily infringe with knowledge that the

'330 Accused Products, or the use thereof, infringe the '330 patent. The UMC Defendants knowingly and intentionally contributed to the direct infringement of the '330 patent by others by supplying these integrated circuit devices that embody a material part of the claimed invention of the '330 patent, which are known by the UMC Defendants to be specially made or adapted for use in an infringing manner. For example, and without limitation, the '330 Accused Products are used in various end products, such as computers, networking gear and mobile telephones. The '330 Accused Products are not staple articles or commodities of commerce suitable for non-infringing use and are especially made for or adapted for use in infringing the '330 patent. There are no substantial uses of the '330 Accused Products that do not infringe the '330 patent. By contributing a material part of the infringing computing products sold, offered for sale, imported and used by their customers, resellers and users, the UMC Defendants have been and are now indirectly infringing the '330 patent under 35 U.S.C. § 271(c).

60. The UMC Defendants' direct and indirect infringement of the '330 patent has injured Lone Star, and Lone Star is entitled to recover damages adequate to compensate for such infringement pursuant to 35 U.S.C. § 284. Unless they cease their infringing activities, the UMC Defendants will continue to injure Lone Star by infringing the '330 patent.

61. On information and belief, the UMC Defendants acted egregiously and with willful misconduct in that their actions constituted direct or indirect infringement of a valid patent, and this was either known or so obvious that the UMC Defendants should have known about it. The UMC Defendants continue to infringe the '330 patent by making, using, selling, offering for sale, and importing in the United States the '330 Accused Products, and to induce the direct infringement of others performing these acts, or they have acted at least in reckless disregard of Lone Star's patent rights. On information and belief, The UMC Defendants will continue their infringement notwithstanding actual knowledge of the '330 patent and without a good faith basis to believe that their activities do not infringe any valid claim of the '330 patent. All infringement of the '330 patent following The UMC Defendants' knowledge of the '330 patent is willful and Lone Star is entitled to treble damages and attorneys' fees and costs incurred in this action under 35 U.S.C. §§ 284 and 285.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs prays for:

1. Judgment that the '372, and '330 patents are each valid and enforceable;

2. Judgment that the '372, and '330 patents are infringed by the UMC Defendants;

3. Judgment that the UMC Defendants' acts of patent infringement relating to the patents are willful;

4. An award of damages arising out of the UMC Defendants' acts of patent infringement, together with pre-judgment and post-judgment interest;

5. Judgment that the damages so adjudged be trebled in accordance with 35 U.S.C. § 284;

6. An award of Plaintiff's attorneys' fees, costs and expenses incurred in this action in accordance with 35 U.S.C. § 285; and

7. Such other and further relief as the Court may deem just and proper.

RESERVATION OF RIGHTS

Plaintiff's investigation is ongoing, and certain material information remains in the sole possession of the UMC Defendants or third parties, which will be obtained via discovery herein. Plaintiff expressly reserves the right to amend or supplement the causes of action set forth herein in accordance with Rule 15 of the Federal Rules of Civil Procedure.

Respectfully,

Dated: September 19, 2019

FITCH, EVEN, TABIN & FLANNERY LLP

/s/ *Joseph F. Marinelli*
Joseph F. Marinelli (admitted *pro hac vice*)

Attorney for Plaintiff
LONE STAR SILICON INNOVATIONS LLC

JURY DEMAND

Plaintiff demands trial by jury of all issues triable of right by a jury.

Respectfully submitted,

Dated: September 19, 2019

FITCH, EVEN, TABIN & FLANNERY LLP

/s/ *Joseph F. Marinelli*
Joseph F. Marinelli (admitted *pro hac vice*)

Attorney for Plaintiff
LONE STAR SILICON INNOVATIONS LLC

Exhibit 1

AMD bank account information redacted pursuant to April 5, 2018 Order (Case No. 18-01680-WHA, D.I. 40)

Confidential

PATENT TRANSFER AGREEMENT

This PATENT TRANSFER AGREEMENT (this "**Agreement**") is entered into on August 4th, 2016 (the "**Effective Date**"), by and between Lone Star Silicon Innovations LLC, an entity organized under the laws of State of Texas having its primary place of business at 5204 Bluewater Drive, Frisco, TX 75034 . ("**Lone Star**") and Advanced Micro Devices, Inc., a Delaware corporation ("**AMD**"). Lone Star and AMD are herein referred to separately as "a party" or collectively as "the parties."

RECITALS

Whereas Lone Star wishes to acquire certain patents and patent applications owned by AMD; and

Whereas AMD is interested in selling such certain patents and patent applications to Lone Star while retaining a license and certain sub-license rights to such patents and patent applications;

Now therefore, in consideration of the mutual covenants and conditions stated herein, and for other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the parties hereby agree as set forth herein.

AGREEMENT

1. DEFINITIONS

"**Affiliate**" means, with respect to a Person, any Person Controlling, Controlled by, or under common Control with such Person. A Person shall be deemed an Affiliate only so long as such Control exists.

"**Agreement**" shall have the meaning set forth in the introduction.

"**Alternate Forum**" shall have the meaning set forth in Section 7.1.

"**AMD**" shall have the meaning set forth in the introduction.

"**Assigned Patents**" means and includes all patents listed in **Exhibit A** hereto. In addition, "Assigned Patents" also includes the following to the extent owned and assignable by AMD: (i) all patents and patent applications listed in **Exhibit B** hereto, (ii) applications for the foregoing in all countries of the world, and (iii) any other procedure or formality with respect to the aforesaid that can result in an enforceable patent right anywhere in the world.

"**Assignment**" shall have the meaning set forth in Section 2.1.

"**Confidentiality and Common Interest Agreement**" means an agreement, in the form set forth on Exhibit D, setting forth the terms under which Lone Star and AMD will seek to protect certain information relating to the Assigned Patents as confidential and/or under the common interest privilege.

"**Control**" means, with respect to a Person, (a) direct or indirect ownership of more than fifty percent (50%) of the outstanding shares representing the right to vote for members of the board of directors or other managing officers of such Person, or (b) for a Person that does not have outstanding shares, more

than fifty percent (50%) of the direct or indirect ownership interest representing the right to make decisions for such Person.

"**Lone Star**" shall have the meaning set forth in the introduction.

"**Disclosure Schedule**" shall refer to the schedule of Exhibit F hereto.

"**Effective Date**" shall have the meaning set forth in the introduction.

"**Existing Encumbrances**" means, in relation to the Assigned Patents, (a) pre-existing patent licenses, covenants not to assert, promises or agreements to license, and/or similar patent immunities; (b) rights to renew or extend pre-existing patent licenses exercised unilaterally by third parties (such as legally binding options); (c) releases for past infringement; and/or (d) pre-existing commitments related to AMD's or its Affiliates' standardization activities or patent pool activities, and other pre-existing specification-related or standards-related licenses, covenants and promises of AMD or any of its Affiliates, which, in each of (a), (b), (c) and (d), shall transfer in connection with the transfer of the Assigned Patent(s) and/or which AMD or any of its Affiliates has committed to maintain in connection with the transfer of such Assigned Patent(s).

"**Former Affiliate**" shall have the meaning set forth in Section 4.1(b)(i)

"**Former Asset**" shall have the meaning set forth in Section 4.1(b)(ii).

"**Forum**" shall have the meaning set forth in Section 7.1.

"**Governmental Authority**" means any governmental agency or authority of the United States, any domestic state or any foreign country, and any political subdivision or agency thereof, and includes any authority having governmental or quasi-governmental powers, including any administrative agency or commission.

"**Grantee**" shall have the meaning set forth in Section 4.1(a).

"**Grantor**" shall have the meaning set forth in Section 4.1(a).

"**Knowledge**" shall have the meaning set forth in Section 6.1.

"**Law**" or "**law**" means all laws, statutes, ordinances, regulations and similar mandates of any Governmental Authority having the effect of law in any jurisdiction, including any judgment, order, decision, writ, injunction, ruling or decree of, or any settlement under the jurisdiction of, any court or Governmental Authority having the effect of law in each such jurisdiction.

"**Law Firm**" means Fitch, Even, Tabin & Flannery LLP, having its principal office at 120 S. LaSalle Street, Suite 1600, Chicago, IL 60603, or such other law firm as Lone Star may retain as its litigation counsel in enforcing, licensing or otherwise monetizing one or more of the Assigned Patents.

"**Licensed Products**" means, with respect to a Person, all of its software, hardware, products, designs, services, and activities.

"**Listed Patents**" means the patents and patent applications listed in Exhibit A hereto.

"**Person**" means any individual, person, trust, corporation, partnership, joint venture, limited liability

company, association, unincorporated organization, or any foreign counterpart of any of the foregoing, or any other legal or governmental entity or organization.

"**Proceeds**" means the receipt and/or collection of anything of value, including without limitation monies, property or compensation of any kind, or any other thing of value received by Lone Star by judgment, award, agreement, license or cross-license, patent sale, settlement, alternative dispute resolution or otherwise, directly or indirectly, in connection, directly or indirectly, with the monetization of the Assigned Patents without regard to any taxes, duties, levies, fees (contingent or otherwise), excises or tariffs imposed on any of Lone Star's activities in connection with this Agreement.

"**Unlicensed Third Party Entity**" means a Person (or an Affiliate thereof) which is not authorized or otherwise granted any rights (other than potentially by an implied license running with a Grantee's Licensed Products) by AMD to the Assigned Patents to use, develop, copy, modify, import, make and have made, offer for sale, sell, lease, import, export, distribute, demonstrate, display, transfer and/or otherwise exploit or dispose of a product or service by the Unlicensed Third Party Entity. Unlicensed Third Party Entity shall be deemed to only include the Persons listed in Exhibit E and their Affiliates and all other Persons that the Parties agree in writing in the future to add to Exhibit E.

2. ASSIGNMENT OF PATENTS; COMPLIANCE WITH EXISTING ENCUMBRANCES

2.1 Patent Assignment. AMD shall, and hereby does, assign to Lone Star, and Lone Star hereby acquires and accepts from AMD all right, title and interest in, to and under the Assigned Patents on an "**AS IS**" basis, subject to section 6.1(b)(vii), including any and all inventions and discoveries claimed therein, any and all legal rights entitled by the original owner of the Assigned Patents and all rights of AMD to sue for past, present and future infringement of any and all of the Assigned Patents, to collect royalties under such Assigned Patents, to prosecute all existing Assigned Patents worldwide, to apply for additional Assigned Patents worldwide and to have Assigned Patents issue in the name of Lone Star.

2.2 Assignment of Causes of Action. AMD shall, and hereby does, assign to Lone Star, and Lone Star hereby acquires and accepts from AMD all right, title and interest in, to and under all causes of action and enforcement rights, whether known, unknown, currently pending, filed, or otherwise, for the Assigned Patents, including all rights to pursue damages, injunctive relief and other remedies for past, current and future infringement of the Assigned Patents. To the extent permissible by law, AMD shall, and hereby does, transfer all rights to assert any work product and attorney client privilege that relate exclusively to the prosecution and enforcement of the Assigned Patents and embodied by or contained in the prosecution history files transferred pursuant to Section 3.2.

2.3 Existing Encumbrances. Subject to section 6.1(b)(vii), the Assigned Patents are hereby assigned and transferred to Lone Star, and Lone Star hereby acquires and accepts from AMD, that the Assigned Patents are subject to the Existing Encumbrances and the license and other rights granted under Section 4, and Lone Star hereby commits to comply with such Existing Encumbrances and the license and other rights granted under Section 4, and to make any and every future sale, transfer, assignment, lien, mortgage or other encumbrance of the Assigned Patents subject to the Existing Encumbrances and the license and other rights granted under Section 4, and compliance therewith.

2.4 Additional Information. For the avoidance of doubt, any pre-existing patent license agreements or other agreements related to the Assigned Patents, including, without limitation, any related royalty payments, shall not be assigned or transferred to Lone Star. AMD hereby commits that it shall, at all times, use reasonable efforts to promptly provide Lone Star, at Lone Star's reasonable request, a description of the type of products and/or services that are or are not covered by any Existing Encumbrances that AMD or any of its Affiliates may be committed to with respect to any specific named

entity under the Assigned Patents, in each case subject to any confidentiality obligations AMD or any of its Affiliates may have under any Existing Encumbrances. If the information requested by Lone Star under this Section 2.4 is subject to non-disclosure obligations preventing disclosure to Lone Star, AMD and Lone Star shall negotiate in good faith and seek to identify a method for providing Lone Star with reasonable access to useful information without breaching any such confidentiality obligations.

2.5 Covenant of AMD. AMD, on behalf of itself and its Affiliates, covenants that it shall not commence, direct or control any legal action seeking to render any of the Assigned Patents invalid or unenforceable nor shall it assist others, directly or indirectly, to do any of the foregoing. However, responses to third party subpoenas, requests for information by a Governmental Authority or court orders shall not be considered assistance hereunder.

2.6 Patent Resale. Any assignment of an Assigned Patent in violation of this Section 2.6 shall be void ab initio. Lone Star will not transfer ownership of any of the Assigned Patents unless: (a) all Assigned Patents are transferred collectively; (b) the proposed successor-in-interest agrees to be bound by this Agreement (with the successor-in-interest taking the place of Lone Star for all purposes of this Agreement) including, but not limited to, obtaining ownership of any of the Assigned Patents subject to any and all Existing Encumbrances, in writing enforceable by AMD and with a copy provided to AMD; and (c)AMD provides its written consent to the transfer, which shall not be unreasonably withheld.

3. DELIVERY AND POST-DELIVERY REQUIREMENTS

3.1 Executed Assignment and Confidentiality and Common Interest Agreement. On the Effective Date, AMD shall execute (i) an assignment (the "**Assignments**"), the form of which is attached hereto as Exhibit C, suitable for filing with the USPTO and other patent offices worldwide, and (ii) the Confidentiality and Common Interest Agreement, the form of which is attached hereto as Exhibit D. Lone Star shall promptly counter-sign and return the Confidentiality and Common Interest Agreement. The terms of the Confidentiality and Common Interest Agreement shall apply to the documents, files and information provided by AMD pursuant to Sections 2.4, 3.2 and 3.3 and the parties' discussions pursuant to Section 3.4 and any other similar provisions in this Agreement.

3.2 Delivery. Within sixty (60) days following the Effective Date, AMD shall, using reasonable commercial efforts, send via Federal Express or other reliable overnight and trackable delivery service, to Lone Star, the executed originals or certified copies of the Assignments along with all material, non-privileged files and documents in the possession of AMD regarding the Assigned Patents, which may include the following, to the extent available: (a) Letters Patents, (b) assignments for the Assigned Patents, (c) documents and materials evidencing dates of invention, including dates of conception and reduction to practice, (d) prosecution history files for all issued, pending or abandoned Assigned Patents, (e) a current electronic copy of a docketing report for the Assigned Patents accurately setting forth to the best of AMD's knowledge any and all dates relevant to the prosecution or maintenance of the Assigned Patents, including information relating to deadlines, payments and filings for the Assigned Patents, and the names, business addresses, email addresses, and phone numbers of all prosecution counsel and agents, and (f) any other material, non-privileged files and documents related to the Assigned Patents not otherwise provided under Section 3.2 in the possession of AMD. AMD shall, within sixty (60) days following the Effective Date, use reasonable efforts to transfer any material, privileged documents in the possession of AMD that directly and exclusively relate to an Assigned Patent. However, AMD shall not be obliged to transfer any privileged documents that relate to AMD's valuation or evaluation of the Assigned Patents (individually or collectively) or AMD's monetization options or plans for the Assigned Patents, such as privileged documents relating to the execution of this Agreement, the negotiations that

preceded this Agreement, and the activities pursuant to the statement of work previously executed by the parties. Notwithstanding anything else herein to the contrary, AMD shall only be obliged to transfer the files and documents that are: (i) actually in the possession of AMD, (ii) able to be located by AMD using reasonable diligence, and (iii) associated with the file of an Assigned Patent in the ordinary course of business.

3.3 Cooperation On and After Effective Date.

(a) On the Effective Date, AMD shall, if instructed by Lone Star, notify or cause to be notified, Lone Star in writing separate from any disclosures made hereunder, of any relevant due dates related to prosecution, filing, defense, enforcement or maintenance of the Assigned Patents that will occur within sixty (60) days after the Effective Date. AMD or its Affiliates shall pay, or cause to be paid, any maintenance fees, annuities and the like relating to the Assigned Patents for which the fee is due within sixty (60) days of the Effective Date; provided that Lone Star shall reimburse AMD for any such fees paid and AMD's and its Affiliates' reasonable out of pocket costs related to such activities. AMD further covenants and agrees that after the Effective Date, it shall, upon reasonable request and without further consideration, execute and deliver to Lone Star any other documents and materials, and take any reasonable further actions (including taking reasonable action to obtain the cooperation of the named inventors), that are reasonably necessary for Lone Star to perfect its title in the Assigned Patents.

(b) In addition, upon reasonable written request of Lone Star and with Lone Star reimbursing AMD's reasonable out-of-pocket cost and expense: (i) AMD shall take, or cause to be taken, reasonable actions to provide reasonable access to inventors and employees of AMD and relevant documents to assist Lone Star in the prosecution and maintenance of the Assigned Patents.

(c) The Parties shall cooperate in good faith in attempting to identify additional third-parties that the Parties may agree, at each's sole discretion, to add to the Exhibit E list of Unlicensed Third Party Entities.

3.4 Patent Non-Renewal. Should Lone Star decide not to pay the renewal, annuity, or maintenance fee on any Assigned Patent (an "**Abandoned Patent**"), Lone Star shall notify AMD of its decision, by written notice, no later than ninety (90) days prior to the time that any such renewal, annuity, or maintenance fee is due. In addition, Lone Star shall assign the Abandoned Patent to AMD or to a Person selected by AMD in AMD's sole discretion if requested by AMD before the due date of such renewal, annuity, or maintenance fee, and Lone Star shall, upon reasonable request, assist AMD and/or a transferee in making a payment to maintain the patent in force (which may include making the payment subject to timely reimbursement by the requestor).

4. LICENSE

4.1 License.

(a) Lone Star on behalf of itself and its present and future Affiliates and any successor or assign (collectively "**Grantor**") hereby grants to AMD and its present and future Affiliates and its and their successors and assigns (each as a "**Grantee**"), effective as of the Effective Date, a fully paid up, irrevocable, worldwide, transferable, non-exclusive, license under the Assigned Patents to use, develop, copy, modify, import, make and have made, offer for sale, sell, lease, import, export, distribute, demonstrate, display, transfer and/or otherwise exploit or dispose of a Grantee's Licensed Products. However, the license shall not extend to any future Affiliate of Grantee that was deemed an Unlicensed Third Party Entity prior to becoming so affiliated with Grantee.

(b) The license grant in Section 4.1(a) shall:

(i) continue to be retained by any Affiliate of AMD as of the Effective Date (and their successors and assigns) even if such Affiliate of AMD (and its successors and assigns), subsequent to the Effective Date, is no longer an Affiliate of AMD (including following any further changes in the Person Controlling such Affiliate) (**"Former Affiliate"**); and

(ii) continue to apply to sales of an asset of AMD and AMD's Affiliates (and its and their successors and assigns) by an acquiring third party of such asset in the event that all rights, title and interest in such asset is sold, transferred or otherwise disposed of by AMD or AMD's Affiliate (and its and their successors and assigns), as applicable (including, without limitation, the sale of a business unit or division of AMD or AMD's Affiliates or a sale of the technology associated with a Licensed Product) (**"Former Asset"**); provided, however, that the license grant in Section 4.1(a) shall apply only for as long as such Former Asset is maintained by such acquiring third party in a manner capable of being independently audited. Notwithstanding the foregoing, the license grant in Section 4.1(a) shall not apply to any assets, software, technology, products or services of the third party (or Affiliates of such third party) that Controls such Former Asset.

(c) Nothing in Section 4.1(b) shall in any way limit, diminish or otherwise impact the license granted under Section 4.1(a) to AMD's present or future Affiliates that remain Affiliates of AMD after the transactions contemplated in Section 4.1(b).

(d) For clarity, the license granted in Section 4 shall extend to the joint venture between AMD and Nantong Fujitsu Microelectronics Co., Ltd. that was formed with the assets of AMD Technologies (China) Co. Ltd. and Advanced Micro Devices Export Sdn. Bhd The agreements forming this joint venture were publically announced by AMD on October 15, 2015.

4.2 Combinations. Without limiting the rights granted hereunder, the licenses granted in Section 4.1 extend to the supply by each Grantee of a Licensed Product that is combined with or intended to be combined with products and services of third parties (and any subsequent sale, offer to sell, importation, exportation, distribution, use, and/or other exploitation of the Licensed Product by those third parties) but only to the extent that:

(a) in the absence of such a license, AMD or any of its Affiliates would be obligated to indemnify such third parties for the use of a Licensed Product that is combined with or intended to be combined with the products or services of such third parties; or

(b) in the absence of such a license, the Grantee's Licensed Product (alone or when combined with the products or services of a third party) would directly or indirectly infringe any of the Assigned Patents.

4.3 Sub-license rights. During the period from the Effective Date until six years following the date of expiration of the last to expire of the Assigned Patents, in the event that Grantor is in breach of section 6.2(f), Grantor hereby grants to Grantee and its present and future Affiliates and its and their successors and assigns, effective as of the Effective Date, a fully paid up, irrevocable, worldwide, transferable, non-exclusive, sublicensable right, sublicensable only to the one or more Persons that are (i) not Unlicensed Third Party Entities, and (ii) which were subjected to an assertion or legal action which resulted in said breach (the "Selected Third Party Entities"), under the Assigned Patents to use, develop, copy, modify, import, make and have made, offer for sale, sell, lease, import, export, distribute, demonstrate, display, transfer and/or otherwise exploit or dispose of the past, present and future products and/or services of the one or more Selected Third Party Entities.

4.4 Covenant Not To Sue. During the period from the Effective Date until six years following the date of expiration of the last to expire of the Assigned Patents, Grantors hereby covenant not to sue, assert, or seek damages, injunctive relief or other remedies for any claims, and covenant to forbid any third party assignee, transferee or delegate of any right, title and/or interest of any intellectual property claim of Grantors from pursuing any of the same, from Grantees, suppliers, distributors and resellers of Grantees, and direct and indirect customers of Grantees, for infringement (whether direct, contributory, by inducement or otherwise) of the Assigned Patents based on the manufacture, sale, offer for sale, lease, importation, export, distribution, display, demonstration, copying, modification, transfer, or use or exploitation of materials, devices, software or firmware, services and products that are used, made or supplied directly or indirectly by or for Grantees. The foregoing covenant shall not constitute a general license, release or covenant to any customer of Grantees and shall apply to a customer only with respect to those materials, software or firmware, services, products and devices originating from or designed by or for Grantees.

4.5 Reservation of Rights. All rights not expressly granted in this Agreement are reserved. No additional rights whatsoever (including any implied licenses) are granted by implication, exhaustion, estoppel or otherwise.

5. PAYMENT TERMS

5.1 Contingent Payments. For any Proceeds received on a given date AMD shall receive:

(a) Thirty-five percent (35%) of such Proceeds if aggregate Proceeds received from all monetization efforts related to the Assigned Patents are less than fifty million U.S. dollars (US$50,000,000.00); and

(b) Fifty percent (50%) of such Proceeds if aggregate Proceeds received from all monetization efforts related to the Assigned patents are equal to or in excess of fifty million U.S. dollars (US$50,000,000.00) (collectively the "Back-end Proceeds").

Lone Star shall require in its retainer agreement with Law Firm, and in all agreements with third-parties pursued under the Assigned Patents, that all Proceeds be received in the first instance by Law Firm. The retainer agreement shall further require that Law Firm shall be responsible to distribute the amount payable to AMD under 5.1(a) – (b), if any, to AMD within forty-five (45) days of actual receipt of Proceeds, with payment made by wire transfer to AMD's bank account provided by AMD in accordance with Section 5.2.

5.2 Amounts Payable by Lone Star to AMD. Back-end Proceeds payable by Lone Star (via Law Firm) to AMD under this Agreement shall be paid in United States dollars without accounting for any withholding, deduction or any other payment of any taxes, duties, levies, fees (contingent or otherwise), excises or tariffs imposed on any of Lone Star's activities in connection with the Assigned Patents. Any payments to AMD shall be made by wire transfer to:

ACCOUNT NAME BENEFICIARY: ADVANCED MICRO DEVICES, INC.

5.3 If the Parties cannot agree on the express dollar value at the time of settlement of any non-cash component included in the Proceeds, the Parties agree to retain the services of a mutually agreeable

accounting or appraisal individual or firm, which will assign a value determined by such person or firm to such item, thing, or agreement for purposes of determining the present cash value of the Proceeds.

5.4 To ensure compliance with the payment terms under this Section 5, Lone Star hereby pledges and grants to the AMD a lien on, and security interest in, and to all of its right, title and interest in, to and under all the Assigned Patents and execute the Security Interest Agreement of Exhibit G attached hereto. Lone Star agrees to provide any documents, information and assistance necessary to enable AMD to register its security interest against the title of the Assigned Patents in the patent office relevant to Assigned Patents.

(a) In the event of the sale, transfer or other disposition of one or more of the Assigned Patents, Lone Star shall request in writing the release of AMD's lien on, and security interest in, and to all of its right, title and interest of the one or more Assigned Patents. Within sixty (60) days of receipt of such written notice from Lone Star requesting the release, then AMD shall be obligated to provide such release of the lien on, and security interest in, and to all of its right, title and interest of the one or more Assigned Patents provided that Lone Star and Law Firm have provided timely access (and no later than fifteen (15) days after transmission of its written request) to all necessary financial records related to the Proceeds sufficient for AMD to reasonably determine that all Back-end Proceeds payable to AMD hereunder have been paid to AMD. AMD shall not be obligated to provide any release under this Section 5.4 if Back-end Proceeds are owed to AMD or if AMD disputes with Lone Star the amounts of Back-end Proceeds payable to AMD.

6. REPRESENTATIONS AND WARRANTIES

6.1 Except as set forth in the applicable section of the attached schedules setting forth specific exceptions to AMD's representations and warranties below (the "**Disclosure Schedule**"), and in any other section of the Disclosure Schedule to the extent the relevance thereto is reasonably apparent from such disclosure, AMD represents and warrants to Lone Star as of the Effective Date (except for such representations and warranties made only as of a specific date) that each of the statements in this Section 6.1 is true and correct. For purposes of this Section 6.1, "**Knowledge**" means the actual knowledge of any of its officers and the members of its IP Law Group formed after a reasonable investigation of AMD's records as kept in the ordinary course of business.

(a) Authority; Enforceability.

(i) AMD is validly existing and in good standing under the laws of the jurisdiction of its incorporation or formation, as the case may be. AMD has the right and authority to enter into this Agreement and to carry out its obligations hereunder and requires no third party consent, approval, and/or other authorization to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Listed Patents to Lone Star. This Agreement has been duly authorized, executed and delivered by AMD and constitutes a valid and binding agreement of AMD, enforceable against AMD in accordance with its terms, subject to bankruptcy, insolvency, fraudulent transfer, reorganization, moratorium and similar laws of general applicability relating to or affecting creditors' rights and to general equity principles.

(ii) The execution and delivery of this Agreement and the performance by AMD of its obligations hereunder do not and will not violate any provision of the organizational documents of AMD and will not result in a breach of the terms, conditions or provisions of, or constitute a default under any contract, instrument, order, judgment or decree to which AMD is subject.

(b) Title and Contest.

(i) To AMD's Knowledge, AMD or one of its Affiliates has been assigned good and marketable title to each Listed Patent it is assigning hereunder, including all rights, title, and interest in each such Listed Patent and the right to sue for past, present and future infringement thereof.

(ii) To AMD's Knowledge, AMD or one of its Affiliates is the original assignee of the Listed Patents. To AMD's Knowledge, AMD has obtained previously executed assignments for each Listed Patent it is assigning hereunder, and either already has or will properly record or cooperate to have the same recorded with the USPTO or any other appropriate US or foreign country as necessary to perfect AMD's rights and title therein in accordance with or as permitted by the governing law and regulations in each respective jurisdiction.

(iii) Except as set forth in Section 6.1(b)(iii) of the Disclosure Schedule, to AMD's Knowledge, neither AMD nor its Affiliates has created or permitted the creation of any liens, mortgages, security interests, or other encumbrances on title, or restrictions on transfer on the Listed Patents, in each case, which exist as of the Effective Date. AMD is not party to any existing contracts, agreements, options, commitments, or rights with, to, or in any person to acquire any of the Listed Patents.

(iv) To AMD's knowledge, none of the Listed Patents have been found invalid or unenforceable for any reason in any administrative, arbitration, or judicial proceeding. To AMD's Knowledge, there is no litigation, opposition, cancellation, proceeding, objection or claim pending, asserted or threatened against AMD concerning the Listed Patents.

(v) Except as set forth in Section 6.1(b)(v) of the Disclosure Schedule, to AMD's Knowledge, neither AMD nor its Affiliates has initiated any enforcement action with respect to any of the Listed Patents.

(vi) Except as set forth in Section 6.1(b)(vi) of the Disclosure Schedule, to AMD's Knowledge none of the Listed Patents is subject to any exclusive grant or right.

(vii) To AMD's knowledge, none of the Unlicensed Third Party Entities have been granted any rights (other than potentially through agreements referenced in Exhibit E, an implied license or through AMD's or its Affiliates' standardization activities (or activities related to specifications that are intended to be widely adopted and/or promulgated) (collectively "Standards"), and other pre-existing specification-related or Standards-related licenses, covenants and promises of AMD or any of its Affiliates) by AMD or its Affiliates to the Assigned Patents to use, develop, copy, modify, import, make and have made, offer for sale, sell, lease, import, export, distribute, demonstrate, display, transfer and/or otherwise exploit or dispose of a product or service by the Unlicensed Third Party.

(c) Litigation. Except as set forth in Section 6.1(c) of the Disclosure Schedule, AMD is not presently subject to any injunction, order or other decree of any Governmental Authority related to the Listed Patents or the transactions contemplated hereby.

6.2 Lone Star. Lone Star hereby represents and warrants to AMD that:

(a) Lone Star has been duly organized, and is validly existing and in good standing under the laws of the jurisdiction of its incorporation or formation, as the case may be.

(b) Lone Star has the right and authority to enter into this Agreement and to carry out its obligations hereunder and requires no third party consent, approval, and/or other authorization to enter

into this Agreement and to carry out its obligations hereunder. This Agreement has been duly authorized, executed and delivered by Lone Star and constitutes a valid and binding agreement of such party, enforceable against such party in accordance with its terms, subject to bankruptcy, insolvency, fraudulent transfer, reorganization, moratorium and similar laws of general applicability relating to or affecting creditors' rights and to general equity principles.

(c) The execution and delivery of this Agreement and the performance by Lone Star of its obligations hereunder do not and will not conflict with, or violate any provision of, the organizational documents of Lone Star and will not conflict with or result in a breach of the terms, conditions or provisions of, or constitute a default under any contract, instrument, order, judgment or decree to which Lone Star is subject.

(d) Lone Star has conducted an independent review of the Listed Patents and its advisors have had the opportunity to request access to any materials (including, but not limited to any, to requesting materials on any Existing Encumbrances and any other relevant materials) related to the Listed Patents and have had an opportunity to request an opportunity to meet (in person or electronically) with appropriate AMD personnel to discuss the Listed Patents, any Existing Encumbrances and any other relevant materials.

(e) Lone Star will maintain all patents in force, unless Lone Star provides the notification to AMD required by Section 3.4, Lone Star will not purport to transfer any Assigned Patent unless such transfer is made in compliance with Section 2.6.

(f) Lone Star acknowledges that the Assigned Patents are subject to Existing Encumbrances to other Persons and that Lone Star represents and warrants that it shall not commence, direct or control any legal action seeking to enforce and/or licensing activity asserting any of the Assigned Patents against a Person that is (1) not an Unlicensed Third Party Entity or Affiliate thereof, or (2) is a distributor, reseller, or direct or indirect customer with respect to materials, devices, software or firmware, services or products that are used, made or supplied directly or indirectly by or for a Person that is not an Unlicensed Third Party Entity.

6.3 Provisions for Breach.

(a) Breach by AMD. The Parties agree that if there is a breach of a representation and warranty as to a particular Assigned Patent (the "**Breaching Patent**") by AMD then the exclusive remedy for such breach shall be that AMD will transfer –one or more Replacement Patents (defined below) to Lone Star. The "**Replacement Patents**" shall include a Selected Patent (defined below) and, to the extent owned by AMD, any divisionals, provisionals, re-exams, continuations, continuations-in-part, extensions or reissues of the Selected Patent, any applications for the foregoing in all countries of the world, and any other procedure or formality with respect to the aforesaid that can result in an enforceable patent right anywhere in the world. The "**Selected Patent**" shall be a U.S. patent selected by AMD in its sole discretion for which all of the following is true: (1) the Selected Patent is wholly owned by AMD, (2) the Selected Patent has not been claim charted by AMD, as evidenced by AMD's written records, (3) the Selected Patent has not been asserted by AMD against any entity, as evidenced by AMD's written records, and (4) the Replacement Patent was selected by AMD from one or more lists of patents provided to AMD by Lone Star.

(b) Breach by Lone Star. The parties agree that if there is a breach of a representation and warranty by Lone Star of:

(i) Section 6.2(f), then the sublicense rights described in Section 4.3 hereby immediately vest in AMD with respect to the patents asserted in violation of Section 6.2(f).

(ii) Section 5, then AMD shall be entitled to recover its reasonable attorney's fees incurred to enforce its right to the Back-end Proceeds.

7. MISCELLANEOUS

7.1 Applicable Law. The validity, construction, and performance of this Agreement shall be governed by and construed first in accordance with the federal laws of the United States to the extent federal subject matter jurisdiction exists, and second in accordance with the laws of the State of California, exclusive of its choice of law rules. With respect to all civil actions or other legal or equitable proceedings directly arising between the parties or any of their affiliates under this Agreement, the parties consent to exclusive jurisdiction and venue in the United States District Court for the Northern District of California located in Santa Clara County (the "**Forum**") unless no federal jurisdiction exists, in which case the parties consent to exclusive jurisdiction and venue in a state court of California located in Santa Clara County (the "**Alternate Forum**"). Each party irrevocably consents to personal jurisdiction and waives the defense of forum non conveniens in the Forum, or Alternate Forum, if applicable, with respect to itself and its Affiliates. Process may be served on either party in the manner authorized by applicable law or court rule.

7.2 LIMITATION ON CONSEQUENTIAL DAMAGES. EXCEPT IN THE CASE OF FRAUD OR BREACH OF SECTION 7.6 (CONFIDENTIALITY), NO PARTY SHALL BE LIABLE TO ANY OTHER FOR ANY SPECIAL, CONSEQUENTIAL OR INCIDENTAL DAMAGES, HOWEVER CAUSED, KNOWN OR UNKNOWN, ANTICIPATED OR UNANTICIPATED, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE PARTIES ACKNOWLEDGE THAT THESE LIMITATIONS ON POTENTIAL DAMAGES WERE AN ESSENTIAL ELEMENT IN SETTING CONSIDERATION UNDER THIS AGREEMENT.

7.3 LIMITATION OF LIABILITY. EXCEPT IN THE CASE OF FRAUD OR BREACH OF SECTION 4 (LICENSE), SECTION 5 (PAYMENT TERMS), SECTION 6 (WARRANTIES), OR SECTION 7.6 (CONFIDENTIALITY), WITHOUT WAIVING ANY OTHER RIGHTS OF THE PARTIES, INCLUDING ANY RIGHT TO SEEK SPECIFIC PERFORMANCE OR SEEK OTHER EQUITABLE RELIEF, NO PARTY'S TOTAL LIABILITY (EXCLUDING PAYMENT OBLIGATIONS) UNDER THIS AGREEMENT SHALL EXCEED TEN THOUSAND US DOLLARS ($10,000.00). FURTHER, WITH RESPECT TO ANY BREACH BY AMD OF SECTION 6.1(b)(i) OR 6.1(b)(ii) DISCOVERED MORE THAN TWO YEARS AFTER THE EFFECTIVE DATE, AMD SHALL BE OBLIGED TO USE BEST EFFORTS TO CURE THE BREACH, BUT AMD'S TOTAL LIABILITY SHALL NOT EXCEED TEN THOUSAND US DOLLARS ($10,000.00). THE PARTIES ACKNOWLEDGE THAT THESE LIMITATIONS ON POTENTIAL LIABILITIES WERE AN ESSENTIAL ELEMENT IN SETTING CONSIDERATION UNDER THIS AGREEMENT.

7.4 DISCLAIMER OF REPRESENTATIONS AND WARRANTIES. NO PARTY MAKES ANY REPRESENTATION OR WARRANTY EXCEPT FOR THEIR RESPECTIVE REPRESENTATIONS AND WARRANTIES SET FORTH IN SECTION 6, AND EACH PARTY DISCLAIMS ALL IMPLIED WARRANTIES, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. EXCEPT AS EXPRESSLY SET FORTH IN SECTION 6 HEREOF, NEITHER PARTY GIVES THE OTHER PARTY ANY ASSURANCE (A) REGARDING THE PATENTABILITY OF ANY CLAIMED INVENTION IN, OR THE VALIDITY, PATENTABILITY, SCOPE, COVERAGE OR ENFORCEABILITY OF ANY PATENT OR (B) THAT MANUFACTURE, USE, SALE, OFFERING FOR SALE, IMPORTATION, EXPORTATION OR

OTHER DISTRIBUTION OF ANY PRODUCT OR METHOD DISCLOSED AND CLAIMED IN ANY PATENT SHALL NOT CONSTITUTE AN INFRINGEMENT OF THE INTELLECTUAL PROPERTY RIGHTS OF OTHER PERSONS. EXCEPT AS SPECIFICALLY PROVIDED IN SECTION 6 HEREOF, THE ASSIGNED PATENTS ARE ASSIGNED ON AN "AS IS" BASIS WITHOUT ANY FURTHER EXPRESS OR IMPLIED REPRESENTATION OR WARRANTY.

7.5 Compliance with Laws. Notwithstanding anything contained in this Agreement to the contrary, the obligations of the parties shall be subject to all laws, present and future, of any government having jurisdiction over the parties and this transaction, and to orders, regulations, directions or requests of any such government.

7.6 Confidentiality of Terms. All terms and conditions in this Agreement and all communications and transactions between the parties and their respective Affiliates related thereto, including without limitation, those made in connection with this Agreement under Section 3.3, shall be kept in confidence by the parties and their respective Affiliates. The parties shall not now or hereafter divulge this Agreement or any of its terms to any third party except: (a) with the prior written consent of the other party; (b) to any Governmental Authority having jurisdiction to require disclosure, or to any arbitral body, to the extent legally compelled by same; (c) as otherwise may be required by law or legal process, including to legal and financial advisors that are bound by a written obligation to maintain such information confidential that is at least as protective as the terms of this Section, in their capacity of advising a party in such matters; (d) during the course of litigation, so long as the disclosure of such terms and conditions are restricted in the same manner as is the highly confidential information of other litigating parties; (e) to the extent reasonably necessary, to accountants, banks, and financing sources, current and future providers of capital, investors, potential acquirors and current and future financing sources and their advisors that are bound by a written or professional obligation to maintain such information confidential that is at least as protective as the terms of this Section, solely in connection with or compliance with an acquisition or financing transactions and any applicable reporting obligations; or (f) while obtaining legal advice from legal counsel as needed in the normal course of business; provided that, in (b) through (e) above, the parties shall use all legitimate and legal means available to minimize the disclosure to third parties, including seeking a confidential treatment request or protective order whenever available. The Confidentiality and Common Interest Agreement shall govern the treatment of all other confidential and/or privileged information provided pursuant to this Agreement.

7.7 Sensitive Information. The parties agree that this Agreement may contain competitively sensitive information, the public disclosure of which would be competitively harmful. The parties agree that each party shall notify the other parties prior to filing the Agreement as an exhibit to any registration statement or periodic report filed with the United States Securities and Exchange Commission or any counterpart under any foreign jurisdiction (a "**Securities Regulator**") and cooperate with the non-filing party, in jointly identifying provisions which the filing party would redact and/or request that they receive confidential treatment in connection with any such filing. The redaction and/or request for confidential treatment shall be made in a manner consistent with applicable Securities Regulator's regulations and guidance. The request shall seek the longest confidentiality term possible. Any confidentiality request shall be submitted to and subject to the non-filing parties' reasonable approval in advance of filing.

7.8 Publicity. No party shall issue any press release or make other public statements with respect to the transactions contemplated by this Agreement or identifying the other party by name without the prior written consent of the other party, except as otherwise permitted by Sections 7.6 or 7.7 or except with respect to disclosures that are consistent with prior disclosures made in compliance with this Section 7.8.

7.9 Termination. The following sections shall survive any termination of this Agreement: Sections 1, 2.3, 4, 5, 6, and 7.

7.10 Entire Agreement; Headings. This Agreement reflects the complete understanding of the parties regarding the subject of the Agreement, and supersedes all prior related negotiations. The section headings contained in this Agreement are for reference purposes only and shall not affect in any way the meaning or interpretation of this Agreement.

7.11 Notices. Any notice under this Agreement shall be effective upon receipt when made in writing and delivered to the other party at the address stated below. Notice by email or facsimile is effective upon receipt if an original signature copy is mailed contemporaneously to the other party at the address stated below:

For AMD:
Advanced Micro Devices, Inc.
7171 Southwest Pkwy, M/S B100.T
Austin, TX 78735 USA
Attn: General Counsel
Facsimile: 1-512-602-1252
E-mail: kevin.oneil@amd.com

For Lone Star:
Lone Star Silicon Innovations LLC
5204 Bluewater Drive, Frisco, TX 75034
Attn: Khaled Fekih-Romdhane, Managing Partner
E-mail: khaled@longhornip.com

7.12 Relationship of Parties. The parties hereto are independent contractors. No party has any express or implied right or authority under this Agreement to assume or create any obligations on behalf of any other party or to bind the other to any contract, agreement or undertaking with any third party. Nothing in this Agreement shall be construed to create a partnership, joint venture, employment or agency relationship between the parties hereto or any beneficiaries hereof.

7.13 Severability. To the extent any terms or conditions of this Agreement are held invalid or unenforceable in a jurisdiction, those terms or conditions shall be enforced to the maximum extent possible in that jurisdiction and the remaining terms and conditions shall retain full force and effect in that jurisdiction, so long as the remaining Agreement continues to express the intent of the parties.

7.14 Waiver. Failure by any party to enforce any term of this Agreement shall not be deemed a waiver of future enforcement of that or any other term in this Agreement.

7.15 Successors; Assignment. AMD and its Affiliates may assign their respective rights in this Agreement to their respective successors in interest. Lone Star may only assign this Agreement with a transfer of all of the Assigned Patents, as provided by Section 2.6.

7.16 Modifications. This Agreement may not be modified after the Effective Date except by a written amendment that expressly references this Agreement and that is signed by an authorized officer of each party.

7.17 Construction. As used in this Agreement, (a) the words "include" and "including" and variations

thereof, shall not be deemed to be terms of limitation, but rather shall be deemed to be followed by the words "without limitation," and (b) unless the context otherwise requires, the word "or" shall be deemed to be an inclusive "or" and shall have the meaning equivalent to "and/or."

7.18 Specific Performance. The parties agree that irreparable damage may occur in the event that any party fails to comply with this Agreement in accordance with its terms and that the parties shall be entitled to seek specific performance in such event, in addition to any other remedy at law or in equity. The parties agree that, in the event of any breach or threatened breach by another party of any covenant or obligation contained in this Agreement, the non-breaching party shall be entitled to seek (a) a decree or order of specific performance to enforce the observance and performance of such covenant or obligation, and (b) an injunction restraining such breach or threatened breach. The parties further agree that no party or any other Person shall be required to obtain, furnish or post any bond or similar instrument in connection with or as a condition to obtaining any remedy referred to in this Section 7.18, and the parties irrevocably waive any rights they may have to require the obtaining, furnishing or posting of any such bond or similar instrument. The remedies available to the parties pursuant to this Section 7.18 shall be in addition to any other remedy to which such parties are entitled at law or in equity, and the election to pursue an injunction or specific performance shall not restrict, impair or otherwise limit such parties from recovery of monetary damages.

7.19 Signatures. This Agreement may be executed in counterparts, each of which shall be deemed an original, but each together shall constitute one and the same instrument. For purposes hereof, an email or facsimile copy of this Agreement, including the executed signature pages hereto, shall be deemed to be an original. Notwithstanding the foregoing, the parties shall deliver original signature copies of this Agreement to each other party as soon as practicable following execution thereof.

IN WITNESS WHEREOF, the parties have executed this Patent Purchase Agreement as of the Effective Date:

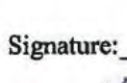
Lone Star Silicon Innovations LLC	ADVANCED MICRO DEVICES, INC.
Signature: 	Signature: 
Name: Christian Dubuc	Name: Kevin O'Neil
Title: Managing Partner	Title: VP - IP & Licensing
Date: August 4, 2016	Date: August 4, 2016

Exhibit A

LISTED PATENTS

Family	Title	Patent No.
1	Semiconductor device having an elevated active region formed in an oxide trench	US6104069
1	Semiconductor device having an elevated active region formed in an oxide trench and method of manufacture thereof	US5872038
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US5956610
2	Local interconnects for improved alignment tolerance and size reduction	US6121663
2	Methods and arrangements for insulating local interconnects for improved alignment tolerance and size reduction	US6399480
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US6303949
3	Run to run control process for controlling critical dimensions	USRE39518
3	Run-to-run control process for controlling critical dimensions	US5926690
4	Method of forming a contact hole in an interlevel dielectric layer using dual etch stops	US5912188
5	Elimination of residual materials in a multiple-layer interconnect structure	US6153933
6	Method and system for providing an interconnect having reduced failure rates due to voids	US6010960
7	Method of making gate dielectric for sub-half micron mos transistors including a graded dielectric constant	US6015739
8	Silicided shallow junction transistor formation and structure with high and low breakdown voltages	US5973372
9	Dual damascene process using sacrificial spin-on materials	US6057239
9	Dual damascene process using sacrificial spin-on materials	US6424039
10	Borderless vias	US5925932
10	High integrity vias	US6097090
10	Borderless vias	US6232221
11	Core cell structure and corresponding process for nand-type high performance flash memory device	US6023085
11	Core cell structure and corresponding process for nand type performance flash memory device	US6372577
12	Methods and arrangements for improved spacer formation within a semiconductor device	US6103611
12	Semiconductor device having uniform spacers	US6380588
13	Semiconductor device having dual gate electrode material and process of fabrication thereof	US6043157
14	Selectively sized spacers	US6046089
15	Trenched gate metal oxide semiconductor device and method	US6097061
15	Trenched gate metal oxide semiconductor device and method	US6667227
16	Integrated circuit having an interlevel interconnect coupled to a source/drain region(s) with source/drain region(s) boundary overlap and reduced parasitic capacitance	US6146978

Family	Title	Patent No.
17	Ultrathin, nitrogen-containing mosfet sidewall spacers using low-temperature semiconductor fabrication process	US6323519
18	Use of silicon oxynitride arc for metal layers	US6326231
19	Semiconductor package with supported overhanging upper die	US6337226
20	Low dielectric constant etch stop layers in integrated circuit interconnects	US6388330

Exhibit B

ASSIGNED PATENTS

Family	Title	Patent No.
1	Semiconductor device having an elevated active region formed in an oxide trench	US6104069
1	Semiconductor device having an elevated active region formed in an oxide trench and method of manufacture thereof	US5872038
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US5956610
2	Local interconnects for improved alignment tolerance and size reduction	US6121663
2	Methods and arrangements for insulating local interconnects for improved alignment tolerance and size reduction	US6399480
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US6303949
3	Run to run control process for controlling critical dimensions	USRE39518
3	Run-to-run control process for controlling critical dimensions	US5926690
4	Method of forming a contact hole in an interlevel dielectric layer using dual etch stops	US5912188
5	Elimination of residual materials in a multiple-layer interconnect structure	US6153933
6	Method and system for providing an interconnect having reduced failure rates due to voids	US6010960
7	Method of making gate dielectric for sub-half micron mos transistors including a graded dielectric constant	US6015739
8	Silicided shallow junction transistor formation and structure with high and low breakdown voltages	US5973372
9	Dual damascene process using sacrificial spin-on materials	US6057239
9	Dual damascene process using sacrificial spin-on materials	US6424039
10	Borderless vias	US5925932
10	High integrity vias	US6097090
10	Borderless vias	US6232221
11	Core cell structure and corresponding process for nand-type high performance flash memory device	US6023085
11	Core cell structure and corresponding process for nand type performance flash memory device	US6372577
12	Methods and arrangements for improved spacer formation within a semiconductor device	US6103611
12	Semiconductor device having uniform spacers	US6380588
13	Semiconductor device having dual gate electrode material and process of fabrication thereof	US6043157
14	Selectively sized spacers	US6046089
15	Trenched gate metal oxide semiconductor device and method	US6097061
15	Trenched gate metal oxide semiconductor device and method	US6667227
16	Integrated circuit having an interlevel interconnect coupled to a source/drain region(s) with source/drain region(s) boundary overlap and reduced parasitic capacitance	US6146978

Family	Title	Patent No.
17	Ultrathin, nitrogen-containing mosfet sidewall spacers using low-temperature semiconductor fabrication process	US6323519
18	Use of silicon oxynitride arc for metal layers	US6326231
19	Semiconductor package with supported overhanging upper die	US6337226
20	Low dielectric constant etch stop layers in integrated circuit interconnects	US6388330

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at MARKHAM, ON on AUGUST 4, 2016.

ASSIGNOR

By: _____

Name: KEVIN ONEIL

Title: VP - IP & LICENSING

(Signature must be notarized)

_____

Before me, LINDA LAM

Notary Public at PROVINCE OF ONTARIO

Date: August 4, 2016

IN TESTIMONY WHEREOF, in accepting said Assignment, I hereunto set my hand as of the date indicated below:

Lone Star Silicon Innovations LLC

AUG 4, 2016
Date

_____
Signature

Name: CHRISTIAN DUBLE
Title: MANAGING PARTNER

(Signature must be notarized)

MICHAEL LEE
Notary Public, State of Texas
My Commission Expires
July 22, 2018

_____

Before me, Michael Lee

Notary Public at Allen, TEXAS

Date: August 4, 2016

Exhibit C

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, Advanced Micro Devices, Inc., a Delaware corporation, with a registered address at One AMD Place, Sunnyvale, CA 94088-3453 USA ("**Assignor**"), does hereby assign, transfer and convey unto Lone Star Silicon Innovations LLC, an entity organized under the laws of Texas having its primary place of business at 5204 Bluewater Drive, Frisco, TX 75034 ("**Assignee**"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Exhibit 1 (collectively "**Patent Rights**"), subject to the terms and conditions of the Confidential Purchase and Sale Agreement (the "**Agreement**"). Assignor and Assignee acknowledge that some of the Patent Rights may be currently expired or abandoned.

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successor and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

Exhibit 1

Family	Title	Patent No.
1	Semiconductor device having an elevated active region formed in an oxide trench	US6104069
1	Semiconductor device having an elevated active region formed in an oxide trench and method of manufacture thereof	US5872038
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US5956610
2	Local interconnects for improved alignment tolerance and size reduction	US6121663
2	Methods and arrangements for insulating local interconnects for improved alignment tolerance and size reduction	US6399480
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US6303949
3	Run to run control process for controlling critical dimensions	USRE39518
3	Run-to-run control process for controlling critical dimensions	US5926690
4	Method of forming a contact hole in an interlevel dielectric layer using dual etch stops	US5912188
5	Elimination of residual materials in a multiple-layer interconnect structure	US6153933
6	Method and system for providing an interconnect having reduced failure rates due to voids	US6010960
7	Method of making gate dielectric for sub-half micron mos transistors including a graded dielectric constant	US6015739
8	Silicided shallow junction transistor formation and structure with high and low breakdown voltages	US5973372
9	Dual damascene process using sacrificial spin-on materials	US6057239
9	Dual damascene process using sacrificial spin-on materials	US6424039
10	Borderless vias	US5925932
10	High integrity vias	US6097090
10	Borderless vias	US6232221
11	Core cell structure and corresponding process for nand-type high performance flash memory device	US6023085
11	Core cell structure and corresponding process for nand type performance flash memory device	US6372577
12	Methods and arrangements for improved spacer formation within a semiconductor device	US6103611
12	Semiconductor device having uniform spacers	US6380588
13	Semiconductor device having dual gate electrode material and process of fabrication thereof	US6043157
14	Selectively sized spacers	US6046089
15	Trenched gate metal oxide semiconductor device and method	US6097061
15	Trenched gate metal oxide semiconductor device and method	US6667227
16	Integrated circuit having an interlevel interconnect coupled to a source/drain region(s) with source/drain region(s) boundary overlap and reduced parasitic capacitance	US6146978

Family	Title	Patent No.
17	Ultrathin, nitrogen-containing mosfet sidewall spacers using low-temperature semiconductor fabrication process	US6323519
18	Use of silicon oxynitride arc for metal layers	US6326231
19	Semiconductor package with supported overhanging upper die	US6337226
20	Low dielectric constant etch stop layers in integrated circuit interconnects	US6388330

Exhibit D

CONFIDENTIALITY AND COMMON INTEREST AGREEMENT

THIS CONFIDENTIALITY AND COMMON INTEREST AGREEMENT ("**Agreement**") is entered into between the undersigned parties.

1. Background.

1.1 Lone Star Silicon Innovations LLC, an entity organized under the laws of Texas having its primary place of business at 5204 Bluewater Drive, Frisco, TX 75034 ("**Purchaser**") and Advanced Micro Devices, Inc., a Delaware company ("**Seller**") (Purchaser and Seller are sometimes hereafter referred to herein as a "**party**" or the "**parties**"), have entered into a Patent Transfer Agreement ("**PPA**") under which Purchaser will acquire all substantial rights of Seller in certain patents and patent applications filed or to be filed throughout the world (the "**Patent Matters**").

1.2 The parties have agreed to exchange privileged and/or confidential information related to the Patent Matters and enforcement thereof. Confidential information includes all non-public information exchanged between the parties that relates to the Patent Matters and that is (a) marked "confidential" or with a similar legend; (b) disclosed in any other manner and identified as confidential at the time of disclosure; (c) accessed through any web based or electronic portal; and/or (d) learned as a result of a visit to a party's facilities.

1.3 The parties have a common interest in the Patent Matters and have agreed to treat their communications and those of their counsel relating to the Patent Matters as protected by the common interest privilege. Furtherance of the Patent Matters requires the exchange of proprietary documents and information, the joint development of legal strategies and the exchange of attorney work product developed by the parties and their respective counsel.

2. Common Interest.

2.1 The parties have a common, joint and mutual legal interest in cooperating with each other, to the extent permitted by law, to share information protected by the attorney-client privilege and by the work product doctrine with respect to the Patent Matters. Any counsel or consultant retained by a party or their counsel to assist in the Patent Matters shall be bound by, and entitled to the benefits of, this Agreement.

2.2 In order to further their common interest, the parties (and their counsel, on behalf of each party) may exchange confidential information and/or privileged and work product information, orally and in writing, including, without limitation, factual analyses, mental impressions, legal memoranda, source materials, draft legal documents, prosecution history files and other information (hereinafter "**Protected Materials**"). It is the mutual understanding of the Parties that the exchange of privileged or otherwise protected Protected Materials is not intended to enhance, diminish, or waive in any way the privileged or otherwise protected status of that information. The Parties also intend and understand that any exchange or discussion among themselves regarding such privileged Protected Materials will not constitute a waiver of any applicable privilege, immunity, or other protection.

2.3 The sole purpose for the exchange of the Protected Materials is to support the parties' common interest with respect to the prosecution and enforcement of the Patent Matters, and the parties may only use Protected Materials to further this purpose. Any Protected Materials exchanged shall continue to be protected under all applicable privileges and no such exchange shall constitute a waiver of any applicable privilege or protection.

3. Confidentiality & Nondisclosure.

3.1 The parties and their Counsel shall use the Protected Materials solely in connection with the Patent Matters and shall take appropriate steps to protect the privileged and confidential nature of the Protected Materials.

3.2 A party receiving Protected Materials ("**Recipient**") from the other party ("**Discloser**") shall protect such Protected Materials by using the same degree of care, but no less than a reasonable degree of care, to prevent the unauthorized use, dissemination or publication of the Protected Materials as Recipient uses to protect its own information of a like nature. Recipient shall not disclose any Protected Materials disclosed hereunder to any third party, and Recipient shall limit disclosure of Protected Materials to only those of its employees and contractors with a need to know and who are bound by confidentiality obligations with Recipient at least as restrictive as those contained in this Agreement. Each party shall be responsible for its employees', contractors', and counsel's adherence to the terms of this Agreement. Further, Recipient shall not reverse engineer, disassemble, or decompile any products, prototypes, software, or other tangible objects that embody Protected Materials.

3.3 Recipient shall not produce privileged Protected Materials unless or until directed to do so by an order of a court of competent jurisdiction, or upon the prior written consent of the other party. No privilege or objection shall be waived by a party hereunder without the prior written consent of the other party.

3.4 The parties agree that the inadvertent or unintentional disclosure of confidential, privileged or work product materials supplied under this Agreement, regardless of whether the information was so designated at the time of disclosure, shall not be deemed a waiver in whole or in part of any applicable confidentiality, privilege or immunity, either as to the specific information disclosed or as to any other information relating thereto or on the same or related subject matter (and no party will assert such a waiver argument). Upon the discovery of the inadvertent error, the disclosing party shall promptly notify the other party, and both parties shall cooperate to restore the confidentiality, privilege or immunity to that disclosed material, including retrieval of all copies, if possible.

3.5 Except as herein provided, in the event that Recipient is requested or required in the context of a litigation, governmental, judicial or regulatory investigation or other similar proceedings (by oral questions, interrogatories, requests for information or documents, subpoenas, civil investigative demands or similar process) to disclose any Protected Materials, the party or their Counsel shall promptly inform the other party and their Counsel, assert all applicable privileges, including, without limitation, the common interest doctrine, the joint prosecution privilege, and take any other reasonable steps (at its own expense) to protect and preserve the confidentiality of and privileges relating to such Protected Materials .

4. Relationship; Additions; Termination.

4.1 This Agreement does not create any agency or similar relationship among the parties. Nothing in this Agreement requires a party to provide information or documents to the other party or to create Protected Materials to provide to the other party. Despite the execution of the PPA by Purchaser and Seller and the delivery of the files and documentation, as per Section 3.2 of the PPA, neither party nor their respective Counsel has the authority to waive any applicable privilege or doctrine on behalf of any other party.

4.2 Nothing in this Agreement affects the separate and independent representation of each party by its respective Counsel or creates an attorney client relationship between the Counsel for a party and the other party to this Agreement.

4.3 This Agreement shall continue until terminated upon the written request of either party. Upon termination, each party and their respective Counsel shall return any Protected Materials furnished by the other party. Notwithstanding termination, this Agreement shall continue to protect all Protected Materials disclosed prior to termination. Sections 3, 4 and 5 shall survive termination of this Agreement.

5. General Terms.

5.1 This Agreement is governed by the laws of the State of California, without regard to its choice of law principles to the contrary. In the event any provision of this Agreement is held by any court of competent jurisdiction to be illegal, void or unenforceable, the remaining terms shall remain in effect. Failure of either party to enforce any provision of this Agreement shall not be deemed a waiver of future enforcement of that or any other provision.

5.2 The parties agree that a breach of this Agreement would result in irreparable injury, that money damages would not be a sufficient remedy and that the disclosing party may be entitled to equitable relief, including injunctive relief, as a non-exclusive remedy for any such breach.

5.3 Notices given under this Agreement shall be given in writing and delivered by messenger or overnight delivery service to a party at the address specified in the PPA, and shall be deemed to have been given on the day received.

5.4 This Agreement memorializes a prior verbal discussion between the parties, and it is effective and binding upon each party at least as of the date it is signed by or on behalf of either party. This Agreement may be amended only by a writing signed by or on behalf of each party, and neither party may assign this Agreement without the prior written consent of the other party. This Agreement may be executed in counterparts. Any signature reproduced or transmitted via email of a .pdf file, photocopy, facsimile or other process of complete and accurate reproduction and transmission shall be considered an original for purposes of this Agreement.

5.5 No Party makes any representation or warranty (express or implied) as to the legal or factual accuracy or completeness of any Protected Materials provided under this Agreement.

5.6 Each provision of this Agreement shall be interpreted in such a manner as to be effective and valid under applicable law. If any provision of this Agreement is determined by a Court of competent jurisdiction to be invalid or unenforceable, the Parties intend for the Court to rewrite the invalid or unenforceable provision to preserve the intention of the Parties to the degree possible, and to keep the remainder of this Agreement in full force and effect.

5.7 This Agreement sets forth the entire agreement and understanding between the parties as to the protection of the Protected Materials and supersedes and merges all prior oral and written agreements, discussions and understandings between them regarding the subject matter of this Agreement. Notwithstanding the foregoing, this Agreement shall not supersede any existing nondisclosure or confidentiality agreement between the parties which contains terms more restrictive than those herein, and this Agreement in no way supersedes, amends or alters the requirements of the PPA.

5.8 This Agreement imposes no obligation upon Recipient with respect to Protected Materials that Recipient can reasonably demonstrate (a) was in Recipient's rightful possession on or before receipt from Discloser; (b) is or becomes a matter of public knowledge through no fault of Recipient; (c) is rightfully received by Recipient from a third party without a duty of confidentiality; or (d) is independently developed by Recipient without use of or reference to Protected Materials.

This Agreement is being executed by each of the undersigned counsel on behalf of the respective party he/she represents. By executing this agreement, the undersigned hereby acknowledge that they have read and understood the terms of this Agreement, that they have authority to bind their respective party, and that by their signing this Agreement, the Party agrees to be bound by all terms, conditions, and obligations contained herein.

Lone Star Silicon Innovations LLC

By: _____

Name: Christian Dubuc

Date: August 4, 2016

Advanced Micro Devices, Inc.

By: _____

Name: KEVIN O'NEIL

Date: AUGUST 4, 2016

Exhibit E

Unlicensed Third Party Entities

Avago Technologies (including Broadcom Limited and LSI Corporation)

Elite Semiconductor Products Inc.

Etron Technology, Inc.

Integrated Silicon Solution Inc.

Kingston Technology Corporation

Marvell Technology Group, Limited

Maxim Integrated Products Inc.

MediaTek Inc.

Micron Technology, Inc.

Nanya Technology Corporation

Qualcomm Inc.***

Toshiba Corporation

SanDisk Corporation

Texas Instruments Incorporated

STMicroelectronics N.V.

Infineon Technologies AG**

United Microelectronics Corporation

Semiconductor Manufacturing International Corporation

Renesas Electronics Corporation

Tower Semiconductor Ltd.

Xilinx, Inc.

Zen-Tel Inc.

** Subject to certain licenses pursuant to AMD-Seimens AG agreement on or about Feb, 1985 and/or Joint Development Contract regarding GDDR5 Specification Development on or about Dec, 2005

*** Subject to certain licenses pursuant to an AMD-Qualcomm transaction related to AMD's former handheld business.

Exhibit F

DISCLOSURE SCHEDULE

Reference is made to that certain Patent Transfer Agreement, dated as of August 4th, 2016 (the "**Agreement**"), by and between Lone Star Silicon Innovations LLC, an entity organized under the laws of [Enter Jurisdiction] having its primary place of business at [Enter Jurisdiction] ("**Lone Star**"), and Advanced Micro Devices, Inc., a Delaware corporation ("**AMD**"). Capitalized terms used but not defined in this disclosure schedule (the "**Disclosure Schedule**") shall have the respective meanings ascribed to such terms in the Agreement.

Any matter disclosed in any section of this Disclosure Schedule shall be deemed to be disclosed with respect to (i) the corresponding section of the Agreement identified or cross-referenced therein, and (ii) any other section of the Agreement to which such disclosure's application or relevance is reasonably apparent on the face of such disclosure.

Matters reflected in this Disclosure Schedule are not necessarily limited to matters required by the Agreement to be reflected herein. Such additional matters are set forth for informational purposes (but do not necessarily include other matters of a similar informational nature).

The disclosure of any specific item in this Disclosure Schedule shall not imply, establish or constitute an admission that such item or other items are or are not material, nor imply, establish or constitute an admission of such item's consequence or relevance to any determination of materiality. In any dispute or controversy between the parties, neither party shall use the fact of the disclosure of any such item as relevant to determine whether any obligation, item or matter not described in the Agreement or included herein is or is not material for purposes of the Agreement. Furthermore, the disclosure of any specific item in this Disclosure Schedule shall not imply, establish or constitute an admission that such item or other items are required to be disclosed under the Agreement.

Any item of information disclosed in this Disclosure Schedule shall be subject to the confidentiality terms and conditions set forth in Sections 7.6, 7.7 and 7.8 (and other terms and conditions if and to the extent relevant) of the Agreement.

Headings, other than numerical references to sections and subsections of the Agreement, are inserted in this Disclosure Schedule for convenience of reference only, and do not amend or change the express description of the section of this Disclosure Schedule referred to in the Agreement.

Section 6.1(b): Title and Contest

Section 6.1(b)(iii):

None.

Section 6.1(b)(vi):

None.

Section 6.1(b)(vi):

None.

Section 6.1(c): Litigation

None.

Exhibit G

PATENT SECURITY AGREEMENT

Patent Security Agreement, dated as of August 4th, 2016, by Lone Star Silicon Innovations LLC, an entity organized under the laws of Texas having its primary place of business at 5204 Bluewater Drive, Frisco, TX 75034 (the "Grantor"), in favor of Advanced Micro Devices, Inc., an entity organized under the laws of Delaware having its primary place of business at 1 AMD Place, Sunnyvale, California, 94088 (the "Grantee").

WITNESSETH:

WHEREAS, the Grantor is party to a Patent Assignment Agreement with an Effective Date of August 4th, 2016 (as amended or otherwise modified from time to time, the "Patent Transfer Agreement") pursuant to which the Grantee is selling its interest in certain patents to the Grantor and the Grantor is required to execute and deliver this Patent Security Agreement;

NOW, THEREFORE, in consideration of the promises and to induce the Grantee, to enter into the Patent Transfer, the Grantor hereby agrees with the Grantee as follows:

SECTION 1. Defined Terms. Unless otherwise defined herein, terms defined in the Patent Assignment Agreement and used herein have the meaning given to them in the Patent Agreement.

SECTION 2. Grant of Security Interest in Patents. The Grantor hereby pledges and grants to the Grantee a lien on, and security interest in, and to all of its right, title and interest in, to and under all the following pledged assets of the Grantor:

(a) the Assigned Patents of the Grantor listed on Schedule I attached hereto.

SECTION 3. The Security Agreement. The security interest granted pursuant to this Patent Security Agreement is granted in conjunction with the security interest granted to the Grantee pursuant to the Patent Transfer Agreement and the Grantor hereby acknowledges and affirms that the rights and remedies of the Grantee with respect to the security interest in the Assigned Patents made and granted hereby are more fully set forth in the Patent Transfer Agreement. In the event that any provision of this Patent Security Agreement is deemed to conflict with the Patent Transfer Agreement, the provisions of the Security Agreement shall control unless the Grantee shall otherwise determine.

SECTION 4. Termination. Upon the termination of the Patent Transfer Agreement, the Grantee shall, at the expense of the Grantor, execute, acknowledge, and deliver to the Grantor an instrument in writing in recordable form releasing the lien on and security interest in the Assigned Patents under this Patent Security Agreement and any other documents required to evidence the termination of the Grantee's interest in the Patents.

SECTION 5. Counterparts. This Patent Security Agreement may be executed in any number of counterparts, all of which shall constitute one and the same instrument, and any party hereto may execute this Patent Security Agreement by signing and delivering one or more counterparts.

Lone Star Silicon Innovations LLC

By: _____

Name: Christian Dubuc

Date: August 4, 2016

Advanced Micro Devices, Inc.

By: _____

Name: Kevin ONeil

Date: August 4, 2016

Exhibit I to Patent Security Agreement

Family	Title	Patent No.
1	Semiconductor device having an elevated active region formed in an oxide trench	US6104069
1	Semiconductor device having an elevated active region formed in an oxide trench and method of manufacture thereof	US5872038
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US5956610
2	Local interconnects for improved alignment tolerance and size reduction	US6121663
2	Methods and arrangements for insulating local interconnects for improved alignment tolerance and size reduction	US6399480
2	Method and system for providing electrical insulation for local interconnect in a logic circuit	US6303949
3	Run to run control process for controlling critical dimensions	USRE39518
3	Run-to-run control process for controlling critical dimensions	US5926690
4	Method of forming a contact hole in an interlevel dielectric layer using dual etch stops	US5912188
5	Elimination of residual materials in a multiple-layer interconnect structure	US6153933
6	Method and system for providing an interconnect having reduced failure rates due to voids	US6010960
7	Method of making gate dielectric for sub-half micron mos transistors including a graded dielectric constant	US6015739
8	Silicided shallow junction transistor formation and structure with high and low breakdown voltages	US5973372
9	Dual damascene process using sacrificial spin-on materials	US6057239
9	Dual damascene process using sacrificial spin-on materials	US6424039
10	Borderless vias	US5925932
10	High integrity vias	US6097090
10	Borderless vias	US6232221
11	Core cell structure and corresponding process for nand-type high performance flash memory device	US6023085
11	Core cell structure and corresponding process for nand type performance flash memory device	US6372577
12	Methods and arrangements for improved spacer formation within a semiconductor device	US6103611
12	Semiconductor device having uniform spacers	US6380588
13	Semiconductor device having dual gate electrode material and process of fabrication thereof	US6043157
14	Selectively sized spacers	US6046089
15	Trenched gate metal oxide semiconductor device and method	US6097061
15	Trenched gate metal oxide semiconductor device and method	US6667227
16	Integrated circuit having an interlevel interconnect coupled to a source/drain region(s) with source/drain region(s) boundary overlap and reduced parasitic capacitance	US6146978

Family	Title	Patent No.
17	Ultrathin, nitrogen-containing mosfet sidewall spacers using low-temperature semiconductor fabrication process	US6323519
18	Use of silicon oxynitride arc for metal layers	US6326231
19	Semiconductor package with supported overhanging upper die	US6337226
20	Low dielectric constant etch stop layers in integrated circuit interconnects	US6388330

Confidential

AMENDMENT to PATENT TRANSFER AGREEMENT

WHEREAS, the undersigned parties entered into a PATENT TRANSFER AGREEMENT, effective August 4, 2016 (the "**Agreement**"), by and among Lone Star Silicon Innovations LLC, an entity organized under the laws of State of Texas having its primary place of business at 8105 Rasor Blvd., Suite 210, Plano, Texas 75024 ("**Lone Star**") and Advanced Micro Devices, Inc., a Delaware corporation ("**AMD**"). Lone Star and AMD are herein referred to separately as "a party" or collectively as "the parties."

WHEREAS, pursuant to the Agreement, Lone Star acquired certain patents (the "**Assigned Patents**") from AMD, and Lone Star is currently engaged in efforts to enforce and license the Assigned Patents;

WHEREAS, pursuant to Paragraph 6.2(f) of the Agreement, Lone Star acknowledged that the Assigned Patents are subject to Existing Encumbrances to other Persons and represented and warranted that Lone Star will not commence, direct or control any legal action seeking to enforce and/or licensing activity asserting any of the Assigned Patents against a Person that is (1) not an Unlicensed Third Party Entity or Affiliate thereof, or (2) is a distributor, reseller, or direct or indirect customer with respect to materials, devices, software or firmware, services or products that are used, made or supplied directly or indirectly by or for a Person that is not an Unlicensed Third Party Entity;

WHEREAS, the Agreement limits Unlicensed Third Party Entity to only those Persons listed in Exhibit E thereof, their Affiliates, and all other Persons that the Parties may agree in writing in the future to add to Exhibit E, and the Parties further agreed in Paragraph 3.3(c) to cooperate in good faith in attempting to identify additional third-parties that they agree to add to the Exhibit E list of Unlicensed Third Party Entities; and

WHEREAS, the Parties now desire to supplement the Exhibit E list to include additional Unlicensed Third Party Entities;

NOW, THERFORE, for good and valuable consideration, the sufficiency of which is hereby acknowledged, the Parties hereby agree to amend the Agreement as follows:

1. The Exhibit E list of Unlicensed Third Party Entities is replaced and superseded in its entirety by the updated Exhibit E, dated November 18, 2016, attached to this AMENDMENT to PATENT TRANSFER AGREEMENT.

All other terms of the Agreement remain in full force and effect.

IN WITNESS WHEREOF, the Parties have executed this AMENDMENT to PATENT TRANSFER AGREEMENT by their duly authorized officers in their respective corporate names.

Lone Star Silicon Innovations LLC	ADVANCED MICRO DEVICES, INC.
Signature: Khaled Fekih Rondhane	Signature:
Name: KHALED FEKIH-RONDHANE	Name: KEVIN ONEIL
Title: Managing Partner	Title: VP, IP & Licensing
Date: 11-19-2016	Date: 11-23-2016

Exhibit E
(Amended November 18, 2016)
Unlicensed Third Party Entities

Avago Technologies (including Broadcom Limited and LSI Corporation)

Elite Semiconductor Products Inc.

Etron Technology, Inc.

Integrated Silicon Solution Inc.

Kingston Technology Corporation

Marvell Technology Group, Limited

Maxim Integrated Products Inc.

MediaTek Inc.

Micron Technology, Inc.

Nanya Technology Corporation

Qualcomm Inc.***

Toshiba Corporation

SanDisk Corporation

Texas Instruments Incorporated

STMicroelectronics N.V.

Infineon Technologies AG**

United Microelectronics Corporation

Semiconductor Manufacturing International Corporation

Renesas Electronics Corporation

Tower Semiconductor Ltd.

Xilinx, Inc.

Zen-Tel Inc.

Western Digital Corporation

RPX Corporation****

**** Subject to certain licenses pursuant to AMD-Seimens AG agreement on or about Feb, 1985 and/or Joint Development Contract regarding GDDR5 Specification Development on or about Dec, 2005**

***** Subject to certain licenses pursuant to an AMD-Qualcomm transaction related to AMD's former handheld business.**

****** Lone Star is permitted to grant RPX Corporation license rights that include the right for RPX to grant sublicenses to any and all RPX members.**

Exhibit 2

US005973372A

United States Patent [19]

Omid-Zohoor et al.

[11] **Patent Number: 5,973,372**

[45] **Date of Patent: Oct. 26, 1999**

[54] **SILICIDED SHALLOW JUNCTION TRANSISTOR FORMATION AND STRUCTURE WITH HIGH AND LOW BREAKDOWN VOLTAGES**

[76] Inventors: **Farrokh Omid-Zohoor**, 8910 Shady Hills, San Antonio, Tex. 78250; **Nader Radjy**, 614 Greer Rd., Palo Alto, Calif. 94303

[21] Appl. No.: **08/986,283**

[22] Filed: **Dec. 6, 1997**

[51] **Int. Cl.**[6] **H01L 29/861**

[52] **U.S. Cl.** **257/383**; 257/754; 257/770; 438/607

[58] **Field of Search** 257/382, 383, 257/384, 754, 757, 769, 770; 438/607, 682, 683

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,225,896 7/1993 Van Roozendaal et al. 257/384

5,416,034 5/1995 Bryant 437/47

Primary Examiner—David B. Hardy

Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A method, and structure resulting therefrom, of forming a metal silicide at a shallow junction in a single crystal substrate without encroaching on the shallow junction by forming a metal layer on the substrate over the junction followed by forming a layer of a silicon material which reacts with the metal faster than the silicon in the single crystal substrate. Titanium is the preferred metal and amorphous silicon is the preferred silicon layer and is of a thickness to react with all of the titanium. The two layers are rapid thermal annealed to form titanium silicide. A second rapid thermal anneal is performed which converts the majority of the C49 phase of the titanium silicide to a less resistive and more conductive C54 phase and causes a silicon epitaxial layer to form between silicon substrate and the titanium silicide.

13 Claims, 4 Drawing Sheets

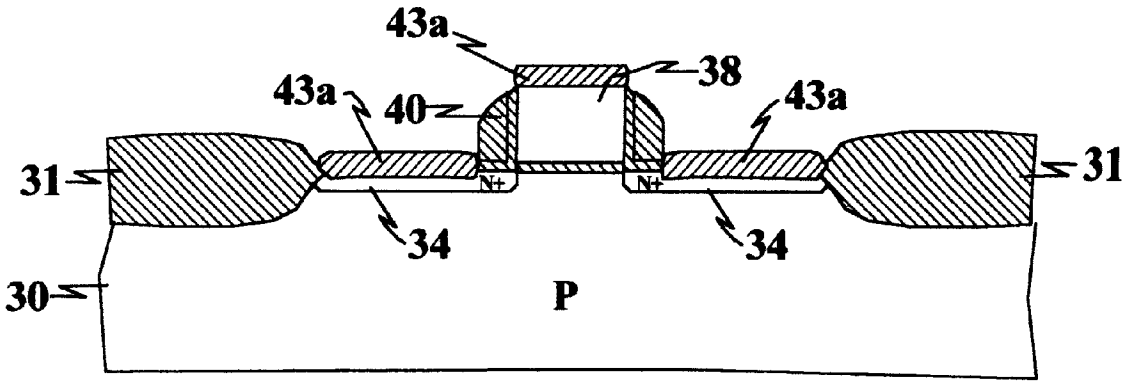


FIG. 1(a)
(Prior Art}

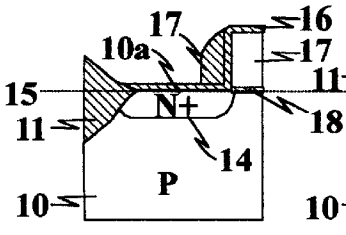


FIG. 1(b)
(Prior Art}

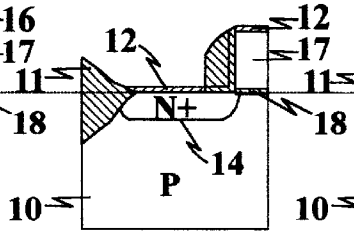


FIG. 1(c)
(Prior Art}

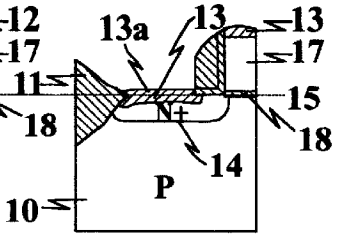


FIG. 2(a)

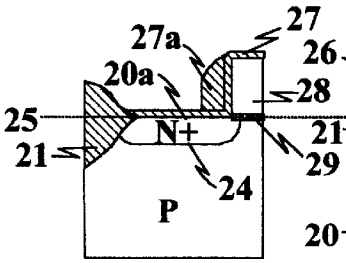


FIG. 2(b)

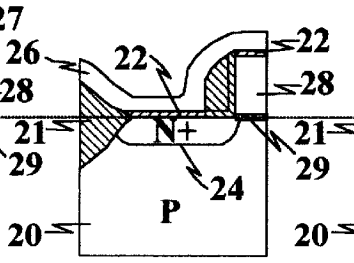


FIG. 2(c)

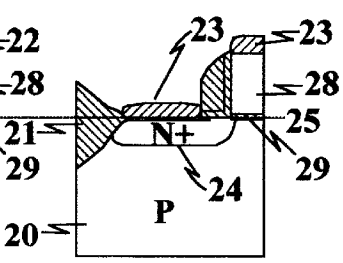


FIG. 3a

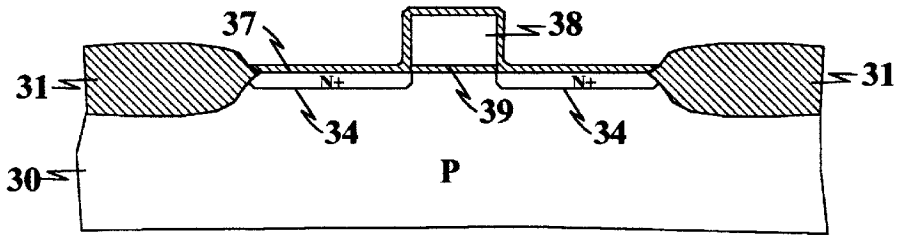


FIG. 3b

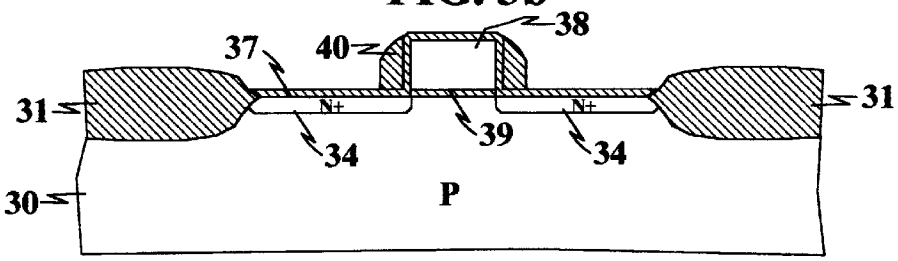


FIG. 3c

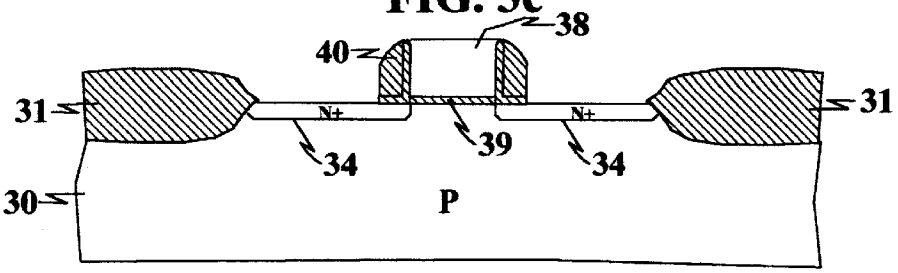


FIG. 3d

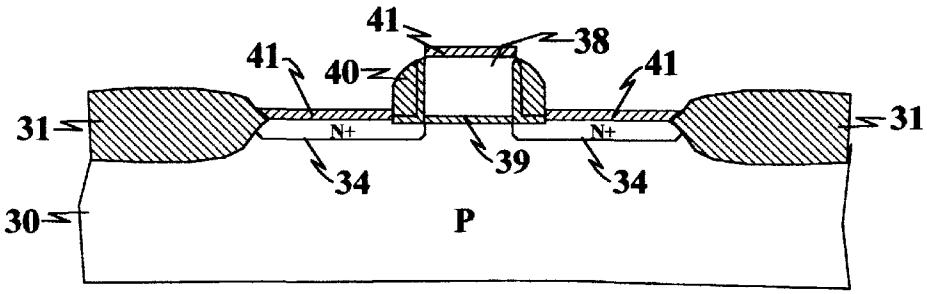


FIG. 3e

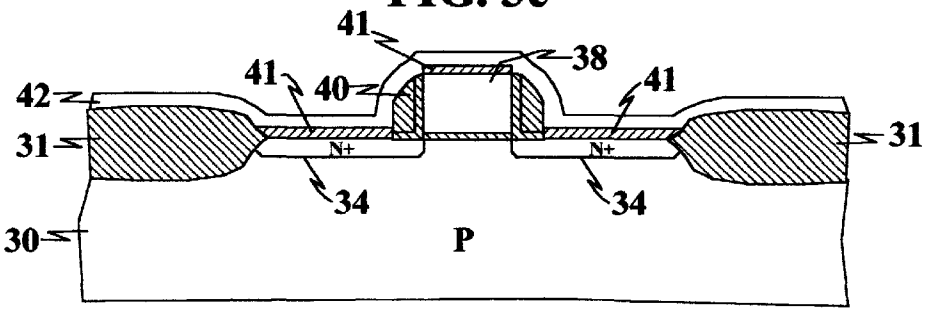


FIG. 3f

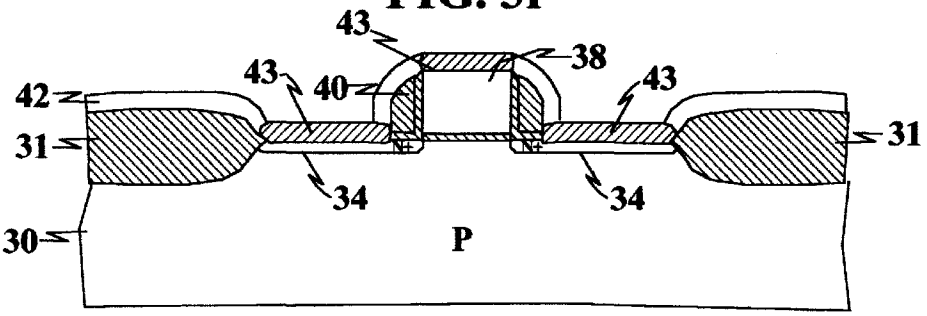


FIG. 3g

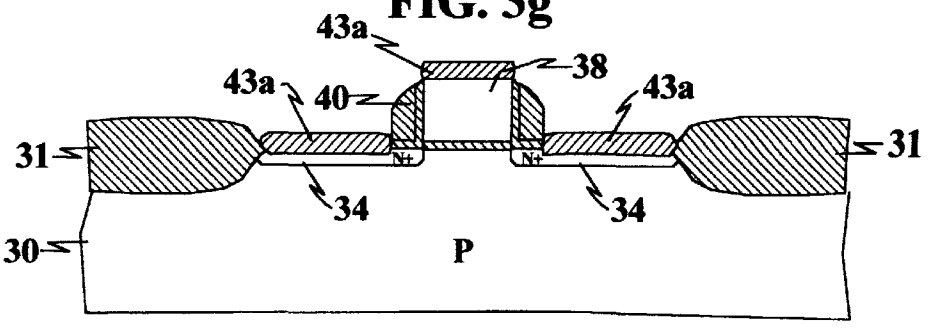


FIG. 3h

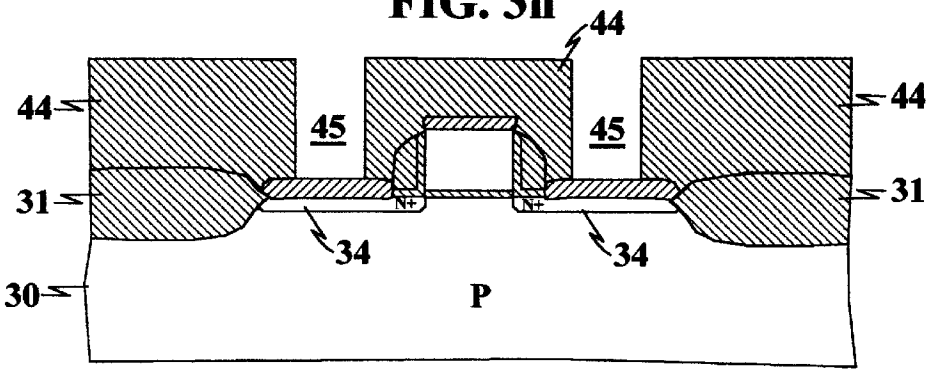


FIG. 3i

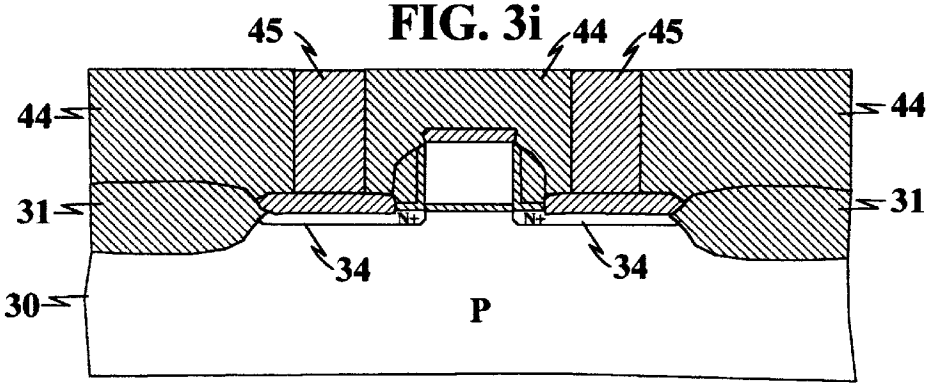


FIG. 4a

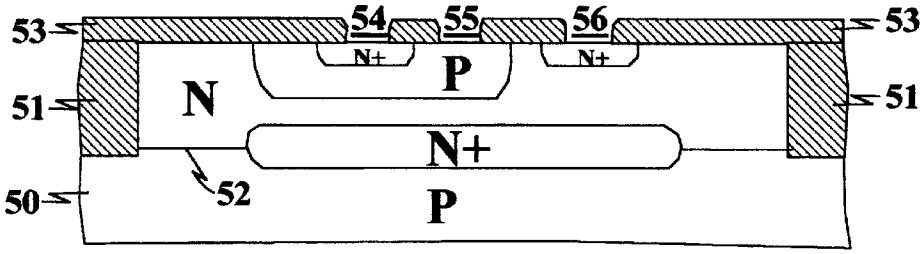


FIG. 4b

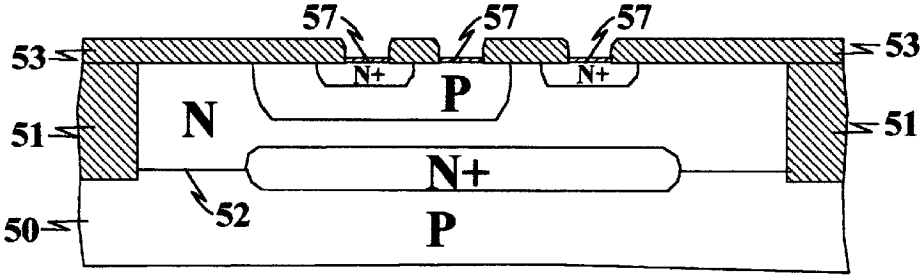


FIG. 4c

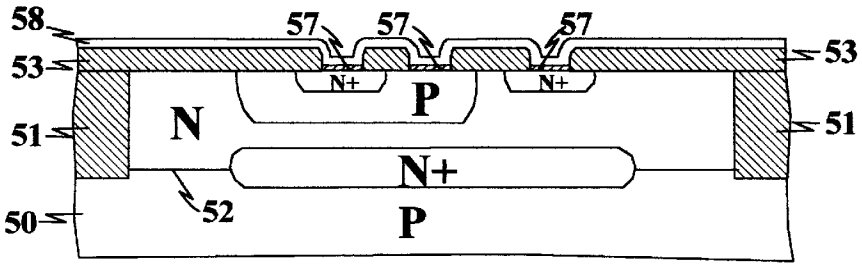


FIG. 4d

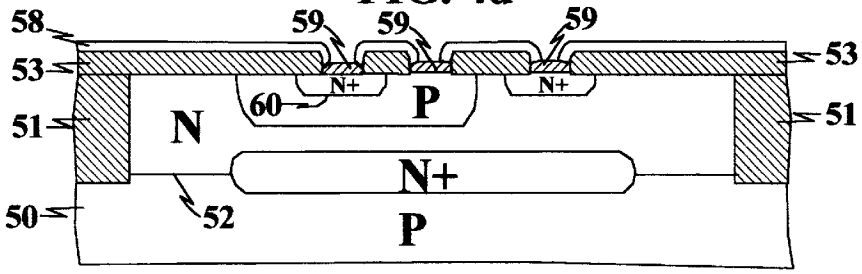


FIG. 4e

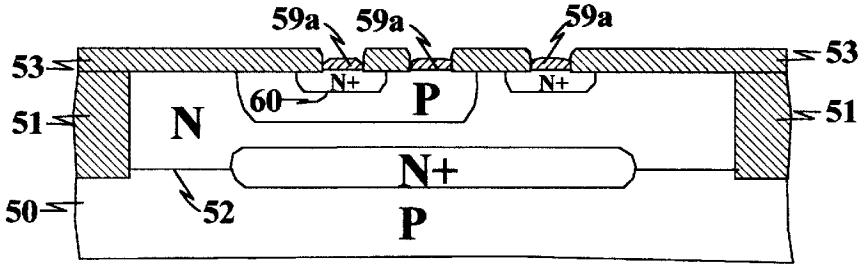


FIG. 4f

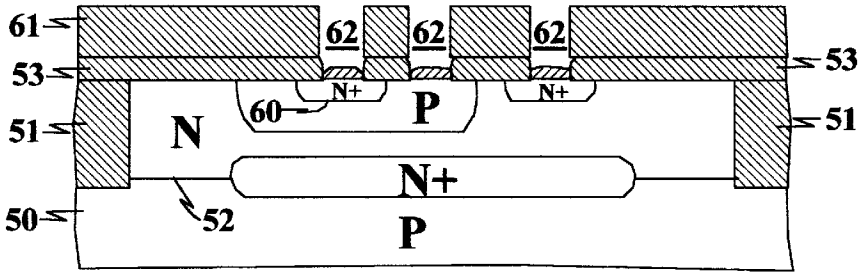
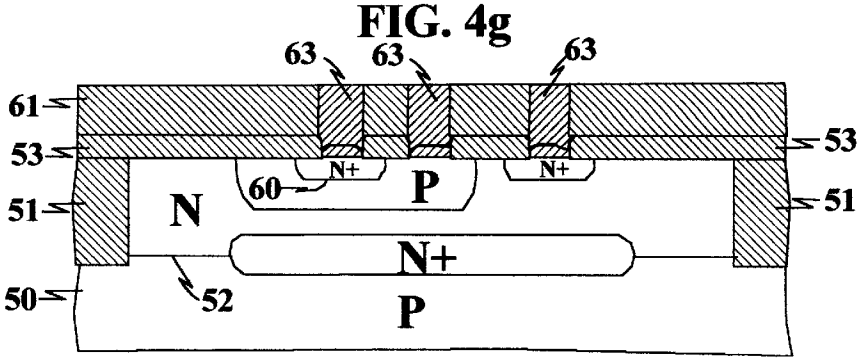


FIG. 4g



SILICIDED SHALLOW JUNCTION TRANSISTOR FORMATION AND STRUCTURE WITH HIGH AND LOW BREAKDOWN VOLTAGES

FIELD OF THE INVENTION

The present invention relates to fabricating integrated circuits and, more specifically, to fabricating silicided shallow junctions and the resultant structure.

BACKGROUND OF THE INVENTION

In the conventional self aligned silicides fabrication, which is has been given the name "salicide process", the silicidation process usually is carried out after the formation of the junctions. In the case of NMOS, PMOS, CMOS and BiCMOS, the silicidation process is after the source/drain implant and anneal and, in the case of bipolar, the silicidation process is after the emitter to base junction formation and anneal. For example, in the conventional CMOS fabrication process, after the gate definition, LDD implant, spacer formation and source/drain implant screen oxide, the source and drains are implanted and annealed. After removal of the screen oxide and a clean step, titanium or another refractory metal or Group VIII metals is deposited and annealed to form the silicide, such as titanium silicide. During the silicidation process with titanium, the silicon is the moving species and, as the silicide is formed, the silicon below the original silicon surface is consumed. It is well established that 1 angstrom of titanium (Ti) will react with 2.27 angstroms of crystalline silicon to produce 2.4 angstroms of titanium silicide ($TiSi_2$).

Advanced high performance submicron NMOS, PMOS, CMOS, biCMOS and bipolar integrated circuits require further down scaling of the devices in the lateral and vertical directions. However, as the gate length is scaled down, the vertical dimension of the devices, such as gate oxide thickness and junction depth need to be scaled down accordingly for optimum performance of the devices and to alleviate short channel effects. However, as vertical and laterally scaling of these devices continues, the fabrication of very shallow junctions create additional challenges due to the very low implant energy required to fabricate very shallow junctions and the higher parasitic source and drain resistance for field effect transistors (FETs), such as CMOS, and emitter resistance for bipolar introduced by the shallow junctions, as well as excessive off leakage current for FETs. To reduce the parasitic resistances, these advanced integrated circuits employ silicides at the shallow junctions and thereby increase device speed and performance. However, a major portion (~one-half) of the originally implanted shallow junction in the silicon substrate is consumed by the silicidation in the conventional salicidation process and such consumption of the silicon substrate during silicidation degrades the integrity of the shallow junctions and sets a lower limit for the junction depth. A similar situation exists in using the conventional method in fabricating silicided shallow emitters in bipolar or biCMOS integrated circuits. In addition, the junction depths of the silicided sources and drains or the junction depth of the silicided emitters are all the same depth and have common device characteristics.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method of fabricating an integrated circuits with salicided shallow junctions without degrading the integrity of the junctions.

Another object of present invention is to provide an integrated circuit fabrication method in which only a minimum of the silicon substrate is consumed during salicidation.

An additional object of the present invention is to provide an integrated circuit structure with silicided shallow junctions with the lower surface of the silicide at or slightly below the silicon substrate.

A further object of the present invention is to provide an integrated circuit fabrication method in which, due to the salicidation process, the transistors of the integrated circuit can be formed with different device characteristics.

A still further object of the present invention is to provide an integrated circuit fabrication method in which, due to the salicidation process, the source and drain of a transistor can be formed with asymmetric junction depths.

In accordance with the present invention, an integrated circuit silicon substrate with at least one shallow junction is fabricated comprising the steps of, after the formation of a shallow junction: depositing a metal layer capable of reacting with silicon to form a silicide at the shallow junction, selectively depositing on the metal a layer of a silicon material which reacts with a metal to form a silicide at a faster rate than silicon in the silicon substrate, and reacting the silicon of the deposited silicon material with the metal to form the metal silicide. Preferably, the metal is a refractory metal or a Group VIII metal and, most preferably, the metal is titanium and the silicon material is amorphous (α) silicon, of which metal preferably is selectively deposited and the α-silicon is sputtered. The silicon material is of a thickness so that the majority of the metal reacts with the silicon of the silicon material and only a small amount of the silicon of the silicon substrate is consumed during the silicide reaction. According to another aspect of the present invention, the deposited silicon material can be doped and the doping can be used as a parameter to control the amount of silicon contibuted from the silicon material and thereby permit different junction depths between transistors in an integrated circuit or even between a source and a drain of the same transistor. According to still another aspect of the present invention, an integrated circuit including a silicon substrate having an upper surface and a shallow junction disposed thereunder comprising: a metal silicide layer having a lower surface and being disposed at the shallow junction, and a silicon epitaxy layer positioned between the upper surface of the silicon substrate and the lower surface of the metal silicide.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiments of the invention with reference in the drawings, in which:

FIGS. **1***a, b* and *c* are cross-sectional views of the prior art method of forming a refractory metal silicide at the surface of an active region of a transistor.

FIGS. **2***a, b* and *c* are cross-sectional views of method of the present invention of forming a refractory metal silicide at the surface of an active region of a transistor.

FIG. **3***a* is a cross-sectional view of the portion of a semiconductor substrate with isolation regions on opposite sides of a partially completed field effect transistor having a source, drain and gate and a conformal insulating layer over the source and drain and covering the gate as the starting point in describing the method of the present invention.

FIG. **3***b* is a cross-sectional view of the portion of the semiconductor substrate of Figure a with insulating sidewalls abutting the insulating layer on the gate.

FIG. **3***c* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***b* with the insulating layer removed over the source and drain and on top of the gate.

FIG. **3***d* is a is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***c* with a refractory metal selectively deposited on semiconductor substrate surface over the source and drain and on top of the gate.

FIG. **3***e* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***d* with a layer of a silicon containing material deposited on the isolation regions, the refractory metal and the sidewalls.

FIG. **3***f* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***e* with the refractory metal reacted with the silicon containing material and slightly with the N+ silicon substrate to form metal silicide.

FIG. **3***g* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***f* with the silicon containing material removed from isolation regions and the sidewalls.

FIG. **3***h* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***g* with an interlevel insulating layer having contact openings to the metal silicide of the source and drain.

FIG. **3***i* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **3***h* with the contact openings filled with a conductive material.

FIG. **4***a* is a cross-sectional view of the portion of a semiconductor substrate with isolation regions on opposite sides of a partially completed bipolar transistor having an emitter, base and collector and an insulating layer over the semiconductor substrate with openings to the emitter, base and collector.

FIG. **4***b* is a is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***a* with a refractory metal selectively deposited on semiconductor substrate surface over the emitter, base and gate.

FIG. **4***c* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***b* with a layer of a silicon containing material deposited on the insulating layer and the refractive metal.

FIG. **4***d* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***c* with the refractive metal reacted with the silicon containing material and slightly with the N+ silicon substrate to form metal silicide.

FIG. **4***e* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***d* with the silicon containing layer removed from the insulating layer.

FIG. **4***f* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***e* with an interlevel insulating layer having contact openings to the metal silicide of the emitter, base and collector.

FIG. **4***g* is a cross-sectional view of the portion of the semiconductor substrate of FIG. **4***f* with the contact openings filled with a conductive material.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to the prior art drawings of FIGS. **1**(*a*)–(*c*), FIG. **1**(*a*) shows a single crystalline P doped silicon substrate **10** with LOCOS isolation **11** and N-type impurities to form a P-N+ shallow junction **14** with the surface **10***a* of the substrate **10** exposed. A insulating layer **16** is on the surface **10***a* of the substrate **10** and on the vertical wall of a gate **17**

on a gate oxide **18** of a partially shown NMOS field effect transistor. An insulating spacer **19** is formed on the vertical wall of the gate **17**. The layer **16** served as an implant screen during the formation of the shallow junction. In FIG. **1**(*b*), the insulating layer is removed and a refractory metal, such as a titanium layer **12**, is deposited on the now exposed surface **10***a*. In FIG. **1**(*c*) titanium silicide **13** is formed by reacting the titanium **12** with the silicon substrate **10**. It will be noted that shape of the titanium silicide **13** is above the original substrate surface **10***a* as evidenced by the dashed line **15** drawn through FIGS. **1**(*a*)–(*c*). More importantly, it will be noted that the major growth of the titanium silicide is into the silicon substrate, again as evidence by the dashed line **15**, and the greatest growth is at the edges where the N+ impurities are in lower concentration than in the center of the active region. Because of this shape of the titanium silicide, the shallow junction becomes ever more shallow and the result is degrading of the integrity of the shallow junctions.

Turning now to FIGS. **2**(*a*)–(*c*) of the present invention, FIG. **2**(*a*) again shows a single crystalline P doped silicon substrate **20** with LOCOS isolation **21** and N-type impurities to form a N+/P shallow junction **24** with the surface **20***a* of the substrate **20** exposed. A insulating layer **27** is preferably thermally grown on the surface **20***a* of the substrate **20** and on the vertical wall and top of a gate **28** on a gate oxide **29** of a partially shown NMOS field effect transistor. A insulating spacer **27***a*, preferably silicon nitride, is formed on the vertical wall of the gate **28**. The layer **27** served as an implant screen during the formation of the shallow junction and the doping of the gate. The layer **27** also can serve as an etch stop during the formation of the silicon nitride spacer due to the difference in etch selectivity between silicon oxide and silicon nitride. In FIG. **2**(*b*), a refractory metal, such as a titanium, or a Group VIII metal layer **22** is selectively deposited on the exposed surface **20***a* followed by the deposition, on the titanium layer **22**, of a layer of a silicon containing material **26**, such as amorphous (α) silicon, which silicides at a faster rate than single crystal silicon. In FIG. **2**(*c*), titanium silicide **23** is formed by reacting the titanium **22** with the amorphous silicon **26** and slightly with the silicon substrate at a temperature of about 650 C. In the prior art silicidation method with the single crystal substrate of FIGS. **1**(*a*)–(*c*), the silicon atoms migrate towards the titanium atoms where they react and form $TiSi_x$ (phase C49). The silicon atoms diffuse towards the titanium atoms through the crystal vacancies or regions which are referred to as the centers for nucleation. Because, in contrast to single crystal silicon, amorphous silicon has many more centers of nucleation and the migration occurs at a much faster rate. Silicon atoms from the amorphous silicon layer **26** and silicon atoms from the single crystal substrate **10** and polycrystalline silicon gate **28** migrate from the top to the bottom and from the bottom to the top, respectively, to the titanium layer **22**. The reaction stops when all of the titanium layer **22** is reacted. Since the amorphous silicon silicides much faster than the single crystal substrate, most of the silicidation occurs upward away from the original silicon surface **20***a*, as evidenced by dashed line **25**, and only a very small portion of shallow junction is consumed, unlike the prior art method of FIGS. **1**(*a*)–(*c*). It is important to note that the silicide formed from single crystal silicon and amorphous silicon is C54 phase after a second anneal. With a thick amorphous silicon layer **26**, which is sufficiently thick so as to not be totally consumed by the silicidation, silicon atoms from the amorphous silicon layer migrate through the titanium silicide **23** and to the single crystal silicon substrate and, in accordance with the device structure

of the present invention, form a solid phase epitaxy layer as shown in the vicinity of the silicide and the N+ boundry in FIG. **2**(*c*). Accordingly, because the titanium silicide **23** is at or above the original silicon surface **10***a,* the shallow junction is not consumed and the integrity of the shallow junction is maintained.

Turning now to FIGS. **3***a*–**3***i,* which illustrate the fabrication method of the present invention, FIG. **3***a* shows the cross-section of a NMOS field effect transistor (FET) to the point of a silicon substrate **30** having formed therein isolation regions **31**, herein LOCOS although trench isolation also can be used. A thin insulating layer **37**, preferably silicon oxide, is on the surface of the silicon substrate and covers a gate **38**, which is doped polysilicon but also may be a composite gate structure, on a gate oxide **39**. N-type impurities or, alternatively, P-type have been implanted into silicon substrate **30** and the gate **38**, using the gate as the alignment mask, and annealed by rapid thermal anneal to diffuse and activate the impurities and form a N+/P or P+/N shallow junction **34**. The shallow junctions are less than about 2500 Å and, with arsenic (As) as the impurity, the desired depth of the N+/P shallow junctions can be achieved by projecting 500 Å for implant energies of 75 keV. In the case of shallow P+/N junction, boron difluoride (BF_2) is used as the impurity and the desired depth can be achieved by projecting about 300 Å for implant energies of 50 keV. In the present instant, the depth of the N+/P shallow junction is about 1000 Å and the P+/N shallow junction is about 1200 Å from the silicon substrate surface. In FIG. **3***b,* insulating spacers **40** are formed is formed on the sidewalls of the gate **38** and is separated from the gate by the insulating layer **37**. The spacers **40** preferably are silicon nitride and are formed by depositing a conformal layer of silicon nitride and then anisotropically etching the layer with a reactive ion etcher to create the spacers **40**. Silicon nitride is the preferred insulating material because the silicon oxide layer **37** serves as an etch stop during the formation of the spacer and prevents gouging of the silicon substrate. In addition, the silicon nitride spacer is not eroded away during the removal by etching of the silicon oxide screen layer **37**, thereby precluding any possible shorting of the gate **38**. After the spacers formation, the substrate is cleaned and subjected to a short hydrogen fluoride etch (herein 100:1) to remove the insulating layer **37**, herein silicon oxide, over the source and drain and on top of the gate **38** as shown in FIG. **3***c*. As previouly stated, the removal of the silicon oxide layer is a further reason for using silicon nitride as the insulating spacer material since silicon nitride has a etch selectivity difference from silicon oxide.

Next, a refractory metal **41**, herein titanium, or a Group VIII is selectively deposited by chemical vapor deposition (CVD), using conventional CVD equipment on the exposed source and drain and on top of gate to a thickness of about 300–400 Å, preferably about 400 Å, as shown in FIG. **3***d*. Although titanium is preferred, other refractory metals, such as tungsten, tantalum and molybdenum, as well as Group VIII metals, such as cobalt, platinum, palladium and nickel, may be used. Now, in accordance with the present invention, a silicon containing material **42** which silicates faster than single crystal silicon and which herein is amorphous silicon is sputter deposited, using conventional sputter equipment with a silicon target, to a thickness of about 650 to 850 Å, preferably about 850 Å as shown in FIG. **3***e*. Although amorphous silicon is the preferred silicon containing material, polycrystalline silicon also may be used.

In addition and in accordance with another aspect of the present invention, the silicon containing material may be doped with an impurity since silicidation occurs less readily with doped amorphous and polysilicon than undoped amorphous silicon and polysilicon. By varying the doping of the amorphous silicon, silicidation reaction rate can be a parameter for controlling the amount of silicon (N+ for N+ source/drain or P+ for P+ source/drain) in the substrate. For N+/P junctions, the amorphous silicon can be doped with an N-type impurity such as phorphous, arsenic, or antimony and, for P+/N junctions, the amorphous silicon can be doped with boron or boron difluoride. With this aspect of the present invention, the amount of silicate from the amorphous silicon can be reduced so that more of the silicate results from the silicon substrate and, in this way, the depth of the shallow junction from the silicate can be varied not only between transistors, but the source and drain of a transistor can be of different junction depths. Accordingly, this ability to dope the deposited silicon material **42** to change the silicidation rate provides the capability to tailor the depth of the junction from the silicide.

The substrate **30** is now subjected to a rapid thermal anneal at about 650° C. to cause the formation of titanium silicide **43**. Because silicidation takes place much faster in amorphous silicon than single crystal silicon, most of titanium silicide forms above the original surface of the silicon substrate **30** and does not encroach on the shallow N+/P junctions **34** as shown in FIG. **3***f*. The silicidation is followed by using a selective etch to remove the unsilicided amorphous silicon without etching the titanium silicide and then the substrate is subjected to another rapid thermal anneal at about 800° C. which converts the C49 phase of the silicide **43** into a much less resistive or more conductive and stable phase C54 of silicide **43***a* with the result being shown in FIG. **3***g*. Silicides of titanium, cobalt, platinum, palladium and nickel exhibit the lowest resistivities and they are 3–8, 16–18, 28–30 30–35 and 50 Ω-cm.

The remainder of the method of the present invention follows conventional practice as shown in FIGS. **3***h* and **3***i* with the deposition of an interlayer insulating layer **44**, herein silicon oxide from a source of tetraethylothosilcate (TEOS) or alternatively tetramethylcyclotetrasiloxane (TMCTS), followed by planarization using preferably chemcial/mechanical polish with a commercially available slurry. Contact opening **45** are plasma etched, using an reactive ion etcher with carbon tetraflouride/hydrogen, in the insulating layer **44** as shown in FIG. **3***h* and filled with a conductive material **46**, herein tungsten, as shown in FIG. **3***i*.

Although this description of silicidation method of the present invention has focused on an N-type transistor, it has equal application to P-type transistors (P+/N shallow junctions) and CMOS transistors (both N+/P and P+/N shallow junctions). This silicidation method also can be used in fabricating bipolar and biCMOS transistors and has special advantages in fabricating bipolar transistors with shallow emitters as will be described in reference to FIGS. **4***a*–**4***g*.

As shown in FIG. **4***a,* a bipolar transistor is shown in a silicon substrate **50** between vertical isolating trenches **51** and N/P horizontal isolation **52**. An insulating layer **53**, herein silicon oxide, is on the surface of the silicon substrate and the layer **53** contains an opening **54** for contacting the emitter, an opening **55** for contacting the base, and an opening **56** for contacting the collector as shown in FIG. **4***a*. Alternatively, the insulating layer **53** can be a composite of an underlying pad silicon oxide layer and an upper silicon nitride layer. A refractory metal **57**, herein titanium, is selectively CVD deposited, using commercially available equipment, on the exposed emitter, base and collector

through openings **54**, **55** and **56**, respectively, to a thickness of about 300–400 Å, preferably about 400 Å, as shown in FIG. **4***b*. Now, in accordance with the present invention, a silicon containing material **58**, which silicates faster than single crystal silicon and which herein is amorphous silicon, is sputter deposited to a thickness of about 650 to 850 Å, using silicon as the target source shown in FIG. **4***c*. The substrate **50** is now subjected to a rapid thermal anneal at about 650° C. to cause the formation of titanium silicide **59**. Because silicidation takes place much faster in amorphous silicon than single crystal silicon, most of titanium silicide forms above the original surface of the silicon substrate **50** and does not encroach on the shallow emitter N+/P junction **60** as shown in FIG. **4***d*. The silicidation is followed by using a plasma etch and an etchant gas, herein carbon tetrafluroide/oxygen, to remove the unsilicided amorphous silicon without etching the titanium silicide and then the substrate is subjected to another rapid thermal anneal at about 800° C. which converts the C49 phase of the silicide **59** into a much less resistive or more conductive phase C54 of silicide **59***a* with the result being shown in FIG. **4***e*.

The remainder of the method of the present invention follows conventional practice as shown in FIGS. **4***f* and **4***g* with the deposition of an interlayer insulating layer **61**, herein silicon oxide from TEOS, followed by planarization using preferably chemcial/mechanical polish and a commercially available slurry. Contact opening **62** are etched in the silicon oxide insulating layer **61**, using anisotropic etching with carbon tetrafluoride/hydrogen as the etchant gas, as shown in FIG. **4***f*, and filled with a conductive material **63**, herein tungsten, as shown in FIG. **4***g*.

Although this invention has been described relative to specific materials, and apparatuses for depositing and etching these materials, it is not limited to the specific materials or apparatuses but only to their specific characteristics. Other materials and apparatus can be substituted for those described herein which will be well understood by those skilled in the microelectronics and semiconductor arts after appreciating the present invention.

We claim:

1. In an integrated circuit in and on a silicon substrate having an active region including a field effect transistor with a source and a drain and a gate, all of which a conductive contact is made comprising:

a single crystalline silicon substrate with a upper surface region;

a shallow junction for each of the source and drain of the transistor underlying said upper surface of the silicon substrate;

a metal silicide layer having a lower surface disposed adjacent the shallow junction of each of the source and drain in the silicon substrate and above said upper surface of the silicon substrate; and

an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the shallow junction of each of the source and drain whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of each of the source and the drain.

2. The integrated circuit of claim **1** wherein the metal silicide is titanium silicide comprising C54 phase.

3. The integrated circuit of claim **1** wherein the shallow junction is N+/P.

4. The integrated circuit of claim **1** wherein the shallow junction is P+/N.

5. The integrated circuit of claim **1** wherein said gate includes and upper surface and a silicide layer is disposed on said upper layer.

6. The integrated circuit of claim **1** wherein the depth of the shallow junction is less than about 2500 Å.

7. The integrated circuit of claim **6** wherein the depth of the N+/P shallow junction is about 1000 Å.

8. The integrated circuit of claim **6** wherein the depth of the P+/N shallow junction is about 1200 Å.

9. The integrated circuit of claim **1** wherein the metal silicide has a resistivity in the range of about 3 to 50 Ω-cm.

10. In an integrated circuit in and on a silicon substrate having an active region including a bipolar transistor with an emitter, base and collector all of which a conductive contact is made comprising:

a single crystalline silicon substrate with a upper surface region;

a shallow junction for the emitter of the transistor underlying said upper surface of the silicon substrate;

a metal silicide layer having a lower surface disposed adjacent the shallow junction of the emitter of the transistor in the silicon substrate and above said upper surface of the silicon substrate; and

an epitaxial silicon layer disposed between said upper silicon surface and said lower surface of metal silicide and adjacent the shallow junction of the emitter whereby the metal silicide does not extend below the upper silicon surface and encroach upon the shallow junction of the emitter.

11. The integrated circuit of claim **10** wherein the metal silicide is titanium silicide comprising C54 phase.

12. The integrated circuit of claim **10** wherein the metal silicide has a resistivity in the range of about 3 to 50 Ω-cm.

13. The integrated circuit of claim **10** wherein the metal silicide is disposed adjacent of the upper silicon surface at the base and collector regions.

* * * * *

Exhibit 3

US006388330B1

(12) **United States Patent**
Ngo et al.

(10) **Patent No.: US 6,388,330 B1**
(45) **Date of Patent: May 14, 2002**

(54) **LOW DIELECTRIC CONSTANT ETCH STOP LAYERS IN INTEGRATED CIRCUIT INTERCONNECTS**

(75) Inventors: **Minh Van Ngo**, Fremont; **Dawn M. Hopper**, San Jose; **Robert A. Huertas**, Hollister; **Terri J. Kitson**, San Jose, all of CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/776,012**

(22) Filed: **Feb. 1, 2001**

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52

(52) **U.S. Cl.** **257/760**; 257/758; 257/759; 257/762; 257/765

(58) **Field of Search** 438/622–624, 438/629, 631, 633, 634, 637–640, 672, 675, 687, 688, 692, 783, 791; 257/758–760, 762, 765

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,071,809 A	*	6/2000	Zhao	438/634
6,168,726 B1	*	1/2001	Li et al.	216/79
6,245,662 B1	*	6/2001	Naik et al.	438/622

FOREIGN PATENT DOCUMENTS

WO	WO 99/33102	*	7/1999

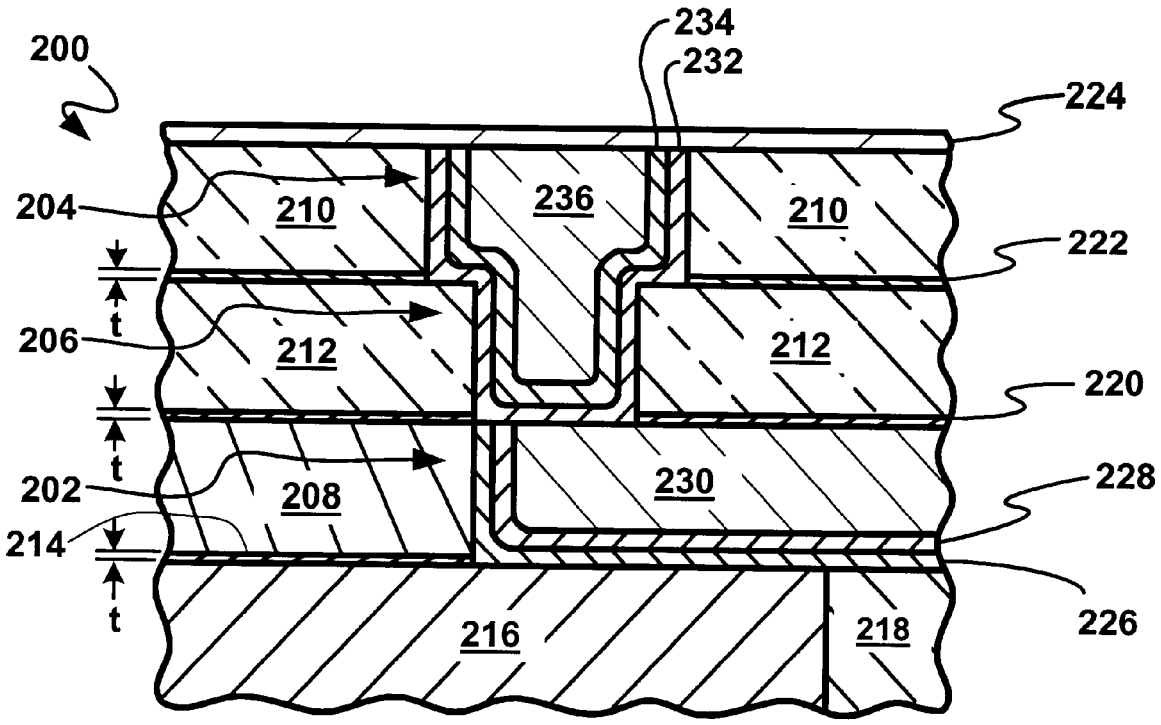
* cited by examiner

Primary Examiner—Ha Tran Nguyen
(74) *Attorney, Agent, or Firm*—Mikio Ishimaru

(57) **ABSTRACT**

An integrated circuit and method of manufacture therefore is provided having a semiconductor substrate with a semiconductor device with a dielectric layer over the semiconductor substrate. A conductor core fills the opening in the dielectric layer. An etch stop layer with a dielectric constant below 5.5 is formed over the first dielectric layer and conductor core. A second dielectric layer over the etch stop layer has an opening provided to the conductor core. A second conductor core fills the second opening and is connected to the first conductor core.

10 Claims, 2 Drawing Sheets



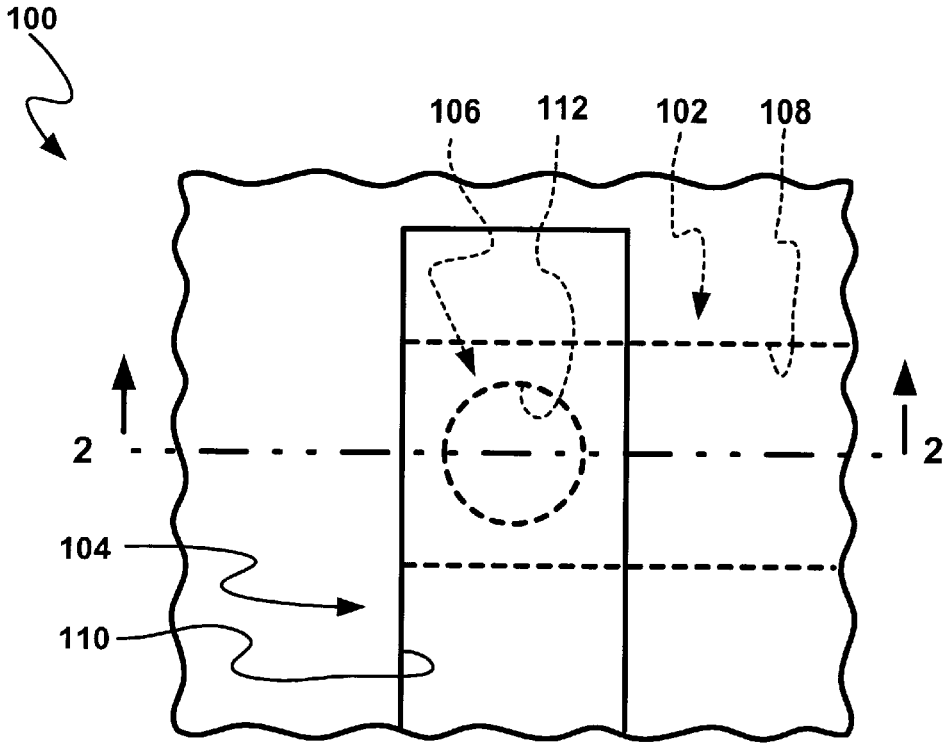


FIG. 1 (PRIOR ART)

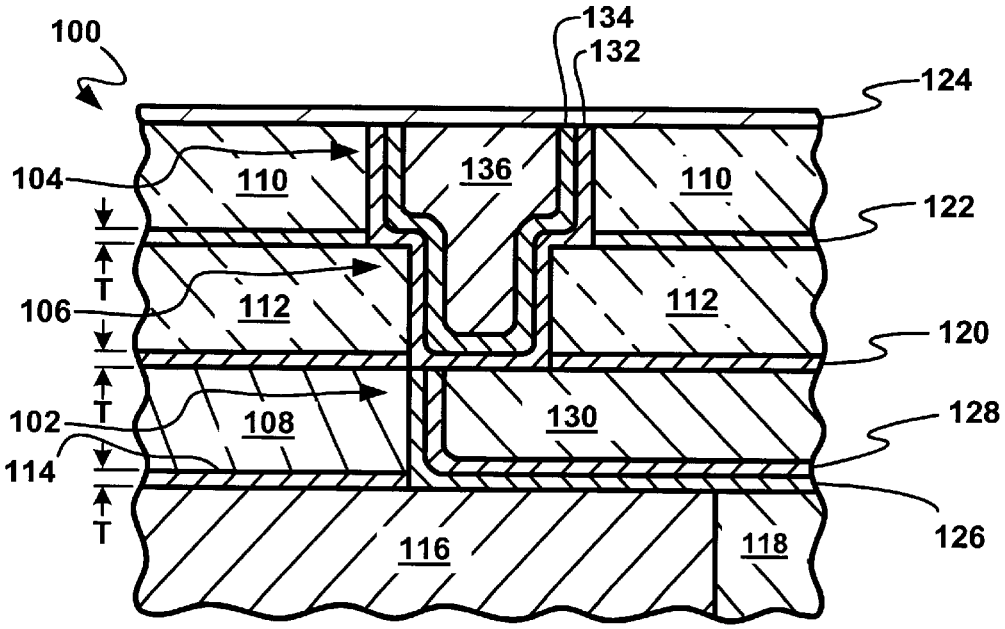


FIG. 2 (PRIOR ART)

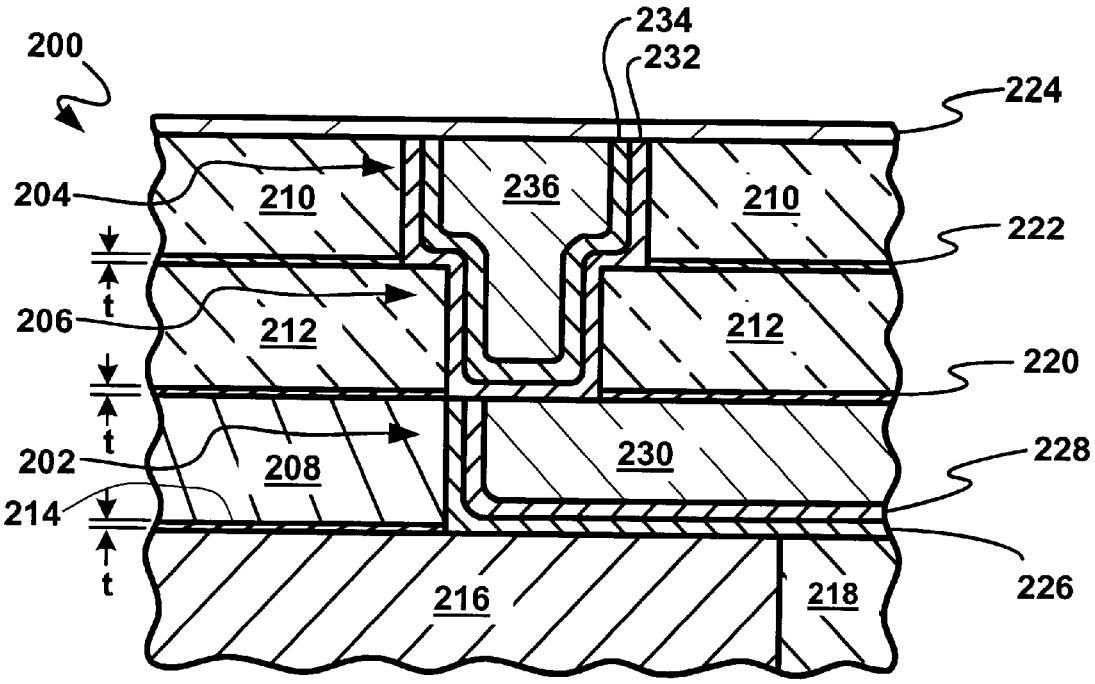

200
234
232
224
204
210
236
210
222
t
206
212
212
220
t
202
208
230
228
214
t
216
218
226

FIG. 3

LOW DIELECTRIC CONSTANT ETCH STOP LAYERS IN INTEGRATED CIRCUIT INTERCONNECTS

TECHNICAL FIELD

The present invention relates generally to semiconductor technology and more specifically to etch stop layers in integrated circuits.

BACKGROUND ART

In the manufacture of integrated circuits, after the individual devices such as the transistors have been fabricated in and on the semiconductor substrate, they must be connected together to perform the desired circuit functions. This interconnection process is generally called "metalization" and is performed using a number of different photolithographic, deposition, and removal techniques.

Briefly, individual semiconductor devices are formed in and on a semiconductor substrate and a device dielectric layer is deposited. Various techniques are used to form gate and source/drain contacts, which extend up to the surface of the device dielectric layer. In a process called the "damascene" technique, dielectric layers are deposited over the device dielectric layers and openings are formed in the dielectric layers. Conductor materials are deposited on the dielectric layers and in the openings. A process is used to planarize the conductor materials with the surface of the dielectric layers so as to cause the conductor materials to be "inlaid" in the dielectric layers.

More specifically, for a single layer of interconnections a "single damascene" technique is used in which the first channel formation of the single damascene process starts with the deposition of a thin first channel stop layer over the device dielectric layer. The first channel stop layer is an etch stop layer which is subject to a photolithographic processing step which involves deposition, patterning, exposure, and development of a photoresist, and an anisotropic etching step through the patterned photoresist to provide openings to the device contacts. The photoresist is then stripped. A first channel dielectric layer is formed on the first channel stop layer. Where the first channel dielectric layer is of an oxide material, such as silicon oxide (SiO_2), the first channel stop layer is a nitride, such as silicon nitride (SiN), so the two layers can be selectively etched.

The first channel dielectric layer is then subject to further photolithographic process and etching steps to form first channel openings in the pattern of the first channels. The photoresist is then stripped.

An optional thin adhesion layer is deposited on the first channel dielectric layer and lines the first channel openings to ensure good adhesion of subsequently deposited material to the first channel dielectric layer. Adhesion layers for copper (Cu) conductor materials are composed of compounds such as tantalum nitride (TaN), titanium nitride (TiN), or tungsten nitride (WN).

These nitride compounds have good adhesion to the dielectric materials and provide fair barrier resistance to the diffusion of copper from the copper conductor materials to the dielectric material. High barrier resistance is necessary with conductor materials such as copper to prevent diffusion of subsequently deposited copper into the dielectric layer, which can cause short circuits in the integrated circuit. However, these nitride compounds also have relatively poor adhesion to copper and relatively high electrical resistance.

Because of the drawbacks, pure refractory metals such as tantalum (Ta), titanium (Ti), or tungsten (W) are deposited

on the adhesion layer to line the adhesion layer in the first channel openings. The refractory metals are good barrier materials, have lower electrical resistance than their nitrides, and have good adhesion to copper.

In some cases, the barrier material has sufficient adhesion to the dielectric material that the adhesion layer is not required, and in other cases, the adhesion and barrier material become integral. The adhesion and barrier layers are often collectively referred to as a "barrier" layer herein.

For conductor materials such as copper, which are deposited by electroplating, a seed layer is deposited on the barrier layer and lines the barrier layer in the first channel openings to act as an electrode for the electroplating process. Processes such as electroless, physical vapor, and chemical vapor deposition are used to deposit the seed layer.

A first conductor material is deposited on the seed layer and fills the first channel opening. The first conductor material and the seed layer generally become integral, and are often collectively referred to as the conductor core when discussing the main current-carrying portion of the channels.

A chemical-mechanical polishing (CMP) process is then used to remove the first conductor material, the seed layer, and the barrier layer above the first channel dielectric layer to form the first channels. When a layer is placed over the first channels as a final layer, it is called a "capping" layer and a "single" damascene process is completed. When the layer is processed further for placement of additional channels over it, the layer is a via stop layer.

For more complex integrated circuits, a "dual damascene" technique is used in which channels of conductor materials are separated by interlayer dielectric layers in vertically separated planes and interconnected by vertical connections, or "vias".

More specifically, the dual damascene process starts with the deposition of a thin etch stop layer, or the via stop layer, over the first channels and the first channel dielectric layer. A via dielectric layer is deposited on the via stop layer. Again, where the via dielectric layer is of an oxide material, such as silicon oxide, the via stop layer is a nitride, such as silicon nitride, so the two layers can be selectively etched.

Second channel stop and second channel dielectric layers are formed on the via dielectric layer. Again, where the second channel dielectric layer is of an oxide material, such as silicon oxide, the second channel stop layer is a nitride, such as silicon nitride, so the two layers can be selectively etched. The second channel and via stop layers and second channel and via dielectric layers are then subject to further photolithographic process, etching, and photoresist removal steps to form via and second channel openings in the pattern of the second channels and the vias.

An optional thin adhesion layer is deposited on the second channel dielectric layer and lines the second channel and the via openings.

A barrier layer is then deposited on the adhesion layer and lines the adhesion layer in the second channel openings and the vias.

Again, for conductor materials such as copper and copper alloys, a seed layer is deposited by electroless deposition on the barrier layer and lines the barrier layer in the second channel openings and the vias.

A second conductor material is deposited on the seed layer and fills the second channel openings and the vias.

A CMP process is then used to remove the second conductor material, the seed layer, and the barrier layer above the second channel dielectric layer to form the second

channels. When a layer is placed over the second channels as a final layer, it is called a "capping" layer and the dual damascene process is completed.

The capping layer may be an etch stop layer and may be processed farther for placement of additional levels of channels and vias over it. Individual and multiple levels of single and dual damascene structures can be formed for single and multiple levels of channels and vias, which are collectively referred to as "interconnects".

The use of the single and dual damascene techniques eliminates metal etch and dielectric gap fill steps typically used in the metalization process. The elimination of metal etch steps is important as the semiconductor industry moves from aluminum (Al) to other metalization materials, such as copper, which are very difficult to etch.

Further for placement of additional levels of channels and vias over it. Individual and multiple levels of single and dual damascene structures can be formed for single and multiple levels of channels and vias, which are collectively referred to as "interconnects".

The use of the single and dual damascene techniques eliminates metal etch and dielectric gap fill steps typically used in the metallization process. The elimination of metal etch steps is important as the semiconductor industry moves from aluminum (Al) to other metallization materials, such as copper, which are very difficult to etch.

With the development of high integration and high-density very large scale integrated circuits, reductions in the size of transistors and interconnects have been accompanied by increases in switching speed of such integrated circuits. The closeness of the interconnects and the higher switching speeds have increased the problems due to switching slow-downs resulting from capacitance coupling effects between the closely positioned, parallel conductive channels connecting high switching speed semiconductor devices in these integrated circuits. Since the capacitance coupling effects are reduced when the dielectric constant of the material between the channels is reduced, this has rendered currently used silicon nitride, which has a dielectric constant in excess of 7.5, problematic for protective dielectric layers, such as etch stop layers.

A solution for reducing the dielectric constant of the materials used in interconnects has been long sought but has eluded those skilled in the art. In this area, even small reductions in the dielectric constant are significant.

DISCLOSURE OF THE INVENTION

The present invention provides an integrated circuit having a semiconductor substrate with a semiconductor device. A dielectric layer is on the semiconductor substrate and has an opening provided therein. A conductor core fills the opening and an etch stop layer over the first dielectric layer and conductor core has a dielectric constant below 5.5. A second dielectric layer over the etch stop layer has an opening provided to the conductor core. A second conductor core fills the second opening and is connected to the first conductor core. The resulting integrated circuit has reduced capacitive coupling effects and is able to operate at higher speeds.

The present invention further provides a method for manufacturing an integrated circuit having a semiconductor substrate with a semiconductor device. A dielectric layer is formed on the semiconductor substrate and an opening is formed in the dielectric layer. A conductor core is deposited to fill the opening and an etch stop layer with a dielectric constant below 5.5 is formed over the first dielectric layer and conductor core. A second dielectric layer is deposited over the etch stop layer and a second opening is formed. A second conductor core is deposited to fill the second opening. The method allows the integrated circuit to have a denser etch stop layer and results in a reduced dielectric constant for the interlayer dielectric layers as a whole.

The above and additional advantages of the present invention will become apparent to those skilled in the art from a reading of the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** (PRIOR ART) is a plan view of aligned channels with a connecting via;

FIG. **2** (PRIOR ART) is a cross-section of FIG. **1** (PRIOR ART) along line **2**—**2**; and

FIG. **3** is a cross-section, similar to FIG. **2** (PRIOR ART), showing the etch stop layer according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to FIG. **1** (PRIOR ART), therein is shown a plan view of a semiconductor wafer **100** with a silicon semiconductor substrate (not shown) having as interconnects first and second channels **102** and **104** connected by a via **106**. The first and second channels **102** and **104** are respectively disposed in first and second channel dielectric layers **108** and **110**. The via **106** is an integral part of the second channel **104** and is disposed in a via dielectric layer **112**.

The term "horizontal" as used in herein is defined as a plane parallel to the conventional plane or surface of a wafer, such as the semiconductor wafer **100**, regardless of the orientation of the wafer. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

Referring now to FIG. **2** (PRIOR ART), therein is shown a cross-section of FIG. **1** (PRIOR ART) along line **2**—**2**. A portion of the first channel **102** is disposed in a first channel stop layer **114** and is on a device dielectric layer **116**, which is on the silicon semiconductor substrate. Generally, metal contacts are formed in the device dielectric layer **116** to connect to an operative semiconductor device (not shown). This is represented by the contact of the first channel **102** with a semiconductor contact **118** embedded in the device dielectric layer **116**. The various layers above the device dielectric layer **116** are sequentially: the first channel stop layer **114**, the first channel dielectric layer **108**, a via stop layer **120**, the via dielectric layer **112**, a second channel stop layer **122**, the second channel dielectric layer **110**, and a capping or next channel stop layer **124** (not shown in FIG. **1**).

The first channel **102** includes a barrier layer **126**, which could optionally be a combined adhesion and barrier layer, and a seed layer **128** around a conductor core **130**. The second channel **104** and the via **106** include a barrier layer **132**, which could also optionally be a combined adhesion and barrier layer, and a seed layer **134** around a conductor core **136**. The barrier layers **126** and **132** are used to prevent diffusion of the conductor materials into the adjacent areas of the semiconductor device. The seed layers **128** and **134** form electrodes on which the conductor material of the

conductor cores **130** and **136** are deposited. The seed layers **128** and **134** are of substantially the same conductor material as the conductor cores **130** and **136** and become part of the respective conductor cores **130** and **136** after the deposition.

In the past, for copper conductor material and seed layers, highly resistive diffusion barrier materials such as tantalum nitride (TaN), titanium nitride (TiN), or tungsten nitride (WN) are used as barrier materials to prevent diffusion.

The first channel stop layer **114**, the via stop layer **120**, and the second channel stop layer **122** are used as layers to stop the etching process which are used to etch and make the various channel and via openings in the respective first channel dielectric layer **108**, the via dielectric layer **112**, and the second channel dielectric layer **110**. The stop layers are of a dielectric material deposited to a thickness "T" by a 500-watt plasma deposition process in an ammonia (NH_3) atmosphere at 4.8 torr pressure. Generally, the stop layer material is silicon nitride (SiN, Si_xN_y), which has a dielectric constant above 7.5 and which is deposited to a thickness "T" from 470 Å to 530 Å.

Referring now to FIG. **3**, therein is shown a cross-section similar to that shown in FIG. **2** (PRIOR ART) of a semiconductor wafer **200** of the present invention. The semiconductor wafer **200** has first and second channels **202** and **204** connected by a via **206**. The first and second channels **202** and **204** are respectively disposed in first and second dielectric layers **208** and **210**. The via **206** is a part of the second channel **204** and is disposed in a via dielectric layer **212**.

A portion of the first channel **202** is disposed in a first channel stop layer **214** and is on a device dielectric layer **216**. Generally, metal contacts (not shown) are formed in the device dielectric layer **216** to connect to an operative semiconductor device (not shown). This is represented by the contact of the first channel **202** with a semiconductor device gate **218** embedded in the device dielectric layer **216**. The various layers above the device dielectric layer **216** are sequentially: the first channel stop layer **214**, the first channel dielectric layer **208**, a via stop layer **220**, the via dielectric layer **212**, a second channel stop layer **222**, the second channel dielectric layer **210**, and a next channel stop layer **224**.

The first channel **202** includes a barrier layer **226** and a seed layer **228** around a conductor core **230**. The second channel **204** and the via **206** include a barrier layer **232** and a seed layer **234** around a conductor core **236**. The barrier layers **226** and **232** are used to prevent diffusion of the conductor materials into the adjacent areas of the semiconductor device. The seed layers **228** and **234** form electrodes on which the conductor material of the conductor cores **230** and **236** is deposited. The seed layers **228** and **234** are of substantially the same conductor material of the conductor cores **230** and **236** and become part of the respective conductor cores **230** and **236** after the deposition.

The first channel stop layer **214**, the via stop layer **220**, and the second channel stop layer **222** are used as layers to stop the etching process which are used to etch and make the various channel and via openings in the respective first channel dielectric layer **208**, the via dielectric layer **212**, and the second channel dielectric layer **210**.

In the present invention, a half thickness, high quality, etch stop layer (compared to the prior art etch stop layer) is deposited.

For example, for silicon nitride, the dielectric constant of an etch stop layer in accordance with the present invention is about 5.5 contrasted to an excess of 7.5 in the prior art.

It has been determined that a number of processes can be used to produce the under 5.5 dielectric constant etch stop layers which are in a thickness "t" as shown in FIG. **3**, where the thickness "t" is from 270 Å to 330 Å thick.

First, multi-layer depositions may be used which eliminates pinholes and produces a denser film. For example, silicon nitride can be deposited in six 50 Å layers, either by successive deposition or by successive deposition and rotation between each deposition of a layer.

Second, for silicon nitride where silane (SiH_4) is used with ammonia (NH_3), the gas flow can be reduced and the pressure can be increased. For example, silicon nitride is formed in a plasma process using silane at a flow rate of 170 to 290 sccm and ammonia at a flow rate of 40 to 48 sccm and under a pressure of 4.0 to 4.8 torr

Third, the silane flow may be reduced to about 50% of the prior art flow with increased pressure and nitrogen (N_2) can be used in place of the ammonia to reduce hydrogen (H_2). For example, silicon nitride is formed in a plasma process using silane at a flow rate of 170 to 290 sccm and nitrogen at a flow rate of 4700 to 6700 sccm and under a pressure of 4.0 to 4.8 torr.

Fourth, a 500 Å thick layer of silicon nitride can be deposited and then densified, for example, at a temperature of 450° C. to 480° C. for up to one hour.

With the reduced dielectric constant and the reduced thickness, the capacitive coupling effect between the first and second channels **202** and **204** is effectively reduced over 25% compared to the prior art.

In various embodiments, the barrier layers are of materials such as tantalum (Ta), titanium (Ti), tungsten (W), compounds thereof, and combinations thereof. The seed layers (where used) are of materials such as copper (Cu), gold (Au), silver (Ag), compounds thereof to and combinations thereof with one or more of the above elements. The conductor cores with or without seed layers are of materials such as copper, aluminum (Al), gold, silver, compounds thereof, and combinations thereof. The dielectric layers are of dielectric materials such as silicon oxide (SiO_x), tetraethoxysilane (TEOS), borophosphosilicate (BPSG) glass, etc. with dielectric constants from 4.2 to 3.9 or low dielectric constant dielectric materials such as fluorinated tetraethoxysilane (FTEOS), hydrogen silsesquioxane (HSQ), benzocyclobutene (BCB), etc. with dielectric constants below 3.9.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters hitherto-fore set forth or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

The invention claimed is:

1. An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;

a first conductor core filling the first opening and connected to the semiconductor device;

an etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the etch stop layer having a dielectric constant below 5.5;

a second dielectric layer formed over the etch stop layer and having a second opening provided therein open to the first conductor core;

a second conductor core filling the second opening and connected to the first conductor core.

2. The integrated circuit as claimed in claim **1** wherein the etch stop layer is a multilayer structure.

3. The integrated circuit as claimed in claim **1** wherein the etch stop layer is a multilayer structure with each of the layers having a different layer orientation.

4. The integrated circuit as claimed in claim **1** wherein the first and second dielectric layers are of a material having a dielectric constant under 3.9.

5. The integrated circuit as claimed in claim **1** wherein the conductor core contains a material selected from a group consisting of copper, aluminum, gold, silver, a compound thereof, and a combination thereof.

6. An integrated circuit comprising:

a semiconductor substrate having a semiconductor device provided thereon;

a first dielectric layer formed over the semiconductor substrate having a first opening provided therein;

a first conductor core filling the first opening and connected to the semiconductor device;

a via etch stop layer of silicon nitride formed over the first dielectric layer and the first conductor core, the via etch stop layer having a dielectric constant below 5.5;

a via dielectric layer formed over the via etch stop layer and having a via opening provided therein open to the first conductor core;

a channel etch stop layer of silicon nitride formed over the via dielectric layer, the channel etch stop layer having a dielectric constant below 5.5;

a second dielectric layer formed over the via dielectric layer and having a second opening provided therein open to the via opening; and

a second conductor core filling the via and second openings and connected to the first conductor core.

7. The integrated circuit as claimed in claim **6** wherein the via and channel etch stop layers are a multilayer structure.

8. The integrated circuit as claimed in claim **6** wherein the via and channel etch stop layers are multilayer structures with each of the layers having a different layer orientation.

9. The integrated circuit as claimed in claim **6** wherein the first, via, and second dielectric layers are of a material having a dielectric constant under 3.9.

10. The integrated circuit as claimed in claim **6** wherein the first and second conductor cores contain materials selected from a group consisting of copper, gold, silver, a compound thereof, and a combination thereof.

* * * * *