

IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION

AIDO LLC

Plaintiff,

V.

RENASAS ELECTRONICS AMERICA INC.

Defendant.

)  
)  
)  
) C.A. No. 6:20-cv-00022  
)  
) **JURY TRIAL DEMANDED**

## COMPLAINT

For its Complaint, Plaintiff Aido LLC ("Aido"), by and through the undersigned counsel, alleges as follows:

## THE PARTIES

1. Aido is a Texas limited liability company with a place of business located at 312 W. 8th Street, Dallas, Texas 75208.

2. Defendant Renesas Electronics America Inc. is a California company, with, upon information and belief, a place of business located in Austin, Texas.

## **JURISDICTION AND VENUE**

3. This action arises under the Patent Act, 35 U.S.C. § 1 *et seq.*

4. Subject matter jurisdiction is proper in this Court under 28 U.S.C. §§ 1331 and 1338.

5. Upon information and belief, Defendant conducts substantial business in this forum, directly or through intermediaries, including: (i) at least a portion of the infringements alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals

in this district.

6. Venue is proper in this district pursuant to § 1400(b).

**THE PATENT-IN-SUIT**

7. On August 19, 2003, U.S. Patent No. 6,609,169 (the "'169 patent"), entitled "Solid-State Audio-Video Playback System," was duly and lawfully issued by the U.S. Patent and Trademark Office. A true and correct copy of the '169 patent is attached hereto as Exhibit A.

8. Aido is the assignee and owner of the right, title and interest in and to the '169 patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of them.

**COUNT I – INFRINGEMENT OF U.S. PATENT NO. 6,609,169**

9. Aido repeats and realleges the allegations of paragraphs 1 through 8 as if fully set forth herein.

10. Without license or authorization and in violation of 35 U.S.C. § 271(a), Defendant has infringed and continues to infringe at least claims 1 and 6 of the '169 patent by making, using, importing, offering for sale, and/or selling electronic memory playback system for reading and playing back electronically stored audio and/or video, including, but not limited to, SH7262 and SH7264 SuperH Microcontrollers (collectively, the "Accused Devices"), because each and every element is met either literally or equivalently.

11. More specifically and upon information and belief, the Accused Devices are an electronic memory playback system for reading and playing back electronically stored audio and/or video data.

**Renesas Technology Releases SH7262 and SH7264 SuperH™ Microcontrollers with 1 Mbyte On-Chip SRAM for Digital Audio and Graphical Dashboard Applications**

— Support for WQVGA-size TFT LCD panel display without external SDRAM; largely single-chip implementation of midrange or low-end systems —

Tokyo, May 12, 2008 — Renesas Technology Corp. today announced a total of eight new product versions of the SH7262 and SH7264 high-performance 32-bit microcontrollers with 1 Mbyte of on-chip SRAM for digital audio and graphical dashboard applications. Sample shipments will begin in August 2008 in Japan.

<http://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=2ahUKEwj20u->

[mqIbmAhWOsJ4KHd2HCiYQFjAAegQIAxAC&url=http%3A%2F%2Fwww.koryo.com.tw%2](http://www.koryo.com.tw/%2Fimages/%2Feniglish/%2F20080512e.pdf&usg=AOvVaw3LBBrXxyXedFXXiDIFLBOG)

[Fe%2Fimages/%2Feniglish/%2F20080512e.pdf&usg=AOvVaw3LBBrXxyXedFXXiDIFLBOG](http://www.koryo.com.tw/%2Fimages/%2Feniglish/%2F20080512e.pdf&usg=AOvVaw3LBBrXxyXedFXXiDIFLBOG)

("Press Release).

- Also implemented on-chip are a USB 2.0 Hi-Speed specification host/function interface and a new video display controller supporting graphical and video display capabilities. When combined with video input functionality, it enables the development of a digital audio system that allows connection with a USB device, such as USB flash memory or a portable audio player, and uses high-speed data transfer to perform video and audio playback. The video display controller can also be used to display menus on the LCD panel of an AV component.

*Id.*

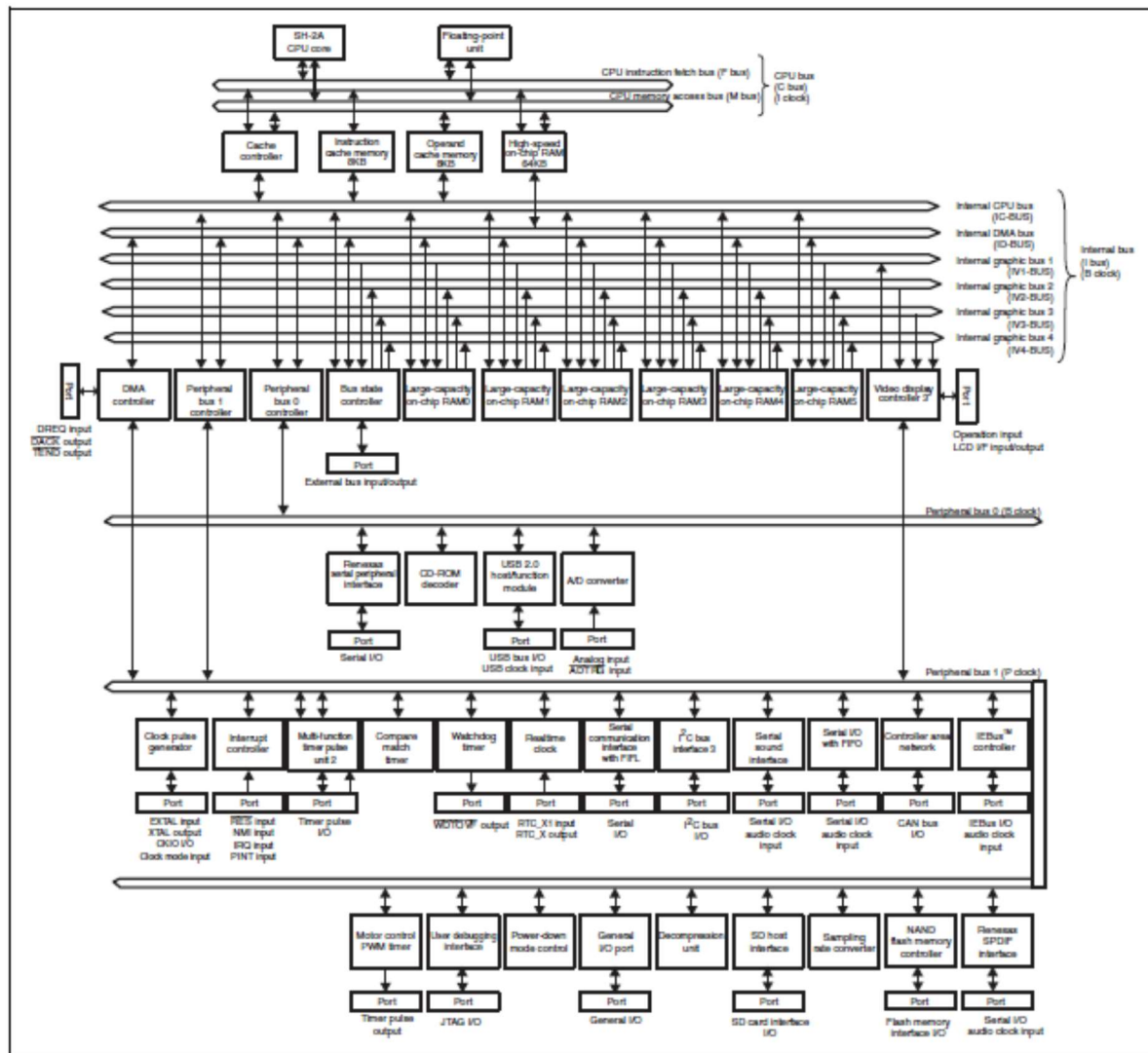
The SH7262 comes in a 176-pin QFP package and the SH7264 in a lead-free 208-pin QFP package. Both have an on-chip debugging function\*<sup>5</sup> that enables realtime debugging at the maximum operating frequency. The E10A-USB emulator, which uses USB bus power and requires no external power supply, is available as a development environment. Renesas Technology supplies middleware with support for digital audio compression standards such as MP3, WMA, and AAC, and it is possible to build a system with multi-codec compatibility. There is also software that supports the ISO 9660 file system used by CD-ROMs and the FAT32 file system used by hard disk drives. These software solutions are intended to facilitate the development of digital audio products.

Future SH7260 Series microcontrollers for the high-end market will include multi-core products offering improved performance, expanded on-chip memory, and enhanced peripheral functions such as advanced display capabilities. Alongside these products offering more speed, better performance, and higher functionality, Renesas Technology will continue to respond to market demand with low-cost products for use in low-end systems.

*Id.*

12. The Accused Devices include a plurality of memory modules for electronically storing audio and/or video, a plurality of module packs daisy chained together, each of said module packs including a plurality of receptacles for receiving said plurality of memory modules, and a module player coupled to said at least one module pack.

### 1.3 Block Diagram



<https://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=2&cad=rja&uact=8&ved=2ahUKEwj20u-mqIbmAhWOsJ4KHd2HCiYQFjABegQIAhAB&url=https%3A%2F%2Fwww.datasheetarchive.com%2FSH7262-datasheet.html&usg=AOvVaw34EzvOvZLrQHm7JmsZSTpj> ("Manual") at p. 14 of 2108.



**Table 31.2 Address Spaces of On-Chip Large-Capacity RAM (1-Mbyte Version)**

<b>Page</b>	<b>Cache-enabled Address</b>	<b>Cache-disabled Address</b>
Page 0 (160 Kbytes)	H'1C000000 to H'1C027FFF	H'3C000000 to H'3C027FFF
Page 1 (80 Kbytes)	H'1C028000 to H'1C03BFFF	H'3C028000 to H'3C03BFFF
Page 2 (80 Kbytes)	H'1C03C000 to H'1C04FFFF	H'3C03C000 to H'3C04FFFF
Page 3 (160 Kbytes)	H'1C050000 to H'1C077FFF	H'3C050000 to H'3C077FFF
Page 4 (240 Kbytes)	H'1C078000 to H'1C0B3FFF	H'3C078000 to H'3C0B3FFF
Page 5 (304 Kbytes)	H'1C0B4000 to H'1C0FFFFF	H'3C0B4000 to H'3C0FFFFF

**Table 31.3 Address Spaces of On-Chip Data Retention RAM (1-Mbyte Version)**

<b>Page</b>	<b>Cache-enabled Address</b>	<b>Cache-disabled Address</b>
Page 0 (16 Kbytes)	H'1C0F8000 to H'1C0FBFFF	H'3C0F8000 to H'3C0FBFFF
Page 1 (16 Kbytes)	H'1C0FC000 to H'1C0FFFFF	H'3C0FC000 to H'3C0FFFFF

**Table 31.4 Address Spaces of On-Chip Large-Capacity RAM (640-Kbyte Version)**

<b>Page</b>	<b>Cache-enabled Address</b>	<b>Cache-disabled Address</b>
Page 0 (160 Kbytes)	H'1C000000 to H'1C027FFF	H'3C000000 to H'3C027FFF
Page 1 (80 Kbytes)	H'1C028000 to H'1C03BFFF	H'3C028000 to H'3C03BFFF
Page 2 (80 Kbytes)	H'1C03C000 to H'1C04FFFF	H'3C03C000 to H'3C04FFFF
Page 3 (160 Kbytes)	H'1C050000 to H'1C077FFF	H'3C050000 to H'3C077FFF
Page 4 (160 Kbytes)	H'1C078000 to H'1C09FFFF	H'3C078000 to H'3C09FFFF

**Table 31.5 Address Spaces of On-Chip Data Retention RAM (640-Kbyte Version)**

<b>Page</b>	<b>Cache-enabled Address</b>	<b>Cache-disabled Address</b>
Page 0 (16 Kbytes)	H'1C000000 to H'1C003FFF	H'3C000000 to H'3C003FFF
Page 1 (16 Kbytes)	H'1C004000 to H'1C007FFF	H'3C004000 to H'3C007FFF
Page 2 (128 Kbytes)	H'1C008000 to H'1C027FFF	H'3C008000 to H'3C027FFF
Page 3 (160 Kbytes)	H'1C028000 to H'1C04FFFF	H'3C028000 to H'3C04FFFF

*Id.* at p. 1672 of 2108.

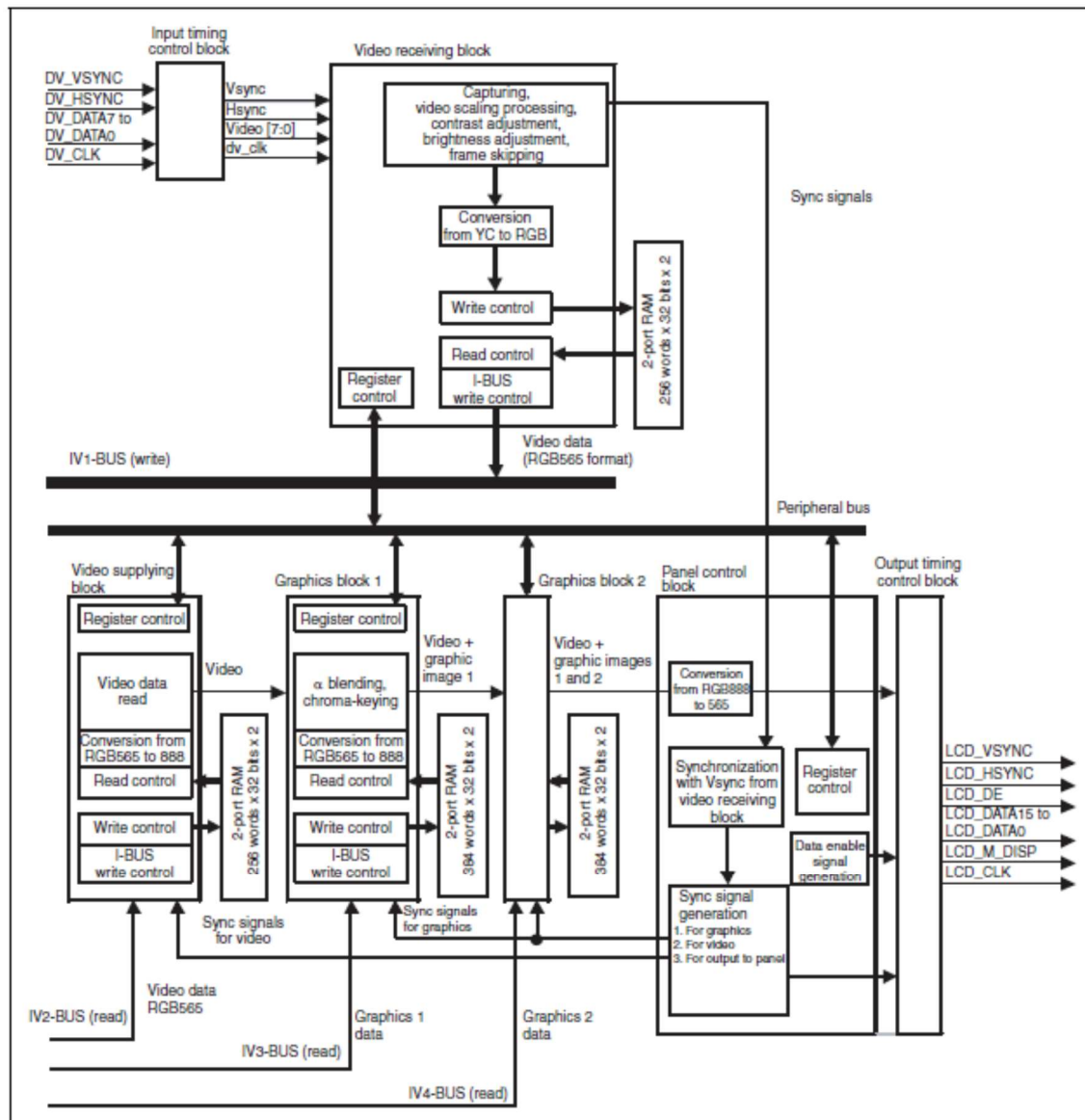


Figure 27.1 Block Diagram

*Id.* at p. 1551 of 2108.

13. The module player coupled to said at least one module pack reads the memory modules stored in the at least one memory module pack and plays back electronically stored audio and/or video data.

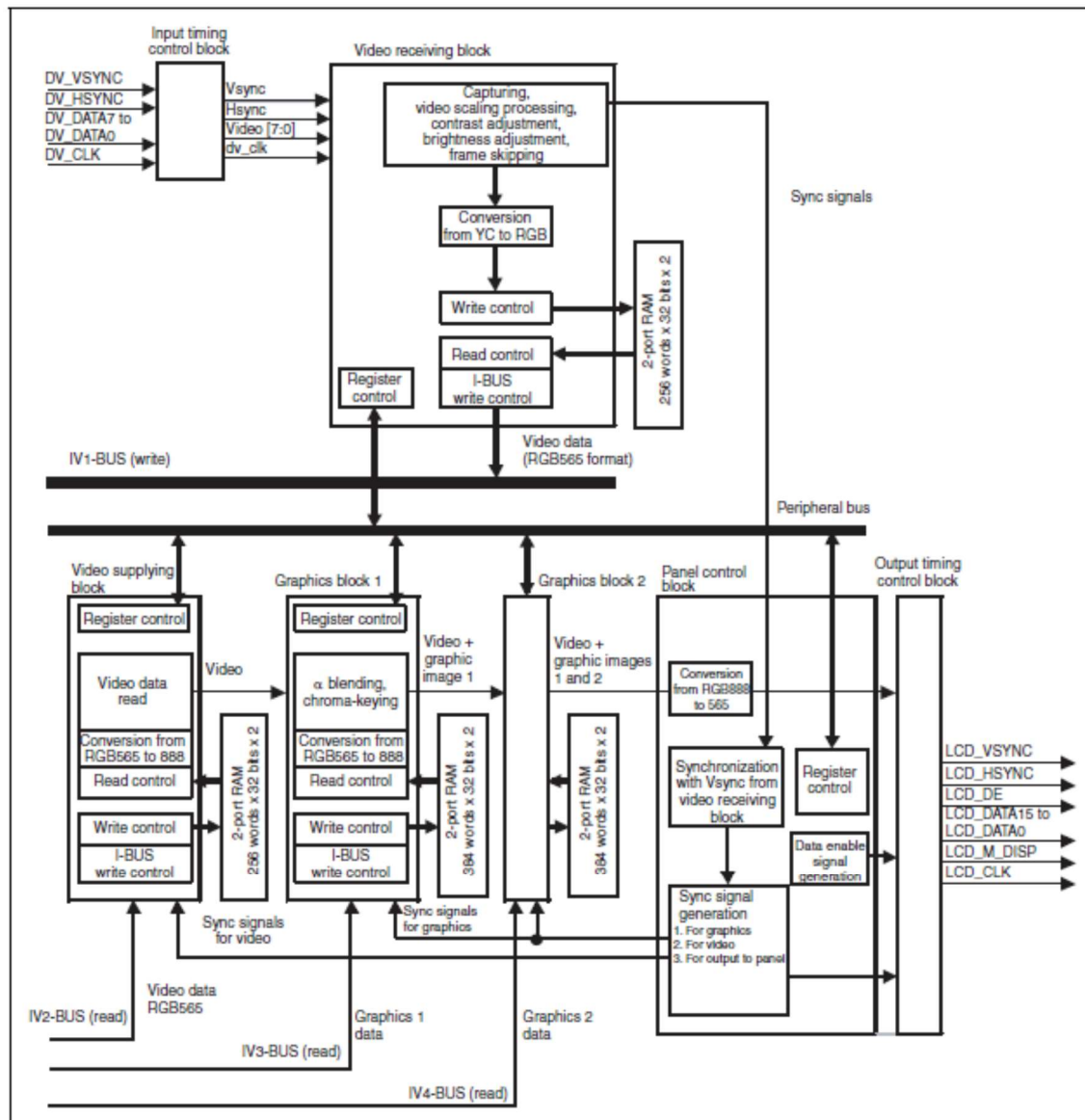


Figure 27.1 Block Diagram

*Id.*

14. The Accused Devices include a data bus included in the at least one module pack for coupling the plurality of memory modules received by receptacles to the memory module player, and the data bus includes a segmented input bus and a continuous output bus.



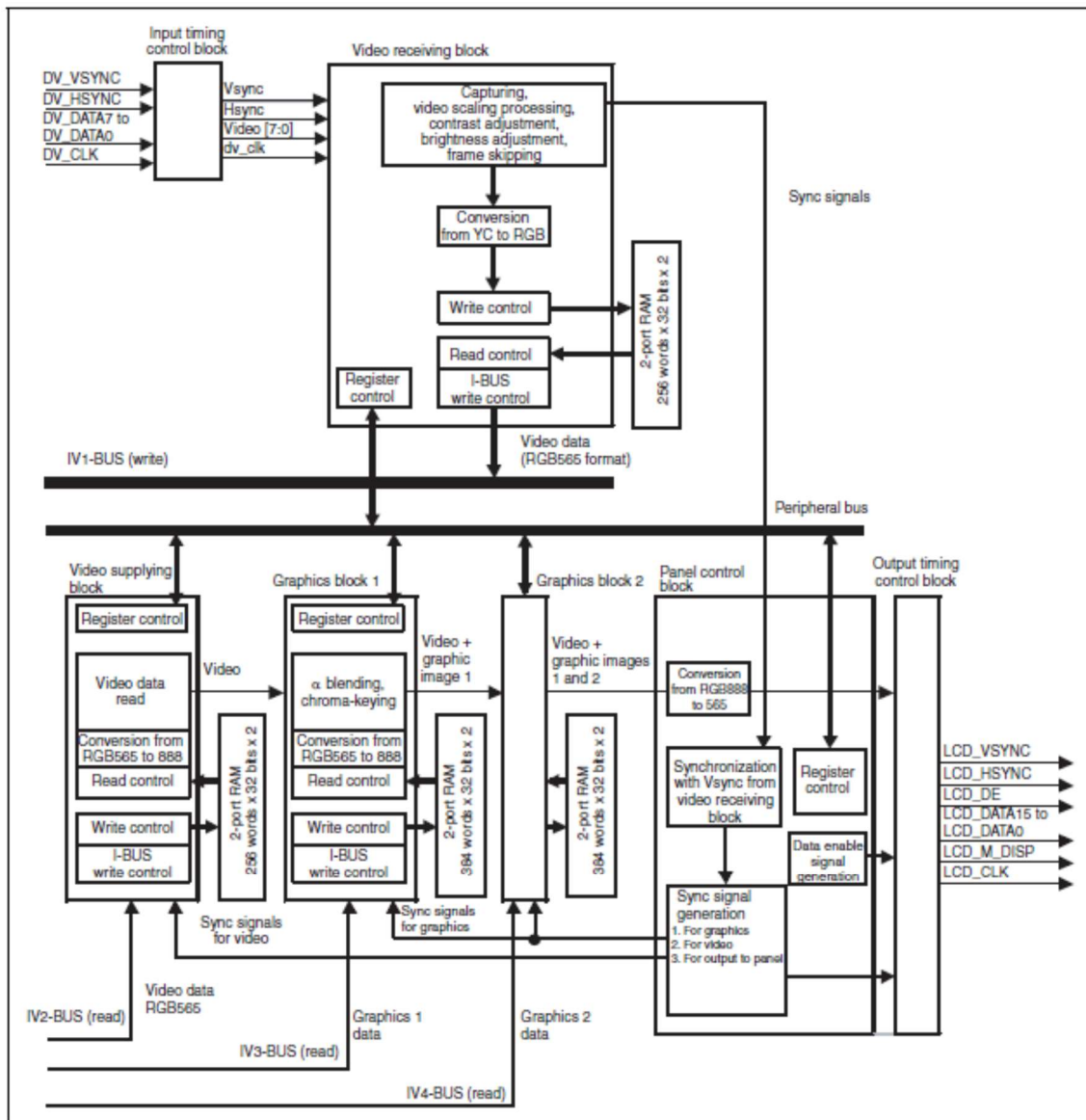
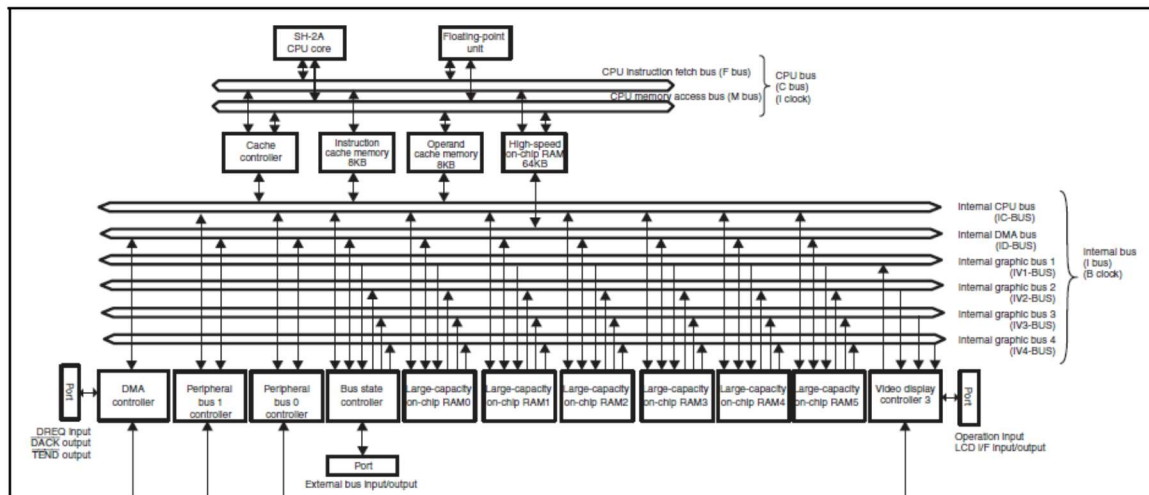


Figure 27.1 Block Diagram

Id.

### 1.3 Block Diagram



*Id.* at p. 14 of 2108.

15. Aido is entitled to recover from Defendant the damages sustained by Aido as a result of Defendant's infringement of the '169 patent in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

### **JURY DEMAND**

Aido hereby demands a trial by jury on all issues so triable.

### **PRAYER FOR RELIEF**

WHEREFORE, Aido requests that this Court enter judgment against Defendant as follows:

- A. An adjudication that Defendant has infringed the patent;
- B. A judgment that Defendant has induced infringement of the '169 patent;
- C. An award of damages to be paid by Defendant adequate to compensate Aido for Defendant's past infringement of the '169 patent and any continuing or future infringement

through the date such judgment is entered, including interest, costs, expenses and an accounting of all infringing acts including, but not limited to, those acts not presented at trial;

D. A declaration that this case is exceptional under 35 U.S.C. § 285, and an award of Aido's reasonable attorneys' fees; and

E. An award to Aido of such further relief at law or in equity as the Court deems just and proper.

Dated: January 14, 2020

Respectfully submitted,

/s/ Raymond W. Mort, III

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