IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff -against- VIA TECHNOLOGIES, INC. Defendant	**Case No.: 6:20-cv-00043** **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO"), for its Complaint against Defendant Via Technologies, Inc. (collectively "Via" or "Defendant"), hereby alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. Via Technologies, Inc. is a Taiwan corporation with its principal place of business at 8F, No. 533, Zhongzheng Rd., Xindian District, New Taipei City 231, Taiwan.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Via of claims of U.S. Patent Nos. 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. Via is subject to personal jurisdiction of this Court because, inter alia, on information and belief (i) Via sells and offers for sale its products in Texas, (ii) Via sells and offers for sale its

products by using distributors and sales representatives located in Texas; (iii) Via places its products in the stream of commers with intent or knowledge that those products would end up in Texas; (iv) Via recruits Texas residents; and (v) Via contracts with a Texas resident, such as for leasing real property, with the performance occurring in Texas. In addition, or in the alternative, this Court has personal jurisdiction over Via pursuant to Fed. R. Civ. P. 4(k)(2).

6. Venue is proper in this district under 28 U.S.C. § 1391(c) because Via is a foreign entity.

BACKGROUND

7. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

8. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

9. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

10. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

11. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

12. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

13. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration

Using Memory Bank Readiness."

14. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

15. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

16. By letter dated May 22, 2019, CCO notified Via of the existence of the Patents-in-Suit, and of infringement the Patents-in-Suit by Via. CCO's letter identified exemplary infringing Via products and an exemplary infringed claim for each of the '234, '386, '069, and '603 Patents. CCO's May 22, 2019 letter invited Via to hold a licensing discussion with CCO. Via received the May 22, 2019 letter on May 31, 2019. CCO received no response to the May 22, 2019 Letter.

17. By email dated October 18, 2019, CCO followed up with Via's CEO regarding the May 22, 2019 letter and attaching its copy. CCO received no response to the October 18, 2019 email.

LICENSING

18. As of the time of this complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, and Qualcomm.

COUNT I: INFRINGEMENT OF THE '234 PATENT

19. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

20. On information and belief, Via has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States processors, chipsets, and systems identified in Attachment 1 ("Accused Via Products").

21. For example, on information and belief, Via has infringed at least claim 28 of the '234

Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Via Products that include Via's DDR Controller with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Via Products and specifically the DDR Controller. Ex. 1, VIA System Programming Manual, VX900 Series All-in-One System Processor, p. 134. An exemplary DDR Controller reduces timing uncertainty in DDR3 memory transmission including calibration using the Mode Register Commands, read centering, write centering, and write leveling. *See* Ex. 1 at 135-137, Ex. 2, JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008, p. 17, 48-51. The DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of input and outputs. Ex. 1 at 134. The DDR Controller further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. *Id.* The DDR Controller DMCs include a main clock for generating a main clock signal (such as the DCLK DLL). *See id*. at 134. The DDR Controller includes a reference clock, such as a reference clock from the DLL, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training. The reference clock is associated with the main clock signal. *See id.* at 135-36. The DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the DCLK signal at the destination. For example, the phase shift circuitry aligns the timing of the DQS signals following write leveling. *See* Ex. 2. at 42-43 ("The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification").

22. On information and belief, Via has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing,

causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Via Products that incorporate the DDR Controller. Via had the knowledge of the '234 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Via Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

23. On information and belief, Via has committed the foregoing infringing activities without a license.

24. On information and belief, Via's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

25. On information and belief, Via knew the '234 Patent existed, knew of an exemplary infringed claim of the '234 Patent, and knew of exemplary infringing Via products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT II: INFRINGEMENT OF THE '386 PATENT

26. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

27. On information and belief, Via has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Via Products.

28. For example, on information and belief, Via has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused Via Products, which include a DDR Controller, adapted to send a plurality of

memory transactions over a memory bus to a memory having a plurality of memory banks. *See, e.g.*, Ex. 1 at 101-102. Exemplary DDR Memory to which the DDR Controller connects has multiple memory banks. *See id*. at 104. *See* e.g., Ex. 2, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The Accused Via Products send the requests over a memory bus. Ex. 1 at 122-123 ("The DRAM controller will send the current write requests to the DRAM bus."). The DDR Controller comprises a queue comprising a plurality of request stations for storing memory transactions. Ex. 1 at 122. Each of the memory transactions is addressed to one of the memory banks. *See* Ex. 2 at 33. The DDR Controller includes an arbiter, such as, for example, DRAM Command Scheduler. *See* Ex. 1 at 122. The arbiter is simultaneously coupled to each of the request stations and adapted to select any of the memory transactions. *See id.* The arbiter is configured to generate a plurality of bank readiness signals, such as following the submission of an activate command to the DDR3 memory. *See* Ex. 2 at 18, 55; Ex. 1 at 178-180. The DDR Controller, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *See* Ex. 1 at 18.

29. On information and belief, Via has induced, and continues to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Via Products. Via had the knowledge of the '386 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Via Products, corresponding technical documentation, and

assisting customers with integrating, testing, and verification thereof.

30. On information and belief, Via has committed the foregoing infringing activities without a license.

31. On information and belief, Via's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

32. Via knew the '386 Patent existed, knew of its claims, and knew of Via infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT III: INFRINGEMENT OF THE '069 PATENT

33. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

34. On information and belief, Via has infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Via Products.

35. For example, on information and belief, Via has infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and verification of the Accused Via Products, which include the DDR Controller, such as a DDR3 memory controller that automatically calibrates skew of DDR3. *See* Ex. 1 at 134, 137; Ex. 2 at 17, 27. The DDR Controller initiates Write Leveling and Read Optimization via the Circuit Macro. *See* Ex. 1 at 134. The Circuit Macro comprises a transmitter and the receiver. *Id.* Via calibrates registers of the receiver, such as the Circuit Macro registers in relation to a reference clock edge, such as a reference clock used in RX capture calibration. *See* Ex. 1 at 134, 136. *See also* Ex. 2 at 13. Via calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver with the Write Leveling feature. *See* Ex. 2 at 186 ("The

memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus."); Ex. 2 at 42. The calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS - DQS# and CK -CK# signals. The calibration is performed for a plurality of data patterns, such as DQS – DQS# patterns with variable delays. Ex. 2 at 42. ("The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification"). Via applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See id.*

36. On information and belief, Via has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Via Products that incorporate the DDR Controller. Via had the knowledge of the '069 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Via Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

37. On information and belief, Via has committed the foregoing infringing activities without a license.

38. On information and belief, Via's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

39. On information and belief, Via knew the '069 Patent existed, knew of an exemplary infringed claim of the '069 Patent, and knew of exemplary infringing Via products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT IV: INFRINGEMENT OF THE '603 PATENT

40. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

41. On information and belief, Via has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Via Products.

42. For example, on information and belief, Via has infringed at least claim 14 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of the Accused Via Products. The DDR Controller of the Accused Via Products use a multiplexer. *See* Ex. 1 at 101. Memory to which the Accused Via Products connect has multiple memory banks. *See id*. at 104. *See* e.g., Ex. 2, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The multiplexer used by the DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions, such as the inputs from V4IF, GMINT, VMINT. *See* Ex. 1 at 101, 122. The multiplexer also comprises a multiplexer output for sending each of the plurality of memory transactions to the memory, such as the interface to the DRAM bus. *Id*. Via receives a plurality of memory transactions at the multiplexer inputs. Each of the memory transactions is addressed to a corresponding memory bank. *See* Ex. 1 at 123; Ex. 2 at p. 33. The

DDR Controller associates a priority with each received memory transaction. Ex. 1 at 122, 125. (Initially, assigning a low priority to requests and then assigning a high priority when pending for a programmable duration). The DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as following the submission of activate commands to the DDR3 memory. *See* Ex. 2 at 18, 55; Ex. 1 at 178-180. The bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. The DDR Controller sends each of the plurality of memory transactions to its corresponding memory bank based on the associated priorities and the bank readiness signals. *See* Ex. 1 at 122-123, 178-180.

43. On information and belief, Via has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, Accused Via Products. Via had the knowledge of the '603 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Via Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

44. On information and belief, Via has committed the foregoing infringing activities without a license.

45. On information and belief, Via's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

46. Via knew the '603 Patent existed, knew of its claims, and knew of Via's infringing

products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Via, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against Via on all counts;

B. Entry of judgment that Via has infringed the Patents-in-Suit;

C. Entry of judgment that Via's infringement of the '234, '386, '069, and '603 Patents has been willful;

D. Award of compensatory damages adequate to compensate CCO for Via's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Award of CCO's costs;

F. Pre-judgment and post-judgment interest on CCO's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Dated: January 22, 2020

Respectfully submitted,

/s/ Dmitry Kheyfits

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ATTACHMENT 1

VX900 Series Media System Processor
VX11 Media System Processor
VIA SOM-6X80 Module
VIA SOM-6X50 Module
VIA AMOS-3005 Edge Computing System
VIA AMOS-3003
VIA ARTiGO A630 Enterprise IoT Gateway System
VIA ARTiGO A600 Smart Automation Control System
VIA ARTiGO A1250 Small Form Factor PC
VIA ALTA DS 4K Android Signage System
VIA ALTA DS 2 Android Signage System
VIA COMe-9X90 COM Express Module
VIA COMe-8X92 COM Express Module
VIA COMe-8X90 COM Express Module
VIA ETX-8X90 ETX Module
VIA ETX-8X90-10GR ETX Module
VIA VAB-600
VIA VAB-630
VIA EPIA-M910
VIA EPIA-P910
VIA VAB-820
VIA VAB-1000
VIA EPIA-M920
VIA VIPRO VP7910