IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff -against- MARVELL INTERNATIONAL, LTD., MARVELL TECHNOLOGY GROUP LTD., MARVELL SEMICONDUCTOR, INC. Defendants	**Case No.: 6:20-cv-00044** **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO"), for its Complaint against Defendants Marvell International, Ltd., Marvell Technology Group Ltd., and Marvell Semiconductor, Inc. (collectively "Marvell" or "Defendants"), hereby alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. Marvell Technology Group Ltd. ("MTGL") is a company organized under the laws of Bermuda. MTGL has its corporate headquarters at Canon's Court, 22 Victoria Street, Hamilton, HM 12, Bermuda.

3. Marvell International, Ltd. ("MIL") is a company organized under the laws of Bermuda. MIL has an office at Canon's Court, 22 Victoria Street, Hamilton, HM 12, Bermuda.

4. Marvell Semiconductor, Inc. ("MSI") is a California corporation with its principal place of business located at 5488 Marvell Lane, Santa Clara, California 95054. MSI has a regular and

established place of business at 13915 Burnet Rd., #400 Austin, TX 78728. MSI is MTGL's U.S. operating subsidiary.

5. MTGL, MIL, and MSI are jointly and severally liable for the patent infringement which arises out of the same transaction, occurrence, or series of transactions or occurrences relating to the making, using, importing into the United States, offering for sale, or selling of the same accused products or processes. On information and belief, a substantial portion of MSI activities in the United States is performed under direction and control of MTGL and MIL

JURISDICTION AND VENUE

6. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Marvell of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

7. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

8. MTGL is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, independently and/or via MSI, (i) MTGL sells and offers for sale its products in Texas, (ii) MTGL sells and offers for sale its products by using distributors and sales representatives located in Texas; (iii) MTGL places its products in the stream of commerce with intent or knowledge that those products would end up in Texas; (iv) MTGL recruits Texas residents; and (v) MTGL contracts with a Texas resident, such as for leasing real property, with performance occurring in Texas.

9. MIL is a wholly owned subsidiary of Marvell Technology Group Ltd. Marvell International, Ltd. is the assignee of record of various trademarks including Marvell®, ARMADA®, Link Street®, Prestera® under which Marvell Technology Group Ltd markets and sells the accused products. On information and belief MIL has agreements with MTLG. and MSI concerning the use of those trademarks.

10. According to a complaint that it filed in the United States International Trade Commission ("ITC"), Marvell International, Ltd. "conducts significant domestic industry activities in the United States" including "MIL's significant investment in plant and equipment" and "significant employment of labor and capital." Specifically, the complaint alleged that "MIL has contracted with MSI [a domestic Marvell affiliate] to conduct research and development," "MIL has significantly invested in U.S.-based plant and equipment used in research and development," "MIL, through MSI, has employed and continues to employ a significant number of employees in U.S. facilities that devote substantial man-hours toward research and development," and "MIL has also invested and continues to invest significantly in U.S.-based research and development and engineering." In that case before the ITC, Marvell International, Ltd. moved for, and was granted, summary determination that Marvell International, Ltd. "satisfied the economic prong of the domestic industry requirement."

11. MIL is subject to personal jurisdiction of this Court because, inter alia, on information and belief, through MSI's activity, which develops products on behalf of MIL and markets these products in the United States, (i) MIL sells and offers for sale its products in Texas, (ii) MIL sells and offers for sale its products by using distributors and sales representatives located in Texas; (iii) MIL places its products in the stream of commers with intent or knowledge that those products would end up in Texas; (iv) MIL recruits Texas residents; and (v) MIL contracts with a Texas resident, such as for leasing real property, with performance occurring in Texas.

12. MSI is MTLG's wholly owned subsidiary.

13. MSI is subject to personal jurisdiction of this Court because, inter alia, on information and belief (i) MSI sells and offers for sale its products in Texas, (ii) MSI sells and offers for sale its products by using distributors and sales representatives located in Texas; (iii) MSI places its

products in the stream of commers with intent or knowledge that those products would end up in Texas; (iv) MSI recruits Texas residents; and (v) MSI contracts with a Texas resident, such as for leasing real property, with the performance occurring in Texas.

14. Venue is proper as to MSI in this district under 28 U.S.C. § 1400(b) because MSI has a regular and established place of business and has committed acts of patent infringement in this judicial district.

15. Venue is proper as to MTGL and MIL in this district under 28 U.S.C. § 1391(c) because, *inter alia*, MTGL and MIL are foreign entities.

BACKGROUND

16. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

17. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

18. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

19. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

20. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

21. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

22. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

23. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

24. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

25. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

26. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

27. By letter dated May 23, 2019, CCO notified MTGL and MSI of the existence of the Patents-in-Suit, and of infringement of the '234, '386, '069, and '603 Patents by Marvell. CCO's letter identified exemplary infringing Marvell products and an exemplary infringed claim for each of the '234, '386, '069, and '603 Patents. CCO's May 23, 2019 letter invited Marvell to hold a licensing discussion with CCO.

28. CCO notified Marvell of the '021 Patent in the May 23, 2019 letter and, at least as of the time of the filing of this complaint, Marvell has had notice of its infringement of the '021 Patent.

LICENSING

29. As of the time of this complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, and Qualcomm.

COUNT I: INFRINGEMENT OF THE '021 PATENT

30. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

31. On information and belief, Marvell has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States processors, microcontrollers, and gateways identified in Attachment 1 ("Accused Marvell Products") that include a Marvell DDR3, DDR4, LPDDR3, LPDDR4, and/or LPDDR4x controller ("DDR Controller").

32. On information and belief, Marvell has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the Accused Marvell Products, including during regular operation and during development, design, testing, and verification of the Accused Marvell Products. *See* Ex. 1, Marvell 88SS1100 SSD Controller, Product Brief, May 2018 p. 1.; Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, p. 195. The DDR Controller continuously transmits data through each DQ transmission line during centering and link training. *See id.* ("Up to 5 consecutive MPC [Write DQ FIFO] command with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command.") The DDR Controller measures a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. *See id.* ("After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC][Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed."). The DDR Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern

transmitted through the transmission line. *See id.* The DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. *See id.*; *see also id*. at 200.

33. On information and belief, Marvell has induced, and continues to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Marvell Products that incorporate the DDR Controller. Marvell had the knowledge of the '021 Patent, at least from the time of filing this complaint, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Marvell Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

34. On information and belief, Marvell has committed the foregoing infringing activities without a license.

35. On information and belief, Marvell's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

COUNT II: INFRINGEMENT OF THE '234 PATENT

36. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

37. On information and belief, Marvell has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Marvell Products.

38. For example, on information and belief, Marvell has infringed at least claim 28 of the

'234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Marvell Products that include the DDR Controller with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Marvell Products and specifically the DDR Controller. Ex. 3, Marvell 88SS1321 SSD Controller, Product Brief, Aug. 2019 p. 2. An exemplary DDR Controller reduces timing uncertainty in LPDDR4/x memory transmission including calibration using the Multi-Purpose Register (MPR), read centering, write centering, and write leveling. *See* Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, pp. 26, 190, 195. *See also* Ex. 4, DDR PHY Interface, DFI 4.0 Specification, p. 55. The DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of input and outputs. The DDR Controller further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. The DDR Controller DMCs include a main clock for generating a main clock signal (such as the DDR Controller Clock). The DDR Controller includes a reference clock, such as an internal clock or a DDR Interface Clock, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training. The reference clock is associated with the main clock signal. The DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the CK signal at the destination. For example, the phase shift circuitry aligns the timing of the DQS signals via write leveling. *See id*. at 186 ("To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this

feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); *See id*. Ex. 4, DDR PHY Interface, DFI 4.0 Specification, p. 157.

39. On information and belief, Marvell has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Marvell Products that incorporate the DDR Controller. Marvell had the knowledge of the '234 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Marvell Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

40. On information and belief, Marvell has committed the foregoing infringing activities without a license.

41. On information and belief, Marvell's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

42. On information and belief, Marvell knew the '234 Patent existed, knew of an exemplary infringed claim of the '234 Patent, and knew of exemplary infringing Marvell products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT III: INFRINGEMENT OF THE '386 PATENT

43. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

44. On information and belief, Marvell has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in

the United States or importing into the United States the Accused Marvell Products.

45. For example, on information and belief, Marvell has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused Marvell Products, which include a DDR Controller, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. *See, e.g.*, Ex. 5, Marvell MV78230, MV78260, and MV78460, ARMADA XP Family of Highly Integrated Multi-Core ARMv7 Based SoC Processors, Functional Specifications, May 2014, p. 179. Exemplary DDR3 Memory to which the DDR Controller connects has multiple memory banks. *See id*. at 74, 179. *See* e.g., Ex. 6, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The Accused Marvell Products send the requests over a memory bus. Ex. 5 at 179. The DDR Controller comprises a queue comprising a plurality of request stations for storing memory transactions, such as read requests, such as a read transaction buffer. *See id*. Each of the memory transactions is addressed to one of the memory banks. *Id.* at 180. *See* Ex. 6 at 33. The DDR Controller includes an arbiter. *See* Ex. 5 at 75, 179 (The DRAM Controller can re-order transactions over the DRAM interface to optimize the DRAM utilization, while still maintaining system level ordering . . .). The arbiter is simultaneously coupled to each of the request stations and adapted to select any of the memory transactions. *See id.* The arbiter is configured to generate a plurality of bank readiness signals, such as following the submission of an activate command to the DDR3 memory. *See id.* at 48, 175, 185. *See also* Ex. 6 at 18, 48, 55. The DDR Controller, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *See* Ex. 5 at 175, 179.

46. On information and belief, Marvell has induced, and continues to induce, infringement of

the ’386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Marvell Products. Marvell had the knowledge of the ’386 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Marvell Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

47. On information and belief, Marvell has committed the foregoing infringing activities without a license.

48. On information and belief, Marvell’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

49. Marvell knew the ’386 Patent existed, knew of its claims, and knew of Marvell infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’386 Patent.

COUNT IV: INFRINGEMENT OF THE ’069 PATENT

50. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

51. On information and belief, Marvell has infringed the ’069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Marvell Products.

52. For example, on information and belief, Marvell has infringed at least claim 12 of the ’069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and verification of the Accused Marvell Products, which include the DDR Controller, such as a

LPDDR4/4x memory controller that automatically calibrates skew of LPDDR4/4x DDRs. *See* Ex. 3, Marvell 88SS1321 SSD Controller, Product Brief, Aug. 2019 p. 2; Ex. 2, JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017, p. 26. The DDR Controller initiates Write Leveling and Read Optimization via the PHY. *See id*. The PHY comprises a transmitter and the receiver. Marvell calibrates registers of the receiver, such as the PHY registers in relation to a reference clock edge, such as a PHY clock. *See* Ex. 4, DDR PHY Interface, DFI 4.0 Specification, pp. 16, 17, 25, 147. Marvell calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver with the Write Leveling feature. *See* Ex. 2 at 186 ("To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); Ex. 4 at 157. The calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS_t-DQS-c and CK_t-CK_c signals. The calibration is performed for a plurality of data patterns, such as DQS_t – DQS_c patterns with variable delays. Ex. 2 at 186. ("5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings. 6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established."). Marvell applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See id.*; Ex. 4 at 144-145.

53. On information and belief, Marvell has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing,

causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Marvell Products that incorporate the DDR Controller. Marvell had the knowledge of the '069 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Marvell Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

54. On information and belief, Marvell has committed the foregoing infringing activities without a license.

55. On information and belief, Marvell's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

56. On information and belief, Marvell knew the '069 Patent existed, knew of an exemplary infringed claim of the '069 Patent, and knew of exemplary infringing Marvell products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT V: INFRINGEMENT OF THE '603 PATENT

57. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

58. On information and belief, Marvell has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Marvell Products.

59. For example, on information and belief, Marvell has infringed at least claim 14 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including

during development, design, testing, and verification of the Accused Marvell Products. The DDR Controller of the Accused Marvell Products includes a multiplexer. *See* Ex. 5, Marvell MV78230, MV78260, and MV78460, ARMADA XP Family of Highly Integrated Multi-Core ARMv7 Based SoC Processors, Functional Specifications, May 2014, p. 179 ("The DRAM controller receives red and write requests from an of the device units through the device's Mbus fabric or from the Marvell CPU via . . . Fast AXI path") . Memory to which the Accused Marvell Products connect has multiple memory banks. *See id.*; *see also Id*. at 74. See e.g., Ex. 6, JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008) at p. 15-16. The multiplexer in the DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions, such as the inputs from Mbus and Fast AXI path. *See* Ex. 5 at 179. The multiplexer also comprises a multiplexer output for sending each of the plurality of memory transactions to the memory, such as the interface to the Marvell DRAM PHY "to drive the transaction of the DRAM interface." *See* Ex. 5 at 175. Marvell receives a plurality of memory transactions at the multiplexer inputs. Each of the memory transactions is addressed to a corresponding memory bank. *Id.* at 180. See Ex. 6 at p. 33. The DDR Controller associates a priority with each received memory transaction. Ex. 5 at 174-175. (". . . latency sensitive transactions may get higher priority and are served first if no ordering hazards apply."). The DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as following the submission of activate commands to the DDR3 memory. *See id*. at 48, 175, 185. See also Ex. 6 at 18, 48, 55. The bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. *See* Ex. 5 at 173 ("Smart memory access scheduler for maximum DRAM utilization with configurable priority scheme"). The DDR

Controller sends each of the plurality of memory transactions to its corresponding memory bank via the Marvell DRAM PHY based on the associated priorities and the bank readiness signals. *See id*. at 174-175 ("The logic will now pick the next transaction to be served to best utilize the DRAM bus on the one hand and maintain system ordering and system level transaction priority on the other hand. For example, latency sensitive transactions may get higher priority and are served first if no ordering hazards apply. In the same way the logic may also reorder the transaction execution to maximize the DRAM bus utilization through improved bank interleaving, minimization of read-write shifts and so on . . .")

60. On information and belief, Marvell has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, Marvell Accused SoC. Marvell had the knowledge of the '603 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Marvell Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

61. On information and belief, Marvell has committed the foregoing infringing activities without a license.

62. On information and belief, Marvell's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

63. Marvell knew the '603 Patent existed, knew of its claims, and knew of Marvell's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly,

and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Marvell, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against Marvell on all counts;

B. Entry of judgment that Marvell has infringed the Patents-in-Suit;

C. Entry of judgment that Marvell's infringement of the '234, '386, '069, and '603 Patents has been willful;

D. Award of compensatory damages adequate to compensate CCO for Marvell's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Award of CCO's costs;

F. Pre-judgment and post-judgment interest on CCO's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Dated: January 22, 2020

Respectfully submitted,

/s/ Dmitry Kheyfits

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ATTACHMENT 1

- ARMADA 3700 Family Single/Dual CPU System on Chip (88F3710 and 88F3720)
- ARMADA 38x Family High-Performance Single/Dual CPU System on Chip (88F6810, 88F6811, 88F6821, 88F6W21, 88F6820, and 88F6828)
- ARMADA 8040 Quad-Core CA72 Processor with Marvell MoChi
- ARMADA XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors (MV78230, MV78260, MV78460)
- ARMADA 7k/8k (88F7020, 88F7040, 88F8020, 88F8040)
- ARMADA 375 (88F6720)
- ARMADA 380/385/388 (88F6810, 88F6820, 88F6828)
- OCTEON II CN62XX Multi-Core MIPS64 Processors
- OCTEON II CN63XX Multi-Core MIPS64 Processors
- OCTEON III CN78XX Multi-Core MIPS64 Processors
- OCTEON Fusion-M CNF73xx
- Eight-Lane PCIe 2.0 to Eight-Port SAS/SATA 6 Gbps RAID-on-Chip Processor (88RC9580)
- Prestera 98DX4211
- Prestera 98DX8212
- ThunderX2 CN99XX
- ThunderX_NT Family of Network Centric Workload Optimized Processors
- Link Street Gateway 88E7251

- Link Street Gateway 88E7221
- Link Street- Gateway 88E6390X
- SAS/SATA RAID-on-Chip Processor 88RC9548/88RC9580
- WLAN Microcontroller (88MW300/302)
- Quad-Core MFP Printer SoC88PA6270
- SSD Controller Chipset (88SS1084/88SS1088)
- QDEO Video Processors (88DE2755)
- Andromeda Box Edge
- SSD Controller (88SS1100/88SS1321)
- Marvell Xelerated HX4100 Family of Network Processors