IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MONTEREY RESEARCH, LLC, Plaintiff, v. ADVANCED MICRO DEVICES, INC., Defendant.	)	C.A. No. 19-cv-2149-CFC **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Monterey Research, LLC ("Monterey"), for its First Amended Complaint for Patent Infringement against Defendant Advanced Micro Devices, Inc. ("AMD"), alleges as follows:

INTRODUCTION

1. Monterey is an intellectual property and technology licensing company. Monterey's patent portfolio comprises over 2,700 active and pending patents worldwide, including approximately 2,000 active United States patents. Monterey's patent portfolio stems from technology developed by a number of leading high-technology companies, including Cypress Semiconductor Corporation, Fujitsu, NVX Corporation, and Ramtron. Those companies developed key innovations that have greatly enhanced the capabilities of computer systems, increased electronic device processing power, and reduced electronic device power consumption. Among other things, those inventions produced significant technological advances, including smaller, faster, and more efficient semiconductors and integrated circuits.

2. AMD infringes Monterey's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. AMD's customers incorporate those products into downstream

products that are made, used, sold, offered for sale, and/or imported throughout the United States, including within this District. Those downstream products include, but are not limited to, motherboards, desktop computers, servers, laptop computers, videogame consoles, and other products that include AMD semiconductor devices and integrated circuits.

3. AMD has infringed and continues to infringe Monterey's patents. AMD has thus far refused to license those patents and, instead, has continued to make, use, sell, offer to sell, and/or import Monterey's intellectual property within the United States without Monterey's permission.

NATURE OF THE CASE

4. This action arises under 35 U.S.C. § 271 for AMD's infringement of Monterey's United States Patent Nos. 6,534,805 ("the '805 patent"); 6,629,226 ("the '226 patent"); 6,651,134 ("the '134 patent"); 6,765,407 ("the '407 patent"); 6,961,807 ("the '807 patent"); and 8,373,455 ("the '455 patent") (collectively, "the Patents-in-Suit").

THE PARTIES

5. Plaintiff Monterey is a Delaware limited liability company with offices in New Jersey and California. Monterey maintains a registered agent for service in Delaware: Intertrust Corporate Services Delaware Ltd. located at 200 Bellevue Parkway, Suite 210, Wilmington, Delaware 19808.

6. Defendant AMD is a Delaware corporation with a principal place of business at 2485 Augustine Drive, Santa Clara, California 95054. AMD is a publicly traded company that may be served through its registered agent for service, The Corporation Trust Company, 1209 Orange Street, Wilmington, Delaware 19801.

JURISDICTION AND VENUE

7. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a) at least because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq*.

8. Personal jurisdiction exists over AMD at least because AMD is a Delaware corporation organized under the laws of the State of Delaware. AMD also has a registered agent for service of process in Delaware. In addition, AMD has committed, aided, abetted, contributed to, and/or participated in the commission of acts of infringement giving rise to this action within the State of Delaware by, *inter alia*, directly and/or indirectly making, using, selling, offering for sale, importing products, and/or practicing methods that practice one or more claims of the Patents-in-Suit. Furthermore, AMD has transacted and conducted business in the State of Delaware and with Delaware residents by making, using, selling, offering to sell, and/or importing (including importing products made by a patented process) products and instrumentalities that practice one or more claims of the Patents-in-Suit. Among other things, AMD, directly and/or through intermediaries, uses, sells, ships, distributes, imports into, offers for sale, and/or advertises or otherwise promotes its products throughout the United States, including in the State of Delaware. *See, e.g.*, www.amd.com/en. At least for those reasons, AMD has the requisite minimum contacts within the forum such that the exercise of jurisdiction over AMD would not offend traditional notions of fair play and substantial justice.

9. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and 1400(b). AMD resides in this district and has committed acts of infringement in this district. AMD has committed acts of infringement in this district by, among other things, selling and offering for sale in this district (and elsewhere) infringing products made, used, developed, tested, and otherwise practiced by AMD. Venue is further proper based on the facts alleged in the preceding paragraphs, which Monterey incorporates by reference as if fully set forth herein.

THE PATENTS-IN-SUIT

10. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

A. U.S. Patent No. 6,534,805

11. The ’805 patent, titled “SRAM Cell Design,” was duly and properly issued by the United States Patent and Trademark Office (“USPTO”) on March 18, 2003. On October 14, 2014, the USPTO issued an Ex Parte Reexamination Certificate for the ’805 patent, which confirmed the patentability of the ’805 patent. A true and correct copy of the ’805 patent and the Ex Parte Reexamination Certificate for the ’805 patent is attached hereto as Exhibit A.

12. Monterey is the owner and assignee of the ’805 patent; owns all right, title, and interest in the ’805 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

B. U.S. Patent No. 6,629,226

13. The ’226 patent, titled “FIFO Read Interface Protocol,” was duly and properly issued by the USPTO on September 30, 2003. A true and correct copy of the ’226 patent is attached hereto as Exhibit B.

14. Monterey is the owner and assignee of the ’226 patent; owns all right, title, and interest in the ’226 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

C. U.S. Patent No. 6,651,134

15. The ’134 patent, titled “Memory Device with Fixed Length Non Interruptible Burst,” was duly and properly issued by the USPTO on November 18, 2003. A true and correct copy of the ’134 patent is attached hereto as Exhibit C.

16. Monterey is the owner and assignee of the ’134 patent; owns all right, title, and interest in the ’134 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

D. U.S. Patent No. 6,765,407

17. The ’407 patent, titled “Digital Configurable Macro Architecture,” was duly and properly issued by the USPTO on July 20, 2004. A true and correct copy of the ’407 patent is attached hereto as Exhibit D.

18. Monterey is the owner and assignee of the ’407 patent; owns all right, title, and interest in the ’407 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

E. U.S. Patent No. 6,961,807

19. The ’807 patent, titled “Device, System and Method for an Integrated Circuit Adaptable for Use in Computing Systems of Differing Memory Requirements,” was duly and properly issued by the USPTO on November 1, 2005. A true and correct copy of the ’807 patent is attached hereto as Exhibit E.

20. Monterey is the owner and assignee of the ’807 patent; owns all right, title, and interest in the ’807 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

F. U.S. Patent No. 8,373,455

21. The ’455 patent, titled “Output Buffer Circuit,” was duly and properly issued by the USPTO on February 12, 2013. A true and correct copy of the ’455 patent is attached hereto as Exhibit F.

22. Monterey is the owner and assignee of the ’455 patent; owns all right, title, and interest in the ’455 patent; and holds the right to sue and recover damages for infringement thereof, including past infringement.

FACTUAL BACKGROUND

23. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

24. The Patents-in-Suit stem from the research and design of innovative and proprietary technology developed by leading high-technology companies, including Cypress Semiconductor Corporation ("Cypress"). Cypress is an American multinational company and pioneer of cutting-edge semiconductor technology. Founded in 1982, Cypress has made substantial investments in researching, developing, and manufacturing high-quality semiconductor devices, integrated circuits, and products containing the same.

25. The Patents-in-Suit are directed to inventive technology relating to semiconductor devices, integrated circuits, and/or products containing the same.

26. Defendant AMD works closely with its customers, OEMs, foundry suppliers, distributors, and/or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and/or products containing the same. Among other things, AMD optimizes its manufacturing process for its customers and optimizes its products for integration into downstream products. AMD's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States include, but are not limited to, any one or combination of: (i) designing specifications for manufacture of its products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of its products; (iii) soliciting and/or sourcing the manufacture of its products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of its products; (v) enabling and encouraging the use, sale, or importation of its products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

27. AMD also provides marketing and/or technical support services for its products from its facilities in the United States. For example, AMD maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for its

products. *See, e.g.*, www.amd.com/en. AMD's publicly-available website also contains user manuals, product documentation, and other materials related to its products. *See, e.g.*, www.amd.com/en. For example, AMD's website contains a knowledge base, software help center, support forum, technical documents, and downloadable graphics drivers. *See, e.g.*, www.amd.com/en.

AMD'S PRE-SUIT KNOWLEDGE OF MONTEREY'S PATENTS AND CHARGE OF INFRINGEMENT

28. Monterey notified AMD that it infringes the '805, '134, '807, and '455 patents on September 24, 2018.

29. AMD was placed on notice of the '407 patent for purposes of 35 U.S.C. § 287(a) as of January 26, 2018, when Monterey sent a notice letter to AMD informing them of the patent and identifying covered AMD products.

COUNT ONE
INFRINGEMENT OF THE '805 PATENT

30. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

31. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '805 patent.

32. The '805 patent is valid and enforceable.

33. The '805 patent is generally directed to static random access memory ("SRAM") cell design, particularly to optimizing SRAM cell design using a simpler geometric layout.

34. As semiconductor structure size continued to shrink with time, one exemplary issue with the prior art of the '805 patent was increased difficulties in manufacturing. Specifically, the then-existing memory cells contained complex geometric designs which required numerous processing steps and larger cell sizes. Generally, more processing steps lead to increased

manufacturing costs and reduced profits.

35. The ’805 patent teaches, among other things, an improved memory cell layout which allows the features to be arranged in such a way as to minimize cell size. For example, the single local interconnect layer of the ’805 patent allows for a thinner product and fewer processing steps.

36. AMD products use SRAM with a six-transistor (“6T”) and/or eight-transistor (“8T”) cell design. AMD’s 6T and 8T SRAM contain a single local interconnect layer. This has resulted in, among other things, AMD’s ability to decrease the size of its SRAM area and to decrease the number of manufacturing steps.

37. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’805 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’805 patent, including, but not limited to, all AMD devices incorporating SRAM with a 6T and/or 8T cell design, such as the A8-3800 semiconductor device and other products in the A-Series, Pro A-Series, Ryzen, Ryzen Pro, Athlon, Epyc, FX, E-Series, Opteron, Phenom, Sempron, and the Turion product families; and all other semiconductor devices, integrated circuits, and products with similar infringing technology (“the Accused ’805 Products”).

38. As one non-limiting example, AMD infringes claim 8 of the ’805 patent. For example, the A8-3800 semiconductor device contains:

a. a memory cell (e.g., SRAM cell of the A8-3800) comprising a plurality of substantially oblong active regions (e.g., N-type and/or P-type diffusion areas of the A8-3800) formed in a semiconductor substrate and arranged substantially in parallel with one another, and a plurality of substantially oblong local interconnects (e.g., structures formed at the polysilicon layer

on top of the substrate of the A8-3800) above said substrate that extend only partially across the memory cell and are arranged substantially in parallel with one another and substantially perpendicular to said active regions; and

b. a single local interconnect layer (e.g., metal 1 ("M1") layer of the A8-3800) comprising local interconnects (e.g., structures formed at the M1 layer of the A8-3800) corresponding to bitlines (e.g., those formed at the metal 2 ("M2") layer of the A8-3800) and a global word-line (e.g., those formed at the metal 3 ("M3") layer of the A8-3800).

39. Claim 8 of the '805 patent applies to each Accused '805 Product at least because each of those products contain the same or similar structures as the AMD A8-3800.

40. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

41. AMD was on notice of the '805 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

42. AMD, knowing its products infringe the '805 patent and with the specific intent for others to infringe the '805 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the '805 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Accused '805 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD's website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses

of AMD's products that infringe the '805 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/53738_PDS_Athlon.pdf. Additional non-limiting examples include the materials found on AMD's websites at www.amd.com/en/processors/athlon-and-a-series and www.amd.com/en/products/specifications/processors/.

43. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the '805 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused '805 Products, which constitute a material part of the invention of the '805 patent, knowing the Accused '805 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/53738_PDS_Athlon.pdf.

44. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

45. AMD's infringement of the '805 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '805 patent and that its conduct constituted and resulted in infringement of the '805 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '805 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of

infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '805 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT TWO
INFRINGEMENT OF THE '226 PATENT

46. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

47. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '226 patent.

48. The '226 patent is valid and enforceable.

49. The '226 patent is generally directed to a method and/or architecture for implementing a multiqueue memory read interface, and more particularly, to a method and/or architecture for implementing a multiqueue read interface protocol for eliminating synchronizing problems for configuration dependent latencies where the protocol may be capable of handling variable size packets.

50. The '226 patent explains that in prior multiqueue memories (e.g., first-in-first-out ("FIFO") memory), a signal, e.g., ADDRESS, was a queue address configured to determine a queue number of the multiqueue memory. The signals, e.g., READ_CLOCK and READ_EN, could control the timing of the presentation of the data signal, e.g., DATA. Because of particular architectures and specifications of particular devices, the latency between enabling a queue address signal, e.g., ADDRESS, and presenting a data signal, e.g., DATA, could differ depending on the particular configuration. Configuration information needed to be written into an external read device. The only event reference available to the external read device was an end of packet or a start of packet, e.g.,

EOP or SOP. In such an environment, the read device was required to monitor this event to generate the queue address signal, e.g., ADDRESS, in a sufficient number of cycles ahead of the read.

51. These prior multiqueue memory systems had the disadvantage of requiring a fixed packet size. A circuit could be required to generate the queue address, e.g., ADDRESS, a certain number of cycles before the end of packet occurs. The particular number of cycles may be the same as the minimum latency requirement. For certain configurations, there was a specific latency between the queue address signal, e.g., ADDRESS, and presenting the signal, e.g., DATA. If the packet size varied randomly, such as when the size of the packet was less than the number of cycles of latency, a read of one or more unwanted packets occurred. Additionally, it may have been difficult for the read device to synchronize the queue address signal, e.g., ADDRESS, with the data received from the memory (e.g., FIFO). Therefore, the read device needed to be configured with enough logic to respond to the different latencies. Such a configuration required extra overhead for the read device.

52. The ’226 patent teaches, among other things, an interface coupled to a multiqueue storage device and configured to interface the multiqueue storage device with one or more handshaking signals. The multiqueue storage device and the interface may be configured to transfer variable size data packets. Such a system provided numerous benefits, including but not limited to: (i) eliminating synchronizing problems with configuration dependent latencies; (ii) being capable of handling variable size packets; (iii) allowing back-to-back reads of variable size packets; and (iv) exchanging address and data between an external read device and a multiqueue storage device.

53. AMD products use a multiqueue storage device, such as an NVM Express (“NVME”) compliant memory. NVME compliant memory can be found in, among other products, the AMD Pro SSG. AMD products use multiqueue storage devices that are compliant with the NVME Base Specification standard and similar versions of the NVME standard that incorporate the innovations

of the ’226 patent’s multiqueue memory read interface. AMD’s multiqueue storage device further interfaces with handshaking signals, and allows back-to-back reads of variable size data packets.

54. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’226 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’226 patent, including, but not limited to, products supporting NVME or with NVME compliant memory, such as the Radeon Pro SSG semiconductor device and other products in the Radeon Pro, Epyc and Ryzen product families; other AMD semiconductor devices, integrated circuits, and products built to utilize NVME compliant memory; and all other semiconductor devices, integrated circuits, and products using a similar multiqueue memory read interface (“the Accused ’226 Products”).

55. As one non-limiting example, AMD infringes claim 18 of the ’226 patent. For example, the Radeon Pro SSG semiconductor device contains: An interface coupled to a multiqueue storage device (e.g., multiqueue memory of the Radeon Pro SSG) and configured to interface said multiqueue storage device with one or more handshaking signals (e.g., data link packets and/or command set of the Radeon Pro SSG), wherein said multiqueue storage device and said interface are configured to allow back-to-back reads of variable size data packets (e.g., via sequential read requests and/or burst read requests, and/or a Scatter Gather List of the Radeon Pro SSG).

56. Claim 18 of the ’226 patent applies to each Accused ’226 Product at least because each of those products contain infringing NVME compliant memory; and/or contain a multiqueue storage device with similar infringing functionality.

57. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement.

58. AMD was on notice of the ’226 patent at least as early as November 15, 2019, the date Monterey filed the first complaint in this action.

59. AMD, knowing its products infringe the ’226 patent and with the specific intent for others to infringe the ’226 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’226 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’226 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’226 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/56245-PUB.pdf. Additional non-limiting examples include the materials found on AMD’s websites at www.amd.com/en/chipsets/str40 and www.amd.com/en/chipsets/x570.

60. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’226 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’226 Products, which constitute a material part of the invention of the ’226 patent, knowing the Accused ’226 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce

suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/56245-PUB.pdf.

61. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

62. AMD's infringement of the '226 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '226 patent and knew that its conduct constituted and resulted in infringement of the '226 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '226 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '226 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT THREE
INFRINGEMENT OF THE '134 PATENT

63. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

64. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '134 patent.

65. The '134 patent is valid and enforceable.

66. The '134 patent generally concerns memory devices, and is more specifically related

to non-interruptible burst read and write access features, as described in JEDEC standard JESD212 GDDR5 SGRAM and similar versions of the JEDEC GDDRx standards.

67. The ’134 patent provides a faster and more efficient way for burst read and write access over conventional DRAM devices existing when the patent was filed in early 2000. Prior to the ’134 patent, DRAM memory devices had a burst mode that had the possibility of needing to continually perform interrupts to perform data refreshes.

68. The ’134 patent teaches, among other things, a fixed burst memory that can have non-interruptible bursts, hide required DRAM refreshes inside a known fixed burst length, free up the address and control busses for multiple cycles, and operate at higher frequencies without needing interrupts to perform refreshes of data.

69. AMD products use memory devices that are compliant with the JESD212 GDDR5 SGRAM standard and similar versions of the JEDEC GDDRx standards that incorporate the innovations of the ’134 patent’s non-interruptible fixed burst length.

70. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’134 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’134 patent, including, but not limited to, products that comply with the JEDEC standards JESD212 GDDR5 SGRAM and similar versions of the JEDEC GDDRx standards that use non-interruptible burst read or write operations, such as the Radeon RX 580 graphics card and other products in the Radeon, Radeon Pro, Embedded Radeon, Mobility Platforms, Instinct, FireStream, and the FirePro product families; the Neo and Liverpool graphics processors; other AMD semiconductor devices, integrated circuits, and products that are compliant with the JESD212 GDDR5 SGRAM standard or similar versions; and all

other semiconductor devices, integrated circuits, and products with similar infringing technology ("the Accused '134 Products").

71. As one non-limiting example, AMD infringes claim 1 of the '134 patent since the AMD Radeon RX 580 semiconductor device contains DDR3 SGRAM memory controllers that operate in conformance with JEDEC's DDR3 SGRAM standard. For example, the AMD Radeon RX 580 contains a circuit comprising:

a. a memory comprising a plurality of storage elements (e.g., banks of storage elements of the Radeon RX 580);

b. each configured to read and write data in response to an internal address signal (e.g., stored bits of memory bank addressed and defined by internal addresses of the Radeon RX 580);

c. a logic circuit configured to generate a predetermined number of said internal address signals (e.g., generating addresses based on bank addresses, row addresses, and column addresses of the Radeon RX 580) in response to an external address signal (e.g., read and/or write signals of the Radeon RX 580), a clock signal (e.g., clock signal of the Radeon RX 580), and one or more control signals (e.g., control signal of the Radeon RX 580);

d. wherein said generation of said predetermined number of internal address signals is non-interruptible (e.g., burst reads or writes cannot be terminated or interrupted in the Radeon RX 580).

72. Claim 1 of the '134 patent applies to each Accused '134 Product at least because each of those products either complies with the same JEDEC JESD212 GDDR5 SGRAM standard, or similar versions of the JEDEC standard, which result in infringing features (e.g., non-interruptible burst oriented read or write operations of the Accused '134 Products) found in the JESD212 GDDR5

SGRAM standard.

73. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

74. AMD was on notice of the ’134 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

75. AMD, knowing its products infringe the ’134 patent and with the specific intent for others to infringe the ’134 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’134 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Accused ’134 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’134 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/graphics/radeon-500-series/radeon-rx-500-series/radeon-rx-580. Additional non-limiting examples include the materials found on AMD’s website at www.amd.com/en/products/graphics/radeon-rx-580#product-specs.

76. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’134 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing

in or into the United States the Accused '134 Products, which constitute a material part of the invention of the '134 patent, knowing the Accused '134 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/graphics/radeon-500-series/radeon-rx-500-series/radeon-rx-580.

77. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

78. AMD's infringement of the '134 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '134 patent and knew that its conduct constituted and resulted in infringement of the '134 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '134 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '134 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT FOUR
INFRINGEMENT OF THE '407 PATENT

79. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

80. Monterey is the assignee and lawful owner of all right, title, and interest in and to the

’407 patent.

81. The ’407 patent is valid and enforceable.

82. The ’407 patent is generally directed to programmable digital circuit architecture, and particularly to programmable digital devices which are configurable to perform any one of various digital functions, by changing the contents of a register.

83. The ’407 patent explains that microcontrollers or controllers have been utilized in various applications for many years. Microcontrollers are frequently found in, for example: appliances, computers and computer equipment, automobiles, environmental control, aerospace, and thousands of other uses. Prior to the ’407 patent, field programmable gate arrays (“FPGA”) were utilized in several microcontroller applications. FPGAs are highly inefficient with respect to chip area, increasing their cost. Moreover, FPGAs need to have their look-up tables re-programmed in order to enable them to implement a new digital function, which is a time consuming task. FPGAs are not ideally suited for microcontroller applications, since, for example, microcontroller applications are very cost-sensitive. A FPGA is not able to realize the number of digital functions that are demanded by certain microcontroller applications within these strict cost constraints.

84. The ’407 patent teaches, among other things, a programmable digital circuit block that can be programmed to perform a variety of predetermined digital functions upon being configured with a single register write operation. This solution allows the configuration of the programmable digital circuit block to be determined by a small number of configuration registers, providing much flexibility. In particular, the configuration of the programmable digital circuit block is fast and easy since changes in configuration are accomplished by changing the contents of the configuration registers, whereas the contents are generally a small number of configuration data bits.

85. AMD products use an array of programmable digital circuit blocks, such as Zen or

Family 17h cores. For example, the Zen or Family 17h core can be found in a number of different AMD Zen microarchitecture based products, as it functions as a processing core of the AMD Zen microarchitecture based processor. The Zen or Family 17h core is programmable to perform a variety of predetermined digital functions by changing the contents of a register.

86. AMD has directly infringed, and continues to directly infringe, one or more claims of the '407 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the '407 patent, including, but not limited to, products with multiple cores utilizing the AMD64 instruction set, such as the Ryzen 3 1200 semiconductor device and other products in the Ryzen, Ryzen Pro, Athlon, Epyc, A-Series, Pro A-Series, FX, E-Series, Opteron, Phenom, Sempron, and the Turion product families; other multicore AMD semiconductor devices, integrated circuits, and products built to utilize the AMD64 instruction set; and all other semiconductor devices, integrated circuits, and products using a similar instruction set ("the Accused '407 Products").

87. As one non-limiting example, AMD infringes claim 8 of the '407 patent. For example, the Ryzen 3 semiconductor device contains:

a. an array of programmable digital circuit block (e.g., Zen or Family 17H cores of the Ryzen 3);

b. where each programmable digital circuit block is configurable to perform a predetermined digital function (e.g., operating a secure virtual machine of the Ryzen 3);

c. upon being configured with a single register write operation (e.g., writing the EFER register of the Ryzen 3).

88. Claim 8 of the '407 patent applies to each Accused '407 Product at least because each

of those products contain infringing Zen, Family 17h, or newer cores; and/or contain AMD64 instruction set based cores containing similar infringing functionality.

89. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

90. AMD was on notice of the ’407 patent under 35 U.S.C. § 287(a) at least as early as January 26, 2018.

91. AMD, knowing its products infringe the ’407 patent and with the specific intent for others to infringe the ’407 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’407 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’407 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’407 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf. Additional non-limiting examples include the materials found on AMD’s websites at www.amd.com/en/technologies/zen-core and www.amd.com/system/files/TechDocs/24593.pdf .

92. AMD has contributed to the infringement of, and continues to contribute to the

infringement of, one or more claims of the ’407 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’407 Products, which constitute a material part of the invention of the ’407 patent, knowing the Accused ’407 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf.

93. Monterey has sustained and is entitled to recover damages as a result of AMD’s infringement.

94. AMD’s infringement of the ’407 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the ’407 patent and knew that its conduct constituted and resulted in infringement of the ’407 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable ’407 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD’s conduct in light of these circumstances is egregious. AMD’s knowing, deliberate, and willful infringement of the ’407 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT FIVE
INFRINGEMENT OF THE ’807 PATENT

95. Monterey incorporates by reference the preceding paragraphs as if fully set forth herein.

96. Monterey is the assignee and lawful owner of all right, title, and interest in and to the ’807 patent.

97. The ’807 patent is valid and enforceable.

98. The ’807 patent is generally directed to integrated circuits and associated memory systems.

99. The ’807 patent explains that in the design of an integrated circuit incorporating a microprocessor, microcontroller, or other logic, it is often difficult to determine the appropriate amount of on-chip memory to incorporate on the die in order to suit the many applications that the integrated circuit may serve.

100. For example, a large amount of on-chip static memory (e.g., RAM) provided the benefit of fast program execution but had a disadvantage in that the large on-chip RAM required an initial program loading operation from an off-chip non-volatile memory (e.g., Flash ROM), which could have the program content stored therein. The use of such a non-volatile memory might add additional costs to the overall system that utilizes the integrated circuit, in part because the integrated circuit packages and corresponding pin counts might be quite large. For example, the interface between the external Flash ROM and the integrated circuit might include a parallel interface having 30 or more pins, which increased the complexity, size, and cost of use of such a system. While the cost and size of such an arrangement might be acceptable in the design of large, complex systems, the cost and size of such an arrangement might be unacceptable if the integrated circuit is to be used in a simple, low-cost system.

101. Alternatively, a large amount of non-volatile memory incorporated on-chip with the

integrated circuit had the advantage of relatively low costs when compared with an arrangement that uses on-chip RAM/external Flash ROM. However, such an arrangement had the disadvantage of relatively slower program execution when compared with on-chip RAM/external Flash ROM, which might be unacceptable for use in a large, complex system.

102. The ’807 patent teaches, among other things, a microprocessor, a cache controller, and a multipurpose memory, wherein the multipurpose memory has a first operating mode for dynamically storing as a cache memory portions of a program obtained from a first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode for storing an entire program obtained from a second external memory device to be run by the microprocessor. A system designer can choose whether to configure the system using the integrated circuit coupled with the first external memory device, or the integrated circuit coupled with the second external memory device. Beneficially, this allows for an architecture for an integrated circuit die that may be utilized with large, complex systems using external memory or with small, low-cost systems.

103. AMD products use a multipurpose memory. AMD’s Radeon processors, for example, contain a multipurpose memory, such as the high bandwidth cache. This has resulted in, among other things, AMD’s ability to provide an architecture for an integrated circuit die that may be utilized with large, complex systems using external memory or with small, low-cost systems.

104. AMD has directly infringed, and continues to directly infringe, one or more claims of the ’807 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the ’807 patent, including, but not limited to, products with a high bandwidth cache, such as the Radeon Pro SSG semiconductor

device and other products in the Radeon Pro, Radeon RX, Radeon Instinct, and the Vega10 product family; other AMD semiconductor devices, integrated circuits, and products with the Vega10 architecture and/or a high bandwidth cache; and all other semiconductor devices, integrated circuits, and products with a similar multipurpose memory architecture ("the Accused '807 Products").

105. As one non-limiting example, AMD infringes claim 1 of the '807 patent. For example, the Radeon Pro SSG semiconductor device contains an integrated circuit device comprising:

a. a microprocessor (e.g., processor of the Radeon Pro SSG);

b. a multipurpose memory (e.g., high bandwidth cache of the Radeon Pro SSG) coupled with the microprocessor;

c. a cache controller (e.g., high bandwidth cache controller of the Radeon Pro SSG);

d. a first memory port (e.g., PCIe port of the Radeon Pro SSG) for coupling a first external memory device (e.g., system memory of the Radeon Pro SSG) with said cache controller; and

e. a second memory port (e.g., PCIe port of the Radeon Pro SSG) for coupling a second external memory device (e.g., NVME memory and/or Pro SSG storage of the Radeon Pro SSG) with said multipurpose memory;

f. wherein the multipurpose memory has a first operating mode (e.g., first cache mode of the Radeon Pro SSG) for dynamically storing as a cache memory portions of a program obtained from the first external memory device for execution by the microprocessor under control of the cache controller, and the multipurpose memory has a second operating mode (e.g., second cache mode of the Radeon Pro SSG) for storing an entire program obtained from the second external memory device to be run by the microprocessor.

106. Claim 1 of the ’807 patent applies to each Accused ’807 Product at least because each of those products contain infringing high bandwidth cache; and/or contain similar infringing features.

107. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

108. AMD was on notice of the ’807 patent under 35 U.S.C. § 287(a) at least as early as September 24, 2018.

109. AMD, knowing its products infringe the ’807 patent and with the specific intent for others to infringe the ’807 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’807 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’807 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’807 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/professional-graphics/radeon-pro/radeon-pro-series/radeon-pro-ssg. Additional non-limiting examples include the materials found on AMD’s website at www.amd.com/en/products/professional-graphics/radeon-pro-ssg.

110. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’807 patent under 35 U.S.C. § 271(c), either literally and/or

under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused '807 Products, which constitute a material part of the invention of the '807 patent, knowing the Accused '807 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs and https://www.amd.com/en/support/professional-graphics/radeon-pro/radeon-pro-series/radeon-pro-ssg.

111. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

112. AMD's infringement of the '807 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '807 patent and knew that its conduct constituted and resulted in infringement of the '807 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '807 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '807 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT SIX
INFRINGEMENT OF THE '455 PATENT

113. Monterey incorporates by reference the preceding paragraphs as if fully set forth

herein.

114. Monterey is the assignee and lawful owner of all right, title, and interest in and to the '455 patent.

115. The '455 patent is valid and enforceable.

116. The '455 patent is directed to output buffers, and particularly to single ended output buffers.

117. The '455 patent explains that in an integrated circuit, output buffers are often used at output pins to transfer signals to the signal lines. The transmission of information across the signal lines can be subject to various problems such as impedance mismatch, signal reflection, or irregular output waveform. Typically, output buffers must meet specifications dictated by applications, such as maintaining a smooth and robust output waveform.

118. Prior to the '455 patent, output buffers had limited flexibility in meeting variations arising from different applications. While the drive strength of an earlier output buffer could be increased by adding additional driver devices in parallel, doing so may only just have met a minimum output impedance necessary to reduce signal reflections on a transmission line driven by the buffer.

119. Another disadvantage of earlier output buffers was that they could be sensitive to operating conditions. While an earlier output buffer could be tuned to meet worst case load conditions, if an actual output transmission line was less than such worst case, it could be difficult to meet driving requirements, such as rise time and fall time—particularly across uncontrollable variations in manufacturing process, differing operating voltages, and/or temperatures.

120. The '455 patent teaches, among other things, an output driver comprising a first driver transistor, a first switch element coupled between a first driver control node and a first power supply node, and a selectable current source coupled between the first driver control node and a second

power supply node, wherein the selectable current source includes a plurality of selectable current legs. This solution describes output driver circuits that can, among other things, vary drive strength according to supply voltage conditions and/or provide programmable drive strength. As a result, the output buffer can, among other things, meet performance requirements over a range of operating voltages. Further, programmability of drive strength can also, among other things, enable the output buffer to be configured to provide a desired signal profile despite variations in transmission line load.

121. As an additional exemplary feature, an output buffer can include output driver transistors that can be enabled in response to current sources sinking or sourcing a current that can vary according to supply voltage and/or are programmable. Beneficially, among other things, this allows drive strength of such devices can be varied without increasing or decreasing the number of driver devices.

122. AMD products use an output driver. AMD's Ryzen processors, for example, contain an output driver circuit, such as the output driver and/or pre-driver in the DDR IO circuitry. This has resulted in, among other things, AMD's ability to provide a desired signal profile despite variations in transmission line load.

123. AMD has directly infringed, and continues to directly infringe, one or more claims of the '455 patent under 35 U.S.C. § 271(a), either literally and/or under the doctrine of equivalents, by, among other things, making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the '455 patent, including, but not limited to, products with an output driver and/or pre-driver in the DDR IO circuitry, such as the Ryzen 7 1700 semiconductor device and other products in the Ryzen product family; other AMD semiconductor devices, integrated circuits, and products with an output driver and/or pre-driver; and all other semiconductor devices, integrated circuits, and products with similar infringing technology

("the Accused '455 Products").

124. As one non-limiting example, AMD infringes claim 7 of the '455 patent. For example, the Ryzen 7 semiconductor device contains an output driver circuit comprising:

a. a first driver transistor that provides a low impedance path to an output node (e.g., output of the output driver and/or pre-driver of the Ryzen 7) in response to a voltage at a first driver control node (e.g., gate of a transistor of the Ryzen 7);

b. a first switch element (e.g., transistor switch of the Ryzen 7) coupled between the first driver control node and a first power supply node (e.g., first power supply of the Ryzen 7); and

c. a selectable current source (e.g., selectable transistor current source of the Ryzen 7) coupled between the first driver control node and a second power supply node (e.g., second power supply of the Ryzen 7), the selectable current source generating a drive current that varies in response to a drive select value,

d. wherein the selectable current source includes a plurality of selectable current legs (e.g., transistor current legs of the Ryzen 7), each connected to a current control node and enabled to provide a current to the current control node in response to a corresponding drive control signal (e.g., control signal of the Ryzen 7).

125. Claim 7 of the '455 patent applies to each Accused '455 Product at least because each of those products contain infringing output drivers and/or pre-drivers; and/or contain circuits with similar infringing functionality.

126. Monterey has complied with the requirements of 35 U.S.C. § 287(a) at least because Monterey provided AMD with written notice of its infringement as discussed above.

127. AMD was on notice of the '455 patent under 35 U.S.C. § 287(a) at least as early as

September 24, 2018.

128. AMD, knowing its products infringe the ’455 patent and with the specific intent for others to infringe the ’455 patent, has induced infringement of, and continues to induce infringement of, one or more claims of the ’455 patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, by, among other things, actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import (including import products made by a patented process) in or into the United States without authorization the Accused ’455 Products, as well as products containing the same. AMD knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, such as those located on AMD’s website at www.amd.com/en. For example, AMD provides data sheets, programmer references, design guides, revision guides, diagrams, white papers, and software instructing customers on uses of AMD’s products that infringe the ’455 patent. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf. Additional non-limiting examples include the materials found on AMD’s websites at www.amd.com/en/ryzen-7 and www.amd.com/en/products/cpu/amd-ryzen-7-1700.

129. AMD has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the ’455 patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, by, among other things, selling, offering to sell, and/or importing in or into the United States the Accused ’455 Products, which constitute a material part of the invention of the ’455 patent, knowing the Accused ’455 Products to be especially made or especially adapted for use in an infringement of such patent, and not a staple article or commodity of commerce

suitable for substantial noninfringing use. *See, e.g.*, https://www.amd.com/en/support/tech-docs: https://www.amd.com/system/files/TechDocs/AMD%20Ryzen%20Processor%20and%20AMD%20Ryzen%20Master%20Overclocking%20Users%20Guide.pdf.

130. Monterey has sustained and is entitled to recover damages as a result of AMD's infringement.

131. AMD's infringement of the '455 patent has been knowing, deliberate, and willful, beginning at least as early as November 15, 2019, the date Monterey filed the first complaint in this action and therefore at least the date by which AMD knew of the '455 patent and knew that its conduct constituted and resulted in infringement of the '455 patent. AMD nonetheless has committed—and continues to commit—acts of direct and indirect infringement despite knowing that its actions constituted infringement of the valid and enforceable '455 patent, despite a risk of infringement that was known or so obvious that it should have been known to AMD, and/or even though AMD otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. AMD's conduct in light of these circumstances is egregious. AMD's knowing, deliberate, and willful infringement of the '455 patent entitles Monterey to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

RELIEF REQUESTED

Wherefore, Monterey respectfully requests that this Court enter judgment against AMD as follows:

A. that AMD has infringed each of the Patents-in-Suit;

B. that AMD's infringement of each of the Patents-in-Suit is and has been willful;

C. that Monterey be awarded damages adequate to compensate it for the patent infringement that has occurred, together with pre-judgment interest, post-judgment interest, and costs;

D. that Monterey be awarded an accounting and additional damages for any infringing sales not presented at trial;

E. that Monterey be awarded all other damages permitted by 35 U.S.C. § 284, including without limitation increased damages up to three times the amount of compensatory damages found;

F. that this is an exceptional case and that Monterey be awarded its costs and reasonable attorneys' fees incurred in this action as provided by 35 U.S.C. § 285;

G. that AMD as well as its officers, directors, agents, employees, representatives, attorneys, and all others acting in privity or in concert with them, its subsidiaries, divisions, successors and assigns be permanently enjoined from further infringement of each of the Patents-in-Suit;

H. that, in the event a permanent injunction preventing further infringement of each of the Patents-in-Suit is not granted, Monterey be awarded a compulsory ongoing licensing fee for any such further infringement; and

I. such other relief as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Monterey hereby demands trial by jury on all claims and issues so triable.

Respectfully submitted,

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