IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

HOME SEMICONDUCTOR CORPORATION and PROMOS TECHNOLOGIES, INC., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC, Defendants.	)	C.A. No. _____ **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiffs Home Semiconductor Corporation ("Home") and ProMOS Technologies, Inc. ("ProMOS") (collectively "Plaintiffs") by and through their undersigned counsel, file this Complaint against Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC. (collectively, "Samsung").

THE PARTIES

1. Home Semiconductor is a Delaware corporation having its principal place of business at 3422 Old Capitol Trail, Suite 700, Wilmington, Delaware 19808-6192, U.S.A.

2. ProMOS is a Taiwanese corporation having its principal place of business at 3A3, No.1, Lixing 1st Rd., East Dist., Hsinchu City 300, Taiwan (R.O.C.).

3. Upon information and belief, Samsung Electronics Co., Ltd. ("SEC") is a Korean corporation having its principal place of business at 250 2 Ka Taepyung, Ro Chung Ku, Seoul, Korea M5 100742. On information and belief, SEC is one of the world's largest electronics companies and it designs, manufactures, uses, sells, and offers to sell in, and imports into, the

United States, a range of electronics products, including consumer electronics, mobile phones, entertainment devices (such as TVs), computers, storage devices, and electronic components, such as the infringing semiconductor chips (i.e., DRAM, flash memory, and LSI chips) at issue in this case. Upon information and belief, SEC is the parent company of an extremely complex and complicated ownership structure that includes numerous subsidiaries and related companies and has manufacturing and assembly plants and sales offices and affiliates in more than 80 countries, including Korea and the United States, and employs more than 300,000 workers.

4. Upon information and belief, Samsung Electronics America, Inc. ("SEA") is a New York corporation having its principal place of business at 85 Challenger Road, Ridgefield Park, New Jersey 07660. Upon information and belief, SEA is a wholly-owned subsidiary of SEC and it manufactures, uses, sells, and offers to sell in, and imports into, the United States, a wide variety of electronics products, including consumer electronics, mobile phones, entertainment devices (such as TVs), computers, storage devices, and electronic components, such as the infringing semiconductor chips (i.e., DRAM, flash memory, and LSI chips) at issue in this case.

5. Upon information and belief, Samsung Semiconductor, Inc. ("SSI") is a California corporation having its principal place of business at 3655 North First Street, San Jose, California 95134 or 601 McCarthy Blvd., Milpitas, California 95035. Upon information and belief, SSI is a subsidiary of SEA and it manufactures, uses, sells, offers to sell in, and imports into, the United States a wide variety of electronics products, including electronic components, such as the infringing semiconductor chips (i.e., DRAM, flash memory, and LSI chips) at issue in this case.

6. Upon information and belief, Samsung Austin Semiconductor, LLC. ("SAS") is a

Delaware limited liability corporation having its principal place of business at 12100 Samsung Boulevard, Austin, Texas 78754. Upon information and belief, SAS is a wholly-owned subsidiary of SSI, is one of the Samsung manufacturing facilities and foundry operations in the U.S., and manufactures, uses, sells, and offers to sell in the United States a wide variety of electronics products, including electronic components, such as the infringing semiconductor chips (i.e., LSI chips) at issue in this case.

7. Upon information and belief, Samsung has conducted and regularly conducts business within this District, has purposefully availed itself of the privileges of conducting business in this District, and has sought protection and benefit from the laws of the State of Delaware.

JURISDICTION AND VENUE

8. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq*., including but not limited to 35 U.S.C. §§ 271, 281, 283, 284, and 285. This Court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has personal jurisdiction over SEC. SEC is amenable to service of summons for this action. Furthermore, personal jurisdiction over SEC in this action comports with due process. SEC has conducted and regularly conducts business within the United States and this District. SEC has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SEC has sought protection and benefit from the laws of the State of Delaware by forming one of its United States affiliates in this District and/or by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they

will be purchased by consumers in this District.

10. SEC – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents –sells, offers to sell, and imports its infringing products in the United States and this District. SEC has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SEC knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SEC has committed the tort of patent infringement in this District.

11. This Court has personal jurisdiction over SEA. SEA is amenable to service of summons for this action. Furthermore, personal jurisdiction over SEA in this action comports with due process. SEA has conducted and regularly conducts business within the United States and this District. SEA has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SEA has sought protection and benefit from the laws of the State of Delaware by forming one of its United States affiliates in this District and/or by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

12. SEA – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – makes, uses, sells, offers to sell, and imports its infringing products in the United States and this District. SEA has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness

and/or intent that they will be purchased by consumers in this District. SEA knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SEA has committed the tort of patent infringement in this District.

13. This Court has personal jurisdiction over SSI. SSI is amenable to service of summons for this action. Furthermore, personal jurisdiction over SSI in this action comports with due process. SSI has conducted and regularly conducts business within the United States and this District. SSI has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SSI has sought protection and benefit from the laws of the State of Delaware by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

14. SSI – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – makes, uses, sells, offers to sell, and imports its infringing products in the United States and this District. SSI has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SSI knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SSI has committed the tort of patent infringement in this District.

15. This Court has personal jurisdiction over SAS because SAS is an LLC organized

under the laws of Delaware. SAS is amenable to service of summons for this action. Furthermore, personal jurisdiction over SAS in this action comports with due process. SAS has conducted and regularly conducts business within the United States and this District. SAS has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in the State of Delaware and this District. SAS has sought protection and benefit from the laws of the State of Delaware by forming in this District.

16. SAS – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – makes, uses, sells, and offers to sell its infringing products in the United States and this District. SAS has purposefully and voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. SAS knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, SAS has committed the tort of patent infringement in this District.

17. Venue is proper in this Court according to the venue provisions set forth by 28 U.S.C. §§ 1391(b)-(d) and 1400(b). SAS is an LLC organized under the laws of Delaware, and thus resides in Delaware. Therefore, venue is appropriate in this District pursuant to 28 U.S.C. § 1400(b). Moreover, Samsung is subject to personal jurisdiction in this District, and therefore is deemed to reside in this District for purposes of venue. Upon information and belief, Samsung has committed acts of infringement within this District and has a regular and established place of business within this District, including but not limited to making sales in this District, providing service and support to its respective customers in this District and/or operating an interactive

website, available to persons in this District that advertises, markets, and/or offers for sale infringing products.

BACKGROUND

18. U.S. Patent No. 6,146,997 titled "Method for Forming Self-Aligned Contact Hole" (the "'997 patent") was duly and legally issued by the U.S. Patent and Trademark Office on November 14, 2000, after full and fair examination. Jacson Liu and Jing-Xian Huang are the inventors listed on the '997 patent. The '997 patent expired on September 29, 2019.

19. The '997 patent was originally assigned by the inventors to Mosel Vitelic.

20. In 2004, the '997 patent was assigned to ProMOS.

21. In 2013, ProMOS entered an agreement to assign the '997 patent to Home Semiconductor Corporation, a Samoan corporation that is the parent of the Home plaintiff. It was the parties' intent to make this assignment to Home Semiconductor Corporation. Due to a typographical error, the agreement referenced Home Semiconductor Inc., a Samoan company that does not, to Plaintiffs' knowledge, exist. This typographical error was corrected in the First Amendment to the relevant agreement, and which made the transfer of the patents to Home Semiconductor Corporation Samoa effective as of 2013.

22. In September 2013, the '997 patent was assigned to plaintiff Home Semiconductor Corporation, a Delaware corporation that is a wholly owned subsidiary of Home Semiconductor Corporation of Samoa. Plaintiff Home Semiconductor Corporation holds all rights, title, and interest in the '997 patent, including the right to collect and receive damages for past, present and future infringements.

23. In a Report and Recommendation dated January 14, 2020, Magistrate Judge Fallon issued a recommendation that concluded that ProMOS had retained sufficient rights in the

'997 patent to be a necessary party to this lawsuit as a co-plaintiff.

24. A true and correct copy of the '997 patent is attached as Exhibit A and made a part hereof.

COUNT I

Infringement of U.S. Patent No. 6,146,997

25. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-18 as though fully set forth herein.

26. Upon information and belief, SAS during the term of the '997 patent, directly infringed at least claim 2 of the '997 patent under 35 U.S.C. § 271(a) by, without authority, making Samsung semiconductor chips (i.e., LSI chips) within the United States using processes that practice all of the limitations of at least claim 2 of the '997 patent, either literally or under the doctrine of equivalents.

27. Upon information and belief, SEC, SEA, and SSI, during the term of the '997 patent, each directly infringed at least claim 2 of the '997 patent under 35 U.S.C. § 271(g) by, without authority, importing into the United States, and offering to sell, selling, and using within the United States Samsung semiconductor chips (i.e., DRAM, flash memory, and LSI chips) and/or products containing Samsung semiconductor chips where those semiconductor chips are made by processes that practice all of the limitations of at least claim 2 of the '997 patent, either literally or under the doctrine of equivalents.

28. Upon information and belief, Samsung semiconductor chips are manufactured using processes that practice each limitation of at least claim 2 of the '997 patent. These processes are used to manufacture infringing semiconductor chips including, but not limited to, buried channel array transistor DRAM, recess channel array transistor DRAM, NAND flash

memory, V-NAND flash memory, and LSI chips.

29. Upon information and belief, Samsung buried channel array transistor DRAM, including but not limited to the Samsung DRAM K4A8G085WC, are manufactured using processes that practice each limitation of at least claim 2 of the ’997 patent.

30. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are manufactured using a process that forms a polysilicon gate electrode on a semiconductor substrate, where the substrate has areas next to the gate electrode for the source/drains, the diffusion regions.

31. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are also made using a process that forms an oxide layer on the sidewalls of the polysilicon gate electrode and over the surface of the silicon substrate, including the diffusion region. Upon information and belief, the process is a thermal oxidation process where the semiconductor wafer having polysilicon gate electrodes on the semiconductor substrate is exposed to heat in the presence of oxygen, forming the oxide layer. Upon information and belief, this thermal oxidation process occurs before the formation the silicon nitride etch barrier layer.

32. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are also made using a process that forms a conformal silicon nitride etch barrier layer overlying the gate electrode and substrate surface. Upon information and belief, the process is a chemical vapor deposition process that deposits silicon nitride onto the semiconductor wafer such that the deposited layer overlies the gate electrodes and substrate surfaces. Upon information and belief, the deposited silicon nitride layer functions as an etch barrier during the contact etch process.

33. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are also made using a process that forms an insulating layer overlying the silicon nitride etch barrier layer and the other structures on the substrate. Upon information and belief, the process deposits insulating material(s) such as silicon oxide onto the semiconductor wafer such that the material(s) overlie the silicon nitride etch barrier layer.

34. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are also made using a process that etches a contact opening so that a contact can be formed. Upon information and belief, a mask structure is formed, patterned, and used for the contact etch. Upon information and belief, the etching process etches the insulating material (i.e., silicon oxide) preferentially over silicon nitride and etches an opening through the insulating layer self-aligned and borderless to the diffusion region, where the opening formed in the insulting layer by the etch process is aligned by the silicon nitride etch barrier layer in addition to the mask and has no contact borders. Upon information and belief, the etch process does not etch through the silicon nitride etch barrier layer, using it as an etch stop.

35. Upon information and belief, Samsung buried channel array transistor DRAM, including at least the structures in the peripheral region of the chip, are also made using a process that anisotropically etches the silicon nitride etch barrier layer underneath the opening, exposing the diffusion region. Upon information and belief, the anisotropic etch process preferentially etches in the vertical direction and does not etch away the silicon nitride etch barrier layer on the sidewalls, and so, simultaneously, this same process step also forms a spacer of the silicon nitride etch barrier material on the sidewall of the gate electrode.

36. Upon information and belief, Samsung recessed channel array transistor DRAM, including but not limited to the Samsung DRAM K4T1G084QF, are manufactured using processes that practice each limitation of at least claim 2 of the ’997 patent.

37. Upon information and belief, Samsung recess channel array transistor DRAM, including at least the structures in the cell array region of the chip, are manufactured using a process that forms a polysilicon gate electrode on a semiconductor substrate, where the substrate has areas next to the gate electrode for the source/drains, the diffusion regions.

38. Upon information and belief, Samsung recess channel array transistor DRAM, including at least the structures in the cell array region of the chip, are also made using a process that forms an oxide layer on the sidewalls of the polysilicon gate electrode and over the surface of the silicon substrate, including the diffusion region. Upon information and belief, the process is a thermal oxidation process where the semiconductor wafer having polysilicon gate electrodes on the semiconductor substrate is exposed to heat in the presence of oxygen, forming the oxide layer. Upon information and belief, this thermal oxidation process occurs before the formation the silicon nitride etch barrier layer.

39. Upon information and belief, Samsung recess channel array transistor DRAM, including at least the structures in the cell array region of the chip, are also made using a process that forms a conformal silicon nitride etch barrier layer overlying the gate electrode and substrate surface. Upon information and belief, the process is a chemical vapor deposition process that deposits silicon nitride onto the semiconductor wafer such that the deposited layer overlies the gate electrodes and substrate surfaces. Upon information and belief, the deposited silicon nitride layer functions as an etch barrier during the contact etch process.

40. Upon information and belief, Samsung recess channel array transistor DRAM,

including at least the structures in the cell array region of the chip, are also made using a process that forms an insulating layer overlying the silicon nitride etch barrier layer and the other structures on the substrate. Upon information and belief, the process deposits insulating material(s) such as silicon oxide onto the semiconductor wafer such that the material(s) overlie the silicon nitride etch barrier layer.

41. Upon information and belief, Samsung recess channel array transistor DRAM, including at least the structures in the cell array region of the chip, are also made using a process that etches a contact opening so that a contact can be formed. Upon information and belief, a mask structure is formed, patterned, and used for the contact etch. Upon information and belief, the etching process etches the insulating material (i.e., silicon oxide) preferentially over silicon nitride and etches an opening through the insulating layer self-aligned and borderless to the diffusion region, where the opening formed in the insulting layer by the etch process is aligned by the silicon nitride etch barrier layer in addition to the mask and has no contact borders. Upon information and belief, the etch process does not etch through the silicon nitride etch barrier layer, using it as an etch stop.

42. Upon information and belief, Samsung recess channel array transistor DRAM, including at least the structures in the cell array region of the chip, are also made using a process that anisotropically etches the silicon nitride etch barrier layer underneath the opening, exposing the diffusion region. Upon information and belief, the anisotropic etch process preferentially etches in the vertical direction and does not etch away the silicon nitride etch barrier layer on the sidewalls, and so, simultaneously, this same process step also forms a spacer of the silicon nitride etch barrier material on the sidewall of the gate electrode.

43. Upon information and belief, Samsung NAND flash memory, including but not

limited to the Samsung flash memory K9GDGD8U0B, are manufactured using processes that practice each limitation of at least claim 2 of the ’997 patent.

44. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are manufactured using a process that forms a polysilicon gate electrode on a semiconductor substrate, where the substrate has areas next to the gate electrode for the source/drains, the diffusion regions.

45. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are also made using a process that forms an oxide layer on the sidewalls of the polysilicon gate electrode and over the surface of the silicon substrate, including the diffusion region. Upon information and belief, the process is a thermal oxidation process where the semiconductor wafer having polysilicon gate electrodes on the semiconductor substrate is exposed to heat in the presence of oxygen, forming the oxide layer. Upon information and belief, this thermal oxidation process occurs before the formation the silicon nitride etch barrier layer.

46. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are also made using a process that forms a conformal silicon nitride etch barrier layer overlying the gate electrode and substrate surface. Upon information and belief, the process is a chemical vapor deposition process that deposits silicon nitride onto the semiconductor wafer such that the deposited layer overlies the gate electrodes and substrate surfaces. Upon information and belief, the deposited silicon nitride layer functions as an etch barrier during the contact etch process.

47. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are also made using a process

that forms an insulating layer overlying the silicon nitride etch barrier layer and the other structures on the substrate. Upon information and belief, the process deposits insulting material(s) such as silicon oxide onto the semiconductor wafer such that the materials(s) overlie the silicon nitride etch barrier layer.

48. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are also made using a process that etches a contact opening so that a contact can be formed. Upon information and belief, a mask structure is formed, patterned, and used for the contact etch. Upon information and belief, the etching process etches the insulating material (i.e., silicon oxide) preferentially over silicon nitride and etches an opening through the insulating layer self-aligned and borderless to the diffusion region, where the opening formed in the insulting layer by the etch process is aligned by the silicon nitride etch barrier layer in addition to the mask and has no contact borders. Upon information and belief, the etch process does not etch through the silicon nitride etch barrier layer, using it as an etch stop.

49. Upon information and belief, Samsung NAND flash memory, including at least the source line contact structures in the array region of the chip, are also made using a process that anisotropically etches the silicon nitride etch barrier layer underneath the opening, exposing the diffusion region. Upon information and belief, the anisotropic etch process preferentially etches in the vertical direction and does not etch away the silicon nitride etch barrier layer on the sidewalls, and so, simultaneously, this same process step also forms a spacer of the silicon nitride etch barrier material on the sidewall of the gate electrode.

50. Upon information and belief, Samsung V-NAND flash memory, including but not limited to the Samsung flash memory K9AFGD8J0B, are manufactured using processes that

practice each limitation of at least claim 2 of the ’997 patent.

51. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are manufactured using a process that forms a polysilicon gate electrode on a semiconductor substrate, where the substrate has areas next to the gate electrode for the source/drains, the diffusion regions.

52. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are also made using a process that forms an oxide layer on the sidewalls of the polysilicon gate electrode and over the surface of the silicon substrate, including the diffusion region. Upon information and belief, the process is a thermal oxidation process where the semiconductor wafer having polysilicon gate electrodes on the semiconductor substrate is exposed to heat in the presence of oxygen, forming the oxide layer. Upon information and belief, this thermal oxidation process occurs before the formation the silicon nitride etch barrier layer.

53. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are also made using a process that forms a conformal silicon nitride etch barrier layer overlying the gate electrode and substrate surface. Upon information and belief, the process is a chemical vapor deposition process that deposits silicon nitride onto the semiconductor wafer such that the deposited layer overlies the gate electrodes and substrate surfaces. Upon information and belief, the deposited silicon nitride layer functions as an etch barrier during the contact etch process.

54. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are also made using a process that forms an insulating layer overlying the silicon nitride etch barrier layer and the other structures on the

substrate. Upon information and belief, the process deposits insulting material(s) such as silicon oxide onto the semiconductor wafer such that the material(s) overlie the silicon nitride etch barrier layer.

55. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are also made using a process that etches a contact opening so that a contact can be formed. Upon information and belief, a mask structure is formed, patterned, and used for the contact etch. Upon information and belief, the etching process etches the insulating material (i.e., silicon oxide) preferentially over silicon nitride and etches an opening through the insulating layer self-aligned and borderless to the diffusion region, where the opening formed in the insulting layer by the etch process is aligned by the silicon nitride etch barrier layer in addition to the mask and has no contact borders. Upon information and belief, the etch process does not etch through the silicon nitride etch barrier layer, using it as an etch stop.

56. Upon information and belief, Samsung V-NAND flash memory, including at least the structures in the peripheral region of the chip, are also made using a process that anisotropically etches the silicon nitride etch barrier layer underneath the opening, exposing the diffusion region. Upon information and belief, the anisotropic etch process preferentially etches in the vertical direction and does not etch away the silicon nitride etch barrier layer on the sidewalls, and so, simultaneously, this same process step also forms a spacer of the silicon nitride etch barrier material on the sidewall of the gate electrode.

57. Upon information and belief, Samsung LSI chips, including but not limited to the Samsung LSI chips NFC Controller S3FWRN5X, Image Sensor S5K2G1XX, and DTV chip S4LL136X01, are manufactured using processes that practice each limitation of at least claim 2

of the ’997 patent.

58. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are manufactured using a process that forms a polysilicon gate electrode on a semiconductor substrate, where the substrate has areas next to the gate electrode for the source/drains, the diffusion regions.

59. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are also made using a process that forms an oxide layer on the sidewalls of the polysilicon gate electrode and over the surface of the silicon substrate, including the diffusion region. Upon information and belief, the process is a thermal oxidation process where the semiconductor wafer having polysilicon gate electrodes on the semiconductor substrate is exposed to heat in the presence of oxygen, forming the oxide layer. Upon information and belief, this thermal oxidation process occurs before the formation the silicon nitride etch barrier layer.

60. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are also made using a process that forms a conformal silicon nitride etch barrier layer overlying the gate electrode and substrate surface. Upon information and belief, the process is a chemical vapor deposition process that deposits silicon nitride onto the semiconductor wafer such that the deposited layer overlies the gate electrodes and substrate surfaces. Upon information and belief, the deposited silicon nitride layer functions as an etch barrier during the contact etch process.

61. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are also made using a process that forms an insulating layer overlying the silicon nitride etch barrier layer and the other structures on the substrate. Upon information and

belief, the process deposits insulting material(s) such as silicon oxide onto the semiconductor wafer such that the material(s) overlie the silicon nitride etch barrier layer.

62. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are also made using a process that etches a contact opening so that a contact can be formed. Upon information and belief, a mask structure is formed, patterned, and used for the contact etch. Upon information and belief, the etching process etches the insulating material (i.e., silicon oxide) preferentially over silicon nitride and etches an opening through the insulating layer self-aligned and borderless to the diffusion region, where the opening formed in the insulting layer by the etch process is aligned by the silicon nitride etch barrier layer in addition to the mask and has no contact borders. Upon information and belief, the etch process does not etch through the silicon nitride etch barrier layer, using it as an etch stop.

63. Upon information and belief, Samsung LSI chips, including at least the MOS contact structures, are also made using a process that anisotropically etches the silicon nitride etch barrier layer underneath the opening, exposing the diffusion region. Upon information and belief, the anisotropic etch process preferentially etches in the vertical direction and does not etch away the silicon nitride etch barrier layer on the sidewalls, and so, simultaneously, this same process step also forms a spacer of the silicon nitride etch barrier material on the sidewall of the gate electrode.

64. Upon information and belief, SEC, SEA, SSI, and SAS had knowledge of the ’997 patent and its infringing conduct at least since October 24, 2013, when SEC was placed on notice of its infringement of the ’997 patent in a letter sent to representatives of SEC.

65. Upon information and belief, SEC, SEA, and SSI, during the term of the ’997 patent, each directly infringed at least claim 2 of the ’997 patent by inducing infringement under

35 U.S.C. § 271(b) by, without authority, advertising, promoting, marketing, directing or instructing how to use, offering to sell and/or selling Samsung semiconductor chips (i.e., DRAM, flash memory, and LSI chips) and/or products containing Samsung semiconductor chips where those semiconductor chips are made by processes that practice all of the limitations of one or more claims of the ’997 patent, including at least claim 2, either literally or under the doctrine of equivalents.

66. Upon information and belief, Samsung knew that importing into the United States, and offering to sell, selling, and using within the United States the Samsung semiconductor chips and/or products containing those chips infringed the ’997 patent because Samsung knew that its semiconductor chips were manufactured by processes that practiced one or more claims of the ’997 patent. Upon information and belief, Samsung knew about its infringing conduct since receiving notice of infringement in October 2013. Home also sued Samsung for infringement in December 2013 and subsequently provided contentions detailing how Samsung’s manufacturing processes practiced the ’997 patent claims. Further, Samsung sought *inter partes* review of the ’997 patent in December 2014, asserting interpretations of the ’997 claims that, when applied to the Samsung manufacturing processes, would establish infringement. Thus, Samsung knew that its manufacture of semiconductor chips (i.e., DRAM, flash memory, and LSI chips) practiced the claims the ’997 patent and would result in infringement.

67. Upon information and belief, since at October 24, 2013, when Home placed SEC on notice of its infringement, SEC, SEA, and SSI have induced, under 35 U.S.C. § 271(b), customers and/or consumers to directly infringe one or more claims of the ’997 patent. SEC, SEA, and SSI do so with knowledge, or with willful blindness of the fact, that the induced acts

constitute infringement of the ’997 patent. Upon information and belief, SEC, SEA, and SSI intend to cause infringement by these customers and/or consumers. SEC, SEA, and SSI have taken affirmative steps to induce infringement by, inter alia, creating advertisements that promote the infringing products, creating an established distribution channel for these products into and within the United States, manufacturing these products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States. Upon information and belief, these customers and/or consumers do directly infringe one or more claims of the ’997 patent by importing into the United States, and offering to sell, selling, and using within the United States Samsung semiconductor chips (i.e., DRAM, flash memory, and LSI chips) and/or products containing Samsung semiconductor chips where those semiconductor chips are made by processes that practice all of the limitations of at least claim 2 of the ’997 patent, either literally or under the doctrine of equivalents.

Samsung’s Willful Infringement

68. Samsung’s infringement of the ’997 patent has been and continues to be willful. Home gave Samsung notice of its infringement of the ’997 patent at least as early as October 24, 2013 when it sent a notice letter to a representative of SEC. Shortly thereafter, on December 16, 2013, Home sued Samsung (*Home Semiconductor Corp. v. Samsung Electronics Co., Ltd. et al.*, Case 1:13-cv-02033-RGA (“Home 1”)) asserting that Samsung’s manufacture of DRAM, flash memory, and LSI chips infringed the ’997 patent.

69. Afterwards, in May 2014, Home offered to license the ’997 patent to Samsung – which Samsung declined.

70. On October 24, 2014, Home served Samsung with detailed infringement contentions in Home 1. These contentions described how Samsung's manufacture of DRAM, flash memory, and LSI chips infringed the claims of the '997 patent, including the claims asserted in this present case. The contentions were based upon and cited to Samsung's technical documentation for its manufacturing processes.

71. In November 2014 and June 2015, Home again offered to license the '997 patent to Samsung. Samsung continued to decline the offers.

72. On December 17, 2014, Samsung sought cancellation of the asserted claims through *inter partes* review before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. During the *inter partes* review process, Samsung read the '997 claims broadly, asserting interpretations that, when applied to Samsung's own manufacturing processes, would establish infringement of the asserted claims. Thus, Samsung understood that its manufacture of DRAM, flash memory, and LSI chips would infringe any surviving claims of the '997 patent. On July 25, 2017, the Federal Circuit confirmed the patentability of claims 2 and 9-14 of the '997 patent.

73. On October 18, 2017 and again on December 7, 2017, Home again had discussions where Home offered to license the '997 patent to Samsung. Again, Samsung declined to take a license.

74. On May 16, 2018 and again on March 19, 2019, Home served Samsung with additional infringement contentions, providing a detailed comparison of the accused processes with claims 2 and 9-14.

75. Further confirmation of Samsung's infringement came on August 21, 2019 when the District Court in Home 1 issued a claim construction order construing the '997 disputed

claim terms. The Court's construction, when properly applied, further establishes Samsung's infringement, consistent with Home's long-standing infringement contentions.

76. On September 26, 2019, Home and Samsung again discussed the potential for a license that covered the '997 patent. The parties could not agree on terms.

77. Samsung has had notice of its infringement of the '997 patent since October 2013. Since that time, Home sued Samsung and provided detailed descriptions of Samsung's infringement based on Samsung's own manufacturing documents. Samsung has further taken positions during the '997 *inter partes* review, that are sufficiently broad as to establish infringement. The Federal Circuit has confirmed the patentability of the asserted claims and the Home 1 claim construction order establishes clear infringement, consistent with Home's long-standing infringement allegations. Despite all this, Samsung has refused a license and continues infringe the patents-in-suit. Accordingly, Samsung's infringement of the '997 patent has been willful.

JURY DEMAND

78. Plaintiffs hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

79. Plaintiffs are entitled to recover from Samsung the damages sustained by Plaintiffs as a result of Samsung's wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

80. Plaintiffs have incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute create an exceptional case within

the meaning of 35 U.S.C. § 285, and Plaintiffs are entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

81. Plaintiffs respectfully request that the Court find in their favor and against Samsung, and that the Court grant Plaintiffs the following relief:

A. A judgment that Samsung has infringed the patent-in-suit as alleged herein;

B. A judgment and order for an accounting of all damages sustained by Plaintiffs as a result of the acts of infringement by Samsung;

C. A judgment and order requiring Samsung to pay post-trial damages in the form of a court-determined royalty;

D. A judgment and order requiring Samsung to pay Plaintiffs damages and any royalties determined to be appropriate pursuant to 35 U.S.C. § 284;

E. A judgment and order requiring Samsung to pay Plaintiffs increased damages under 35 U.S.C. § 284 for Samsung's willful infringement;

F. A judgment and order requiring Samsung to pay Plaintiffs pre-judgment and post-judgment interest on the damages awarded;

G. A judgment and order finding this to be an exceptional case and requiring Samsung to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. § 285; and

H. Such other and further relief as the Court deems just and equitable.

Respectfully submitted,

Dated: March 10, 2020

MCCARTER ENGLISH, LLP

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