IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

BELL SEMICONDUCTOR, LLC, Plaintiff, v. NXP SEMICONDUCTORS, N.V.; NXP, B.V.; and NXP USA, INC., Defendants.	Civil Action No. 6:20-cv-00210 **JURY TRIAL DEMANDED**

BELL SEMICONDUCTOR, LLC'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Bell Semiconductor, LLC ("Bell Semic") as and for its complaint against NXP Semiconductors, N.V.; NXP, B.V.; and NXP USA, Inc., alleges as follows:

INTRODUCTION

1. Bell Semic is a technology and intellectual property licensing company. Bell Semic's patent portfolio comprises over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world's leading semiconductor technology innovators, including AT&T Bell Laboratories, Lucent Technologies (Lucent), Agere Systems (Agere), LSI Logic and LSI Corporation (LSI). The portfolio reflects expertise developed at the various R&D laboratories and manufacturing locations of these companies around the world. The technology created, developed, and patented at those companies underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables,

digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors and wireless connectors.

2. Bell Semic was formed in 2017 to manage this portfolio of semiconductor-related intellectual property acquired from Broadcom and assigned to Bell Semic. Several Bell Semic executives previously served as engineers and in leadership roles within the intellectual property departments of Lucent, Agere, LSI, Avago Technologies (Avago), and Broadcom. As a result, Bell Semic executives were personally involved in creating, patenting, and licensing various aspects of the portfolio even before Broadcom assigned it to Bell Semic, including:

- Bell Semic's Chief Executive Officer and Board Member, Mr. John Veschi, served as General Manager of the Intellectual Property business at LSI, had similar responsibilities at Agere, and began his in-house intellectual property experience with the formation of Lucent.
- Bell Semic's President and General Counsel, Mr. Chad Hilyard, served as Managing IP Counsel and in other roles at LSI and Agere, where he was involved in licensing many of the patents in the portfolio now assigned to Bell Semic;
- Bell Semic's Chief Technology Officer, Dr. Sailesh Merchant was a Fellow at Broadcom, Avago, and LSI Corporation; a Distinguished Engineer at LSI Corporation; and a Distinguished Member of the Technical Staff of Agere and Lucent. Dr. Merchant is also a Senior Member of the IEEE and an inventor on more than 250 worldwide patents—including many of the patents in Bell Semic's portfolio—and three of the patents asserted in this Complaint;
- Bell Semic's Senior Director for IP, Mr. Kouros Azimi, served as Director of Intellectual Property at Avago/Broadcom; a Patent Engineer and Director of Patent Development at

LSI/Avago Technologies; and a Member of the Technical Staff at Agere, Lucent, and AT&T Bell Labs. Mr. Azimi is also a Senior Member of the IEEE.

3. Defendants NXP Semiconductors, N.V. ("NXP NV"); NXP, B.V. ("NXP BV"); and NXP USA, Inc. ("NXP USA") (collectively, "NXP" or "Defendants") have infringed and continue to infringe Bell Semic's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. NXP's customers incorporate those products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States and within this District. Such downstream products include, but are not limited to, the NXP 80V18 PN80V near field communications (NFC) controller used in the iPhone X; the NXP LS1088AXN7Q1A QorIQ Layerscape communications processor used in high-performance open virtual edge appliance platforms; and NXP's MWCT1012CFM wireless charging transmitter used in handheld consumer applications.

4. Bell Semic has notified NXP of its infringement in writing multiple times since January 2019 and provided detailed claim charts showing NXP's infringement of numerous Bell Semic patents by numerous different NXP semiconductor devices, but NXP has failed to provide a substantive response and has otherwise refused to have a meeting with Bell Semic to discuss licensing of the Bell Semic portfolio, including the infringed Bell Semic patents. Instead, NXP has continued to infringe, and thus its infringement is and has been willful under the Patent Act.

NATURE OF THE CASE

5. This action arises under 35 U.S.C. § 271 for NXP's infringement of Bell Semic's United States Patent Nos. 8,049,340 ("the Hall 340 Patent"); 8,288,269 ("the Hall 269 Patent"); 7,566,964 ("the Kang Patent"); 6,281,129 ("the Merchant Patent"); 6,596,639 ("the Easter Patent"); 6,153,543 ("the Chesire Patent"); 6,743,669 ("the Lin Patent"); 6,544,907 ("the Ma

Patent"); 6,342,734 ("the Allman Patent"); and 6,960,836 ("the Bachman Patent") (collectively, Bell Semic's "Asserted Patents").

PARTIES

6. Bell Semiconductor, LLC is a Delaware limited liability company with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

7. On information and belief, NXP Semiconductors, N.V. ("NXP NV") is a Dutch public company with limited liability (nammloze vennootschap) organized under the laws of the Netherlands with a global headquarters at 60 High Tech Campus, Eindhoven, Netherlands, 5656 AG. NXP Semiconductors, N.V.'s only material assets are the direct ownership of 100% of the shares of NXP, B.V.

8. On information and belief, NXP, B.V. ("NXP BV") is a Dutch private company with limited liability (besloten vennootschap met beperkte aansprakelijkheid) organized under the laws of the Netherlands with a place of business at 60 High Tech Campus, Eindhoven, Netherlands, 5656 AG.

9. On information and belief, NXP USA, Inc. ("NXP USA") is a corporation organized under the laws of Delaware, with a principal place of business at 6501 William Cannon Drive West, Austin, TX 78735. NXP USA, Inc. may be served with process through its registered agent Corporation Service Company d/b/a CSC - Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

10. On information and belief, NXP USA was formerly known as Freescale Semiconductor, Inc. Upon NXP's merger with Freescale in 2016, Freescale Semiconductor, Inc. changed its name to NXP USA and became NXP NV's registered agent in the United States.

11. NXP is a global semiconductor company that designs, manufactures, and provides to the United States and other markets a wide variety of semiconductors that are used in a wide-

range of end-market applications, such as automotive, industrial and Internet of Things (IOT), mobile, and communication infrastructure.

JURISDICTION AND VENUE

12. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

13. This Court has personal jurisdiction over NXP NV and NXP BV. NXP NV and NXP BV have purposefully and voluntarily availed themselves of the privileges of conducting business in the United States, in the State of Texas, and in the Western District of Texas by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they, or third party products incorporating them, will be purchased by consumers in the Western District of Texas. NXP NV has also established NXP USA, headquartered within the Western District of Texas, as its "registered agent in the United States." NXP NV and NXP BV through intermediaries (including customers, distributors, sales agents, and others), ship, distribute, offer for sale, sell, advertise, and/or use its products (including, but not limited to, the products that are accused of patent infringement in this lawsuit), and/or products incorporating these products, in the United States, the State of Texas, and the Western District of Texas.

14. This Court has personal jurisdiction over NXP USA at least because NXP USA is a resident of Texas as defined by Texas law. NXP USA is also subject to this Court's specific and general personal jurisdiction because NXP USA has sufficient minimum contacts within the State of Texas and this District, pursuant to due process and/or the Texas Long Arm Statute. NXP USA is headquartered in the State of Texas and in this District, and NXP USA has conducted and continues to regularly conduct business within the State of Texas. NXP USA is

registered to do business within the State of Texas and maintains an agent for service of process in Texas. NXP USA has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Texas, and in the Western District of Texas by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in the United States and in the Western District of Texas. NXP USA directly and/or through intermediaries (including distributors, sales agents, and others), ships, distributes, offers for sale, sells, advertises, and/or uses its products (including, but not limited to, the products that are accused of patent infringement in this lawsuit) in the United States, the State of Texas, and the Western District of Texas.

15. NXP USA has derived substantial revenues from its infringing acts occurring within the United States, the State of Texas and within this District.

16. Venue is proper as to NXP NV and NXP BV under 28 U.S.C. § 1391(c)(3) in that they are not residents of the United States and may, therefore, be sued in any judicial district. *Brunette Mach. Works, Ltd. v. Kockum Indus., Inc.,* 406 U.S. 706, 714 (1972).

17. Venue is proper as to NXP USA under 28 U.S.C. § 1400(b) because it has committed acts of infringement in this District and has regular and established places of business within this District. *TC Heartland LLC v. Kraft Foods Grp. Brands LLC*, 137 S. Ct. 1514, 1521 (2017). Specifically, NXP maintains its "Oak Hill" facility at 6501 William Cannon Drive West, Austin, TX 78735, and its 960,000 square foot "Ed Bluestein" facility at 3501 Ed Bluestein Blvd., Austin, TX 78721.

18. NXP USA has not disputed this District's personal jurisdiction over it in other recent patent infringement actions, nor has NXP USA disputed that venue is proper as to it in the

Western District of Texas. *See, e.g.*, *Bicameral LLC v. NXP USA, Inc., et al.,* Case No. 6:18-cv-00294 (W.D. Tex.), Dkt. 25 at ¶¶ 10-11.

19. Joinder of NXP NV, NXP BV, and NXP USA is proper because they are related parties who are either jointly and severally liable for infringement, or who make, use, sell, offer for sale, or import the same or similar accused products that practice the same Asserted Patents. On information and belief, NXP BV and NXP USA are wholly owned subsidiaries of NXP NV. Further, on information and belief, NXP NV, NXP BV, and NXP USA use the same underlying hardware and/or software in their infringing products and therefore the factual question of infringement will substantially overlap between NXP NV, NXP BV, and NXP USA. Further, Plaintiff anticipates that there will be substantial overlap during the discovery process.

20. NXP has committed acts of infringement in this District giving rise to this action and does business in this District, including making sales and/or providing service and support for its respective customers in this District. NXP purposefully and voluntarily sold one or more of the infringing products with the expectation that they would be purchased by consumers in this District and/or incorporated into products that would be purchased by consumers in this District. These infringing products have been and continue to be purchased by consumers in this District. NXP has committed acts of patent infringement within the United States, the State of Texas, and the Western District of Texas.

BELL SEMIC'S ASSERTED PATENTS

A. U.S. Patent No. 8,049,340 (Hall 340 Patent)

21. Bell Semic is the owner by assignment of U.S. Patent No. 8,049,340 ("the Hall 340 Patent"), owns all right, title, and interest in the Hall 340 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 340 Patent

is entitled "Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package." A true and correct copy of the Hall 340 Patent is attached as **Exhibit A**.

22. The inventors of the Hall 340 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

23. The application for the Hall 340 Patent was filed on March 22, 2006, and it duly and properly issued as a patent on November 1, 2011.

24. As of March 2020, the Hall 340 Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 2 patents and published applications filed by leading technology companies Alcatel Lucent and Intel.

B. U.S. Patent No. 8,288,269 (Hall 269 Patent)

25. Bell Semic is the owner by assignment of U.S. Patent No. 8,288,269 ("the Hall 269 Patent"), owns all right, title, and interest in the Hall 269 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 269 Patent is entitled "Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package." The Hall 269 Patent issued on October 16, 2012. A true and correct copy of the Hall 269 Patent is attached as **Exhibit B**.

26. The inventors of the Hall 269 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

27. The application for the Hall 269 Patent was filed on October 4, 2011, and claims priority to the application leading to the Hall 340 Patent, which was filed on March 22, 2006. The Hall 269 Patent issued as a patent on October 16, 2012.

C. U.S. Patent No. 7,566,964 (Kang Patent)

28. Bell Semic is the owner by assignment of U.S. Patent No. 7,566,964 ("the Kang Patent"), owns all right, title, and interest in the Kang Patent; and holds the right to sue and

recover damages for infringement thereof, including past infringement. The Kang Patent is entitled "Aluminum Pad Power Bus and Signal Routing for Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures." A true and correct copy of the Kang Patent is attached as **Exhibit C**.

29. The inventors of the Kang Patent are Seung H. Kang, Roland P. Krebs, Kurt George Steiner, Michael C. Ayukawa, and Dr. Sailesh M. Merchant.

30. The application for the Kang Patent was filed on September 30, 2003, and it claims priority to Provisional Application No. 60/462,504, filed on April 10, 2003. The Kang Patent issued as a patent on July 28, 2009.

31. As of March 2020, the Kang Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 2 patents and published applications filed by leading technology companies such as IBM, Texas Instruments, Renesas, and Advanced Semiconductor Engineering.

D. U.S. Patent No. 6,281,129 (Merchant Patent)

32. Bell Semic is the owner by assignment of U.S. Patent No. 6,281,129 (the "Merchant Patent"), owns all right, title, and interest in the Merchant Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Merchant Patent is entitled "Corrosion-Resistant Polishing Pad Conditioner." A true and correct copy of the Merchant Patent is attached as **Exhibit D.**

33. The inventors of the Merchant Patent are Dr. Sailesh M. Merchant, William G. Easter, and John A. Maze.

34. The application for the Merchant Patent was filed on September 20, 1999, and it issued as a patent on August 28, 2001.

35. As of March 2020, the Merchant Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 22 patents and published applications.

E. U.S. Patent No. 6,596,639 (Easter Patent)

36. Bell Semic is the owner by assignment of U.S. Patent No. 6,596,639 (the "Easter Patent"), owns all right, title, and interest in the Easter Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Easter Patent is entitled "Method for Chemical/Mechanical Planarization of a Semiconductor Wafer Having Dissimilar Metal Pattern Densities." A true and correct copy of the Easter Patent is attached as **Exhibit E.**

37. The inventors of the Easter Patent are William G. Easter, Sudhanshu Misra, and Vivek Saxena.

38. The application for the Easter Patent was filed on October 8, 1999, and it issued as a patent on July 22, 2003.

39. As of March 2020, the Easter Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 8 patents and published applications filed by leading technology companies such as IBM, STMicroelectronics, Intel, Facebook and Micron Technology.

F. U.S. Patent No. 6,153,543 (Chesire Patent)

40. BSL is the owner by assignment of U.S. Patent No. 6,153,543 (the "Chesire Patent"). The Chesire Patent is entitled "High Density Plasma Passivation Layer and Method of Application." A true and correct copy of the Chesire Patent is attached as **Exhibit F.**

41. The inventors of the Chesire Patent are Daniel P. Chesire, Edward P. Martin, Jr., Leonard J. Olmer, Barbara D. Kotzias, and Rafael N. Barba.

42. The application for the Chesire Patent was filed on August 9, 1999, and it issued as a patent on November 28, 2000.

43. As of March 2020, the Chesire Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 25 issued patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Nanya, Cypress Semiconductor, Hynix Semiconductor, and Sandisk.

G. U.S. Patent No. 6,743,669 (Lin Patent)

44. Bell Semic is the owner by assignment of U.S. Patent No. 6,743,669 (the "Lin Patent"), owns all right, title, and interest in the Lin Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Lin Patent is entitled "Method of Reducing Leakage Using Si_3N_4 or SiON Block Dielectric Films." A true and correct copy of the Lin Patent is attached as **Exhibit G**.

45. The inventors of the Lin Patent are Hong Lin, Shiqun Gu, and Peter McGrath.

46. The application for the Lin Patent was filed on June 5, 2002, and it issued as a patent on June 1, 2004.

47. As of March 2020, the Lin Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 14 issued patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Samsung, IBM, Fujitsu, and United Microelectronics Corp.

H. U.S. Patent No. 6,544,907 (Ma Patent)

48. Bell Semic is the owner by assignment of U.S. Patent No. 6,544,907 (the "Ma Patent"), owns all right, title, and interest in the Ma Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Ma Patent is entitled

"Method of Forming a High Quality Gate Oxide Layer Having a Uniform Thickness." A true and correct copy of the Ma Patent is attached as **Exhibit H**.

49. The inventors of the Ma Patent are Yi Ma and Edith Yang.

50. The application for the Ma Patent was filed on October 12, 2000, and it issued as a patent on April 8, 2003.

51. As of March 2020, the Ma Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 2 patents and published applications filed by leading technology companies Hynix Semiconductor and Semiconductor Manufacturing International Corp.

I. U.S. Patent No. 6,342,734 (Allman Patent)

52. Bell Semic is the owner by assignment of U.S. Patent No. 6,342,734 (the "Allman Patent"), owns all right, title, and interest in the Allman Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Allman Patent is entitled "Interconnect-Integrated Metal-Insulator-Metal Capacitor and Method of Fabricating Same." A true and correct copy of the Allman Patent is attached as **Exhibit I**.

53. The inventors of the Allman Patent are Derryl D. J. Allman, John Q. Walker, Verne C. Hornback, and Todd A. Randazzo.

54. The application for the Allman Patent was filed on April 27, 2000, and it issued as a patent on January 29, 2002.

55. As of March 2020, the Allman Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 37 issued patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as IBM, Mitsubishi, Samsung, Taiwan Semiconductor Manufacturing Company, Sharp, Philips, Fujitsu, Renesas, and Qualcomm.

J. U.S. Patent No. 6,960,836 (Bachman Patent)

56. Bell Semic is the owner by assignment of U.S. Patent No. 6,960,836 (the "Bachman Patent"), owns all right, title, and interest in the Bachman Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Bachman Patent is entitled "Reinforced Bond Pad." A true and correct copy of the Bachman Patent is attached as **Exhibit J**.

57. The inventors of the Bachman Patent are Mark Adam Bachman, Daniel Patrick Chesire, Dr. Sailesh M. Merchant, John William Osenbach, and Kurt George Steiner.

58. The application for the Bachman Patent was filed on September 30, 2003, and it issued as a patent on November 1, 2005.

59. As of March 2020, the Bachman Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 17 issued patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Texas Instruments, Infineon, Taiwan Semiconductor Manufacturing Company, Northrup Gruman, Renesas, and Fujitsu.

FACTUAL BACKGROUND

60. Bell Semic incorporates the preceding paragraphs as if fully set forth herein.

61. On June 1, 2002, Lucent, having its roots with Bell Laboratories and AT&T Corporation, spun off its microelectronics business as Agere. Agere later merged with LSI Logic forming LSI Corporation in 2007, which was in turn acquired by Avago in 2014. In 2016, Avago purchased Broadcom and assumed its name to become the current Broadcom Inc. In 2017, Broadcom assigned a patent portfolio containing over 1,900 worldwide patents and applications, approximately 1,500 of which are active U.S. patents, to Bell Semic that included patents originally assigned or issued to Bell Labs, Lucent, Agere, LSI Logic, and LSI.

62. Portions of the Bell Semic portfolio are presently licensed and/or were previously licensed to leading technology companies by Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*See supra* ¶ 2.) Portions of the Bell Semic portfolio were also invented and co-invented by other Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*Id.*)

63. Bell Semic's Asserted Patents arise out of the research, conception, creation, and design of innovative technology developed by leading high-technology companies, including LSI Logic, Agere, and LSI Corporation. Prior to their ultimate acquisition by Avago (now Broadcom), those companies were pioneers of innovative semiconductor technology—and made substantial investments into researching, inventing, creating, and manufacturing cutting-edge semiconductor technology. Bell Semic's Asserted Patents are directed to this inventive technology relating to semiconductors, integrated circuits and related products.

64. NXP infringes and has infringed by making, selling, offering to sell, using, and/or importing products (including importing products made by a patented process) throughout the United States. Moreover, NXP works closely with its customers, foundry suppliers, distributors, OEMs, or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and related products. NXP tailors its manufacturing process for its customers and designs its products to be integrated into downstream products. In addition to its own manufacturing, NXP's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States by itself and others further include, without limitation, any one or a combination of: (i) designing specifications for manufacture of NXP's products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of NXP's products; (iii) soliciting and/or sourcing

the manufacture of NXP's products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of their products; (v) enabling and encouraging the use, sale, or importation of their products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

65. NXP provides marketing and/or technical support services for its products from its facilities in the United States. For example, NXP maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for their products. (*See, e.g.*, https://www.nxp.com/.) NXP's publicly-available website also contains datasheets, application notes, fact sheets, and other materials related to its products. (*See* https://www.nxp.com/design/documentation:DOCUMENTATION#/.) For example, NXP's website contains reference designs (https://www.nxp.com/design/designs:REFDSGNHOME#/), spanning at least audio, interfaces, peripherals and logic, power management, processors and microcontrollers, RFID, security and authentication, sensors, and wireless connectivity; development support including design toolboxes, evaluation and development boards, and a library of RF designs (https://www.nxp.com/design/development-boards:EVDEBRDSSYS#/); software including application design software, integrated development environment software, and software development kits (https://www.nxp.com/design/software:SOFTWARE-CENTER#/home/query/~query~/~filter~/popularity/0); and customer support through NXP's support forums (https://community.nxp.com/welcome).

66. In addition to these resources, NXP also provides numerous support resources for the customers of its semiconductor devices in addition to datasheets and application notes, including online and in-person training through NXP Connects and NXP Technology Days

(https://www.nxp.com/design/training:TRAINING-EVENTS#/). This training includes: NXP Connects, which is "a world-class program combining in-depth technical training, a first-look at cutting-edge live demonstrations, and unique opportunities to hear from an array of industry leaders whose technology is shaping the future" (https://www.nxp.com/design/training/nxp-connects:NXP-CONNECTS); "NXP Technology Days," which provide "a deep-dive, technical training program for engineers designing solutions with embedded technology" (https://www.nxp.com/design/training/nxp-technology-days:NXP-TECH-DAYS); and access to commercial support and engineering services (https://www.nxp.com/design/engineering-services:SW-SUPPORT). Moreover, NXP supports an "NXP Partner Directory," which is "a global network of independent engineering companies that offer the vital tools, software, technology, engineering services and training to speed [NXP customer's] design" (https://www.nxp.com/support/support/nxp-partner-directory:PARTNER-DIRECTORY#/).

NXP'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT FROM BELL SEMIC

67. Before filing this lawsuit, Bell Semic notified NXP that Broadcom assigned to Bell Semic a large portfolio of semiconductor patents, identified NXP Technology Nodes that infringe Bell Semic's Asserted Patents, further identified exemplary products from those Technology Nodes that infringe the Asserted Patents, and offered to license those patents to NXP.

68. Specifically, on January 9, 2019, Mr. Hilyard, sent a letter to NXP's Austin, Texas headquarters addressed to Mr. Changhae Park (NXP's Senior Vice President and Chief IP Officer):

> "I am writing to inform you that Bell Semic acquired the semiconductor-related patent assets previously owned by Agere Systems Inc. and LSI Corporation. We understand that both NXP and Freescale have been licensed to at least a portion of these patents in

> the past. As you probably know, this portfolio includes patents originally assigned to Bell Labs and Lucent Technologies, as well as those assigned to Agere and LSI.
>
> As you are most likely aware, the portfolio reflects expertise and inventions developed at various R&D labs and manufacturing facilities associated with these companies around the world . . . The patent portfolio comprises over 3,000 worldwide patents and applications – approximately 2,000 of which are active U.S. patents.
>
> Our records indicate that NXP's most recent license to this portfolio expired at the end of 2014 and Freescale's most recent license to this portfolio expired in October 2016. Because NXP and Freescale have previously enjoyed a license to this portfolio, we believe you understand and appreciate the value of the unique and ground-breaking technologies covered by this patent portfolio.
>
> By way of background, I've previously served as part of the Agere/LSI licensing team. At Bell Semiconductor, I am joined by other former members of the Lucent/Agere/LSI licensing teams, including John Veschi and Sailesh Merchant. We are very familiar with this pioneering patent portfolio and have licensed this portfolio to many of the world's leading semiconductor companies. Our goal is to build upon the amicable licensing history between Lucent/Agere/LSI and NXP and Freescale – as well as the similar relationships we previously established throughout the semiconductor industry. Over the last few months, we have been acquiring NXP products and conducting reverse engineering to establish NXP's use of exemplary patents in the portfolio. Our preliminary analysis evidences that NXP is currently making, using, selling, or offering for sale products that infringe one or more of Bell Semic's patents."

69. Bell Semic's January 9, 2019 letter also provided NXP with notice of infringement by NXP's Technology Nodes and exemplary products from those Nodes, including the Allman, Chesire, Merchant, and Easter Asserted Patents as follows:

Exemplary List of Bell Semic's Patents Infringed by NPX Products

Device	Product Application	Device Type	Technology Node	Allman 6342734	Ali 6591410	Chesire 6153543	Chittipeddi 6207547	Easter 6281129	Easter 6596639	Esry 6406999
PN5180A0HN/C3E	Identification & Security	NFC Reader	0.18um						X	X
TDA18250AHN/C1,557	Media & Audio	Silicon Tuners	0.30um	X	X					
TDF8530TH/N2,118	Media & Audio	Class-D Power Amp (Car radio)	0.18um						X	
NXP 80V18: PN80V	NFC	Bluetooth	0.18um					X		X
ASL2500SHNY	Power Management	Automotive Lighting	0.18um			X		X	X	X
MK70FX512VMJ15	Processors & Microcontrollers	ARM Cortex Processor	90nm					X		
LPC11U35FET48/501	Processors & Microcontrollers	ARM Cortex Processor	90nm			X	X	X	X	X
BGU8009	RF	LNA for GPS	0.35um					X		
FXTH87EH11DT1	Sensors	Tire Pressure Monitoring Sensor	0.25um	X		X	X	X		
FXAS21002CQR1	Sensors	Gyroscope	0.18um	X		X		X	X	X

70. In the January 9, 2019 letter, Bell Semic also proposed having a near-term dialogue with NXP to discuss details about the licensing program and the patent portfolio, as well as providing claim charts.

71. On February 4, 2019, having not received a response, Mr. Hilyard again sent an email to Mr. Park requesting to set up a phone call.

72. On February 8, 2019, Mr. Mark Patrick, Senior Law Director, Intellectual Property at NXP responded, stating "In your letter, Bell Semic claims that Bell Semic's patents are infringed by NXP products. You seek to have a dialogue with NXP about Bell Semic's licensing program and patent portfolio. Prior to any such dialogue, NXP requires that Bell Semic substantiate its accusations by providing claim charts of the Bell Semic patents to NXP for NXP's review and comment."

73. On June 10, 2019, Bell Semic attached a proposed non-disclosure agreement, and stated, "Sorry for the delay in getting back to you. We have been diligently preparing claim

charts for your review. We are now in a position to provide them to you, but we would like to have an NDA in place before we do that. Attached is an NDA for your review and consideration. Please let me know if you have any comments on the draft."

74. On June 12, 2019, NXP responded, "NXP does not enter into confidentiality or other like agreements in connection with patent accusations against NXP. To engage in patent licensing discussions with NXP, Bell Semic would need to provide to NXP the claim charts without any confidentiality requirement or use restriction. However, we do recognize and accept that the claim charts would be provided subject to Rule 408 of the Federal Rules of Civil Procedure."

75. On September 12, 2019, Mr. Hilyard provided claim charts for the Asserted Patents – Allman, Chesire, Merchant, Easter, Hall 340, and Kang, among others. Each of these claim charts provided detailed mappings, including reverse engineering, of the products identified in Bell Semic's January 9, 2019 letter for these Asserted Patents.

76. In the September 12, 2019 emails, Bell Semic requested an in-person meeting at the beginning of October: "Also, as I mentioned previously, we believe a face-to-face meeting to discuss the charts in detail is the best way to proceed. Please let me know if you and your team can meet the first or second week of October. If so, please provide dates and times during those weeks that will work. If you would like to discuss, let me know and we can set-up a call."

77. On October 9, 2019, Bell Semic's Mr. Hilyard sent another email to NXP requesting a meeting, "We would like to schedule a meeting to discuss the claim charts I forwarded to you. Are you and your team available for a meeting the week of October 28 or November 4. We can make most of those days work."

78. On October 12, 2019, NXP responded, stating "It wasn't clear from your prior response that you won't be providing more claim charts. Please confirm that there will be no more claim charts to follow."

79. Bell Semic responded the same day, confirming that there were no new claim charts.

80. On October 15, 2019, NXP responded, stating that NXP was "now able to involve our expert in the review of the charts. We will provide an initial written response, including if an in-person meeting is justified. I can't confirm the timeframe for our response at this moment."

81. On October 25, 2019, NXP responded, "I received an initial response back from our expert that most of the claim charts are incomplete. Here are the particulars:

> '543 Chesire. Page 2 is blank.
> . . .
> '129 Easter. Pages 2 and 3 are blank. No independent claim is asserted (pages 7, 8, 9, 10 and 11 show photos and arrows only).
> . . .
> '734 Allman. Page 2 is blank.
> '639 Easter. Page 2 is blank.
> '964 Kang. Page 2 is blank.
> '340 Hall. Page 2 is blank."

82. On October 30, 2019, "Sorry for the confusion on these. For some reason, a few pictures were deleted when converting to PDF. All the page 2s are just a snapshot of the front page of each patent. They don't have anything to do with the mappings. We are working on fixing the others. We will send shortly."

83. On December 9, 2019, Mr. Hilyard provided the corrected claim charts in four separate emails, and responded, "As I mentioned in my previous email, for the majority of the CCs, the only pictures missing were the front pages of the patent, so you should have been able to review." These claim charts also mapped additional NXP products to the Asserted Patents.

84. On January 8, 2020, having not received a response from NXP, Mr. Hilyard sent another email to NXP to follow up and attempt to set up a meeting to discuss the claim charts.

85. On February 21, 2020, still having not received a response from NXP, Mr. Veschi sent an email to Mr. Patrick from NXP, attaching a letter addressed to Ms. Jennifer Wuamett, NXP's Executive Vice President and General Counsel. Mr. Veschi indicated Bell Semic's desire to "meet in the next two weeks to discuss licensing options if at all possible."

86. Mr. Veschi's letter to Ms. Wuamett stated, "We are following up on our previous communications with NXP Semiconductors regarding the above matter. Since our initial communication in January 2019, we have provided NXP with claim charts illustrating products produced and/or sold by NXP Semiconductors that infringe one or more of the patents within the Bell Semiconductor Portfolio. We have continued our reverse engineering efforts of your products and are providing an updated summary of our infringement analysis to date in the table below. Please let me know your availability for a meeting in the next two weeks to discuss licensing options for the patents and products identified below as well as the broader Bell Semiconductor portfolio."

87. The chart referenced by Mr. Veschi included an identification of numerous NXP products and provided exemplary patents that these products infringed, including an identification of the previously claim charted products:

NXP Device	Product Application	Device Type	Tech Node	Allman 6342734	Bachman 6960836	Bachman 7221173	Chesire 6153543	Chitlipeddi 6207547	Downey 6194323	Easter 6281129	Easter 6596639	Esry 6406999	Kang 7566964	Lin 6743669	Ma 6544907	Miller 6459049	Greenberg 6140710	Govind 6531932	Hall 8288269	Hall 8049340
BGU8009	RF	LNA for GPS	0.35um							X										
TDA18250AHN/C	Media & Audio	Silicon Tuners	0.30um	X						X										
FXTH87EH11DT1	Sensors	Tire Pressure Monitoring Sensor	0.25um	X			X	X		X										
FXAS21002CQR1	Sensors	Gyroscope	0.18um	X			X		X	X	X	X								
PN5180A0HN/C3E	Identification & Security	NFC Reader	0.18um		X				X	X	X	X								
TDF8530TH/N2	Media & Audio	Audio Amplifier	0.18um							X	X									
NXP 80V18: PN80V	NFC	Bluetooth	0.18um		X				X	X	X	X								
ASL2500SHNY	Power Management	Automotive Lighting	0.18um		X		X	X	X	X	X	X								
MK70FX512VMJ15	Processors & Microcontrollers	ARM Cortex Processor	90nm							X			X	X						
LPC11U35FET48	Processors & Microcontrollers	ARM Cortex Processor	90nm				X	X	X	X	X	X								
MWCT1012CFM	Power Management	Wireless Charging IC	90nm							X			X	X						
MCIMX281AVM4B	Processors & Microcontrollers	ARM Automotive Processor	90nm							X			X							
MKW41Z512VHT4	Wireless	Zigbee	90 nm					X		X			X							
NxH2280C1	RF	Radio for Wireless Streaming	90nm			X				X										
MCIMX7S5EVM08SC	Processors & Microcontrollers	Application Processor	28 nm							X				X	X					
PCIMX7D7DVM10SA	Processors & SoC	i.MX 7 Dual: 2x Cortex-A7, Cortex-M4,	28 nm							X				X	X					
PCIMX7U5DVP08SC	Microprocessor	i.MX 7ULP	28 nm							X			X							
FS32V234CMN1VUB	Automotive	Vision Processor	28 nm													X				
MIMXRT1061DVL6A	Microprocessor	ARM Cortex m7 600 mhz	28 nm							X			X							
MIMX8MM6DVTLZAA	Microprocessor	i.MX 8M Mini - ARM Cortex-A53, Cortex-M4	14 nm Finfet							X					X					
NTAG210	RFID	NTAG 21x, NFC Forum Type 2 Tag						X												
LPC11U37FBD48/401	Processors & Microcontrollers	LPC Cortex	48 LQFP							X										
MIMX8MQ6DVAJZAA	Processors & Microcontrollers	Quad Applications Processor	FCBGA													X			X	X
MCIMX6QP4AVT1AA	Processors & Microcontrollers	Application Processor	624 FCBGA																X	X
LS1088AXN7Q1A	Processors & Microcontrollers	Communications Processor	780 FBGA																X	X
MPC8543VJANGD	Processors & Microcontrollers	PowerQUICC III Processor	783 BGA																X	X
BSC9131NXN1KHKB	Processors & Microcontrollers	Multicore Baseband Processor	FCBGA													X	X	X		

X January 9, 2019 Notice
X + X Claim charts sent (September 12, 2019 and December 9, 2019)
X February 21, 2020 Notice

88. Despite Bell Semic's continuous and repeated efforts since January 9, 2019, NXP has thus far refused to engage in any meaningful discussions to end their infringement of Bell Semic's Asserted Patents with a license. Thus, NXP continues to knowingly and willfully infringe Bell Semic's Asserted Patents directly, contributorily, and by inducement—to obtain the substantial benefits of those inventions without a license from Bell Semic. Bell Semic is thus left with no other choice but to seek relief from this Court.

COUNT 1

Willful Infringement of U.S. Patent No. 8,049,340 (Hall 340 Patent)

89. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

90. The Hall 340 Patent is generally related to an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board. (*See* Hall 340 Patent, Abstract.)

91. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the NXP MIMX8MQ6DVA described below includes 621 pins). In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 340 Patent teaches the use of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

92. The Hall 340 Patent contains 3 independent claims and 19 total claims, covering various integrated circuit package substrates. Claim 12 reads:

An integrated circuit package substrate, comprising:

a first layer comprising a plurality of rows of electrical contacts;

a plurality of electrically conductive layers disposed immediately proximate the first layer;

a plurality of dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other, and

a plurality of rows of cutouts formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers.

93. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Hall 340 Patent (*e.g.*, claims 1, 4, 5, and 12-13),[1] including, but not limited to:

- NXP products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts;
- NXP's MIMX8MQ6DVA, an NXP i.MX 8M Quad processor that includes a quad Arm Cortex-A53 core for use in consumer products;
- NXP's MCIMX6QP4AVT1AA, an NXP i.MX 6 series 32-bit MPU that includes a quad Arm Cortex-A9 core;
- NXP's LS1088AXN7Q1A, an NXP QorIQ Layerscape communications processor;

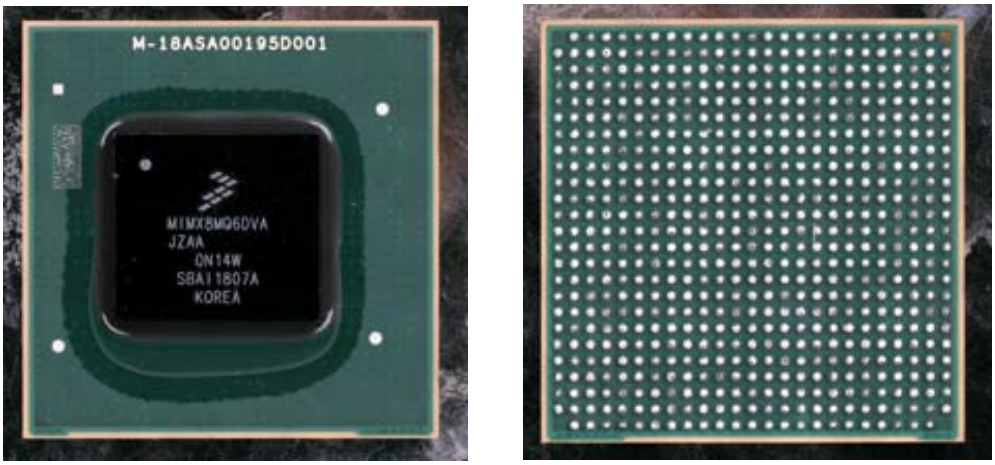
[1] Throughout this Complaint, wherever Bell Semic identifies specific claims of the Asserted Patents that NXP infringes, Bell Semic expressly reserves the right to identify additional asserted claims and products in its infringement contentions in accordance with the local patent rules. Specifically identified claims throughout this Complaint are provided for notice pleading only and are not presented as "exemplary" claims of all other claims for any Asserted Patent.

- NXP's MPC8543VJANGD, an NXP PowerQUICC III processor with high-speed connectivity; and
- NXP's devices that are variants of the above-identified products;

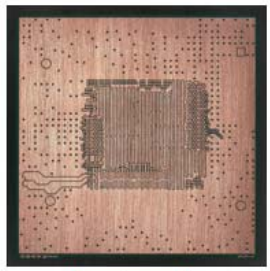
(collectively, the "Hall 340 Accused Products").

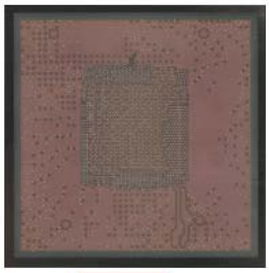
94. By way of non-limiting example only, NXP's MIMX8MQ6DVA infringes claim 12 of the Hall 340 Patent because it is an integrated circuit that has an integrated circuit package substrate with (1) a first layer that has two or more rows of electrical contacts; (2) two or more electrically conductive layers disposed immediately proximate the first layer; (3) two or more dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other; and (4) two or more rows of cutouts formed in each of the two or more electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the two or more electrically conductive layers.

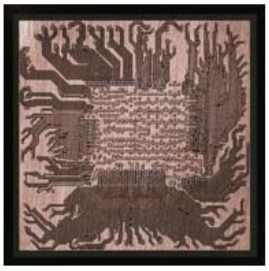
95. As shown below, NXP's MIMX8MQ6DVA is an integrated circuit with an integrated circuit package substrate.



96. The integrated circuit package substrate of the NXP MIMX8MQ6DVA has 6 metal layers and 5 via layers.

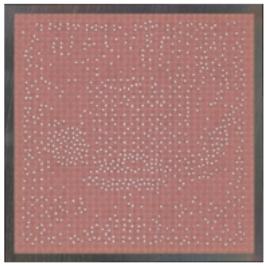

Metal Layer 1


Via Layer 1

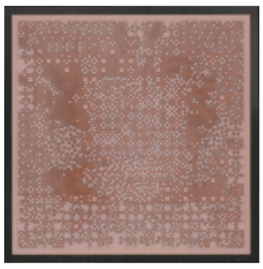

Metal Layer 2


Via Layer 2

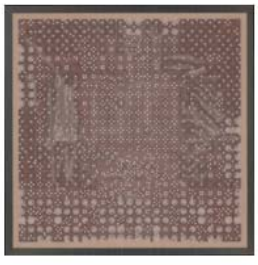

Metal Layer 3

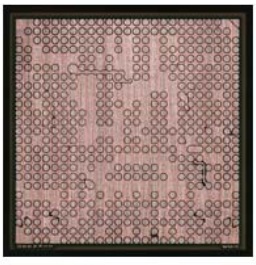

Via Layer 3


Metal Layer 4

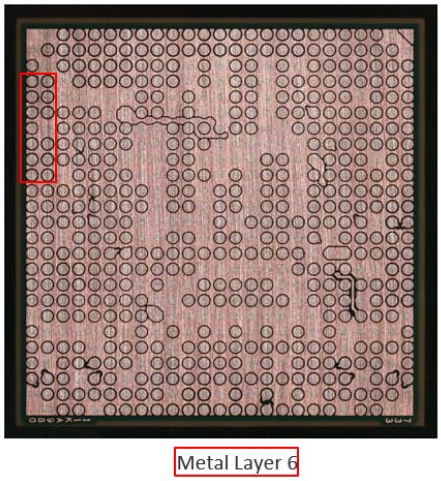

Via Layer 4


Metal Layer 5

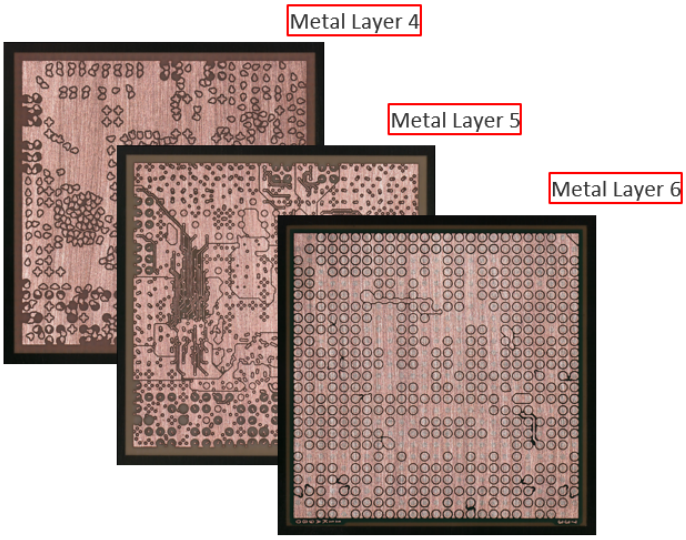

Via Layer 5


Metal Layer 6

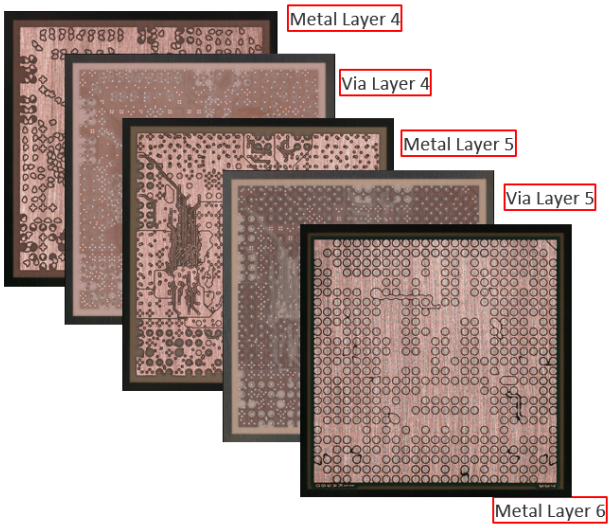
97. The first layer (metal layer 6) of the NXP MIMX8MQ6DVA has a plurality of rows of electrical contacts and forms the ball grid array layer with solder balls, removed for clarity (for example, as indicated in red below).



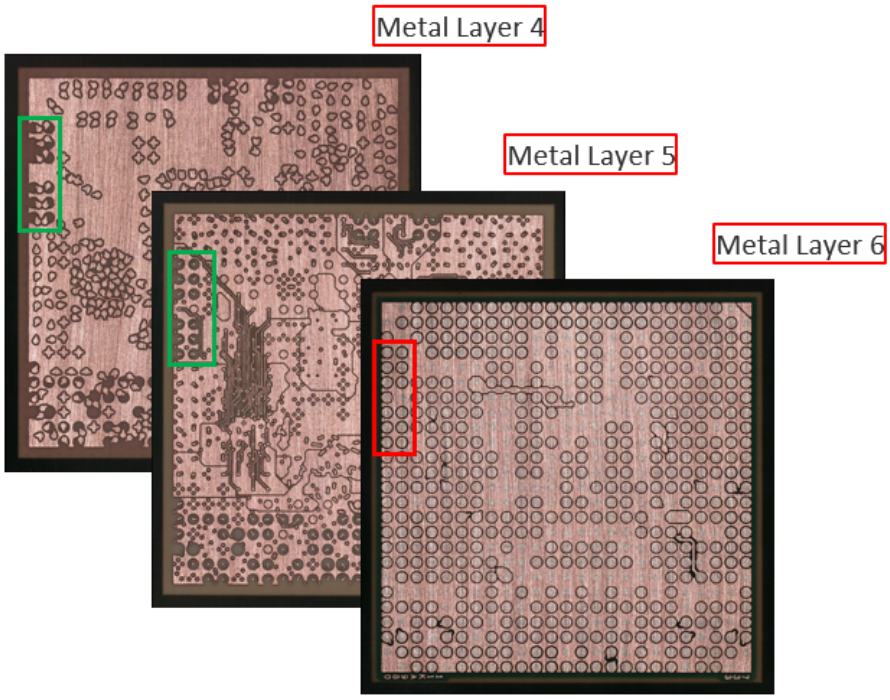
98. The NXP MIMX8MQ6DVA also has a plurality of electrically conductive layers (for example, metal layers 4 and 5) disposed immediately proximate the first layer (metal layer 6).



99. The NXP MIMX8MQ6DVA further has a plurality of dielectric layers (for example, via layers 4 and 5) separating, respectively, the electrically conductive layers (metal layers 4 and 5) and the first layer (metal layer 6) from each other.



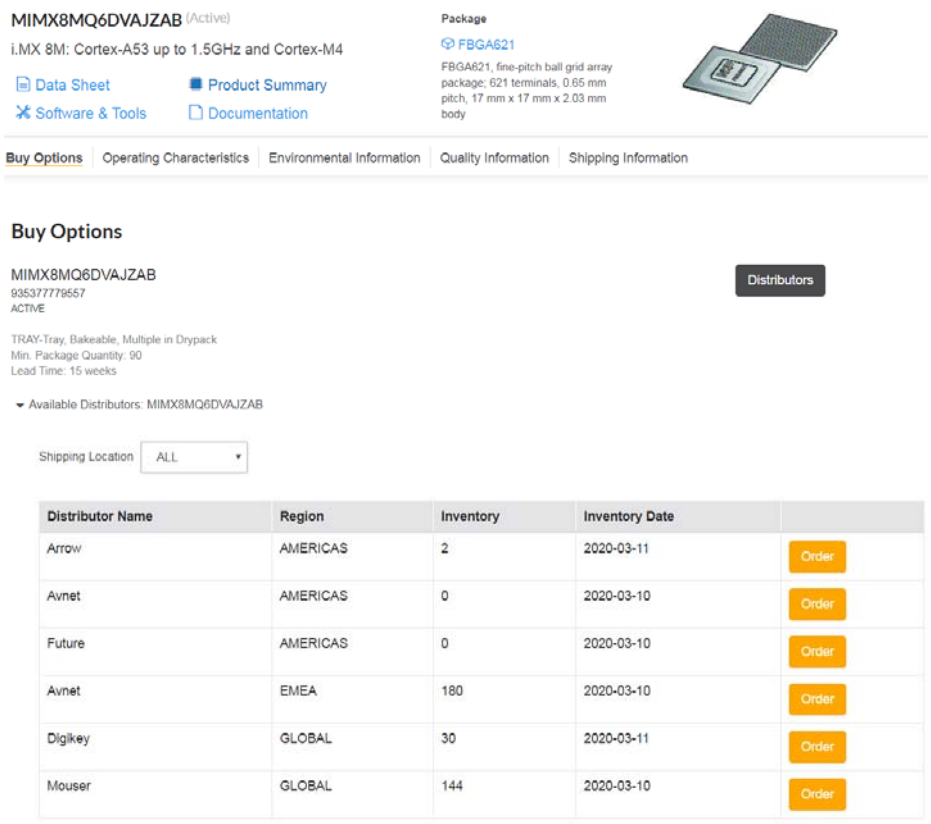
100. The NXP MIMX8MQ6DVA further has a plurality of rows of cutouts (for example, in green below) formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts (for example, in red below) for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers:



101. Claim 12 of the Hall 340 Patent applies to each Hall 340 Accused Product at least because each of those products contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts, like the NXP MIMX8MQ6DVA.

102. On information and belief, each of the Hall 340 Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

103. By way of example only, the NXP MIMX8MQ6DVA has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Global or Americas distributors:



MIMX8MQ6DVAJZAB (Active)

i.MX 8M: Cortex-A53 up to 1.5GHz and Cortex-M4

Data Sheet | Product Summary | Software & Tools | Documentation

Package

FBGA621

FBGA621, fine-pitch ball grid array package; 621 terminals, 0.65 mm pitch, 17 mm x 17 mm x 2.03 mm body

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

MIMX8MQ6DVAJZAB
935377779557
ACTIVE

TRAY-Tray, Bakeable, Multiple in Drypack
Min. Package Quantity: 90
Lead Time: 15 weeks

Distributors

Available Distributors: MIMX8MQ6DVAJZAB

Shipping Location ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	2	2020-03-11	Order
Avnet	AMERICAS	0	2020-03-10	Order
Future	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	180	2020-03-10	Order
Digikey	GLOBAL	30	2020-03-11	Order
Mouser	GLOBAL	144	2020-03-10	Order

See https://www.nxp.com/part/MIMX8MQ6DVAJZAB#/ (last visited March 11, 2020).

104. NXP has known of the Hall 340 Patent and has been on notice of its infringement of the Hall 340 Patent since at least September 12, 2019, when Bell Semic provided a claim chart showing the NXP MIMX8MQ6DVA as infringing and exemplary of NXP's infringement of the Hall 340 Patent. On February 21, 2020, Bell Semic sent a letter to NXP further identifying the MCIMX6QP4AVT1AA, LS1088AXN7Q1A, and MPC8543VJANGD as exemplary of NXP's infringement of the Hall 340 Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products.

105. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 340 Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

106. NXP, knowing its products infringe the Hall 340 Patent and with specific intent for others to infringe the Hall 340 Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Hall 340 Accused Products, as well as products containing the same. NXP knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website. NXP actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Hall 340 Accused Products in the United States. NXP knows, and has known since at least September 12, 2019, that the Hall 340 Accused Products infringe the Hall 340 Patent, and purposefully and knowingly sells and offers to sell the Hall 340 Accused Products to its customers with the knowledge and expectation that the Hall 340 Accused Products and/or products containing the same will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

107. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 340 Accused Products and/or products incorporating the Hall 340 Accused Products in the United States by marketing the Hall 340 Accused Products in the United States; providing information such as detailed datasheets supporting use of the Hall 340 Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Hall 340 Accused Products; providing technical documentation for the Hall 340 Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Hall 340 Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Hall 340 Accused Products, including live training and video.

108. NXP USA has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Hall 340 Accused Products, which constitute a material part of the invention of the Hall 340 Patent, knowing the Hall 340 Accused Products to be especially made or especially adapted for use in infringement of the Hall 340 Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

109. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

110. NXP's infringement of the Hall 340 Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Hall 340 Patent no later than September 12, 2019. As detailed above, on September 12, 2019, Bell Semic provided a claim chart showing the NXP MIMX8MQ6DVA as infringing and exemplary of NXP's infringement of the Hall 340 Patent. On February 21, 2020, Bell Semic sent a letter to NXP further identifying 3 additional NXP products as exemplary of NXP's infringement of the Hall 340 Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products. Despite these efforts, and knowing that it was willfully infringing the Hall 340 Patent, NXP continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Hall 340 Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Hall 340 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 2

Willful Infringement of U.S. Patent No. 8,288,269 (Hall 269 Patent)

111. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

112. The Hall 269 Patent is generally related to methods for avoiding parasitic capacitance in an integrated circuit package, such as an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board. (*See* Hall 269 Patent, Abstract.)

113. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the NXP MIMX8MQ6DVA described below includes 621 pins) while packages decrease in size. In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 269 Patent teaches the formation of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

114. The Hall 269 Patent contains 2 independent claims and 20 total claims, covering various methods. Claim 1 reads:

A method, comprising steps of:

forming a first electrically conductive layer including a plurality of rows of contact pads;

forming an electrically insulating layer on the first electrically conductive layer; and

forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

115. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Hall 269 Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Hall 269 Patent, and/or NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Hall 269 Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Hall 269 Patent (*e.g.*, claims 1, 4, 7, and 10-13). Such products manufactured using these infringing methods include, but are not limited to:

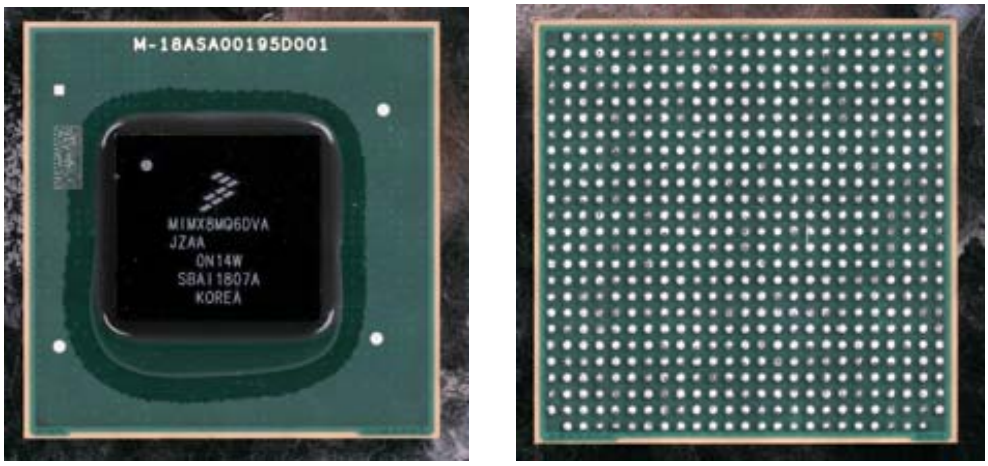
- NXP products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts;
- NXP's MIMX8MQ6DVA, an NXP i.MX 8M Quad processor that includes a quad Arm Cortex-A53 core for use in consumer products;
- NXP's MCIMX6QP4AVT1AA, an NXP i.MX 6 series 32-bit MPU that includes a quad Arm Cortex-A9 core;

- NXP's LS1088AXN7Q1A, an NXP QorIQ Layerscape communications processor;
- NXP's MPC8543VJANGD, an NXP PowerQUICC III processor with high-speed connectivity; and
- NXP's devices that are variants of the above-identified products;

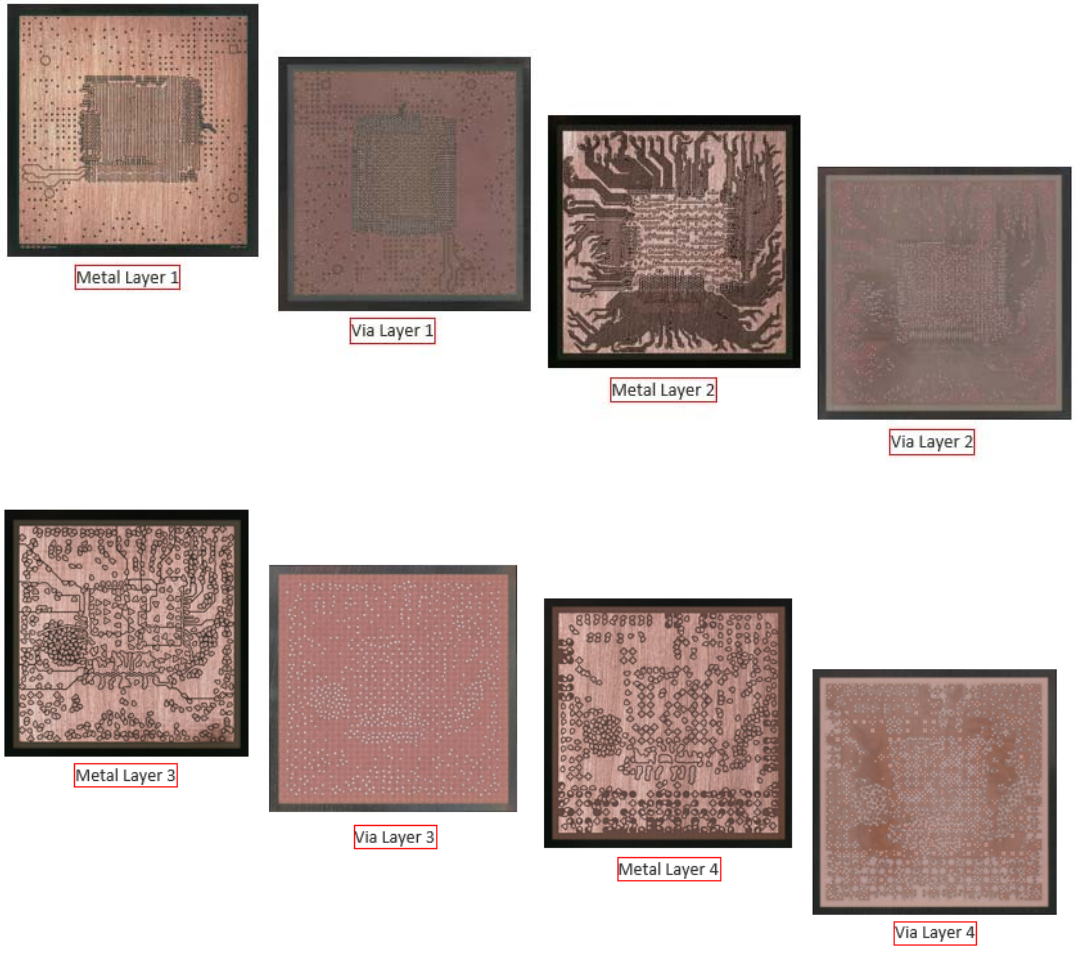
(collectively "Hall 269 Accused Products").

116. By way of example only, the process of manufacturing the NXP MIMX8MQ6DVA meets all the steps of claim 1 of the Hall 269 Patent including: (1) forming a first electrically conductive layer including a plurality of rows of contact pads; (2) forming an electrically insulating layer on the first electrically conductive layer; and (3) forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layers and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

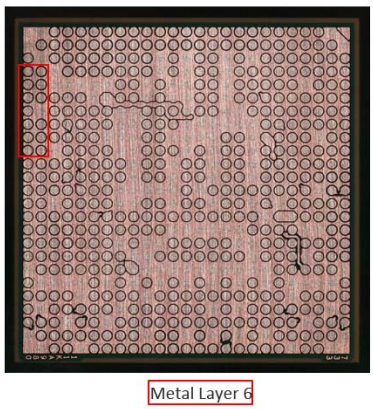
117. As shown below, the NXP MIMX8MQ6DVA is an integrated circuit with an integrated circuit package substrate.



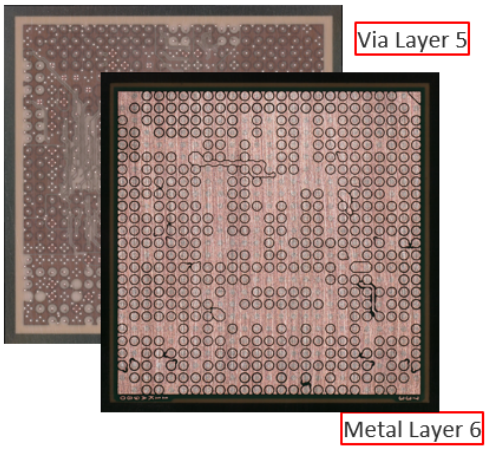
118. The integrated circuit package substrate of the NXP MIMX8MQ6DVA is manufactured to have 6 metal layers and 5 via layers.



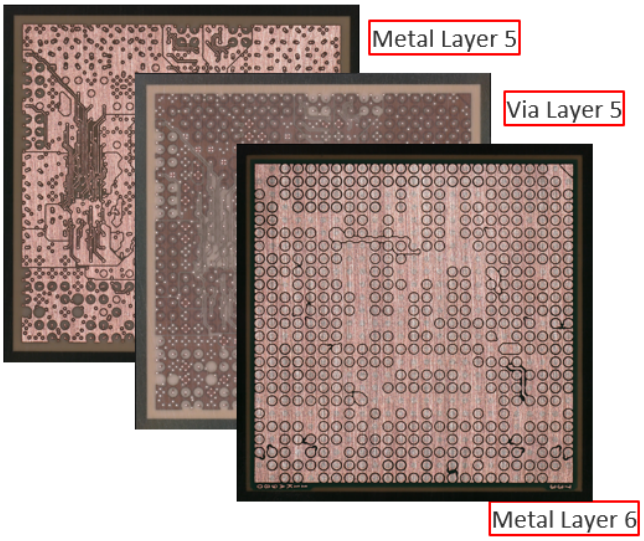
119. During manufacture of the NXP MIMX8MQ6DVA, a first electrically conductive layer (metal layer 6) with a plurality of rows of contact pads (for example, shown in red below) is formed.



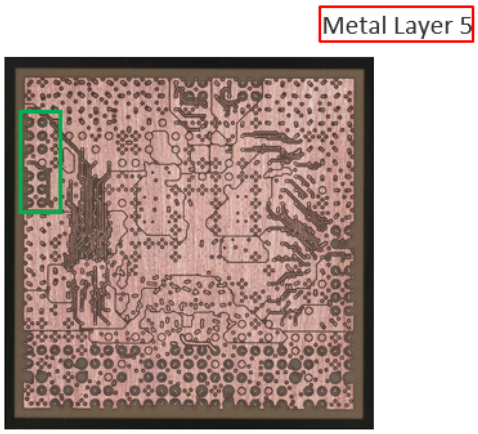
120. During manufacture of the NXP MIMX8MQ6DVA, an electrically insulating layer (via layer 5 below) is formed on the first electrically conductive layer (metal layer 6).



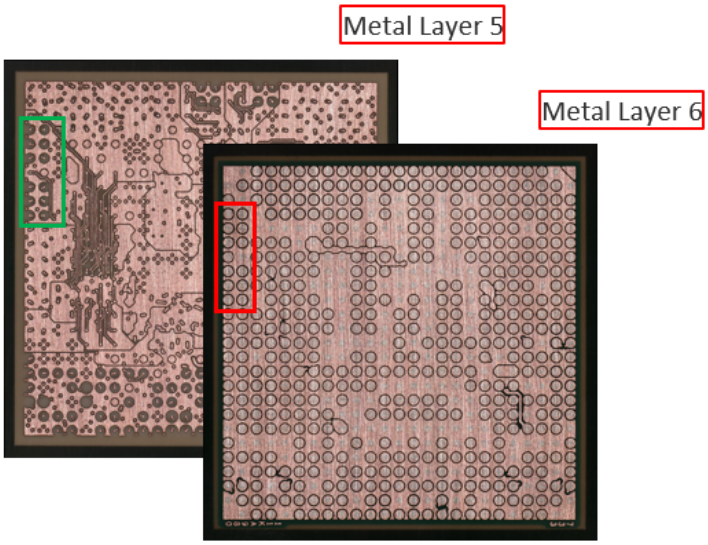
121. During manufacture of the NXP MIMX8MQ6DVA, a second electrically conductive layer (metal layer 5) is formed over the electrically insulating layer (via layer 5), such that there is no intermediate conductive layer between the first and second electrically conductive layers (metal layers 6 and 5):



122. The second electrically conductive layer (metal layer 5) comprises metal and has two or more cutouts (for example, as shown in green on metal layer 5 below), wherein each cutout encloses an electrically insulating area within the second electrically conductive layer.



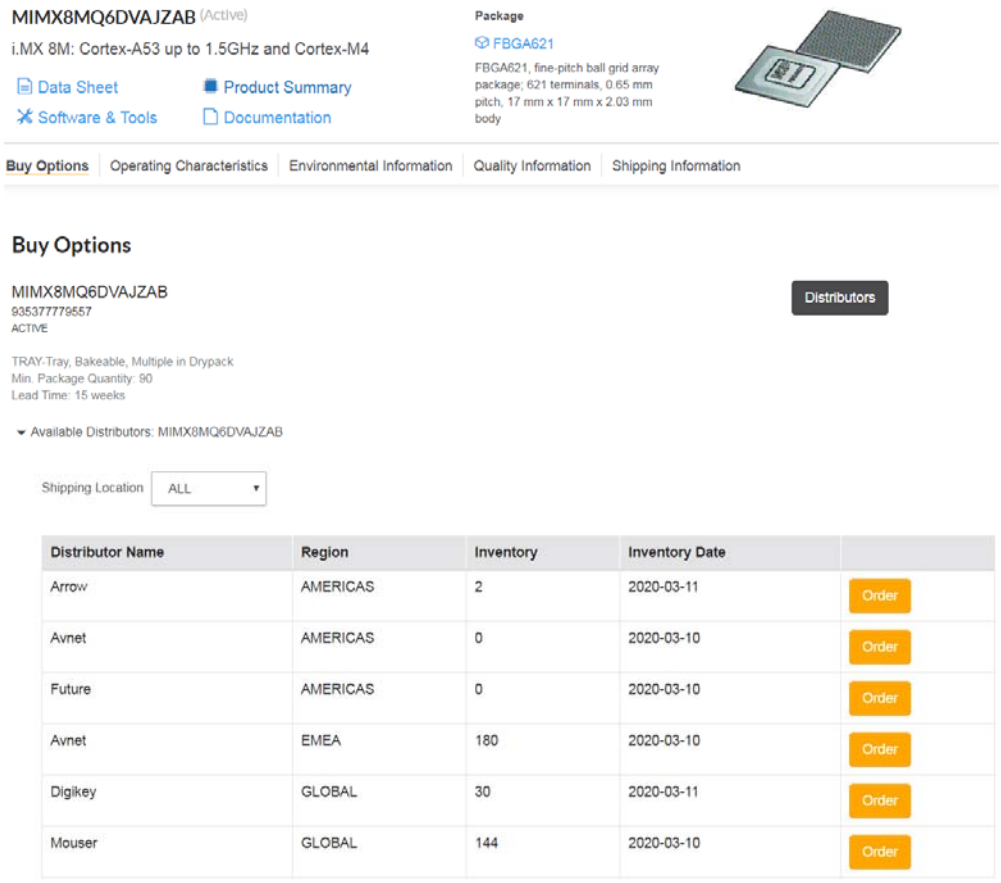
123. Each electrically insulating area (for example, in green) also completely overlaps a corresponding one of the contact pads (in red below) such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.



124. Claim 1 of the Hall 269 Patent applies to each Hall 269 Accused Product at least because each of those products was manufactured to contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts, like the NXP MIMX8MQ6DVA.

125. On information and belief, each of the Hall 269 Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

126. By way of example only, the NXP MIMX8MQ6DVA has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Americas and Global distributors:



MIMX8MQ6DVAJZAB (Active)

i.MX 8M: Cortex-A53 up to 1.5GHz and Cortex-M4

Data Sheet | Product Summary | Software & Tools | Documentation

Package

FBGA621

FBGA621, fine-pitch ball grid array package; 621 terminals, 0.65 mm pitch, 17 mm x 17 mm x 2.03 mm body

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

MIMX8MQ6DVAJZAB
935377779557
ACTIVE

Distributors

TRAY-Tray, Bakeable, Multiple in Drypack
Min. Package Quantity: 90
Lead Time: 15 weeks

Available Distributors: MIMX8MQ6DVAJZAB

Shipping Location ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	2	2020-03-11	Order
Avnet	AMERICAS	0	2020-03-10	Order
Future	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	180	2020-03-10	Order
Digikey	GLOBAL	30	2020-03-11	Order
Mouser	GLOBAL	144	2020-03-10	Order

See https://www.nxp.com/part/MIMX8MQ6DVAJZAB#/ (last visited March 11, 2020).

127. NXP has known of the Hall 269 Patent and has been on notice of its infringement of the Hall 269 Patent since at least February 21, 2020, when Bell Semic sent a letter identifying the NXP MIMX8MQ6DVAJZAA, MCIMX6QP4AVT1AA, LS1088AXN7Q1A, and MPC8543VJANGD as exemplary of NXP's infringement of the Hall 269 Patent. NXP has not responded to this letter.

128. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 269 Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

129. NXP, knowing that the process of manufacturing its Accused Hall 269 Products infringes the Hall 269 Patent and with specific intent for others to infringe the Hall 269 Patent,

has induced infringement of, and continues to induce infringement of, one or more claims of the Hall 269 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Hall 269 Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Hall 269 Accused Products, as well as products incorporating the same.

130. NXP knows, and has known since at least February 21, 2020, that the process of manufacturing the Hall 269 Accused Products infringes the Hall 269 Patent. Despite this knowledge, NXP knowingly and intentionally instructed, and continues to instruct, its OEMs, package assemblers, and foundry suppliers to infringe the Hall 269 Patent through the unlicensed manufacture and assembly of the Hall 269 Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent by its customers', distributors', and/or other third parties' sale and distribution of the Hall 269 Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowing and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent through use, sale, offers for sale, and/or importing in or into the United States of the Hall 269 Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

131. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 269 Accused Products and/or products

incorporating the Hall 269 Accused Products in the United States by marketing the Hall 269 Accused Products in the United States; providing detailed datasheets supporting use of the Hall 269 Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Hall 269 Accused Products; providing technical documentation for the Hall 269 Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Hall 269 Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Hall 269 Accused Products, including live training and video.

132. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement of the Hall 269 Patent, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

133. NXP's infringement of the Hall 269 Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Hall 269 Patent no later than February 21, 2020. As detailed above, on February 21, 2020, Bell Semic sent a letter identifying 4 NXP products as exemplary of NXP's infringement of the Hall 269 Patent. NXP has not responded to this letter. Despite these efforts, and knowing that it was willfully infringing the Hall 269 Patent, NXP continued, and continues, to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Hall 269 Patent, despite

a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Hall 269 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 3

Willful Infringement of U.S. Patent No. 7,566,964 (Kang Patent)

134. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

135. The Kang Patent is generally related to an integrated circuit device structure and process for fabricating the structure wherein a power bus interconnect structure is formed in the aluminum pad or contact layer. An interconnect structure for interconnecting underlying levels of interconnect can also be formed in the aluminum pad layer. (*See* Kang Patent, Abstract.)

136. Power buses are required in interconnect systems within integrated circuits in order to supply power to the various device elements. In prior interconnect systems, power buses were formed as an additional interconnect layer. The formation of this additional interconnect layer increased fabrication cost due to the increased number of mask steps, mask layers, and process steps involved. The additional process steps also lowered device yield as they presented more opportunities for processing defects to occur. Furthermore, because this power bus interconnect layer conducted a relatively high current, it generally had a greater width, thickness, and pitch than the signal interconnect layers, and was also a source of noise and parasitic capacitance that could disrupt the performance of proximate devices and interconnect structures. To overcome this problem, the power bus could be isolated from other device structures, but this

isolation would correspondingly consume more device area. The interconnect system and power bus taught in the Kang Patent solves these problems by teaching the formation of the power bus in the same aluminum-copper alloy layer as the bond pad. In doing so, the same masking, patterning, and etching steps that are used to form the aluminum bond pad layer were also used to form the power bus in the aluminum layer. Thus, an entire metallization layer can be eliminated, including the associated process steps and mask requirements.

137. The Kang Patent contains 1 independent claim and 7 total claims, covering various integrated circuit devices. Claim 1 reads:

> An integrated circuit device comprising:
>
> a metallization interconnect system overlying a semiconductor substrate, the metallization interconnect system including at least a first and a second interconnect feature located within a dielectric layer;
>
> a power bus located over the metallization interconnect system, the power bus comprising an alloy of aluminum and copper, and further wherein the power bus includes a first contact pad region configured for connection external to the integrated circuit device that is in contact with the first interconnect feature, and a second region in contact with the second interconnect feature; and
>
> a passivation layer overlying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.

138. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Kang Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Kang Patent (*e.g.*, claims 1-4 and 6-7), including, but not limited to:

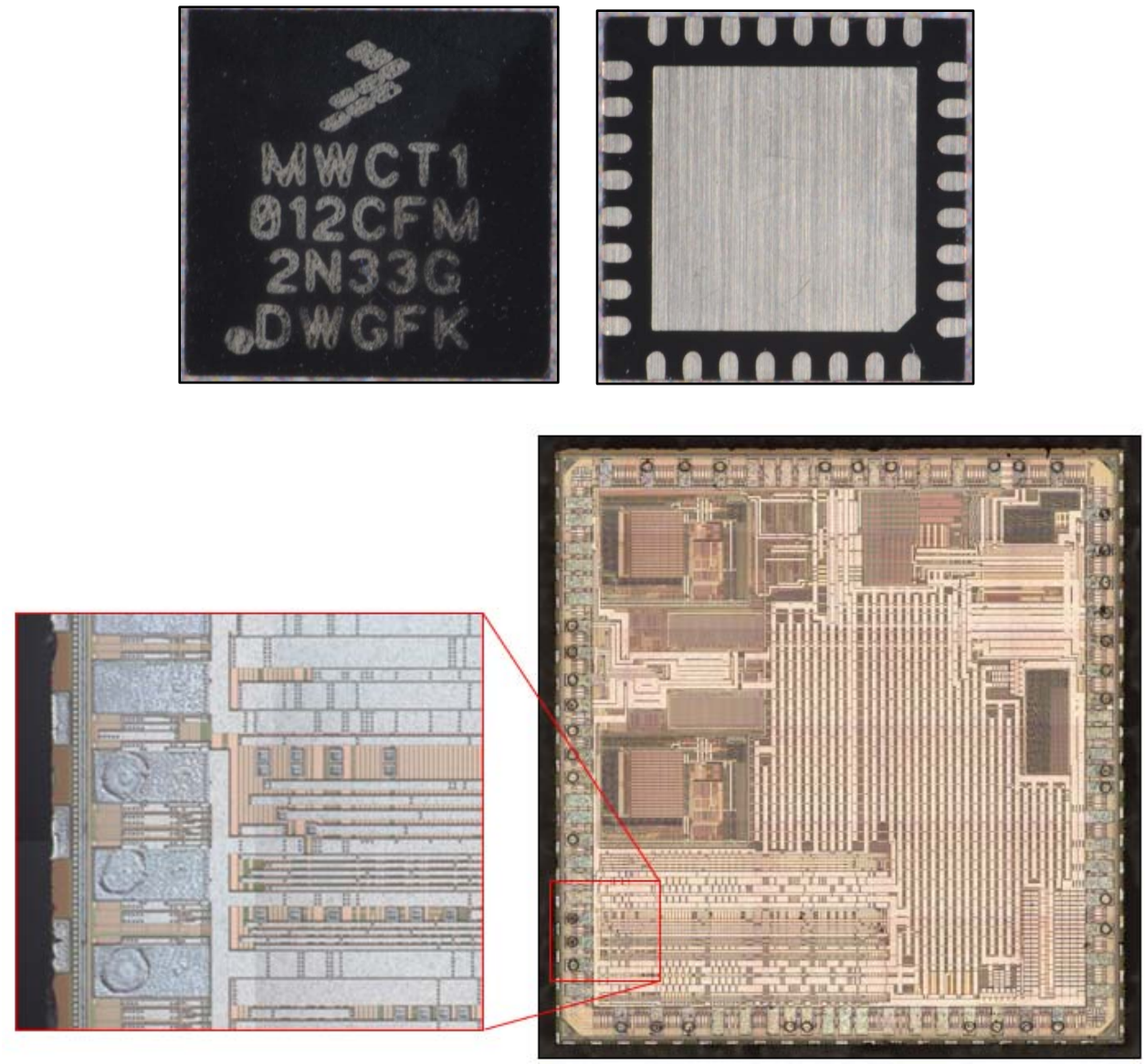
- NXP's copper-based products that have a metallization interconnect system and a top-level aluminum power bus;

- NXP's MWCT1012CFM, a wireless charging transmitter used in handheld consumer applications;
- NXP's MK70FX512VMJ15, an ARM cortex processor used in applications such as industrial control panels, navigational displays, point-of-sale terminals, and medical monitoring equipment;
- NXP's MCIMX281AVM4B, an ARM9 Core automotive processor used in infotainment systems that don't require a display;
- NXP's MKW41Z512VHT4, a wireless radio microcontroller used in Thread and Zigbee wireless/mesh networks; and
- NXP's devices that are variants of the above-identified products;

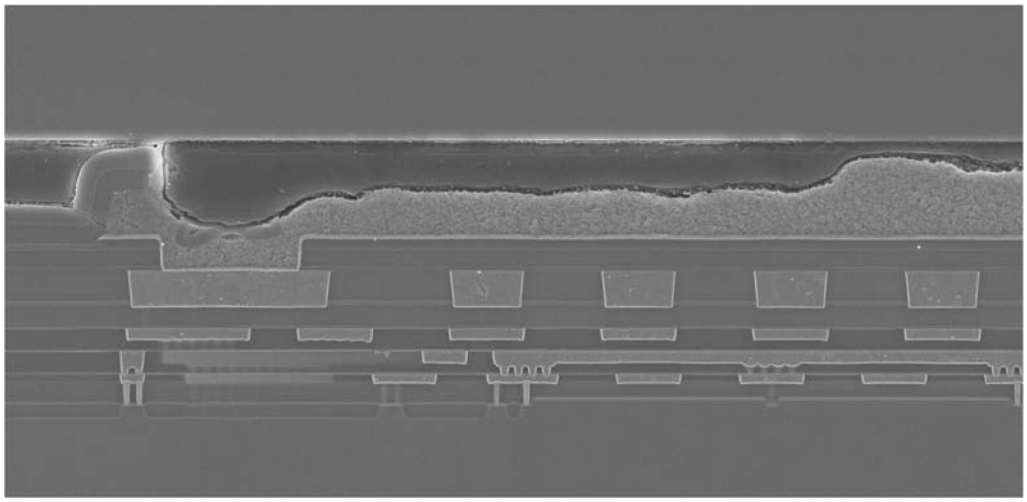
(collectively "Kang Accused Products").

139. By way of non-limiting example only, NXP's MWCT1012CFM infringes claim 1 of the Kang Patent because it is an integrated circuit device that has (1) a metallization interconnect system overlying a semiconductor substrate, the metallization interconnect system including at least a first and a second interconnect feature located within a dielectric layer; (2) a power bus located over the metallization interconnect system, the power bus comprising an alloy of aluminum and copper, and further wherein the power bus includes a first contact pad region configured for connection external to the integrated circuit device that is in contact with the first interconnect feature, and a second region in contact with the second interconnect feature; and (3) a passivation layer overlaying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.

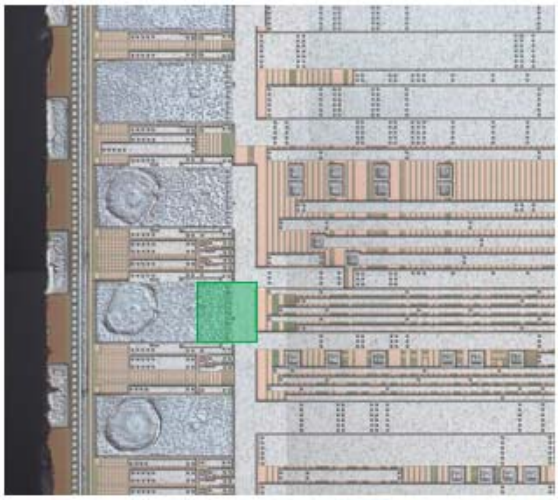
140. As shown below, the NXP MWCT1012CFM is an integrated circuit device.

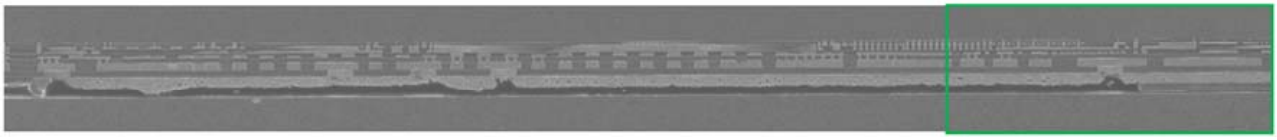


141. The NXP MWCT1012CFM has a metallization interconnect system, comprised of more than one layer of copper connected to an aluminum power bus, overlying a semiconductor substrate.

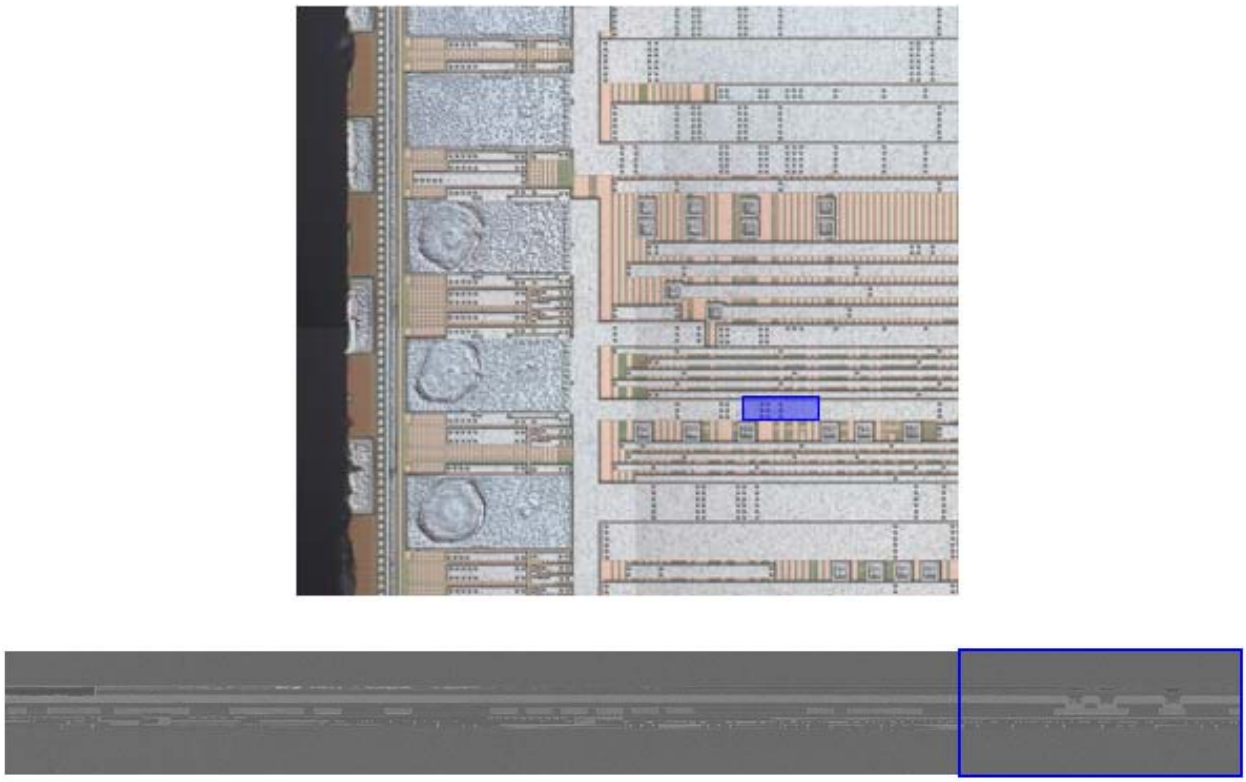


142. The metallization interconnect system in the NXP MWCT1012CFM includes at least a first interconnect feature (*e.g.*, in green below) located within a dielectric layer.

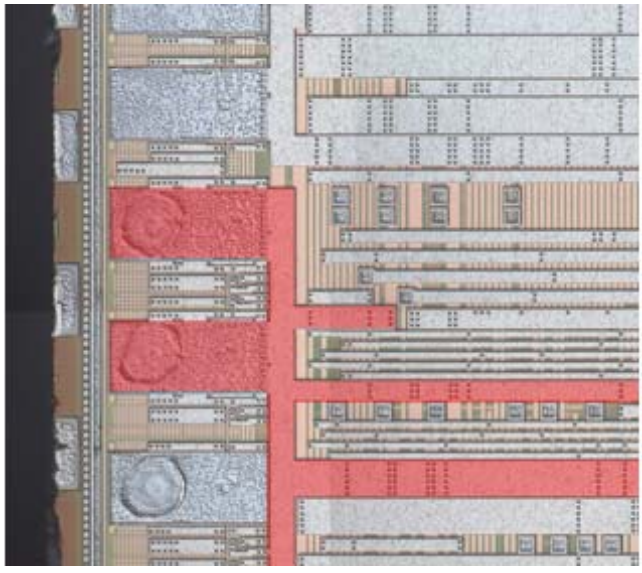




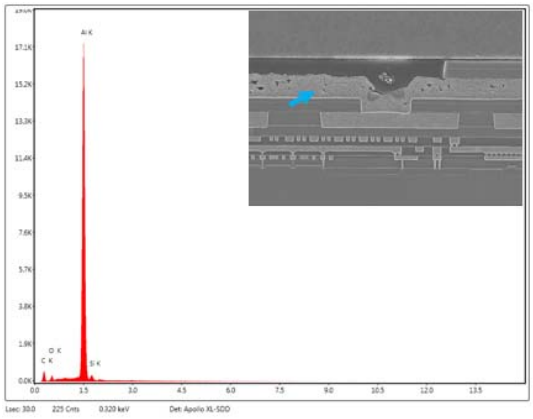
143. The metallization interconnect system in the NXP MWCT1012CFM also includes a second interconnect feature (*e.g.*, in purple below) located within a dielectric layer.

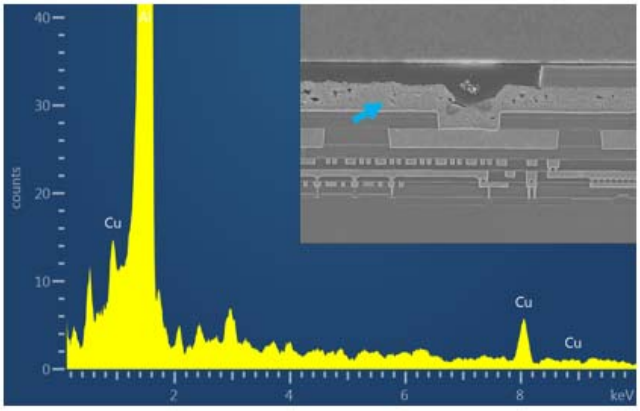


144. The NXP MWCT1012CFM has a power bus (*e.g.*, in red below) located over the metallization interconnect system.

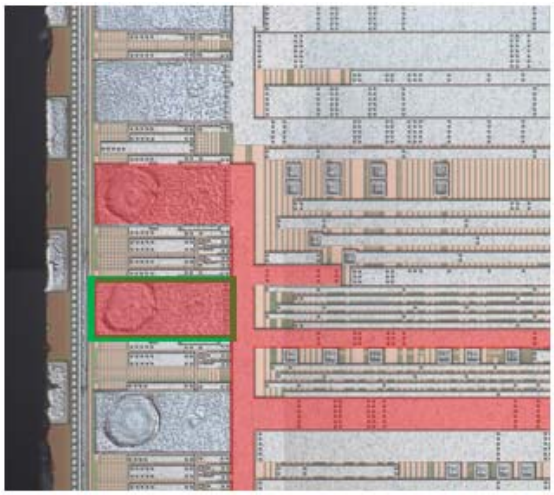


145. The power bus comprises an alloy of aluminum and copper. *See, e.g.*, analysis below evidencing an alloy of aluminum and copper.

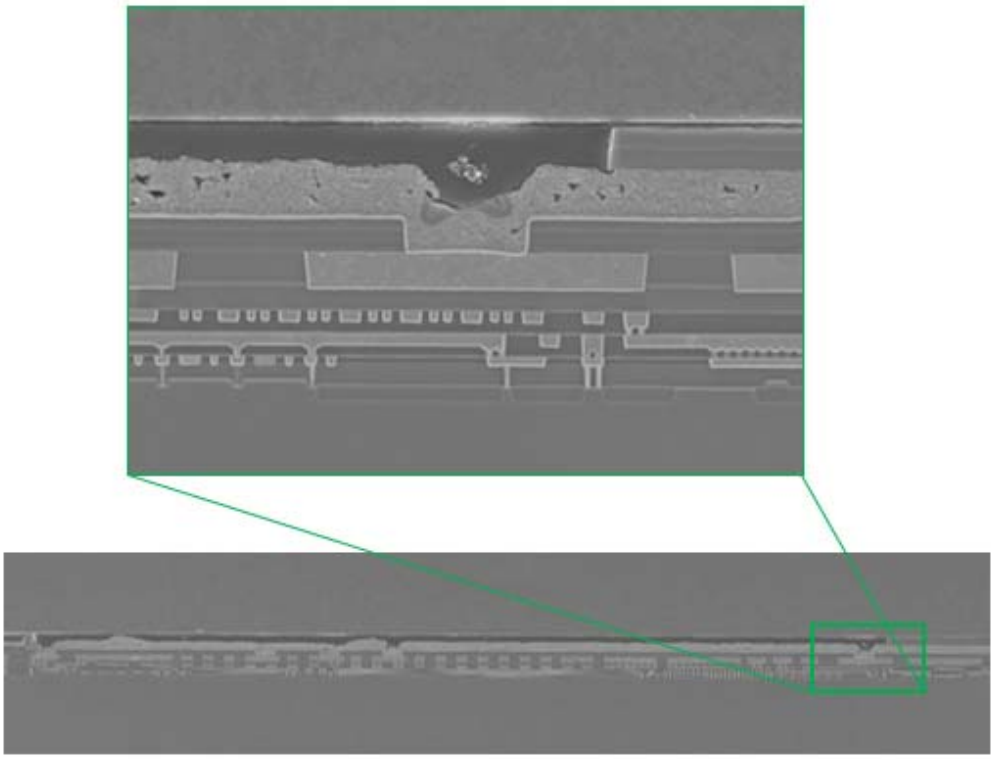




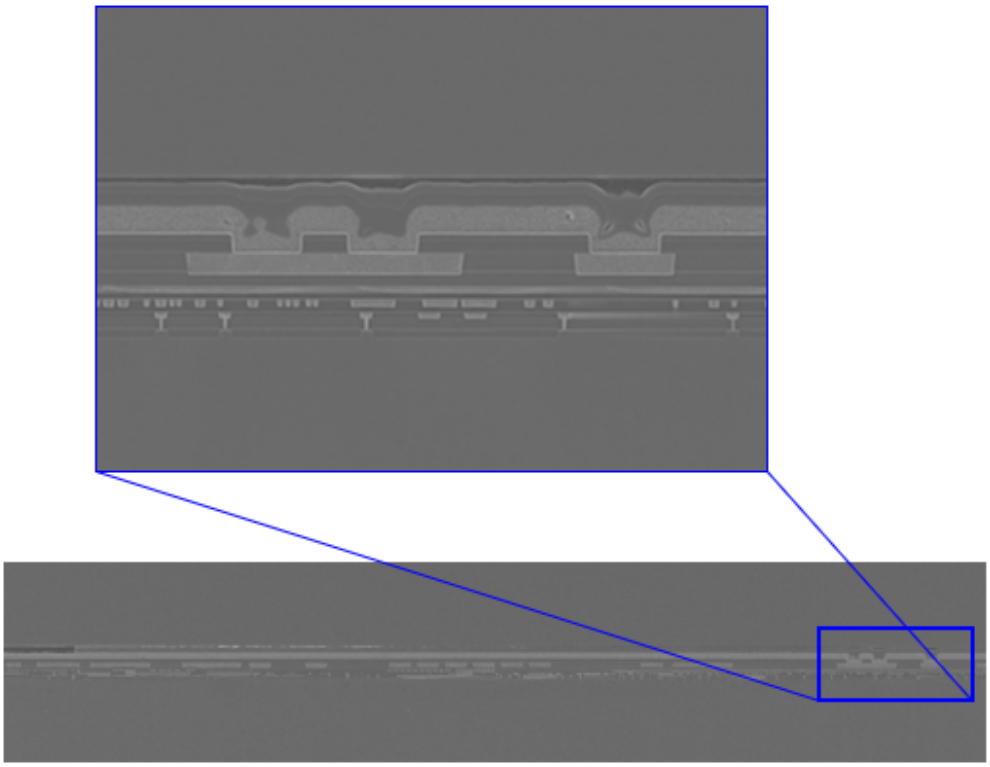
146. The power bus also includes a first contact pad region (*e.g.*, green below) configured for connection external to the integrated circuit device.



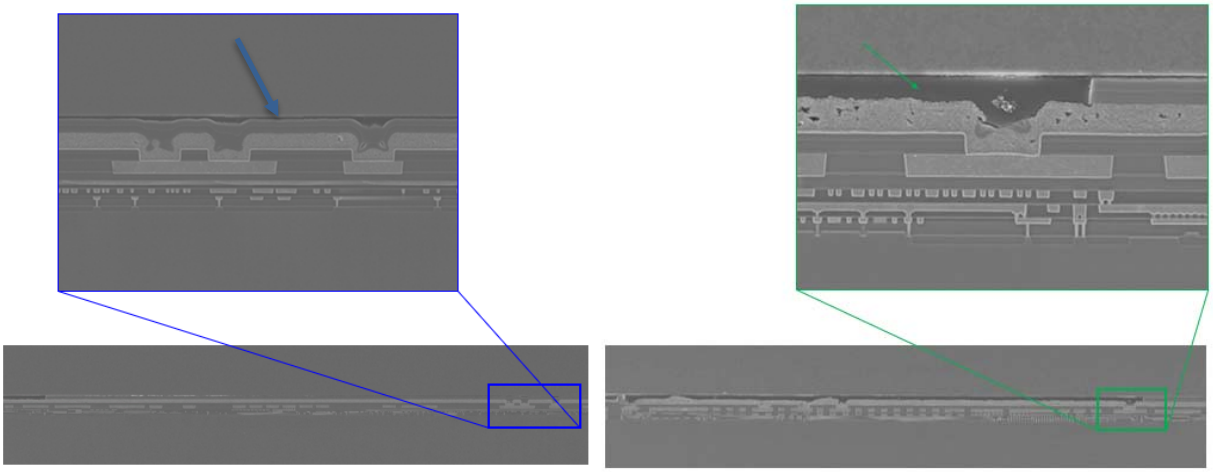
147. The first contact pad region is in contact with the first interconnect feature.



148. The second region is in contact with the second interconnect feature.



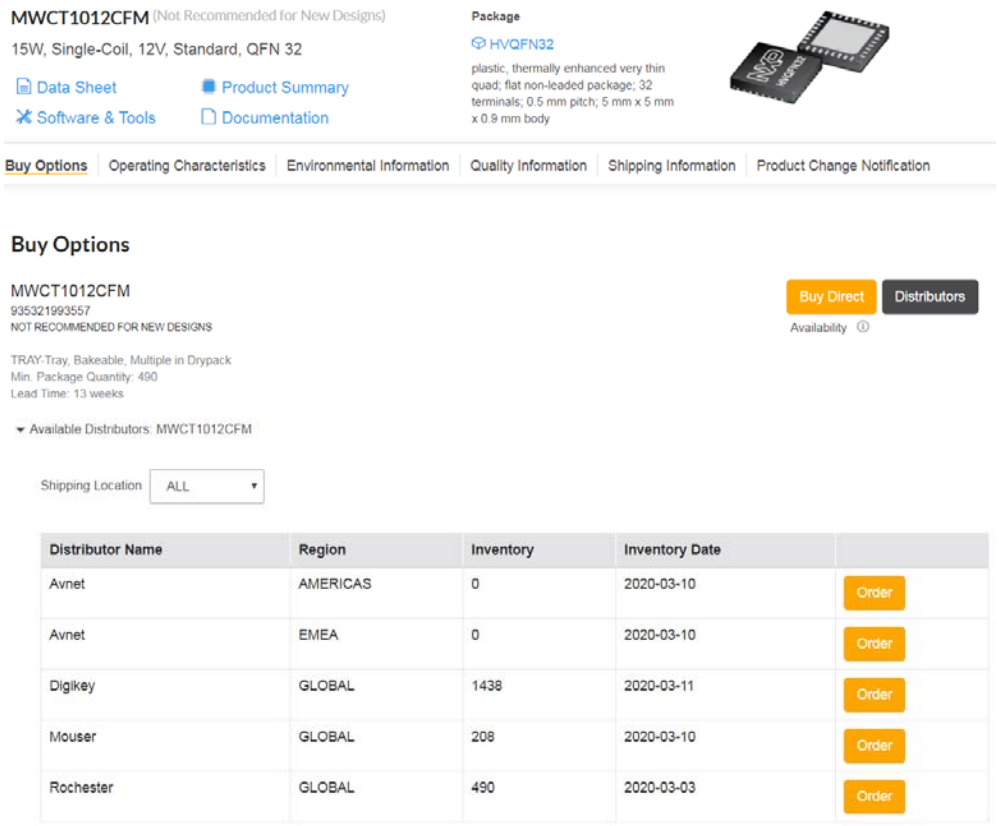
149. The NXP MWCT1012CFM also has a passivation layer overlying at least a portion of the power bus to expose at least a portion of the first contact pad region (*e.g.*, see green arrow pointing to exposed portion of the first contact pad region) and protect the second region (*e.g.*, see blue arrow point to passivation layer over second region).



150. Claim 1 of the Kang Patent applies to each Kang Accused Product at least because each of those products contain the same or similar copper-based metallization interconnect system and a top-level aluminum power bus, like the NXP MWCT1012CFM.

151. On information and belief, each of the Kang Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

152. By way of example only, the NXP MWCT1012CFM has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least four NXP-authorized Americas and Global distributors:



MWCT1012CFM (Not Recommended for New Designs)

15W, Single-Coil, 12V, Standard, QFN 32

Data Sheet | Product Summary | Software & Tools | Documentation

Package

HVQFN32

plastic, thermally enhanced very thin quad; flat non-leaded package; 32 terminals; 0.5 mm pitch; 5 mm x 5 mm x 0.9 mm body

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information | Product Change Notification

Buy Options

MWCT1012CFM
935321993557
NOT RECOMMENDED FOR NEW DESIGNS

TRAY-Tray, Bakeable, Multiple in Drypack
Min. Package Quantity: 490
Lead Time: 13 weeks

Buy Direct | Distributors

Availability

Available Distributors: MWCT1012CFM

Shipping Location: ALL

Distributor Name	Region	Inventory	Inventory Date	
Avnet	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	0	2020-03-10	Order
Digikey	GLOBAL	1438	2020-03-11	Order
Mouser	GLOBAL	208	2020-03-10	Order
Rochester	GLOBAL	490	2020-03-03	Order

See https://www.nxp.com/part/MWCT1012CFM#/ (last visited March 11, 2020).

153. NXP has known of the Kang Patent and has been on notice of its infringement of the Kang Patent since at least September 12, 2019, when Bell Semic provided a claim chart showing the NXP MWCT1012CFM as infringing and exemplary of NXP's infringement of the Kang Patent. On February 21, 2020, Bell Semic sent a letter to NXP further identifying the MK70FX512VMJ15, MCIMX281AVM4B, and MKW41Z512VHT4 as infringing the Kang Patent. NXP has not substantively responded to the identification of these infringing products or the infringement allegations in the claim chart.

154. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Kang Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

155. NXP, knowing its products infringe the Kang Patent and with specific intent for others to infringe the Kang Patent, has induced infringement, and continues to induce infringement, of one or more claims of the Kang Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Kang Accused Products, as well as products containing the same. NXP knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website. NXP actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Kang Accused Products in the United States. NXP knows, and has known since at least September 12,

2019, that the Kang Accused Products infringe the Kang Patent, and purposefully and knowingly sells and offers to sell the Kang Accused Products to its customers with the knowledge and expectation that the Kang Accused Products, and/or products incorporating the same, will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

156. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Kang Accused Products and/or products incorporating the Kang Accused Products in the United States by marketing the Kang Accused Products in the United States; providing information such as detailed datasheets supporting use of the Kang Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Kang Accused Products; providing technical documentation for the Kang Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Kang Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Kang Accused Products, including live training and video.

157. NXP USA has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Kang Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Kang Accused Products, which constitute a material

part of the invention of the Kang Patent, knowing the Kang Accused Products to be especially made or especially adapted for use in infringement of the Kang Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

158. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

159. NXP's infringement of the Kang Patent is and has been knowing, deliberate, and willful NXP learned of its infringement of the Kang Patent no later than September 12, 2019. As detailed above, Bell Semic provided a claim chart showing the NXP MWCT1012CFM as infringing and exemplary of NXP's infringement of the Kang Patent. On February 21, 2020, Bell Semic sent a letter to NXP further identifying the MK70FX512VMJ15, MCIMX281AVM4B, and MKW41Z512VHT4 as infringing the Kant Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products. Despite these efforts, and knowing that it was willfully infringing the Kang Patent, NXP continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Kang Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Kang Patent entitles Bell Semic to increased

damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 4

Willful Infringement of U.S. Patent No. 6,281,129 (Merchant Patent)

160. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

161. The Merchant Patent is generally related to methods of manufacturing a semiconductor device by using a polishing apparatus with a polishing pad conditioning wheel that has a conditioning head, a setting alloy, an abrasive material, and a corrosion resistant coating. The conditioning head has opposing first and second faces with the first face coupleable to the polishing apparatus. The setting alloy is coupled to the conditioning head at the second face, and the abrasive material is embedded in the setting alloy, which is substantially covered by the corrosion resistant coating. (*See* Merchant Patent, Abstract.)

162. Chemical mechanical planarization (CMP) is used in the manufacture of semiconductor devices in order to create dielectric and metal layers that are extremely flat and of a precise thickness needed to pattern the features that comprise a semiconductor device. CMP involves the polishing of a wafer using a polishing pad and a chemical/mechanical polishing slurry. The polishing process results in pad material and slurry residues collecting in pores of the polishing pad, requiring that the polishing pad be conditioned using a conditioning wheel. During conditioning, the conditioning wheel comes into contact with residue of the chemical/mechanical polishing slurry from the polishing pad, which attacks the setting alloy that holds the abrasive materials on the conditioning wheel. As a result, over time, the abrasive materials loosen from the conditioning wheel, reducing the effective surface area of the conditioning wheel and slowing the conditioning process. The Merchant Patent addresses this

problem by teaching the use of a corrosion resistant coating and a hard-facing metal alloy, such as a nickel / chromium / iron alloy, as the setting alloy in the conditioning wheel. Due to the corrosion resistant coating and the use of the hard-facing metal alloy, which is significantly resistive to the corrosive effects of the materials used in chemical/mechanical slurries, the usable lifetime of the conditioning head is improved.

163. The Merchant Patent contains 2 independent claims and 9 total claims, covering various methods. Claim 5 depends from independent claim 1 and reads:

> [A method of manufacturing a semiconductor device, comprising:
>
> polishing a semiconductor wafer with a chemical/mechanical slurry against a polishing pad, the polishing forming variations in a polishing surface of the polishing pad; and
>
> conditioning the polishing surface with a polishing pad conditioning wheel comprising:
>
> a conditioning head having opposing first and second faces, the first face coupleable to a polishing apparatus;
>
> a setting alloy coupled to the conditioning head at the second face;
>
> abrasive material embedded in the setting alloy; and
>
> a corrosion resistant coating affixed to the setting alloy],
>
> wherein conditioning includes conditioning with a polishing pad conditioning wheel wherein the setting alloy comprises a hard facing metal alloy.

164. NXP USA has directly infringed one or more claims of the Merchant Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Merchant Patent, and/or NXP USA has directly infringed one or more claims of the Merchant Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are

made by a process using one or more claims of the Merchant Patent (*e.g.*, claims 5-7). Such products manufactured using these infringing methods include, but are not limited to:

- NXP products manufactured using a chemical-mechanical polishing process to polish metals including tungsten and copper;
- NXP's 80V18: PN80V, a near field communications (NFC) controller used in mobile phone products like the Apple iPhone X;
- NXP's ASL2500SHNY, a two-phase automotive LED boost driver;
- NXP's FXAS21002CQR1, a 3-axis gyroscope for use in game controllers, electronic compass stabilization, and enhanced motion control;
- NXP's FXTH87EH11DT1, a tire pressure sensor with a dual-axis accelerometer architecture;
- NXP's BGU8009, a SiGe:C low-noise amplifier for GNSS receiver and LTE Band 32 down link applications used to jam signals from co-existing cellular transmitters;
- NXP's MK70FX512VMJ15, an ARM cortex processor used in applications such as industrial control panels, navigational displays, point-of-sale terminals, and medical monitoring equipment;
- NXP's LPC11U35FET48, an ARM Cortex-M0 based, 32-bit microcontroller (MCU);
- NXP's PN5180A0HN/C3E, an NFC Forum-compliant frontend IC for various contactless communication methods and protocols;
- NXP's TDF8530TH/N2, an I2C-bus controller quad channel power amplifier;
- NXP's TDA18250AHN, a silicon tuner used in set top boxes (STBs);
- NXP's MWCT1012CFM, a wireless charging transmitter used in handheld consumer applications;

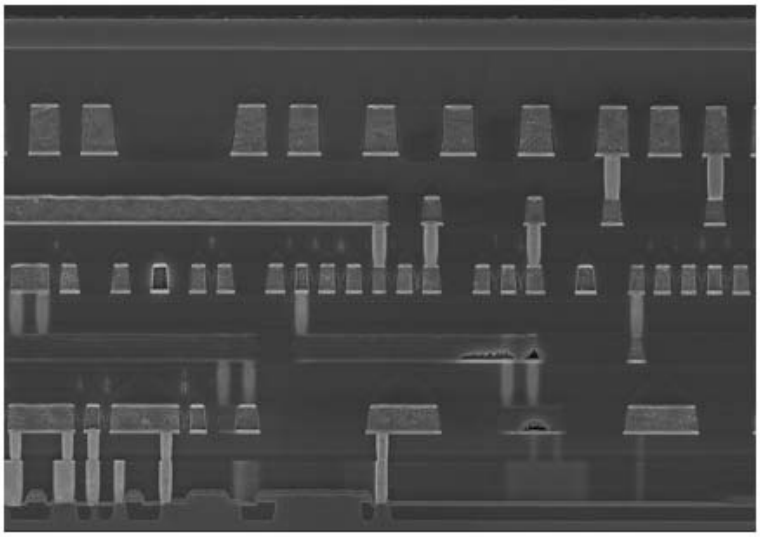
- NXP's MCIMX281AVM4B, an ARM9 Core automotive processor used in infotainment systems that don't require a display;
- NXP's NxH2280C1, a near field magnetic induction radio used in wireless audio and data streaming; and
- NXP's devices that are variants of the above-identified products;

(collectively "Merchant Accused Products").

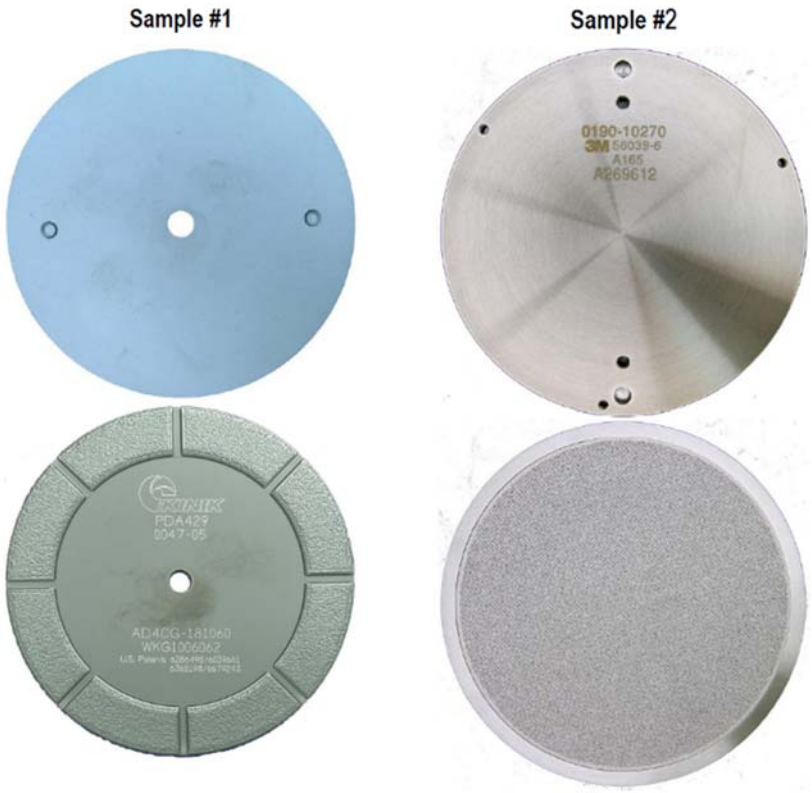
165. By way of non-limiting example only, the process of manufacturing the NXP 80V18:PN80V meets all the steps of claim 5 of the Merchant Patent including the steps of (1) polishing a semiconductor wafer with a chemical/mechanical slurry against a polishing pad, the polishing forming variations in a polishing surface of the polishing pad; and (2) conditioning the polishing surface with a polishing pad conditioning wheel that has (i) a conditioning head with opposing first and second faces, where the first face is coupleable to a polishing apparatus; (ii) a setting alloy coupled to the conditioning head at the second face; (iii) abrasive material embedded in the setting alloy; and (iv) a corrosion resistant coating affixed to the setting alloy, and the setting alloy comprises a hard-facing metal alloy.

166. As shown below, the NXP 80V18:PN80V is a semiconductor device.

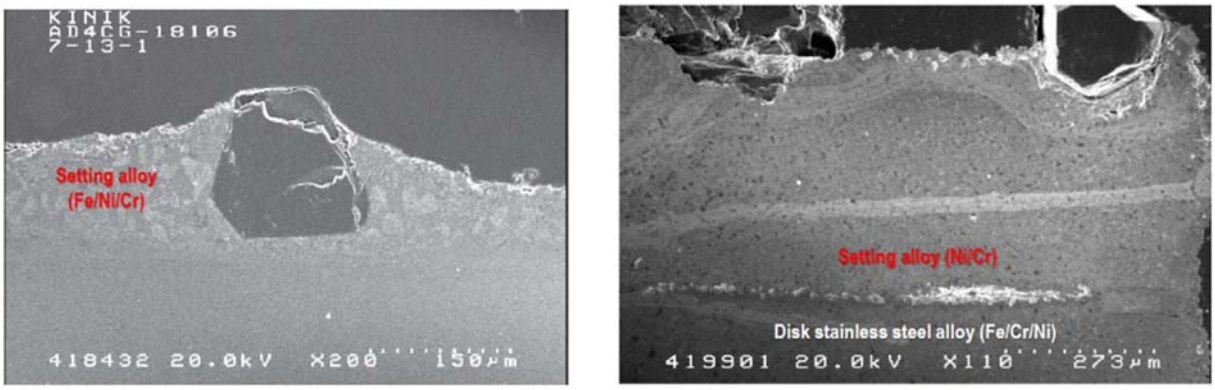
167. On information and belief, the NXP 80V18:PN80V is manufactured using a chemical mechanical planarization step to create an extremely flat and precise thickness that is necessary to manufacture a functioning device. The chemical mechanical planarization process includes the polishing of a semiconductor wafer with a chemical/mechanical slurry against a polishing pad. The polishing process inherently causes the polishing pad to become clogged with pad material and slurry residue, making it necessary to condition the polishing pad to restore its full functionality.



168. On information and belief, this polishing included the use of an industry standard polishing pad conditioning wheel, such as the two sample conditioning wheels below. The top picture of each sample shows a first face that can be coupled to a polishing apparatus.

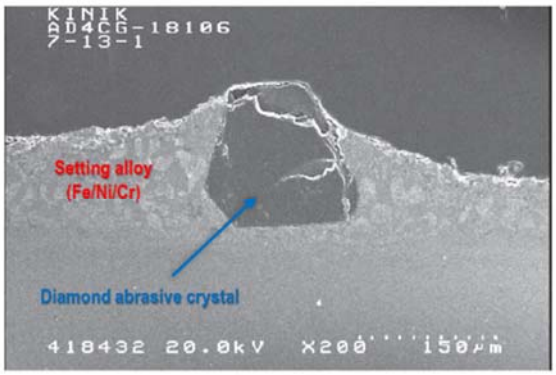


169. These sample conditioning wheels each have a setting alloy coupled to the conditioning head at the second face.

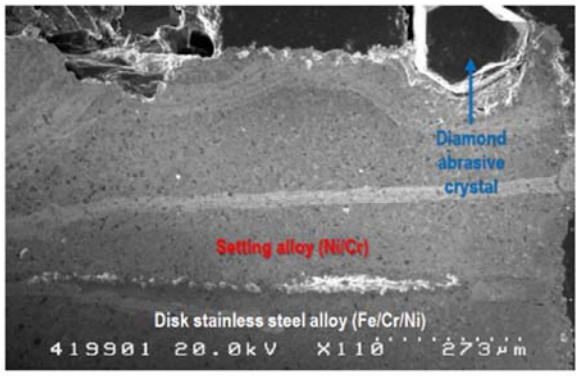


Sample #1 Sample #2

170. These sample conditioning wheels further have abrasive material embedded in the setting alloy.

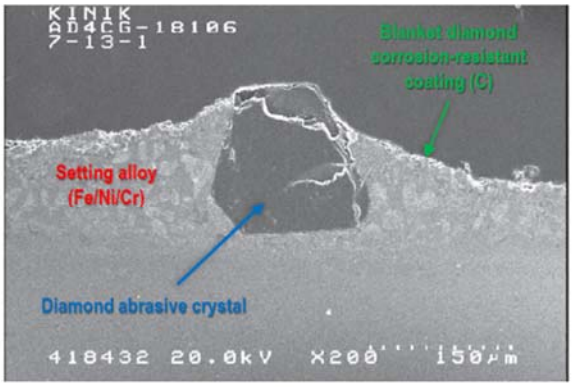


Sample #1

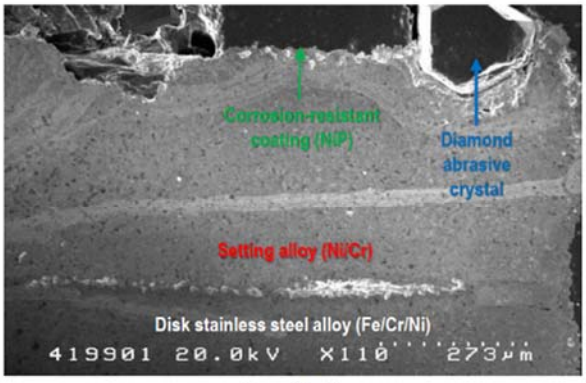


Sample #2

171. These sample conditioning wheels further have a corrosion resistant coating affixed to the setting alloy.

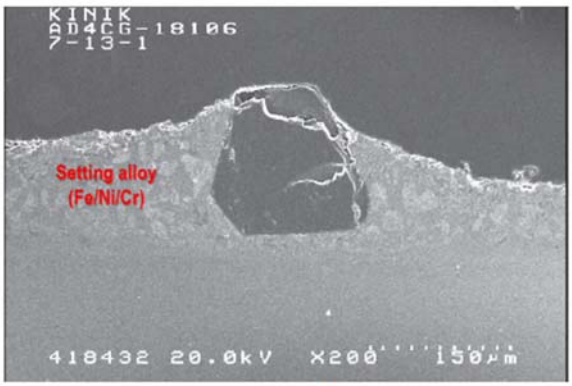


Sample #1

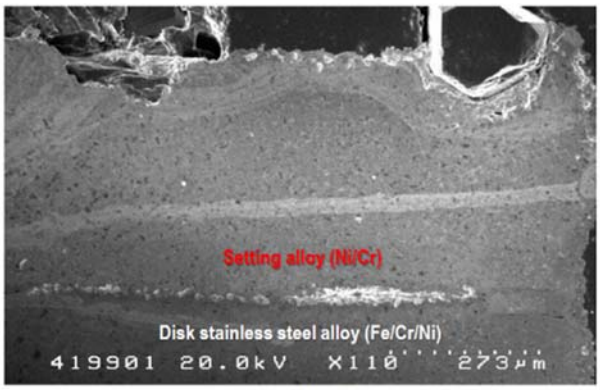


Sample #2

172. The setting alloy used in these sample conditioning wheels is a hard facing metal alloy, *i.e.,* iron nickel chromium and nickel chromium alloys, respectively.



Sample #1

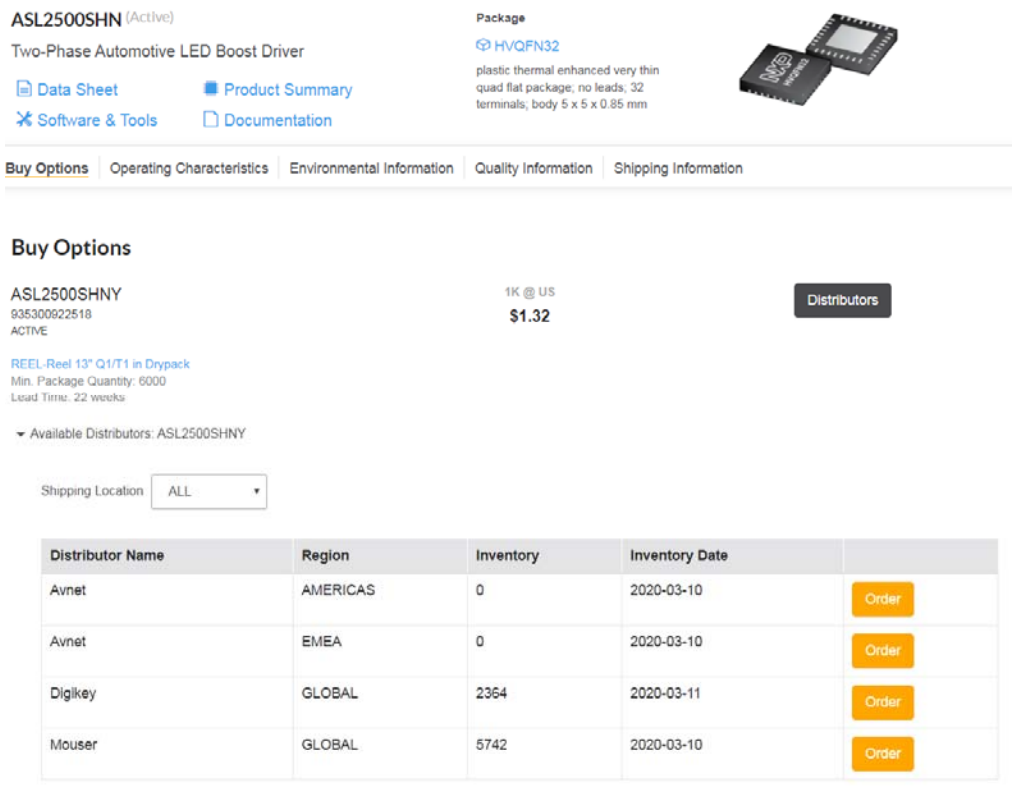


Sample #2

173. Claim 5 of the Merchant Patent applies to each Merchant Accused Product at least because each of those products are manufactured using the same or similar CMP process to polish metals including tungsten and copper as the NXP 80V18:PN80V.

174. On information and belief, each of the Merchant Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

175. By way of example only, the NXP ASL2500SHN has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least three NXP-authorized Americas and Global distributors:



ASL2500SHN (Active)

Two-Phase Automotive LED Boost Driver

Data Sheet | Product Summary | Software & Tools | Documentation

Package

HVQFN32

plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

ASL2500SHNY
935300922518
ACTIVE

1K @ US
$1.32

Distributors

REEL-Reel 13" Q1/T1 in Drypack
Min. Package Quantity: 6000
Lead Time: 22 weeks

Available Distributors: ASL2500SHNY

Shipping Location ALL

Distributor Name	Region	Inventory	Inventory Date	
Avnet	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	0	2020-03-10	Order
Digikey	GLOBAL	2364	2020-03-11	Order
Mouser	GLOBAL	5742	2020-03-10	Order

See https://www.nxp.com/part/ASL2500SHN#/ (last visited March 11, 2020).

176. NXP has known of the Merchant Patent and has been on notice of its infringement of the Merchant Patent since at least January 9, 2019, when Bell Semic first identified the BGU8009, FXTH87EH11DT1, FXAS21002CQR1, 80V18: PN80V, ASL2500SHNY, MK70FX512VMJ15, and LPC11U35FET48 as exemplary of NXP's infringement of the Merchant Patent. On September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Merchant Patent to these same products, as well as the TDA18250AHN/C, PN5180A0HN/C3E, TDF8530TH/N2, MWCT1012CFM, MCIMX281AVM4B, and NxH2280C1. On February 21, 2020, Bell Semic further identified the MKW41Z512VHT4, MCIMX7S5EVM08SC, PCIMX7D7DVM10SA, PCIMX7U5DVP08SC, MIMXRT1061DVL6A, MIMX8MM6DVTLZAA, and LPC11U37FBD48/401 as exemplary of NXP's infringement of the Merchant Patent. NXP has not substantively responded in any way to

the infringement allegations in this claim chart or Bell Semic's further identification of infringing products.

177. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Merchant Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

178. NXP, knowing that the process of manufacturing its Accused Merchant Products infringed the Merchant Patent and with specific intent for others to infringe the Merchant Patent, induced infringement of one or more claims of the Merchant Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least (1) by actively inducing others to make in the United States without authorization the Merchant Accused Products; and/or (2) by actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Merchant Accused Products, and products incorporating the same.

179. NXP has known since at least January 9, 2019 that the process of manufacturing the Merchant Accused Products infringed the Merchant Patent. Despite this knowledge, NXP knowingly and intentionally instructed its OEMs and foundry suppliers to infringe the Merchant Patent through the unlicensed manufacture of the Merchant Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Merchant Patent by its customers', distributors', and/or other third parties' sale and distribution of the Merchant Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Merchant Patent through the use, sale, offers

for sale and/or importing in or into the United States of the Merchant Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

180. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Merchant Accused Products and/or products incorporating the Merchant Accused Products in the United States by marketing the Merchant Accused Products in the United States; providing information such as detailed datasheets supporting use of the Merchant Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Merchant Accused Products; providing technical documentation for the Merchant Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Merchant Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Merchant Accused Products, including live training and video.

181. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

182. NXP's infringement of the Merchant Patent was knowing, deliberate, and willful. NXP learned of its infringement of the Merchant Patent no later than January 9, 2019. As detailed above, Bell Semic first identified 7 products as exemplary of NXP's infringement of the Merchant Patent. As detailed above, on September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Merchant Patent to these same products, as well as an additional 6 products. On February 21, 2020, Bell Semic further identified 7 NXP products as exemplary of NXP's infringement of the Merchant Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's identification of infringing products. Despite these efforts, and knowing that it was willfully infringing the Merchant Patent, NXP continued to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Merchant Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct was egregious. NXP's knowing, deliberate, and willful infringement of the Merchant Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 5

Willful Infringement of U.S. Patent No. 6,596,639 (Easter Patent)

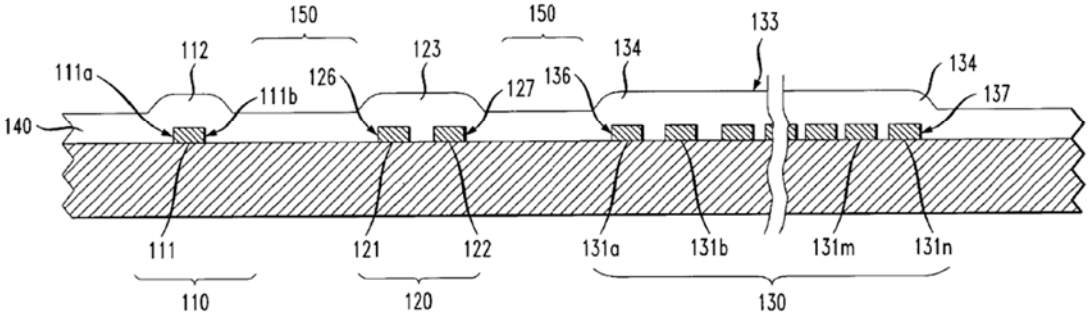
183. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

184. The Easter Patent is generally related to methods for planarizing a semiconductor surface, such as manufacturing a semiconductor device by forming a dielectric layer over a first

level having an irregular topography, depositing a sacrificial material over the dielectric layer, and then planarizing the semiconductor wafer surface. (*See* Easter Patent, Abstract.)

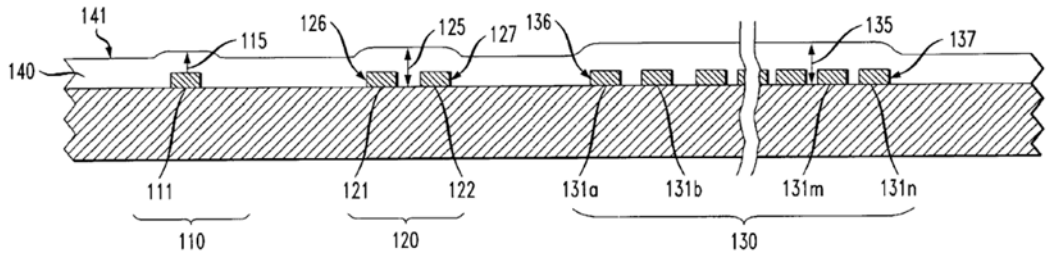
185. Chemical mechanical planarization (CMP) is used in the manufacture of semiconductor devices in order to create dielectric and metal layers that are extremely flat and of a precise thickness needed to pattern the features that comprise a semiconductor device. During planarization, CMP removes the high portions on the wafer surface. However, as a result of the deposition of interlayer dielectric (ILD) layers upon features, dielectric "mushrooms" form over the features, such as 112, 123, and 134 below.

FIG. 1A
PRIOR ART



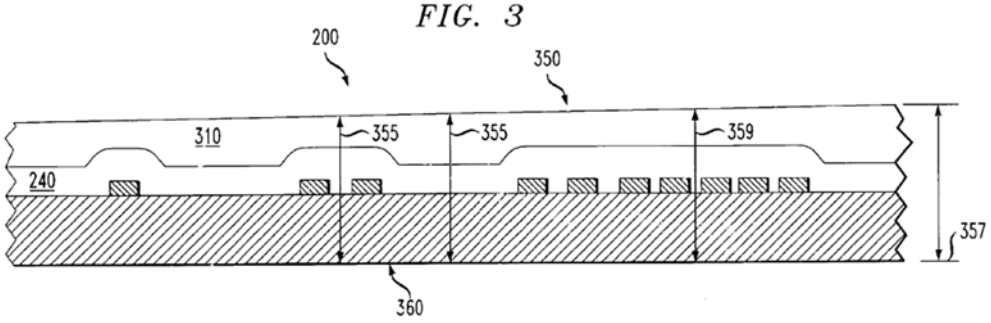
After CMP of such ILD layers, the height of the dielectric layer varies, and thus, the dielectric surface is not planar.

FIG. 1B
PRIOR ART



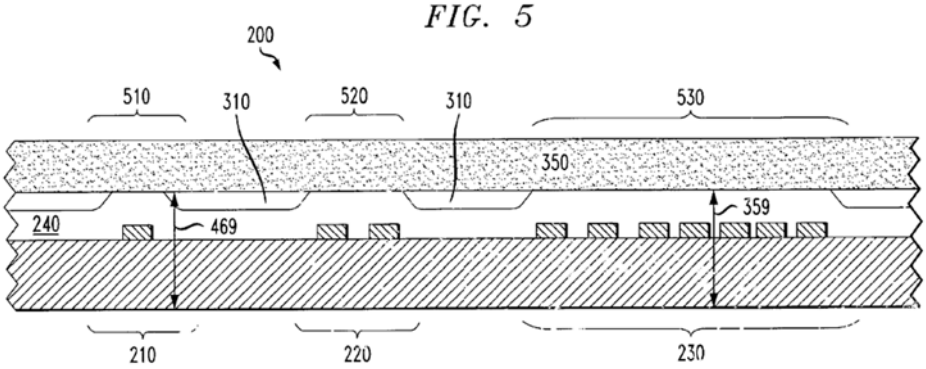
The Easter Patent solves this problem by teaching the deposition of a sacrificial layer, *e.g.,* 310 in the figure below, that fills in the areas between the "mushrooms" over the features.

FIG. 3



Thus, when CMP is performed after the sacrificial layer is deposited, the surface of the ILD layer is substantially planar.

FIG. 5



186. The Easter Patent contains 2 independent claims and 14 total claims, covering various methods. Claim 1 reads:

> A method for planarizing a semiconductor wafer surface, comprising:
>
> forming a dielectric layer over a first level having an irregular topography, said dielectric layer substantially conforming to said irregular topography;
>
> depositing a sacrificial material over said dielectric layer, said sacrificial material forming a substantially planar surface and having a chemical/mechanical planarization (CMP) process removal rate substantially equal to a CMP process removal rate of said dielectric layer, wherein said CMP process removal rates of said sacrificial material and said dielectric layer provide a substantially uniform CMP process removal rate across a semiconductor wafer surface; and then
>
> planarizing said semiconductor wafer surface to a planar surface by removing said sacrificial material and a portion of said dielectric layer with a CMP process.

187. NXP has directly infringed one or more claims of the Easter Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Easter Patent and/or NXP has directly infringed one or more claims of the Easter Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Easter Patent (*e.g.*, claims 1, 2, 8, and 9). Such products manufactured using these infringing methods include, but are not limited to:

- NXP products manufactured using a CMP process to planarize a wafer surface by removing the sacrificial material and a portion of the dielectric layer;
- NXP's PN5180A0HN/C3E, an NFC Forum-compliant frontend IC for various contactless communication methods and protocols;
- NXP's TDF8530TH/N2, an I2C-bus controller quad channel power amplifier;
- NXP's ASL2500SHNY, a two-phase automotive LED boost driver;
- NXP's FXAS21002CQR1, a 3-axis gyroscope for use in game controllers, electronic compass stabilization, and enhanced motion control;
- NXP's LPC11U35FET48, an ARM Cortex-M0 based, 32-bit microcontroller (MCU); and
- NXP's devices that are variants of the above-identified products;

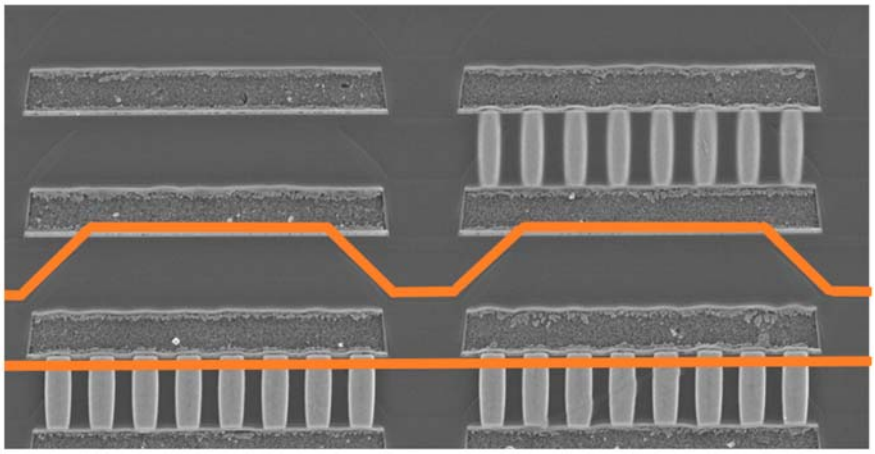
(collectively "Easter Accused Products").

188. By way of non-limiting example only, the process of manufacturing the NXP PN5180A0HN/C3E meets all the steps of claim 1 of the Easter Patent including planarizing a semiconductor wafer surface including the steps of (1) forming a dielectric layer over a first level

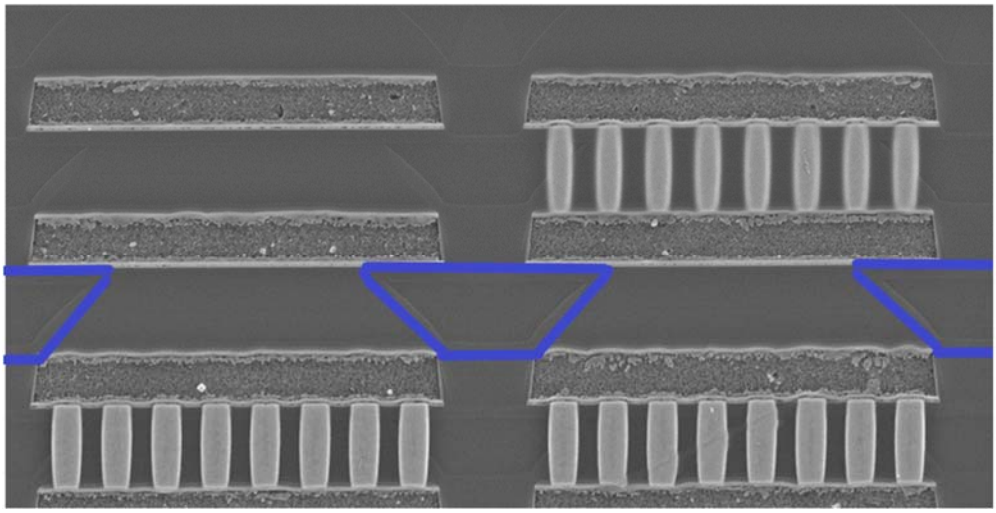
having an irregular topography, the dielectric layer substantially conforming to the irregular topography; (2) depositing a sacrificial material over the dielectric layer, the sacrificial material forming a substantially planar surface and having a chemical/mechanical planarization (CMP) process removal rate substantially equal to a CMP process removal rate of the dielectric layer, wherein the CMP process removals rates of the sacrificial material and the dielectric layer provide a substantially uniform CMP process removal rate across a semiconductor wafer surface; and then (3) planarizing the semiconductor wafer surface to a planar surface by removing the sacrificial material and a portion of the dielectric layer with a CMP process.

189. As shown below, the NXP PN5180A0HN/C3E is a semiconductor device.

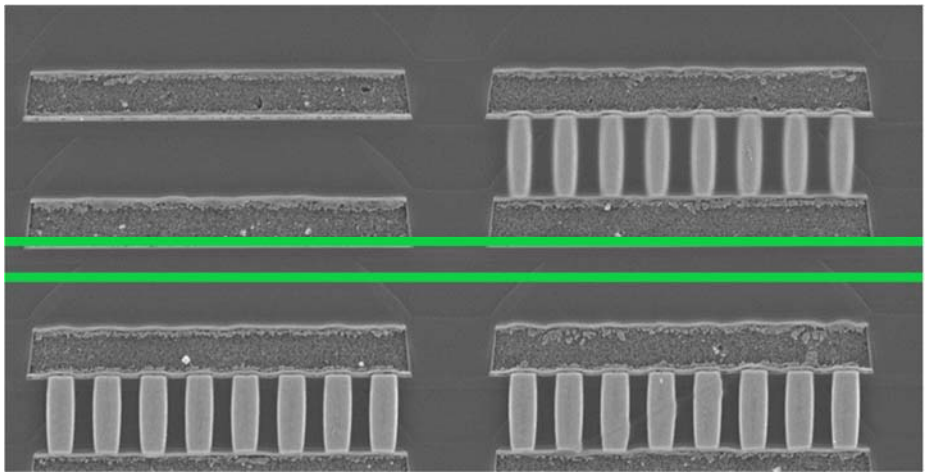
190. During the manufacture of the NXP PN5180A0HN/C3E, a semiconductor wafer surface was planarized. This process includes the step of forming a dielectric layer over a first level having an irregular topography, where the dielectric layer substantially conformed to the irregular topography. As shown in the picture below, a dielectric layer is over a level that has an irregular topography due to the features placed at that level. As can be seen above the features, this dielectric layer substantially conforms to this irregular topography.



191. This planarization process also included the step of depositing a sacrificial material (as shown in the blue box below) over the dielectric layer. The sacrificial material forming a substantially planar surface and having a CMP process removal rate substantially equal to a CMP process removal rate of the dielectric layer, wherein the CMP process removal rates of the sacrificial material and the dielectric layer provide a substantially uniform CMP process removal rate across a semiconductor wafer surface. As can be seen below, a sacrificial layer was then deposited over the first dielectric layer so that, on information and belief, it formed a substantially planar surface (which was then subjected to CMP pursuant to the next step).



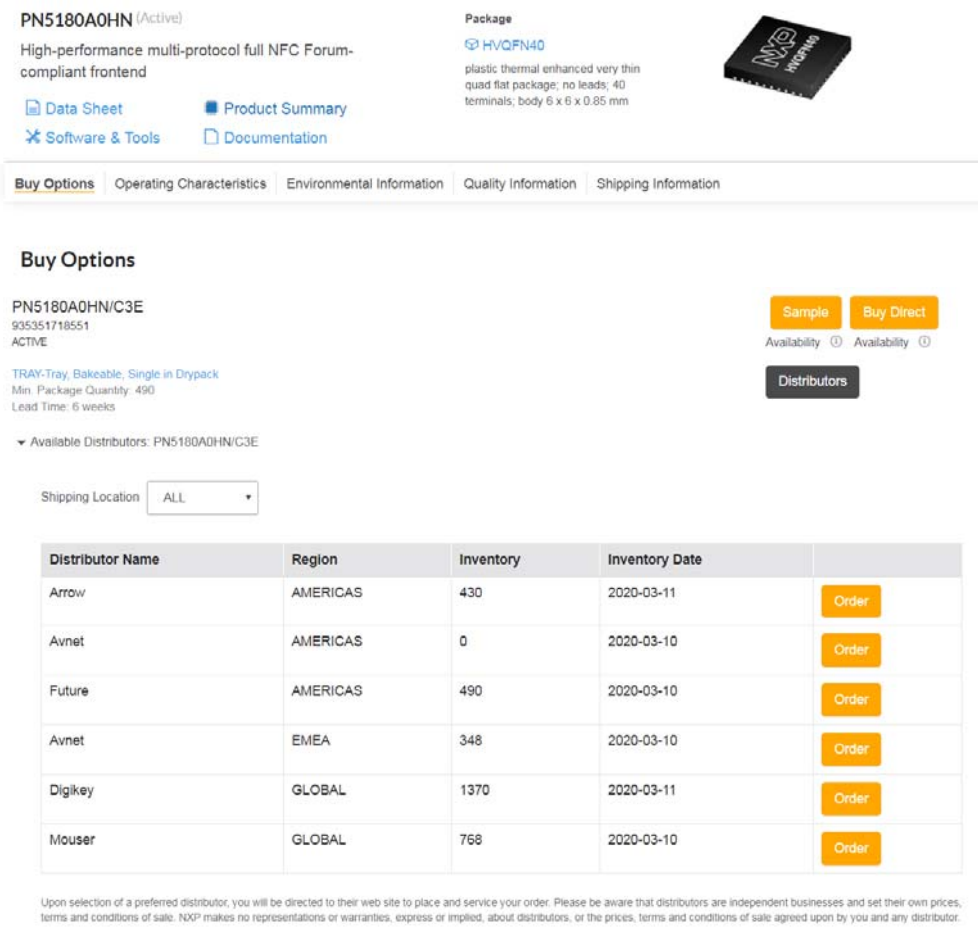
192. After the step of depositing a sacrificial material over the dielectric layer, the planarization process included the step of planarizing the semiconductor wafer surface to a planar surface by removing the sacrificial material and a portion of the dielectric layer with a CMP process. As can be seen in green below, a CMP process was used to planarize the wafer surface by removing the sacrificial material and a portion of the dielectric layer.



193. Claim 1 of the Easter Patent applies to each Easter Accused Product at least because each of those products were manufactured using the same or similar CMP process to planarize a wafer surface by removing the sacrificial material and a portion of the dielectric layer as the NXP PN5180A0HN/C3E.

194. On information and belief, each of the Easter Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

195. By way of example only, the NXP PN5180A0HN/C3E has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Americas and Global distributors:



PN5180A0HN (Active)

High-performance multi-protocol full NFC Forum-compliant frontend

Data Sheet | Product Summary | Software & Tools | Documentation

Package

HVQFN40

plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

PN5180A0HN/C3E
935351718551
ACTIVE

TRAY-Tray, Bakeable, Single in Drypack
Min. Package Quantity: 490
Lead Time: 6 weeks

Sample | Buy Direct
Availability | Availability
Distributors

Available Distributors: PN5180A0HN/C3E

Shipping Location: ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	430	2020-03-11	Order
Avnet	AMERICAS	0	2020-03-10	Order
Future	AMERICAS	490	2020-03-10	Order
Avnet	EMEA	348	2020-03-10	Order
Digikey	GLOBAL	1370	2020-03-11	Order
Mouser	GLOBAL	768	2020-03-10	Order

Upon selection of a preferred distributor, you will be directed to their web site to place and service your order. Please be aware that distributors are independent businesses and set their own prices, terms and conditions of sale. NXP makes no representations or warranties, express or implied, about distributors, or the prices, terms and conditions of sale agreed upon by you and any distributor.

See https://www.nxp.com/part/PN5180A0HN#/ (last visited March 11, 2020).

196. NXP has known of the Easter Patent and has been on notice of its infringement of the Easter Patent since at least January 9, 2019, when Bell Semic first identified the FXAS21002CQR1, PN5180A0HN/C3E, TDF8530TH/N2, ASL2500SHNY, and LPC11U35FET48 as exemplary of NXP's infringement of the Easter Patent. On September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Easter Patent to these same products. On February 21, 2020, Bell Semic further identified the 80V18: PN80V as exemplary of NXP's infringement of the Easter Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products.

197. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Easter Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

198. NXP, knowing that the process of manufacturing its Accused Easter Products infringed the Easter Patent and with specific intent for others to infringe the Easter Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Easter Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Easter Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Easter Accused Products, as well as products incorporating the same.

199. NXP has known since at least January 9, 2019 that the process of manufacturing the Easter Accused Products infringed the Easter Patent. Despite this knowledge, NXP knowingly and intentionally instructed its OEMs and foundry suppliers to infringe the Easter Patent through the unlicensed manufacture of the Easter Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Easter Patent by its customers', distributors', and/or other third parties' sale and distribution of the Easter Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Easter Patent through the use, sale, offer for sale, and/or importing the Easter

Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

200. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Easter Accused Products and/or products incorporating the Easter Accused Products in the United States by marketing the Easter Accused Products in the United States; providing information such as detailed datasheets supporting use of the Easter Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Easter Accused Products; providing technical documentation for the Easter Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Easter Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Easter Accused Products, including live training and video.

201. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

202. NXP's infringement of the Easter Patent was knowing, deliberate, and willful. NXP learned of its infringement of the Easter Patent no later than January 9, 2019. As detailed

above, on January 9, 2019, Bell Semic identified 4 NXP products as exemplary of NXP's infringement of the Easter Patent. As detailed above, on September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Easter Patent to these same products. On February 21, 2020, Bell Semic further identified an additional NXP product as exemplary of NXP's infringement of the Easter Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products. Despite these efforts, and knowing that it was willfully infringing the Easter Patent, NXP continued to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Easter Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct was egregious. NXP's knowing, deliberate, and willful infringement of the Easter Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 6

Willful Infringement of U.S. Patent No. 6,153,543 (Chesire Patent)

203. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

204. The Chesire Patent is generally related to a method of forming a passivation layer over features located on a top layer of a semiconductor device. The method involves depositing a first void-free dielectric layer over the top layer using high density plasma chemical vapor deposition, and depositing a second void-free dielectric layer over the first void-free layer. (*See* Chesire Patent, Abstract.)

205. During the manufacture of semiconductor devices, dielectric and metal layers are added onto a wafer until a final layer of metal is added, *i.e.*, the "top metal layer". Typically, a passivation layer is placed over the top metal layer to maintain the mechanical integrity of the semiconductor device, prevent mobile ion diffusion, and provide some radiation protection for the semiconductor device. Prior art methods of applying passivation layers were capable of filling gaps between adjacent features when the distance between the features was large, however, as the size of features and gaps became smaller, unfilled gaps were left in the passivation layer which became voids in the passivation layer. These voids can cause reliability problems due to entrapment of gases or liquids in the voids. These voids can also act as stress raisers, which can result in inferior mechanical strength of the passivation layer and allow metal interconnections to stress relieve into the voids. The inferior mechanical strength caused by these voids can also be a problem when the chip is removed from the wafer and pressed into the die assembly or other chip carrier. This pressing of the chip transmits a significant force to the passivation level of the chip. A common result of such a transmission of force is damage to the runners in the top metal layer. This damage can be even more prevalent when the runners have high aspect ratios such that the height dimension is significantly greater than the width dimension. Features having this type of aspect ratio are more susceptible to a force applied in the vertical or transverse direction, which occurs when the chip is pressed. One method of compensating for the voids has been to provide a very thick passivation level, however, a thick passivation level, besides being more costly, does not solve the problems associated with the voids. The Chesire Patent solved these problems by using high density plasma chemical vapor deposition to deposit a first void-free layer of a first dielectric over the top layer at a first deposition/sputtering-rate ratio, and then depositing a second void-free layer of a second-layer of

a second dielectric over the first void-free layer at a deposition/sputtering-rate ratio greater than the first.

206. The Chesire Patent contains 1 independent claim and 9 total claims, covering various methods. Claim 5 reads:

> [A method of forming a passivation layer over features located on a top layer of a semiconductor device, comprising the steps of:
>
> depositing a first void-free layer of a first dielectric over said top layer using high density plasma chemical vapor deposition at a first D/S ratio, and
>
> depositing a second void-free layer of a second dielectric over said first void-free layer at a second D/S ratio, wherein said second D/S ratio is greater than said first D/S ratio],
>
> wherein said first layer is applied with a thickness of at least 40% of the height of said features.

207. NXP USA has directly infringed one or more claims of the Chesire Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Chesire Patent and/or NXP USA has directly infringed one or more claims of the Chesire Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Chesire Patent (*e.g.*, claims 5-8). Such products manufactured using these infringing methods include, but are not limited to:

- NXP products with two or more void-free layers of passivation located on the top layer of a semiconductor device with the final metal layer being aluminum;
- NXP's ASL2500SHNY, a two-phase automotive LED boost driver;
- NXP's FXTH87EH11DT1, a tire pressure sensor with a dual-axis accelerometer architecture;

- NXP's FXAS21002CQR1, a 3-axis gyroscope for use in game controllers, electronic compass stabilization, and enhanced motion control;
- NXP's LPC11U35FET48, an ARM Cortex-M0 based, 32-bit microcontroller (MCU); and
- NXP's devices that are variants of the above-identified products;

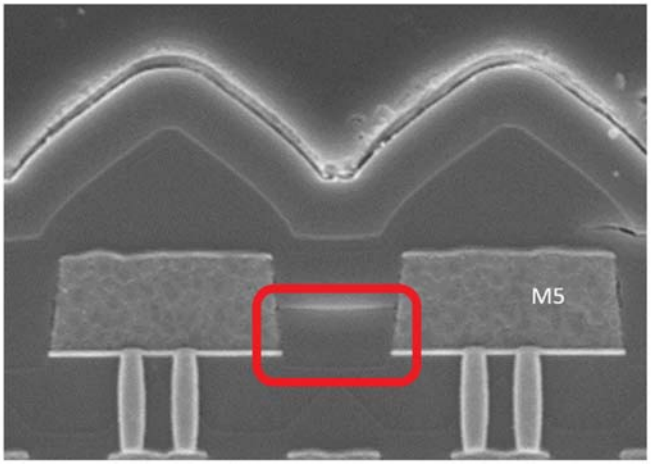
(collectively "Chesire Accused Products").

208. By way of non-limiting example only, the process of manufacturing the NXP ASL2500SHNY meets all the steps of claim 5 of the Chesire Patent including forming a passivation layer over features located on a top layer of a semiconductor device, including the steps of (1) depositing a first void-free layer of a first dielectric over the top layer using high density plasma chemical vapor deposition at a first D/S ratio; (2) depositing a second void-free layer of a second dielectric over the first void-free layer at a second D/S ratio, where the second D/S ratio is greater than the first D/S ratio and where the first layer is applied with a thickness of at least 40% of the height of the features.

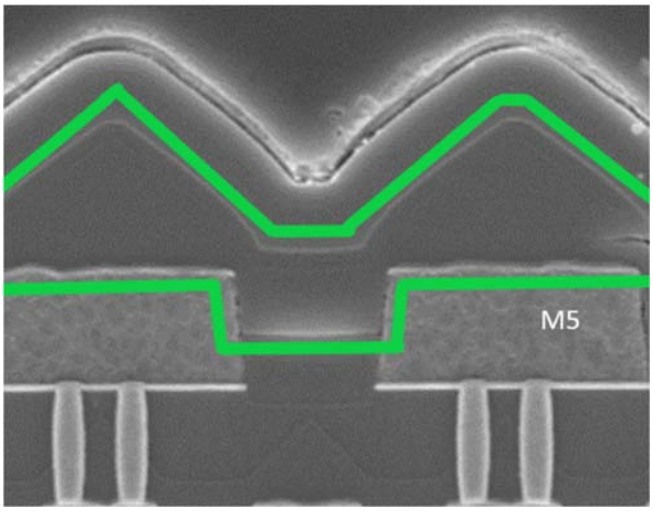
209. As shown below, the NXP ASL2500SHNY is a semiconductor device.

210. During the manufacture of the NXP ASL2500SHNY, a passivation layer was formed over features located on a top layer of a semiconductor device including the step of

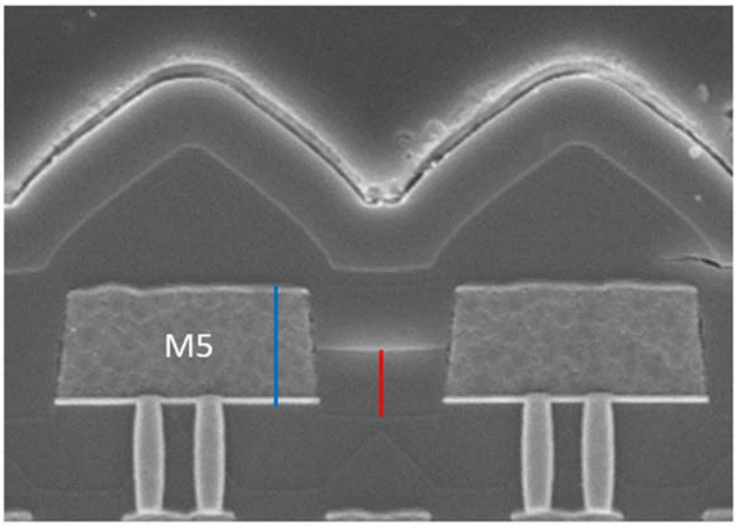
depositing a first void-free layer of a first dielectric over the top layer using high density plasma chemical vapor deposition at a first D/S ratio.



211. During the manufacture of the NXP ASL2500SHNY, a second void-free layer of a second dielectric was deposited over the first void-free layer at a second D/S ratio:



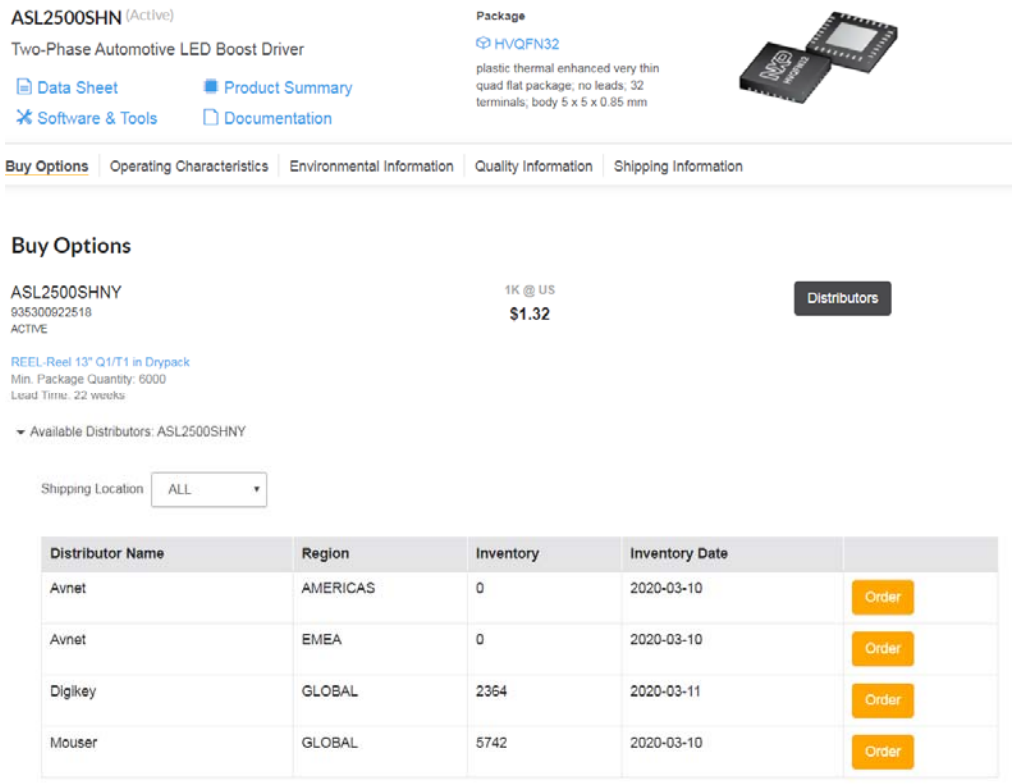
212. The first layer was also applied with a thickness of at least 40% (here, approximately 55%) of the height of the features.



213. Claim 5 of the Chesire Patent applies to each Chesire Accused Product at least because each of those products were manufactured with the same or similar two or more void-free layers of passivation located on the top layer of a semiconductor device with the final metal layer being aluminum, like the NXP ASL2500SHNY.

214. On information and belief, each of the Chesire Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

215. By way of example only, the NXP ASL2500SHNY has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least three NXP-authorized Americas and Global distributors:



ASL2500SHN (Active)

Two-Phase Automotive LED Boost Driver

Data Sheet | Product Summary | Software & Tools | Documentation

Package

HVQFN32

plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

ASL2500SHNY
935300922518
ACTIVE

1K @ US
$1.32

Distributors

REEL-Reel 13" Q1/T1 in Drypack
Min. Package Quantity: 6000
Lead Time: 22 weeks

Available Distributors: ASL2500SHNY

Shipping Location ALL

Distributor Name	Region	Inventory	Inventory Date	
Avnet	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	0	2020-03-10	Order
Digikey	GLOBAL	2364	2020-03-11	Order
Mouser	GLOBAL	5742	2020-03-10	Order

See https://www.nxp.com/part/ASL2500SHN#/ (last visited March 11, 2020).

216. NXP has known of the Chesire Patent and has been on notice of its infringement of the Chesire Patent since at least January 22, 2007. On January 22, 2007, Mr. Jim Zajko, Senior Manager of Intellectual Property, for Agere, then-assignee of the Chesire Patent, sent a letter to Mr. Hans Pennings, Senior Vice President of Intellectual Property & Licensing, for NXP, identifying NXP's PNX7850E and PCF5213EL1 Die B as infringing and exemplary of NXP's infringement of the Chesire Patent. On information and belief, Agere and LSI, the subsequent assignee of the Chesire Patent, engaged in licensing discussions with NXP over the next year. On February 1, 2008, NXP filed a declaratory judgment of invalidity of the Chesire Patent, among other patents, against LSI, a prior assignee of the Chesire Patent. *See NXP Semiconductors USA, Inc. v. LSI Corporation,* Case No. 5:08-cv-0775 (N.D. Cal.) ("LSI Litigation"). On information and belief, the LSI Litigation led to a since-expired license between

NXP and LSI that included the Chesire Patent. On January 9, 2019, Bell Semic sent a letter to NXP identifying the FXTH87EH11DT1, FXAS21002CQR1, ASL2500SHNY, and LPC11U35FET48 as infringing and exemplary of NXP's infringement of the Chesire Patent. NXP has not substantively responded to the allegations in this letter.

217. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Chesire Patent at least because NXP has had notice of the Chesire Patent since January 22, 2007 and had previously entered into a license for the Chesire Patent.

218. NXP, knowing that the process of manufacturing its Accused Chesire Products infringed the Chesire Patent and with specific intent for others to infringe the Chesire Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Chesire Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Chesire Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Chesire Accused Products, as well as products incorporating the same.

219. NXP has known since at least January 22, 2007 that the process of manufacturing the Chesire Accused Products infringed the Chesire Patent. Despite this knowledge, NXP knowingly and intentionally instructed its OEMs and foundry suppliers to infringe the Chesire Patent through the unlicensed manufacture of the Chesire Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Chesire Patent by its customers', distributors', and/or other third parties' sale and distribution of the Chesire Accused Products with the expectation that such

products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted infringement of the Chesire Patent through the use, sale, offer for sale, and/or importing the Chesire Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

220. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Chesire Accused Products and/or products incorporating the Chesire Accused Products in the United States by marketing the Chesire Accused Products in the United States; providing information such as detailed datasheets supporting use of the Chesire Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Chesire Accused Products; providing technical documentation for the Chesire Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Chesire Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Chesire Accused Products, including live training and video.

221. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past infringement, in an amount adequate to compensate for NXP's infringement, but in no event

less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

222. NXP's infringement of the Chesire Patent was knowing, deliberate, and willful. NXP learned of its infringement of the Chesire Patent no later than January 22, 2007. As detailed above, on January 22, 2007, Agere, a prior assignee of the Chesire Patent, sent a letter to NXP identifying two NXP products as infringing and exemplary of NXP's infringement of the Chesire Patent, and subsequently engaged in licensing discussions over the next year. On February 1, 2008, NXP filed the LSI Litigation, which, on information and belief, led to a since-expired license between NXP and LSI that included the Chesire Patent. On January 9, 2019, Bell Semic sent a letter to NXP identifying three additional NXP products as infringing and exemplary of NXP's infringement of the Chesire Patent. NXP has not substantively responded to this letter. Despite these efforts, and knowing that it was willfully infringing the Chesire Patent, NXP continued to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Chesire Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct was egregious. NXP's knowing, deliberate, and willful infringement of the Chesire Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 7

Willful Infringement of U.S. Patent No. 6,743,669 (Lin Patent)

223. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

224. The Lin Patent is generally related to a dielectric film block used in semiconductor processing to protect selected areas of the wafer, which may include resistors, from silicidation. (*See* Lin Patent, Abstract.)

225. Silicides are used in the manufacture of semiconductor devices to enhance signal propagation through transistors. A conventional silicide process produces a low resistance silicide region on the top of a transistor's polysilicon ("poly") gate electrode and interconnect. The silicide has a lower resistance than the underlying doped silicon or poly. As a result, signal propagation through the transistor (gate and interconnect) is enhanced. A silicide prepared by a self-aligned process is called a salicide. Though silicide formation may be desirable to reduce interconnect resistance in active devices, it is undesirable in applications where resistors are formed. Both active and passive (i.e., capacitors and resistors) components are commonly found in semiconductor devices. During the salicidation process, salicide blocks are used to mask the resistor areas from silicide films, maintaining the high resistance characteristics of the poly or other type of resistor. The conventional salicide block process generally includes the deposition of a relatively thick low-temperature oxide which is then masked to protect the resistor areas. The exposed areas are etched using a timing etched process to create a thin oxide to remain in the active areas. But this timed-etch suffers from variability induced by the etching process and salicide preclean steps. This variability creates conditions of over etch producing oxide areas that are too thin or conditions of under etch resulting in incomplete salicidation. The Lin Patent solved this problem by providing a more effective salicide block process with greater process margin.

226. The Lin Patent contains 2 independent claims and 19 total claims, covering various methods. Claim 1 reads:

A method of forming a dielectric layer to protect selected areas of a semiconductor wafer from a silicide process, the method comprising:

disposing an oxide film on the wafer;

disposing a block dielectric layer comprising one of Si_3N_4 and SiON on the oxide film;

forming a block mask over the wafer having the oxide film and block dielectric layer disposed on it, wherein the block mask is patterned to divide the mask into masked areas over the selected areas and unmasked areas left exposed, the selected areas including at least one resistor;

etching the block dielectric layer in the unmasked areas to expose the oxide film, wherein the oxide film is used as an etch stop layer;

removing said block mask;

removing the exposed portions of the oxide film after removing said block mask to expose at least one silicon area; and

forming a silicide on the exposed at least one silicon area of the semiconductor wafer.

227. NXP USA has directly infringed one or more claims of the Lin Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Lin Patent and/or NXP USA has directly infringed one or more claims of the Lin Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Lin Patent (*e.g.*, claims 5-8). Such products manufactured using these infringing methods include, but are not limited to:

- NXP products manufactured using block dielectric layers over selected poly resistors to prevent silicidation;

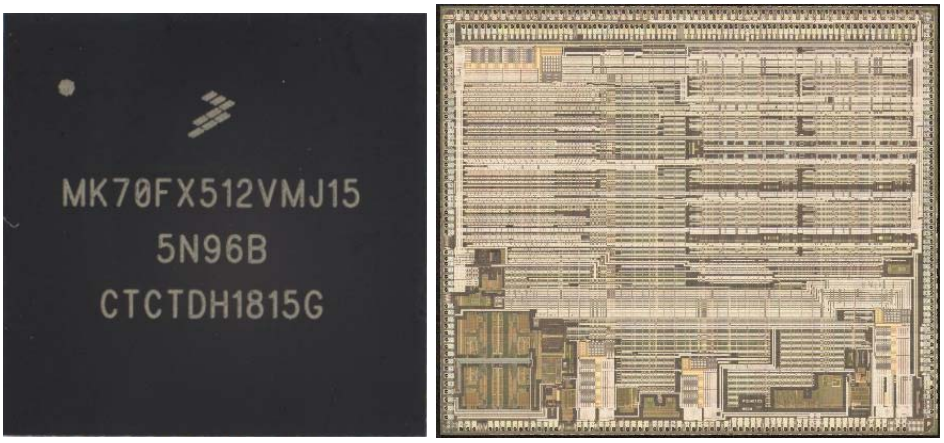
- NXP's MK70FX512VMJ15, an ARM cortex processor used in applications such as industrial control panels, navigational displays, point-of-sale terminals, and medical monitoring equipment;
- NXP's MWCT1012CFM, a wireless charging transmitter used for handheld consumer applications;
- NXP's MCIMX7S5EVM08SC, an i.MX 7Solo processor used in audio, connected devices, access control panels, human-machine interfaces, portable medical and health care, IP phones, smart applications, PoS devices, eReaders, wearables, and home energy management systems;
- NXP's Freescale PCIMX7D7DVM10SA, an i.MX applications processor; and
- NXP's devices that are variants of the above-identified products;

(collectively "Lin Accused Products").

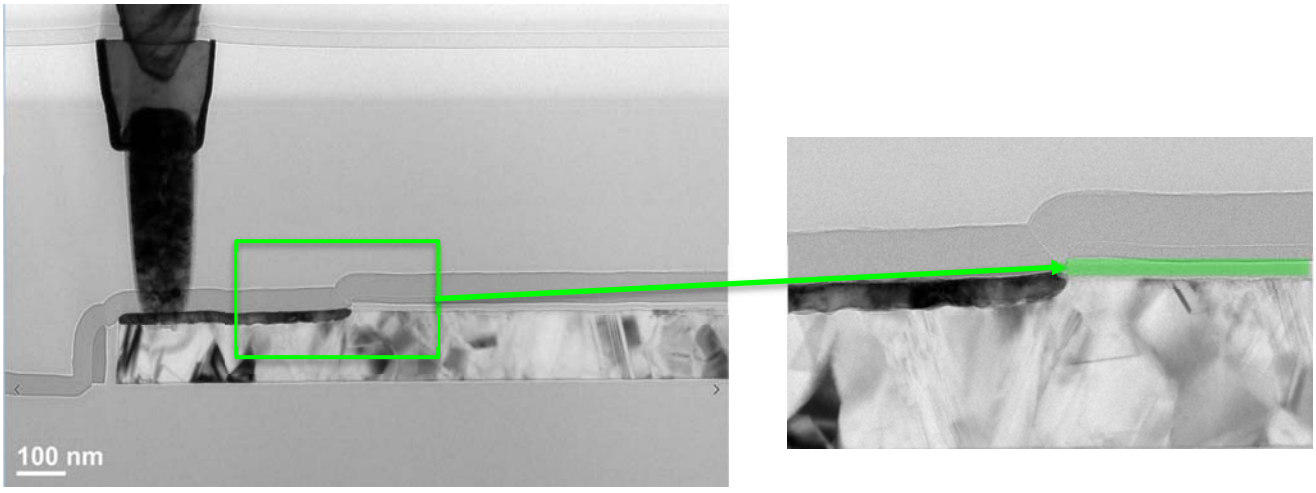
228. By way of non-limiting example only, the process of manufacturing the NXP MK70FX512VMJ15 meets all the steps of claim 1 of the Lin Patent including forming a dielectric layer to protect selected areas of a semiconductor wafer from a silicide process, including the steps of (1) disposing an oxide film on the wafer; (2) disposing a block dielectric layer comprising one of Si_3N_4 and SiON on the oxide film; (3) forming a block mask over the wafer having the oxide film and block dielectric layer disposed on it, wherein the block mask is patterned to divide the mask into masked areas over the selected areas and unmasked areas left exposed, the selected areas including at least one resistor; (4) etching the block dielectric layer in the unmasked areas to expose the oxide film, wherein the oxide film is used as an etch stop layer; (5) removing the block mask; (6) removing the exposed portions of the oxide film after removing

the block mask to expose at least one silicon area; and (7) forming a silicide on the exposed at least one silicon area of the semiconductor wafer.

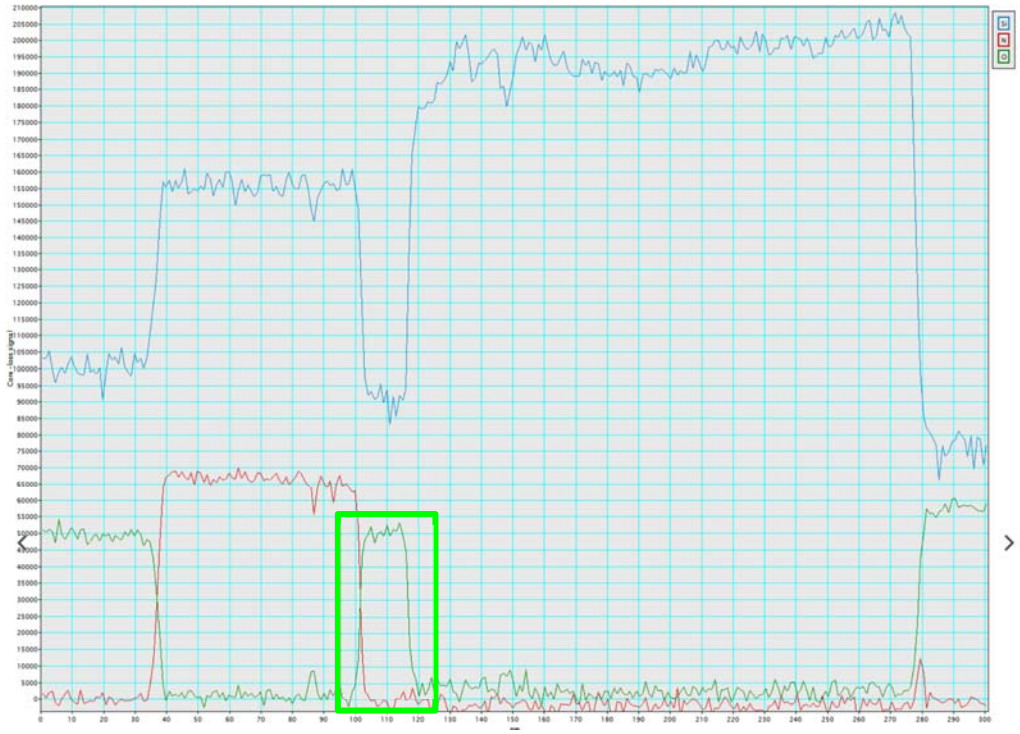
229. As shown below, the NXP MK70FX512VMJ15 is a semiconductor device.



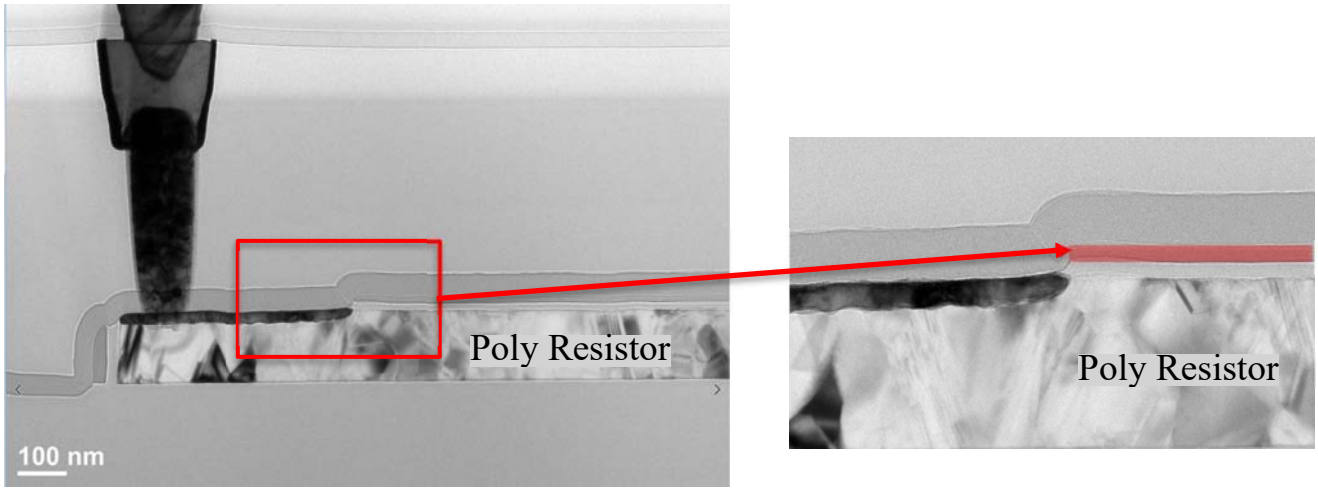
230. During manufacture of the NXP MK70FX512VMJ15, an oxide film is disposed on the semiconductor wafer (see enlarged green section and green line showing the oxide layer).



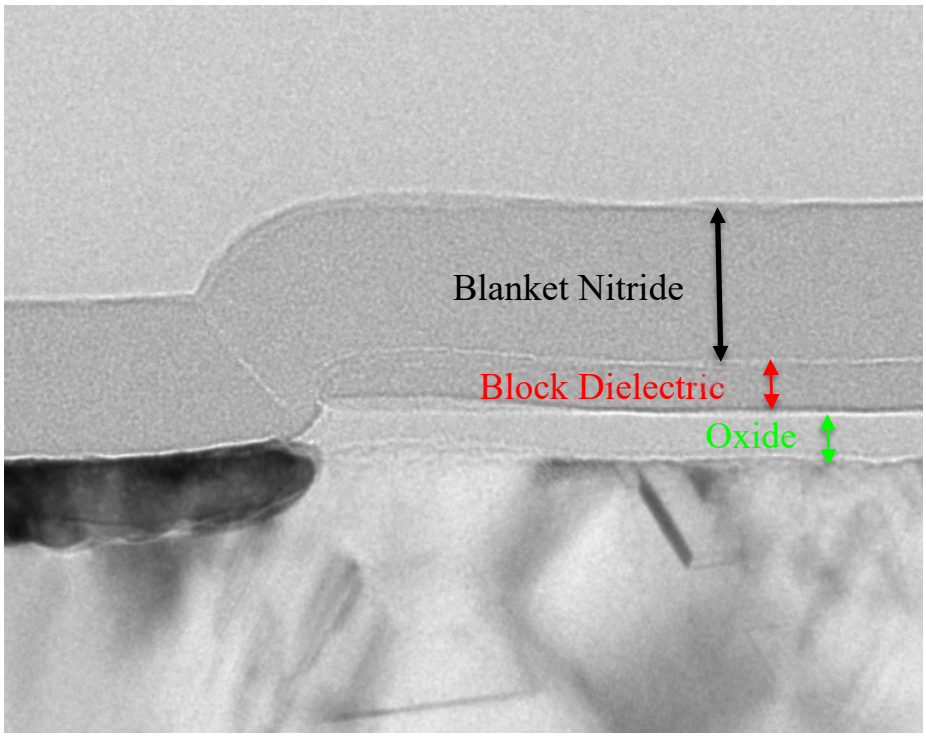
A spectrum profile shows this layer is an oxide film approximately 15nm thick (*see* green outline below). The blue, red, and green lines indicate silicon, nitrogen, and oxygen, respectively:



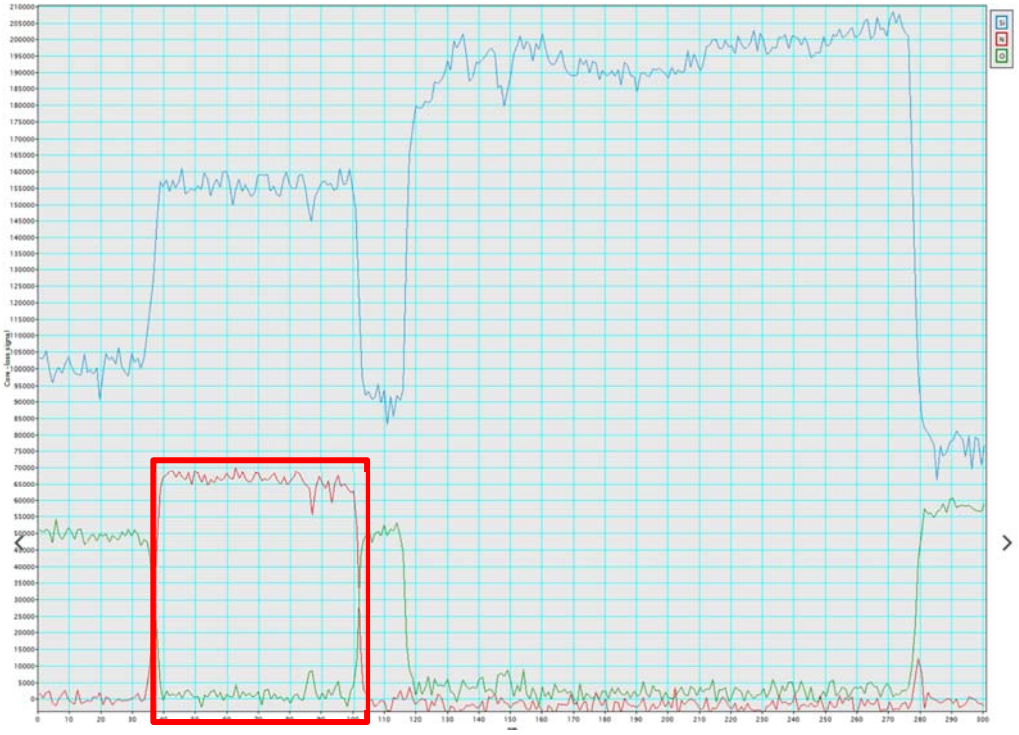
231. During manufacture of the NXP MK70FX512VMJ15, a block dielectric layer comprising one of Si_3N_4 and SiON is disposed on the oxide film. The film (designated with the red arrow) over the oxide film and poly resistor comprises the block dielectric layer with a thicker blanket nitride layer disposed over the resistor and active regions.



An enlarged section of the resistor more clearly shows the delineation between the oxide film, the block dielectric layer, and the thicker blanket nitride layer.

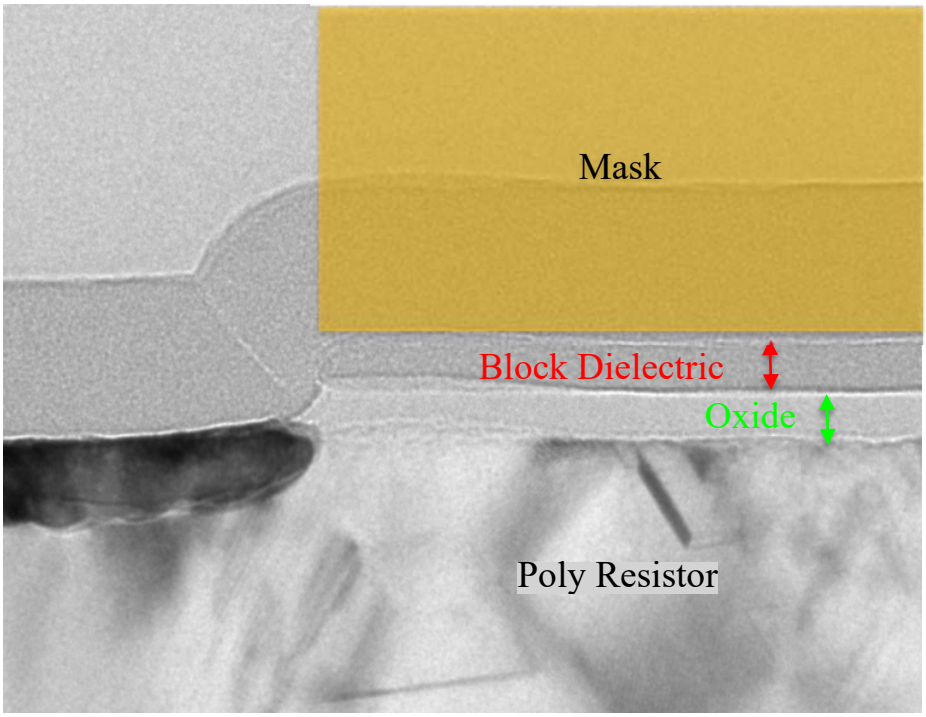


A spectrum profile shows the block dielectric layer and blanket nitride layer are each silicon nitride layers (*see* red outline below). The total nitride stack is approximately 60-65nm thick, and the block dielectric layer is approximately the same thickness as the oxide layer.



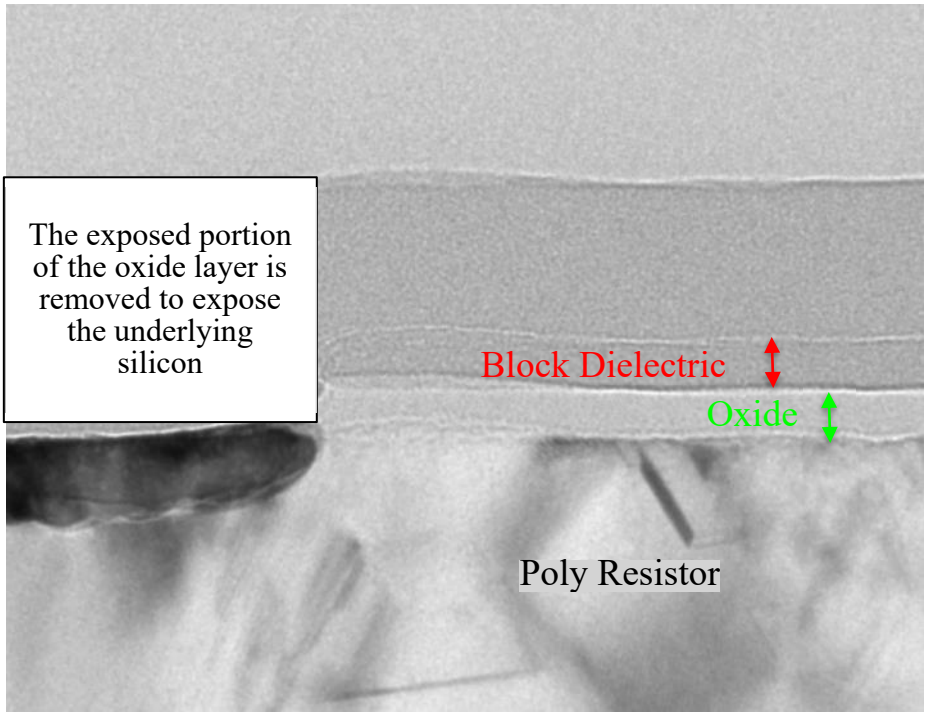
232. During manufacture of the NXP MK70FX512VMJ15, a block mask is formed over the wafer having the oxide film and block dielectric layer disposed on it, wherein the block mask is patterned to divide the mask into masked areas over the selected areas and unmasked areas left exposed, where the selected areas include at least one resistor.

233. During manufacture of the NXP MK70FX512VMJ15, the block dielectric layer is etched in the unmasked areas to expose the oxide film, wherein the oxide film is used as an etch stop layer. This is illustrated by the absence of a block dielectric layer in the unmasked area, which was etched to expose the underlying oxide film.

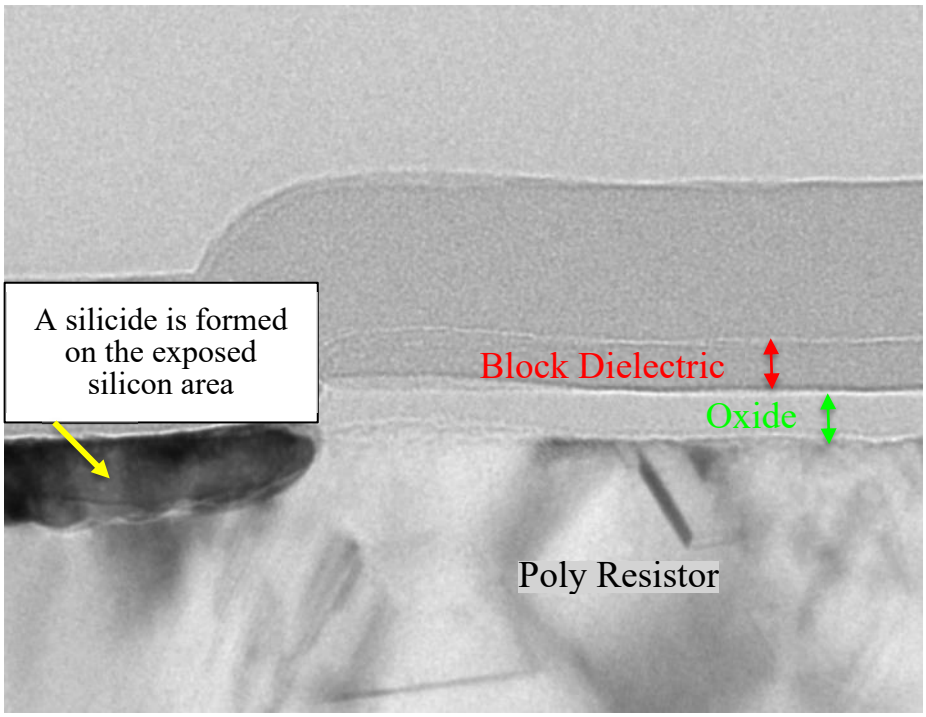


234. During manufacture of the NXP MK70FX512VMJ15, the block mask is removed.

235. During manufacture of the NXP MK70FX512VMJ15, the exposed portions of the oxide film are etched after removing the block mask to expose at least one silicon area.



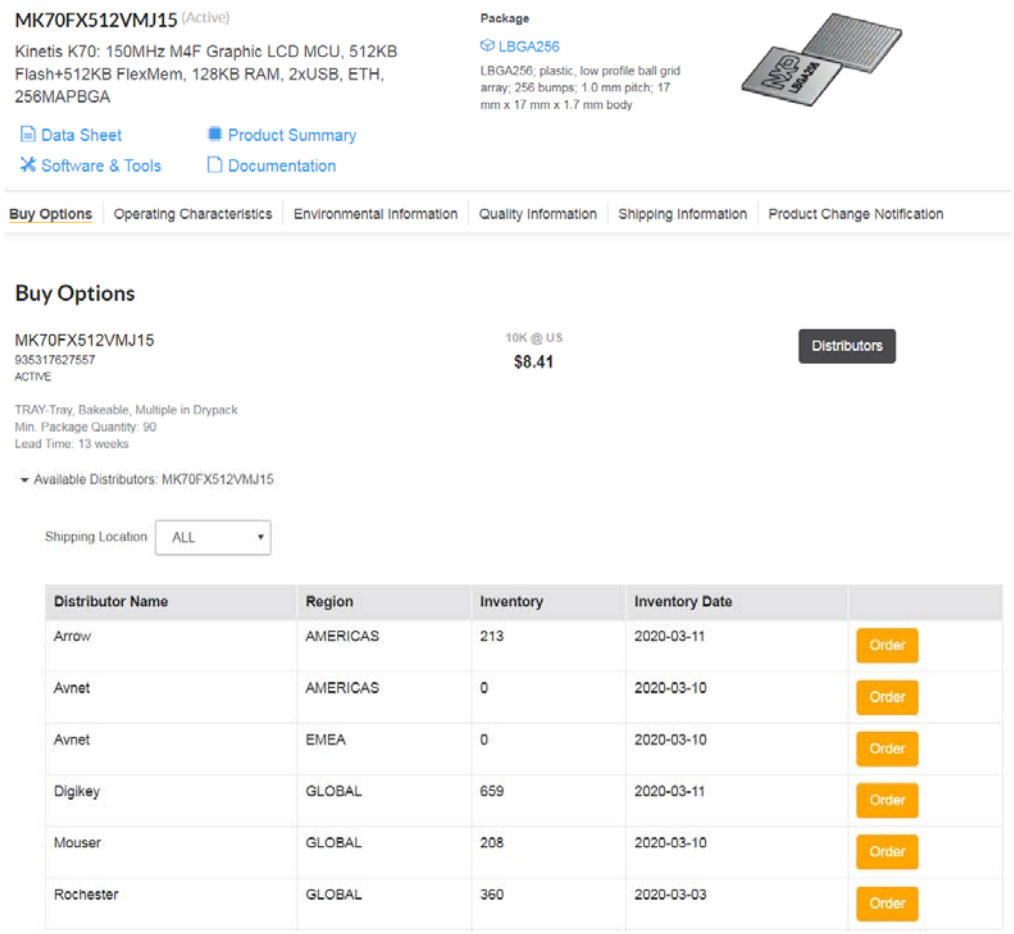
236. During manufacture of the NXP MK70FX512VMJ15, a silicide is formed on the exposed at least one silicon area of the semiconductor wafer.



237. Claim 1 of the Lin Patent applies to each Lin Accused Product at least because each of those products were manufactured using the same or similar block dielectric layers over selected poly resistors to prevent silicidation, like the NXP MK70FX512VMJ15.

238. On information and belief, each of the Lin Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

239. By way of example only, the NXP MK70FX512VMJ15 has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Americas and Global distributors:



MK70FX512VMJ15 (Active)

Kinetis K70: 150MHz M4F Graphic LCD MCU, 512KB Flash+512KB FlexMem, 128KB RAM, 2xUSB, ETH, 256MAPBGA

Data Sheet | Product Summary | Software & Tools | Documentation

Package

LBGA256

LBGA256; plastic, low profile ball grid array; 256 bumps; 1.0 mm pitch; 17 mm x 17 mm x 1.7 mm body

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information | Product Change Notification

Buy Options

MK70FX512VMJ15
935317627557
ACTIVE

TRAY-Tray, Bakeable, Multiple in Drypack
Min. Package Quantity: 90
Lead Time: 13 weeks

10K @ US
$8.41

Distributors

Available Distributors: MK70FX512VMJ15

Shipping Location ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	213	2020-03-11	Order
Avnet	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	0	2020-03-10	Order
Digikey	GLOBAL	659	2020-03-11	Order
Mouser	GLOBAL	208	2020-03-10	Order
Rochester	GLOBAL	360	2020-03-03	Order

See https://www.nxp.com/part/MK70FX512VMJ15#/ (last visited March 11, 2020).

240. NXP has known of the Lin Patent and has been on notice of its infringement of the Lin Patent since at least February 21, 2020, when Bell Semic first identified the MK70FX512VMJ15, MWCT1012CFM, MCIMX7S5EVM08SC, and PCIMX7U5DVP08SC as exemplary of NXP's infringement of the Lin Patent. NXP has not responded to this letter.

241. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Lin Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

242. NXP, knowing that the process of manufacturing its Accused Lin Products infringed the Lin Patent and with specific intent for others to infringe the Lin Patent, has induced

infringement of, and continues to induce infringement of, one or more claims of the Lin Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Lin Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Lin Accused Products, as well as products incorporating the same.

243. NXP has known since at least February 21, 2020 that the process of manufacturing the Lin Accused Products infringed the Lin Patent. Despite this knowledge, NXP knowingly and intentionally instructed, and continues to instruct, its OEMs and foundry suppliers to infringe the Lin Patent through the unlicensed manufacture of the Lin Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Lin Patent by its customers', distributors', and/or other third parties' sale and distribution of the Lin Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Lin Patent through the use, sale, offer for sale, and/or importing the Lin Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

244. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Lin Accused Products and/or products incorporating the Lin Accused Products in the United States by marketing the Lin Accused

Products in the United States; providing information such as detailed datasheets supporting use of the Lin Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Lin Accused Products; providing technical documentation for the Lin Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Lin Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Lin Accused Products, including live training and video.

245. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

246. NXP's infringement of the Lin Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Lin Patent no later than February 21, 2020. As detailed above, Bell Semic sent a letter on February 21, 2020, identifying 4 NXP products as exemplary of NXP's infringement of the Lin Patent. NXP has not responded to this letter. Despite these efforts, and knowing that it was willfully infringing the Lin Patent, NXP continued and continues to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Lin Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP

otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Lin Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 8

Willful Infringement of U.S. Patent No. 6,544,907 (Ma Patent)

247. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

248. The Ma Patent is generally related to methods for manufacturing a high-quality gate oxide layer having a uniform thickness, including providing a semiconductor substrate, and forming an oxide layer having a substantially uniform thickness on the semiconductor substrate, and in a zone of pressure of less than about 4 Torr or greater than about 25 Torr. (*See* Ma Patent, Abstract.)

249. During the manufacture of metal-oxide-semiconductor transistors, a gate oxide layer is formed. The thickness and uniformity of the gate oxide layer can significantly impact the overall operation of the device being formed. As transistors have shrunk in size, the thickness of the gate oxide has correspondingly shrunk. And, as the thickness has continued to decrease, the thickness uniformity of the gate oxide layer has become increasingly important. Prior to the Ma Patent, gate oxide layer manufacturing was performed at pressures ranging from 10 Torr to about 15 Torr, however, forming gate oxides within such pressure ranges produces very non-uniform gate oxides. The Ma Patent provided a solution to these non-uniform gate oxides by teaching the formation of gate oxide layers at pressures of less than about 4 Torr or greater than about 25

Torr, which can be used to form a substantially uniform gate oxide layer, such as one that has a thickness that varies by less than about 0.2 nm.

250. The Ma Patent contains 4 independent claims and 17 total claims, covering various semiconductor devices and methods. Claim 1 reads:

> A method for manufacturing a high quality oxide layer having a uniform thickness, comprising:
>
> providing a semiconductor substrate, and
>
> forming a gate oxide layer having a substantially uniform thickness on the semiconductor substrate, the gate oxide layer having a range of thicknesses that varies by less than about 0.2 nm.

251. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Ma Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Ma Patent, and/or NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Ma Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Ma Patent (*e.g.*, claims 1, 2, 7, 9, 14, and 15). Such products manufactured using these infringing methods include, but are not limited to:

- NXP products with a high quality oxide layer having a substantially uniform thickness, including at least those products manufactured on Technology Nodes 28 nm through 14 nm;
- NXP's PCIMX7D7DVM10SA, an i.MX applications processor;
- NXP's MCIMX7S5EVM08SC, an i.MX 7Solo processor used in audio, connected devices, access control panels, human-machine interfaces, portable medical and

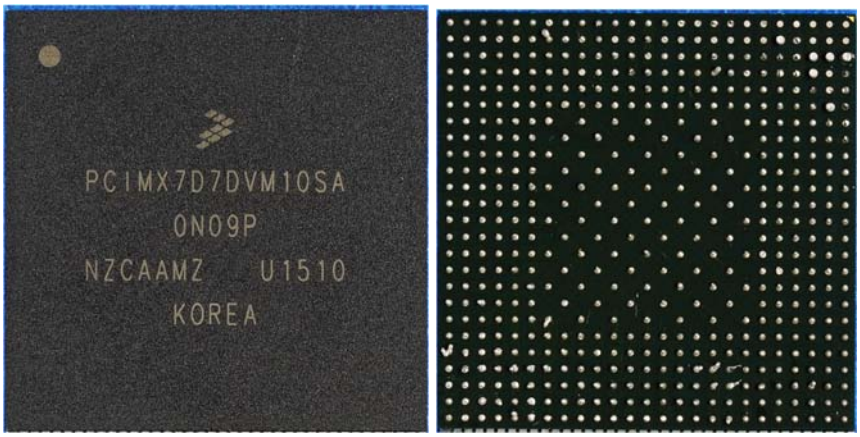
health care, IP phones, smart applications, PoS devices, eReaders, wearables, and home energy management systems;

- NXP's MIMX8MM6DVTLZAA, an i.MX 8M Mini application processor; and
- NXP's devices that are variants of the above-identified products;

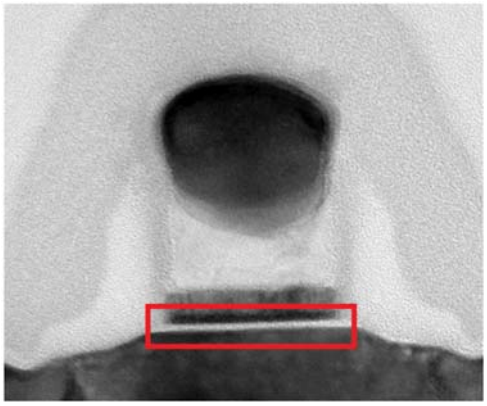
(collectively "Ma Accused Products").

252. By way of non-limiting example only, the processes of manufacturing the PCIMX7D7DVM10SA and the MIMX8MM6DVTLZAA meet all the steps of claim 1 of the Ma Patent including forming a gate oxide layer having a substantially uniform thickness on the semiconductor substrate, wherein the gate oxide layer has a range of thicknesses that varies by less than about 0.2 nm.

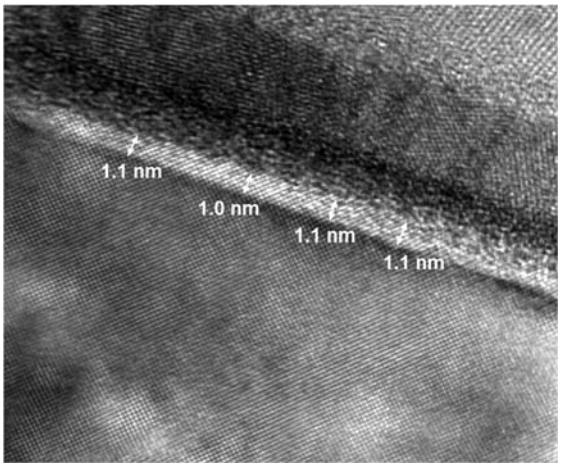
253. As shown below, the NXP PCIMX7D7DVM10SA is a semiconductor device:



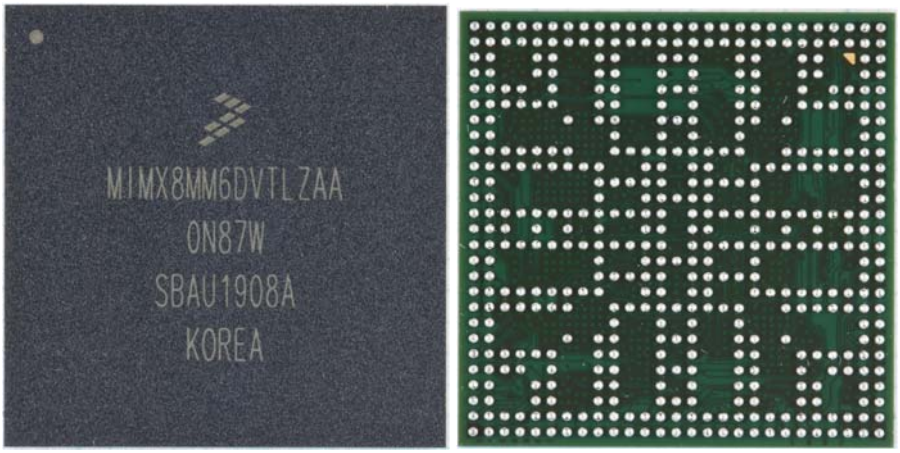
254. The NXP PCIMX7D7DVM10SA is manufactured to have a gate oxide layer (identified in red below) formed that has a substantially uniform thickness on a semiconductor substrate:



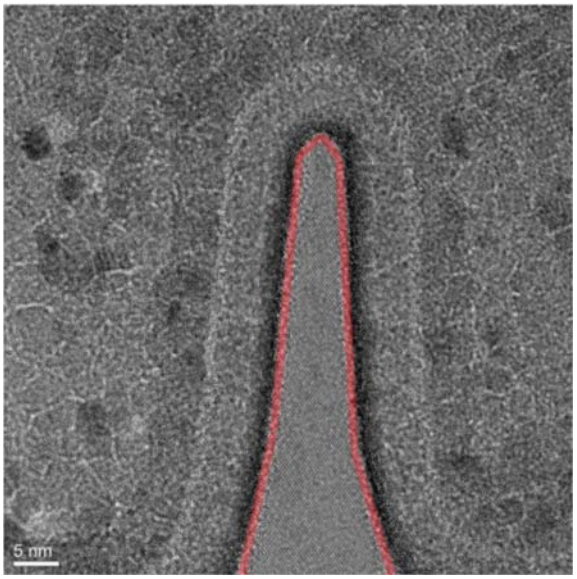
255. As shown below, the gate oxide layer of the NXP PCIMX7D7DVM10SA has a substantially uniform thickness that varies less than 0.2 nm:



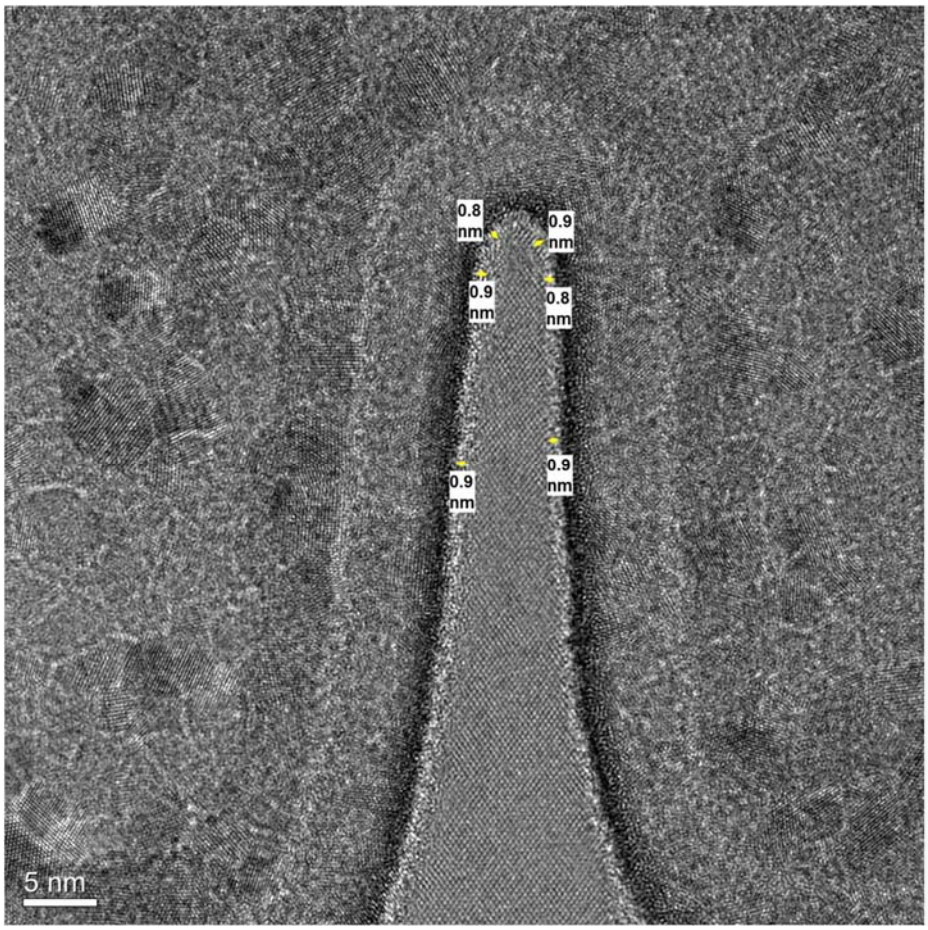
256. As shown below, the NXP MIMX8MM6DVTLZAA is a semiconductor device:



257. The NXP MIMX8MM6DVTLZAA is manufactured to have a gate oxide layer (in red below) formed that has a substantially uniform thickness on a semiconductor substrate:



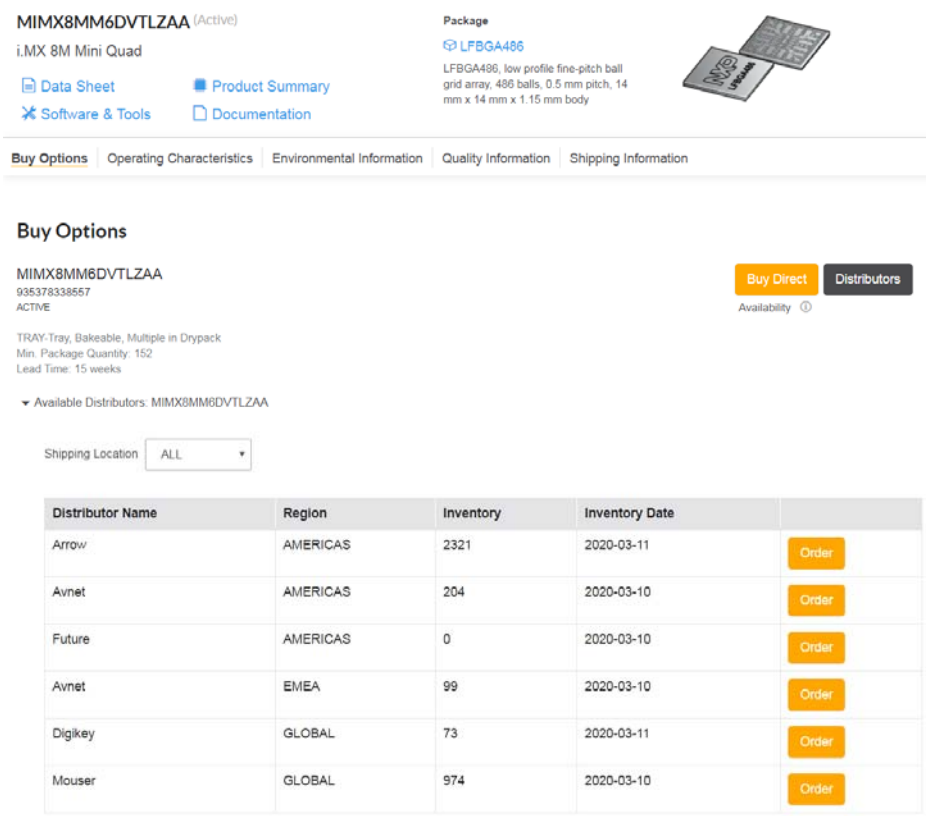
258. As shown below, the gate oxide layer of the NXP MIMX8MM6DVTLZAA has a substantially uniform thickness that varies less than 0.2 nm:



259. Claim 1 of the Ma Patent applies to each Ma Accused Product at least because each of those products are manufactured on the same or similar technology nodes, including at least Technology Nodes 28 nm through 14 nm, as the above-identified products or other technology nodes using similar processes.

260. On information and belief, each of the Ma Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

261. By way of example only, the NXP MIMX8MM6DVTLZAA has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Americas and Global distributors:



MIMX8MM6DVTLZAA (Active)

i.MX 8M Mini Quad

Data Sheet | Product Summary

Software & Tools | Documentation

Package

LFBGA486

LFBGA486, low profile fine-pitch ball grid array, 486 balls, 0.5 mm pitch, 14 mm x 14 mm x 1.15 mm body

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

MIMX8MM6DVTLZAA
935378338557
ACTIVE

TRAY-Tray, Bakeable, Multiple in Drypack
Min. Package Quantity: 152
Lead Time: 15 weeks

Buy Direct | Distributors

Availability

Available Distributors: MIMX8MM6DVTLZAA

Shipping Location: ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	2321	2020-03-11	Order
Avnet	AMERICAS	204	2020-03-10	Order
Future	AMERICAS	0	2020-03-10	Order
Avnet	EMEA	99	2020-03-10	Order
Digikey	GLOBAL	73	2020-03-11	Order
Mouser	GLOBAL	974	2020-03-10	Order

See https://www.nxp.com/part/MIMX8MM6DVTLZAA#/ (last visited March 11, 2020).

262. NXP has known of the Ma Patent and has been on notice of its infringement of the Ma Patent since at least February 21, 2020, when Bell Semic sent a letter to NXP identifying the MCIMX7S5EVM08SC, PCIMX7D7DVM10SA, and MIMX8MMDVTLZAA as infringing the Ma Patent. NXP has not responded to this letter.

263. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Ma Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

264. NXP, knowing that the process of manufacturing its Accused Ma Products infringes the Ma Patent and with specific intent for others to infringe the Ma Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Ma Patent

under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Ma Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Ma Accused Products, and products incorporating same.

265. NXP knows, and has known since at least February 21, 2020, that the process of manufacturing the Ma Accused Products infringes the Ma Patent. Despite this knowledge, NXP knowingly and intentionally instructed, and continues to instruct, its OEMs, package assemblers, and foundry suppliers to infringe the Ma Patent through the unlicensed manufacture and assembly of the Ma Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. NXP further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Ma Patent by its customers', distributors', and/or other third parties' sale and distribution of the Ma Accused Products with the expectation that such products, and/or products incorporating the same, will be imported into the United States market where they will be used, sold, and/or offered for sale. NXP further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Ma Patent through the use, sale, offers for sale, and/or importation in or into the United States the Ma Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website.

266. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Ma Accused Products and/or products incorporating the Ma Accused Products in the United States by marketing the Ma Accused Products in the United States; providing information such as detailed datasheets supporting use

of the Ma Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Ma Accused Products; providing technical documentation for the Ma Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Ma Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Ma Accused Products, including live training and video.

267. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement of the Ma Patent, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

268. NXP's infringement of the Ma Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Ma Patent no later than February 21, 2020. As detailed above, Bell Semic sent a letter to NXP on February 21, 2020, identifying the Ma Patent as being infringed by 3 NXP products. NXP has not responded to the letter. Despite these efforts, and knowing that it was willfully infringing the Ma Patent, NXP continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Ma Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement

of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Ma Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 9

Willful Infringement of U.S. Patent No. 6,342,734 (Allman Patent)

269. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

270. The Allman Patent is generally related to a metal-insulator-metal capacitor formed between interconnect layers of an integrated circuit with one of the plates of the capacitor formed integrally with one of the interconnect layers. (*See* Allman Patent, Abstract.)

271. Due to advances in fabrication of integrated circuits, such as through improvements in planarization processes such as chemical mechanical polishing (CMP), multiple layers of interconnects were able to be fabricated. With multiple interconnect layers, capacitors were then able to be incorporated between the interconnect layers in the intermetal dielectric insulating material separating the interconnect layers. Such capacitors typically were metal-insulator-metal (MIM) capacitors having metal plates formed on the metal conductors of the interconnect layers. The Allman Patent teaches an improved metal-insulator-metal (MIM) capacitor, where one of the plates of the capacitor is integrated with a layer of metal in an interconnect, thus facilitating the simultaneous fabrication of the interconnect layer and a part of the capacitor. This straightforward construction led to greater reliability, more control over the capacitive characteristics, and lowered risks of an improperly formed capacitor and/or diminished effectiveness of the integrated circuit.

272. The Allman Patent contains 2 independent claims and 15 total claims, covering various integrated circuit package substrates. Claim 1 reads:

> In an integrated circuit (IC) having a substrate containing functional components and an interconnect layer overlying the substrate to connect selected ones of the functional components, an improvement comprising:
>
> a capacitor comprising two plates and a dielectric layer interposed between the two plates, a bottom one of the plates comprising a portion of the interconnect layer and a top one of the plates comprising a single metal layer.

273. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Allman Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Allman Patent (*e.g.*, claims 1-9 and 12-15), including, but not limited to:

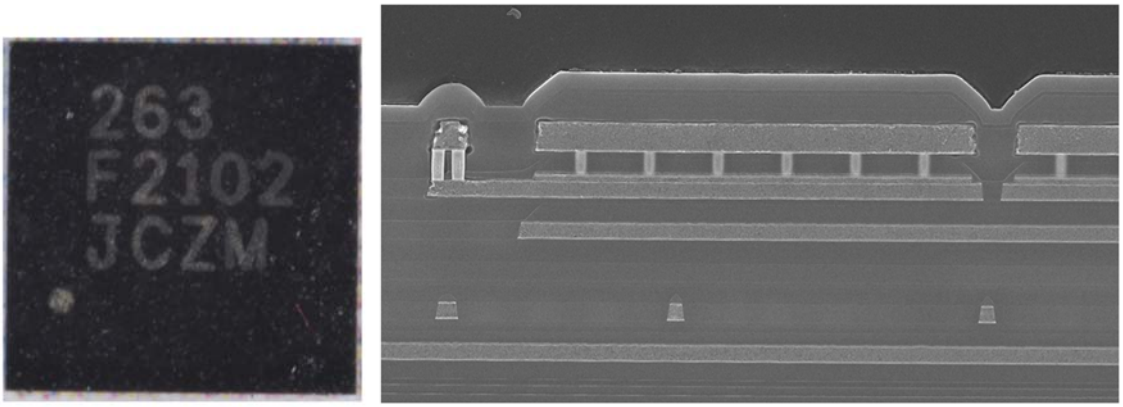
- NXP products with a capacitor with two plates where the bottom plate is part of the interconnect layer and the top plate is a metal layer positioned within the inter-layer dielectric;
- NXP's FXAS21002CQR1, a 3-axis gyroscope for use in game controllers, electronic compass stabilization and enhanced motion control;
- NXP's TDA18250AHN/C, a silicon tuner used in set top boxes (STBs);
- NXP's FXTH87EH11DT1, a tire pressure sensor with a dual-axis accelerometer architecture; and
- NXP's devices that are variants of the above-identified products;

(collectively, the "Allman Accused Products").

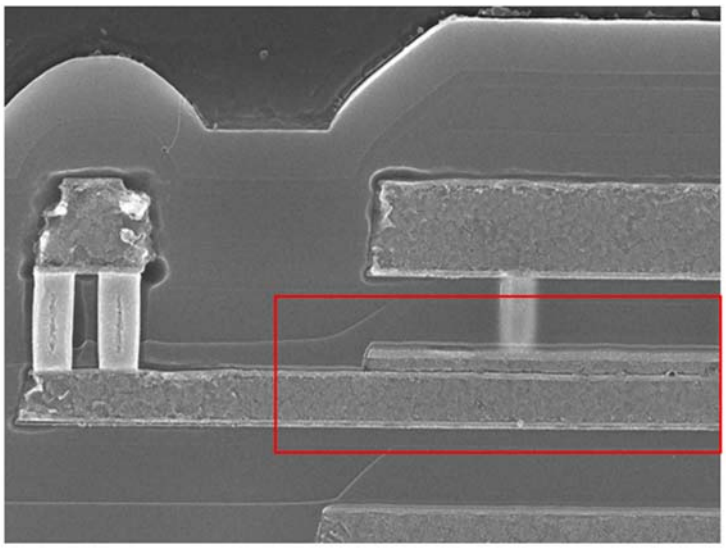
274. By way of non-limiting example only, NXP's FXAS21002CQR1 infringes claim 1 of the Allman Patent because it is an integrated circuit that has a substrate with functional

components and an interconnect layer overlaying the substrate to connect selected ones of the functional components, that includes a capacitor with two plates and a dielectric layer interposed between the two plates, where a bottom one of the plates includes a portion of the interconnect layer and a top one of the plates includes a single metal layer.

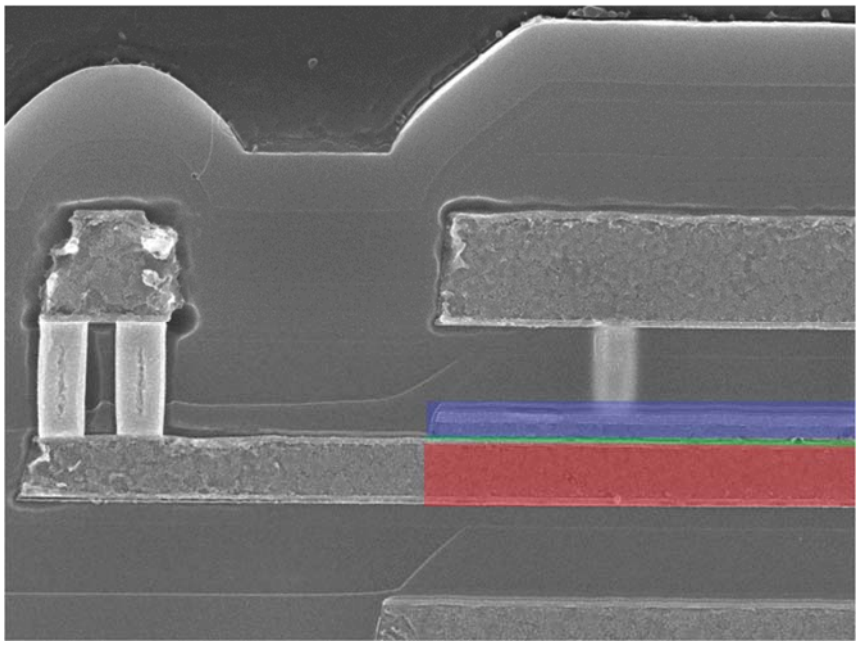
275. As shown below, NXP's FXAS21002CQR1 is an integrated circuit that has a substrate with functional components and an interconnect layer overlaying the substrate to connect selected ones of the functional components.



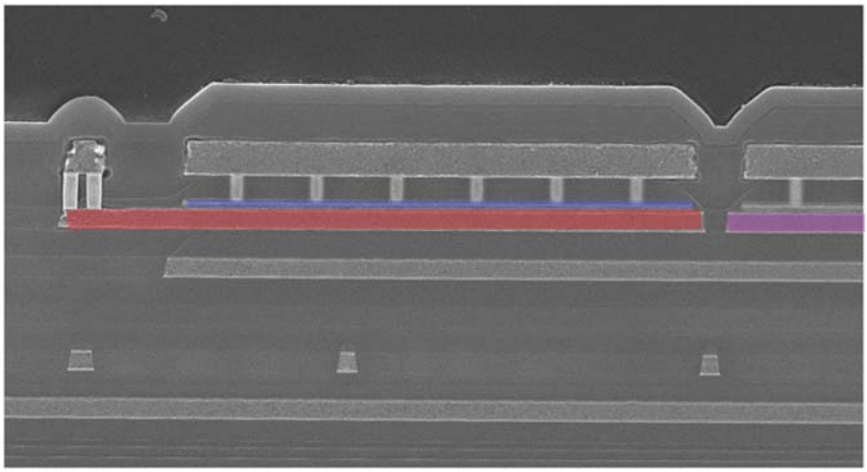
276. NXP's FXAS21002CQR1 includes a capacitor.



277. This capacitor includes two plates (*e.g.*, blue and red below) and a dielectric layer (*e.g.*, green below) interposed between the two plates.



278. The bottom plate (e.g., red below) comprises a portion of the interconnect layer (interconnect layer also includes at least portion in purple below). The top plate (e.g., blue below) comprises a single metal layer.

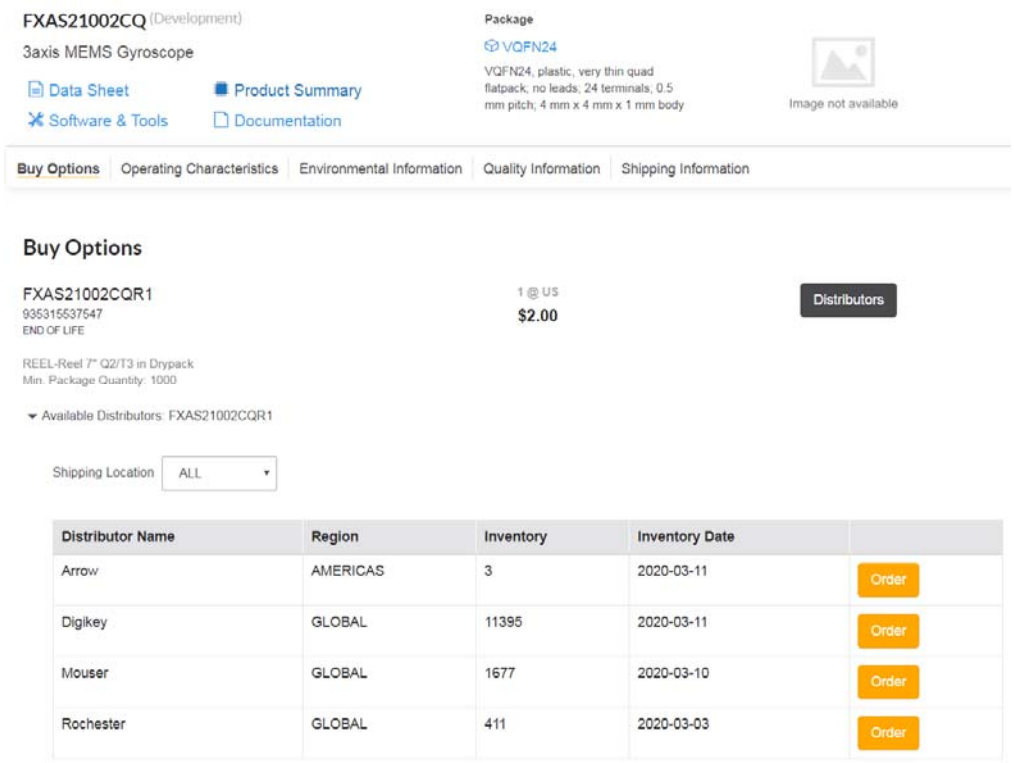


279. Claim 1 of the Allman Patent applies to each Allman Accused Product at least because each of those products includes the same or similar capacitor with two plates where the

bottom plate is part of the interconnect layer and the top plate is a metal layer positioned within the inter-layer dielectric, like the NXP FXAS21002CQR1.

280. On information and belief, each of the Allman Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

281. By way of example only, the NXP FXAS21002CQR1 has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least four NXP-authorized Americas and Global distributors:



See https://www.nxp.com/part/FXAS21002CQ#/ (last visited March 11, 2020).

282. NXP has known of the Allman Patent and has been on notice of its infringement of the Allman Patent since at least January 9, 2019 when Bell Semic first identified the TDA18250AHN/C and FXAS21002CQR1 as exemplary of NXP's infringement of the Allman

Patent. On September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Allman Patent to these same products. On February 21, 2020, Bell Semic sent a letter further identifying the FXTH87EH11DT1 as exemplary of NXP's infringement of the Allman Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products.

283. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Allman Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

284. NXP, knowing its products infringe the Allman Patent and with specific intent for others to infringe the Allman Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Allman Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Allman Accused Products, as well as products incorporating the same. NXP knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website. NXP actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Allman Accused Products in the United States. NXP knows, and has known since at least January 9, 2019, that the Allman Accused Products infringe the Allman Patent, and purposefully and knowingly sells and offers to sell the Allman Accused

Products to its customers with the knowledge and expectation that the Allman Accused Products, and/or products incorporating the same, will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

285. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Allman Accused Products and/or products incorporating the Allman Accused Products in the United States by marketing the Allman Accused Products in the United States; providing information such as detailed datasheets supporting use of the Allman Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Allman Accused Products; providing technical documentation for the Allman Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development environment software); providing support and training through NXP Community; and by promoting the incorporation of the Allman Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Allman Accused Products, including live training and video.

286. NXP USA has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Allman Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Allman Accused Products, which constitute a material part of the invention of the Allman Patent, knowing the Allman Accused Products to be

especially made or especially adapted for use in infringement of the Allman Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

287. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

288. NXP's infringement of the Allman Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Allman Patent no later than January 9, 2019. As detailed above, Bell Semic sent a letter on January 9, 2019 identifying the TDA18250AHN/C and FXAS21002CQR1 as exemplary of NXP's infringement of the Allman Patent. On September 12, 2019, Bell Semic provided a claim chart to NXP mapping the claims of the Allman Patent to these same products. On February 21, 2020, Bell Semic sent a letter further identifying an additional NXP product as exemplary of NXP's infringement of the Allman Patent. NXP has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products. Despite these efforts, and knowing that it was willfully infringing the Allman Patent, NXP continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Allman Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Allman Patent entitles

Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 10

Willful Infringement of U.S. Patent No. 6,960,836 (Bachman Patent)

289. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

290. The Bachman Patent is generally related to a reinforcing system and method for reinforcing a contact pad of an integrated circuit, where the reinforcing structure is interposed between a top contact pad layer and an underlying metal layer. (*See* Bachman Patent, Abstract.)

291. Bond pads are typically disposed above one or more stacks of brittle and/or soft dielectric materials. During the bonding process, however, mechanical loading and ultrasonic stresses applied by the bonding capillary tip to the bond pad often result in fracture of the underlying dielectrics, deformation of the underlying metal structures, and delamination of the layers in the metal structures. These bonding failures may appear as craters in the bond pad and underlying layers as the bonding capillary tip is pulled away from the bonding pad. However, these defects often are not apparent during bonding but manifest themselves during subsequent bond pull and shear tests, reliability tests, or upon de-processing and cross-sectioning. Further, weakness of the bond pad structure may also reveal itself during wafer probing prior to bonding. Traditionally, bonding failures have been addressed by altering bonding parameters. However, much time is spent experimenting with parameter settings and combinations. Despite the development of general guidelines of parameter set points and configurations, bonding failures persisted at a sufficiently significant level to continually threaten the reliability of integrated circuit devices. Technological advances also did not alleviate the situation, as new and mechanically weaker dielectric materials with lower dielectric constants were being used to

increase circuit speeds, decreasing bond pad dimensions necessitated increased vertical bonding forces, and fear of damage from the use of higher bond parameter settings resulted in longer bond formation time (and thus, lost throughput). The Bachman Patent provided a solution to these issues by teaching a bond pad and reinforcing system that eliminated, or at least substantially reduced, these disadvantages by providing improved structural integrity of bond pads so that forces exerted during bonding to not damage the bond pad and underlying structures.

292. The Bachman Patent contains 1 independent claim and 6 total claims, covering various wire bonding pad reinforcing systems. Claim 1 reads:

> A wire bonding pad reinforcing system for an integrated circuit of the type using brittle inter-level dielectrics comprising:
>
> a wire bonding pad formed of a metal;
>
> a metal reinforcing layer formed under and in contact with the wire bonding pad, the metal reinforcing layer being structured to stiffen the wire bonding pad and to distribute bonding forces over an extended area;
>
> at least one metal layer disposed under and in contact with said reinforcing layer; and
>
> at least one brittle inter-level dielectric extending within the integrated circuit below said at least one metal layer.

293. NXP USA has directly infringed, and continues to directly infringe, one or more claims of the Bachman Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Bachman Patent (*e.g.*, claims 1-6), including, but not limited to:

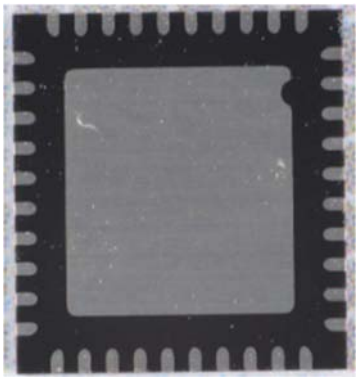
- NXP products that use a bond pad support structure with metal reinforcing layers structured to stiffen the wire bonding pad and distribute bonding forces over an extended area;

- NXP's PN5180A0HN/C3E, an NFC Forum-compliant frontend IC for various contactless communication methods and protocols;
- NXP's 80V18: PN80V, an NFC controller used in mobile phone products like the Apple iPhone X;
- NXP's ASL2500SHNY, a two-phase automotive LED boost driver; and
- NXP's devices that are variants of the above-identified products;

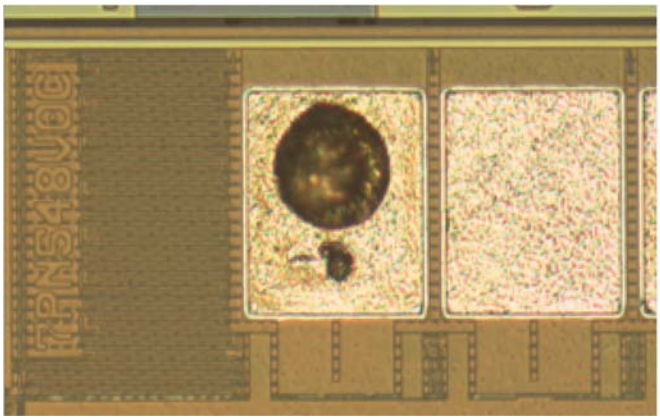
(collectively, the "Bachman Accused Products").

294. By way of non-limiting example only, NXP's PN5180A0HN/C3E infringes claim 1 of the Bachman Patent because it is an integrated circuit that uses brittle inter-level dielectrics and has a wire bonding pad reinforcing system including (1) a wire bonding pad formed of a metal; (2) a metal reinforcing layer formed under and in contact with the wire bonding pad, the metal reinforcing layer being structured to stiffen the wire bonding pad and to distribute bonding forces over an extended area; (3) at least one metal layer disposed under and in contact with the reinforcing layer; and (4) at least one brittle inter-level dielectric extending within the integrated circuit below the at least one metal layer.

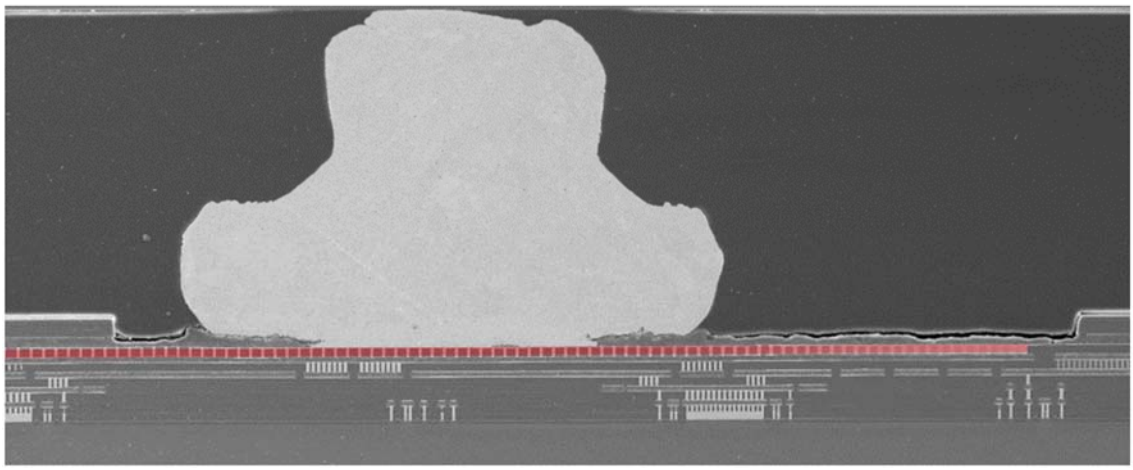
295. As shown below, NXP's PN5180A0HN/C3E is an integrated circuit.

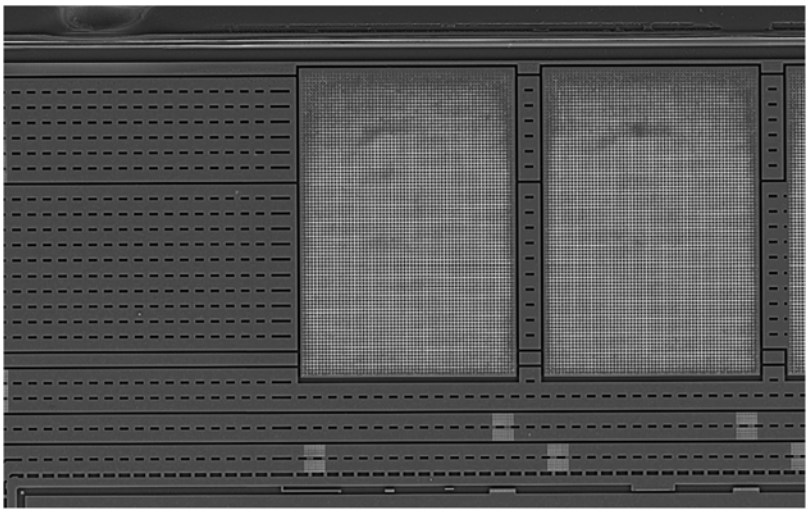


296. NXP's PN5180A0HN/C3E has wire bonding pads formed of a metal.

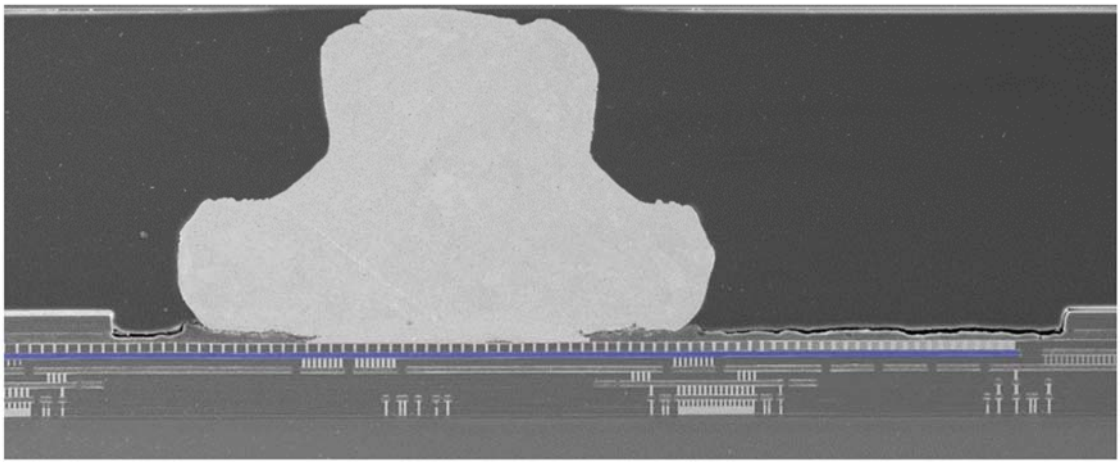


297. NXP's PN5180A0HN/C3E has a metal reinforcing layer (*e.g.*, in red below) formed under and in contact with the wire bonding pad. The metal reinforcing layer is structured to stiffen the wire bonding pad and to distribute bonding forces over an extended area.

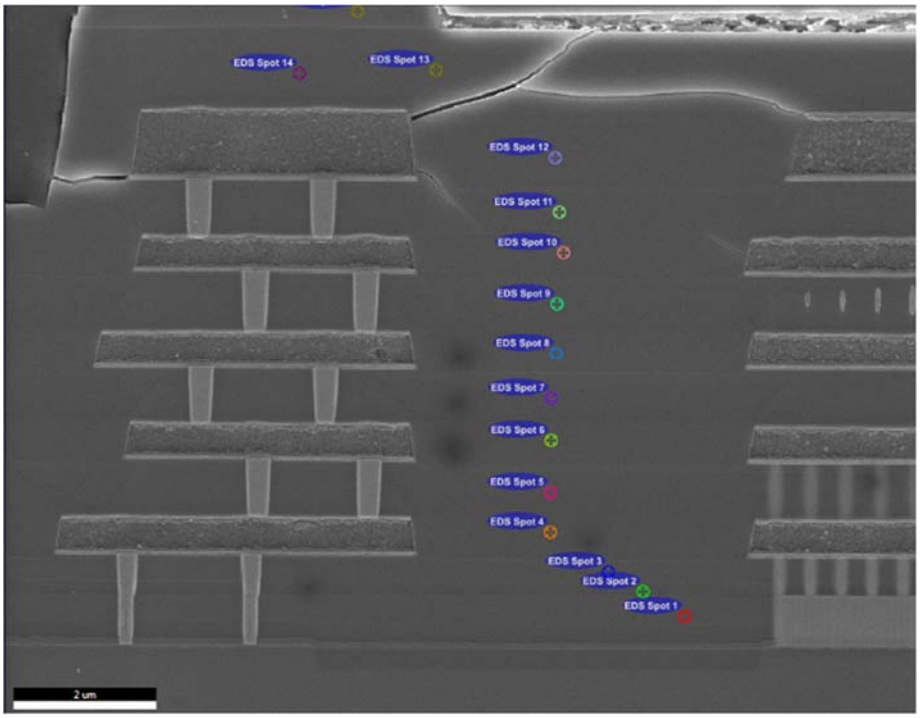


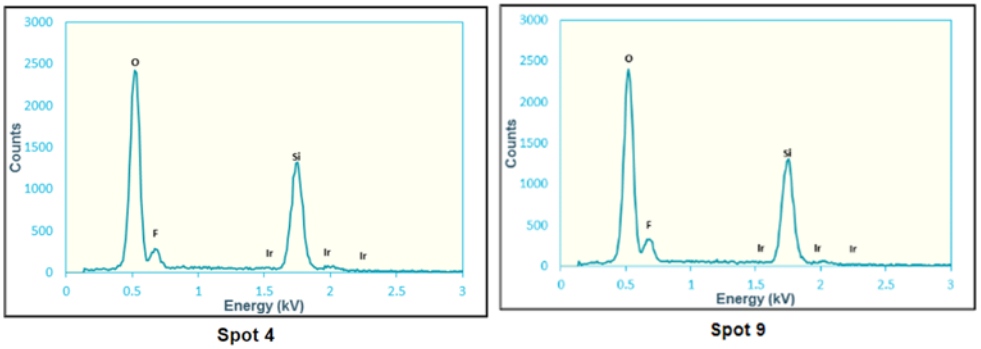


298. NXP's PN5180A0HN/C3E has a metal layer (*e.g.*, in blue below) disposed under and in contact with the reinforcing layer.



299. NXP's PN5180A0HN/C3E has a brittle inter-level dielectric, i.e., a low-k fluorine-doped oxide, extending within the integrated circuit below the metal layer.

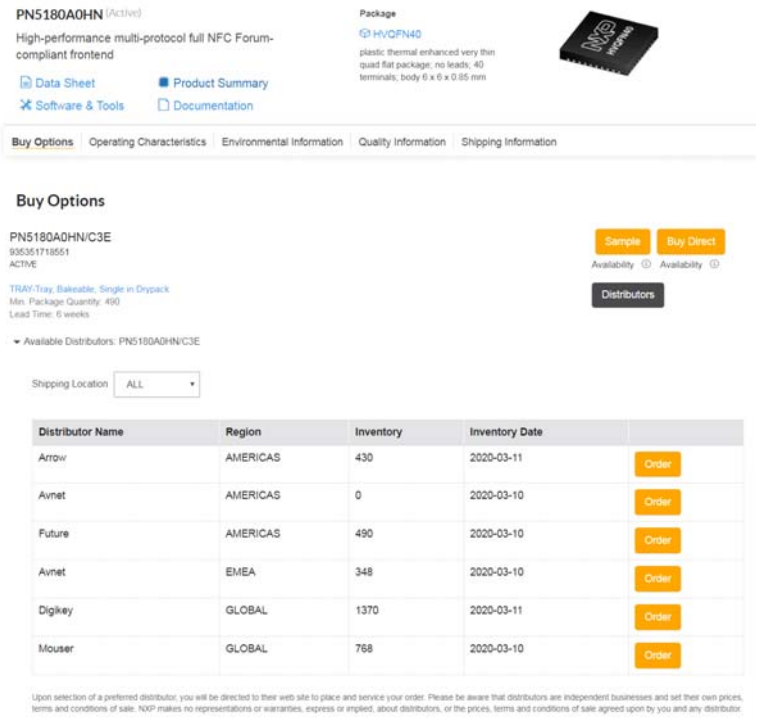




300. Claim 1 of the Bachman Patent applies to each Bachman Accused Product at least because each of those use a same or similar bond pad support structure with metal reinforcing layers structured to stiffen the wire bonding pad and distribute bonding forces over an extended area, like the NXP PN5180A0HN/C3E.

301. On information and belief, each of the Bachman Accused Products have been available for purchase in the United States, including but not limited to, directly from NXP, through NXP's website, and/or through NXP-authorized Americas distributors.

302. By way of example only, the NXP PN5180A0HN/C3E has been available for purchase in the United States, including but not limited to through NXP's website, either directly from NXP or through at least five NXP-authorized Americas and Global distributors:



PN5180A0HN (Active)

High-performance multi-protocol full NFC Forum-compliant frontend

Data Sheet | Product Summary | Software & Tools | Documentation

Package: HVQFN40 — plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

Buy Options | Operating Characteristics | Environmental Information | Quality Information | Shipping Information

Buy Options

PN5180A0HN/C3E
935351718551
ACTIVE

TRAY-Tray, Bakeable, Single in Drypack
Min. Package Quantity: 490
Lead Time: 6 weeks

Sample | Buy Direct
Availability | Availability
Distributors

Available Distributors: PN5180A0HN/C3E

Shipping Location: ALL

Distributor Name	Region	Inventory	Inventory Date	
Arrow	AMERICAS	430	2020-03-11	Order
Avnet	AMERICAS	0	2020-03-10	Order
Future	AMERICAS	490	2020-03-10	Order
Avnet	EMEA	348	2020-03-10	Order
Digikey	GLOBAL	1370	2020-03-11	Order
Mouser	GLOBAL	768	2020-03-10	Order

Upon selection of a preferred distributor, you will be directed to their web site to place and service your order. Please be aware that distributors are independent businesses and set their own prices, terms and conditions of sale. NXP makes no representations or warranties, express or implied, about distributors, or the prices, terms and conditions of sale agreed upon by you and any distributor.

See https://www.nxp.com/part/PN5180A0HN#/ (last visited March 11, 2020).

303. NXP has known of the Bachman Patent and has been on notice of its infringement of the Bachman Patent since at least February 21, 2020, when Bell Semic first identified the NXP PN5180A0HN/C3E, the NXP 80V18:PN80V, and the NXP ASL2500SHNY as exemplary of NXP's infringement of the Bachman Patent. NXP has not responded to this letter.

304. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Bachman Patent at least because Bell Semic provided NXP with written notice of its infringement as detailed above.

305. NXP, knowing its products infringe the Bachman Patent and with specific intent for others to infringe the Bachman Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Bachman Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or

other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Bachman Accused Products, as well as products incorporating the same. NXP knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on NXP's website. NXP actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Bachman Accused Products in the United States. NXP knows, and has known since at least February 21, 2020, that the Bachman Accused Products infringe the Bachman Patent, and purposefully and knowingly sells and offers to sell the Bachman Accused Products to its customers with the knowledge and expectation that the Bachman Accused Products, and/or products incorporating the same, will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

306. NXP further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Bachman Accused Products and/or products incorporating the Bachman Accused Products in the United States by marketing the Bachman Accused Products in the United States; providing information such as detailed datasheets supporting use of the Bachman Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Bachman Accused Products; providing technical documentation for the Bachman Accused Products including application notes, user guides, and reference manuals describing how to implement, optimize, and test applications; providing design and development tools (such as integrated development

environment software); providing support and training through NXP Community; and by promoting the incorporation of the Bachman Accused Products into end-user products by providing for its customers reference designs; commercial support and engineering services; hardware, software, and development tools; and robust customer support. In addition to these resources, NXP also provides numerous support resources for the customers of its Bachman Accused Products, including live training and video.

307. NXP USA has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Bachman Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Bachman Accused Products, which constitute a material part of the invention of the Bachman Patent, knowing the Bachman Accused Products to be especially made or especially adapted for use in infringement of the Bachman Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

308. Bell Semic has sustained and is entitled to recover damages as a result of NXP's past and continuing infringement, in an amount adequate to compensate for NXP's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

309. NXP's infringement of the Bachman Patent is and has been knowing, deliberate, and willful. NXP learned of its infringement of the Bachman Patent no later than February 21, 2020. As detailed above, Bell Semic sent a letter on February 21, 2020, identifying 3 NXP products as exemplary of NXP's infringement of the Bachman Patent. NXP has not responded to this letter. Despite these efforts, and knowing that it was willfully infringing the Bachman Patent, NXP continued and continues to commit acts of direct and indirect infringement despite

knowing its actions constitute infringement of the valid and enforceable Bachman Patent, despite a risk of infringement that was known or so obvious that it should have been known to NXP, and/or even though NXP otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, NXP's conduct is and has been egregious. NXP's knowing, deliberate, and willful infringement of the Bachman Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Bell Semic prays for the following relief:

A. A judgment that NXP has infringed one or more claims of each Asserted Patent;

B. An award of damages resulting from NXP's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order requiring NXP to provide accountings and to pay supplemental damages to Bell Semic, including, without limitation, additional damages for any infringing sales not presented at trial, and prejudgment and post-judgment interest;

D. A judgment and order finding that NXP's acts of infringement were willful and egregious and trebling damages under 35 U.S.C. § 284;

E. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Bell Semic its reasonable attorneys' fees against NXP.

F. A permanent injunction enjoining NXP and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in active concert or participation with NXP, from infringing the Hall 340, Hall 269, Kang, Lin, Ma, Allman, and Bachman Patents;

G. If a permanent injunction preventing further infringement of the Hall 340, Hall 269, Kang, Lin, Ma, Allman, and Bachman Patents is not granted, a compulsory ongoing licensing fee for any such further infringement; and

H. Any and all other relief to which Plaintiff may show itself to be entitled.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Dated: March 23, 2020

/s/ *Paul J. Skiermont*
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Steven W. Hartsell (TX Bar No. 24040199)
(*pro hac vice* to be filed)
Jaime K. Olin (TX Bar No. 24070363)
(*pro hac vice* to be filed)
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