IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

BELL SEMICONDUCTOR, LLC, Plaintiff, v. INTEGRATED DEVICE TECHNOLOGY, INC. Defendant.	Civil Action No. 19-cv-2155-LPS **JURY TRIAL DEMANDED**

BELL SEMICONDUCTOR, LLC'S
FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Bell Semiconductor, LLC ("Bell Semic") as and for its complaint against Integrated Device Technology, Inc. ("IDT" or "Defendant") alleges as follows:

INTRODUCTION

1. Bell Semic is a technology and intellectual property licensing company. Bell Semic's patent portfolio comprises over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world's leading semiconductor technology innovators, including AT&T Bell Laboratories, Lucent Technologies (Lucent), Agere Systems (Agere), LSI Logic and LSI Corporation (LSI). The portfolio reflects expertise developed at the various R&D laboratories and manufacturing locations of these companies around the world. The technology created, developed, and patented at those companies underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors and wireless connectors.

2. Bell Semic was formed in 2017 to manage this portfolio of semiconductor-related intellectual property acquired from Broadcom and assigned to Bell Semic. Several Bell Semic executives previously served as engineers and in leadership roles within the intellectual property departments of Lucent, Agere, LSI, Avago Technologies (Avago), and Broadcom. As a result, Bell Semic executives were personally involved in creating, patenting, and licensing various aspects of the portfolio even before Broadcom assigned it to Bell Semic, including:

- Bell Semic's Chief Executive Officer and Board Member, Mr. John Veschi, served as General Manager of the Intellectual Property business at LSI, had similar responsibilities at Agere, and began his in-house intellectual property experience with the formation of Lucent.
- Bell Semic's President and General Counsel, Mr. Chad Hilyard, served as Managing IP Counsel and in other roles at LSI and Agere, where he was involved in licensing many of the patents in the portfolio now assigned to Bell Semic;
- Bell Semic's Chief Technology Officer, Dr. Sailesh Merchant was a Fellow at Broadcom, Avago, and LSI Corporation; a Distinguished Engineer at LSI Corporation; and a Distinguished Member of the Technical Staff of Agere and Lucent. Dr. Merchant is also a Senior Member of the IEEE and an inventor on more than 250 worldwide patents—including many of the patents in Bell Semic's portfolio—and three of the patents asserted in this Complaint;
- Bell Semic's Senior Director for IP, Mr. Kouros Azimi, served as a Member of the Technical Staff at AT&T Bell Labs, Lucent, and Agere; Director of Intellectual Property at Avago/Broadcom, and a Patent Engineer and Director of Patent Development at LSI/Avago Technologies.

3. IDT has infringed and continues to infringe Bell Semic's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. IDT's customers incorporate those products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States and within this District. Such downstream products include, but are not limited to, clock and clock timing solutions including RapidIO devices; memory, memory interface, and logic devices; high-performance interface and connectivity solutions; power management devices; RF and microwave devices; sensors; and wireless power receivers and transmitters.

4. Bell Semic has notified IDT of its infringement in writing more than once—but IDT did not respond or acknowledge Bell Semic or its intellectual property before Bell Semic filed its Original Complaint in this Action. Instead, IDT continued to infringe, and thus its infringement is and has been willful under the Patent Act.

NATURE OF THE CASE

5. This action arises under 35 U.S.C. § 271 for IDT's infringement of Bell Semic's United States Patent Nos. 8,049,340 (Hall 340); 8,288,269 (Hall 269); 7,319,272 (Ramakrishnan); and 6,624,007 (Kobayakawa) (collectively, Bell Semic's "Asserted Patents").

PARTIES

6. Bell Semiconductor, LLC is a Delaware limited liability company with a principal place of business of One West Broad Street, Suite 901, Bethlehem, PA 18018.

7. On information and belief, Defendant Integrated Device Technology, Inc. ("IDT") is a corporation organized under the laws of the State of Delaware, headquartered at 6024 Silver Creek Valley Road, San Jose, CA 95138. IDT may be served through its registered agent, The

Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801.

JURISDICTION AND VENUE

8. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has specific and general jurisdiction over Defendant pursuant to due process and/or the Delaware Long Arm Statute, due to Defendant having availed itself of the rights and benefits of Delaware by incorporating under Delaware law and due to its substantial business in this forum, including: (i) at least a portion of the infringement alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to individuals in Delaware and in this Judicial District.

10. Venue is proper in this District under 28 U.S.C. §§ 1391(b)-(c) and 1400(b) because Defendant is resident in this District as it is incorporated in Delaware.

11. IDT has committed acts of infringement in this District giving rise to this action and does business in this District, including making sales and/or providing service and support for its respective customers in this District. IDT purposefully and voluntarily sold one or more of its infringing products with the expectation that they, or products incorporating the infringing products, would be purchased by consumers in this District. These infringing products have been and continue to be purchased by consumers in this District. IDT has committed acts of patent infringement within the United States, the State of Delaware, and the District of Delaware.

BELL SEMIC'S ASSERTED PATENTS

1) Overview of U.S. Patent No. 8,049,340 (Hall et al.)

12. Bell Semic is the owner by assignment of U.S. Patent No. 8,049,340 (the "Hall 340 Patent"), owns all right, title, and interest in the Hall 340 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 340 Patent is entitled "Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package." A true and correct copy of the Hall 340 Patent is attached as **Exhibit 1**.

13. The inventors of the Hall 340 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

14. The application for the Hall 340 Patent was filed on March 22, 2006, and it issued on November 1, 2011.

15. As of March 2020, the Hall 340 Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 2 patents and published applications filed by leading technology companies Alcatel Lucent and Intel.

2) Overview of U.S. Patent No. 8,288,269 (Hall et al.)

16. Bell Semic is the owner by assignment of U.S. Patent No. 8,288,269 (the "Hall 269 Patent"), owns all right, title, and interest in the Hall 269 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 269 Patent is entitled "Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package." The Hall 269 Patent issued on October 16, 2012. A true and correct copy of the Hall 269 Patent is attached as **Exhibit 2**.

17. The inventors of the Hall 269 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

18. The application for the Hall 269 Patent was filed on October 4, 2011, and claims priority to the application leading to the Hall 340 Patent, which was filed on March 22, 2006. The Hall 269 Patent issued as a patent on October 16, 2012

3) Overview of U.S. Patent No. 7,319,272 (Ramakrishnan et al.)

19. Bell Semic is the owner by assignment of U.S. Patent No. 7,319,272 (the "Ramakrishnan Patent"), owns all right, title, and interest in the Ramakrishnan Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Ramakrishnan Patent is entitled "Ball Assignment System." A true and correct copy of the Ramakrishnan Patent is attached as **Exhibit 3**.

20. The inventors of the Ramakrishnan Patent are Arun Ramakrishnan, Farshad Ghahghahi, Aritharan Thurairajaratnam, and Leah M. Miller.

21. The application for the Ramakrishnan Patent was filed on April 1, 2005, and it issued as a patent on January 15, 2008.

4) Overview of U.S. Patent No. 6,624,007 (Kobayakawa et al.)

22. Bell Semic is the owner by assignment of U.S. Patent No. 6,624,007 (the "Kobayakawa Patent"), owns all right, title, and interest in the Kobayakawa Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Kobayakawa Patent is entitled "Method of Making Leadframe by Mechanical Processing." A true and correct copy of the Kobayakawa Patent is attached as **Exhibit 4**.

23. The inventors of the Kobayakawa Patent are Masahiko Kobayakawa and Masahide Maeda.

24. The application for the Kobayakawa Patent was filed on July 25, 2002, and it issued as a patent on September 23, 2003.

25. As of March 2020, the Kobayakawa Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 7 patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Nichia, Infineon, and Texas Instruments.

FACTUAL BACKGROUND

26. Bell Semic incorporates the preceding paragraphs as if fully set forth herein.

27. On June 1, 2002, Lucent, having its roots with Bell Laboratories and AT&T Corporation, spun off its microelectronics business as Agere. Agere later merged with LSI Logic forming LSI Corporation in 2007, which was in turn acquired by Avago in 2014. In 2016, Avago purchased Broadcom and assumed its name to become the current Broadcom Inc. In 2017, Broadcom assigned a patent portfolio containing over 1,900 worldwide patents and applications, approximately 1,500 of which are active U.S. patents, to Bell Semic that included patents originally assigned or issued to Bell Labs, Lucent, Agere, LSI Logic, and LSI.

28. Portions of the Bell Semic portfolio are presently licensed and/or were previously licensed to leading technology companies by Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*See supra* ¶ 2.) Portions of the Bell Semic portfolio were also invented and co-invented by other Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*Id*.)

29. Bell Semic's Asserted Patents arise out of the research, conception, creation, and design of innovative technology developed by leading high-technology companies, including LSI Logic, Agere, and LSI Corporation. Prior to their ultimate acquisition by Avago (now Broadcom), those companies were pioneers of innovative semiconductor technology—and made substantial investments into researching, inventing, creating, and manufacturing cutting-edge

semiconductor technology. Bell Semic's Asserted Patents are directed to this inventive technology relating to semiconductors, integrated circuits and related products.

30. IDT infringes and has infringed by selling, offering to sell, using, and/or importing products (including importing products made by a patented process) throughout the United States. Moreover, IDT works closely with its customers, foundry suppliers, distributors, OEMs, or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and related products. IDT directs and controls the manufacture and design of its products to be integrated into downstream products for its customers. In addition, IDT's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States by itself and others further include, without limitation, any one or a combination of: (i) designing specifications for manufacture of IDT's products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of IDT's products; (iii) soliciting and/or sourcing the manufacture of IDT's products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of their products; (v) enabling and encouraging the use, sale, or importation of their products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

31. IDT provides marketing and/or technical support services for its products from its facilities in the United States. For example, IDT maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for their products. (*See, e.g.*, https://www.idt.com/us/en.) IDT's publicly-available website also contains user manuals, product documentation, and other materials related to its products. (*Id.*) For example, IDT's website supports incorporation of its products into end-user products

through partner programs, including the IDT Partner Program, which is a "network of third party companies that offer unique capabilities and services that complement and extend IDT's products and services to serve our joint customers." (*See* https://www.idt.com/us/en/support/partners).

32. In addition to these resources, IDT also provides numerous support resources for the customers of its semiconductor devices, including documentation and tools for its products, including white papers, brochures, datasheets, and manuals (https://www.idt.com/us/en/support/document-search); complimentary design review services (https://www.idt.com/us/en/support/clock-tree-design-service); automated utilities, calculators, and reference designs (*see, e.g.*, https://www.idt.com/us/en/jitter-measurement-utility; https://www.idt.com/us/en/support/calculators; https://www.idt.com/us/en/support/reference-designs); and blog posts further explaining IDT products (https://www.idt.com/us/en/blogs).

IDT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT FROM BELL SEMIC

33. Before filing this lawsuit, Bell Semic notified IDT that Broadcom has assigned to Bell Semic a large portfolio of semiconductor patents, identified IDT products that infringe Bell Semic's Asserted Patents, further identified exemplary products from those Technology Nodes that infringe the Asserted Patents, and offered to license those patents to IDT.

34. Specifically, on March 15, 2019, Mr. Hilyard, sent a letter via email to Dr. Sailesh Chittipeddi (IDT's Executive VP, Global Operations and Chief Technology Officer) to inform IDT that Bell Semic "acquired all of the semiconductor-related patent assets previously owned by Agere Systems Inc. and LSI Corporation. As you may know, this portfolio includes patents originally assigned to Bell Labs and Lucent Technologies, as well as those assigned to Agere, LSI[,] and Avago Corporation . . . the portfolio reflects expertise and inventions developed at

various R&D labs and manufacturing facilities associated with these companies around the world . . . The patent portfolio comprises approximately 1,900 active worldwide patents and applications – approximately 1,500 of which are active US patents. . . . By way of background, I was previously part of the Agere/LSI licensing team . . . and am joined by other former members Lucent/Agere/LSI licensing teams whom you know, including John Veschi and Sailesh Merchant. As you can appreciate, we are very familiar with this pioneering patent portfolio and have licensed this portfolio to many of the world's leading semiconductor companies. Our goal is to build upon the amicable licensing history between AT&T/Lucent/Agere/LSI and IDT – as well as the similar relationships we previously established throughout the semiconductor industry." . . . [w]e have been acquiring IDT products and conducting reverse engineering to establish IDT's use of exemplary patents in the portfolio. Our preliminary analysis reveals that IDT is currently making, using, selling, or offering for sale products that infringe one or more of Bell Semic's patents."

35. Bell Semic's March 15, 2019 letter also identified specific Bell Semic patents that IDT infringes—and identified exemplary IDT products infringing Bell Semic's patents: "Over the last few months, we have been acquiring IDT products and conducting reverse engineering to establish IDT's use of exemplary patents in the portfolio. Our preliminary analysis reveals that IDT is currently making, using, selling, or offering for sale products that infringe one or more of Bell Semic's patents. The table below is an exemplary list of IDT products that infringe one or more claims of at least the listed patents. Please keep in mind that the patents below are exemplary, and IDT products most likely infringe other patents in the larger portfolio."

36. The table to Bell Semic's March 15, 2019 letter put IDT on notice of Bell Semic's patents and IDT's exemplary infringing products of those patent, including the Hall 340 and Hall 269 Asserted Patents as follows:

Exemplary List of Bell Semic's Patents Infringed by IDT

U.S. Patent	Title	IDT Product Codes
US 6,140,710 *Greenberg*	Power and Ground and Signal Layout for Higher Density Integrated Circuit Connections with Flip-Chip Bonding	IDT89H64H16AG2ZCBLGI
		IDT80HCPS1432CHMI
US 8,049,340 *Hall et. al.*	Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package	IDT80HCPS1432CHMI
US 8,288,269 *Hall et. al.*	Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package	IDT80HCPS1432CHMI

37. Bell Semic's March 15, 2019 letter reminded IDT of its responsibilities under the Patent Act and also invited IDT to engage in a dialogue and offered to answer any IDT questions, and offered to meet on a date, time, and location of IDT's choosing—all in an effort to attempt to reach a license agreement: "We would like to propose having a near-term dialogue with IDT with the goal of providing more details about our licensing program and the patent portfolio (including providing specific claim charts), answering any questions you may have, and reaching an agreement on a path forward to put in place a new license agreement covering this semiconductor patent portfolio. To that end, please propose some dates and times when your team is available for a meeting. We are happy to meet with you at a location of your choice . . . If you would like to have a brief call regarding logistics or about any other matter, please feel free to contact me directly at the number listed above. I look forward to your reply and thank you in advance for your prompt attention to these matters."

38. IDT did not respond to Bell Semic's March 15, 2019 Notice Letter.

39. On April 23, 2019, Bell Semic's Mr. Hilyard again emailed IDT's Executive VP, Global Operations and Chief Technology Officer, and copied IDT's President and Chief

Executive Officer to follow-up on Bell Semic's March 15, 2019 letter, and invited IDT to discuss the subject matter of the March 15, 2019 letter.

40. IDT did not respond to Bell Semic's April 23, 2019 Notice Letter.

41. Despite Bell Semic's continuous and repeated efforts since March 15, 2019 and prior to Bell Semic filing its Original Complaint, IDT had completely ignored Bell Semic and had refused to engage in any meaningful discussions to end their infringement of Bell Semic's Asserted Patents with a license. Bell Semic was thus left with no other choice but to seek relief from this Court by filing its Original Complaint in this matter.

42. Since Bell Semic filed its Original Complaint, IDT contacted and met with Bell Semic in December 2019 to discuss its infringement of the Asserted Patents. However, meaningful discussions have not progressed, and instead, IDT continues to knowingly and willfully infringe Bell Semic's Asserted Patents directly, contributorily, and by inducement—to obtain the substantial benefits of those inventions without a license from Bell Semic.

43. More recently, on March 26, 2020, Mr. Veschi wrote to IDT identifying exemplary IDT products infringing the Kobayakawa Patent. Among others, this correspondence identified the IDT 5P49V60 as exemplary of infringing the Kobayakawa Patent.

COUNT 1

Willful Infringement of U.S. Patent No. 8,049,340 (Hall 340 Patent)

44. Plaintiff re-alleges and incorporates by reference the allegations in paragraphs 1-15 and 26-43 as if fully set forth herein.

45. The Hall 340 Patent is generally related to an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for

making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board. (*See* Hall 340 Patent, Abstract.)

46. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the IDT 80HCPS1432CHMHI described below includes 576 ball counts) while packages decrease in size. In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 340 Patent teaches the use of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

47. The Hall 340 Patent contains 3 independent claims and 19 total claims, covering various integrated circuit package substrates. Claim 12 reads:

> An integrated circuit package substrate, comprising:
>
> a first layer comprising a plurality of rows of electrical contacts;
>
> a plurality of electrically conductive layers disposed immediately proximate the first layer;
>
> a plurality of dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other, and
>
> a plurality of rows of cutouts formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first

layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers.

48. IDT has directly infringed, and continues to directly infringe, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Hall 340 Patent (*e.g.*, claims 1, 4, 5, 12-13, and 19),[1] including, but not limited to:

- IDT products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts, including IDT RapidIO devices;
- IDT's 80HCPS1432CHMHI, a RapidIO compliant central packet switch intended for intensive processing applications which require a multiplicity of DSPs, CPUs, and/or FPGAs working together in a cluster; and
- IDT's devices that are variants of the above-identified products; (collectively, the "Hall 340 Accused Products").

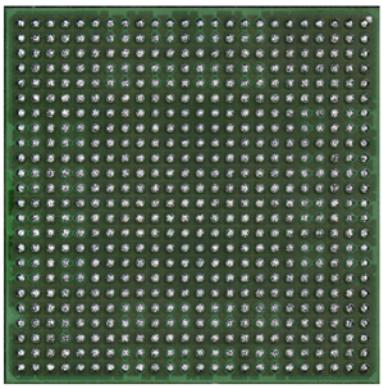
49. By way of non-limiting example only, the IDT 80HCPS1432CHMHI infringes claim 12 of the Hall 340 Patent because it is an integrated circuit that has an integrated circuit package substrate with (1) a first layer that has two or more rows of electrical contacts; (2) two or more electrically conductive layers disposed immediately proximate the first layer; (3) two or more dieletric layers separating, respectively, the electrically conductive layers and the first layer

[1] Throughout this First Amended Complaint, wherever Bell Semic identifies specific claims of the Asserted Patents that IDT infringes, Bell Semic expressly reserves the right to identify additional asserted claims and products in its infringement contentions in accordance with the local rules, the Court's Revised Procedures for Managing Patent Cases, and the Case Management Order. Specifically identified claims throughout this First Amended Complaint are provided for notice pleading only and are not presented as "exemplary" claims of all other claims for any Asserted Patent.

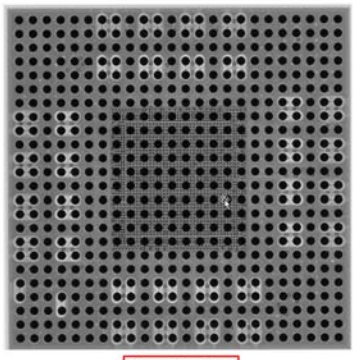
from each other; and (4) two or more rows of cutouts formed in each of the two or more electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the two or more electrically conductive layers.

50. As shown below, the IDT 80HCPS1432CHMHI is an integrated circuit with an integrated circuit package substrate:

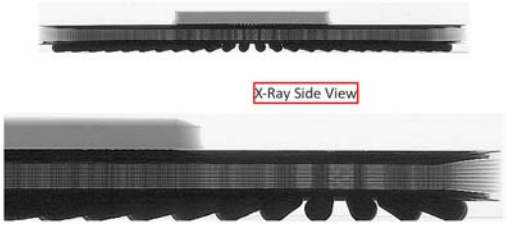
Component – Top View



Component – Bottom View/BGA

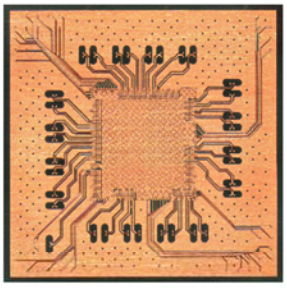


X-Ray – Top View

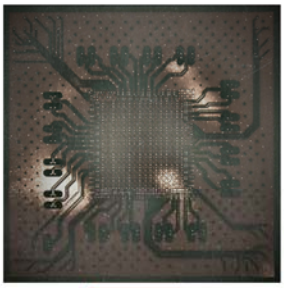


X-Ray Side View

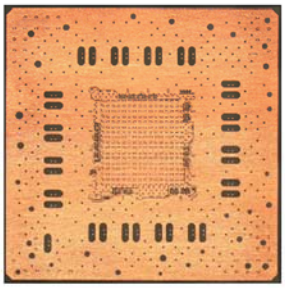
51. The integrated circuit package substrate of the IDT 80HCPS1432CHMHI has 8 metal layers and 7 via layers:



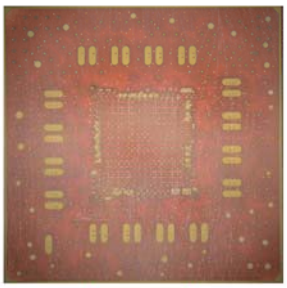
Metal Layer 1



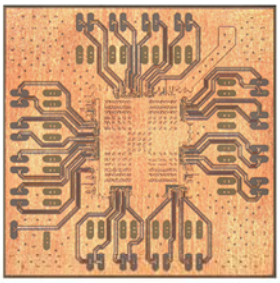
Via Layer 1



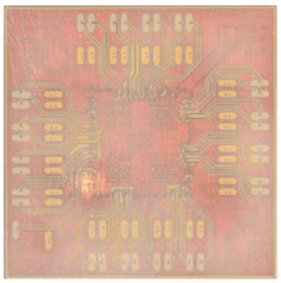
Metal Layer 2



Via Layer 2



Metal Layer 3



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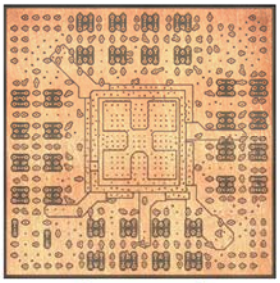
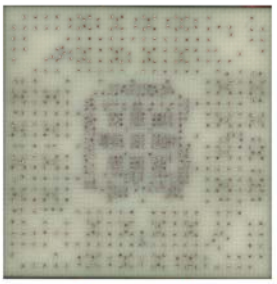
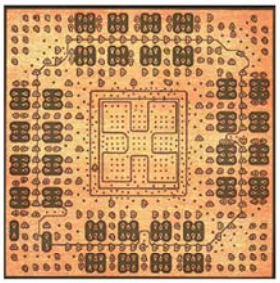


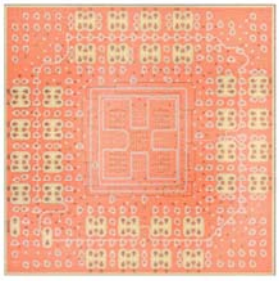
Metal Layer 4



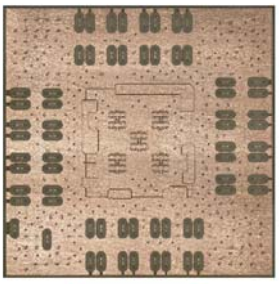
Via Layer 4



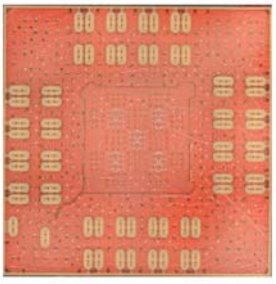
Metal Layer 5



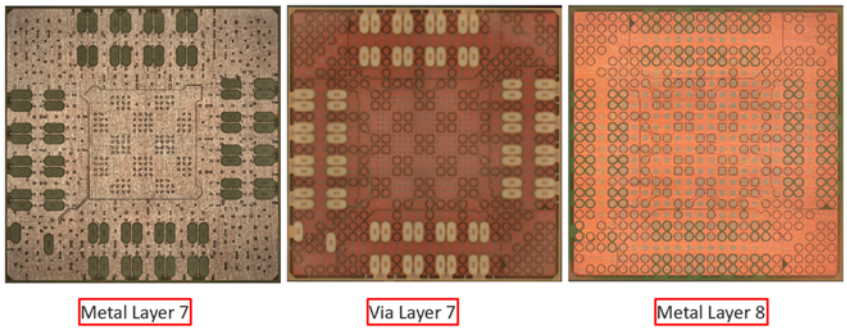
Via Layer 5



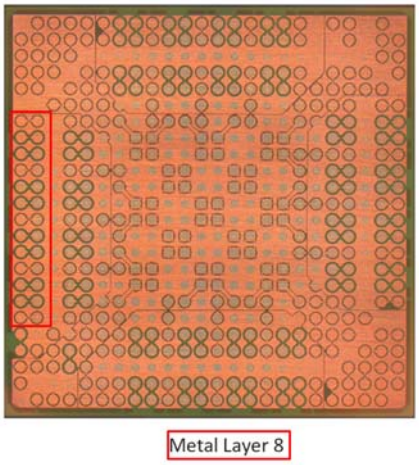
Metal Layer 6



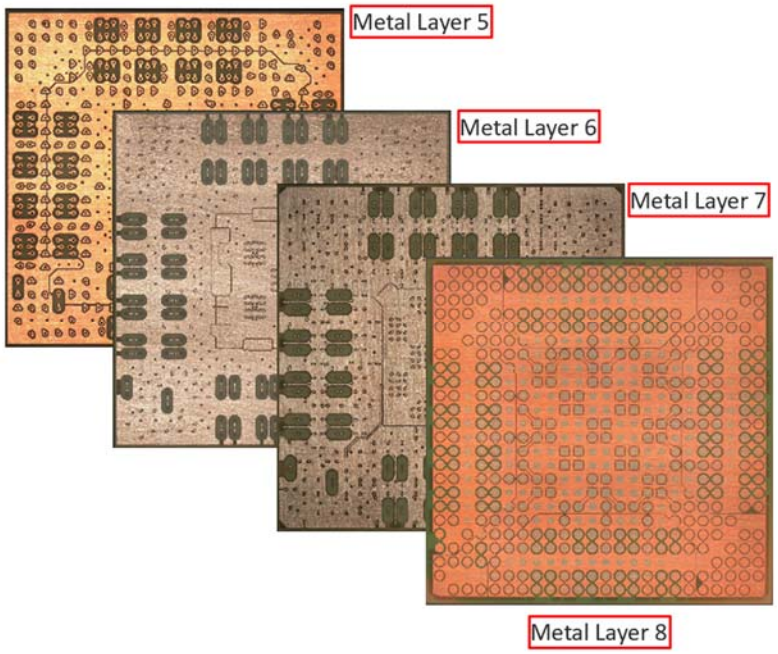
Via Layer 6



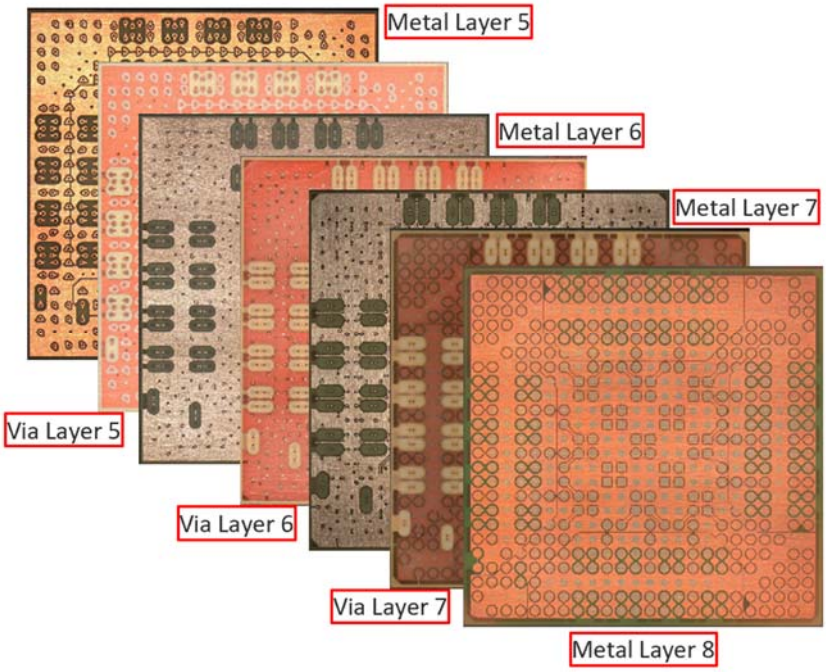
52. The first layer (metal layer 8) of the IDT 80HCPS1432CHMHI has a plurality of rows of electrical contacts and forms the ball grid array layer with solder balls, removed for clarity (for example, as indicated in red below):



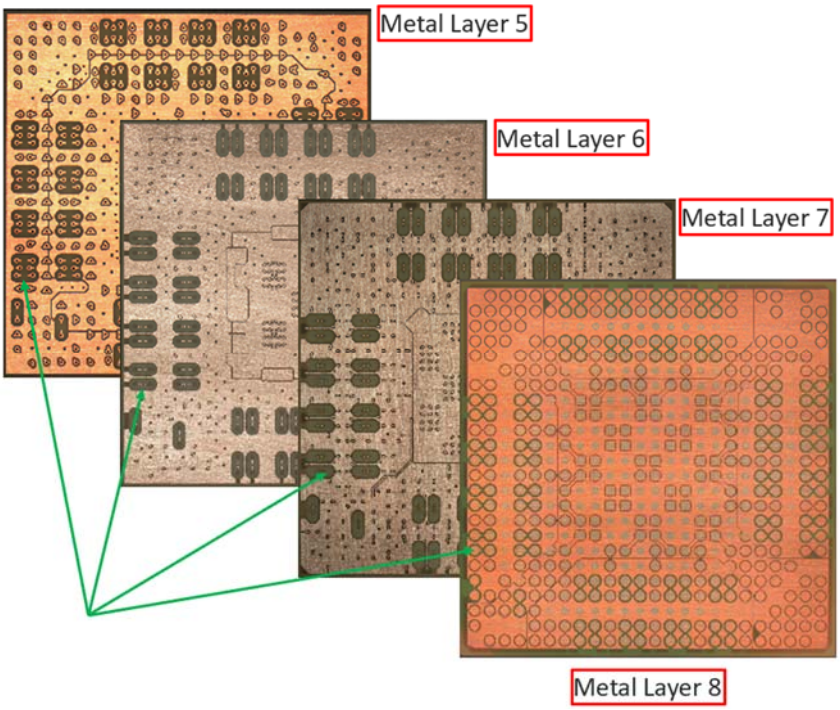
53. The IDT 80HCPS1432CHMHI also has a plurality of electrically conductive layers (for example, metal layers 5, 6, and 7) disposed immediately proximate the first layer (metal layer 8):



54. The IDT 80HCPS1432CHMHI further has a plurality of dieletric layers (for example, via layers 5, 6, and 7) separating, respectively, the electrically conductive layers (metal layers 5, 6, and 7) and the first layer (metal 8) from each other:



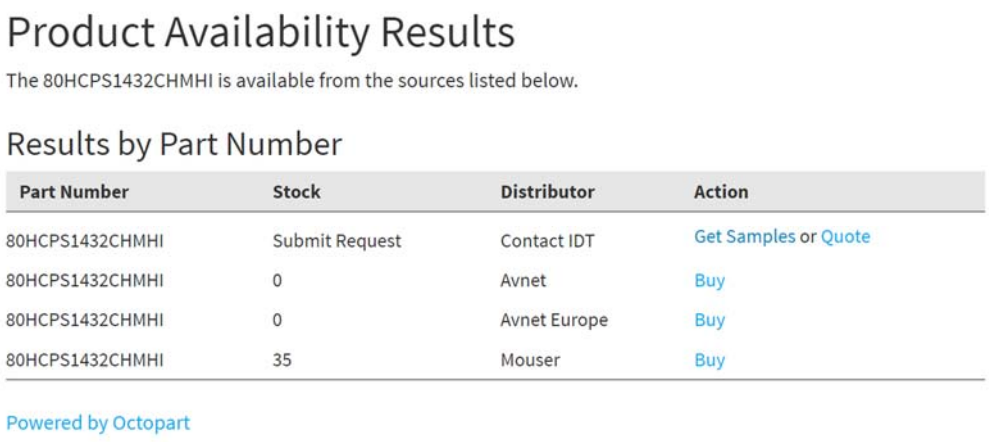
55. The IDT 80HCPS1432CHMHI further has a plurality of rows of cutouts formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers (for example, as indicated by the green arrows below):



56. Claim 12 of the Hall 340 Patent applies to each Hall 340 Accused Product at least because each of those products contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts as the IDT 80HCPS1432CHMHI.

57. On information and belief, each of the Hall 340 Accused Products have been available for purchase in the United States, including but not limited to, directly from IDT, through IDT's website, and/or through IDT-authorized Americas distributors.

58. By way of example only, on information and belief, the IDT 80HCPS1432CHMHI and other IDT RapidIO devices have been available for purchase in the United States, including but not limited to through IDT's website, either directly from IDT or through IDT-authorized distributors:



Product Availability Results

The 80HCPS1432CHMHI is available from the sources listed below.

Results by Part Number

Part Number	Stock	Distributor	Action
80HCPS1432CHMHI	Submit Request	Contact IDT	Get Samples or Quote
80HCPS1432CHMHI	0	Avnet	Buy
80HCPS1432CHMHI	0	Avnet Europe	Buy
80HCPS1432CHMHI	35	Mouser	Buy

Powered by Octopart

See https://www.idt.com/buy-sample/check-inventory/result?show_price=1&partno=80HCPS1432CHMHI&exact=1 (last visited March 3, 2020).

59. IDT has known of the Hall 340 Patent and has been on notice of its infringement since at least March 15, 2019, when Bell Semic first identified the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement of the Hall 340 Patent. After IDT did not respond, on April 23, 2019 Bell Semic again sent an email to IDT identifying the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement. IDT did not respond to these emails before Bell Semic filed its Original Complaint.

60. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 340 Patent at least because Bell Semic provided IDT with written notice of its infringement as detailed above.

61. IDT, knowing its products infringe the Hall 340 Patent and with specific intent for others to infringe the Hall 340 Patent, has induced infringement of, and continue to induce

infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Hall 340 Accused Products, as well as products containing the same. IDT knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on IDT's website. IDT actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Hall 340 Accused Products in the United States. IDT knows, and has known since at least March 15, 2019, that the Hall 340 Accused Products infringe the Hall 340 Patent, and purposefully and knowingly sells and offers to sell the Hall 340 Accused Products to its customers with the knowledge and expectation that the Hall 340 Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

62. IDT further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 340 Accused Products and/or products incorporating the Hall 340 Accused Products in the United States by marketing the Hall 340 Accused Products in the United States; providing information such as detailed datasheets supporting use of the Hall 340 Patent Accused Products that promote their features, specifications, and applications; promoting the incorporation of the Hall 340 Patent Accused Products into end-user products through partner programs, including the IDT Partner Program

(*see, e.g.*, https://www.idt.com/us/en/support/partners). IDT further encourages the use of its infringing products by providing for its customers, by way of example only, (1) documentation and tools for its products, including white papers, brochures, datasheets, and manuals (https://www.idt.com/us/en/support/document-search); (2) complimentary design review services (https://www.idt.com/us/en/support/clock-tree-design-service); (3) automated utilities, calculators, and reference designs (*see, e.g.*, https://www.idt.com/us/en/jitter-measurement-utility; https://www.idt.com/us/en/support/calculators; https://www.idt.com/us/en/support/reference-designs); and (4) blog posts further explaining IDT products (https://www.idt.com/us/en/blogs).

63. IDT has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Hall 340 Accused Products, which constitute a material part of the invention of the Hall 340 Patent, knowing the Hall 340 Accused Products to be especially made or especially adapted for use in infringement of the Hall 340 Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

64. Bell Semic has sustained and is entitled to recover damages as a result of IDT's past and continuing infringement, in an amount adequate to compensate for IDT's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

65. IDT's infringement of the Hall 340 Patent is and has been knowing, deliberate, and willful. IDT learned of its infringement of the Hall 340 Patent no later than March 15, 2019. As detailed above, Bell Semic sent an email to IDT on March 15, 2019 and April 23, 2019 with

an attached letter, identifying the Hall 340 Patent as being infringed by IDT's exemplary 80HCPS1432CHMHI product. IDT did not respond to either of these emails before Bell Semic filed its Original Complaint. Despite these efforts, and knowing that it was willfully infringing the Hall 340 Patent, IDT continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Hall 340 Patent, despite a risk of infringement that was known or so obvious that it should have been known to IDT, and/or even though IDT otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, IDT's conduct is and has been egregious. IDT's knowing, deliberate, and willful infringement of the Hall 340 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 2

Willful Infringement of U.S. Patent No. 8,288,269 (Hall 269 Patent)

66. Plaintiff re-alleges and incorporates by reference the allegations in paragraphs 1-11, 16-18, and 26-43 as if fully set forth herein.

67. The Hall 269 Patent is generally related to methods for avoiding parasitic capacitance in an integrated circuit package, such as an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the

additional electrically conductive layer and the printed circuit board. (*See* Hall 269 Patent, Abstract.)

68. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the IDT 80HCPS1432CHMHI described below includes 576 ball counts) while packages decrease in size. In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 269 Patent teaches the formation of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

69. The Hall 269 Patent contains 2 independent claims and 20 total claims, covering various methods. Claim 1 reads:

> A method, comprising steps of:
>
> forming a first electrically conductive layer including a plurality of rows of contact pads;
>
> forming an electrically insulating layer on the first electrically conductive layer; and
>
> forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

70. IDT has directly infringed, and continues to directly infringe, one or more claims of the Hall 269 Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. §

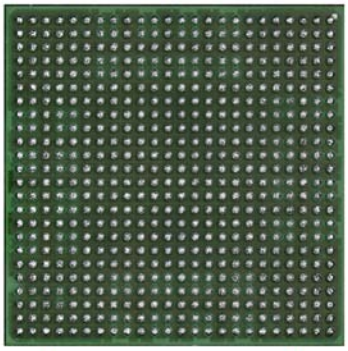
271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Hall 269 Patent (*e.g.*, claims 1, 4, 7, and 10-13). Such products manufactured using these infringing methods include, but are not limited to:

- IDT products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts, including IDT RapidIO devices;
- IDT's 80HCPS1432CHMHI, a RapidIO compliant central packet switch intended for intensive processing applications which require a multiplicity of DSPs, CPUs, and/or FPGAs working together in a cluster; and
- IDT's devices that are variants of the above-identified products; (collectively, the "Hall 269 Accused Products").

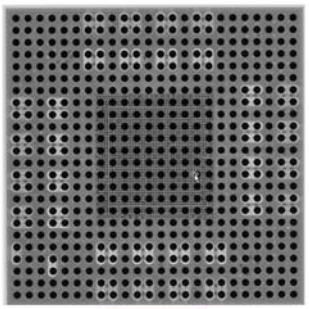
71. By way of non-limiting example only, the process of manufacturing the IDT 80HCPS1432CHMHI meets all of the steps of claim 1 of the Hall 269 Patent including (1) forming a first electrically conductive layer including two or more rows of contact pads; (2) forming an electrically insulating layer on the first electrically conductive layer; and (3) forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and two or more cutouts where each cutout encloses an electrically insulating area within the second electrically conductive layer and where each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

72. As shown below, the IDT 80HCPS1432CHMHI is an integrated circuit with an integrated circuit package substrate:

Component – Top View



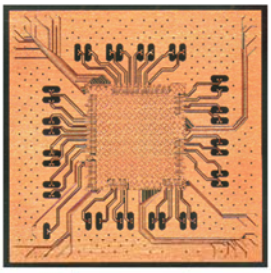
Component – Bottom View/BGA



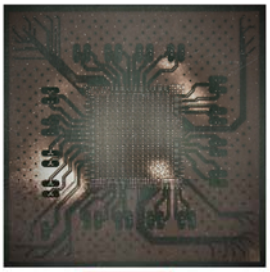
X-Ray – Top View

X-Ray Side View

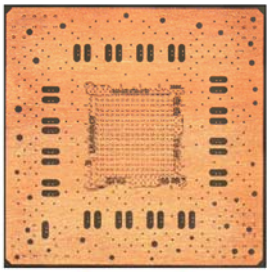
73. The integrated circuit package substrate of the IDT 80HCPS1432CHMHI is manufactured to have 8 metal layers and 7 via layers



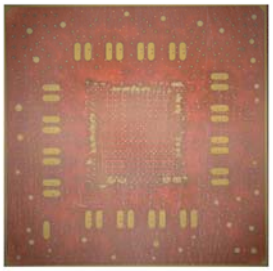
Metal Layer 1



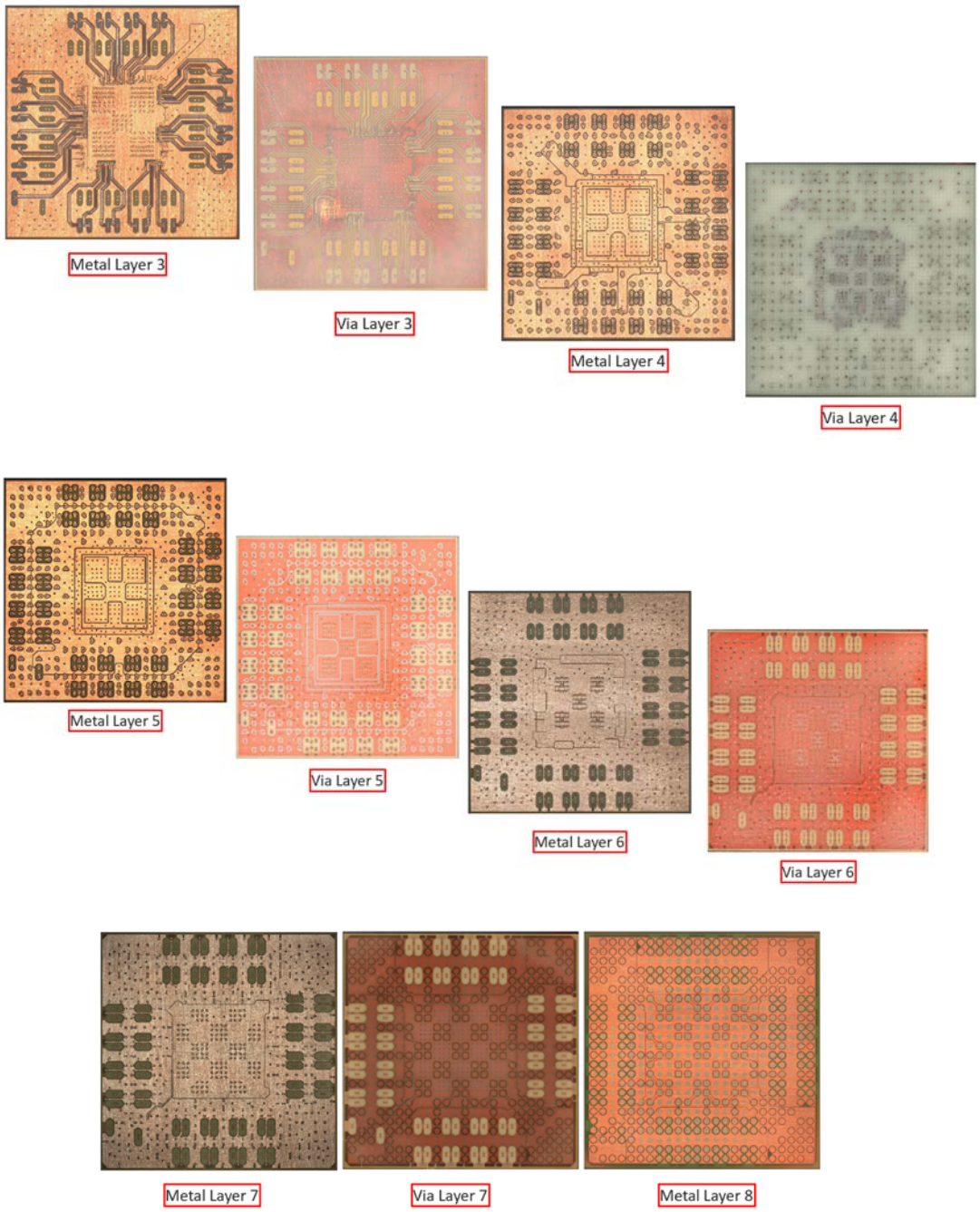
Via Layer 1



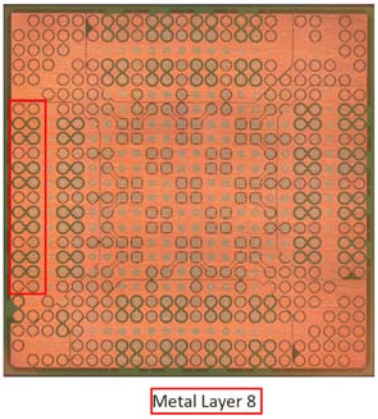
Metal Layer 2



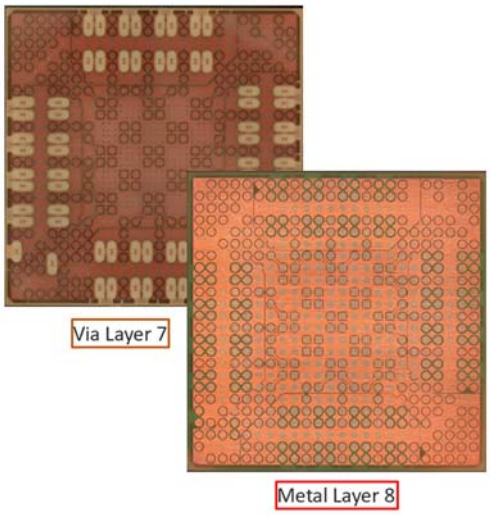
Via Layer 2



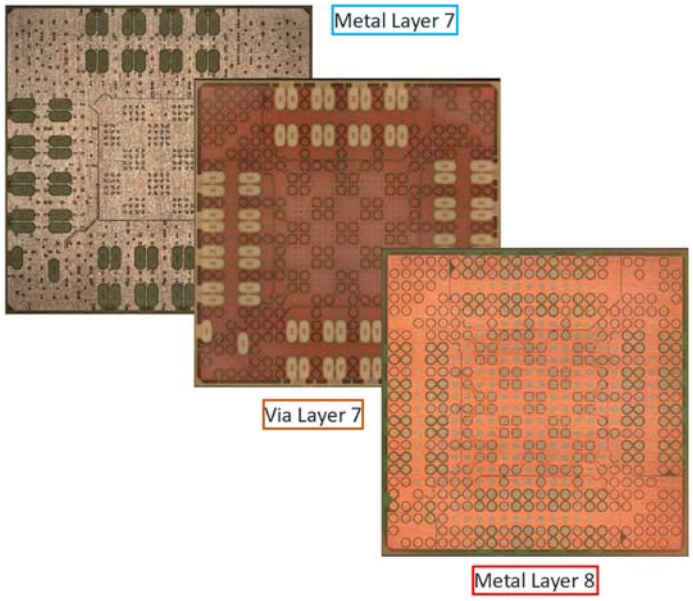
74. During manufacture of the IDT 80HCPS1432CHMHI, a first electrically conductive layer (metal layer 8) with a plurality of rows of contact pads (for example, shown in red below) is formed:



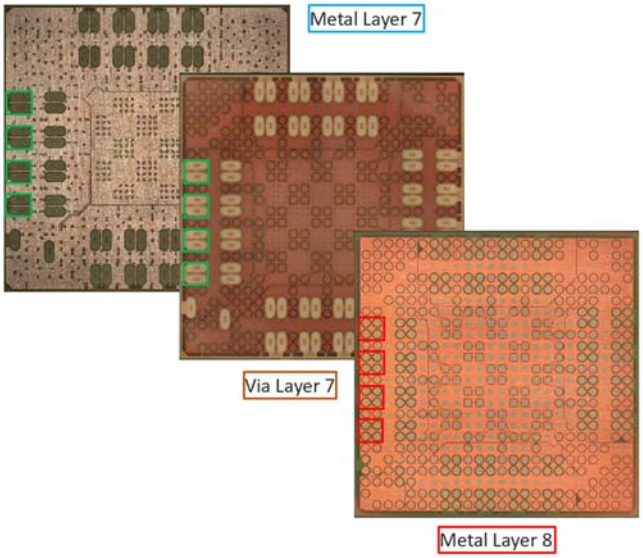
75. During manufacture of the IDT 80HCPS1432CHMHI, an electrically insulating layer (via layer 7 below) is formed on the first electrically conductive layer (metal layer 8):



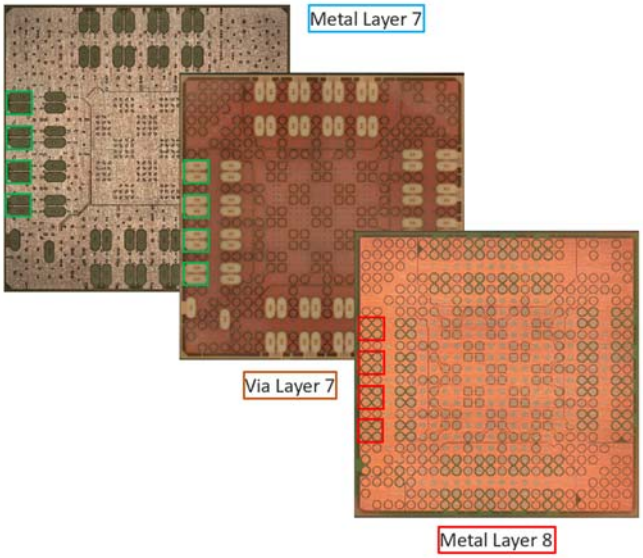
76. During manufacture of the IDT 80HCPS1432CHMHI, a second electrically conductive layer (metal layer 7) is formed over the electrically insulating layer (via layer 7), such that there is no intermediate conductive layer between the first and second electrically conductive layers (metal layers 8 and 7):



77. The second electrically conductive layer (metal layer 7) comprises metal and has two or more cutouts (for example, as shown in green on metal layer 7 below), wherein each cutout encloses an electrically insulating area within the second electrically conductive layer.



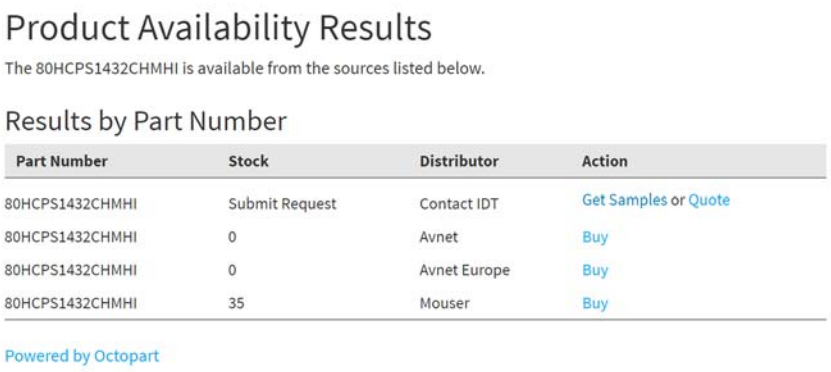
78. Each electrically insulating area (for example, in green) also completely overlaps a corresponding one of the contact pads (in red below) such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.



79. Claim 1 of the Hall 269 Patent applies to each Hall 269 Accused Product at least because each of those products contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts as the IDT 80HCPS1432CHMHI.

80. On information and belief, each of the Hall 269 Accused Products have been available for purchase in the United States, including but not limited to, directly from IDT, through IDT's website, and/or through IDT-authorized Americas distributors.

81. By way of example only, on information and belief, the IDT 80HCPS1432CHMHI and other IDT RapidIO devices have been available for purchase in the United States, including but not limited to through IDT's website, either directly from IDT or through IDT-authorized distributors:



Product Availability Results

The 80HCPS1432CHMHI is available from the sources listed below.

Results by Part Number

Part Number	Stock	Distributor	Action
80HCPS1432CHMHI	Submit Request	Contact IDT	Get Samples or Quote
80HCPS1432CHMHI	0	Avnet	Buy
80HCPS1432CHMHI	0	Avnet Europe	Buy
80HCPS1432CHMHI	35	Mouser	Buy

Powered by Octopart

See https://www.idt.com/buy-sample/check-inventory/result?show_price=1&partno=80HCPS1432CHMHI&exact=1 (last visited March 3, 2020).

82. IDT has known of the Hall 269 Patent and has been on notice of its infringement since at least March 15, 2019, when Bell Semic first identified the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement of the Hall 269 Patent. After IDT did not respond, on April 23, 2019 Bell Semic again sent an email to IDT identifying the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement. IDT did not respond to these emails before Bell Semic filed its Original Complaint.

83. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 269 Patent at least because Bell Semic provided IDT with written notice of its infringement as detailed above.

84. IDT, knowing that the process of manufacturing its Accused Hall 269 Products infringes the Hall 269 Patent and with specific intent for others to infringe the Hall 269 Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Hall 269 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Hall 269 Accused Products; and/or (2) actively inducing others to use, sell,

offer to sell, and/or import in or into the United States without authorization the Hall 269 Accused Products, as well as products incorporating the same.

85. IDT knows, and has known since at least March 15, 2019, that the process of manufacturing the Hall 269 Accused Products infringes the Hall 269 Patent. Despite this knowledge, IDT knowingly and intentionally instructed, and continues to instruct, its OEMs, package assemblers, and foundry suppliers to infringe the Hall 269 Patent through the unlicensed manufacture and assembly of the Hall 269 Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States. IDT further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent by its customers', distributors', and/or other third parties' sale and distribution of the Hall 269 Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. IDT further knowing and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent through use, sale, offers for sale, and/or importing in or into the United States of the Hall 269 Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on IDT's website.

86. IDT further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 269 Accused Products and/or products incorporating the Hall 269 Accused Products in the United States by marketing the Hall 269 Accused Products in the United States; providing information such as detailed datasheets supporting use of the Hall 269 Patent Accused Products that promote their features, specifications, and applications; promoting the incorporation of the Hall 269 Patent Accused

Products into end-user products through partner programs, including the IDT Partner Program (*see, e.g.*, https://www.idt.com/us/en/support/partners). IDT further encourages the use of its infringing products by providing for its customers, by way of example only, (1) documentation and tools for its products, including white papers, brochures, datasheets, and manuals (https://www.idt.com/us/en/support/document-search); (2) complimentary design review services (https://www.idt.com/us/en/support/clock-tree-design-service); (3) automated utilities, calculators, and reference designs (*see, e.g.*, https://www.idt.com/us/en/jitter-measurement-utility; https://www.idt.com/us/en/support/calculators; https://www.idt.com/us/en/support/reference-designs); and (4) blog posts further explaining IDT products (https://www.idt.com/us/en/blogs).

87. Bell Semic has sustained and is entitled to recover damages as a result of IDT's past and continuing infringement of the Hall 269 Patent, in an amount adequate to compensate for IDT's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

88. IDT's infringement of the Hall 269 Patent is and has been knowing, deliberate, and willful. IDT learned of its infringement of the Hall 269 Patent no later than March 15, 2019. As detailed above, Bell Semic sent an email to IDT on March 15, 2019 identified the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement of the Hall 269 Patent. After IDT did not respond, on April 23, 2019 Bell Semic again sent an email to IDT identifying the IDT 80HCPS1432CHMHI as infringing and exemplary of IDT's infringement. IDT did not respond to these emails before Bell Semic filed its Original Complaint. Despite these efforts, and knowing that it is willfully infringing the Hall 269 Patent, IDT continued, and continues to commit acts of direct and indirect infringement despite knowing its actions constitute

infringement of the valid and enforceable Hall 269 Patent, despite a risk of infringement that was known or so obvious that it should have been known to IDT, and/or even though IDT otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, IDT's conduct is and has been egregious. IDT's knowing, deliberate, and willful infringement of the Hall 269 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 3

Willful Infringement of U.S. Patent No. 7,319,272 (Ramakrishnan Patent)

89. Plaintiff re-alleges and incorporates by reference the allegations in paragraphs 1-11, 19-21, and 26-43 as if fully set forth herein.

90. The Ramakrishnan Patent is generally related to a pattern of contacts including high-speed transmitter contacts disposed in a first portion of the pattern in transmitter differential pairs. High-speed receiver contacts are disposed in a second portion of the pattern, where the first portion of the pattern is not interspersed with the second portion of the pattern, and the high-speed receiver contacts are disposed in receiver differential pairs. At least one unbroken line of other contacts is disposed between the first portion of the pattern and the second portion of the pattern, where the other contacts do not contain any high-speed transmitter contacts and high-speed receiver contacts. Low speed IO contacts are disposed in a third portion of the pattern that is disposed in an interior portion of the pattern relative to both the first portion of the pattern and the second portion of the pattern. Substantially all of the contacts are disposed at a standard pitch from one another on a single contact surface. (*See* Ramakrishnan Patent, Abstract.)

91. To ensure performance of high-speed integrated circuits, isolation of transmitter and receiver pairs of high-speed signals and between high-speed signals and other signals in integrated circuits, package substrate, and circuit board are critical factors to consider. It is advantageous to route integrated circuits so that high-speed signals are adequately isolated in the package substrate and also in the printed circuit board. Additionally, routing of high-speed signals in the lowest possible number of printed circuit board layers reduces the overall cost of the system. By configuring the contact pattern, as taught by the Ramakrishnan Patent, better separation between the high-speed transmitter contacts and the high-speed receiver contacts is achieved, and the high-speed signals are more easily routed out of the pattern.

92. The Ramakrishnan Patent contains 3 independent claims and 20 total claims, covering various methods. Claim 17 reads:

> A package substrate having a pattern of contacts comprising:
>
> high speed transmitter contacts disposed in a first portion of the pattern, where the high speed transmitter contacts are disposed in transmitter differential pairs,
>
> high speed receiver contacts disposed in a second portion of the pattern, where the first portion of the pattern is not interspersed with the second portion of the pattern, and the high speed receiver contacts are disposed in receiver differential pairs,
>
> at least one unbroken line of other contacts disposed between the first portion of the pattern and the second portion of the pattern, where the other contacts do not contain any high speed transmitter contacts and high speed receiver contacts, and
>
> low speed IO contacts disposed in a third portion of the pattern, where a part of the third portion of the pattern is disposed in an interior portion of the pattern relative to both the first portion of the pattern and the second portion of the pattern,

93. IDT has directly infringed, and continues to directly infringe, one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the

United States without authorization products covered by one or more claims of the Ramakrishnan Patent (*e.g.*, claims 17-19), including, but not limited to:

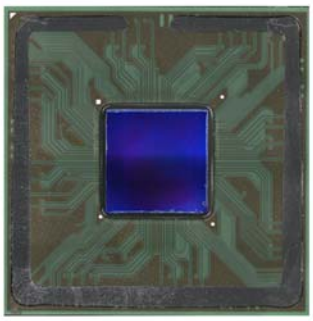
- IDT products that have transmitter and receiver contacts with an unbroken line of other contacts between them, and I/O contacts in the interior portion of the contacts relative to the transmitter and receiver contacts;
- IDT's 89H64H16AG2ZC, a 64-lane, 16-port PCIe Gen2 System Interconnect Switch intended for high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows such as servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication; and
- IDT's devices that are variants of the above-identified products; (collectively, the "Ramakrishnan Accused Products").

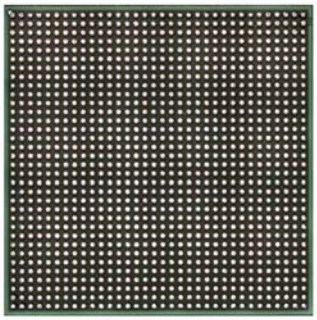
94. By way of non-limiting example only, the IDT 89H64H16AG2ZC infringes claim 17 of the Ramakrishnan Patent because it is an integrated circuit with a package substrate having a pattern of contacts that has (1) high-speed transmitter contacts disposed in a first portion of the pattern that are disposed in transmitter differential pairs; (2) high-speed receiver contacts disposed in a second portion of the pattern where the first portion of the pattern is not interspersed with the second portion of the pattern and the high-speed receiver contacts are disposed in receiver differential pairs; (3) an unbroken line of other contacts disposed between the first and second portions of the pattern, where the other contacts do not contain any high-speed transmitter contacts and high-speed receiver contacts; and (4) low speed IO contacts disposed in a third portion of the pattern that has a part of it disposed in an interior portion of the pattern relative to both the first and second portions of the pattern. Substantially all of the

contacts in the IDT 89H64H16AG2ZC are also disposed at a first pitch one from another on a single contact surface.

95. As shown below, the IDT 89H64H16AG2ZC is an integrated circuit with a package substrate having a pattern of contacts:

Component – Top View


Component – Top View (Lid removed)


Component – Bottom View/BGA View

96. The data sheet for the IDT 89H64H16AG2ZC provides a top view of the pinout:

89H64H16AG2 Active Samples Available

64-lane, 16-port PCIe Gen2 System Interconnect Switch

Provides 64 PCIe Gen2 lanes and 16 ports of high-performance, deterministic system interconnect switching. All ports receive full line rate, non-blocking throughput for multiple traffic flows regardless of switch loading.

DOWNLOAD DATASHEET

Features

- 64 PCIe Gen2 Lanes, 16 Switch Ports
- Non-blocking switch architecture optimized for High Performance System Interconnect
- Partionable switch architecture for true mutli-root support
- Internal buffering and flow control credits optimized for maximum bandwidth and large payloads
- Low latency, Low power

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Product Options

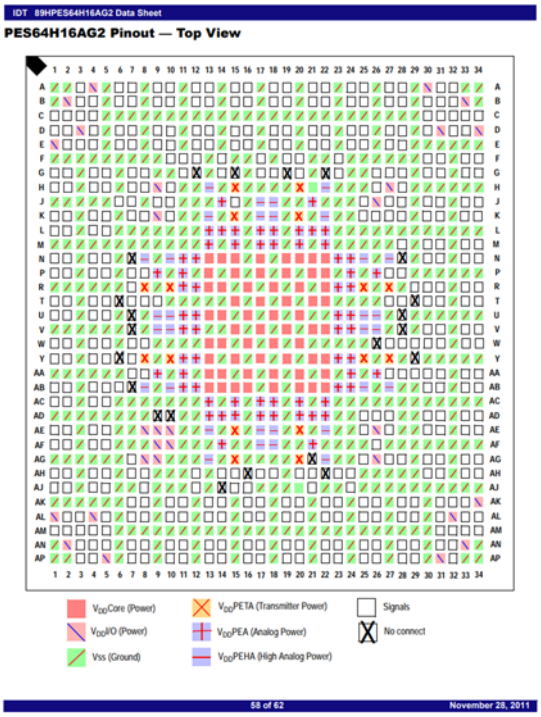
Orderable Part ID	Part Status	Pkg. Code	Pkg. Type	Lead Count (#)	Temp. Grade	Pb (Lead) Free	Carrier Type	Buy Sample
89H64H16AG2ZCBLG	Active	BLG1156	FCBGA	1156	C	Yes	Tray	Get Samples Buy / Quote
89H64H16AG2ZCBLGI	Active	BLG1156	FCBGA	1156	I	Yes	Tray	Get Samples Buy / Quote

☐ Show Obsolete and NRND

Tools & Support

GET SAMPLES
TECHNICAL SUPPORT
QUALITY/PACKAGE SUPPORT

See https://www.idt.com/products/interface-connectivity/pci-express-solutions/pci-express-switches/89h64h16ag2-64-lane-16-port-pcie-gen2-system-interconnect-switch (last accessed March 3, 2020).

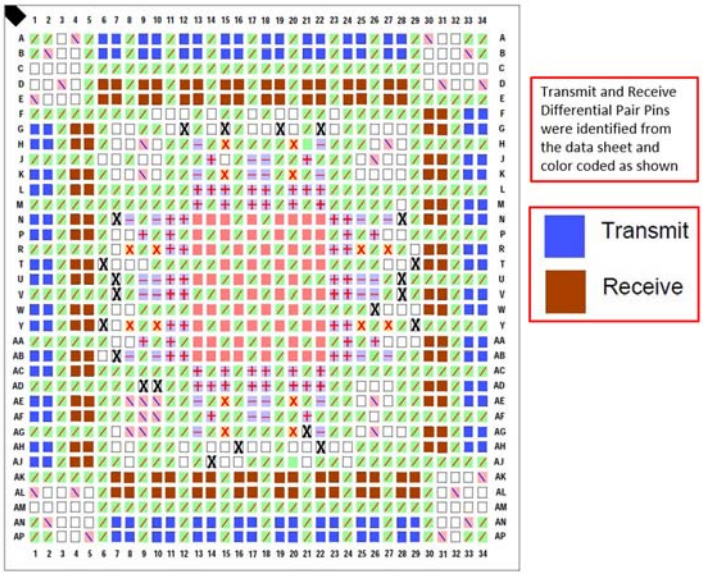


97. The datasheet for the IDT 89H64H16AG2ZC also provides a table connecting the pin numbers above with signal names, including with transmitting and receiving differential pairs, with examples identified in blue and brown, respectively, below:

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.

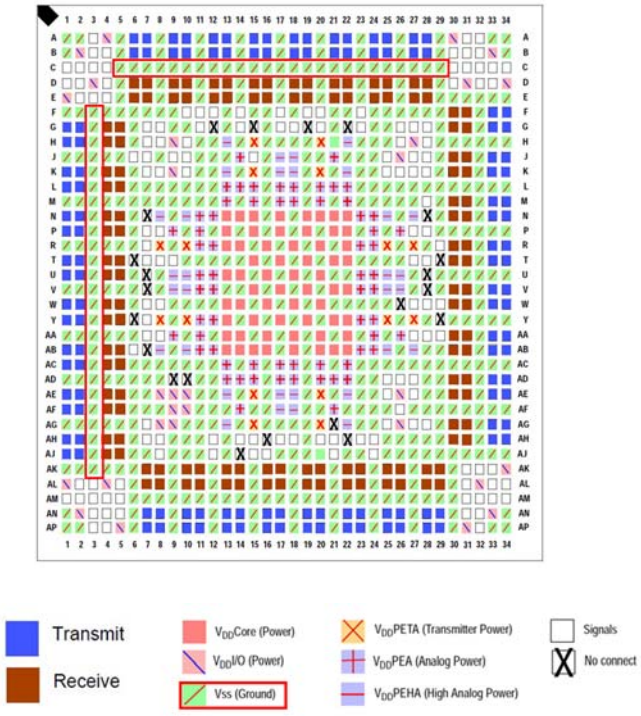
Table 2 PCI Express Interface Pins (Part 1 of 3)

98. The diagram below applies blue and brown colors for these transmitting and receiving pin numbers to the top view of the pinout:

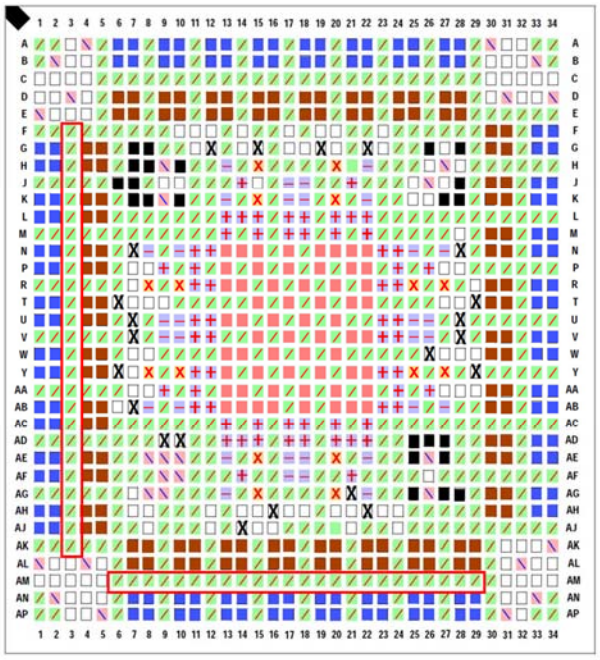


99. As shown in the diagram above, the IDT 89H64H16AG2ZC has high-speed transmitter contacts (in blue) disposed in a first portion of the pattern of contacts, where the high-speed transmitter contacts are disposed in transmitter differential pairs (for example, A24-B24 or A25-B25). This diagram also shows high-speed receiver contacts (in brown) disposed in a second portion of the pattern, where the first portion of the pattern is not interspersed with the second portion of the pattern, and the high-speed receiver contacts are disposed in receiver differential pairs (for example, D24-E24 or D25-E25).

100. The IDT 89H64H16AG2ZC also has an unbroken line of other contacts disposed between the first and second portions of the pattern, where the other contacts do not contain any high-speed transmitter contacts or high-speed receiver contacts (for example, the lines of ground contacts circled in red below):



101. As shown in the diagram and table below, the IDT 89H64H16AG2ZC has low speed IO contacts (denoted in black below, for example, pins G26 and G28, with function GPIO_33 and GPIO_32, general purpose I/O) disposed in a third portion of the pattern with a part of the third portion of the pattern disposed in an interior portion of the pattern relative to both the first and second portions of the pattern:



IDT 89HPES64H16AG2 Data Sheet

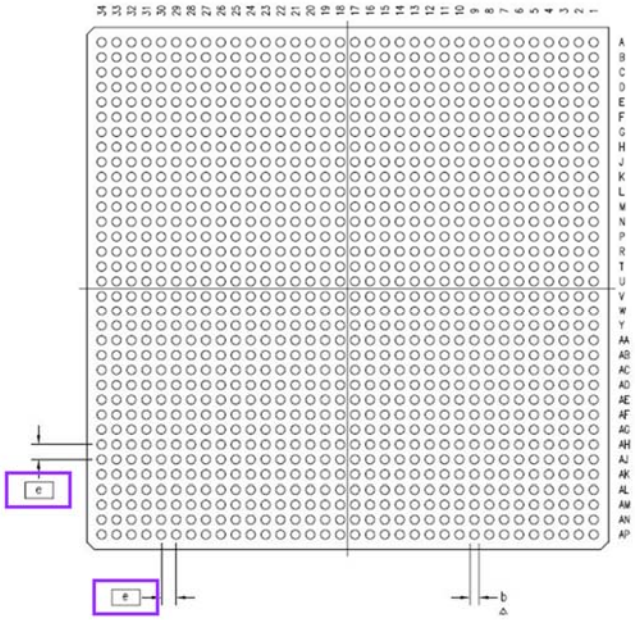
Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
E1	V_{DD}I/O		F1	V_{SS}		G1	PE10TP0		H1	PE10TP1	
E2	GPIO_30	2	F2	V_{SS}		G2	PE10TN0		H2	PE10TN1	
E3	GPIO_31	2	F3	V_{SS}		G3	V_{SS}		H3	V_{SS}	
E4	GPIO_24	2	F4	V_{SS}		G4	PE10RN0		H4	PE10RN1	
E5	V_{SS}		F5	V_{SS}		G5	PE10RP0		H5	PE10RP1	
E6	PE09RP3		F6	V_{SS}		G6	V_{SS}		H6	V_{SS}	
E7	PE09RP2		F7	V_{SS}		G7	GPIO_46	2	H7	GPIO_48	2
E8	V_{SS}		F8	V_{SS}		G8	GPIO_45	2	H8	GPIO_20	1
E9	PE09RP1		F9	V_{SS}		G9	V_{SS}		H9	V_{DD}I/O	
E10	PE09RP0		F10	REFRES09		G10	V_{CC}		H10	GPIO_47	2
E11	V_{SS}		F11	P09CLKP		G11	P09CLKN		H11	V_{SS}	
E12	PE08RP3		F12	V_{SS}		G12	NC		H12	V_{SS}	
E13	PE08RP2		F13	V_{SS}		G13	V_{SS}		H13	V_{DD}PEHA	
E14	V_{SS}		F14	P08CLKP		G14	P08CLKN		H14	V_{SS}	
E15	PE08RP1		F15	V_{SS}		G15	NC		H15	V_{DD}PETA	
E16	PE08RP0		F16	V_{SS}		G16	V_{SS}		H16	V_{SS}	
E17	V_{SS}		F17	REFRESPLL		G17	GCLKN0		H17	V_{SS}	
E18	PE03RP3		F18	V_{SS}		G18	GCLKP0		H18	V_{SS}	
E19	PE03RP2		F19	REFRES03		G19	NC		H19	V_{SS}	
E20	V_{SS}		F20	P03CLKP		G20	P03CLKN		H20	V_{DD}PETA	
E21	PE03RP1		F21	V_{SS}		G21	V_{SS}		H21	REFRES02	
E22	PE03RP0		F22	V_{SS}		G22	NC		H22	V_{DD}PEHA	
E23	V_{SS}		F23	P02CLKP		G23	P02CLKN		H23	V_{SS}	
E24	PE02RP3		F24	V_{SS}		G24	V_{SS}		H24	V_{SS}	
E25	PE02RP2		F25	V_{SS}		G25	V_{SS}		H25	V_{SS}	
E26	V_{SS}		F26	V_{SS}		G26	GPIO_33	2	H26	MSMBDAT	
E27	PE02RP1		F27	V_{SS}		G27	MSMBCLK		H27	V_{DD}I/O	
E28	PE02RP0		F28	V_{SS}		G28	GPIO_32	2	H28	SSMBCLK	
E29	V_{SS}		F29	V_{SS}		G29	V_{SS}		H29	V_{SS}	
E30	V_{SS}		F30	PE01RP3		G30	PE01RP2		H30	V_{SS}	
E31	V_{SS}		F31	PE01RN3		G31	PE01RN2		H31	V_{SS}	
E32	V_{SS}		F32	V_{SS}		G32	V_{SS}		H32	V_{SS}	
E33	V_{SS}		F33	PE01TN3		G33	PE01TN2		H33	V_{SS}	
E34	V_{SS}		F34	PE01TP3		G34	PE01TP2		H34	V_{SS}	

Table 23 PES64H16AG2 1156-pin Signal Pin-Out (Part 2 of 9)

GPIO[32]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2AIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Attention Indicator Output. 2nd Alternate function pin name: P6LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Up Status Output.
GPIO[33]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PIN 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Indicator Output. 2nd Alternate function pin name: P6ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 6 Link Active Status Output.
GPIO[34]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: HP2PEP 1st Alternate function pin type: Output 1st Alternate function: Hot Plug Signal Group 2 Power Enable Output. 2nd Alternate function pin name: P7LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 7 Link Up Status Output.

Table 5 General Purpose I/O Pins (Part 4 of 7)

102. As shown below, in the IDT 89H64H16AG2ZC, substantially all of the contacts are disposed at a first pitch (1.0 mm, indicated by “e”) from another on a single contact surface:



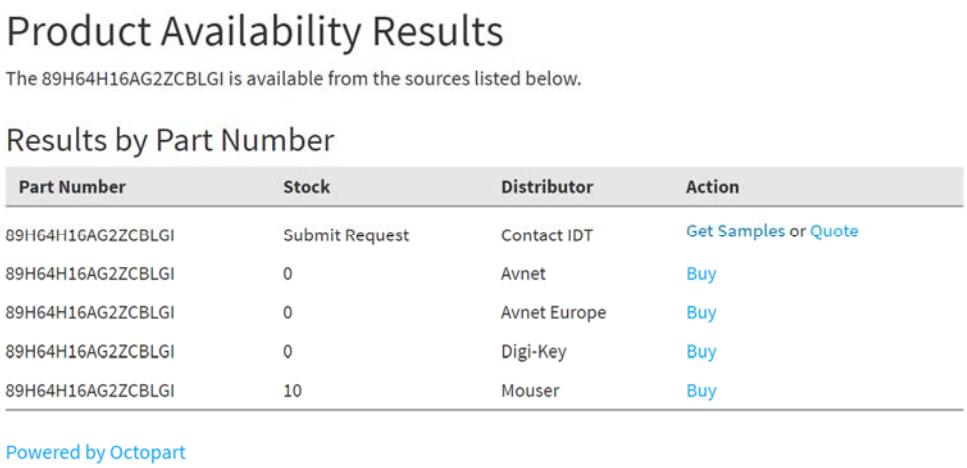
SYMBOL	JEDEC VARIATION NONE			NOTE
	MIN	NOM	MAX	
A	–	–	3.42	
A1	.30	–	–	
A2	2.16	–	2.82	
D	35.00 BSC			
E	35.00 BSC			
M	.34			3
N	1156			4
e	1.00 BSC			
b	.50	.60	.70	5
CENTER BALL MATRIX	N/A			

The solder ball contacts are all disposed on the BGA surface at a 1.0 mm pitch

103. Claim 17 of the Ramakrishnan Patent applies to each Ramakrishnan Accused Product at least because each of those products contain the same or similar transmitter and receiver contacts with an unbroken line of other contacts between them, and I/O contacts in the interior portion of the contacts relative to the transmitter and receiver contacts, as the IDT 89H64H16AG2ZC.

104. On information and belief, each of the Ramakrishnan Accused Products have been available for purchase in the United States, including but not limited to, directly from IDT, through IDT's website, and/or through IDT-authorized Americas distributors.

105. By way of example only, on information and belief, the IDT 89H64H16AG2ZC and other Ramakrishnan Patent Accused Products have been available for purchase in the United States, including but not limited to through IDT's website, either directly from IDT or through IDT-authorized distributors:



Product Availability Results

The 89H64H16AG2ZCBLGI is available from the sources listed below.

Results by Part Number

Part Number	Stock	Distributor	Action
89H64H16AG2ZCBLGI	Submit Request	Contact IDT	Get Samples or Quote
89H64H16AG2ZCBLGI	0	Avnet	Buy
89H64H16AG2ZCBLGI	0	Avnet Europe	Buy
89H64H16AG2ZCBLGI	0	Digi-Key	Buy
89H64H16AG2ZCBLGI	10	Mouser	Buy

Powered by Octopart

See https://www.idt.com/buy-sample/check-inventory/result?show_price=1&partno=89H64H16AG2ZCBLGI&exact=1 (last visited March 3, 2020).

106. IDT has known of the Ramakrishnan Patent and has been on notice of its infringement since at least November 18, 2019 when Bell Semic filed its Original Complaint, which included the above detailed allegations of infringement of the IDT 89H64H16AG2ZC and description of other similarly infringing products.

107. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Ramakrishnan Patent at least because Bell Semic provided IDT with written notice of its infringement as detailed above.

108. IDT, knowing its products infringe the Ramakrishnan Patent and with specific intent for others to infringe the Ramakrishnan Patent, has induced infringement of, and continue to induce infringement of, one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Ramakrishnan Accused Products, as well as products containing the same. IDT knowingly and intentionally instructs its customers, OEMs, foundry

suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on IDT's website. IDT actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Ramakrishnan Accused Products in the United States. IDT knows, and has known since at least November 18, 2019, that the Ramakrishnan Accused Products infringe the Ramakrishnan Patent, and purposefully and knowingly sells and offers to sell the Ramakrishnan Accused Products to its customers with the knowledge and expectation that the Ramakrishnan Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

109. IDT further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Ramakrishnan Accused Products and/or products incorporating the Ramakrishnan Accused Products in the United States by marketing the Ramakrishnan Accused Products in the United States; providing information such as detailed datasheets supporting use of the Ramakrishnan Patent Accused Products that promote their features, specifications, and applications; promoting the incorporation of the Ramakrishnan Patent Accused Products into end-user products through partner programs, including the IDT Partner Program (*see, e.g.*, https://www.idt.com/us/en/support/partners). IDT further encourages the use of its infringing products by providing for its customers, by way of example only, (1) documentation and tools for its products, including white papers, brochures, datasheets, and manuals (https://www.idt.com/us/en/support/document-search); (2) complimentary design review services (https://www.idt.com/us/en/support/clock-tree-design-service); (3) automated

utilities, calculators, and reference designs (*see, e.g.*, https://www.idt.com/us/en/jitter-measurement-utility; https://www.idt.com/us/en/support/calculators; https://www.idt.com/us/en/support/reference-designs); and (4) blog posts further explaining IDT products (https://www.idt.com/us/en/blogs).

110. IDT has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Ramakrishnan Accused Products, which constitute a material part of the invention of the Ramakrishnan Patent, knowing the Ramakrishnan Accused Products to be especially made or especially adapted for use in infringement of the Ramakrishnan Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

111. Bell Semic has sustained and is entitled to recover damages as a result of IDT's past and continuing infringement, in an amount adequate to compensate for IDT's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

112. IDT's infringement of the Ramakrishnan Patent is and has been knowing, deliberate, and willful. IDT learned of its infringement of the Ramakrishnan Patent no later than November 18, 2019, when Bell Semic filed the Original Complaint in this Action. Knowing that it was willfully infringing the Ramakrishnan Patent, IDT continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Ramakrishnan Patent, despite a risk of infringement that was known or so obvious that it should have been known to IDT, and/or even though IDT otherwise knew or

should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, IDT's conduct is and has been egregious. IDT's knowing, deliberate, and willful infringement of the Ramakrishnan Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 4

Willful Infringement of U.S. Patent No. 6,624,007 (Kobayakawa Patent)

113. Plaintiff re-alleges and incorporates by reference the allegations in paragraphs 1-11 and 22-43 as if fully set forth herein.

114. The Kobayakawa Patent is generally related to methods for making a leadframe used for fabricating a semiconductor device. Semiconductor chips are mounted on a leadframe, wire-bonded, and then enclosed with resin, creating an intermediate product. The intermediate product is cut into separate, finished devices by using two cutters. One cutter is relatively thin, while the other cutter is relatively thick. The thin cutter is used for making a full cut in the leadframe, while the thick cutter is used for making a half-depth cut in the leadframe. (*See* Kobayakawa Patent, Abstract.)

115. The Kobayakawa Patent contains 2 independent claims and 8 total claims, covering various methods. Claim 1 reads:

> A method of making a semiconductor device, the method comprising the steps of:
>
> mounting a semiconductor chip on a leadframe;
>
> producing an intermediate product by forming a packaging layer to enclose the chip, the intermediate product including the leadframe, the chip and the packaging layer; and
>
> cutting the intermediate product;

> wherein the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness greater than the first thickness, the first cutter being used for making a full cut in the leadframe, the second cutter being used for making a partial cut in the leadframe, the full cut and the partial cut corresponding in position to each other.

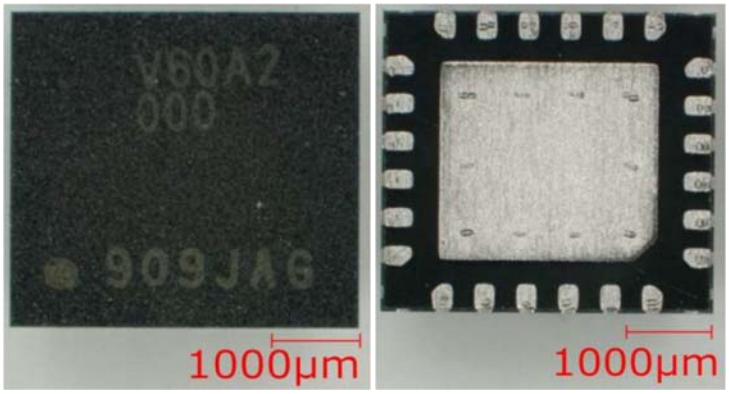
116. IDT has directly infringed, and continues to directly infringe, one or more claims of the Kobayakawa Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Kobayakawa Patent (*e.g.*, claims 1, 3, and 4). Such products manufactured using these infringing methods include, but are not limited to:

- IDT products with step cut wettable flank packages, including IDT's VFQFPN and DFN package types with wettable flanks;
- IDT's 5P49V60, a VersaClock 6E programmable clock generator intended for automotive applications such as infotainment, dashboard, video processing, in-vehicle networking, as well as applications based on PCI-Express or USB 3; and
- IDT's devices that are variants of the above-identified products; (collectively, the "Kobayakawa Accused Products").

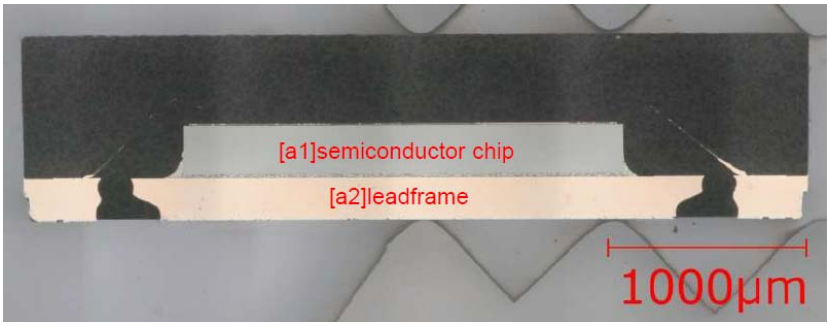
117. By way of non-limiting example only, the process of manufacturing the IDT 5P49V60 meets all of the steps of claim 1 of the Kobayakawa Patent including (1) mounting a semiconductor chip on a leadframe; (2) producing an intermediate product by forming a packaging layer to enclose the chip, the intermediate product including the leadframe, the chip and the packaging layer; and (3) cutting the intermediate product; wherein the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness greater than the first thickness, the first cutter being used for making a full cut in the

leadframe, the second cutter being used for making a partial cut in the leadframe, the full cut and the partial cut corresponding in position to each other.

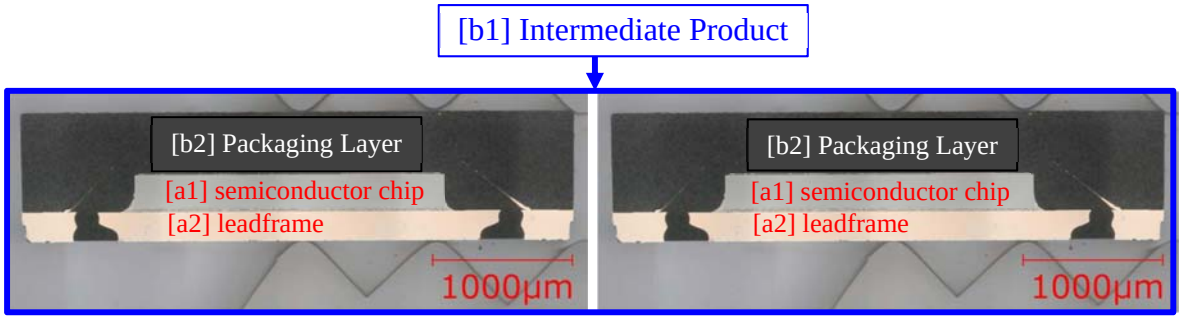
118. As shown below, the IDT 5P49V60 is semiconductor device:



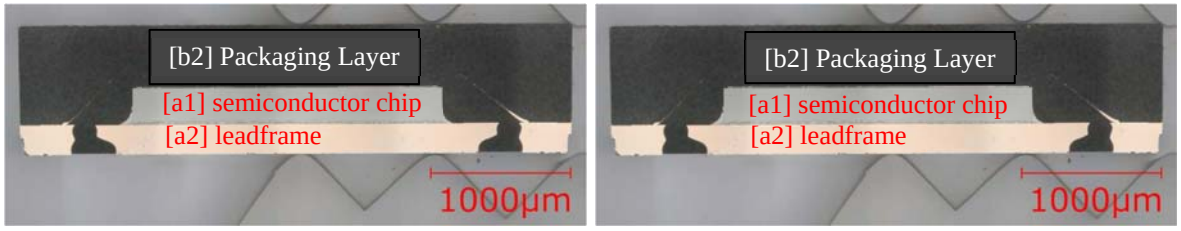
119. The IDT 5P49V60 contains a semiconductor chip [a1] mounted on a leadframe [a2]:



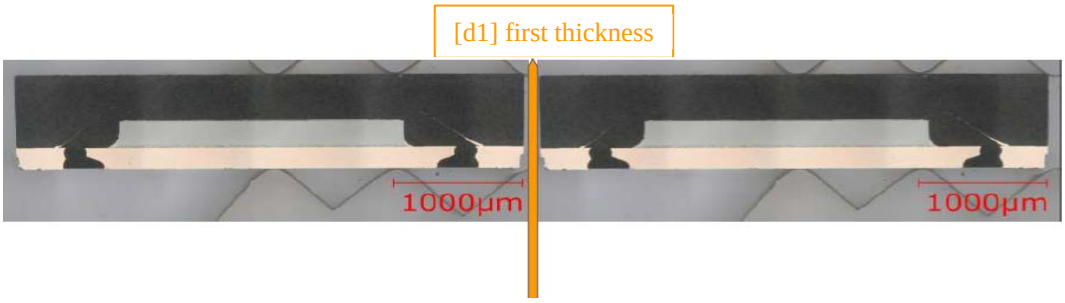
120. The IDT 5P49V60 is produced from an intermediate product ([b1]) by forming a packaging layer to enclose the chip, the intermediate product including the leadframe [a2], the chip[a1], and the packaging layer [b2] :



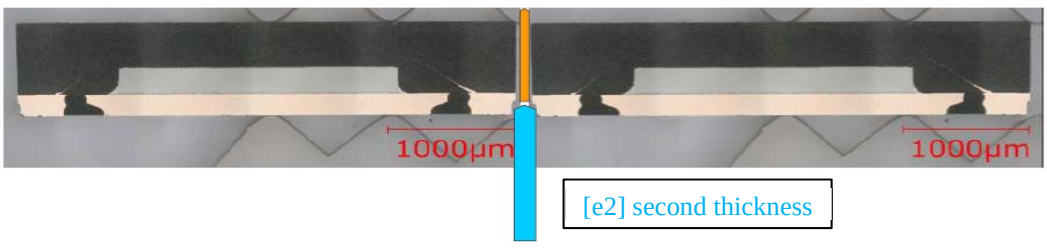
121. During manufacture of the IDT 5P49V60, the intermediate product is cut:



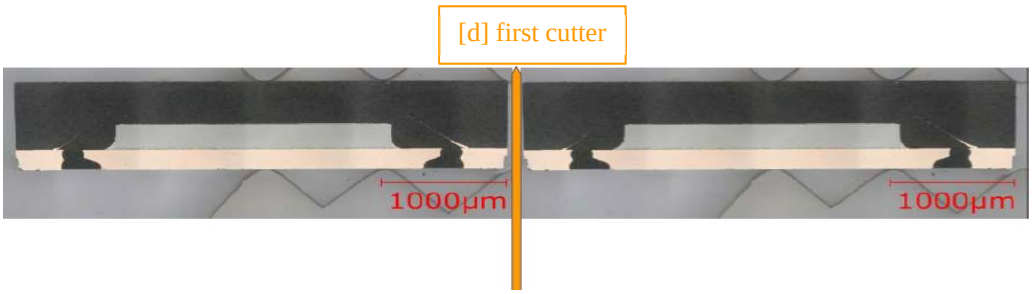
122. During manufacture of the IDT 5P49V60, the cutting step is performed by using a first cutter having a first thickness [d1]:



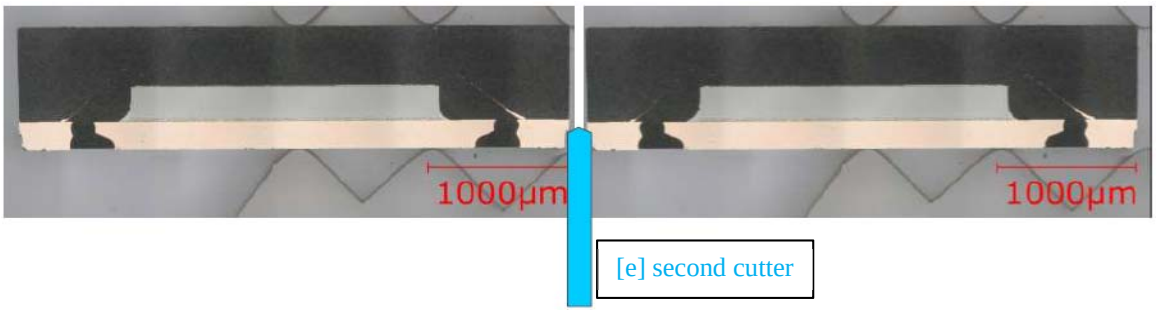
123. During manufacture of the IDT 5P49V60, the cutting step is performed by using a first cutter having a first thickness and a second cutter having a second thickness [e2] greater than the first thickness:



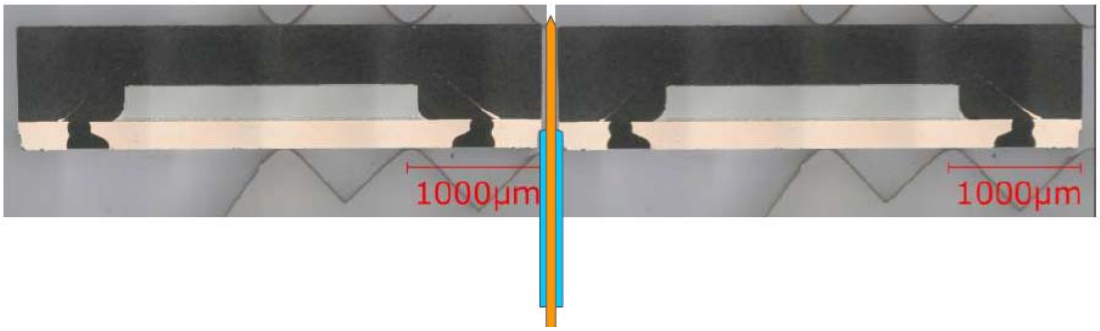
124. During manufacture of the IDT 5P49V60, the first cutter [d] is used for making a full cut in the leadframe:



125. During manufacture of the IDT 5P49V60, the second cutter [e] is used for making a partial cut in the leadframe:



126. The full and partial cut correspond in position to each other:



127. Claim 1 of the Kobayakawa Patent applies to each Kobayakawa Accused Product at least because each of those products are manufactured to have step cut wettable flank packages, like the IDT 5P49V60.

128. On information and belief, each of the Kobayakawa Accused Products have been available for purchase in the United States, including but not limited to, directly from IDT, through IDT's website, and/or through IDT-authorized Americas distributors.

129. By way of example only, on information and belief, the IDT 5P49V60 has been available for purchase in the United States, including but not limited to through IDT's website, either directly from IDT or through IDT-authorized distributors:

Product Availability Results

The 5P49V60A000NLG2 is available from the sources listed below.

Results by Part Number

Part Number	Stock	Distributor	Action
5P49V60A000NLG2	Submit Request	Contact IDT	Get Samples or Quote
5P49V60A000NLG2	0	Avnet	Buy
5P49V60A000NLG2	774	Farnell	Buy
5P49V60A000NLG2	774	Newark	Buy
5P49V60A000NLG2	507	Digi-Key	Buy
5P49V60A000NLG2	658	Mouser	Buy
5P49V60A000NLG2	0	RFMW	Buy

See https://www.idt.com/us/en/buy-sample/check-inventory/result?show_price=1&partno=5P49V60A000NLG2&exact=1 (last visited March 24, 2020).

130. IDT has known of the Kobayakawa Patent and has been on notice of its infringement since at since at least March 26, 2020, when Bell Semic wrote to IDT and identified the IDT 5P49V60 as exemplary of IDT's infringement of the Kobayakawa Patent.

131. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Kobayakawa Patent at least because Bell Semic provided IDT with written notice of its infringement as detailed above.

132. IDT, knowing that the process of manufacturing its Kobayakawa Accused Products infringes the Kobayakawa Patent and with specific intent for others to infringe the

Kobayakawa Patent induces infringement of, one or more claims of the Kobayakawa Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Kobayakawa Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Kobayakawa Accused Products, as well as products incorporating the same.

133. IDT knows since at least March 26, 2020 that the process of manufacturing the Kobayakawa Accused Products infringes the Kobayakawa Patent. Despite this knowledge, IDT knowingly and intentionally instructs its OEMs, package assemblers, and foundry suppliers to infringe the Kobayakawa Patent through the unlicensed manufacture and assembly of the Kobayakawa Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States. IDT further knowingly and intentionally aids and abets infringement of the Kobayakawa Patent by its customers', distributors', and/or other third parties' sale and distribution of the Kobayakawa Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. IDT further knowing and intentionally aids and abets infringement of the Kobayakawa Patent through use, sale, offers for sale, and/or importing in or into the United States of the Kobayakawa Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on IDT's website.

134. IDT further induces infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Kobayakawa Accused Products and/or products incorporating the Kobayakawa Accused Products in the United States by marketing the

Kobayakawa Accused Products in the United States; providing information such as detailed datasheets supporting use of the Kobayakawa Patent Accused Products that promote their features, specifications, and applications; promoting the incorporation of the Kobayakawa Patent Accused Products into end-user products through partner programs, including the IDT Partner Program (*see, e.g.*, https://www.idt.com/us/en/support/partners). IDT further encourages the use of its infringing products by providing for its customers, by way of example only, (1) documentation and tools for its products, including white papers, brochures, datasheets, and manuals (https://www.idt.com/us/en/support/document-search); (2) complimentary design review services (https://www.idt.com/us/en/support/clock-tree-design-service); (3) automated utilities, calculators, and reference designs (*see, e.g.*, https://www.idt.com/us/en/jitter-measurement-utility; https://www.idt.com/us/en/support/calculators; https://www.idt.com/us/en/support/reference-designs); and (4) blog posts further explaining IDT products (https://www.idt.com/us/en/blogs).

135. Bell Semic has sustained and is entitled to recover damages as a result of IDT's past and continuing infringement of the Kobayakawa Patent, in an amount adequate to compensate for IDT's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

136. IDT's infringement of the Kobayakawa Patent is and has been knowing, deliberate, and willful. IDT learned of its infringement of the Kobayakawa Patent no later than March 26, 2020. As detailed above, Bell Semic sent an email to IDT on March 26, 2020, identifying the Kobayakawa Patent as being infringed by the exemplary Kobayakawa Accused Products. Despite these efforts, and knowing that it was willfully infringing the Kobayakawa Patent, IDT continued, and continues, to commit acts of direct and indirect infringement despite

knowing its actions constitute infringement of the valid and enforceable Kobayakawa Patent, despite a risk of infringement that was known or so obvious that it should have been known to IDT, and/or even though IDT otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, IDT's conduct is and has been egregious. IDT's knowing, deliberate, and willful infringement of the Kobayakawa Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Plaintiff prays for the following relief:

A. A judgment that IDT has infringed one or more claims of the Asserted Patents;

B. An award of damages resulting from IDT's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order requiring IDT to provide accountings and to pay supplemental damages to Bell Semic, including, without limitation, prejudgment and post-judgment interest;

D. A judgment and order finding that IDT's acts of infringement were willful and egregious and trebling damages under 35 U.S.C. § 284;

E. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Bell Semic its reasonable attorneys' fees against IDT;

F. A permanent injunction enjoining IDT and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in active concert or participation with IDT, from infringing the Asserted Patents;

G. If a permanent injunction preventing further infringement of the Asserted Patents is not granted, a compulsory ongoing licensing fee for any such further infringement; and

H. Any and all other relief to which Bell Semic may show itself to be entitled.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Dated: March 30, 2020

Respectfully submitted,

FARNAN LLP

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