IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff -against- ACER INC., ACER AMERICA CORPORATION, MEDIATEK INC., MEDIATEK USA INC., and FUZHOU ROCKCHIP ELECTRONICS CO., LTD., Defendants.	Civil Action No.: 6:20-cv-00419 **Jury Trial Demanded**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO"), for its First Amended Complaint against Defendants Acer Inc. and Acer America Corporation (collectively "Acer"), Mediatek Inc., and Mediatek USA Inc. (collectively "Mediatek"), and Fuzhou Rockchip Electronics Co., Ltd. ("Rockchip"), (collectively "Defendants") hereby alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. On information and belief, Defendant Acer Inc. is a corporation organized under the laws of Taiwan, with a principal place of business at 1F, 88, Sec. 1, Xintai 5th Rd., Xizhi, New Taipei City 221, Taiwan.

3. On information and belief, Defendant Acer America Corporation is a California corporation with its principal place of business located at 333 W. San Carlos Street, Suite 1500,

San Jose, CA 95110.

4. On information and belief, Defendant Mediatek Inc. is a Taiwanese company incorporated under the laws of Taiwan, with its principal place of business at No.1, Dusing 1st Rd., Hsinchu Science Park, Hsinchu, 30078, Taiwan.

5. On information and belief, Defendant Mediatek USA Inc. is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business at 96 Corporate Park, Irvine, CA 92606.

6. On information and belief, Defendant Rockchip is a Chinese company organized and existing under the laws of China, with its principal place of business at No.18 Building, A District, Fuzhou Software Park, 89 Soft Avenue, Tongpan Road, Gulou District, Fuzhou, Postal Code 350003, People's Republic of China.

JURISDICTION AND VENUE

7. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Defendants of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

8. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. Acer Inc. is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) Acer Inc. sells and offers for sale its products in Texas, (ii) Acer Inc. sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) Acer Inc. places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. For example, Acer Inc. sells its products including its chromebooks and tablets (directly or through agents) in Texas and/or to residents of Texas. In addition, or in the alternative, this Court has personal jurisdiction over Acer Inc. pursuant to Fed. R. Civ. P. 4(k)(2).

10. Acer America Corporation is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) Acer America Corporation sells and offers for sale its products in Texas, (ii) Acer America Corporation sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) Acer America Corporation places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. For example, Acer America Corporation sells its products including its chromebooks and tablets (directly or through agents) in Texas and/or to residents of Texas.

11. Mediatek Inc. is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, independently and/or via its agents, (i) Mediatek Inc. sells and offers for sale its products in Texas, (ii) Mediatek Inc. sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) Mediatek Inc. places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. For example, Mediatek Inc. sells its systems on chip (SoCs) to Acer and other tablet manufacturers with knowledge and intent that the products incorporating those SoCs would be sold in Texas and/or residents of Texas. In addition, or in the alternative, this Court has personal jurisdiction over Mediatek Inc. pursuant to Fed. R. Civ. P. 4(k)(2).

12. Mediatek USA Inc. is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, independently and/or via its agents, (i) Mediatek USA Inc. has a place of business at 5914 West Courtyard Drive, Austin, Texas 78730; (ii) Mediatek USA Inc. sells and offers for sale its products in Texas, (iii) Mediatek USA Inc. sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iv) Mediatek USA Inc. places its products in the stream of commerce with intent or knowledge that those products

would end up in Texas. For example, Mediatek USA Inc. sells systems on chip (SoCs) to Acer and other tablet manufacturers with knowledge and intent that the products incorporating those SoCs would be sold in Texas and/or residents of Texas.

13. Rockchip is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, independently and/or via its agents, (i) Rockchip sells and offers for sale its products in Texas, (ii) Rockchip sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) Rockchip places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. For example, Rockchip sells its systems on chip (SoCs) to Acer and other tablet manufacturers with knowledge and intent that the products incorporating those SoCs would be sold in Texas and/or residents of Texas. In addition, or in the alternative, this Court has personal jurisdiction over Rockchip pursuant to Fed. R. Civ. P. 4(k)(2).

14. Venue is proper as to Acer Inc. in this District under 28 U.S.C. § 1391(c) because Acer Inc. is a foreign corporation.

15. Venue is proper as to Acer America Corporation in this District under 35 U.S.C. § 1400(b) because Acer America Corporation operates a regular and established place of business, which includes at least a repair and service facility within the Western District of Texas located at 1394 Eberhardt Rd, Temple, Texas 76504 and commits acts of infringement in this judicial district.

16. Venue is proper as to Mediatek Inc. in this District under 28 U.S.C. § 1391(c) because Mediatek Inc. is a foreign corporation.

17. Venue is proper as to Mediatek USA Inc. in this District under 35 U.S.C. § 1400(b) because Mediatek USA Inc. operates a regular and established place of business within the

Western District of Texas located at 5914 West Courtyard Drive, Austin, Texas 78730 and commits acts of infringement in this judicial district.

18. Venue is proper as to Rockchip in this District under 28 U.S.C. § 1391(c) because Rockchip is a foreign corporation.

BACKGROUND

19. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

20. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

21. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

22. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

23. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

24. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

25. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

26. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and

Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

27. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

28. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

29. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

30. By letter dated May 22, 2019, CCO notified Mediatek of the existence of the '234, '386, '069, and '603 Patents, and of infringement of the Patents-in-Suit by Acer. CCO's letter identified exemplary infringing Mediatek products and an exemplary infringed claim for each of the '234, '386, '069, and '603 Patents. CCO's May 22, 2019 letter invited Mediatek to hold a licensing discussion with CCO.

31. CCO's licensing discussion with Mediatek reached an impasse.

32. By letter dated June 21, 2019, CCO notified Acer of the existence of the '234, '386, '069, and '603 Patents, and of infringement of the Patents-in-Suit by Acer. CCO's letter identified exemplary infringing Acer products and an exemplary infringed claim for each of the '234, '386, '069, and '603 Patents. CCO's June 21, 2019 letter invited Acer to hold a licensing discussion with CCO.

33. CCO's licensing discussion with Acer reached an impasse.

34. By letter dated April 30, 2019, CCO notified Rockchip of the existence of the '234, '386, '069, and '603 Patents, and of infringement of the Patents-in-Suit by Rockchip. CCO's letter identified exemplary infringing Rockchip products and an exemplary infringed claim for each of

the ’234, ’386, ’069, and ’603 Patents. CCO’s April 30, 2019 letter invited Rockhip to hold a licensing discussion with CCO. Not having received a response to the April 30, 2019 letter and unable to confirm the receipt by Rockchip, On November 20, 2019, CCO sent an email to Rockchip’s CEO and to the general service email address, attaching the April 30, 2019 letter and advising it of the possibility of having a licensing discussion. To date, CCO has not received a response from Rockchip.

35. Acer, Mediatek, and Rockchip have also been on notice of the Patents-in-Suit and of their infringement of the Patents-in-Suit as of the date of the original complaint in this action.

LICENSING

36. As of the time of this complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, Qualcomm, and VIA Technologies.

COUNT I: INFRINGEMENT OF THE ’234 PATENT

37. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

38. On information and belief, Defendants have infringed the ’234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States Acer tablets, including Acer Chromebook R13, Iconia One 7, Iconia One 10, and other devices using Mediatek Systems-on-Chip (“SoC”) and Mediatek SoC’s themselves (including, for example, Helio X30, Helio X27, Helio X25, Helio X23, Helio X20, Helio P90, Helio P70, Helio P60, Helio P35, Helio P30, Helio P25, Helio P23, Helio P22, Helio P20, Helio P18, Helio P10, Helio A22, MT6753, MT6752, MT6750, MT6739, MT6738, MT6737T, MT6737, MT6735, MT6732, MT6731, MT6595, MT6592, MT8176, MT8173, MT8167A, MT8167B, MT8163V/A, MT8163V/B, MT8127, MT8785, MT8783, MT8735D, MT8735B, MT8735P, MT8735M, and MT8321 SoCs), as well as Acer Chromebook Tab 10, and other devices using Rockchip SoCs and Rockchip SoC’s

themselves (including for example, RK3399Pro, RK3399, RK3326, RK3328, RK3288, RK3229, RK3188, RK3128, RK3126, RV1108, PX30, and PX5 series SoCs) (collectively "Accused Products"), that include a DDR3, DDR4, LPDDR3, LPDDR4, and/or LPDDR4x controller ("DDR Controller").

39. On information and belief, Defendants have infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Products. For example, on information and belief, Defendants have infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Products that include the DDR Controller with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Products and specifically the DDR Controller. For example, the Acer Chromebook R13 includes Mediatek SoCs, such as the MT8173C. *See* Ex. 1, Screenshot from Acer Website for Chromebook R13 (showing Chromebook R13 SoC part numbers, including MediaTek M8173C processor). As another example, the Acer Chromebook Tab 10, includes Rockchip SoCs, such as RK3399. *See* Ex. 2, Screenshot from website for Chromebook Tab 10 (showing Chromebook Tab 10 product details, including the RK3399 Rockchip processor). Mediatek SoCs include memory controllers, such as LPDDR3/4 memory controllers, with a timing uncertainty reduction system for calibration of a high speed communication apparatus. *See* Ex. 3, MediaTek MT6757 LTE-A Smartphone Application Processor Technical Brief Version 1.3 at pp. 8 and 18 (showing functionality of LPDDR3/4 memory controllers). Similarly, Rockchip SoCs include LPDDR4 and LPDDR3 Dynamic Memory Interface (DMC) with a timing uncertainty reduction system for calibration of

a high speed communication apparatus. *See* Ex. 4, Rockchip RK3399 TRM Revision 1.3 December 2016, p. 540 (showing architecture of memory controller). For example, LPDDR4/4x memory controllers include a system for reducing timing uncertainty in LPDDR4/4x memory transmission, including calibration using Multi-Purpose Commands and Registers, read centering, write centering and write leveling. *See* Ex. 5, MediaTek MT6737 LTE Smartphone Application Processor Functional Specification Version 1.0 at p. 116 (describing a feature that supports input DQS/DQ timing calibration for PVT variation); *see also* Ex. 6, JEDEC Standard, LPDDR4, JESD209-4B, February 2017 at pp. 26, 190 and 195 (describing write leveling, MPC Read Calibration, RD DQ Calibration, and DQS-DQ training for center-aligning); *see also* Ex. 7, JEDEC Standard, LPDDR3, JESD209-3C, August 2015 at pp. 61 and 68 (describing write-leveling mode and DQ Calibration); *see also* Ex. 4 at pp. 539-540 (describing Rockchip's Dynamic Memory Interface, including the DDR Controller handling of training and calibration). The DDR Controller of the Accused Products comprises at least one driving register for latching transmitted DQ signals, with a plurality of input and outputs. The DDR Controller of the Accused Products further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. The DDR Controller of the Accused Products includes a main clock for generating a main clock signal (such as the MC Clock). *See* Ex. 8, DDR PHY Interface, DFI 4.0 Specification, April 2018 at p. 120 (noting that the "MC clock is always the DFI clock and all DFI signals are referenced from the MC clock."); *see also* Ex. 4 at pp. 539, 888 (discussing a controller clock). Mediatek's LPDDR4/4x and LPDDR3 memory controllers and Rockchip's LPDDR4 and LPDDR3 DMCs include a reference clock for generating a reference signal for calibrating the receiving register or registers, and the reference clock is associated with the main clock signal. For example, LPDDR4/4x and LPDDR3 memory

controllers and LPDDR4 and LPDDR3 DMCs in the Accused Products include a reference clock, such as an internal clock or a PHY clock, for generating a reference signal for calibrating and receiving register or registers, such as during DQ read centering/read training, and the reference clock is associated with the main clock signal. *See* Ex. 5 at pp. 116-117 (showing Mediatek memory controller calibration examples and clocks); *see also* Ex. 4 at pp. 540, 888 (showing Rockchip calibration examples); *see also* Ex. 6 at pp. 190, 195; *see also* Ex. 9, DDR PHY Interface, DFI 3.1 Specification, March 2014 at p. 93 (discussing MC clock). The DDR Controller of the Accused Products includes phase shift circuitry to align the timing of the driving signals relative to the CK signal at the destination. For example, the phase shift circuitry aligns the timing of the DQS signals via write leveling. *See* Ex. 6 at p. 186 ("To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); *see also* Ex. 7 at p. 68; *see also* Ex. 4 at p. 539 (discussing training and calibration).

40. On information and belief, Defendants have induced, and continue to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, their customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products that incorporate DDR Controllers. Defendants had knowledge of the '234 Patent and acted with specific intent to encourage their customers and end users to make, use, sell, and/or offer to sell in the United States and/or import

into the United States the infringing instrumentalities described above, including by providing the Accused Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

41. On information and belief, Defendants have committed the foregoing infringing activities without a license.

42. On information and belief, Defendants' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

43. On information and belief, Defendants knew the '234 Patent existed, knew of an exemplary infringed claim of the '234 Patent, and knew of exemplary infringing Accused Products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT II: INFRINGEMENT OF THE '386 PATENT

44. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

45. On information and belief, Defendants have infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Products.

46. For example, on information and belief, Defendants have infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused Products, which include a DDR Controller, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. For example, the Acer Chromebook R13 includes a Mediatek SoC, such as the MT8173C, which includes a LPDDR3 controller, an apparatus adapted to send a plurality of memory transmissions over a memory bus to a memory having a plurality of memory banks. *See* Ex. 1 (showing

Chromebook R13 components, including a Mediatek M8173C processor).[1] *see also* Ex. 5 at pp. 112-116 (showing the functionality of LPDDR3/4 memory controllers and showing that Mediatek's DDR Controllers are adapted to send a plurality of memory transactions over a memory bus). Similarly, the Acer Chromebook Tab 10 includes a Rockchip SoC, such as the RK3399, which includes a Dynamic Memory Interface, which is an apparatus adapted to send a plurality of memory transactions, such as read requests, to the memory. *See* Ex. 2 (showing the product details for Acer Chromebook Tab 10, including a Rockchip RK3399 processor); *see also* Ex. 4 at p. 28 (showing External Memory Interface, including DDR3/DDR3L/LPDDR3/ LPDDR4). Exemplary DDR Memory to which the Mediatek DRAM Controller connects has multiple memory banks. *See* Ex. 5 at p. 116 (". . . are used to select the bank and row to be accessed."); *see also* Ex. 7 at p. 16 (evidencing multiple memory banks). Similarly, in the Acer Chromebook Tab 10, the memory, to which the Dynamic Memory Interface connects has multiple memory banks. *See* Ex. 7 at p. 16 (evidencing multiple memory banks). The Accused Acer Products send the requests over a memory bus. *See, e.g.*, See Ex. 5 at p. 114 ("DRAM bus signals"); *see also* Ex. 4 at p. 12 ("maximizing bus utilization"). The DDR Controller of the Accused Products comprises a queue comprising a plurality of request stations for storing memory transactions, such as read requests. *See* Ex. 5 at p. 117 (command FIFO); *see also* Ex. 10, Cadence FD-SOI: Ecosystem and IP Design at p. 16 (command Queue). Each of the memory transactions is addressed to one of the memory banks. *See* Ex. 7 at p. 16 (showing requests addressed to one of the memory banks). The DDR Controller includes an arbiter that is simultaneously coupled to each of the request stations and adapted to select any of the memory transactions. *See* Ex. 5 at pp. 116-117 (the DDR Controller comprising an arbiter including for

[1] Mediatek provides details as to the functionality of its memory controllers in, for example, the MT6737 and MT6757 technical documents.

example, Scheduler A, Schedule B, and/or Timing controller); *see also* Ex. 10 at p. 16 (showing that the DDR Controller comprises an arbiter that includes the Look Ahead Optimization feature). The arbiter is configured to generate a plurality of bank readiness signals. For example, the arbiter generates a readiness signal following the issuance of an Activate command that indicates the readiness of a memory bank to accept a memory transaction, such as a read request. *See* Ex. 5 at p. 117; *see also* Ex. 7 at pp. 16, 38-39 (describing the ACTIVE command and burst read operation to LPDDR3 SDRAM)); *see also* Ex. 11, DDR4: Double the Speed, Double the Latency? Marc Greenberg - Cadence (discussing that the memory controller "will include look-ahead queue or pipeline for upcoming transactions to allow the memory controller to prepare the DRAM for transactions in the pipeline"). The DDR Controller, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *See* Ex. 5 at pp. 116-117 (describing that bus scheduler deciding which command is issued); *see also* Ex. 12, Design IP Brochure: Denali Controller IP for DDR at p. 2 (showing that the RK3399 DDR Controller's arbiter look-ahead optimization); *see also* Ex. 7 at pp. 16, 38-39 (showing the Activate Command applied before a READ or WRITE operation can be executed); *see also* Ex. 13, Cadence Blog: Squeeze Bandwidth Inefficiencies out of DDR DRAMS in Memory Subsystem Designs (showing lookahead optimization); *see also* Ex. 4 at p. 12 ("Advanced command reordering and scheduling to maximize bus utilization").

47. On information and belief, Defendants have induced, and continue to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, their customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products. Defendants had knowledge of the '386

Patent and acted with specific intent to encourage their customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

48. On information and belief, Defendants have committed the foregoing infringing activities without a license.

49. On information and belief, Defendants' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

50. Defendants knew the '386 Patent existed, knew of its claims, and knew of Defendants' infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT III: INFRINGEMENT OF THE '069 PATENT

51. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

52. On information and belief, Defendants have infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Products.

53. For example, on information and belief, Defendants have infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and verification of the Accused Products, which include the DDR Controller, such as a LPDDR4/4x or LPDDR3 memory controller that automatically calibrates skew of LPDDR4/4x or LPDDR3 DDRs. *See* Ex. 1 (showing that Acer Chromebook R13 includes Mediatek SoC, such as the MT8173C); *see also* Ex. 2 (showing the Acer Chromebook Tab 10 product details,

including an RK3399 Rockchip processor); *see also* Ex. 3 at pp. 8, 18 (showing that Mediatek SoCs include LPDDR3 and LPDDR4/4x memory controllers that automatically calibrate skew of LPDDR3 and LPDDR4/4x systems, by including a transmitter that sends CK and DQS signals to a receiver on LPDDR3 or LPDDR4/4x memory); *see also* Ex. 4 at pp. 539, 540, 868 (showing that Rockchip SoCs include an LPDDR4 and LPDDR3 Dynamic Memory Interface (DMC) that performs a method for automatic skew calibration of LPDDR4 or LPDDR3 systems, by including a transmitter that sends CK and DQS signals, and receivers on LPDDR3/4 memory controllers system); *see also* Ex. 6 at p. 26 (showing LPDDR4/4x memory controller systems include write training feature, including write leveling); *see also* Ex. 7 at p. 68 (showing LPDDR3 write training); *see also* Ex. 5 at p. 116 (showing DQS/DQ timing calibration); *see also* Ex. 9 at pp. 119-120 (showing PHY write leveling); *see also* Ex. 8 at p. 157 (showing PHY write leveling). The DDR Controllers of the Accused Products calibrate registers of the receiver in relation to a reference clock. For example, LPDDR4/4x and LPDDR3 memory controllers calibrate receiving registers of the PHY in relation to a reference clock edge, such as during initialization. The PHY comprises a transmitter and the receiver. Defendants calibrate registers of the receiver, such as the PHY registers in relation to a reference clock edge, such as a PHY clock. *See* Ex. 5 at p. 116-117 (showing PHY and DQS edges); *see also* Ex. 4 at pp. 539-540, 888 (Rockchip DMC calibration examples and clocks). Defendants calibrate propagation delays of registers of the transmitter, using the calibrated registers of the receiver with the Write Leveling feature. For example, LPDDR4/4x memory controllers calibrate delays of DQS registers of the memory controller, by, for example using calibrated registers of the receiver, such as the PHY or interface registers calibrated to receive the samples of CK_t-_CK_c during write leveling. *See* Ex. 6 at p. 186 ("To improve signal-integrity performance, the LPDDR4

SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair"); *see also* Ex. 7 at p. 68; *see also* Ex. 4 at p. 540 (showing that DCMs calibrate the propagation delays of DQS registers of the memory controllers). The calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS_t-DQS-c and CK_t-CK_c signals. The calibration is performed for a plurality of data patterns, such as DQS_t – DQS_c patterns with variable delays. *See* Ex. 6 at p. 186 ("5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings. 6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established."); *see also* Ex. 7 at p. 68 (showing that LPDDR3 DMCs take measurements for a plurality of data patterns); *see also* Ex. 4 at p. 868 (discussing delay needed for tDQSCK). Defendants apply the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See* Ex. 6 at p. 186 (showing that LPDDR4/4x memory controllers apply the measured time offset (DQS delay) to compensate for the inter-signal skew by aligning the DQS and CK signals); *see also* Ex. 7 at p. 68 (showing same for the LPDDR3 standard); *see also* Ex. 9 at pp. 115-116 ("The DFI training requires the MC to support the training sequences to the PHY by generating MRW commands, toggling the enable parameter, generating appropriate strobe signals, and evaluating the response"); *see also* Ex. 8 at pp. 144-145.

54. On information and belief, Defendants have induced, and continue to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly

inducing, directing, causing, and encouraging others, including, but not limited to, their customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products that incorporate the DDR Controller. Defendants had the knowledge of the '069 Patent and acted with specific intent to encourage their customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

55. On information and belief, Defendants have committed the foregoing infringing activities without a license.

56. On information and belief, Defendants' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

57. On information and belief, Defendants knew the '069 Patent existed, knew of an exemplary infringed claim of the '069 Patent, and knew of exemplary infringing Defendants' products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT IV: INFRINGEMENT OF THE '603 PATENT

58. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

59. On information and belief, Defendants have infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Products.

60. For example, on information and belief, Defendants have infringed at least claim 14 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including

during development, design, testing, and verification of the Accused Products. The DDR Controller of the Accused Products use a multiplexer. *See* Ex. 1 (showing Chromebook R13 SoC part numbers, including MediaTek M8173C processor, and LPDDR3 memory); *see also* Ex. 5 at pp. 112-113, 117 (for example, showing a multiplexer); *see also* Ex. 2 (showing Chromebook Tab 10 SoC part numbers, including RK3399 Rockchip Processor, which include memory controllers and perform a method of using a multiplexer); *see also* Ex. 4 at p. 28 (showing, for example, the RK3399 includes Dynamic Memory Interface, which is an apparatus adapted to send a plurality of memory transactions, such as read requests, to the memory) and at pp. 539, 542 (showing that the Dynamic Memory Interface comprises a Cadence Denali DDR controller); *see also* Ex. 12 (showing that the Dynamic Memory Interface comprises a Cadence Denali DDR IP controller); *see also* Ex. 10 at p. 16 (showing that the DDR controller comprises a multiplexer). Memory to which the Accused Products connect has multiple memory banks. *See e.g.,* Ex. 7 at p. 16 (evidencing multiple memory banks). The multiplexer used by the DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions. *See* Ex. 5 at pp. 116-117 (receiving a plurality of memory transactions (such as read or write transactions) on the inputs of the multiplexer discussed above); *see also* Ex. 10 at p. 16 (showing multiple ports). The multiplexer also comprises a multiplexer output for sending each of the plurality of memory transactions to the memory, such as the interface to the DDR PHY. See Ex. 5 at pp. 112-113 (showing the DDR Controller outputting transactions to LPDDR3); *see also* Ex. 10 at p. 16 (DDR Controller's connection to PHY, External memory, such as LPDDR3, among others). The Accused Products receive a plurality of memory transactions at the multiplexer inputs. Each of the memory transactions is addressed to a corresponding memory bank. *See* Ex. 5 at 116-117 (". . . READ and WRITE command are used

to select the bank and the starting column location for the burst access."); *see also* Ex. 7 at p. 16 ("The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.") The DDR Controller associates a priority with each received memory transaction. *See* Ex. 5 pp. 112-113 ("There are plenty of schedule options to schedule the command, which are: . . . • High priority"); *see also* Ex. 12 (e.g., Round Robin, Priority Bandwidth, Weighted Round Robin). The DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as following the submission of activate commands to the LPDDR3 memory. *See* Ex. 5 at pp. 116-117 (For example, the DDR Controller generates a readiness signal following the issuance of an Activate command that indicates the readiness of a memory bank to accept a memory transaction); *see also* Ex. 13 (showing that the DK3399 DDR Controller generates a plurality of bank readiness signals following the issuance of an Activate command); Ex. 7 at pp. 16, 38-39 (describing Activate command and Burst Read Operation). The bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. *See id.* The DDR Controller sends each of the plurality of memory transactions to its corresponding memory bank via the DRAM PHY based on the associated priorities and the bank readiness signals. *See* Ex. 5 at pp. 116-117 (The sequence and timing of sending each of the transactions is based on the assigned priorities and the bank readiness signals); *see also* Ex. 4 at p. 12 (showing that in the RK3399 DDR Controller, for example, the sequence and timing of sending each of the transactions is based on the assigned priorities and the bank readiness signals); *see also* Ex. 13 (readiness signals);); *see also* Ex. 12 at p. 2 (showing Look-Ahead Optimization); *see also* Ex. 11 (same).

61. On information and belief, Defendants have induced, and continue to induce, infringement of the ’603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, their customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, Accused Products. Defendants had the knowledge of the ’603 Patent and acted with specific intent to encourage their customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

62. On information and belief, Defendants have committed the foregoing infringing activities without a license.

63. On information and belief, Defendants’ infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

64. Defendants knew the ’603 Patent existed, knew of its claims, and knew of Defendants’ infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’603 Patent.

COUNT V: INFRINGEMENT OF THE ’021 PATENT

65. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

66. On information and belief, Defendants have infringed the ’021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Products.

67. For example, on information and belief, Defendants have infringed at least claim 11 of the ’021 Patent by performing a method of eliminating skew caused by inter-symbol interference

and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the Accused Products, including during regular operation and during development, design, testing, and verification of the Accused Products. *See* Ex. 2, (showing the Acer Chromebook Tab 10 product details, including an RK3399 Rockchip processor); s*ee also* Ex. 4 at p. 540 (showing architecture of memory controller); Ex. 6, p. 195. The DDR Controller continuously transmits data through each DQ transmission line during centering and link training. *See id.* ("Up to 5 consecutive MPC [Write DQ FIFO] command with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command.") The DDR Controller measures a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. *See id.* ("After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC][Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed."). The DDR Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. *See id.* The DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. *See id.*; *see also id*. at 200.

68. On information and belief, Defendants have induced, and continue to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, their

customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products that incorporate the DDR Controller. Defendants had the knowledge of the '021 Patent and acted with specific intent to encourage their customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

69. On information and belief, Defendants have committed the foregoing infringing activities without a license.

70. On information and belief, Defendants' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Defendants, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against Defendants on all counts;

B. Entry of judgment that Defendants have infringed the Patents-in-Suit;

C. Entry of judgment that Defendants' infringement of the '234, '386, '069, and '603 Patents has been willful;

D. An order permanently enjoining Defendants from infringing the Patent-in-Suit

E. Award of compensatory damages adequate to compensate CCO for Defendants' infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

F. Award of CCO's costs;

G. Pre-judgment and post-judgment interest on CCO's award; and

H. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Dated: May 30, 2020

Respectfully submitted,

/s/ Raymond W. Mort, III

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