HOGAN LOVELLS US LLP
Krista S. Schwartz (Bar No. 303604)
Patrick T. Michael (Bar No. 169745)
Helen Y. Trac (Bar No. 285824)
Gurtej Singh (Bar No. 286547)
Madeleine Bech (Bar No. 328778)
3 Embarcadero Center, Suite 1500
San Francisco, California 94111
Telephone: (415) 374–2300
Facsimile: (415) 374–2499
krista.schwartz@hoganlovells.com
patrick.michael@hoganlovells.com
helen.trac@hoganlovells.com
tej.singh@hoganlovells.com
madeleine.bech@hoganlovells.com

Aaron S. Oakley (*pro hac vice* forthcoming)
1601 Wewatta Street, Suite 900
Denver, Colorado 80202
Telephone: (303) 899–7300
Facsimile: (303) 899–7333
aaron.oakley@hoganlovells.com

Attorneys for Plaintiff
SYNOPSYS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SYNOPSYS, INC.,

Plaintiff,

v.

AVATAR INTEGRATED SYSTEMS, INC.,

Defendant.

Case No. 3:20-cv-04151-SK

"CORRECTED" COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Synopsys, Inc. ("Synopsys") submits the following Complaint against Defendant Avatar Integrated Systems, Inc. ("Avatar") for infringement of U.S. Patent No. 8,407,640 ("the '640 Patent"); U.S. Patent No. 7,103,863 ("the '863 Patent"); U.S. Patent No. 7,546,567 ("the '567 Patent"); U.S. Patent No. 7,853,915 ("the '915 Patent"); U.S. Patent No. 8,234,614 ("the '614 Patent"); and U.S. Patent No. 8,407,655 ("the '655 Patent") (collectively, the "Patents-in-Suit").

NATURE OF THE ACTION

1. Synopsys is a leader in the electronic design automation ("EDA") and semiconductor intellectual property industry. It develops, manufactures, sells and licenses products and services that enable designers to create, model and verify complex integrated circuit ("IC") designs from concept to silicon. Since 1986, engineers around the world have used Synopsys technology to design and create billions of integrated circuits and systems.

2. Synopsys' IC Compiler and IC Compiler II products (collectively, "IC Compiler") provide customers with a comprehensive place-and-route system that, among other things, determines where each gate should be located on the physical chip (the placement portion of place-and-route), and routes wires between different elements on the chip while minimizing wire delay (the route portion of place-and-route). Along with placement and routing, IC Compiler also handles clock tree synthesis, power routing, and block level floorplanning. IC Compiler also contains static timing technology which computes the expected timing of a digital circuit without requiring simulation.

3. Synopsys has a separate, timing sign-off tool, PrimeTime, that also computes the expected timing of a digital circuit without requiring simulation. Among other things, PrimeTime provides customers with a trusted solution for timing sign-off, a required verification step before manufacturing of an integrated circuit chip. Synopsys' IC Compiler and PrimeTime products are tightly correlated (*i.e.* the timing engines of these two products are correlated to produce closely matched timing results) because Synopsys uses some of the same proprietary static timing technology in both products.

4. Avatar describes itself as a leading software company in the Electronic Design

Automation (EDA) industry focused on physical design implementation. Avatar's Aprisa and Apogee products compete with certain Synopsys products, including IC Compiler and PrimeTime.

5. Avatar acquired certain assets from ATopTech, Inc. ("ATopTech") pursuant to an April 18, 2017 Asset Purchase Agreement entered into in connection with ATopTech's Chapter 11 bankruptcy case, Case No. 17–10111–MFW (Del.). Among other things, Avatar acquired the Aprisa and Apogee products from ATopTech, including source code, product documentation, and the Aprisa / Apogee JIRA issue tracking and product management system and history.

6. On May 25, 2020, concerned that Avatar was improperly using Synopsys' intellectual property, counsel for Synopsys wrote to Avatar and requested the opportunity to conduct an inspection of the most recent version of Avatar's Aprisa product in order to resolve Synopsys' concerns. In its May 29, 2020 responsive letter, counsel for Avatar ignored Synopsys' request to conduct an inspection.

7. As a result, Synopsys has no choice but to seek judicial relief. Avatar's Aprisa product infringes Synopsys' patents and unfairly competes with and trades on Synopsys' industry leading EDA tools. Accordingly and as more specifically alleged herein, Synopsys brings this suit for federal patent infringement.

THE PARTIES

8. Synopsys is a corporation organized under Delaware law with its principal place of business in Santa Clara County at 690 East Middlefield Road, Mountain View, California 94043.

9. On information and belief, Avatar is a corporation organized under Delaware law with its principal place of business in Santa Clara County at 2111 Tasman Drive, Santa Clara, California 95054. Avatar also claims to have offices in Japan, Taiwan, Korea, and India.

JURISDICTION AND VENUE

10. This action arises in part under the patent laws of the United States, 35 U.S.C. § 100, *et seq.* This Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338.

11. Avatar is subject to this Court's specific and general personal jurisdiction pursuant

to due process and/or the California Long Arm Statute because (1) it is incorporated in the State of California and has its principal place of business within this judicial district, and (2) has substantial business within this State and judicial district, including at least part of its infringing activities alleged herein and regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale and sold, as well as services provided to California residents.

12. Venue in this judicial district is appropriate under 28 U.S.C. §§ 1391 and 1400. Venue is proper in this judicial district because, among other things, (1) Avatar has a regular and established place of business in this judicial district, and (2) a substantial part of the events or omissions which give rise to the claims herein occurred in Santa Clara County, California.

INTRADISTRICT ASSIGNMENT

13. This is an intellectual property action and is assigned on a district-wide basis under Civil Local Rule 3-2(c) and General Order No. 44.

SYNOPSYS INTELLECTUAL PROPERTY

14. As a world leader in EDA, Synopsys is helping the electronics market innovate smarter, connected and more secure technology in all aspects of semiconductor design, verification, IP integration, and application security testing. Synopsys provides a complete front-to-back design and test environment, software-level to silicon-level verification, design reuse technology, field-programmable gate array solutions, and professional services to help its customers get their silicon working quickly and accurately. These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. Since 1986, engineers around the world have used Synopsys technology to design and create billions of integrated circuits and systems.

15. To address the important issue of timing in integrated circuit designs, Synopsys spent years investing in and developing PrimeTime – its proprietary static timing analysis ("STA") tool that computes the expected timing of a digital circuit without requiring simulation – and provides customers with a trusted solution for timing sign-off, a required verification step before manufacturing. PrimeTime is a successful product and is widely used for gate-level static

timing analysis.

16. To address the need for a place-and-route solution that delivers quality of results for next generation integrated circuit designs, Synopsys spent years investing in and developing the IC Compiler products.

17. Synopsys has developed novel techniques and technologies related to integrated circuit design, testing, and verification, which are protected by numerous U.S. Patents.

18. U.S. Patent No. 8,407,640, entitled "Sensitivity-Based Complex Statistical Modeling for Random On-Chip Variation," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on March 26, 2013. Synopsys is the assignee and holder of all rights, title, and interests in the '640 Patent, including without limitation all rights to sue for damages for infringement thereof. A true and correct copy of the '640 Patent is attached hereto as Exhibit 1.

19. U.S. Patent No. 7,103,863, entitled "Representing the design of a sub-module in a hierarchical integrated circuit design & analysis system," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on September 5, 2006. Synopsys is the assignee and holder of all rights, title, and interests in the '863 Patent, including without limitation all rights to sue for damages for infringement thereof. A true and correct copy of the '863 Patent is attached hereto as Exhibit 2.

20. U.S. Patent No. 7,546,567, entitled "Method and apparatus for generating a variation-tolerant clock-tree for an integrated circuit chip," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on June 9, 2009. Synopsys is the assignee and holder of all rights, title, and interests in the '567 Patent, including without limitation all rights to sue for damages for infringement thereof. A true and correct copy of the '567 Patent is attached hereto as Exhibit 3.

21. U.S. Patent No. 7,853,915, entitled "Interconnect-driven physical synthesis using persistent virtual routing," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on December 14, 2010. Synopsys is the assignee and holder of all rights, title, and interests in the '915 Patent, including without limitation all rights to sue for damages for

infringement thereof. A true and correct copy of the '915 Patent is attached hereto as Exhibit 4.

22. U.S. Patent No. 8,234,614, entitled "Multi-threaded global routing," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on July 31, 2012. Synopsys is the assignee and holder of all rights, title, and interests in the '614 Patent, including without limitation all rights to sue for damages for infringement thereof. A true and correct copy of the '614 Patent is attached hereto as Exhibit 5.

23. U.S. Patent No. 8,407,655, entitled "Fixing design requirement violations in multiple multi-corner multi-mode scenarios," was duly and legally issued by the U.S. Patent and Trademark Office ("USPTO") on March 26, 2013. Synopsys is the assignee and holder of all rights, title, and interests in the '655 Patent, including without limitation all rights to sue for damages for infringement thereof. A true and correct copy of the '655 Patent is attached hereto as Exhibit 6.

COUNT I: INFRINGEMENT OF THE '640 PATENT

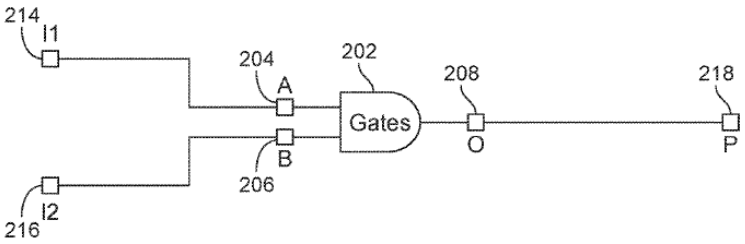
24. Synopsys incorporates paragraphs 1–23 as if fully set forth herein.

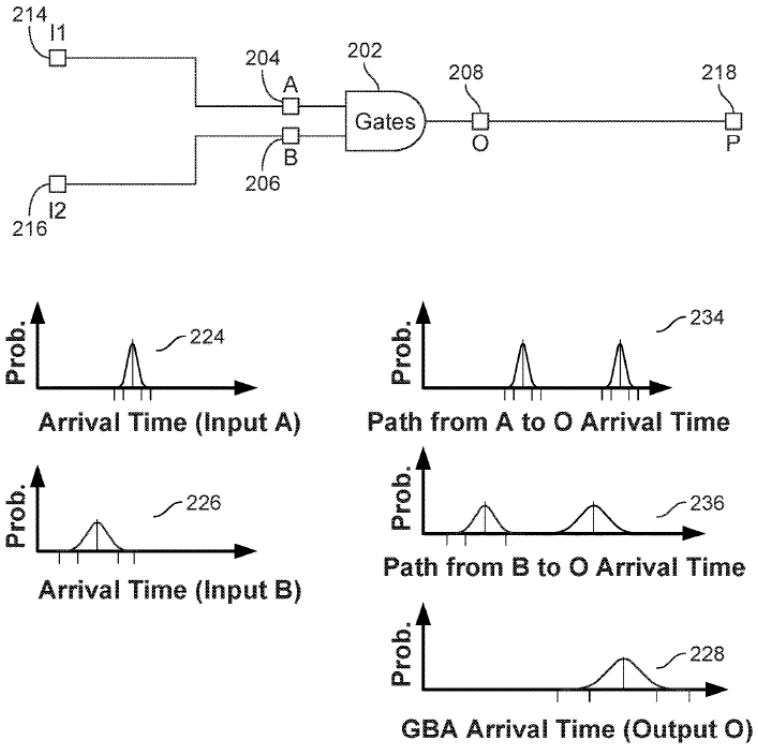
25. On information and belief, Avatar and/or users of the Avatar Aprisa software product have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '640 Patent by making, using, offering to sell, and/or selling Aprisa within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

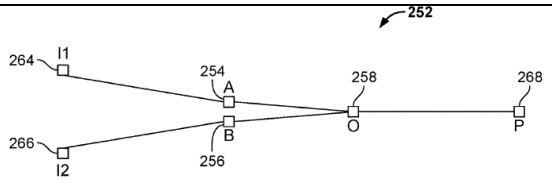
26. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '640 Patent against Aprisa. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

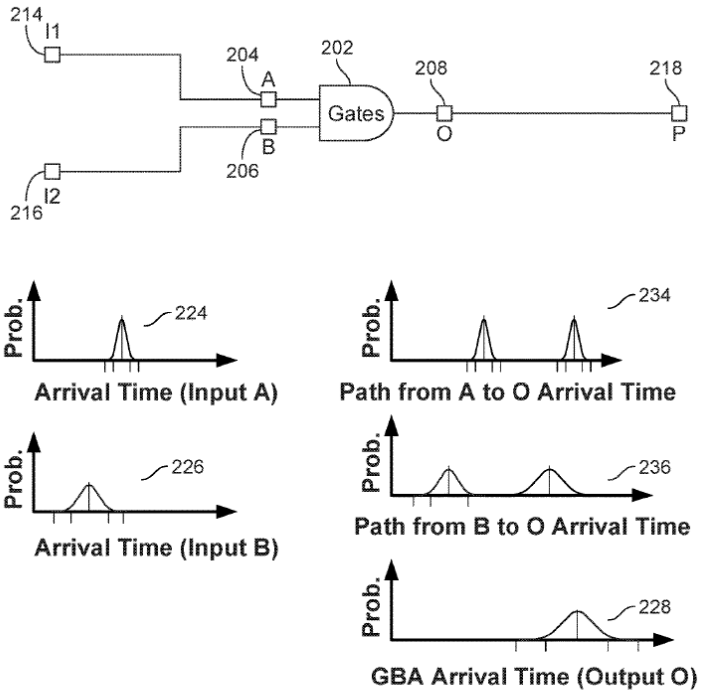
'640 Patent Claim 1	**Avatar Aprisa**
A computer-implemented method of statistical static timing analysis (SSTA) comprising:	The Aprisa tool has a timing engine that performs statistical static timing analysis using statistical OCV (SOCV) methodology. "The core of the technology is the detailed-route-centric architecture and the hierarchical database. Built upon that, there are common 'analysis engines', such as RC extraction, DRC engine, and an ***advanced, extremely fast timing engine to solve the complex timing issues associated with OCV***, SI and MCMM analysis." Aprisa Detailed-Route-Centric

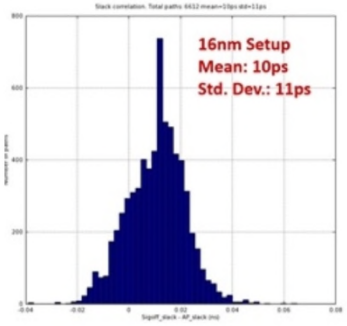
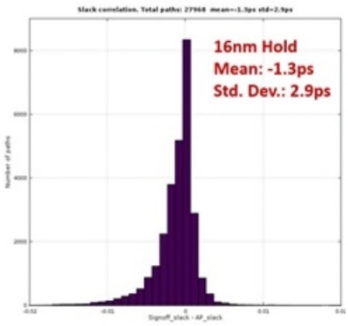
	Physical Implementation Solution, Avatar Integrated Systems, available at https://www.avatar-da.com/product-aprisa ("Aprisa Webpage") (emphasis added); *see also* "A Place-and-Route Paradigm Shift: Detailed-Route-Centric Solution Now Required," Avatar Integrated Systems, September 27, 2018, at 2 (https://www.avatar-da.com/downloads/Aprisa_data_sheet_route_centric_V7.pdf) ("Aprisa Whitepaper"). "Statistical Optimization to avoid over-designs ***•Full SOCV / LVF support*** •Full path-based analysis and optimization support •Reduce the timing pessimism and over-design against signoff." Aprisa Webpage (emphasis added). "Timing and Analysis Aprisa includes a next generation timing analysis engine with many advanced features [including] ***Native OCV timing analysis***." Aprisa Webpage (emphasis added). "To avoid the correlation problem between the timing results during implementation and the timing results from sign-off analysis, Aprisa's optimization engine supports sign-off timing analysis, that is, IR, SI, and OCV modeling. Aprisa supports both AOCV as well as LOCV and POCV." Using Parametric and Local On-Chip Variation Modeling, Aprisa Application Note, Release 11.08.rel.2.0 at 2 (December 12, 2011) ("Aprisa Application Note").
receiving, by a computer, information describing a circuit, the information comprising:	The Aprisa tool, which operates on a computer, receives information describing a circuit, including Verilog, SDC, LEF/DEF, Liberty, and/or GDSII files. "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing, optimization and embedded analysis engines. It supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, Liberty, and GDSII." Aprisa Webpage.
a first input node, a second input node, and an output node, such that there is a first path from the first input node to the output node, and a second path from the second input node to the output node, the first path and the second path converging at the output node,	The Verilog file received by the Aprisa tool contains a register-transfer-level (RTL) description of the circuit design, which may include a first path from the first input node to the output node and a second path from the second input node to the output node, where the first path and the second path converges at the output node. U.S. Patent No. 10,296,700 ("'700 Patent"), entitled "Multimode circuit place and route optimization," is assigned to Avatar Integrated Systems and describes techniques practiced by Avatar's Aprisa tool. '700 Patent at 5:45–50 ("disclosed techniques are applicable for incorporation in placement and routing systems, for example and without limitation in AVATAR Aprisa"). '700 Patent Figure 2A, a portion of which is reproduced below, shows a circuit design with a first path from the first input node I1 to the output node O and a second path from the second input node I2 to the output node O, where the first path and the second path converges at the output node O.

	 "FIG. 2A is an illustration of a sample circuit and pin arrival times. … Gate (202) has two input pins, A (204) and B (206) and output pin O (208). The pin I1 (214), for example from an output D-flipflop, is connected to input pin A (204), the pin I2 (216) is connected to input pin B (206) and pin P (218), for example to an input D-flipflop is connected to output pin O (208)." '700 Patent at 5:7–15, Fig. 2A.
each path associated with a parametric delay represented as a nominal delay value and a standard deviation value, the standard deviation value representing a timing impact of local random variation;	The Liberty file, which includes Liberty Variation Format (LVF) extensions, received by the Aprisa tool includes parametric delays associated with various cells, represented using mean (nominal delay value) and standard deviation (sigma σ) values. The delay of a path is a function of the delays associated with the cells on the path. Aprisa associates each path with a nominal and a standard deviation delay value. Upon information and belief, standard deviation represents the amount of random variation in a probability distribution. "Statistical Moments-Based LVF Models For Ultra-Low Voltage Designs The LVF models for OCV now support asymmetric, biased, or non-Gaussian distributions of timing variation. This is useful to accurately model ultra-low voltage libraries. To capture the shape of a biased timing variation distribution, ***the LVF models use the statistical moments including the mean, standard deviation***, and skewness of the distribution." Liberty User Guides and Reference Manual Suite Version 2017.06 at 2 (https://media.c3d2.de/mgoblin_media/media_entries/659/Liberty_User_Guides_and_Reference_Manual_Suite_Version_2017.06.pdf). "Each library cell needs a sigma value which specifies the standard deviation relative to the nominal delay. Use the set_variation Tcl command to specify the sigma value for one or more cells…. The -sigma argument is a positive value that specifies the magnitude of the variation." Aprisa Application Note at 2–3. "[POCV, which is a type of statistical OCV (SOCV)] analysis takes the following input: Gaussian distribution of delays inside library cells. Use the set_variation Tcl command to specify the standard deviation of these delays for specific cells." Aprisa User Guide (12.06.rel.3.0) at 296 (December 2012) ("Aprisa User Guide"). "Use the report_timing Tcl command with the -variation argument to examine the ***expected (mean) path delays***. Use the report_timing Tcl command with the -sigma n argument to examine the n-***sigma delay***, that is, the delays at n sigmas from

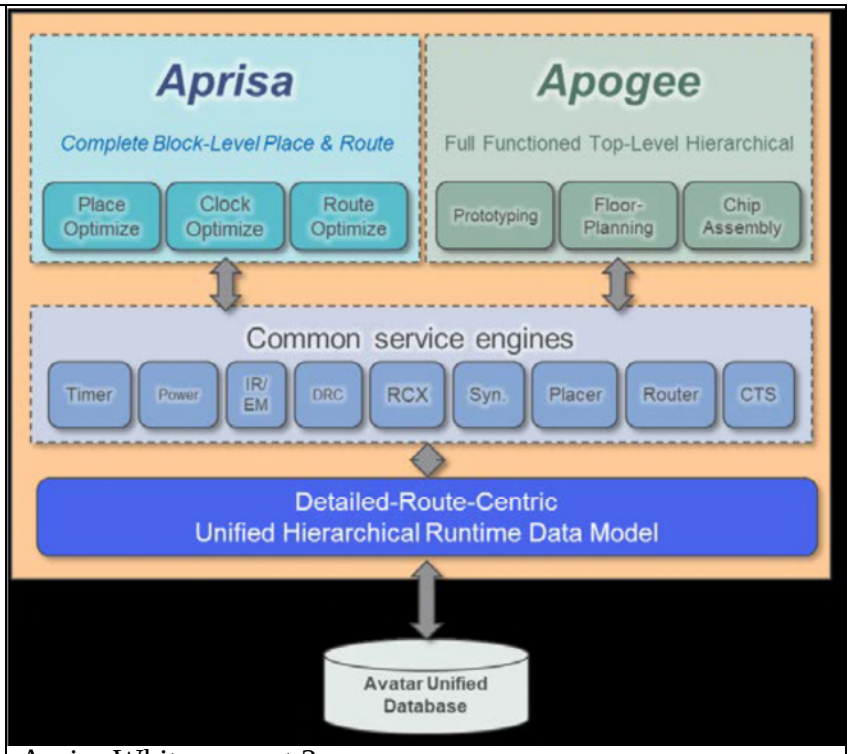
	the expected delay." *Id.* (emphasis added). The '700 Patent shows a first and second path having delays represented by a mean and standard deviation value. The delay of path I1-A-O is characterized by the mean and sigma in the probability distribution function 234 and timing of path I2-B-O is characterized by the mean and sigma in the probability distribution function 236. "As shown in FIG. 2A [reproduced below], the arrival time at output pin O (208) becomes a path specific attribute, with a path from A to O arrival time pdf (234) and a path from B to O arrival time pdf (236)." '700 Patent at 5:36–40.  FIG. 2A
performing statistical timing analysis (SSTA) based on on-chip variation (OCV) model, the SSTA comprising, determining a parametric delay at the output node based on a statistical maximum of parametric delay through the first path and parametric delay through the second path, wherein the statistical maximum preserves N sigma corner delay values, and determining the statistical	Aprisa performs statistical timing analysis based on an OCV model, which comprises determining a parametric delay at the output node based on the statistical maximum of the delay through the first path and the delay through the second path. The '700 Patent shows determining a parametric delay at output node O as a statistical maximum of parametric delay through the first path (I1-A-O) and parametric delay through the second path (I2-B-O). *See* '700 Patent at Fig. 2B (reproduced below).

maximum comprises:	 **PBA Analysis:** • Separate Path Analysis for A-O and B-O Paths. • AO = AOpba • BO = BOpba **GBA Analysis:** • Simplistic Worst Case analysis Identical for all Paths. • O = Max (AOpba, BOpba) FIG. 2B "A GBA analysis may be thought of as a simplistic analysis being identical for all paths, thus O=max (AOpba, BOpba)." *Id.* at 6:1–3 ("GBA" refers to "graph based analysis" and "pba" refers to "path based analysis"). Upon information and belief, Aprisa uses a statistical maximum operator that preserves N sigma corner delay values, which prevents the delay at the output node from being overly pessimistic. "Statistical Optimization to avoid over-designs [including] … Reduc[ing] the timing pessimism and over-design against signoff." Aprisa Webpage. "Enabling Parametric On-Chip Variation (POCV) Modeling Based on the knowledge of local random variation, parametric on-chip analysis can accurately assess the impact of local random delay variation on circuit timing, thus reducing the pessimism of the traditional global on-chip variation timing modeling." Aprisa User Guide at 296. "While faster, the timing analysis used during the design implementation typically is overly pessimistic. … Aprisa avoids this problem by supporting these advanced POCV and LOCV models during optimization." Aprisa Application Note at 1. "Aprisa includes a next generation timing analysis engine with many advanced features [including] … CRPR Support (clock convergence pessimism removal)." Aprisa Webpage.
determining a nominal delay value of the parametric delay at the output node based on a maximum of: nominal delay value of the parametric delay through the first path, and nominal delay of the parametric delay through the second path; and	Aprisa determines the nominal (mean) delay value of the parametric delay at the output node as the maximum of the nominal delay values of the first and second path. Aprisa determines the nominal delay for each pin in the timing path, including the output pin/node. Application Note at 5 ("Use the report_timing Tcl command with the -variation argument to generate a report with both the mean and the standard deviation for each pin in the timing path"). The '700 Patent shows the nominal delay value of output node O being set to the nominal delay value of path I1-A-O, which is greater than the nominal delay value of path I2-B-O. "The nominal arrival time at pin O (208) is primarily correlated with input A (204) and the corresponding edge delay from A to O, as shown in the input A arrival time pdf (probability density

	function) (224)." *Id.* at 5:19–22.  FIG. 2A "A GBA analysis may be thought of as a simplistic analysis being identical for all paths, thus O=max (AOpba, BOpba)." *Id.* at 6:1–3 ("GBA" refers to "graph based analysis" and "pba" refers to "path based analysis").
determining a standard deviation value of the parametric delay at the output node, comprising:	Aprisa determines the standard deviation (i.e., variation) of the delay for each pin in the timing path, including the output pin/node. Application Note at 5 ("Use the report_timing Tcl command with the -variation argument to generate a report with both the mean and the standard deviation for each pin in the timing path"); *see also*'700 Patent, Fig. 2A (probability distribution function 228 at output O). "The arrival time variation at pin O (208) is primarily correlated with input B (206), as shown in the input B pdf (226)." *Id.* at 5:23–25. "[T]he two ***output pin worst case arrival time attributes***, nominal arrival time and ***arrival time variation***, are correlated separately between the two input pins A and B." *Id.* at 5:26–28 (emphasis added).
determining a first value as a maximum of: a weighted sum of nominal delay value and standard deviation value of the parametric delay through the first path, and a weighted sum of nominal	Aprisa calculates an n-sigma delay for each path, which is equal to the sum of the nominal path delay plus n times the standard deviation of the path delay (*i.e.*, a weighted sum with weights 1 and n). Upon information and belief, the Aprisa tool determines a standard deviation for the delay of the output node based on the larger n-sigma delay of the first and second path, in order to preserve the larger N sigma corner delay. "Use the report_timing Tcl command with the -sigma n argument to examine the n-sigma delay, that is, the delays at n

delay value and standard deviation value of the parametric delay through the second path;	sigmas from the expected [path] delay." Aprisa User Guide at 296. "In the following example, a POCV analysis is performed and a … max timing report is requested for a three sigma confidence interval, that is, all delay values are reported at three sigmas from the mean value." *Id.* at 297. Aprisa uses a default or user-specified number of sigmas (*i.e.*, standard deviations) during timing analysis. Application Note at 3 ("Run optimization and generate a timing report using the default or user-specified confidence interval (number of sigmas)"). "You specify the confidence interval relative to the variation. By default, a 3-sigma confidence interval is used. You can modify the confidence interval using the following parameter: set_param ta timing_pocvm_n_sigma $sigma If you want to view the results with a 4-sigma confidence, use the -sigma argument as follows: report_timing -sigma 4." *Id*. at 4. "A GBA analysis may be thought of as a simplistic analysis being identical for all paths, thus O=max (AOpba, BOpba)." '700 Patent at 6:1–3. Preserving the worse N sigma corner of the two paths allows Aprisa's timing engine to achieve results that correlate with the timing results of Synopsys' industry-leading static timing analysis (STA) sign-off tool, PrimeTime. "Avatar R&D has expertise in signoff STA and created complete signoff quality STA within our P&R based on our unified runtime data model. ***Aprisa's built-in STA enjoys a reputation of excellent correlation against signoff STA***. … And since ***our built-in STA has excellent correlation with standalone signoff STA***, it significantly cuts the number of timing ECO iterations. …  Figure 3 Setup timing difference between Aprisa and signoff  Figure 4 Hold timing difference between Aprisa and signoff ***The above histograms show the setup and hold timing differences between Aprisa and signoff STA***. Both figures are from customer 16nm designs with all the advanced timing features, including PBA, waveform analysis, low voltage, CCS for delay and SI analysis. ***Note the tight correlation of Aprisa timing with signoff STA*** -- with very small mean and std deviation for both setup and hold time." "Subject: Chi-Ping Hsu answers the 6 big technical doubts about Avatar PnR," DeepChip, April 23, 2019. (http://www.deepchip.com/items/0586-06.html) (emphasis added). "Another feature [of Aprisa] is ***near sign-off timing analysis***.

	The embedded timer ***correlates with sign-off timing tools and supports various on-chip variation methods, including*** AOCV, SBOCV, ***SOCV*** and LVF. ***It also supports graph based and path based analysis*** and optimisation and advanced signal integrity and noise analysis. All timing features are enabled during optimisation, which is claimed to increase the speed of convergence." "DAC: Avatar planning tools are based around unified hierarchical database," Electronics Weekly.com, June 26, 2018 (https://www.electronicsweekly.com/news/products/software-products/dac-planning-tools-based-around-unified-hierarchical-database-2018-06/) (emphasis added). "Timing optimization and correlation with PrimeTime-SI - Aprisa has a built-in timer; its final timing was within +/- 50 psec of PrimeTime for most of our paths -- we would not be able to finish the chip otherwise. - We used Avatar's settings to help ensure their results match with PrimeTime's results, e.g. adjusting our capacitance values between wires to be more optimistic or pessimistic." "Subject: Avatar Aprisa benchmarks vs. Innovus/ICC2 at 7nm is Best of 2019 #7b," DeepChip, April 30, 2020 (http://www.deepchip.com/items/dac19-07b.html).
determining a second value as a maximum of: the nominal delay value of the parametric delay through the first path, and the nominal delay value of the parametric delay through the second path; and	Aprisa determines a second value equal to the maximum of the nominal delay values of the first and second path. The second value is the same as the nominal (mean) delay value of the output node discussed above, and thus has already been determined as discussed above.
determining the difference between the first value and the second value; and	Upon information and belief, Aprisa determines a standard deviation for the delay of the output node which preserves the larger N sigma corner of the first and second path by determining the difference between the first value and the second value. Determining the standard deviation of the output node in this manner allows Aprisa's timing engine to achieve results that correlate with the timing results of Synopsys' industry-leading static timing analysis (STA) sign-off tool, PrimeTime.
storing the nominal delay and the standard deviation value of the parametric delay for the output node.	Aprisa stores the nominal and standard deviation values of the output node delay in a database, *e.g.* the Avatar unified database, for use by its timing engine in performing static timing analysis of the circuit design.



Aprisa Whitepaper at 2.

"Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. Nothing gets lost in translation between flow steps." *Id.*

27. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '640 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa to directly infringe the '640 Patent. In particular, Avatar had actual knowledge of the '640 Patent no later than upon receipt of Synopsys' May 2020 letter and/or the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa to directly infringe one or more claims of the '640 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and uses thereof, including infringing uses (*see, e.g.,* Aprisa Webpage); Avatar knows (or should know) that its actions will induce Aprisa users to directly infringe one or more claims of the '640 Patent; and users of Aprisa directly infringe one or more claims of the '640 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that installation and use of Aprisa will infringe one or more claims of the '640 Patent and that Avatar's customers then directly infringe one or more

claims of the ’640 Patent by installing and using Aprisa in accordance with Avatar’s product literature. *See, e.g.*, Aprisa Webpage.

28. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the ’640 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or selling components that contribute to the direct infringement of one or more claims of the ’640 Patent. In particular, Avatar had actual knowledge of the ’640 Patent no later than receipt of Synopsys’ May 2020 letter and/or the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the ’640 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the ’640 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the ’640 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of statistical static timing analysis (SSTA). Aprisa is a material component of the computer-implemented method that meets one or more claims of the ’640 Patent. *See, e.g.*, Aprisa Webpage. Further, Avatar especially made and/or adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the ’640 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar’s customers directly infringe one or more claims of the ’640 Patent by installing Aprisa on a computer device and using Aprisa to perform statistical static timing analysis (SSTA) as part of a place-and-route process. *See* Aprisa Webpage.

29. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar’s infringement of the ‘640 Patent, including, without limitation, a reasonable royalty and lost profits.

30. Avatar’s infringement of the ’640 Patent is also willful because Real Intent had actual knowledge of the ’640 Patent or was willfully blind to its existence no later than upon receipt of Synopsys’ May 25, 2020 letter; engaged in the aforementioned activity despite an objectively high likelihood that Real Intent’s actions constituted infringement of the ’640 Patent;

and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

31. Avatar's infringement of the '640 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

32. Avatar's infringement of the '640 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

33. Avatar's infringement of the '640 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

COUNT II: INFRINGEMENT OF THE '863 PATENT

34. Synopsys incorporates paragraphs 1–33 as if fully set forth herein.

35. On information and belief, Avatar and/or users of the Avatar Aprisa and/or Apogee software products have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '863 Patent by making, using, offering to sell, and/or selling Aprisa and/or Apogee within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

36. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '863 Patent against Aprisa and/or Apogee. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

'863 Patent Claim 1	Avatar Aprisa and/or Apogee
A method used in producing a design of an integrated circuit said circuit design having cells and interconnects, said circuit having a representation that is hierarchically decomposed into a top-level and a plurality of blocks, at least some of the plurality of said blocks being capable of being further hierarchically decomposed and of having a parent block associated therewith, said method comprising:	Avatar's Aprisa and/or Apogee products (collectively referred to below as "Aprisa") produce a design of an integrated circuit with cells and interconnects. The circuit has a representation that is hierarchically decomposed into a top-level and a plurality of blocks, at least some of the plurality of said blocks being capable of being further hierarchically decomposed and of having a parent block associated therewith. For example: "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing, optimization and embedded analysis engines. It supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, Liberty, and GDSII. The state-of-the-art technologies and tightly integrated functions ensure superior quality-of-result and competitive runtime for IC design projects." Aprisa Webpage. "Floorplanning Aprisa provides an easy-to-use floor-planner that enables fast analysis of design hierarchy. Automation of many of

	the traditionally manual tasks such as manual macro placement and blockage creation helps the designers converge on an optimal floor-plan much faster. … The rich feature set includes: … ***Multiple libraries, and multi-height standard cells***." Aprisa Webpage (emphasis added). "Key features … In-Hierarchy Optimization (iHO) for top-level timing closure." Aprisa Webpage. "Key benefits … Faster and easier top-level timing closure without long cycle of timing re-budgeting and timing model updating." Aprisa Webpage. "***Interconnect Centric 'Precision Optimization'*** Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past." Aprisa Webpage (emphasis added). "Apogee is a complete top down floor planning and chip assembly tool that complements Aprisa. ATopTech's block level implementation tool. Apogee and Aprisa's shared timing, placement, and routing engines enable excellent correlation between block and top level timing, and provide a seamless integrated design environment for complex chip designs." Avatar website page on Apogee, https://www.avatar-da.com/product-apogee ("Apogee Webpage"). "Features … Automatic hierarchy partitioning with full rectilinear support … Unique, on-the-fly timing and physical abstraction eliminates creating of extra files and models for blocks while drastically reducing run time and memory." Apogee Webpage.
processing at least one of said blocks such that an abstraction is created that includes physical interconnect information relating to interconnects between components within said at least one block, said physical interconnect information modeling parasitic electrical and physical effects of interconnects upon an estimated behavior of said integrated circuit, wherein said processing includes:	Aprisa processes at least one of said blocks such that an abstraction is created that includes physical interconnect information relating to interconnects between components within said at least one block, said physical interconnect information modeling parasitic electrical and physical effects of interconnects upon an estimated behavior of said integrated circuit. For example: "Key features … In-Hierarchy Optimization (iHO) for top-level timing closure." Aprisa Webpage. "***Interconnect Centric 'Precision Optimization'*** Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing." Aprisa Webpage (emphasis added). "Features … Automatic hierarchy partitioning with full rectilinear support … Database level access for manipulating netlist hierarchy within physical design environment Hierarchical flow support for various advanced clock topologies including multi-point, mesh, and H-tree Unique, on-the-fly timing and physical abstraction eliminates creating of extra files and models for

	blocks while drastically reducing run time and memory." Apogee Webpage. On information and belief, the block-level and hierarchical processing features in Aprisa create an abstraction. In addition, Avatar advertises interconnect centric optimization. Those features include physical interconnect information including at least information obtained from parasitic extraction, which is one example of physical interconnect information modeling parasitic electrical and physical effects of interconnects upon an estimated behavior of said integrated circuit.
retaining only a sub-set of all of said physical interconnect information which influences physical and electrical behavior of said parent block; and	Aprisa retains only a sub-set of all of said physical interconnect information which influences physical and electrical behavior of said parent block. For example: "Key benefits … Easier to support hierarchical flow." Aprisa Webpage. "Features … Automatic hierarchy partitioning with full rectilinear support … Unique, on-the-fly timing and physical abstraction eliminates creating of extra files and models for blocks while drastically reducing run time and memory." Apogee Webpage. Physical and electrical behaviors are basic aspects of a block. Aprisa's "physical abstraction" and "hierarchical" approaches include steps of handling at least various types of interconnect information separately. On information and belief, Aprisa's on-the-fly timing and physical abstraction feature retains only a subset of such information in that it eliminates creating extra files and models.
retaining only a sub-set of cells which influences a logical behavior of said parent block; and	Aprisa retains only a sub-set of cells which influences a logical behavior of said parent block. For example: "Features … Automatic hierarchy partitioning with full rectilinear support … Unique, on-the-fly timing and physical abstraction eliminates creating of extra files and models for blocks while drastically reducing run time and memory." Apogee Webpage. "Key benefits … Easier to support hierarchical flow." Aprisa Webpage. "Floorplanning Aprisa provides an easy-to-use floor-planner that enables fast analysis of design hierarchy. Automation of many of the traditionally manual tasks such as manual macro placement and blockage creation helps the designers converge on an optimal floor-plan much faster. … The rich feature set includes: … ***Multiple libraries, and multi-height standard cells***." Aprisa Webpage (emphasis added). Logical behavior is a basic aspect of a block. Aprisa's "physical abstraction" and "hierarchical" approaches include handling at least various types of interconnect information separately. On information and belief, Aprisa's on-the-fly timing and physical abstraction feature retains only a subset of cells which influence logical behavior in that it eliminates creating extra files and models.

utilizing said abstraction in another development phase performed on said parent block.	Aprisa utilizes said abstraction in another development phase performed on said parent block. For example: "Kev features … In-Hierarchy Optimization (iHO) for top-level timing closure." Aprisa Webpage. "Kev benefits … Faster and easier top-level timing closure without long cycle of timing re-budgeting and timing model updating." Aprisa Webpage. "***Interconnect Centric 'Precision Optimization'*** Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing." Aprisa Webpage (emphasis added). "Features … Automatic hierarchy partitioning with full rectilinear support … Virtual top level timing optimization and block timing budgeting. Rapid budget-less prototyping with unique 'transparent hierarchy' optimization … Repeated block optimization … Database level access for manipulating netlist hierarchy within physical design environment. Hierarchical flow support for various advanced clock topologies including multi-point, mesh, and H-tree. Unique, on-the-fly timing and physical abstraction eliminates creating of extra files and models for blocks while drastically reducing run time and memory … Fast, top level optimization and router that correlate well with block level timing." Apogee Webpage. On information and belief, Aprisa uses an abstraction in at least two of floorplanning, placement and optimization, timing and analysis, global route and optimization and detailed route and optimization. On information and belief, Aprisa's virtual top level optimization, transparent hierarchical optimization and "fast, top level optimization and router that correlate well with block level timing" are all features that utilize an abstraction on another development phase performed on said parent block.

37. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '863 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa and/or Apogee to directly infringe the '863 Patent. In particular, Avatar had actual knowledge of the '863 Patent no later than the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa and/or Apogee to directly infringe one or more claims of the '863 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and/or Apogee and uses thereof, including infringing uses (*see, e.g.*, Aprisa Webpage & Apogee Webpage); Avatar knows (or should know) that its actions will

induce Aprisa users to directly infringe one or more claims of the '863 Patent; and users of Aprisa directly infringe one or more claims of the '863 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that installation and use of Aprisa will infringe one or more claims of the '863 Patent and that Avatar's customers then directly infringe one or more claims of the '863 Patent by installing and using Aprisa and Apogee in accordance with Avatar's product literature. *See, e.g.*, Aprisa Webpage & Apogee Webpage.

38. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '863 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or selling components that contribute to the direct infringement of one or more claims of the '863 Patent. In particular, Avatar had actual knowledge of the '863 Patent no later than the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the '863 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the '863 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the '863 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of producing a design of an integrated circuit using a circuit representation that is hierarchically decomposed into a top-level and a plurality of blocks. Aprisa is a material component of the computer-implemented method that meets one or more claims of the '863 Patent. *See, e.g.*, Aprisa Webpage & Apogee Webpage. Further, Avatar especially made and/or adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the '863 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar's customers directly infringe one or more claims of the '863 Patent by installing Aprisa on a computer device and using Aprisa to process circuit representations that are hierarchically decomposed into a top-level and a plurality of blocks as part of a place-and-route process. *See* Aprisa Webpage & Apogee Webpage.

39. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar's infringement of the '863 Patent, including, without limitation, a

reasonable royalty and lost profits.

40. Avatar's infringement of the '863 Patent is also willful because Real Intent had actual knowledge of the '863 Patent or was willfully blind to its existence no later than upon receipt of a June 16, 2020 letter sent by counsel for Synopsys to counsel for Avatar informing Avatar that it was infringing on several Synopsys patents, including the '863 Patent; engaged in the aforementioned activity despite an objectively high likelihood that Real Intent's actions constituted infringement of the '863 Patent; and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

41. Avatar's infringement of the '863 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

42. Avatar's infringement of the '863 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

43. Avatar's infringement of the '863 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

COUNT III: INFRINGEMENT OF THE '567 PATENT

44. Synopsys incorporates paragraphs 1–43 as if fully set forth herein.

45. On information and belief, Avatar and/or users of the Avatar Aprisa software product have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '567 Patent by making, using, offering to sell, and/or selling Aprisa within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

46. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '567 Patent against Aprisa. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

'567 Patent Claim 1	**Avatar Aprisa**
A method for generating a clock-tree on an integrated circuit (IC) chip	Aprisa performs a method for generating a clock-tree on an integrated circuit chip. For example: "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing,

	optimization and embedded analysis engines. It supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, Liberty, and GDSII. The state-of-the-art technologies and tightly integrated functions ensure superior quality-of-result and competitive runtime for IC design projects." Aprisa Webpage. "Clock Tree Synthesis (CTS) and Optimization Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: Cluster-based clock trees or meshes." Aprisa Webpage.
receiving a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout;	Aprisa receives a placement for a chip layout, where the placement includes a set of registers at fixed locations in the chip layout. For example: "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing, optimization and embedded analysis engines." Aprisa Webpage. "Key features … Progressive MCMM CTS Skewgroup-based CTS Slack-driven CTS Multi-point CTS Support for mesh and H-tree Power aware clock tree optimization with useful skew." Aprisa Webpage. "Clock Tree Synthesis (CTS) and Optimization Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: Cluster-based clock trees or meshes." Aprisa Webpage. On information and belief, Aprisa performs placement and optimization prior to clock tree synthesis. The clock tree synthesis module then receives the placement data, which includes registers at fixed locations. Cluster-based clock trees or meshes necessarily include registers.
generating, using a computer, a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers	Aprisa generates a timing criticality profile for the set of registers, wherein the timing criticality profile specifies timing criticalities between pairs of registers in the set of registers (and does so using a computer). For example: "Clock Tree Synthesis (CTS) and Optimization" Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-

	clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: Cluster-based clock trees or meshes." Aprisa Webpage. "Key features … Skewgroup-based CTS Slack-driven CTS Multi-point CTS … Power aware clock tree optimization with useful skew." Aprisa Webpage. Aprisa "optimizes" clock tree synthesis, "minimizes the number of buffers, and "overall timing optimization." Upon information and belief, a timing criticality profile is a necessary in order to achieve optimization. The clock tree "skew," "local and inter-clock skew" and "local skew" all specify timing criticalities between pairs of registers. "Slack" in slack-driven CTS specifically refers to timing criticality or lack thereof. Upon information and belief, the "complex designs" Aprisa is designed to handle will have multiple registers and Aprisa's timing criticality necessarily includes timing criticalities between pairs of registers. *See* Aprisa Webpage.
clustering the set of registers based on the timing criticality profile to create a clock-tree for the set of registers,	Aprisa clusters the set of registers based on the timing criticality profile to create a clock-tree for the set of registers. For example: "Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: ***Cluster-based clock trees or meshes*** Gated and generated clocks Synchronization of generated clock pins Automatic clock gate cloning and de-cloning Matching of latency targets specified by user for any pins Automatic creation of special routing constraints (layer, double width/spacing/via, shielding, etc.) Low-Power Clock Tree Synthesis Multi-corner and multi-mode clock tree synthesis and clock optimization Level-balanced Clock Tree Synthesis Route-based clock tree optimization." Aprisa Webpage (emphasis added). Aprisa performs clock tree synthesis, which includes creating a clock tree for a set of registers. Upon information and belief, doing so in a way that achieves "optimization" includes clustering the set of registers based on the timing criticality profile. Additionally, Aprisa performs "level-balanced clock tree synthesis." Upon information and belief, level-balancing takes into consideration levels of timing criticality and balances priority of clustering of registers based thereon.
wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each	Aprisa performs a clustering step wherein clustering the set of registers involves clustering a first pair of registers which has a higher timing criticality between each other prior to clustering a second pair of registers which has a lower timing criticality between each other. *See* the above discussion of the "clustering"

other prior to clustering a second pair of registers which has a lower timing criticality between each other;	limitation. On information and belief, optimizing clock tree synthesis for area, skew and timing involves clustering pairs of registers based on timing criticality.
wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs.	Aprisa performs a clustering step wherein clustering registers based on the timing criticality profile facilitates using commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs. *See* the above discussion of the "clustering" limitation. "Aprisa includes a next generation timing analysis engine with many advanced features. Features Very fast, typically 5 minutes per million instances Read SDC natively without any translation Native OCV timing analysis ***CRPR Support (clock convergence pessimism removal)***." Aprisa Webpage (emphasis added). On information and belief, to achieve route-based clock tree optimization for cluster-based clock trees or meshes, Aprisa uses commonly-shared clock paths in the clock-tree to provide clock signals to timing critical register pairs.

47. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '567 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa to directly infringe the '567 Patent. In particular, Avatar had actual knowledge of the '567 Patent no later than the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa to directly infringe one or more claims of the '567 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and uses thereof, including infringing uses (*see, e.g.,* Aprisa Webpage); Avatar knows (or should know) that its actions will induce Aprisa users to directly infringe one or more claims of the '567 Patent; and users of Aprisa directly infringe one or more claims of the '567 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that installation and use of Aprisa will infringe one or more claims of the '567 Patent and that Avatar's customers then directly infringe one or more claims of the '567 Patent by installing and using Aprisa in accordance with Avatar's product literature. *See, e.g.,* Aprisa Webpage.

48. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '567 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or

selling components that contribute to the direct infringement of one or more claims of the '567 Patent. In particular, Avatar had actual knowledge of the '567 Patent no later than the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the '567 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the '567 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the '567 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of generating a clock-tree on an integrated circuit chip. Aprisa is a material component of the computer-implemented method that meets one or more claims of the '567 Patent. *See, e.g.*, Aprisa Webpage. Further, Avatar especially made and/or adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the '567 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar's customers directly infringe one or more claims of the '567 Patent by installing Aprisa on a computer device and using Aprisa to generate a clock-tree as part of a place-and-route process. *See* Aprisa Webpage.

49. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar's infringement of the '567 Patent, including, without limitation, a reasonable royalty and lost profits.

50. Avatar's infringement of the '567 Patent is also willful because Real Intent had actual knowledge of the '567 Patent or was willfully blind to its existence no later than upon receipt of a June 16, 2020 letter sent by counsel for Synopsys to counsel for Avatar informing Avatar that it was infringing on several Synopsys patents, including the '567 Patent; engaged in the aforementioned activity despite an objectively high likelihood that Real Intent's actions constituted infringement of the '567 Patent; and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

51. Avatar's infringement of the '567 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

52. Avatar's infringement of the '567 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

53. Avatar's infringement of the '567 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

COUNT IV: INFRINGEMENT OF THE '915 PATENT

54. Synopsys incorporates paragraphs 1–53 as if fully set forth herein.

55. On information and belief, Avatar and/or users of the Avatar Aprisa software product have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '915 Patent by making, using, offering to sell, and/or selling Aprisa within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

56. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '915 Patent against Aprisa. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

'915 Patent Claim 1	**Avatar Aprisa**
A method of performing physical synthesis using persistence-driven optimization, the method comprising:	Avatar's Aprisa product performs a method of physical synthesis using persistence-driven optimization. For example: "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing, optimization and embedded analysis engines. It supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, Liberty, and GDSII. The state-of-the-art technologies and tightly integrated functions ensure superior quality-of-result and competitive runtime for IC design projects." Aprisa Webpage. "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes. The global route includes track assignment so that near detailed route information can be used ***to generate delays and signal integrity information***. Combined with precision optimization sizing, buffering, and wire spreading can all be looked at concurrently to achieve the best possible solution. All of this is done ***with MCMM timing***. The key is to eliminate the problems such as congestion and signal integrity issues before the detailed route phase. The unique feature of this step is that it is trying to address gross signal-integrity problems during global route stage. This allows more changes than is possible during post-route stage. Support includes: ***Iterative fixing of timing and routing to achieve timing closure SI aware timing engine enabling fixing the noise violations where they happen i.e. not an after-thought to***

	fix the SI violations. Route aware area recovery Route aware leakage power optimization Metal fill emulation to get accurate prediction of final timing." Aprisa Webpage (emphasis added). "Industry's First Detailed-Route-Centric P&R Architecture Detailed-Route-Centric architecture is Avatar's newest technology which enables efficient and frequent detailed route layers, patterns, congestions, pin-access, etc. to be ***available throughout the place and route flow***, which reduce the number of place and route iterations and accelerate design closure." Aprisa Webpage (emphasis added).
using a processor, ranking nets in a design based on unpredictability and expected quality-of-result impact;	Aprisa ranks nets in a design based on unpredictability and expected quality-of-result impact. For example: "Key features … SI-aware placement optimization and global route optimization." Aprisa Webpage. "PowerFirst™ Optimization Starts from best power solution and optimize the design for better timing Applied to the flow from placement to routing Including algorithms for static-power-centric and dynamic-power-centric flows." Aprisa Webpage. "PowerFirst™ CTS Consider both power and timing cost during Clock Tree Synthesis and Optimization for best power while meeting timing." Aprisa Webpage. "Statistical Optimization to avoid over-designs Full SOCV / LVF support Full path-based analysis and optimization support Reduce the timing pessimism and over-design against signoff." Aprisa Webpage. "Placement and Optimization Aprisa's placement technology is a timing and congestion driven analytical based placer. The placer calls the timing analysis engine frequently to dynamically obtain and update the best net weightings throughout the flow. ***The placement and optimization engines iterates intelligently between wire-length, routing congestion, area, leakage power and other critical factors to achieve optimal timing, area and power for the block/configuration under consideration.***" Aprisa Webpage (emphasis added). "Clock Tree Synthesis (CTS) and Optimization … Optimizing for both area and leakage power, it minimizes the number of buffers." Aprisa Webpage. "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. ***At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration.*** Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure." Aprisa Whitepaper (emphasis added). "***The Route Service Engine (RSE) provides proper routing***

	information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure. The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. ***Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.***" Aprisa Whitepaper (emphasis added). "RSE engine at work on critical nets The figures below shows the RSE engine ***at work on critical nets***. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). On information and belief, Aprisa's global routing engine prioritizes high-impact nets for routing prior to low-impact nets. For example "critical nets" are prioritized. This prioritization includes ranking nets based on the expected quality-of-result impact based on non-default route rules and timing uncertainty.
selecting a first predetermined top percentage of the ranked nets as first persistent nets;	Aprisa selects a first predetermined top percentage of the ranked nets as first persistent nets. For example: "Key features … SI-aware placement optimization and global route optimization." Aprisa Webpage. "PowerFirst™ Optimization Starts from best power solution and optimize the design for better timing Applied to the flow from placement to routing Including algorithms for static-power-centric and dynamic-power-centric flows." Aprisa Webpage. "PowerFirst™ CTS Consider both power and timing cost during Clock Tree Synthesis and Optimization for best power while meeting timing." Aprisa Webpage. "Statistical Optimization to avoid over-designs Full SOCV / LVF support Full path-based analysis and optimization support Reduce the timing pessimism and over-design against signoff." Aprisa Webpage. "Placement and Optimization Aprisa's placement technology is a timing and congestion driven analytical based placer. The placer calls the timing analysis engine frequently to dynamically obtain and update the best net weightings throughout the flow. ***The placement and optimization engines iterates intelligently between wire-length, routing congestion, area, leakage power and other critical factors to achieve optimal timing, area and power for the block/configuration under consideration.***" Aprisa

	Webpage (emphasis added). "Clock Tree Synthesis (CTS) and Optimization … Optimizing for both area and leakage power, it minimizes the number of buffers." Aprisa Webpage. "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. ***At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration.*** Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure." Aprisa Whitepaper (emphasis added). "***The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure.*** The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. ***Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.***" Aprisa Whitepaper (emphasis added). "RSE engine at work on critical nets The figures below shows the RSE engine ***at work on critical nets***. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). On information and belief, Aprisa's global routing engine prioritizes high-impact nets for routing prior to low-impact nets. For example "critical nets" are prioritized. This prioritization includes selecting a predetermined top percentage of the ranked nets as first persistent nets.
performing timing-driven global routing on the first persistent nets;	Aprisa performs timing-driven global routing on the first persistent nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes. The global route includes track assignment so that near detailed route information can be used ***to generate delays and signal integrity information***.

	Combined with precision optimization sizing, buffering, and wire spreading can all be looked at concurrently to achieve the best possible solution. All of this is done ***with MCMM timing***. The key is to eliminate the problems such as congestion and signal integrity issues before the detailed route phase. The unique feature of this step is that it is trying to address gross signal-integrity problems during global route stage. This allows more changes than is possible during post-route stage. Support includes: ***Iterative fixing of timing and routing to achieve timing closure*** SI aware ***timing engine*** enabling fixing the noise violations where they happen i.e. not an after-thought to fix the SI violations. Route aware area recovery Route aware leakage power optimization Metal fill emulation to get accurate prediction of final timing." Aprisa Webpage (emphasis added). Aprisa iteratively fixes timing and routing to achieve timing closure. Aprisa performs timing-driven global routing on the first persistent nets at least during a first iteration.
back-annotating a timing graph with actual delays and parasitics determined by performing the timing-driven global routing on the first persistent nets;	Aprisa back-annotates a timing graph with actual delays and parasitics determined by performing the timing-driven global routing on the first persistent nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes. The global route includes track assignment so that near detailed route information can be used to generate delays and signal integrity information." Aprisa Webpage. "Interconnect Centric 'Precision Optimization' Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. ***This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing.***" Aprisa Webpage (emphasis added). "Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. ***Nothing gets lost in translation between flow steps.***" Aprisa Whitepaper (emphasis added). "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. ***At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration.*** Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure." Aprisa Whitepaper (emphasis added).

	"***The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure.*** The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. ***Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.***" Aprisa Whitepaper (emphasis added). Aprisa makes design information derived at any point during the flow, including actual delays and parasitics, available to any other engine through the UDM and RSE. Aprisa performs optimization throughout the flow, during placement, CTS, and both global and detailed routing. This feature indicates that it uses updated data to make updates and improvements. On information and belief, the UDM includes a timing graph, which would be necessary for the RSE to provide delta delays, and the process of updating that timing graph for use in other aspects of the flow includes at least back annotating.
running synthesis for the nets in the design using the actual delays and the parasitics for the first persistent nets, wherein the synthesis maintains and updates routing for the first persistent nets;	Aprisa runs synthesis for the nets in the design using the actual delays and the parasitics for the first persistent nets, wherein the synthesis maintains and updates routing for the first persistent nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes. The global route includes track assignment ***so that near detailed route information can be used to generate delays and signal integrity information***. Combined with precision optimization sizing, buffering, and wire spreading can all be looked at concurrently to achieve the best possible solution. All of this is done with MCMM timing. The key is to eliminate the problems such as congestion and signal integrity issues before the detailed route phase. The unique feature of this step is that it is trying to address gross signal-integrity problems during global route stage. This allows more changes than is possible during post-route stage. Support includes: ***Iterative fixing of timing and routing to achieve timing closure***." Aprisa Webpage (emphasis added). "Interconnect Centric 'Precision Optimization' Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, ***precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy***. ***This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing***." Aprisa Webpage (emphasis added). "The placement and optimization engines iterates intelligently between wire-length, routing congestion, area, leakage power and

	other critical factors to achieve optimal timing, area and power for the block/configuration under consideration." Aprisa Webpage. Aprisa uses actual delays, signal integrity information and parasitics to run synthesis. Aprisa iteratively fixes timing and routing to achieve timing closure. Aprisa performs synthesis on prioritized nets at least during a first iteration by and that operation necessarily includes both maintaining routing for the prioritized nets and updating routing for the prioritized nets.
re-ranking the nets in the design after synthesis based on unpredictability and expected quality-of-result impact;	Aprisa re-ranks the nets in the design after synthesis based on unpredictability and expected quality-of-result impact. For example: "Key features … SI-aware placement optimization and global route optimization." Aprisa Webpage. "PowerFirst™ Optimization Starts from best power solution and optimize the design for better timing Applied to the flow from placement to routing Including algorithms for static-power-centric and dynamic-power-centric flows." Aprisa Webpage. "PowerFirst™ CTS Consider both power and timing cost during Clock Tree Synthesis and Optimization for best power while meeting timing." Aprisa Webpage. "Statistical Optimization to avoid over-designs Full SOCV / LVF support Full path-based analysis and optimization support Reduce the timing pessimism and over-design against signoff" Aprisa Webpage. "Placement and Optimization Aprisa's placement technology is a timing and congestion driven analytical based placer. The placer calls the timing analysis engine frequently to dynamically obtain and update the best net weightings throughout the flow. ***The placement and optimization engines iterates intelligently between wire-length, routing congestion, area, leakage power and other critical factors to achieve optimal timing, area and power for the block/configuration under consideration.***" Aprisa Webpage (emphasis added). "Clock Tree Synthesis (CTS) and Optimization … Optimizing for both area and leakage power, it minimizes the number of buffers." Aprisa Webpage. "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. ***At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration.*** Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure." Aprisa Whitepaper (emphasis added). "***The Route Service Engine (RSE) provides proper routing***

	information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure. The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. ***Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.***" Aprisa Whitepaper (emphasis added). "RSE engine at work on critical nets The figures below shows the RSE engine ***at work on critical nets***. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). On information and belief, Aprisa's global routing engine prioritizes high-impact nets for routing prior to low-impact nets. For example "critical nets" are prioritized. This prioritization includes ranking nets based on the expected quality-of-result impact based on non-default route rules and timing uncertainty. In subsequent iterations, the prioritized nets include a second subset of nets.
selecting a second predetermined top percentage of the re-ranked nets as second persistent nets;	Aprisa selects a second predetermined top percentage of the re-ranked nets as second persistent nets. For example: "Key features … SI-aware placement optimization and global route optimization." Aprisa Webpage. "PowerFirst™ Optimization Starts from best power solution and optimize the design for better timing Applied to the flow from placement to routing Including algorithms for static-power-centric and dynamic-power-centric flows." Aprisa Webpage. "PowerFirst™ CTS Consider both power and timing cost during Clock Tree Synthesis and Optimization for best power while meeting timing." Aprisa Webpage. "Statistical Optimization to avoid over-designs Full SOCV / LVF support Full path-based analysis and optimization support Reduce the timing pessimism and over-design against signoff" Aprisa Webpage. "Placement and Optimization Aprisa's placement technology is a timing and congestion driven analytical based placer. The placer calls the timing analysis engine frequently to dynamically obtain and update the best net weightings throughout the flow. ***The placement and optimization engines iterates intelligently between wire-length, routing congestion, area, leakage power***

	and other critical factors to achieve optimal timing, area and power for the block/configuration under consideration." Aprisa Webpage (emphasis added). "Clock Tree Synthesis (CTS) and Optimization … Optimizing for both area and leakage power, it minimizes the number of buffers." Aprisa Webpage. "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. ***At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration.*** Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure." Aprisa Whitepaper (emphasis added). "***The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure.*** The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. ***Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.***" Aprisa Whitepaper (emphasis added). "RSE engine at work on critical nets The figures below shows the RSE engine ***at work on critical nets***. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). On information and belief, Aprisa's global routing engine prioritizes high-impact nets for routing prior to low-impact nets. For example "critical nets" are prioritized. In a second iteration, this prioritization includes selecting a predetermined top percentage of the ranked nets as second persistent nets.
performing timing-driven global routing on the second persistent nets that had not been selected among the	Aprisa performs timing-driven global routing on the second persistent nets that had not been selected among the first persistent nets. For example: "Global Route and Optimization Aprisa's fast global route

first persistent nets;	engine can route millions of nets in minutes. The global route includes track assignment so that near detailed route information can be used ***to generate delays and signal integrity information***. Combined with precision optimization sizing, buffering, and wire spreading can all be looked at concurrently to achieve the best possible solution. All of this is done ***with MCMM timing***. The key is to eliminate the problems such as congestion and signal integrity issues before the detailed route phase. The unique feature of this step is that it is trying to address gross signal-integrity problems during global route stage. This allows more changes than is possible during post-route stage. Support includes: ***Iterative fixing of timing and routing to achieve timing closure*** SI aware ***timing engine*** enabling fixing the noise violations where they happen i.e. not an after-thought to fix the SI violations. Route aware area recovery Route aware leakage power optimization Metal fill emulation to get accurate prediction of final timing." Aprisa Webpage (emphasis added). Aprisa iteratively fixes timing and routing to achieve timing closure. Aprisa performs timing-driven global routing on the second persistent nets at least during a second iteration.
performing global routing on the nets of the design while maintaining existing routes of the second persistent nets; and	Aprisa performs global routing on the nets of the design while maintaining existing routes of the second persistent nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes. The global route includes track assignment so that near detailed route information can be used ***to generate delays and signal integrity information***. Combined with precision optimization sizing, buffering, and wire spreading can all be looked at concurrently to achieve the best possible solution. All of this is done ***with MCMM timing***. The key is to eliminate the problems such as congestion and signal integrity issues before the detailed route phase. The unique feature of this step is that it is trying to address gross signal-integrity problems during global route stage. This allows more changes than is possible during post-route stage. Support includes: ***Iterative fixing of timing and routing to achieve timing closure*** SI aware ***timing engine*** enabling fixing the noise violations where they happen i.e. not an after-thought to fix the SI violations. Route aware area recovery Route aware leakage power optimization Metal fill emulation to get accurate prediction of final timing." Aprisa Webpage (emphasis added). Aprisa iteratively fixes timing and routing to achieve timing closure. Aprisa performs global routing of other nets of the design after prioritized nets while maintaining the routes of the previously routed prioritized nets.
outputting a final layout of the design based on the global routing.	Aprisa outputs a final layout of the design based on the global routing. For example: "Aprisa is a complete full-functioned block-level place and route (P&R) system with placement, clock tree synthesis, routing, optimization and embedded analysis engines. It supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF,

	Liberty, and GDSII. The state-of-the-art technologies and tightly integrated functions ensure superior quality-of-result and competitive runtime for IC design projects." Aprisa Webpage.

57. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '915 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa to directly infringe the '915 Patent. In particular, Avatar had actual knowledge of the '915 Patent no later than the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa to directly infringe one or more claims of the '915 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and uses thereof, including infringing uses (*see, e.g.*, Aprisa Webpage); Avatar knows (or should know) that its actions will induce Aprisa users to directly infringe one or more claims of the '915 Patent; and users of Aprisa directly infringe one or more claims of the '915 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that installation and use of Aprisa will infringe one or more claims of the '915 Patent and that Avatar's customers then directly infringe one or more claims of the '915 Patent by installing and using Aprisa in accordance with Avatar's product literature. *See, e.g.*, Aprisa Webpage.

58. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '915 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or selling components that contribute to the direct infringement of one or more claims of the '915 Patent. In particular, Avatar had actual knowledge of the '915 Patent no later than the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the '915 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the '915 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the '915 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of physical synthesis using persistence-driven optimization. Aprisa is a material component of the computer-implemented method that meets one or more claims of the '915 Patent. *See, e.g.*, Aprisa Webpage. Further, Avatar especially made and/or

adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the '915 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar's customers directly infringe one or more claims of the '915 Patent by installing Aprisa on a computer device and using Aprisa to perform persistence-driven optimization as part of a place-and-route process. *See* Aprisa Webpage.

59. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar's infringement of the '915 Patent, including, without limitation, a reasonable royalty and lost profits.

60. Avatar's infringement of the '915 Patent is also willful because Real Intent had actual knowledge of the '915 Patent or was willfully blind to its existence no later than upon receipt of a June 16, 2020 letter sent by counsel for Synopsys to counsel for Avatar informing Avatar that it was infringing on several Synopsys patents, including the '915 Patent; engaged in the aforementioned activity despite an objectively high likelihood that Real Intent's actions constituted infringement of the '915 Patent; and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

61. Avatar's infringement of the '915 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

62. Avatar's infringement of the '915 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

63. Avatar's infringement of the '915 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

COUNT V: INFRINGEMENT OF THE '614 PATENT

64. Synopsys incorporates paragraphs 1–63 as if fully set forth herein.

65. On information and belief, Avatar and/or users of the Avatar Aprisa software product have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '614 Patent by making, using, offering to sell, and/or selling Aprisa within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

66. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '614 Patent against Aprisa. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

'614 Patent Claim 1	**Avatar Aprisa**
A method of routing a semiconductor chip's global nets, comprising:	Avatar's Aprisa product performs a method of routing a semiconductor chip's global nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes." Aprisa Webpage.
ranking said semiconductor chip's global nets, wherein said ranking includes at least one of the following: ranking power/ground nets over clock signal nets; ranking power/ground nets over timing/slew critical nets; ranking clock signal nets over timing/slew critical nets; ranking shorter length and lower fan-out nets over longer length and higher fan-out nets;	Aprisa ranks a semiconductor chip's global nets including at least by ranking power/ground nets over clock signal nets, ranking power/ground nets over timing/slew critical nets, and ranking clock signal nets over timing/slew critical nets. For example: "Floorplanning Aprisa provides an easy-to-use floor-planner that enables fast analysis of design hierarchy. Automation of many of the traditionally manual tasks such as manual macro placement and blockage creation helps the designers converge on an optimal floor-plan much faster. Common placement, routing, and timing engines mean good correlation for congestion and timing from floorplanning stage all the way through the final routing stage. The rich feature set includes: … Parametric multit-headed [sic] routing for power/ground grid creation." Aprisa Webpage. "Clock Tree Synthesis (CTS) and Optimization Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: … Route-based clock tree optimization." Aprisa Webpage. "The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. ***Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure.*** The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently." Aprisa Whitepaper (emphasis added). "The figures below shows [sic] the RSE engine at work on critical nets. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the

	same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). On information and belief, Aprisa's parametric multi-threaded routing for power/ground grid creation feature ranks power/ground nets over clock signal nets and/or ranking power/ground nets over timing/slew critical nets. On information and belief, Aprisa's route-based clock tree optimization feature ranks clock signal nets over timing/slew critical nets.
identifying a subset of said global nets;	Aprisa identifies a subset of said global nets. For example: "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes." Aprisa Webpage. "Floorplanning Aprisa provides an easy-to-use floor-planner that enables fast analysis of design hierarchy. Automation of many of the traditionally manual tasks such as manual macro placement and blockage creation helps the designers converge on an optimal floor-plan much faster. Common placement, routing, and timing engines mean good correlation for congestion and timing from floorplanning stage all the way through the final routing stage. The rich feature set includes: … Parametric multit-headed [sic] routing for power/ground grid creation." Aprisa Webpage. "Clock Tree Synthesis (CTS) and Optimization Aprisa's sophisticated CTS engine handles scenarios for complex designs. Optimizing for both area and leakage power, it minimizes the number of buffers. The CTS engine does optimization for skew, minimization of global, local and inter-clock skew and supports useful local skew control for overall timing optimization. In addition, the engine supports: … Route-based clock tree optimization." Aprisa Webpage. "The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing 'Total Net Delay' for the design is key to the Aprisa route-centric system. ***Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure.*** The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently." Aprisa Whitepaper (emphasis added). "The figures below shows [sic] the RSE engine at work on critical nets. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. ***These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase***, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not

	have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser." Aprisa Whitepaper (emphasis added). In order to "route millions of nets" using a "global route engine", a subset of global nets must be identified. On information and belief, Aprisa's parametric multi-threaded routing for power/ground grid creation feature identifies a subset of power/grounds nets in at least some operating modes. On information and belief, in at least some operating modes, Aprisa does not route all power/ground nets simultaneously and therefore must select a subset with which to start. On information and belief, Aprisa's route-based clock tree optimization feature identifies a subset of clock signal nets in at least some operating modes. On information and belief, in at least some operating modes, Aprisa does not route all clock nets simultaneously and therefore must select a subset with which to start.
routing said subset of global nets using multiple threads, each of said global nets within said subset routed by one of said threads in isolation of said subset's other global nets;	Aprisa routes a first subset of global nets using multiple threads and routes each of the global nets within that subset by one thread in isolation of the subset's other global nets. For example: "Aprisa uses state-of-the-art multi-threading and distributed processing technology to further speed up the process and avoid the exploding runtime issues with modern nanoscale design." Aprisa Webpage. "Global Route and Optimization Aprisa's fast global route engine can route millions of nets in minutes." Aprisa Webpage. "Floorplanning … Parametric multit-headed [sic] routing for power/ground grid creation" Aprisa Webpage. "Key features … Scalable multi-threaded routing." Aprisa Webpage. "Multi-threaded engine with near linear performance. An 8 cpu machine will achieve 7-7.5X the performance of a single CPU. Routes 250K instance in about 5 minutes on an 8 CPU machine." Aprisa Webpage. Aprisa utilizes "multi-threading and distributed processing technology" and handles circuit designs with multiple global nets. The application of "multi-threading" to circuits with multiple global nets means global nets will the routed independently of another global net.
identifying a second subset of said global nets;	Aprisa identifies a second subset of global nets. For example: See the above discussion of the "identifying a subset of said global nets" limitation. On information and belief, Aprisa's parametric multi-threaded routing for power/ground grid creation feature identifies a second subset of power/grounds nets in at least some operating modes. On information and belief, in at least some operating modes, Aprisa does not route all power/ground nets simultaneously and therefore must select a first subset with which to start and a second subset with which to continue processing. On information

	and belief, Aprisa's route-based clock tree optimization feature identifies a subset of clock signal nets in at least some operating modes. On information and belief, in at least some operating modes, Aprisa does not route all clock nets simultaneously and therefore must select a first subset with which to start and a second subset with which to continue processing.
routing said second subset of global nets using said multiple threads, each of said global nets within said second subset routed by one of said threads in isolation of said second subset's other global nets but in respect of the routes of said subset of global nets.	Aprisa routes a second subset of global nets using multiple threads and routes each of the global nets within that subset by one thread in isolation of the second subset's other global nets but in respect of the routes of the first subset of global nets. For example: See the above discussion of the "routing said subset of global nets using multiple threads,…" limitation. "Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electromigration. Every step of the flow is aware of, and can react to the effects of routing on the design." Aprisa Whitepaper. Aprisa utilizes "multi-threading and distributed processing technology" and handles circuit designs with multiple global nets. The application of "multi-threading" to the second subset of nets means that the second subset of global nets will the routed independently of one another. On information and belief, Aprisa's router-centric solution which considers route effects means that the second subset is routed in respect of the routes of the first subset of global nets.

67. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '614 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa to directly infringe the '614 Patent. In particular, Avatar had actual knowledge of the '614 Patent no later than the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa to directly infringe one or more claims of the '614 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and uses thereof, including infringing uses (*see, e.g.,* Aprisa Webpage); Avatar knows (or should know) that its actions will induce Aprisa users to directly infringe one or more claims of the '614 Patent; and users of Aprisa directly infringe one or more claims of the '614 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that

installation and use of Aprisa will infringe one or more claims of the '614 Patent and that Avatar's customers then directly infringe one or more claims of the '614 Patent by installing and using Aprisa in accordance with Avatar's product literature. *See, e.g.*, Aprisa Webpage.

68. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '614 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or selling components that contribute to the direct infringement of one or more claims of the '614 Patent. In particular, Avatar had actual knowledge of the '614 Patent no later than the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the '614 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the '614 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the '614 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of routing a semiconductor chip's global nets. Aprisa is a material component of the computer-implemented method that meets one or more claims of the '614 Patent. *See, e.g.*, Aprisa Webpage. Further, Avatar especially made and/or adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the '614 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar's customers directly infringe one or more claims of the '614 Patent by installing Aprisa on a computer device and using Aprisa to perform global net routing as part of a place-and-route process. *See* Aprisa Webpage.

69. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar's infringement of the '614 Patent, including, without limitation, a reasonable royalty and lost profits.

70. Avatar's infringement of the '614 Patent is also willful because Real Intent had actual knowledge of the '614 Patent or was willfully blind to its existence no later than upon receipt of a June 16, 2020 letter sent by counsel for Synopsys to counsel for Avatar informing Avatar that it was infringing on several Synopsys patents, including the '614 Patent; engaged in

the aforementioned activity despite an objectively high likelihood that Real Intent's actions constituted infringement of the '614 Patent; and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

71. Avatar's infringement of the '614 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

72. Avatar's infringement of the '614 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

73. Avatar's infringement of the '614 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

COUNT VI: INFRINGEMENT OF THE '655 PATENT

74. Synopsys incorporates paragraphs 1–73 as if fully set forth herein.

75. On information and belief, Avatar and/or users of the Avatar Aprisa software product have directly infringed (either literally or under the doctrine of equivalents) and continue to directly infringe one or more claims of the '655 Patent by making, using, offering to sell, and/or selling Aprisa within the United States without authority or license, in violation of 35 U.S.C. § 271(a).

76. As just one non-limiting example, set forth below is an exemplary infringement claim chart for claim 1 of the '655 Patent against Aprisa. Synopsys reserves the right to modify this chart, including on the basis of information it learns through discovery.

'655 Patent Claim 1	**Avatar Aprisa**
A method for fixing design requirement violations in a circuit design in multiple scenarios, the method comprising:	Avatar's Aprisa product performs a method of fixing design requirement violations in a circuit design in multiple scenarios. For example: "The core of the technology is the detailed-route-centric architecture and the hierarchical database. Built upon that, there are common 'analysis engines', such as RC extraction, ***DRC engine***, and an advanced, extremely fast timing engine to solve the complex timing issues associated with OCV, SI and MCMM analysis. Those engines support the precision optimization engine which is consistently used across every P&R step. Aprisa uses state-of-the-art multi-threading and distributed processing technology to further speed up the process and avoid the exploding runtime issues with modern nanoscale design." Aprisa Webpage (emphasis added).

	"Key benefits … Easier to apply hierarchical ECO … Fewer rounds of design iterations and ECO's." Aprisa Webpage. "Multi-corner Multi-mode Analysis … Sophisticated mechanism: unlimited number of scenarios are analyzed in either sequential, multi-threaded, or distributed mode Adaptive MCMM automatically groups scenarios and analyzes them in mixed sequential/multi-threaded mode, thus achieves optimal balance of memory usage and run time for any given computation resources. Flexible scenario creation: each scenario has its own mode (SDC), library corner, and RC condition. … Allows different set of "effective scenarios" to be analyzed at different stage of the flow." Aprisa Webpage. "Global Route and Optimization … SI aware timing engine enabling fixing the noise violations where they happen i.e. not an after-thought to fix the SI violations." Aprisa Webpage. "Detailed Route and Optimization Aprisa's detailed router is a hybrid technology. Although the router is gridded, it can route to any off-grid pin when necessary. Unlike other routers which handle lot of DRC as an afterthought, Aprisa router handles all the DRC violations while actually routing the. [sic] Coupled with the router is the precision optimization engine to do route based optimization concurrently to fix SI aware timing. Features … No separate step need to fix SI related timing violation; they get concurrently fixed while doing route based optimization." Aprisa Webpage. "Physical-Aware Scope-based Sign-off (PASS™) timing ECO, which delivers fast physically-aware ECOs and timing closure based on sign-off timing information and scope-based timing analysis technology. PASS dramatically reduces memory and run time requirements while providing far fewer ECO loops than traditional ECO methods." BusinessWire (May 30, 2013), https://www.businesswire.com/news/home/20130530005848/en/ATopTech-Introduces-New-Technologies-Aprisa-Apogee-Physical. Aprisa provides a method or methods of fixing circuit design violations such as noise violations, DRC violations, and timing violations and also handles unlimited number of scenarios.
receiving a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario;	Aprisa receives a scenario image, wherein the scenario image stores parameter values for circuit objects in a scenario. For example: "Key features *New* detailed-route-centric architecture and hierarchical database." Aprisa Webpage. "Interconnect Centric 'Precision Optimization' Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. This optimization happens through out the flow, during placement, CTS, and both global

	route and detailed routing." Aprisa Webpage. "Clock Tree Synthesis (CTS) and Optimization Aprisa's sophisticated CTS engine handles scenarios for complex designs." Aprisa Webpage. "Multi-corner Multi-mode Analysis … Sophisticated mechanism: unlimited number of scenarios are analyzed in either sequential, multi-threaded, or distributed mode Adaptive MCMM automatically groups scenarios and analyzes them in mixed sequential/multi-threaded mode, thus achieves optimal balance of memory usage and run time for any given computation resources. Flexible scenario creation: each scenario has its own mode (SDC), library corner, and RC condition. … Allows different set of 'effective scenarios' to be analyzed at different stage of the flow." Aprisa Webpage. "Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. Nothing gets lost in translation between flow steps." Aprisa Whitepaper. "Features … Database level access for manipulating netlist hierarchy within physical design environment." Aprisa Webpage. "Physical-Aware Scope-based Sign-off (PASS™) timing ECO, which delivers fast physically-aware ECOs and timing closure based on sign-off timing information and scope-based timing analysis technology. PASS dramatically reduces memory and run time requirements while providing far fewer ECO loops than traditional ECO methods." BusinessWire (May 30, 2013), https://www.businesswire.com/news/home/20130530005848/en/ATopTech-Introduces-New-Technologies-Aprisa-Apogee-Physical. Aprisa is designed to handle multiple scenarios for complex designs, which entails receiving a scenario image. On information and belief, Aprisa's representation of each scenario image in Aprisa's Unified Data Model includes parameter values for circuit objects in that scenario, such as for example, parasitic values and timing values.
receiving a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios; and	Aprisa receives a multi-scenario engineering change order (ECO) database, wherein the multi-scenario ECO database stores a subset of parameter values for a subset of circuit objects in the multiple scenarios. For example: "The core of the technology is the detailed-route-centric architecture and the hierarchical database. Built upon that, there are common 'analysis engines', such as RC extraction, ***DRC engine***, and an advanced, extremely fast timing engine to solve the complex timing issues associated with OCV, SI and MCMM analysis." Aprisa Webpage (emphasis added). "Key benefits … Easier to apply hierarchical ECO … Fewer rounds of design iterations and ECO's." Aprisa Webpage. "Interconnect Centric 'Precision Optimization' Precision optimization allows Aprisa to do optimization based on much

	more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing." Aprisa Webpage. "Multi-corner Multi-mode Analysis … Sophisticated mechanism: unlimited number of scenarios are analyzed in either sequential, multi-threaded, or distributed mode Adaptive MCMM automatically groups scenarios and analyzes them in mixed sequential/multi-threaded mode, thus achieves optimal balance of memory usage and run time for any given computation resources. Flexible scenario creation: each scenario has its own mode (SDC), library corner, and RC condition. … Allows different set of 'effective scenarios' to be analyzed at different stage of the flow." Aprisa Webpage. "Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. Nothing gets lost in translation between flow steps." Aprisa Whitepaper. "Features … Database level access for manipulating netlist hierarchy within physical design environment." Aprisa Webpage. "Physical-Aware Scope-based Sign-off (PASS™) timing ECO, which delivers fast physically-aware ECOs and timing closure based on sign-off timing information and scope-based timing analysis technology. PASS dramatically reduces memory and run time requirements while providing far fewer ECO loops than traditional ECO methods." BusinessWire (May 30, 2013), https://www.businesswire.com/news/home/20130530005848/en/ATopTech-Introduces-New-Technologies-Aprisa-Apogee-Physical. Aprisa automatically groups scenarios for analysis, which means that engineering change orders resulting from that process include a multi-scenario engineering change order database. On information and belief, Aprisa's representation of each scenario image in Aprisa's Unified Data Model includes parameter values for circuit objects in that scenario, such as for example, parasitic values and timing values. On information and belief, engineering change order databases do not include all circuit objects, but rather a subset relevant to the ECO, and do not contain all parameter values, but rather subset relevant to the ECO.
determining, by using one or more processors, an ECO to fix one or more design requirement violations, wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based	Aprisa determines an ECO to fix one or more design requirement violations, wherein said determining includes estimating parameter values for circuit objects in at least some of the multiple scenarios based on parameter values stored in the scenario image and the multi-scenario ECO database. Aprisa operates on one or more processors. For example: "The core of the technology is the detailed-route-centric architecture and the hierarchical database. Built upon that, there

on parameter values stored in the scenario image and the multi-scenario ECO database.	are common 'analysis engines', such as RC extraction, ***DRC engine***, and an advanced, extremely fast timing engine to solve the complex timing issues associated with OCV, SI and MCMM analysis." Aprisa Webpage (emphasis added). "Physical-Aware Scope-based Sign-off (PASS™) timing ECO, which delivers fast physically-aware ECOs and timing closure based on sign-off timing information and scope-based timing analysis technology. PASS dramatically reduces memory and run time requirements while providing far fewer ECO loops than traditional ECO methods." BusinessWire (May 30, 2013), https://www.businesswire.com/news/home/20130530005848/en/ATopTech-Introduces-New-Technologies-Aprisa-Apogee-Physical. "Interconnect Centric 'Precision Optimization' Precision optimization allows Aprisa to do optimization based on much more accurate information than tools in the past. Rather than using very pessimistic models or using a margin based approach, precision optimization is based on very accurate 2.5D parasitic extraction (which is multi-threaded) and SI analysis that is based on near detail route level accuracy. This optimization happens through out the flow, during placement, CTS, and both global route and detailed routing." Aprisa Webpage. "Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. Nothing gets lost in translation between flow steps." Aprisa Whitepaper. "Features … Database level access for manipulating netlist hierarchy within physical design environment." Aprisa Webpage. Aprisa's DRC engine and PASS feature determine engineering change orders to fix one or more DRC violations. On information and belief, to determine whether changes are suitable for the design and will resolve the DRC, Aprisa's DRC engine estimates parameter values for circuit objects in some or all of the multiple scenarios. Those estimations are based on information received, which include parameter values stored in the scenario image and the multi-scenario ECO database.

77. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '655 Patent, in violation of 35 U.S.C. § 271(b), by actively inducing users of Aprisa to directly infringe the '655 Patent. In particular, Avatar had actual knowledge of the '655 Patent no later than the filing of this complaint; Avatar intentionally causes, urges, or encourages users of Aprisa to directly infringe one or more claims of the '655 Patent by promoting, advertising, and instructing customers and potential customers about Aprisa and uses thereof, including infringing uses (*see, e.g.*, Aprisa Webpage); Avatar knows (or should know)

that its actions will induce Aprisa users to directly infringe one or more claims of the '655 Patent; and users of Aprisa directly infringe one or more claims of the '655 Patent. For example, at a minimum, Avatar has supplied and continues to supply Aprisa to customers while knowing that installation and use of Aprisa will infringe one or more claims of the '655 Patent and that Avatar's customers then directly infringe one or more claims of the '655 Patent by installing and using Aprisa in accordance with Avatar's product literature. *See, e.g.,* Aprisa Webpage.

78. Additionally and/or alternatively, Avatar has indirectly infringed and continues to indirectly infringe the '655 Patent, in violation of 35 U.S.C. § 271(c), by offering to sell and/or selling components that contribute to the direct infringement of one or more claims of the '655 Patent. In particular, Avatar had actual knowledge of the '655 Patent no later than the filing of this complaint; Avatar offers for sale and/or sells Aprisa, which is a material component of the '655 Patent and is not a staple article of commerce suitable for substantial non-infringing use; Avatar knows (or should know) that Aprisa was especially made or especially adapted for use in an infringement of the '655 Patent; and users of devices that comprise Aprisa directly infringe one or more claims of the '655 Patent. For example, Avatar has offered and offers to sell and/or has sold and sells Aprisa to customers for installation on computers in order to perform a computer-implemented method of fixing design requirement violations in a circuit design in multiple scenarios. Aprisa is a material component of the computer-implemented method that meets one or more claims of the '655 Patent. *See, e.g.,* Aprisa Webpage. Further, Avatar especially made and/or adapted Aprisa for use in computers in order to perform a computer-implemented method that meets one or more claims of the '655 Patent, and Aprisa is not a staple article of commerce suitable for substantial non-infringing use. Avatar's customers directly infringe one or more claims of the '655 Patent by installing Aprisa on a computer device and using Aprisa to fix design requirement violations in multiple scenarios as part of a place-and-route process. *See* Aprisa Webpage.

79. Synopsys is entitled to recover from Avatar all damages that Synopsys has sustained as a result of Avatar's infringement of the '655 Patent, including, without limitation, a reasonable royalty and lost profits.

80. Avatar's infringement of the '655 3 Patent is also willful because Real Intent had actual knowledge of the '655 Patent or was willfully blind to its existence no later than upon receipt of a June 16, 2020 letter sent by counsel for Synopsys to counsel for Avatar informing Avatar that it was infringing on several Synopsys patents, including the '655 Patent; engaged in the aforementioned activity despite an objectively high likelihood that Real Intent's actions constituted infringement of the '655 Patent; and this objectively defined risk was either known or so obvious that it should have been known to Avatar.

81. Avatar's infringement of the '655 Patent was and continues to be willful and deliberate, entitling Synopsys to enhanced damages.

82. Avatar's infringement of the '655 Patent is exceptional and entitles Synopsys to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

83. Avatar's infringement of the '655 Patent has caused irreparable harm, including the loss of market share, to Synopsys and will continue to do so unless enjoined by this Court.

RELIEF SOUGHT

Wherefore, Synopsys respectfully requests:

A. Judgment be entered that Avatar infringed one or more claims of the '640 Patent, and that such infringement is willful;

B. Judgment be entered that Avatar infringed one or more claims of the '863 Patent and that such infringement is willful;

C. Judgment be entered that Avatar infringed one or more claims of the '567 Patent and that such infringement is willful;

D. Judgment be entered that Avatar infringed one or more claims of the '915 Patent and that such infringement is willful;

E. Judgment be entered that Avatar infringed one or more claims of the '614 Patent and that such infringement is willful;

F. Judgment be entered that Avatar infringed one or more claims of the '655 Patent and that such infringement is willful;

G. An injunction enjoining Avatar, its officers, agents, servants, employees,

successors, assigns and all persons acting in concert with it or them, from directly or indirectly engaging in acts that infringe the Patents-in-Suit;

H. An award of damages sufficient to compensate Synopsys for Avatar's patent infringement pursuant to 35 U.S.C. §§ 284–285, including an enhancement of damages on account of Avatar's willful infringement;

I. An award of attorneys' fees pursuant to 35 U.S.C. § 285;

J. Costs and expenses in this action; and

K. Any and all other legal or equitable relief that the Court deems just and proper.

Dated: July 6, 2020

Respectfully submitted,

HOGAN LOVELLS US LLP

By: /s/ *Krista S. Schwartz*
Krista S. Schwartz

Attorneys for Plaintiff
Synopsys, Inc.

JURY TRIAL DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Synopsys demands a trial by jury of all issues triable of right by jury.

Dated: July 6, 2020

Respectfully submitted,

HOGAN LOVELLS US LLP

By: /s/ *Krista S. Schwartz*
Krista S. Schwartz

Attorneys for Plaintiff
Synopsys, Inc.