IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF TEXAS
WACO DIVISION

FG SRC LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Case No. 6:20-cv-00315-ADA JURY TRIAL DEMANDED

PLAINTIFF'S FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff FG SRC LLC ("SRC") files this First Amended Complaint for Patent Infringement ("Complaint") against Defendant Intel Corporation ("Defendant" or "Intel"). Plaintiff alleges as follows:

I. NATURE OF THE ACTION

1. This is an action for infringement of U.S. Patent No. 7,149,867 (the "'867 patent").

2. SRC is a limited liability company incorporated in Delaware and is the successor to SRC Computers, LLC ("SRC Computers").

3. Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business in the Western District of Texas, including at 1300 S. Mopac Expressway, Austin, Texas 78746.

II. JURISDICTION

4. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.*, including 35 U.S.C. §§ 271, 281, 283, 284, and 285. This is a patent infringement lawsuit over which this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. This United States District Court for the Western District of Texas has general and specific personal jurisdiction over Defendant because Defendant is present in and transacts and conducts business in and with residents of this District and the State of Texas. Defendant has also purposefully and voluntarily availed itself of the privileges of conducting business in the United States, the State of Texas, and the Western District of Texas by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in Texas and this District.

6. Defendant maintains regular and established places of business in the State of Texas and in the Western District of Texas.

7. Plaintiff's causes of action arise, at least in part, from Defendant's contacts with and activities in the State of Texas and this District. Upon information and belief, Defendant committed acts of infringement in this District giving rise to this action and does business in this District, including making sales and/or providing services and support for its customers in this District. Defendant purposefully and voluntarily sold one or more of its infringing products with the expectation that they would be purchased by consumers in this District. These infringing products have been and continue to be purchased by consumers in this District. Defendant committed acts of patent infringement within the United States, the State of Texas, and the Western District of Texas.

8. Defendant, directly and/or through intermediaries, uses, sells, offers for sale, ships, distributes, advertises, and/or otherwise promotes products in this District and the State of Texas. Defendant regularly conducts and solicits business in, engages in other persistent

courses of conduct in, and/or derives substantial revenue from goods and services provided to residents of this District and the State of Texas.

III. VENUE

9. Venue is proper in this District under 35 U.S.C. § 1400(b) because: (1) Defendant has a physical place located in this District, (2) it is a regular and established place of business, and (3) it belongs to Defendant. *See In re Cray Inc.*, 871 F.3d 1355, 1360 (Fed. Cir. 2017).

10. Defendant maintains several facilities, which it refers to as campuses, in this District. https://www.intel.com/content/www/us/en/location/usa.html.

11. Defendant maintains a campus at 1300 S. Mopac Expressway, Austin, Texas 78746. This is a regular and established place of business belonging to Defendant.

12. Defendant maintains a campus at 6500 River Place Blvd, Bldg. 7, Austin, Texas 78730. This is a regular and established place of business belonging to Defendant.

13. Defendant maintains a campus at 5113 Southwest Parkway, Austin, Texas 78735. This is a regular and established place of business belonging to Defendant.

14. Defendant operates its Programmable Solutions Group ("PSG") in this District.

15. Members of Defendant's PSG work in this District.

16. Members of Defendant's PSG work at one or more of its campuses in Austin, Texas.

17. Defendant acquired Altera Corporation ("Altera") in December 2015.

18. Defendant purchased Altera for approximately $16.7 billion.

19. Defendant acquired Altera at least in part because it was a "leading provider of field-programmable gate array (FPGA) technology." https://www.sec.gov/Archives/edgar/data/50863/000119312515414642/d105836dex991.htm.

20. Altera is now part of Intel. *Id.*

21. PSG was formed after Intel's acquisition of Altera. *Id.*

22. Altera was headquartered within the State of Texas at 3400 Waterview Parkway, #300, Richardson, Texas 75080.

23. Altera maintained a regular and established place of business at 9442 N. Capital of Texas Hwy, #1-850, Austin, Texas 78759.

24. Altera maintained a regular and established place of business at 5113 Southwest Pkwy, Austin, Texas 78735.

25. As part of Intel, PSG creates programmable logic devices, including FPGAs. https://jobsearcher.com/j/system-validation-engineering-intern-at-intel-in-austin-tx-AZGgGE?utm_campaign=google_jobs_apply&utm_source=google_jobs_apply&utm_medium=organic.

26. Intel was actively recruiting a System Validation Engineering Intern (the "Intern"), in this District, as of March 16, 2019. https://jobsearcher.com/j/system-validation-engineering-intern-at-intel-in-austin-tx-AZGgGE?utm_campaign=google_jobs_apply&utm_source=google_jobs_apply&utm_medium=organic.

27. Intel was or is recruiting the Intern to work in its PSG group. *Id.*

28. Intel was or is recruiting the Intern to work in its PSG group in Austin, Texas. *Id.*

29. Intel was actively recruiting a Network Performance and Analytics Engineer (the "Network Engineer") to work in this District as of April 11, 2020. https://jobsearcher.com/j/jr0132726-network-performance-and-analytics-engineer-at-intel-corporation-in-austin-texas-DDQVad.

30. One of the posted requirements for the Analytics Engineer is that said engineer has "Familiarity with Intel Processors, FPGA & NICs within a data center context." https://jobsearcher.com/j/jr0132726-network-performance-and-analytics-engineer-at-intel-corporation-in-austin-texas-DDQVad.

31. Intel was actively recruiting a Systems Performance and Analytics Engineer (the "Systems Engineer") to work in this District as of April 11, 2020. https://jobsearcher.com/j/jr0132727-systems-performance-and-analytics-engineer-at-intel-corporation-in-austin-texas-LW6Vdl.

32. One of the posted requirements for the Systems Engineer is that said engineer has "Familiarity with Intel Processors, FPGA & NICs within a data center context."

33. Intel was actively recruiting a Firmware Engineering Manager (the "Engineering Manager"), in this District, as of February 29, 2020. https://jobsearcher.com/j/firmware-engineering-manager-at-intel-corporation-in-austin-texas-2dBgdV?utm_campaign=google_jobs_apply&utm_source=google_jobs_apply&utm_medium=organic.

34. Intel was or is recruiting the Engineering Manager to work in its PSG group. *Id.*

35. Intel was or is recruiting the Engineering Manager to work in its PSG group in Austin, Texas. *Id.*

IV. FG SRC LLC AND DEFENDANT'S PRODUCTS

A. FG SRC LLC

36. SRC Computers was co-founded by Seymour R. Cray, Jim Guzy, and Jon Huppenthal in 1996 to produce unique high-performance computer systems using Intel's Merced microprocessor.

37. SRC is the successor to SRC Computers.

38. Jim Guzy is a co-founder of Intel Corporation and served on Intel's board for 38 years.

39. Mr. Guzy was named to Forbes Midas List, which surveys the top tech deal makers in the world, in 2006 and 2007.

40. Seymour Cray was an American electrical engineer and supercomputer architect who designed a series of computers that were the fastest in the world for decades.

41. Mr. Cray has been credited with creating the supercomputing industry.

42. Unfortunately, Mr. Cray died shortly after founding SRC Computers.

43. But his legacy was carried on by Jon Huppenthal and a talented team of engineers that worked with Mr. Cray and Mr. Huppenthal for decades.

44. SRC Computers' focus was creating easy-to-program, general-purpose reconfigurable computing systems.

45. In early 1997, Mr. Huppenthal and his team realized that the microprocessors of the day had many shortcomings relative to the custom processing engines that they were used to.

46. As a result, they decided to incorporate dedicated processing elements built from Field Programmable Gate Arrays ("FPGAs") and that idea quickly evolved into a novel system combining reconfigurable processors and CPUs.

47. SRC Computers' heterogenous system had 100x performance, $1/50^{th}$ of the operating expense, $1/100^{th}$ of the power usage, and required $1/500^{th}$ of the space of more traditional computer systems.

48. SRC Computers' proven systems are used for some of the most demanding military and intelligence applications, including the simultaneous real-time processing and analysis of

radar, flight and mission data collected from a variety of aerial vehicles in over 1,000 successful counter-terrorism and counter-insurgency missions for the U.S. Department of Defense.

49. SRC Computers offered its first commercial product in 2015 called the Saturn 1 server.

50. The Saturn 1 was 100 times faster than a server with standard Intel microprocessors while using one percent of the power.

51. The Saturn 1 was designed to be used in HP's Moonshot server chassis for data centers.

52. SRC Computers has had over 30 U.S. patents issued for its innovative technology.

53. SRC Computers' patent portfolio covers numerous aspects of reconfigurable computing and has more than 2,090 forward citations.

54. In February 2016, SRC Computers restructured into three new entities: a corporate parent FG SRC LLC, an operating company DirectStream, LLC ("DirectStream"), and a licensing entity SRC Labs, LLC.

B. Accused Products

55. In this complaint, Plaintiff accuses the following Intel products (collectively "Accused Products") of infringing the '867 patent:

(a) Intel FPGA PACs (Programmable Acceleration Cards) including the Intel FPGA PAC D5005; Intel FPGA PAC N3000, and Intel FPGA PAC with Arria 10 GX FPGA;

(b) Intel FPGA development kits including the Intel Stratix SoC Development Kit;

(c) Agilex F-Series FPGA and SoC FPGA products including the AGF 004, AGF 006, AGF 008, AGF 012, AGF 014, AGF 022, and AGF 027;

(d) Agilex I-Series SoC FPGA products including the AGI 022 and AGI 027;

(e) Stratix 10 GX FPGA products including the GX 400, GX 500, GX 650, GX 850, GX 1100, GX 1650, GX 2100, GX 2500, GX 2800, GX 1660, GX 2110, GX 10M, GX 4500, and GX 5500;

(f) Stratix 10 SX SoC FPGA products including the SX 400, SX 500, SX 650, SX 850, SX 1100, SX 1650, SX 2100, SX 2500, SX 2800, SX 4500, and SX 5500;

(g) Stratix 10 TX SoC FPGA products including the TX 400, TX 850, TX 1100, TX 1650, TX 2100, TX 2500, and TX 2800;

(h) Stratix 10 MX FPGA products including the MX 1650 and MX 2100;

(i) Stratix 10 DX SoC FPGA products including the DX 1100, DX 2100, and DX 2800;

(j) Arria 10 GT FPGA products including the GT 900 and GT 1150;

(k) Arria 10 GX FPGA products including the GX 160, GX 220, GX 270, GX 320, GX 480, GX 570, GX 660, GX 900, and GX 1150;

(l) Arria 10 SX SoC FPGA products including the SX 160, SX 220, SX 270, SX 320, SX 480, SX 570, and SX 660;

(m) Cyclone 10 GX FPGA products including the 10CX085, 10CX105, 10CX150, and 10CX220;

(n) Arria V GX FPGA products including the 5AGXA1, 5AGXA3, 5AGXA5, 5AGXA7, 5AGXB1, 5AGXB3, 5AGXB5, and 5AGXB7;

(o) Arria V GT FPGA products including the 5AGTC3, 5AGTC7, 5AGTD3, and 5AGTD7;

(p) Arria V GZ FPGA products including the 5AGZE1, 5AGZE3, 5AGZE5, and 5AGZE7;

(q) Arria V SX SoC FPGA products including the 5ASXB3 and 5ASXB5;

(r) Arria V ST SoC FPGA products including the 5ASTD3 and 5ASTD5;

(s) Cyclone 10 LP FPGA products including the 10CL006, 10CL010, 10CL016, 10CL025, 10CL040, 10CL055, 10CL080, and 10CL120;

(t) Cyclone V E FPGA products including the 5CEA2, 5CEA4, 5CEA5, 5CEA7, and 5CEA9;

(u) Cyclone V GX FPGA products including the 5CGXC3, 5CGXC4, 5CGXC5, 5CGXC7, and 5CGXC9;

(v) Cyclone V GT FPGA products including the 5CGTD5, 5CGTD7, and 5CGTD9;

(w) Cyclone V SE SoC FPGA products including the 5CSEA2, 5CSEA4, 5CSEA5, and 5CSEA6;

(x) Cyclone V SX SoC FPGA products including the 5CSXC2, 5CSXC4, 5CSXC5, and 5CSXC6;

(y) Cyclone V ST SoC FPGA products including the 5CSTD5 and 5CSTD6; and

(z) Max 10 FPGA products including the 10M02, 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50.

56. Each of the Accused Products includes an FPGA.

57. In contrast to a purpose-built chip, which is designed with a single function in mind and then hardwired to implement it, an FPGA is more flexible.

58. With an FPGA, a large majority of the electrical functionality can be changed; more specifically, said functionality can be changed by the design engineer, changed during the PCB assembly process, or even changed after the equipment has been shipped to customers out in the field.

59. FPGAs provide off-load and acceleration functions to CPUs, effectively speeding up the entire system performance.

60. FPGAs provide benefits to designers of many types of electronic equipment, ranging from smart energy grids, aircraft navigation, automotive driver's assistance, medical ultrasounds and data center search engines – just to name a few.

61. Today's FPGAs include on-die processors, transceiver I/O's at 28 Gbps (or faster), RAM blocks, DSP engines, and more. More functions within the FPGA mean fewer devices on the circuit board, increasing reliability by reducing the number of device failures.

62. FPGA functionality can change upon every power-up of the device.

63. Programming an FPGA is a matter of connecting them up to create the desired logical functions (AND, OR, XOR, and so forth) or storage elements (flip-flops and shift registers).

64. Unlike a CPU, which is essentially serial (with a few parallel elements) and has fixed-size instructions and data paths (typically 32 or 64 bit), an FPGA can be programmed to perform many operations in parallel, and the operations themselves can be of almost any width, large or small.

65. The highly parallelized model in FPGAs is ideal for building custom accelerators to process computer-intensive problems.

66. Properly programmed, an FPGA has the potential to provide a 30x or greater speedup to many types of genomics, seismic analysis, financial risk analysis, big data search, and encryption algorithms and applications.

67. Defendant's customers can use FPGAs to accelerate its applications more than 30x when compared with servers that use CPUs alone.

68. The speed increase is a result of the FPGAs handling computer-intensive, deeply pipelined, hardware-accelerated operations, which also allows for highly parallelized computing.

V. MARKING AND NOTICE

A. Marking and Constructive Notice to Defendant.

69. SRC Computers complied with 35 U.S.C. § 287 by (i) placing the required notice on all, or substantially all, of its products made, offered for sale, sold, or imported into the United States, or (ii) providing actual notice to Defendant.

70. For example, SRC Computers placed notices such as the following on all, or substantially all, of its products since at least February 19, 2013:[1]

[1] *E.g.,* https://web.archive.org/web/20100930014237/http://www.srccomp.com/techpubs/patentedtech.asp.

71. The website listed in the notice, WWW.SRCCOMP.COM/ TECHPUBS/PATENTEDTECH.ASP, stated the following:

> **SRC® PATENTED TECHNOLOGY**
>
> SRC Computers holds fundamental U.S. and foreign patents covering hardware and software techniques for vastly accelerating data processing through the use of reconfigurable elements comprising one or more Direct Execution Logic blocks operating in conjunction with one or more commodity microprocessors.
>
> SRC patented technology, with filing dates back to 1997, also includes a number of general applications of Direct Execution Logic computing systems for parallelizing the execution of user-defined algorithms including acceleration of web site access and processing.
>
> SRC Computers has exclusive rights to the following patents:

72. The website also listed at least the following patents since September 30, 2010. The ’867 patent, asserted in this case, is highlighted:

Patent #	Patent Title
6,026,459	System and method for dynamic priority conflict resolution in a multi-processor computer system having shared memory resources
6,076,152	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem
6,247,110	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem
6,295,598	Split directory-based cache coherency technique for a multi-processor computer system
6,339,819	Multiprocessor with each processor element accessing operands in loaded input buffer and forwarding results to FIFO output buffer
6,434,687	System and method for accelerating web site access and processing utilizing a computer system incorporating reconfigurable processors operating under a single operating system image
6,356,983	System and method providing cache coherency and atomic memory operations in a multiprocessor computer architecture
6,594,736	System and method for semaphore and atomic operation management in a multiprocessor
6,627,985	Reconfigurable processor module comprising hybrid stacked integrated circuit die elements
6,781,226	Reconfigurable processor module comprising hybrid stacked integrated circuit die elements
6,836,823	Bandwidth enhancement for uncached devices
6,941,539	Efficiency of reconfigurable hardware
6,961,841	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem
6,964,029	System and method for partitioning control-dataflow graph representations
6,983,456	Process for converting programs in high-level programming languages to a unified executable for hybrid computing platforms
6,996,656	System and method for providing an arbitrated memory bus in a hybrid computing system
7,003,593	Computer system architecture and memory controller for close-coupling within a hybrid processing system utilizing an adaptive processor interface port
7,124,211	System and method for explicit communication of messages between processes running on different nodes in a clustered multiprocessor system
7,126,214	Reconfigurable processor module comprising hybrid stacked integrated circuit die elements
7,134,120	Map compiler pipelined loop structure

7,149,867	System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware
7,155,602	Interface for integrating reconfigurable processors into a general purpose computing system
7,155,708	Debugging and performance profiling using control-dataflow graph representations with reconfigurable hardware emulation
7,167,976	Interface for integrating reconfigurable processors into a general purpose computing system
7,197,575	Switch/network adapter port coupling a reconfigurable processing element to one or more microprocessors for use with interleaved memory controllers
7,225,324	Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions
7,237,091	Multiprocessor computer architecture incorporating a plurality of memory algorithm processors in the memory subsystem
7,282,951	Reconfigurable processor module comprising hybrid stacked integrated circuit die elements
7,299,458	System and method for converting control flow graph representations to control-dataflow graph representations
7,373,440	Switch/network adapter port for clustered computers employing a chain of multi-adaptive processors in a dual in-line memory module format
7,406,573	Reconfigurable processor element utilizing both coarse and fine grained reconfigurable elements
7,421,524	Switch/network adapter port for clustered computers employing a chain of multi-adaptive processors in a dual in-line memory module format
7,424,552	Switch/network adapter port incorporating shared memory resources selectively accessible by a direct execution logic element and one or more dense logic devices
7,565,461	Switch/network adapter port coupling a reconfigurable processing element to one or more microprocessors for use with interleaved memory controllers
7,620,800	Multi-adaptive processing systems and techniques for enhancing parallelism and performance of computational functions

B. Actual Notice to Defendant.

73. Intel learned of the ’867 patent and its infringement of said patent at least as a result of the filing and/or service of SRC’s Original Complaint for Patent Infringement, which included detailed claim charts illustrating how the Accused Products infringe the ’867 patent. This

complaint additionally provides notice of the '867 patent and infringement by the Accused Products.

74. As discussed in more detail below, Intel knew of the '867 patent before this lawsuit was filed.

75. Between July 2015 and September 2015 SRC Computers and Intel met and corresponded regarding a potential acquisition by Intel of SRC Computers and/or its intellectual property ("IP"), including the '867 patent. Persons involved on behalf of SRC Computers included SRC Computers' chairman and controlling shareholder, Brandon Freeman, and Jon Huppenthal, President and CEO of SRC Computers. Persons involved on behalf of Intel included at least the following individuals: (1) Matthew Hulse, Associate General Counsel & Director, Patent Transactions Group, (2) Trina Van Pelt, Vice President and Managing Director, Strategic Transactions Group, (3) Steve Megli, Vice President and General Manager, Strategic Transactions Group, (4) Bob Nunn, Managing Director, Strategic Transactions Group, (5) Milan Djukic, Strategic Business Development, Strategic Transactions Group, (6) PK Gupta, Engineering Manager, Data Center Group, and (7) Sheldon Bernard, Strategic Business Development, Strategic Transactions Group.

76. A third party, 3LP Advisors, LLC ("3LP"), assisted with discussions on behalf of SRC Computers.

77. In order to assist Intel with reviewing SRC Computers' patent portfolio, at SRC Computers' request, 3LP prepared a presentation entitled "SRC IP Portfolio Overview," which was provided to Intel on or around July 30, 2015.

78. The presentation referenced the '867 patent eight times. An excerpt from the presentation, in which highlighting has been added, follows.

3LP has already identified several patents which appear to be relevant to different areas of the value chain

Patent	Title	Big Data / Cloud Players	HPC FPGA-CPU Systems	Chip Player	Network Card Accel.	Compilers	Tech Category	Citations per year	Expiration (earliest)
US6434687B1	Recon. Computer Business	3	2	0	1	0	Accelerator	2.58	2.7
US6026459A	Conflict Resolution	2	3	1	0	0	Memory Access	1.50	2.9
US7003593B2	Chip Set Connection for MAP	1	3	1	0	0	System Architecture	0.75	2.9
US6961841B2	MAP Continuation in part	2	3	3	1	0	Reconfigurable Processor	0.89	3.2
US6594736B1	Hardware Semaphore Management	2	2	0	0	0	System Architecture	2.27	6.5
US6964029B2	Control/Data Flow Partitioning	2	2	0	1	2	MAP Compiler	3.67	8.0
US7149867B2	Explicit memory access units	2	2	0	1	0	FPGA Configuration	0.89	8.2
US6983456B2	Top Level Compiler	1	2	2	0	3	MAP Compiler	7.88	8.4
US7155602B2	MAP Command List	1	2	2	0	3	FPGA Configuration	1.88	8.5
US7225324B2	Application Acceleration	2	2	0	2	0	Accelerator	3.43	9.1

"Mapping" based on 3LP's review of claim elements

79. Previously, at least between February 2006 and August 2013 SRC Computers and Altera met and/or corresponded on several occasions. During that time, on several occasions SRC Computers made Altera aware of its patent portfolio, which included the '867 patent. Altera employees, including Mike Strickland and Martin Langhammer, participated. On information and belief, Martin Langhammer is currently a Principal Engineer at Intel. *See* https://www.linkedin.com/in/martin-langhammer-8056b17/?originalSubdomain=uk. On information and belief, Mike Strickland is currently a Senior Manager at Altera, which was acquired by Intel. *See* https://www.linkedin.com/in/strickland-michael-2715924/.

80. On or around February 22, 2013, counsel for SRC Computers sent a notice letter to Altera advising that "Our client has recently become aware of Altera's SoC FGPAs which are stated to integrate an ARM-based hard processor system (HPS) consisting of processor,

peripherals, and memory interfaces with the FPGA fabric using a high-bandwidth interconnect backbone. From the information presently available to us, these devices may possibly involve SRC Computers' patented technology."

81. On information and belief, Intel also knew of the '867 patent as a result of its prosecution activities. More specifically, on information and belief, Intel learned of the '867 patent when prosecuting U.S. Patent Application No. 11/314,229 (the "'229 application), which was published as US2007/0143546. During prosecution of the '229 application, the Examiner and Intel discussed US2004/0260884 (the '867 publication")—the publication corresponding to the '867 patent—during an interview, and the Examiner explicitly referenced the '867 publication in a rejection dated April 23, 2013. On information and belief, these prosecution activities would have brought the '867 patent to Intel's attention, particularly in light of the fact that the '867 patent issued well before the interview.

VI. THE '867 PATENT

A. The '867 Patent is Owned by SRC.

82. On January 22, 2020, DirectStream assigned the '867 patent to SRC. The assignment was recorded with the USPTO on January 24 at Reel/Frame 051615/0344.

83. All maintenance fees have been paid to the USPTO to keep the '867 patent enforceable for its full term.

B. Description of the Asserted Patent.

84. The '867 patent is entitled "System and method of enhancing efficiency and utilization of memory bandwidth in reconfigurable hardware" and issued on December 12, 2006.

85. A true and correct copy of the '867 patent is attached as **Exhibit A**.

86. The '867 patent is valid and enforceable.

VII. COUNT ONE: DIRECT INFRINGEMENT OF THE '867 PATENT

87. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

88. Defendant has at no time, either expressly or impliedly, been licensed under the '867 patent.

89. Defendant has and continues to directly infringe the '867 patent by making, using, offering for sale, selling, and/or importing in or into the United States in violation of 35 U.S.C. § 271(a) the Accused Products. For example, on information and belief Defendant tests, manufactures, and uses each of the Accused Products in an infringing manner at least in order to (1) ensure that functionality such as that appearing in SRC's claim charts attached hereto, including but not limited to those portions of the chart describing descriptors appearing in its Embedded Peripherals User Guide, works as described and (2) provide support to its customers and partners, such as members of the FPGA Partner Program, which provides "[t]echnical support for product optimization." *See* https://www.intel.com/content/dam/www/public/us/en/documents/flyers/intel-fpga-partner-program-flyer.pdf.

90. Defendant's direct infringement of the '867 patent by the Accused Products has caused, and will continue to cause, substantial and irreparable damage to Plaintiff. Plaintiff is therefore entitled to an award of damages adequate to compensate for Defendant's infringement, but not less than a reasonable royalty, together with pre- and post-judgment interest and costs as fixed by the Court under 35 U.S.C. § 284.

91. Plaintiff adopts, and incorporates by reference, as if fully stated herein, **Exhibits B through J**, which are claim charts that describe and demonstrate how the Accused Products

infringe exemplary claims of the '867 patent. These charts collectively show that Intel infringes at least claims 1, 3, 4, 9, 11, and 12 of the '867 patent.

VIII. COUNT TWO: INDIRECT INFRINGEMENT OF THE '867 PATENT

92. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

93. Defendant induces infringement under 35 U.S.C. § 271(b) by actively and knowingly aiding and abetting direct infringement by its users.

94. As discussed in § 5.B, Defendant received actual and constructive notice of the '867 patent.

95. Defendant learned of its infringement of the '867 patent at least as a result of the filing of the Original Complaint in this case as well as the filing of the instant complaint.

96. Through at least the filing of the Original Complaint and the instant complaint, and the claim charts attached to both complaints, Defendant learned that its actions would result in users of the Accused Products infringing the '867 patent.

97. For example, the claim charts attached to both complaints show how Defendant's Embedded Peripherals IP User Guide specifically provides users with instructions on using the Accused Devices in an infringing manner, such as by providing instructions regarding descriptors used with said products, and said guide and descriptors are explicitly illustrated in Plaintiff's claim charts.

98. Moreover, Defendant provides training and support to its customers, including through its FPGA Partner Program in which it provides "[t]echnical support for product optimization" such as that shown in Plaintiff's claim charts. *See* https://www.intel.com/content/dam/www/public/us/en/documents/flyers/intel-fpga-

partner-program-flyer.pdf; *see also* https://www.intel.com/content/www/us/en/partner/fpga-innovation-partners/overview.html (listing Intel partners).

99. On information and belief Intel teaches users to optimize applications including optimizing usage of direct memory access, such as that shown by usage of the descriptors in SRC's claim charts.

100. For example, Intel taught its users how to use its FPGA acceleration cards with its OpenVINO toolkit to accelerate vision inference for facial recognition purposes. *See* https://www.youtube.com/watch?v=1GfZpubYm8s.

101. Intel also taught in its Inference Engine Developer Guide how to perform direct memory access using an implementation of a vision processing unit ("VPU"). *See* https://docs.openvinotoolkit.org/latest/_docs_IE_DG_Extensibility_DG_VPU_Kernel.html.

102. The VPU example referenced above teaches:

(1) copying data from the DDR RAM memory (corresponding to the second memory of claim 1) to local (on chip) memory (corresponding to the first memory of claim 1) having 24x higher throughput (showing that the two memories each have a different "characteristic memory bandwidth" as required by claim 1),

(2) "copying used sub-tensor by workgroup into local memory" and

(3) matching the format of data for the calculation.

103. For example, with respect to format matching, step 10 of the example discloses that "Local size is equal to (width of the input sensor, 1, 1) to define a large enough work group to get code automatically vectorized and unrolled, while global size is (width of the input tensor, height of the input sensor, 1)."

104. The example DMA is thus configured to prefetch data required by the algorithm and to match the format and location of data between the memories.

105. Those teachings apply to both the referenced Neural Compute Stick 2 and also to Intel's FPGA products.

106. Intel actively provides support services for its products. An important part of Intel's support services is the Intel Support Community. *See* https://community.intel.com/ Intel hosts Community Forums (including a forum for FPGAs and Programmable Solutions) where members can ask questions and receive support both from Intel engineers and fellow members.

107. In one example Intel Community Forum thread (https://community.intel.com/t5/Nios-II-Embedded-Design-Suite/DMA-vs-MSGDMA/m-p/194510#M45669) a specific video processing example is discussed and suggestions for implementation are sought and offered.

108. The thread provides information on prefetching with the purpose of breaking up an image into lines or into small portions of the frame using an optimized mSGDMA (modular scatter gather DMA) for maximizing throughput in a manner similar to that taught in SRC's claim charts (which illustrate said optimization).

109. More specifically, the advice provided in the forum includes (1) a discussion of why mSGDMA is advantageous (vs. DMA), (2) suggestions on how to break up an image into lines or small portions of the frame, (3) how to optimize the application, and (4) how to use an mSGDMA to move data from SDRAM to the FPGA, and use a second mSGDMA to pull the results back from the FPGA to SDRAM.

110. The problem addressed in the thread referenced above involves moving data from SDRAM (corresponding to the "second memory" in claim 1 of the '867 patent) to FPGA

memory (corresponding to the "first memory" in claim 1 of the '867 patent) using mSGDMA (which corresponds to the "data prefetch unit" of claim 1).

111. The suggestions from the thread of breaking the image into lines or into small portions of the frame corresponds to and meets the requirement of claim 1 that "the first memory and data prefetch unit are configured to conform to needs of the algorithm, and the data prefetch unit is configured to match format and location of data in the second memory."

112. Defendant induces infringement of the '867 patent by marketing the Accused Products and providing documentation (i.e. the Embedded Peripherals User Guide), training, and support (i.e. through its FPGA Partner Program, and support for non-program members) on how to use them in ways that infringe the '867 patent.

113. For example, Defendant induces infringement by providing development kits that allow users to develop, simulate, debug, and compile FGPA applications. Defendant actively provides support services for its development kits, and other products, directly and through the Intel Support Community, in which Intel hosts Community Forums and Intel engineers provide support to users.

114. Defendant specifically intends for users of its products to infringe and knows that its acts will result in patent infringement.

IX. COUNT THREE: WILLFUL INFRINGEMENT OF THE '867 PATENT

115. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

116. As discussed in § 5, Defendant received actual and constructive notice of the '867 patent.

117. Despite knowing of the '867 patent, Defendant continued and continues making, using, offering for sale, and selling the Accused Products resulting in infringement as discussed

in Counts One and Two herein. At least because of its knowledge of the '867 patent and its claims, Intel knew or should have known that its conduct resulted in infringement of several claims of the '867 patent. Moreover, Defendant was provided information regarding its infringement in the Original Complaint and the instant complaint.

118. Defendant continues its infringement of the '867 patent despite its knowing that the asserted claims of the '867 patent were held valid on May 10, 2019 by the Patent Trial and Appeal Board in *inter partes* review proceeding IPR2019-00103.

119. Therefore, Defendant's infringement was intentional or knowing. Defendant knows or should know that its continued activities result in infringement of the '867 patent.

120. Defendant's actions have not been consistent with the standards of behavior in its industry.

121. Defendant made no effort to avoid infringing the '867 patent.

122. Intel's infringement of the '867 patent is willful, deliberate, and/or consciously wrongful, and therefore Plaintiff should receive enhanced damages up to three times the amount of actual damages for Defendant's willful infringement under 35 U.S.C. § 284.

X. CONCLUSION

123. Plaintiff is entitled to recover from Defendant the damages sustained by SRC as a result of Intel's wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

124. Plaintiff has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action.

125. Plaintiff reserves the right to amend, supplement, or modify its allegations of infringement as facts regarding such allegations arise during the course of this case.

XI.JURY DEMAND

126. Plaintiff hereby demands a trial by jury for all causes of action.

XII. PRAYER FOR RELIEF

Plaintiff requests the following relief:

A. A judgment that Defendant has infringed and continues to infringe the '867 patent;

B. A judgment and order requiring Defendant to pay Plaintiff damages under 35 U.S.C. § 284, including treble damages for willful infringement as provided by 35 U.S.C. § 284, and supplemental damages for any continuing post-verdict infringement up until entry of the final judgment with an accounting as needed;

C. A judgment and order requiring Defendant to pay Plaintiff pre-judgment and post-judgment interest on the damages awarded;

D. A judgment and order awarding a compulsory ongoing royalty; and

E. Such other and further relief as the Court deems just and equitable.

Dated: July 9, 2020

Respectfully submitted,

/s/ Alfonso Chan

Michael W. Shore (Texas 18294915)
Alfonso G. Chan (Texas 24012408)
Ari B. Rafilson (Texas 24060456)
William D. Ellerman (24007151)
SHORE CHAN DEPUMPO LLP
901 Main Street, Suite 3300
Dallas, Texas 75202
Telephone: (214) 593-9110
Facsimile: (214) 593-9111

Price Ainsworth (TX Bar No. 00950300)
price@ainsworth-law.com
Law Offices of Price Ainsworth, P.C.
48 East Avenue
Austin, Texas 78701
Tel: (512) 233-1111
Fax: (512) 472-9157

Counsel for Plaintiff FG SRC LLC

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above document has been served upon all counsel of record via the Court's ECF system on July 9, 2020.

/s/ Alfonso Chan
Alfonso Chan