UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

JAMES B. GOODMAN, Plaintiff v. DELL INC., DELL TECHNOLOGIES, INC. and DELL TECHNOLOGIES, LLC, Defendants	**Case No.** 6:20-cv-00703 **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff James B. Goodman ("Plaintiff" or "Goodman") hereby files this Original Complaint for Patent Infringement against Defendants Dell Inc., Dell Technologies, Inc. and Dell Technologies, LLC ("Defendant" or "Dell"), and alleges, on information and belief, as follows:

THE PARTIES

1. James Goodman is an individual residing in the State of Texas.

2. On information and belief, Defendant Dell Inc. is a company organized and existing under the laws of Delaware, with a principal place of business at 1 Dell Way, Round Rock, Texas 78682. Dell Inc. may be served through its registered agent, Corporation Service Company, at 211 E. 7th Street, Suite 620, Austin, Texas 78701.

3. On information and belief, Defendant Dell Technologies, Inc. is a company organized and existing under the laws of Delaware, with a principal place of business at 1 Dell Way, Round

Rock, Texas 78682. Dell Inc. may be served through its registered agent, Corporation Service Company, at 251 Little Falls Drive, Wilmington, Delaware 19808.

4. On information and belief, Defendant Dell Technologies, LLC is a company organized and existing under the laws of Delaware, with a principal place of business at 1 Dell Way, Round Rock, Texas 78682. Dell Inc. may be served through its registered agent, Registered Agents, Ltd., at 1013 Centre Road, Suite 403-A, Wilmington, Delaware 19805.

JURISDICTION AND VENUE

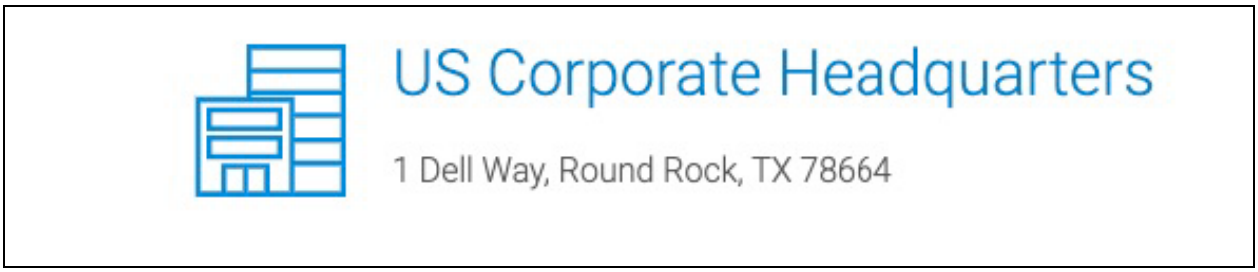
5. This action arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331, 1332 and 1338(a).

6. Defendant has committed acts of infringement in this judicial district.

7. On information and belief, Defendant maintains regular and systematic business interests in this district and throughout the State of Texas including through its representatives, employees and physical facilities.

8. On information and belief, the Court has personal jurisdiction over Defendant because Defendant has committed, and continues to commit, acts of infringement in the State of Texas, has conducted business in the State of Texas, and/or has engaged in continuous and systematic activities in the State of Texas. On information and belief, Defendant's accused instrumentalities that are alleged herein to infringe were and continue to be used, imported, offered for sale, and/or sold in the Western District of Texas.

9. On information and belief, Defendant voluntarily conducts business, has 71 job openings currently in Austin, Texas and Round Rock, Texas within this District, including, but not limited to, its headquarters located at 1 Dell Way, Round Rock, Texas 78682. *See, e.g.:*



Dell website as visited on July 23, 2020:https://www.delltechnologies.com/en-us/contactus.htm.

Dell Corporate Office Address

Dell Corporate Office Headquarters Address, Email, Phone Number

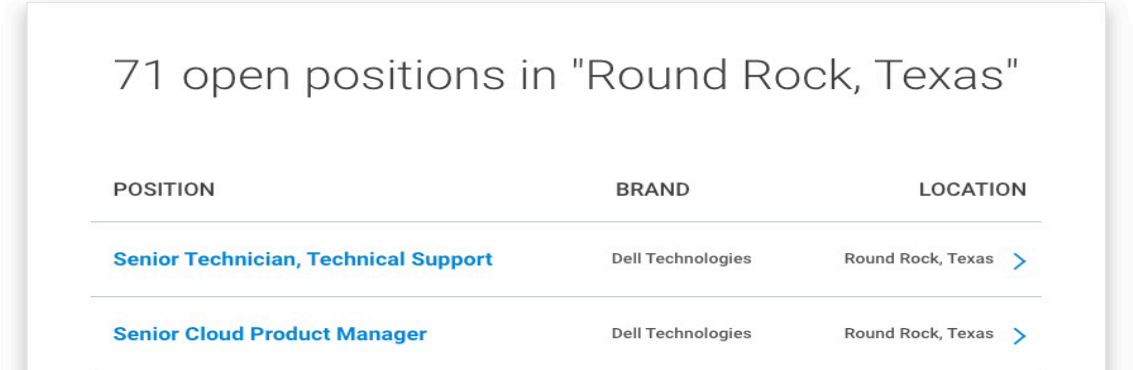
DELL HEADQUARTERS ADDRESS | DELL CORPORATE PHONE NUMBERS	
Dell Headquarters | Dell Round Rock Address	One Dell Way Round Rock, TX 78682, USA.

Source as visited on July 23, 2020 at: https://headquarters-address.com/dell-corporate-office-headquarters-address-email-phone-number/.

71 open positions in "Austin, Texas"

POSITION	BRAND	LOCATION
Senior Principal Front-End Developer - Cloud Platform Team	Dell Technologies	Seattle, Washington
Lead Software Architect / Technical Leader: Endpoint Sensors - Secureworks - Austin, TX; Atlanta, GA; US Remote	Secureworks	Austin, Texas
Senior Security Researcher - Endpoint - Secureworks - Remote	Secureworks	Atlanta, Georgia
Staff Engineer II - Bitfusion (Accelerator Virtualization Group)	VMware	Austin, Texas
Technical Staff: Cloud Architect	Dell Technologies	Seattle, Washington
Senior Product Manager: On-Premise Private & Hybrid Cloud (IaaS-Virtualization & Containers)	Dell Technologies	Austin, Texas

Dell website as visited on July 23, 2020 at: https://jobs.dell.com/search-jobs/Austin%2C%20Texas/375-30225/4/6252001-4736286-4737316-4671654/30x26715/-97x74306/50/2.



71 open positions in "Round Rock, Texas"

POSITION	BRAND	LOCATION
Senior Technician, Technical Support	Dell Technologies	Round Rock, Texas
Senior Cloud Product Manager	Dell Technologies	Round Rock, Texas

Dell website as visited on July 23, 2020 at: https://jobs.dell.com/search-jobs/Round%20Rock%2C%20Texas/375-30225/4/6252001-4736286-4742143-4724129/30x50826/-97x6789/50/2

10. On information and belief, Defendant generates substantial revenue within this District and from the acts of infringement as carried out in this District. As such, the exercise of jurisdiction over Defendant would not offend the traditional notions of fair play and substantial justice.

11. Venue is proper in the Western District of Texas pursuant to 28 U.S.C. § 1400(b) and 28 U.S.C. § 1391(c)(3).

NOTICE OF GOODMANS PATENTS

12. Goodman is the inventor and owner of U.S. Patent No. 4,617,624B2 ("the '624 Patent") entitled "Multiple configuration memory circuit." A copy may be obtained at: https://patents.google.com/patent/US4617624A/

13. Goodman is the inventor and owner of U.S. Patent No. 6,243,315B1 ("the '315 Patent" and "the Patent-in-Suit") entitled "Computer memory system with a low power down mode." A copy may be obtained at: https://patents.google.com/patent/US6243315B1/en?oq=6%2c243%2c315.

14. Goodman is the co-inventor and owner of U.S. Patent No. 6,257,911B1 ("the '911 Patent") entitled "Low insertion force connector with wipe." A copy may be obtained at: https://patents.google.com/patent/US6257911.

15. The foregoing Patents are collectively referred to as "the Goodman Patents."

16. The Goodman Patents are valid, enforceable, and were duly issued in full compliance with Title 35 of the United States Code.

17. Defendants, at least by the date of this Original Complaint, are on notice of the Goodman Patents.

ACCUSED INSTRUMENTALITIES

18. On information and belief, Defendants make, use, import, sell, and/or offer for sale a multitude of products and services as memory systems including, but not limited to: Dell PowerEdge RAID Controller H740P • Eight internal ports • 72-bit DDR4-2133 DRAM interface with 8GB non-volatile cache memory; PERC H740P 8 GB DDR4 2133 Mhz cache; PERC H745 4 GB DDR4 2133 Mhz cache; PERC H745P MX 8 GB DDR4 2133 Mhz cache; H840 8 GB DDR4 2133 Mhz cache; Dell EMC PowerEdge RAID Controller 10 User's Guide H345, H740P, H745, H745P MX, and H840 (individually and collectively, the "Accused Instrumentalities"). On information and belief, the Accused Instrumentalities are made, used, sold, offered for sale, and/or imported in the United States by Defendants. *See e.g.,*

Dell Press Release dated: 1/9/2018, *Dell Pushes Boundaries with New PCs, Software and Partnerships at CES 2018*, located at: https://www.dell.com/learn/us/en/uscorp1/press-releases/2018-01-08-dell-pushes-boundaries-with-new-pcs-software-and-partnerships-at-ces-2018

Dell Latitude 7290 7390 7490 Technical Guidebook (Dated 2018) located at: https://topics-cdn.dell.com/pdf/latitude-12-7290-laptop_reference-guide3_en-us.pdf

Latitude 7290

- DDR4 2400 SDRAM operates at 2133 with Intel 7th Gen
- DDR4 2400 SDRAM operates at 2400 with Intel 8th Gen
- One DIMM slot up to 16 GB

Latitude 7390

- DDR4 2400 SDRAM operates at 2133 with Intel 7th Gen
- DDR4 2400 SDRAM operates at 2400 with Intel 8th Gen
- One DIMM slot up to 16 GB

Latitude 7490

- DDR4 2400 SDRAM operates at 2133 with Intel 7th Gen
- DDR4 2400 SDRAM operates at 2400 with Intel 8th Gen
- 2 DIMM slots supporting up to 32GB

19. Dell makes, offers for sale many computer related products, including desktop computers, laptop computers, servers, and the like, and many of these Dell computer related products incorporate memory products known in the industry as DDR4, memory products. The use of the term “DDR4", to include in the designation of a memory product requires the performance of the memory product to comply with the respective industry standards for performance, and operations.

20. The standards published by the Joint Electron Device Engineering Council Solid State Technology Association (“JEDEC”) state for the respective DDR4, memory products and their variation: "No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met."

21. On information and belief, the use of the terms “DDR4", and variations thereof implies that the respective memory products comply with the corresponding JEDEC Standards.

22. Therefore, the DDR4, memory products and their variations must operate in compliance with the respective standards established by the JEDEC Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201.

23. Any memory product identified as being a DDR4 memory product after June 2017 or a variation thereof including the term “DDR4" must comply with JEDEC Standard JESD79-4B and JESD79-4C.

24. On information and belief, the JEDEC JESD79-4B Standard for DDR4 memory product have several relevant operating capabilities in common when installed in an Dell computer related product, for example: (a) Each memory product has at least two banks of volatile memory, and this is the equivalent of a plurality of volatile solid state memory devices under the doctrine of equivalents; (b) A first external device (supplied by Dell computer related product)

connected to the memory product can provide signals for selectively electrically isolating the address and control lines so that signals on the address and control lines do not reach the memory devices; and (c) A second external device (supplied by Dell computer related product) connected to the memory product can determine when the memory system is not being accessed and can initiate a low power for the memory system wherein the first external device isolates the memory devices and places the memory devices in self refresh mode, thereby reducing the electrical energy drawn from the electrical power supply of the Dell computer related product.

25. On information and belief, the aforementioned Dell computer related products incorporating a JEDEC JESD79-4B Standard DDR4 memory product provide the aforementioned first and second external devices in order to take advantage of the respective operating specification of the memory products, including the low power mode that saves electrical energy while protecting the memory product against potential signals which could damage or corrupt the stored data.

COUNT I
(Infringement of U.S. Patent No. 6,243,315B1)

26. Goodman incorporates the above paragraphs by reference.

27. Defendant has been on notice of the ’315 Patent at least as early as the date it received service of this Original Complaint.

28. On information and belief, Defendant has directly infringed and continue to infringe the ’315 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

29. On information and belief, Defendant, with knowledge of the ’315 Patent, indirectly infringes the ’315 Patent by inducing others to infringe the ’315 Patent. In particular, Defendant

intends to induce customers to infringe the ’315 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

30. On information and belief, Defendant also induces others, including its customers, to infringe the ’315 Patent by providing technical support for the use of the Accused Instrumentalities.

31. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the ‘315 Patent when used as intended.

32. On information and belief, the Accused Instrumentalities infringe at least Claim 5 of the ’315 Patent by providing a memory system for use in a computer system that have a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and capable of being placed in a self refresh mode. For example, the memory systems are DRAM semiconductor microchip. Further, Defendant provides a memory system that is compatible with the dimensions and pin assignments in accordance with JEDEC industry standard 144 PIN SODIMM connector.

33. Further, The Smart Modular Court has determined that a “memory system” is “a system capable of retaining data”. The JESD Standard No. 79-4B, P 12 Section 3.2 Basic Functionality states the DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bank group for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data

transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

34. The Smart Modular Court has determined that "memory device" means "integrated circuit or chip"; that "a plurality of volatile solid state memory devices" means "two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while a electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information" The JESD79-4B at p. 135 refers to the DDR4 SDRAM as being a "chip". See Sec. 4.26 stating, "the chip enters a Refresh cycle". It appears that the DDR4 is a chip. The JESD79-4B at sec. 3.2 p. 12 refers to the DDR4 SDRAM as being at the "internal DRAM core". It appears that the DDR4 internal DRAM core is an integrated circuit. The JESD79-4B at p. 174, Table 81 states the absolute maximum DC Ratings. P. 174, Table 82 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages. It appears that the DDR4 requires a specific range of applied of voltage to retain data.

35. The following is a Claim Chart for Claim 5 of the '315 Patent for the DDR4 memory product:

Claim 1. A memory system for use in a computer system, said memory system comprising: a plurality of volatile solid state memory devices that retain information when an electrical power source is applied to said memory devices within a predetermined voltage range and	The Smart Modular Court has determined that a "memory system" is "**a system capable of retaining data**". The JESD Standard No. 79-4B, P 12 Section 3.2 Basic Functionality states the DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bank group for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. The Smart Modular Court has determined that "memory device" means "**integrated circuit or chip**"; that "a plurality of volatile solid state memory devices" means "**two or more memory devices in the memory system into which data may be written or from which data may be retrieved that retain information while a electrical power source, having a predetermined voltage range, is applied to the memory devices and when the voltage reaches a predetermined threshold outside of that range, the memory devices will no longer retain their current state of information**" The JESD79-4B atp. 135 refers to the DDR4 SDRAM as being a "chip". See Sec. 4.26 stating, "the chip enters a Refresh cycle". It appears that the DDR4 is a chip.

	The JESD79-4B at sec. 3.2 p. 12 refers to the DDR4 SDRAM as being at the "**internal DRAM core**". It appears that the DDR4 **internal DRAM core** is an **integrated circuit**. The JESD79-4B at p. 174, Table 81 states the absolute maximum DC Ratings. P. 174, Table 82 shows the recommended DC Operating Conditions with a minimum and maximum for the DC voltages. It appears that the DDR4 requires a specific range of applied of voltage to retain data.

capable of being placed in a self refresh mode;	The JESD79-4B shows that the DDR4 is capable of being refreshed at the following places: p. 41, Sec. 4.9.5 entitled, "Self Refresh entry and exit"; p. 135, Sec. 4.25.7 entitled, "Refresh Command"; and p. 137, Sec. 4.27 entitled, "Self refresh Operation". JESD79-4B, Page 6 2.7 Input Description shows CKE HIGH activates, and CKE Low **deactivates**, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. NOTE 15 "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins. JESD79-4B, P 137 The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking. The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock. Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge

	state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. JESD79-4B, P137, When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care. JESD79-4B, P6, CKE HIGH activates, and CKE Low **deactivates**, internal clock signals and **device input buffers** and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.

said memory devices having address lines and control lines; a control device for selectively electrically isolating said memory devices from respective address lines and respective control lines so that when said memory devices are electrically isolated, any signals received on said respective address lines and respective control lines do not reach said memory devices; and	The Court has determined that "control device" means "**a device in the memory system that is interposed between the respective address lines and respective control lines that electrically isolates the memory devices**"; that "selectively electrically isolating said memory devices from respective address lines and respective control lines' means "**inhibiting signals on the respective address and respective control lines from the memory devices such that signals on those lines do not arrive at the memory devices**"; that "address lines" mean "**lines that carry signals specifying a memory location to be accessed**"; "control lines" mean "**lines that carry control signals**"; and "control signals" mean "**signals that control the sequence of addressing and the memory mode**". During testing and evaluation of the DDR4, it is necessary for DELL to connect subsystems to the DDR4 using the input and output terminals of the DDR4. Obviously, the use of the term "interposed" relates to the electrically operation of the control device, not a physical positioning. The JESD79-4B at p. 6, Sec. 2.7 identifies **address lines** connected to inputs such as for symbols "BA0-BA2", and "A0-A17". The JESD79-4B uses the terms "command signal", and "command line" for the defined "**control signal**" and "control line". At p. 13, Sec. 2.3, RAS, CAS, WE (line over each) are command inputs. The command signals on the input terminals connect into the DDR4 on "control lines" to control the sequence and memory mode. See Command Truth Table, p. 28, Sec. 4.1

a memory access enable control device coupled to said control device and to said control lines for determining when said memory system is not being accessed and for initiating a low power mode for said memory system wherein said control device electrically isolates said memory devices and places said memory devices in said self refresh mode, thereby reducing the amount of electrical energy being drawn from an electrical power supply for said computer system.	JESD79-4B, p. 137, Sec. 4.27 states, the Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock. Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VRefCA) must be at valid levels. JESD79-4B, Page 29 Sec. 4.2 CKE Truth Table **Table 18** NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state. JESD79-4B, Page 29 Sec. 4.2 CKE Truth Table **Table 18** NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See 4.27 "Self-Refresh Operation" on page 137 and See 4.28

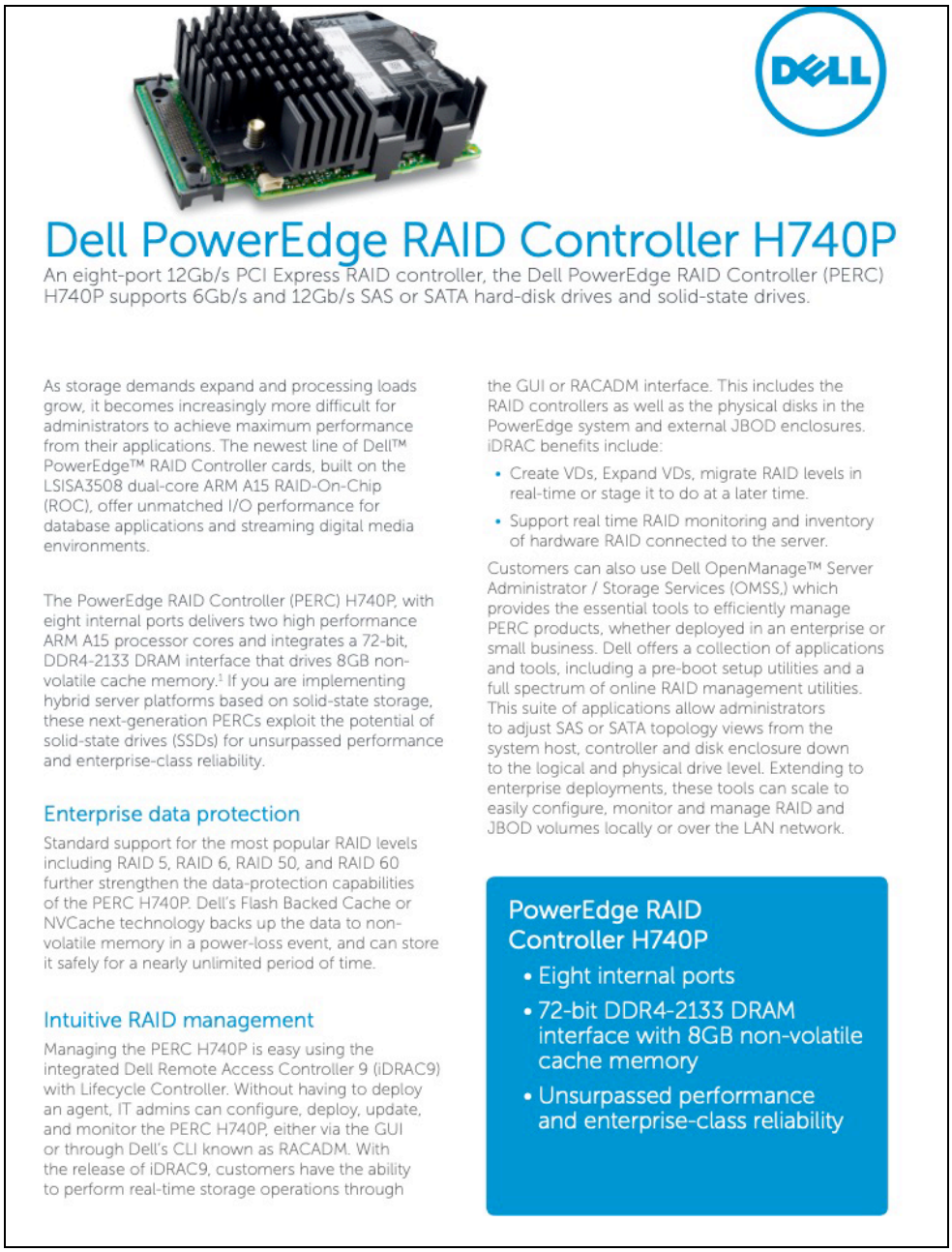
5. The memory system as claimed in claim 1, wherein the memory devices are DRAM semiconductor microchips.	"Power-Down Modes" on page 140. JESD79-4B, Page 6 Sec. 2.7 Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. JESD 79-4B, Page 135, Sec.4.26 Refresh Command The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS_n, RAS_n/A16 and CAS_n/A15 are held Low and WE_n/A14 and ACT_n are held High at the rising edge of the clock, **the chip enters a Refresh cycle**. JESD79-4B, P. 12 Sec. 3.2 Basic Functionality states the DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

	JESD79-4B P.2, Section 2 DDR4 SDRAM Package Pinout and Addressing.

2.7 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c. ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.

JESD79-4B Standard Website as visited on July 28, 2020:
http://www.softnology.biz/pdf/JESD79-4B.pdf.



Dell PowerEdge RAID Controller H740P

An eight-port 12Gb/s PCI Express RAID controller, the Dell PowerEdge RAID Controller (PERC) H740P supports 6Gb/s and 12Gb/s SAS or SATA hard-disk drives and solid-state drives.

As storage demands expand and processing loads grow, it becomes increasingly more difficult for administrators to achieve maximum performance from their applications. The newest line of Dell™ PowerEdge™ RAID Controller cards, built on the LSISA3508 dual-core ARM A15 RAID-On-Chip (ROC), offer unmatched I/O performance for database applications and streaming digital media environments.

The PowerEdge RAID Controller (PERC) H740P, with eight internal ports delivers two high performance ARM A15 processor cores and integrates a 72-bit, DDR4-2133 DRAM interface that drives 8GB non-volatile cache memory.[1] If you are implementing hybrid server platforms based on solid-state storage, these next-generation PERCs exploit the potential of solid-state drives (SSDs) for unsurpassed performance and enterprise-class reliability.

Enterprise data protection

Standard support for the most popular RAID levels including RAID 5, RAID 6, RAID 50, and RAID 60 further strengthen the data-protection capabilities of the PERC H740P. Dell's Flash Backed Cache or NVCache technology backs up the data to non-volatile memory in a power-loss event, and can store it safely for a nearly unlimited period of time.

Intuitive RAID management

Managing the PERC H740P is easy using the integrated Dell Remote Access Controller 9 (iDRAC9) with Lifecycle Controller. Without having to deploy an agent, IT admins can configure, deploy, update, and monitor the PERC H740P, either via the GUI or through Dell's CLI known as RACADM. With the release of iDRAC9, customers have the ability to perform real-time storage operations through the GUI or RACADM interface. This includes the RAID controllers as well as the physical disks in the PowerEdge system and external JBOD enclosures. iDRAC benefits include:

- Create VDs, Expand VDs, migrate RAID levels in real-time or stage it to do at a later time.
- Support real time RAID monitoring and inventory of hardware RAID connected to the server.

Customers can also use Dell OpenManage™ Server Administrator / Storage Services (OMSS,) which provides the essential tools to efficiently manage PERC products, whether deployed in an enterprise or small business. Dell offers a collection of applications and tools, including a pre-boot setup utilities and a full spectrum of online RAID management utilities. This suite of applications allow administrators to adjust SAS or SATA topology views from the system host, controller and disk enclosure down to the logical and physical drive level. Extending to enterprise deployments, these tools can scale to easily configure, monitor and manage RAID and JBOD volumes locally or over the LAN network.

PowerEdge RAID Controller H740P

- Eight internal ports
- 72-bit DDR4-2133 DRAM interface with 8GB non-volatile cache memory
- Unsurpassed performance and enterprise-class reliability

Dell website as visited on July 23, 2020: https://i.dell.com/sites/doccontent/shared-content/data-sheets/en/Documents/Dell-PowerEdge-RAID-Controller-H740P.pdf.

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Overview

The PowerEdge RAID Controller (PERC) 10 series consist of the H345, H740P, H745, H745P MX, and H840 cards. The PERC 10 family of storage controller cards has the following characteristics:

- Complies with serial-attached SCSI (SAS) 3.0 providing up to 12 Gb/sec throughput.
- Supports Dell-qualified serial-attached SCSI (SAS) hard drives, SATA hard drives, and solid-state drives (SSDs).

  NOTE: Mixing SAS and SATA drives within a virtual disk is not supported. Also, mixing hard drives and SSDs within a virtual disk is not supported.

  NOTE: Mixing disks of different speed (7,200 rpm, 10,000 rpm, or 15,000 rpm) and bandwidth (3 Gbps, 6 Gbps or 12 Gbps) while maintaining the same drive type (SAS or SATA) and technology (HDD or SSD) is supported.
- Offers RAID control capabilities including support for RAID levels 0, 1, 5, 6, 10, 50, and 60.

  NOTE: RAID levels 5, 6, 50 and 60 are not supported on PERC H345.
- Provides reliability, high performance, and fault-tolerant disk subsystem management.

Supported operating systems

See Dell EMC Enterprise operating systems support for a list of supported operating systems by a specific server for the PERC 10 series cards.

NOTE: The PERC 10 driver for VMware ESXi is bundled with the VMware ISO image available from Dell. For more information, see www.dell.com/virtualizationsolutions.

PERC card specifications

The table below lists and describes the different PERC cards that comprise the PERC 10 series and their specifications:

Table 1. PERC cards

Feature	PERC H345	PERC H740P	PERC H745	PERC H745P MX	PERC H840
RAID levels	0, 1, 10	0, 1, 5, 6, 10, 50, 60	0, 1, 5, 6, 10, 50, 60	0, 1, 5, 6, 10, 50, 60	0, 1, 5, 6, 10, 50, 60
Enclosures per port	Not applicable	Not applicable	Not applicable	Not applicable	4
Processor	Dell adapter SAS RAID-on-chip, 8-port with LSI 3516 chipset	Dell adapter SAS RAID-on-chip, 8-port with LSI 3508 chipset	Dell adapter SAS RAID-on-chip, 16-port with LSI 3516 chipset	Dell adapter SAS RAID-on-chip, 16-port with LSI 3516 chipset	Dell adapter SAS RAID-on-chip, 8-port with LSI 3508 chipset
Battery backup unit	No	Yes	Yes	Yes	Yes
eHBA	No	Yes	Yes	Yes	No
LKM security	No	Yes	Yes	Yes	Yes
Enterprise key manager mode	No	Yes	Yes	No	No
Non-volatile cache	No	Yes	Yes	Yes	Yes
Cache memory	N/A	8 GB DDR4 2133 Mhz cache	4 GB DDR4 2133 Mhz cache	8 GB DDR4 2133 Mhz cache	8 GB DDR4 2133 Mhz cache
Cache function	Write through and no read ahead	Write back, write through, no read	Write back, write through, no read	Write back, write through, no read	Write back, write through, no read ahead, and read ahead

8 Overview

Dell website as visited on July 23, 2020: https://topics-cdn.dell.com/pdf/perc10_ug_en-us.pdf, page 8.

PRAYER FOR RELIEF

WHEREFORE, Goodman respectfully requests the Court enter judgment against Defendant:

1. declaring that the Defendant has infringed each of the Patent-in-Suit;

2. awarding Goodman its damages suffered as a result of Defendant's infringement of the Patent-in-Suit;

3. awarding Goodman its costs, attorneys' fees, expenses, and interest;

4. awarding Goodman ongoing post-trial royalties; and

5. granting Goodman such further relief as the Court finds appropriate.

JURY DEMAND

Goodman demands trial by jury, under Fed. R. Civ. P. 38.

Dated: July 30, 2020

Respectfully Submitted

/s/ M. Scott Fuller

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