IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

BELL SEMICONDUCTOR, LLC, Plaintiff, v. TEXAS INSTRUMENTS INCORPORATED, Defendant.	Civil Action No. 2:20-cv-00048 **JURY TRIAL DEMANDED**

BELL SEMICONDUCTOR, LLC'S
FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Bell Semiconductor, LLC ("Bell Semic") as and for its complaint against Texas Instruments Incorporated alleges as follows:

INTRODUCTION

1. Bell Semic is a technology and intellectual property licensing company. Bell Semic's patent portfolio comprises over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world's leading semiconductor technology innovators, including AT&T Bell Laboratories, Lucent Technologies (Lucent), Agere Systems (Agere), LSI Logic and LSI Corporation (LSI). The portfolio reflects expertise developed at the various R&D laboratories and manufacturing locations of these companies around the world. The technology created, developed, and patented at those companies underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors and wireless connectors.

2. Bell Semic was formed in 2017 to manage this portfolio of semiconductor-related intellectual property acquired from Broadcom and assigned to Bell Semic. Several Bell Semic executives previously served as engineers and in leadership roles within the intellectual property departments of Lucent, Agere, LSI, Avago Technologies (Avago), and Broadcom. As a result, Bell Semic executives were personally involved in creating, patenting, and licensing various aspects of the portfolio even before Broadcom assigned it to Bell Semic, including:

- Bell Semic's Chief Executive Officer and Board Member, Mr. John Veschi, served as General Manager of the Intellectual Property business at LSI, had similar responsibilities at Agere, and began his in-house intellectual property experience with the formation of Lucent.
- Bell Semic's President and General Counsel, Mr. Chad Hilyard, served as Managing IP Counsel and in other roles at LSI and Agere, where he was involved in licensing many of the patents in the portfolio now assigned to Bell Semic;
- Bell Semic's Chief Technology Officer, Dr. Sailesh Merchant was a Fellow at Broadcom, Avago, and LSI Corporation; a Distinguished Engineer at LSI Corporation; and a Distinguished Member of the Technical Staff of Agere and Lucent. Dr. Merchant is also a Senior Member of the IEEE and an inventor on more than 250 worldwide patents—including many of the patents in Bell Semic's portfolio—and three of the patents asserted in this Complaint;
- Bell Semic's Senior Director for IP, Mr. Kouros Azimi, served as a Member of the Technical Staff at AT&T Bell Labs, Lucent, and Agere; Director of Intellectual Property at Avago/Broadcom, and a Patent Engineer and Director of Patent Development at LSI/Avago Technologies.

3. Defendant Texas Instruments Incorporated ("TI" or "Defendant") has infringed and continues to infringe Bell Semic's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. TI's customers incorporate those products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States and within this District. Such downstream products include, but are not limited to, power and display drivers for LCD and OLED displays, audio amplifiers and processors, wireless products for the Internet-of-Things, mmWave sensors used in automotive and industrial settings, digital signal processors, high-performance microcontrollers, and Digital Light Projectors (DLP), among others. Examples of infringing TI devices used in such downstream products include TI's DRV2624 haptic motor driver for the Google Pixel 2; TI's TPS65912 power management device used in the cutting-edge Magic Leap 1 headset; and TI's DLP3010AFQK 720p digital-mirror-device in Sunty's SP-001 Digital Light Processor projector.

4. Bell Semic has notified TI of its infringement in writing more than once—but before Bell Semic filed its original Complaint, TI did not respond or acknowledge Bell Semic or its intellectual property. Instead, TI continues to infringe, and thus its infringement is and has been willful under the Patent Act.

NATURE OF THE CASE

5. This action arises under 35 U.S.C. § 271 for TI's infringement of Bell Semic's United States Patent Nos. 8,049,340 ("the Hall 340 Patent"); 8,288,269 ("the Hall 269 Patent"); 7,566,964 ("the Kang Patent"); 6,281,129 ("the Merchant Patent"); 6,879,046 ("the Gibson Patent"); 6,707,132 ("the Banerjee Patent"): 6,544,907 ("the Ma Patent"); 6,492,712 ("the Chen Patent"); 7,319,727 ("the Ramakrishnan Patent"); and 6,441,499 ("the Nagarajan Patent") (collectively, Bell Semic's "Asserted Patents").

PARTIES

6. Bell Semiconductor, LLC is a Delaware limited liability company with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

7. On information and belief, TI is a corporation organized under the laws of Delaware, with a principal place of business at 12500 TI Boulevard, Dallas, TX 75243. TI may be served with process through its registered agent CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, TX 75201.

8. TI is a global semiconductor company that designs, manufactures, and provides to the United States and other markets a wide variety of semiconductors, including a wide array of analog and embedded semiconductor products.

JURISDICTION AND VENUE

9. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

10. This Court has general personal jurisdiction over TI at least because TI is a resident of Texas as defined by Texas law. TI is also subject to this Court's specific and general personal jurisdiction because TI has sufficient minimum contacts within the State of Texas and this District, pursuant to due process and/or the Texas Long Arm Statute. TI is headquartered in the State of Texas, and TI has conducted and continues to regularly conduct business within the State of Texas. TI is registered to do business within the State of Texas and maintains an agent for service of process in Texas. TI has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Texas, and in the Eastern District of Texas by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by

consumers in the United States and in the Eastern District of Texas. TI directly and/or through intermediaries (including distributors, sales agents, and others), ships, distributes, offers for sale, sells, advertises, and/or uses its products (including, but not limited to, the products that are accused of patent infringement in this lawsuit) in the United States, the State of Texas, and the Eastern District of Texas.

11. TI has derived substantial revenues from its infringing acts occurring within the United States, the State of Texas and within this District.

12. Venue is proper as to TI under 28 U.S.C. § 1400(b) because it has committed acts of infringement in this District and has regular and established places of business within this District. *TC Heartland LLC v. Kraft Foods Grp. Brands LLC*, 137 S. Ct. 1514, 1521 (2017). Specifically, TI maintains a 300-millimeter semiconductor production facility at 300 West Renner Road, Richardson, Texas 75080, and a 150-millimeter semiconductor production facility at 6412 US-75, Sherman, Texas 75090.

13. TI has not disputed this District's personal jurisdiction over it in other recent patent infringement actions, nor has TI disputed that venue is proper as to it in the Eastern District of Texas. *See, e.g.*, Answer [ECF 14] at ¶¶ 8 & 13, *Phenix Longhorn, LLC v. Texas Instruments, Inc.*, No. 2:18-cv-00020-RWS (E.D. Tex. Jan. 22, 2018); Answer [ECF 23] at ¶¶ 6 & 7, *Complex Memory, LLC v. Texas Instruments, Inc. et al.*, No. 2:17-cv-00699-JRG (E.D. Tex. Oct. 13, 2017).

14. TI has committed acts of infringement in this District giving rise to this action and does business in this District, including making sales and/or providing service and support for its respective customers in this District. TI purposefully and voluntarily sold one or more of the infringing products with the expectation that they would be purchased by consumers in this

District. These infringing products have been and continue to be purchased by consumers in this District. TI has committed acts of patent infringement within the United States, the State of Texas, and the Eastern District of Texas.

BELL SEMIC'S ASSERTED PATENTS

A. U.S. Patent No. 8,049,340 (Hall 340 Patent)

15. Bell Semic is the owner by assignment of U.S. Patent No. 8,049,340 ("the Hall 340 Patent"), owns all right, title, and interest in the Hall 340 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 340 Patent is entitled "Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package." A true and correct copy of the Hall 340 Patent is attached as **Exhibit A**.

16. The inventors of the Hall 340 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

17. The application for the Hall 340 Patent was filed on March 22, 2006, and it duly and properly issued as a patent on November 1, 2011.

B. U.S. Patent No. 8,288,269 (Hall 269 Patent)

18. Bell Semic is the owner by assignment of U.S. Patent No. 8,288,269 ("the Hall 269 Patent"), owns all right, title, and interest in the Hall 269 Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Hall 269 Patent is entitled "Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package." The Hall 269 Patent issued on October 16, 2012. A true and correct copy of the Hall 269 Patent is attached as **Exhibit B**.

19. The inventors of the Hall 269 Patent are Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins.

20. The application for the Hall 269 Patent was filed on October 4, 2011, and claims priority to the application leading to the Hall 340 Patent, which was filed on March 22, 2006. The Hall 269 Patent issued as a patent on October 16, 2012.

C. U.S. Patent No. 7,566,964 (Kang Patent)

21. Bell Semic is the owner by assignment of U.S. Patent No. 7,566,964 ("the Kang Patent"), owns all right, title, and interest in the Kang Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Kang Patent is entitled "Aluminum Pad Power Bus and Signal Routing for Integrated Circuit Devices Utilizing Copper Technology Interconnect Structures." A true and correct copy of the Kang Patent is attached as **Exhibit C**.

22. The inventors of the Kang Patent are Seung H. Kang, Roland P. Krebs, Kurt George Steiner, Michael C. Ayukawa, and Dr. Merchant.

23. The application for the Kang Patent was filed on September 30, 2003, and it claims priority to Provisional Application No. 60/462,504, filed on April 10, 2003. The Kang Patent issued as a patent on July 28, 2009.

24. As of February 2020, the Kang Patent's disclosure has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 14 patents and published applications filed by leading technology companies such as Texas Instruments, IBM, Apple, GlobalFoundries, and Taiwan Semiconductor Manufacturing Co.

D. U.S. Patent No. 6,281,129 (Merchant Patent)

25. Bell Semic is the owner by assignment of U.S. Patent No. 6,281,129 (the "Merchant Patent"), owns all right, title, and interest in the Merchant Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Merchant

Patent is entitled "Corrosion-Resistant Polishing Pad Conditioner." A true and correct copy of the Merchant Patent is attached as **Exhibit D.**

26. The inventors of the Merchant Patent are Dr. Merchant, William G. Easter, and John A. Maze.

27. The application for the Merchant Patent was filed on September 20, 1999, and it issued as a patent on August 28, 2001.

28. As of February 2020, the Merchant Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 22 patents and published applications.

E. U.S. Patent No. 6,879,046 (Gibson Patent)

29. Bell Semic is the owner by assignment of U.S. Patent No. 6,879,046 (the "Gibson Patent"), owns all right, title, and interest in the Gibson Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Gibson Patent is entitled "Split Barrier Layer Including Nitrogen-Containing Portion and Oxygen-Containing Portion." A true and correct copy of the Gibson Patent is attached as **Exhibit E**.

30. The inventors of the Gibson patent are Gerald W. Gibson, Jr., Scott Jessen, Steven Alan Lytle, Kurt George Steiner, and Susan Clay Vitkavage.

31. The application for the Gibson Patent was filed on January 2, 2002, and it claims priority to Provisional Application No. 60/301,295, filed on June 28, 2001. The Gibson Patent issued on April 12, 2005.

32. As of February 2020, the Gibson Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 54 patents and published applications—including during the prosecution of patent applications filed by leading technology

companies such as Texas Instruments, Taiwan Semiconductor Manufacturing Co., Micron Technology, Intel, and Panasonic Corp.

F. U.S. Patent No. 6,707,132 (Banerjee Patent)

33. Bell Semic is the owner by assignment of U.S. Patent No. 6,707,132 (the "Banerjee Patent"), owns all right, title, and interest in the Banerjee Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Banerjee Patent is entitled "High Performance Si-Ge Device Module with CMOS Technology." A true and correct copy of the Banerjee Patent is attached as **Exhibit F**.

34. The inventors of the Banerjee patent are Robi Banerjee, Derryl J. Allman, and David T. Price.

35. The application for the Banerjee Patent was filed on November 5, 2002, and it issued as a patent on March 16, 2004.

36. As of February 2020, the Banerjee Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 7 patents and published applications filed by leading technology companies such as Texas Instruments, Taiwan Semiconductor Manufacturing Co., IBM, and National Semiconductor Corp.

G. U.S. Patent No. 6,544,907 (Ma Patent)

37. Bell Semic is the owner by assignment of U.S. Patent No. 6,544,907 (the "Ma Patent"), owns all right, title, and interest in the Ma Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Ma Patent is entitled "Method of Forming a High Quality Gate Oxide Layer Having a Uniform Thickness." A true and correct copy of the Ma Patent is attached as **Exhibit G**.

38. The inventors of the Ma patent are Yi Ma and Edith Yang.

39. The application for the Ma Patent was filed on October 12, 2000, and it issued as a patent on April 8, 2003.

H. U.S. Patent No. 6,492,712 (Chen Patent)

40. Bell Semic is the owner by assignment of U.S. Patent No. 6,492,712 (the "Chen Patent"), owns all right, title, and interest in the Chen Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Chen Patent is entitled "High Quality Oxide for Use in Integrated Circuits." A true and correct copy of the Chen Patent is attached as **Exhibit H**.

41. The inventors of the Chen patent are Yuanning Chen, Sundar Srinivasan Chetlur, Dr. Merchant, and Pradip Kumar Roy.

42. The application for the Chen Patent was filed on June 20, 2000, and it claims priority to Provisional Application No. 60/140,909, filed on June 24, 1999. The Chen Patent issued on December 10, 2002.

43. As of February 2020, the Chen Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 7 patents and published applications filed by leading technology companies such as Toshiba, Fujitsu, and Sanyo Electric.

I. U.S. Patent No. 7,319,272 (Ramakrishnan Patent)

44. Bell Semic is the owner by assignment of U.S. Patent No. 7,319,272 (the "Ramakrishnan Patent"), owns all right, title, and interest in the Ramakrishnan Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Ramakrishnan Patent is entitled "Ball Assignment System." A true and correct copy of the Ramakrishnan Patent is attached as **Exhibit I**.

45. The inventors of the Ramakrishnan patent are Arun Ramakrishnan, Farshad Ghahghahi, Aritharan Thurairajaratnam, and Leah M. Miller.

46. The application for the Ramakrishnan Patent was filed on October 5, 2006, and it issued as a patent on January 15, 2008.

J. U.S. Patent No. 6,441,499 (Nagarajan Patent)

47. Bell Semic is the owner by assignment of U.S. Patent No. 6,441,499 (the "Nagarajan Patent"), owns all right, title, and interest in the Nagarajan Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Nagarajan Patent is entitled "Thin Form Factor Flip Chip Ball Grid Array." A true and correct copy of the Nagarajan Patent is attached as **Exhibit J**.

48. The inventors of the Nagarajan patent are Kumar Nagarajan and Sarathy Rajagopalan.

49. The application for the Nagarajan Patent was filed on August 30, 2000, and it issued as a patent on December 10, 2002.

50. As of July 2020, the Nagarajan Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 17 patents and published applications filed by leading technology companies, such as Fujitsu, Macronix, and NXP. The Nagarajan Patent was also cited by USPTO examiner George Eckert during prosecution of Defendant TI's patent application that published as U.S. 2005/0127484.

FACTUAL BACKGROUND

51. Bell Semic incorporates the preceding paragraphs as if fully set forth herein.

52. On June 1, 2002, Lucent, having its roots with Bell Laboratories and AT&T Corporation, spun off its microelectronics business as Agere. Agere later merged with LSI Logic forming LSI Corporation in 2007, which was in turn acquired by Avago in 2014. In 2016, Avago purchased Broadcom and assumed its name to become the current Broadcom Inc. In 2017, Broadcom assigned a patent portfolio containing over 1,900 worldwide patents and applications,

approximately 1,500 of which are active U.S. patents, to Bell Semic that included patents originally assigned or issued to Bell Labs, Lucent, Agere, LSI Logic, and LSI.

53. Portions of the Bell Semic portfolio are presently licensed and/or were previously licensed to leading technology companies by Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*See supra ¶* 2.) Portions of the Bell Semic portfolio were also invented and co-invented by other Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*Id.*)

54. Bell Semic's Asserted Patents arise out of the research, conception, creation, and design of innovative technology developed by leading high-technology companies, including LSI Logic, Agere, and LSI Corporation. Prior to their ultimate acquisition by Avago (now Broadcom), those companies were pioneers of innovative semiconductor technology—and made substantial investments into researching, inventing, creating, and manufacturing cutting-edge semiconductor technology. Bell Semic's Asserted Patents are directed to this inventive technology relating to semiconductors, integrated circuits and related products.

55. TI infringes and has infringed by making, selling, offering to sell, using, and/or importing products (including importing products made by a patented process) throughout the United States. Moreover, TI works closely with its customers, foundry suppliers, distributors, OEMs, or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and related products. TI tailors its manufacturing process for its customers and designs its products to be integrated into downstream products. In addition to its own manufacturing, TI's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States by itself and others further include, without limitation, any one or a combination of: (i) designing specifications for

manufacture of TI's products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of TI's products; (iii) soliciting and/or sourcing the manufacture of TI's products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of their products; (v) enabling and encouraging the use, sale, or importation of their products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

56. TI provides marketing and/or technical support services for its products from its facilities in the United States. For example, TI maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for their products. (*See, e.g.*, http://www.ti.com/.) TI's publicly-available website also contains user manuals, product documentation, and other materials related to its products. (*Id.*) For example, TI's website contains over 4,000 reference designs (http://www.ti.com/reference-designs/index.html), spanning automotive, communication equipment, enterprise systems, industrial, and personal electronics markets; complimentary design review services such as selection tools, calculators, simulation tools, and model libraries that aid the entire design process (http://www.ti.com/design-resources/design-tools-simulation.html); hardware, software, and development tools to accelerate its customer's time to market (http://www.ti.com/design-resources/embedded-development.html); and robust customer support through TI's E2E support forums, which is an "engineer's go-to source for help throughout every step of the design process" (https://e2e.ti.com/).

57. In addition to these resources, TI also provides numerous support resources for the customers of its semiconductor devices in addition to user manuals and datasheets, including live training and video tutorials to help customers "design and develop with TI products, tools,

software[,] and applications" (https://training.ti.com/). This training includes: "TI Precisions Labs," which is video curriculum spanning analog signal chain products events (https://training.ti.com/ti-precision-labs-overview); "Tech Days," which are free, technical seminars and interactive demonstrations showcasing TI products (https://training.ti.com/tech-days); power supply design seminars (http://www.ti.com/ww/en/power-training/login.shtml?DCMP=pwr-psds-archive&HQS=pwr-psds-archive-psds), and access to design journals (http://www.ti.com/analog-circuit/analog-design-journal.html), technical documents (http://www.ti.com/technical-documents/techdoc?siloId=1), and articles (https://e2e.ti.com/blogs_/), covering TI technology and products. Moreover, TI supports a "Third-Party Network," which is "a worldwide community of respected, well-established companies offering products and services that complement" TI's semiconductor device solutions, including a broad range of reference designs, turnkey products and services, system modules, embedded software, engineering services, and development tools that help its customers accelerate development efforts and reduce time-to-market (http://www.ti.com/design-resources/third-party-network.html).

TI'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT FROM BELL SEMIC

58. Before filing this lawsuit, Bell Semic notified TI that Broadcom has assigned to Bell Semic a large portfolio of semiconductor patents, identified TI Technology Nodes that infringe Bell Semic's Asserted Patents, further identified exemplary products from those Technology Nodes that infringe the Asserted Patents, and offered to license those patents to TI.

59. Specifically, on March 25, 2019, Mr. Hilyard, sent a letter to TI's headquarters addressed to Mr. Larry J. Bassuk (TI's Deputy General Patent Counsel) to inform TI that Bell Semic "acquired the semiconductor-related patent assets previously owned by Agere Systems

Inc. and LSI Corporation. This portfolio comprises patents originating from Bell Labs, Lucent Technologies, as well as patents originally assigned to Agere, LSI and Avago Corporation. The portfolio reflects expertise and inventions developed at various R&D labs and manufacturing facilities associated with these companies around the world . . . The patent portfolio comprises over 1,900 worldwide patents and applications, approximately 1,500 of which are in force in the United States Patents. By way of background, I was previously part of the Lucent/Agere/LSI licensing team and am joined by other former members of that licensing team. Accordingly, we are very familiar with this pioneering patent portfolio and have licensed this portfolio to many of the world's leading semiconductor companies. We have been acquiring products and conducting reverse engineering to establish manufacturers' use of exemplary patents in the portfolio. Our preliminary analysis reveals that TI is currently making, using, selling, or offering for sale products that infringe one or more of Bell Semic's patents."

60. Bell Semic's March 25, 2019 letter to TI also invited TI to engage in a dialogue and offered to answer any TI questions, and offered to meet on a date, time, and location of TI's choosing—all in an effort to attempt to reach a license agreement: "We would like to have a near-term dialogue with TI, with the goal of answering any questions you may have about the portfolio, providing more details about the portfolio's contents as well as providing specific claim charts demonstrating how your products read on exemplary patents. The goal of course is to come to an amicable, mutually beneficial licensing agreement between us for the portfolio. To that end, please propose some dates and times when your team is available for a meeting. We are happy to meet with you at a location of your choice. If you would like to chat telephonically regarding logistics, or about any other matter, please feel free to call me directly at the number

listed above. I look forward to your reply and thank you in advance for your prompt attention to these matters."

61. TI did not respond to Bell Semic's March 25, 2019 Notice Letter.

62. On August 30, 2019, Bell Semic's Mr. Hilyard again wrote to TI's Deputy General Patent Counsel, and copied TI's Senior Vice President, Secretary, and General Counsel, Ms. Cynthia Hoff Trochu, to follow-up on Bell Semic's March 25, 2019 letter, and invited TI to enter into a license agreement: "I am writing to follow up on my letter of March 25, 2019. As we noted previously, Bell Semiconductor, LLC ("Bell Semic") acquired the semiconductor-related patent assets previously owned by Agere Systems Inc. and LSI Corporation as well as patents originally assigned to Avago Corporation. We would like to engage with you to discuss a license agreement to this portfolio that will continue for a period of between five and ten years."

63. Bell Semic's August 30, 2019 letter also identified specific Bell Semic patents that TI infringes—and identified the TI Technology Nodes that infringe those patents, and exemplary infringing products from TI's infringing Technology Nodes: "Over the last several months, we have been acquiring products manufactured by Texas Instruments and conducting reverse engineering to establish Texas Instruments' use of Bell Semiconductor's patented technology. Our recent analysis of Texas Instruments products evidences that Texas Instruments is currently making, using, selling, or offering for sale products that infringe one or more of Bell Semic's patents. The table in the attached Exhibit A below shows products Bell Semic has recently reverse engineered, and exemplary patents those products and processing nodes infringe."

64. Exhibit A to Bell Semic's August 30, 2019 letter put TI on notice of TI's infringing Technology Nodes and exemplary infringing products from those Nodes, including the Merchant, Nagarajan, Hall 340, and Hall 269 Asserted Patents as follows:

Exemplary List of Bell Semic's Patents Infringed by Texas Instruments

Texas Instruments Device Type	Texas Instruments Product Code	Texas Instruments Technology Node	US 6,281,129 Easter	US 6,406,999 Esry	US 6,596,639 Easter	US 6,743,669 Lin	US 7,068,139 Harris	US 6,441,499 Nagarajan	US 8,049,340 Hall	US 8,288,269 Hall
Battery Management	BQ24725	220 nm	X		X	X				
AMOLED Display Power Supply	TPS65632	220 nm	X	X	X	X				
LED Matrix Manager Automotive	TPS92661	500 nm	X		X					
Audio Amplifier	TPA3110D2	250 nm	X		X	X				
HDMI	TPD12S015A	180 - 200 nm	X	X	X	X				
Haptic Driver	DRV2624	150 - 160 nm	X		X	X				
PMU for Processor	TPS65912	180 - 200 nm	X		X					
A/D Converter	ADS1261	220 nm	X		X					
Touch Screen Controller	TSC2004	250 nm	X		X	X				
WiFi-RF WiLink Module	WL1807MOD	50 nm	X				X			
Processor-MCU	RM48L952	65 nm	X							
Radar Sensor Transceiver	AWR1642	40 nm	X							
MCU	TM4C123GH6PGEI	65 nm	X							
DSP Dig Media Processor	TMS320DM6467	90 nm	X							
720p DMD	DLP3010AFQK	160 nm	X	X	X					
Quad-channel Transceiver	TLK10034AAJ	65 nm	X						X	X
DSP + ARM SOC	66AK2G12ABYA60E							X		
DM Processor	DM3725CUS	45 nm	X							

65. Bell Semic's August 30, 3019 letter reminded TI of its responsibilities under the Patent Act, attached a draft NDA to facilitate open and honest discussions, and once again offered to meet with TI on a date, time, and location of TI's choosing: "As I am sure you are aware, Texas Instruments has an affirmative responsibility to ensure that it has secured all necessary patent rights to manufacture and sell the products listed below, as well as others that might be infringing Bell Semic's intellectual property. . . We would like to propose having a near-term dialogue with Texas Instruments with the goal of providing more details about our licensing program and the patent portfolio (including providing specific claim charts), answering any questions you may have, and reaching an agreement on a path forward to put in place a new license agreement covering this semiconductor patent portfolio. To that end, please propose

some dates and times when your team is available for a meeting. We are happy to meet with you at a location of your choice."

66. TI did not respond to Bell Semic's August 30, 2019 Notice Letter.

67. On January 10, 2020, Mr. Veschi wrote to TI's Deputy General Patent Counsel to follow up on Mr. Hilyard's August 30, 2019 letter and provided an update on Bell Semic's reverse engineering of TI products: "It has been 4 months since our letter to you dated August 30, 2019 from Mr. Hilyard. During this time we have not received a response and have proceeded in our reverse engineering efforts regarding products made by Texas Instruments. We have confirmed to date infringement of five (5) additional patents by eight (8) products across three (3) process technology nodes. A summary of the previously noticed infringement along with recently discovered infringing products is provided in the table below."

68. Bell Semic's January 10, 2020 letter once again invited TI to license the identified patents and further put TI on notice of infringement by TI's Technology Nodes and exemplary products from those Nodes, including the Merchant, Kang, Hall 340, Hall 269, Gibson, Ma, Chen, and Nagarajan Asserted Patents as follows:

Texas Instruments Device Type	Texas Instruments Product Code	Texas Instruments Technology Node	US 6,281,129 Easter	US6544907 Ma	US 6,406,999 Esry	US6492712 Chen	US 6,596,639 Easter	US6683382 Cwynar	US 6,743,669 Lin	US6879046 Gibson	US 7,068,139 Harris	US 6,441,499 Nagarajan	US7566964 Kang	US 8,049,340 Hall	US 8,288,269 Hall
Battery Management	BQ24725	220 nm	X				X		X						
AMOLED Display Power Supply	TPS65632	220 nm	X		X		X		X						
LED Matrix Manager Automotive	TPS92661	500 nm	X				X								
Audio Amplifier	TPA3110D2	250 nm	X				X		X						
HDMI	TPD12S015A	180 - 200 nm	X		X		X		X						
Haptic Driver	DRV2624	150 - 160 nm	X				X		X						
PMU for Processor	TPS65912	180 - 200 nm	X				X								
A/D Converter	ADS1261	220 nm	X				X								
Touch Screen Controller	TSC2004	250 nm	X				X		X						
WiFi-RF WiLink Module	WL1807MOD	50 nm	X	X		X				X	X				
Processor-MCU	RM48L952	65 nm	X	X		X		X							
Radar Sensor Transceiver	AWR1642	40 nm	X	X		X									
MCU	TM4C123GH6PGEI	65 nm	X	X		X		X					X		
DSP Dig Media Processor	TMS320DM6467	90 nm	X												
720p DMD	DLP3010AFQK	160 nm	X		X		X								
Quad-channel Transceiver	TLK10034AAJ	65 nm	X	X		X								X	X
DSP + ARM SOC	66AK2G12ABYA60E											X			
DM Processor	DM3725CUS	45 nm	X	X		X									
RF Systen on a Chip - SOC	AWR1443FQIGABLQ1	45 nm RF CMOS	X	X		X									
RF Systen on a Chip - SOC	IWR1642AQAGABLR	45 nm RF CMOS	X	X		X									

X	August 2019 Notice Letter
X	January 2020 Notice Letter

69. Bell Semic's January 10, 2020 Notice Letter again offered to meet with TI on a date, time, and location of TI's choosing: "Please let me know when you are available for a near-term meeting to discuss licensing options for the patents and products identified below as well as the broader Bell Semiconductor portfolio."

70. TI did not respond to Bell Semic's January 10, 2020 Notice Letter before Bell Semic filed its original Complain in this action.

71. TI knowingly and willfully infringes, and continues to knowingly and willfully infringe, Bell Semic's Asserted Patents directly, contributorily, and by inducement—to obtain the substantial benefits of those inventions without a license from Bell Semic. Thus, Bell Semic has been left with no other choice but to seek relief from this Court.

COUNT 1

Willful Infringement of U.S. Patent No. 8,049,340 (Hall 340 Patent)

72. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

73. The Hall 340 Patent is generally related to an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board. (*See* Hall 340 Patent, Abstract.)

74. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the TI TLK10034AAJ described below includes 324 pins) while packages decrease in size. In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 340 Patent teaches the use of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

75. The Hall 340 Patent contains 3 independent claims and 19 total claims, covering various integrated circuit package substrates. Claim 12 reads:

> An integrated circuit package substrate, comprising:
>
> a first layer comprising a plurality of rows of electrical contacts;
>
> a plurality of electrically conductive layers disposed immediately proximate the first layer;

a plurality of dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other, and

a plurality of rows of cutouts formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers.

76. TI has directly infringed, and continues to directly infringe, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Hall 340 Patent (*e.g.*, claims 12-13),[1] including, but not limited to:

- TI products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts;
- TI's TLK10034AAJ quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems;
- TI's 66AK2E05XABD25 multicore DSP+ARM System-on-Chip (SoC) for developers of a range of applications including enterprise grade networking end equipment, data center networking, avionics and defense, medical imaging, test and automation;
- TI's 66AK2H05DAAW2 multicore DSP+ARM SoC for applications that include cloud computing, media processing, transcoding, security, and gaming;

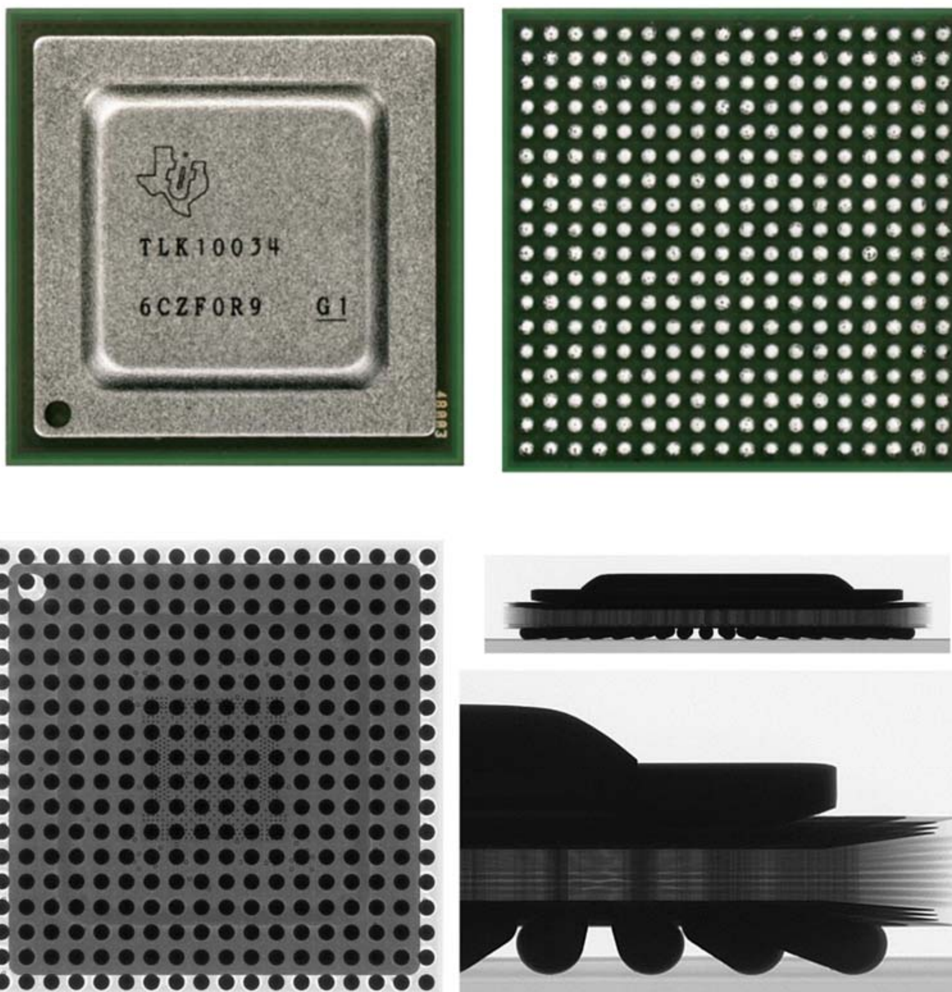
[1] Throughout this Complaint, wherever Bell Semic identifies specific claims of the Asserted Patents that TI infringes, Bell Semic expressly reserves the right to identify additional asserted claims and products in its infringement contentions in accordance with the local patent rules. Specifically identified claims throughout this Complaint are provided for notice pleading only and are not presented as "exemplary" claims of all other claims for any Asserted Patent.

- TI's DS280DF810ABVT eight-channel multi-rate retimer with integrated signal conditioning used to extend the reach and robustness of long, lossy, cross-talk impaired high-speed serial links with a low bit error rate;
- TI's DS125DF1610FB/NOPB sixteen-channel multi-rate retimer with integrated signal conditioning that enables longer distance transmission in lossy copper interconnects and backplanes with multiple connectors; and
- TI's devices that are variants of the above-identified products;

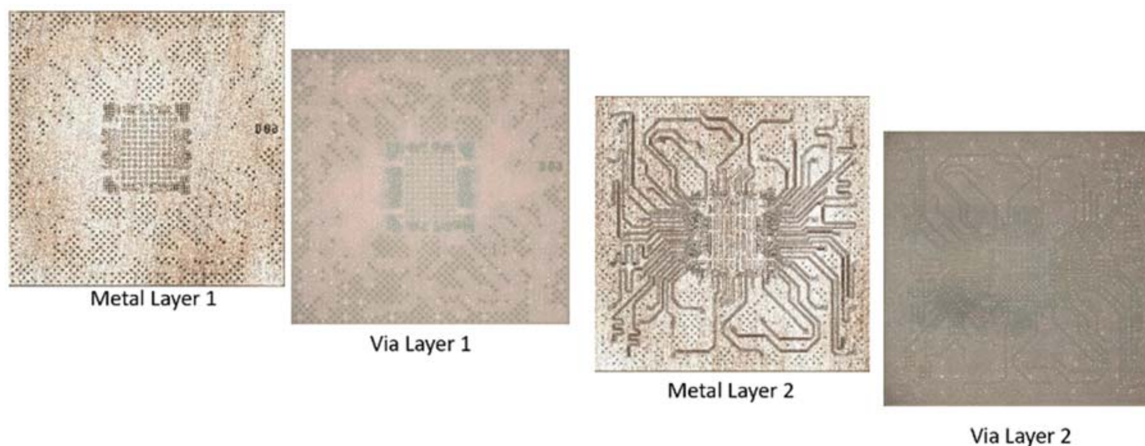
(collectively, the "Hall 340 Accused Products").

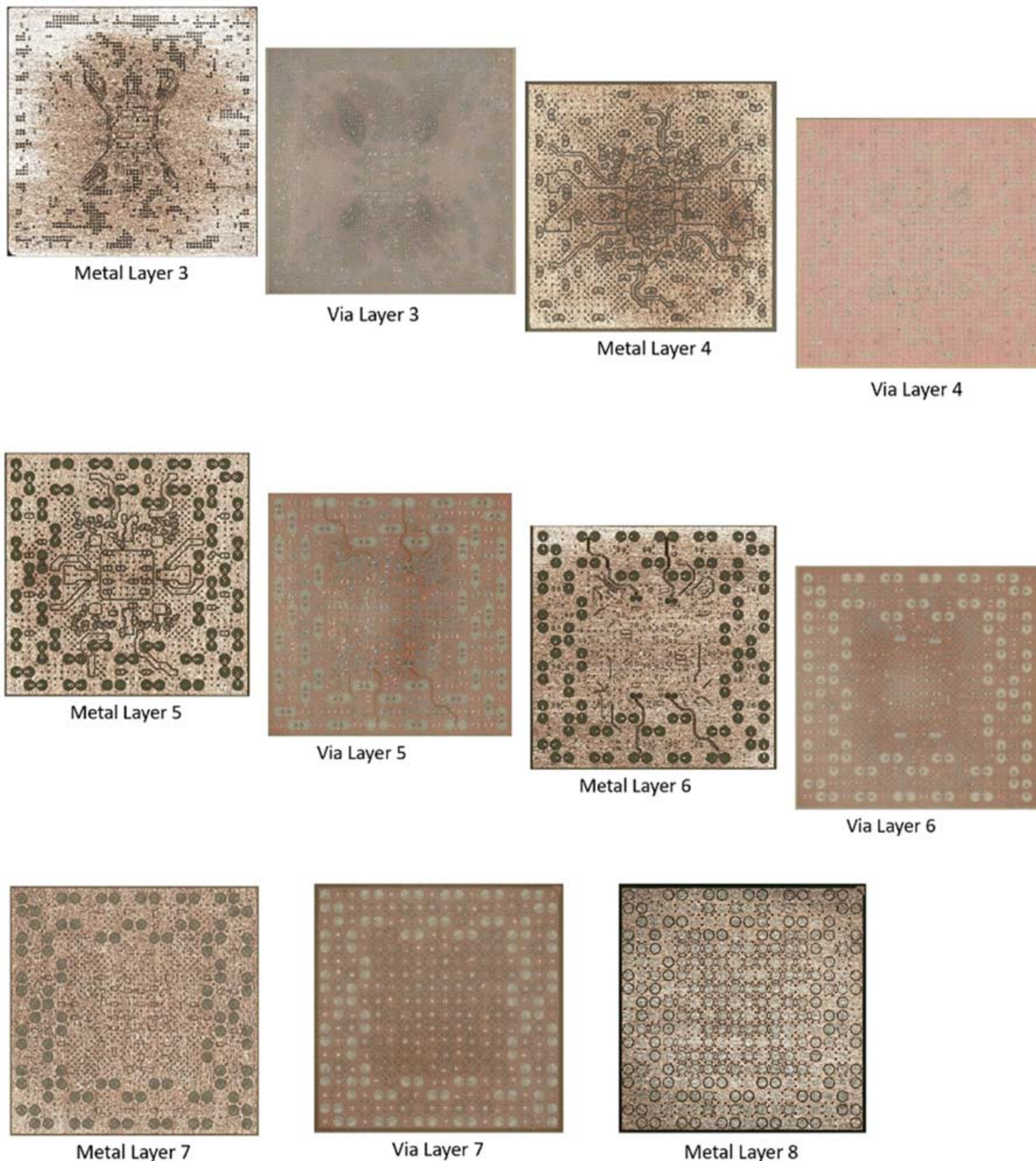
77. By way of non-limiting example only, TI's TLK10034AAJ infringes claim 12 of the Hall 340 Patent because it is an integrated circuit that has an integrated circuit package substrate with (1) a first layer that has two or more rows of electrical contacts; (2) two or more electrically conductive layers disposed immediately proximate the first layer; (3) two or more dielectric layers separating, respectively, the electrically conductive layers and the first layer from each other; and (4) two or more rows of cutouts formed in each of the two or more electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the two or more electrically conductive layers.

78. As shown below, TI's TLK10034AAJ is an integrated circuit with an integrated circuit package substrate.

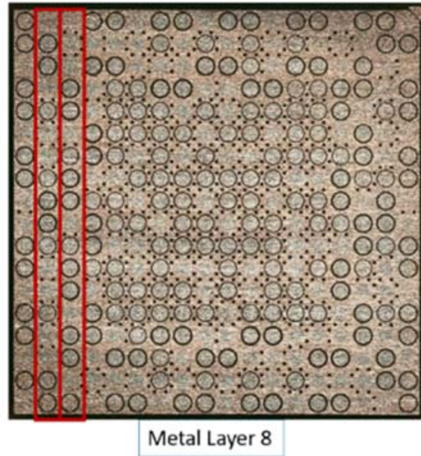


79. The integrated circuit package substrate of the TI TLK10034AAJ has 8 metal layers and 7 via layers.

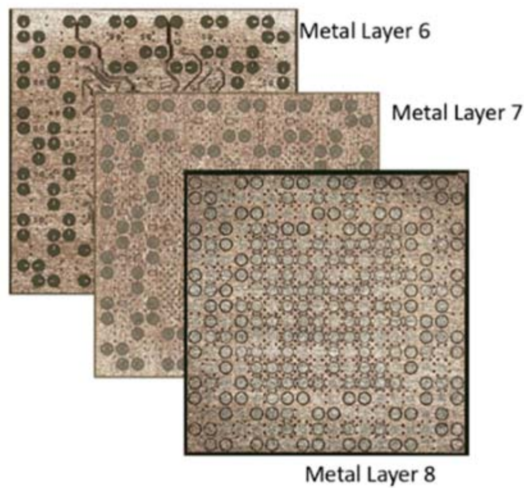




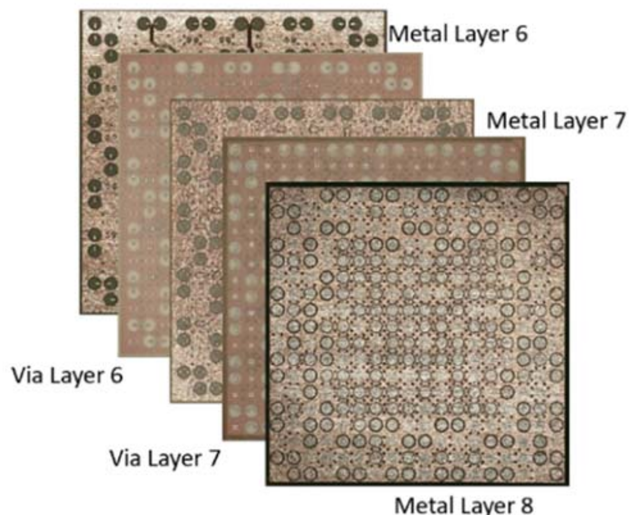
80. The first layer (metal layer 8) of the TI TLK10034AAJ has a plurality of rows of electrical contacts and forms the ball grid array layer with solder balls, removed for clarity (for example, as indicated in red below).



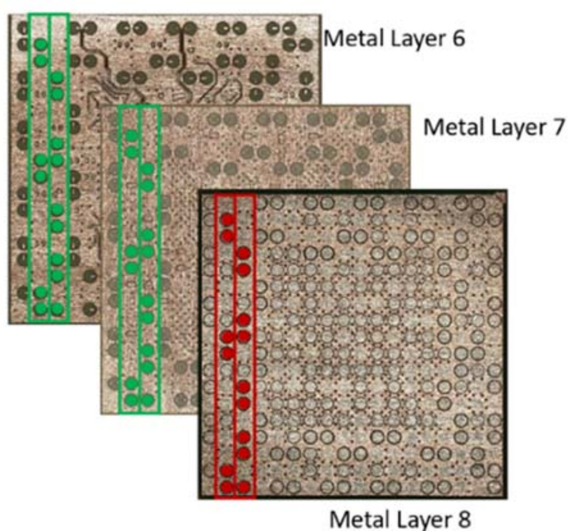
81. The TI TLK10034AAJ also has a plurality of electrically conductive layers (for example, metal layers 6 and 7) disposed immediately proximate the first layer (metal layer 8).



82. The TI TLK10034AAJ further has a plurality of dielectric layers (for example, via layers 6 and 7) separating, respectively, the electrically conductive layers (metal layers 6 and 7) and the first layer (metal 8) from each other.



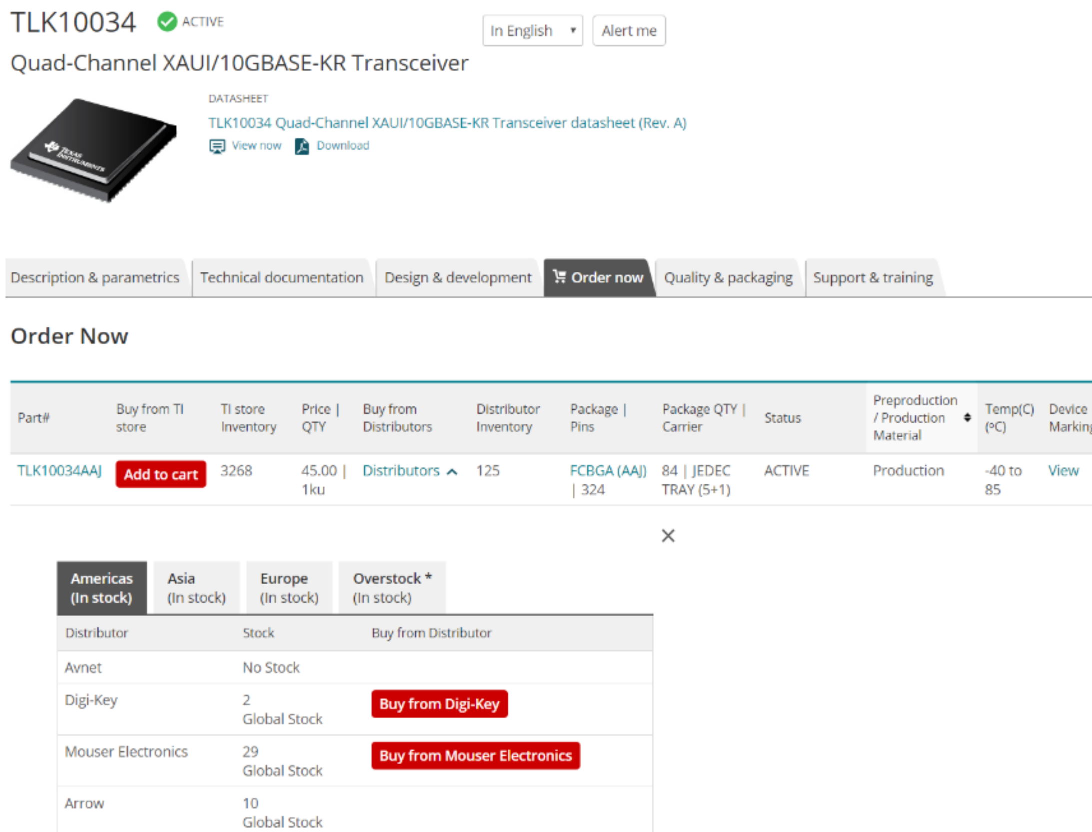
83. The TI TLK10034AAJ further has a plurality of rows of cutouts (for example, in green below) formed in each of the plurality of the electrically conductive layers, each of the cutouts overlapping a corresponding one of the electrical contacts (for example, in red below) for reducing parasitic capacitance between the electrically conductive layers and the first layer such that there is substantially no overlap of the rows of electrical contacts with metal in the plurality of electrically conductive layers:



84. Claim 12 of the Hall 340 Patent applies to each Hall 340 Accused Product at least because each of those products contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts as the TI TLK10034AAJ.

85. On information and belief, each of the Hall 340 Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

86. By way of example only, the TLK10034AAJ has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



See http://www.ti.com/product/TLK10034/samplebuy (last visited February 6, 2020).

87. TI has known of the Hall 340 Patent and has been on notice of its infringement of Hall 340 Patent since at least August 30, 2019, when Bell Semic first identified the TLK10034AAJ as infringing and exemplary of TI's infringement of the Hall 340 Patent. After TI did not respond to that letter, Bell Semic sent another letter to TI on January 10, 2020, again identifying the TLK10034AAJ as infringing and exemplary of TI's infringement. TI also did not respond to that letter.

88. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 340 Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

89. TI, knowing its products infringe the Hall 340 Patent and with specific intent for others to infringe the Hall 340 Patent, has induced infringement of, and continue to induce infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Hall 340 Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Hall 340 Accused Products in the United States. TI knows, and has known since at least August 30, 2019, that the Hall 340 Accused Products

infringe the Hall 340 Patent, and purposefully and knowingly sells and offers to sell the Hall 340 Accused Products to its customers with the knowledge and expectation that the Hall 340 Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

90. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 340 Accused Products and/or products incorporating the Hall 340 Accused Products in the United States by marketing the Hall 340 Accused Products in the United States; providing information such as detailed datasheets supporting use of the Hall 340 Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Hall 340 Accused Products; providing technical documentation for the Hall 340 Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Hall 340 Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Hall 340 Accused Products, including live training and video.

91. TI has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Hall 340 Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Hall 340 Accused Products, which constitute a material

part of the invention of the Hall 340 Patent, knowing the Hall 340 Accused Products to be especially made or especially adapted for use in infringement of the Hall 340 Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

92. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

93. TI's infringement of the Hall 340 Patent is and has been knowing, deliberate, and willful. TI learned of its infringement of the Hall 340 Patent no later than August 30, 2019. As detailed above, Bell Semic sent letters to TI on August 30, 2019 and January 10, 2020 identifying the Hall 340 Patent as being infringed by TI's exemplary TLK10034AAJ product. TI did not respond to either of these letters. Despite these efforts, and knowing that it was willfully infringing the Hall 340 Patent, TI continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Hall 340 Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Hall 340 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 2

Willful Infringement of U.S. Patent No. 8,288,269 (Hall 269 Patent)

94. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

95. The Hall 269 Patent is generally related to methods for avoiding parasitic capacitance in an integrated circuit package, such as an integrated circuit package substrate that has a first and an additional electrically conductive layer separated from each other by an electrically insulating layer, a contact pad formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board, and a cutout formed in the additional electrically conductive layer that encloses an area that completely surrounds the contact pad for avoiding parasitic capacitance between the additional electrically conductive layer and the printed circuit board. (*See* Hall 269 Patent, Abstract.)

96. Parasitic capacitance results when parts in an electronic circuit are in close proximity to each other, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections (for example, the TI TLK10034AAJ described below includes 324 pins) while packages decrease in size. In order to reduce parasitic capacitance in the multi-layer packages for these integrated circuits, the Hall 269 Patent teaches the formation of cutouts over the electrical contacts in electrically conductive layers so that there would be substantially no overlap between the electrical contacts and metal in the electrically conductive layers.

97. The Hall 269 Patent contains 2 independent claims and 20 total claims, covering various methods. Claim 1 reads:

> A method, comprising steps of:
>
> forming a first electrically conductive layer including a plurality of rows of contact pads;
>
> forming an electrically insulating layer on the first electrically conductive layer; and

> forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

98. TI has directly infringed, and continues to directly infringe, one or more claims of the Hall 269 Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Hall 269 Patent, and/or TI has directly infringed, and continues to directly infringe, one or more claims of the Hall 269 Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Hall 269 Patent (*e.g.*, claims 1, 4, 7, and 10-13). Such products manufactured using these infringing methods include, but are not limited to:

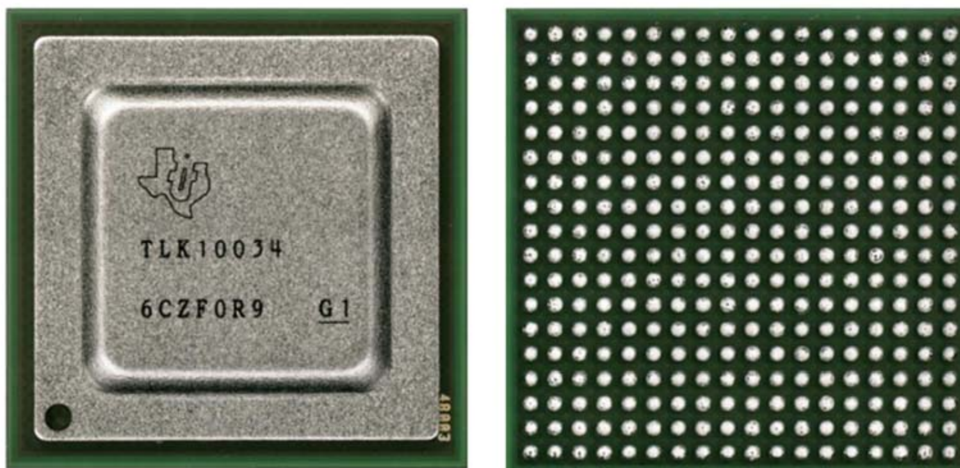
- TI products with at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts;
- TI's TLK10034AAJ quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems;
- TI's 66AK2E05XABD25 multicore DSP+ARM System-on-Chip (SoC) for developers of a range of applications including enterprise grade networking end equipment, data center networking, avionics and defense, medical imaging, test and automation;
- TI's 66AK2H05DAAW2 multicore DSP+ARM SoC for applications that include cloud computing, media processing, transcoding, security, and gaming;

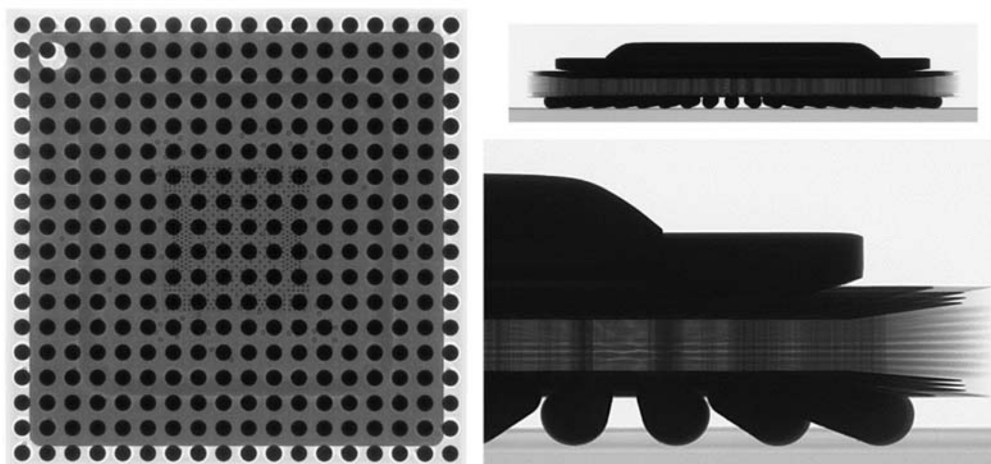
- TI's DS280DF810ABVT eight-channel multi-rate retimer with integrated signal conditioning used to extend the reach and robustness of long, lossy, cross-talk impaired high-speed serial links with a low bit error rate;
- TI's DS125DF1610FB/NOPB sixteen-channel multi-rate retimer with integrated signal conditioning that enables longer distance transmission in lossy copper interconnects and backplanes with multiple connectors; and
- TI's devices that are variants of the above-identified products;

(collectively "Hall 269 Accused Products").

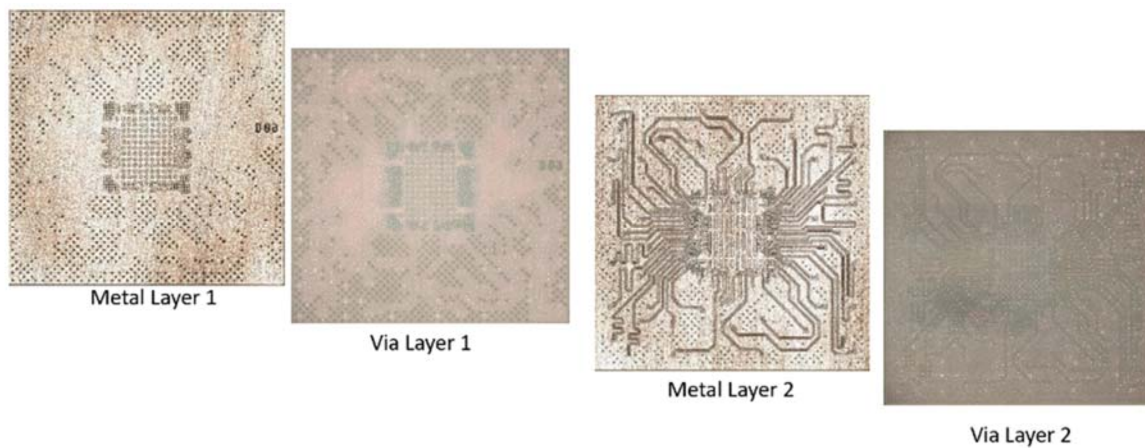
99. By way of example only, the process of manufacturing the TI TLK10034AAJ meets all the steps of claim 1 of the Hall 269 Patent including: (1) forming a first electrically conductive layer including a plurality of rows of contact pads; (2) forming an electrically insulating layer on the first electrically conductive layer; and (3) forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layers and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

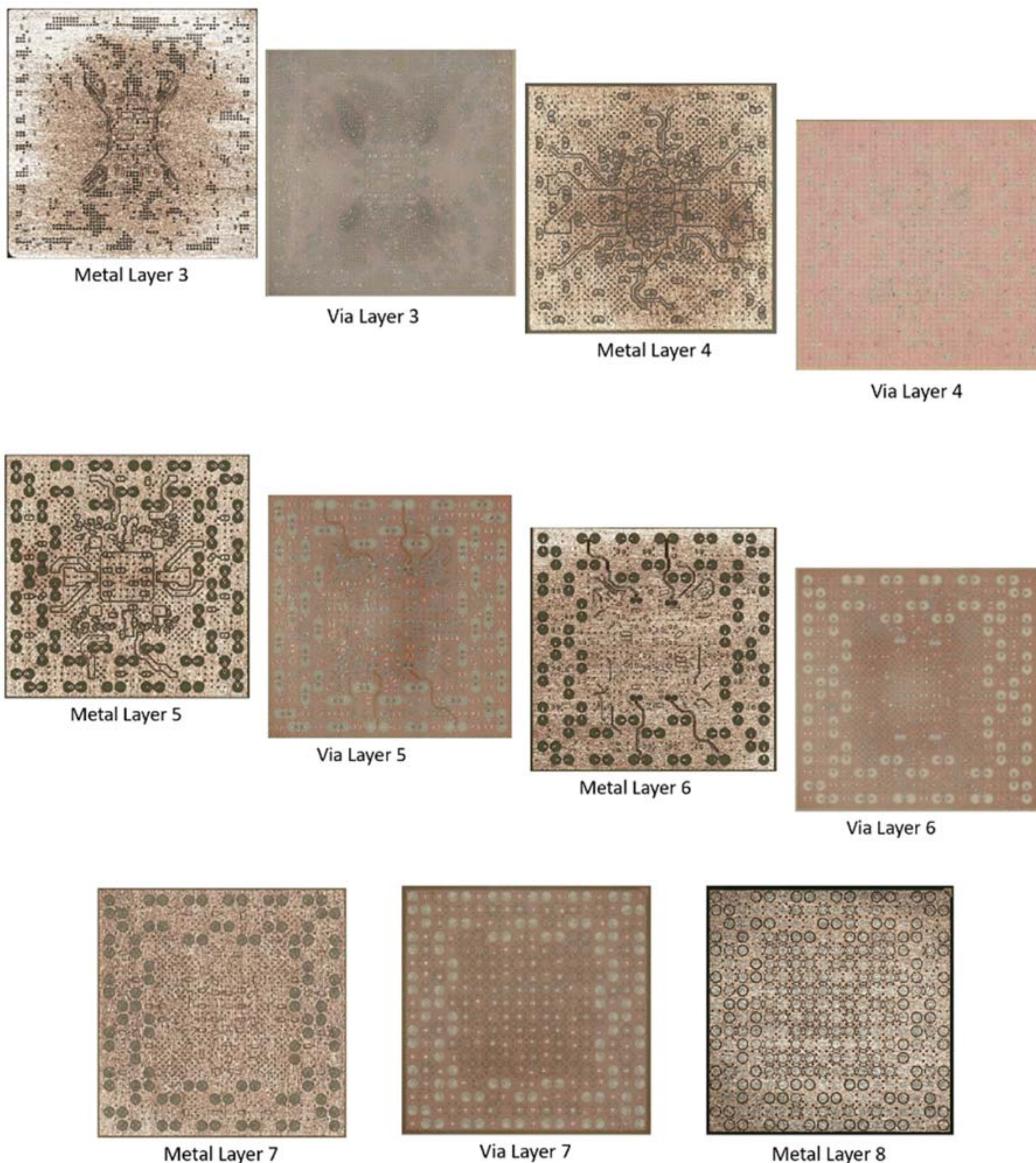
100. As shown below, the TLK10034AAJ is an integrated circuit with an integrated circuit package substrate.



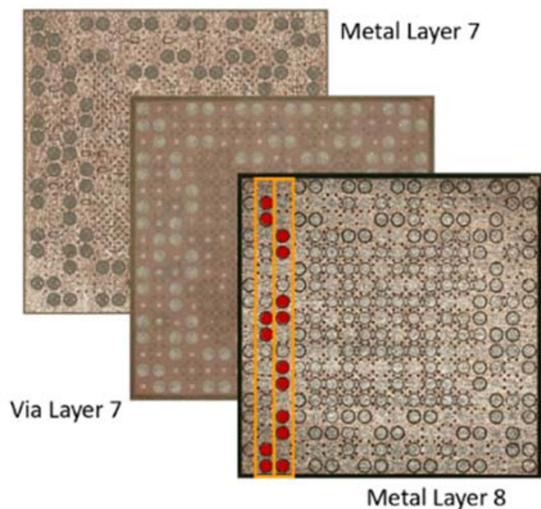


101. The integrated circuit package substrate of the TI TLK10034AAJ is manufactured to have 8 metal layers and 7 via layers.

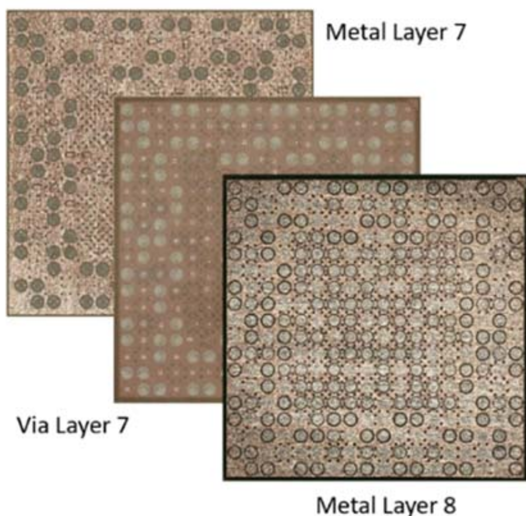




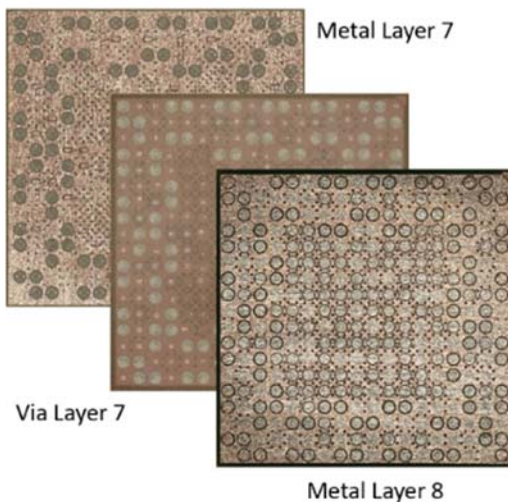
102. During manufacture of the TI TLK10034AAJ, a first electrically conductive layer (metal layer 8) with a plurality of rows (for example, in orange below) of contact pads (for example, shown in red below) is formed.



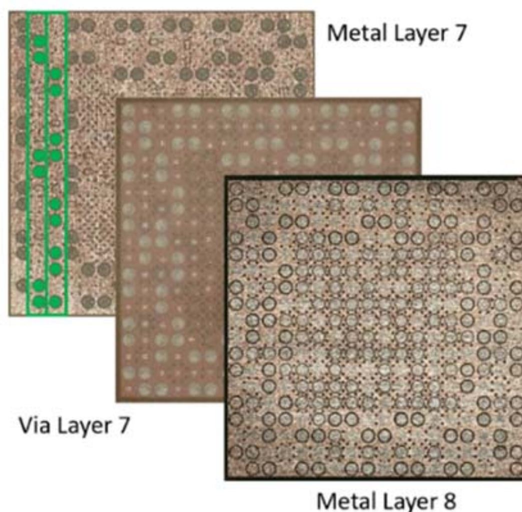
103. During manufacture of the TI TLK10034AAJ, an electrically insulating layer (via layer 7 below) is formed on the first electrically conductive layer (metal layer 8).



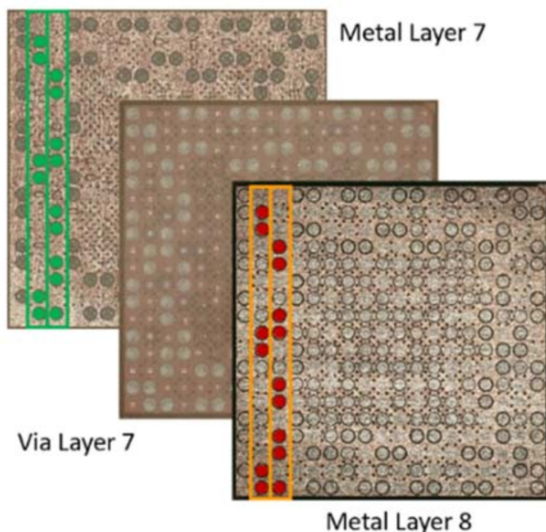
104. During manufacture of the TI TLK10034AAJ, a second electrically conductive layer (metal layer 7) is formed over the electrically insulating layer (via layer 7), such that there is no intermediate conductive layer between the first and second electrically conductive layers (metal layers 8 and 7):



105. The second electrically conductive layer (metal layer 7) comprises metal and has two or more cutouts (for example, as shown in green on metal layer 7 below), wherein each cutout encloses an electrically insulating area within the second electrically conductive layer.



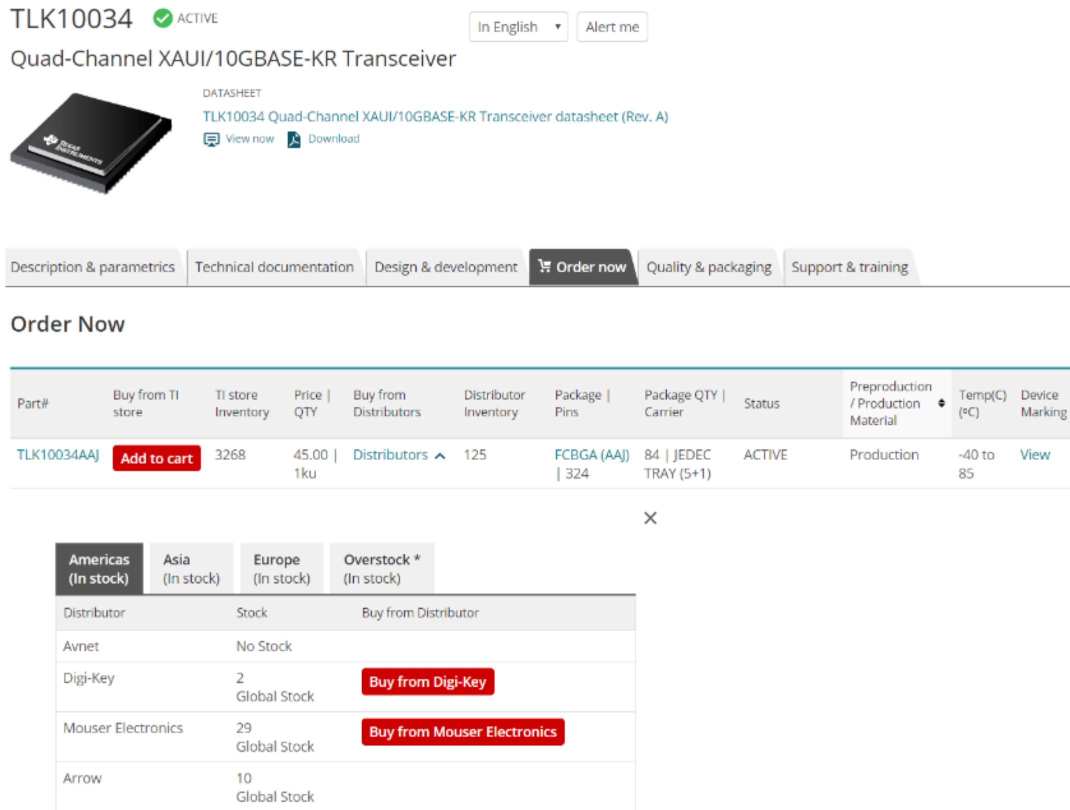
106. Each electrically insulating area (for example, in green) also completely overlaps a corresponding one of the contact pads (in red below) such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.



107. Claim 1 of the Hall 269 Patent applies to each Hall 269 Accused Product at least because each of those products was manufactured to contain the same or similar at least one metal layer, proximate to another metal layer having electrical contacts, that has cutouts as the TI TLK10034AAJ.

108. On information and belief, each of the Hall 269 Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

109. By way of example only, the TLK10034AAJ has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



See http://www.ti.com/product/TLK10034/samplebuy (last visited February 6, 2020).

110. TI has known of the Hall 269 Patent and has been on notice of its infringement of Hall 269 Patent since at least August 30, 2019, when Bell Semic first identified the TLK10034AAJ as infringing and exemplary of TI's infringement of the Hall 269 Patent. After TI did not respond to that letter, Bell Semic sent another letter to TI on January 10, 2020, again identifying the TLK10034AAJ as infringing and exemplary of TI's infringement. TI also did not respond to that letter.

111. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Hall 269 Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

112. TI, knowing that the process of manufacturing its Accused Hall 269 Products infringes the Hall 269 Patent and with specific intent for others to infringe the Hall 269 Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Hall 269 Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Hall 269 Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Hall 269 Accused Products, as well as products incorporating the same.

113. TI knows, and has known since at least August 30, 2019, that the process of manufacturing the Hall 269 Accused Products infringes the Hall 269 Patent. Despite this knowledge, TI knowingly and intentionally instructed, and continues to instruct, its OEMs, package assemblers, and foundry suppliers to infringe the Hall 269 Patent through the unlicensed manufacture and assembly of the Hall 269 Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States. TI further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent by its customers', distributors', and/or other third parties' sale and distribution of the Hall 269 Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. TI further knowing and intentionally aided and abetted, and continues to aid and abet, infringement of the Hall 269 Patent through use, sale, offers for sale, and/or importing in or into the United States of the Hall 269 Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website.

114. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Hall 269 Accused Products and/or products incorporating the Hall 269 Accused Products in the United States by marketing the Hall 269 Accused Products in the United States; providing information such as detailed datasheets supporting use of the Hall 269 Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Hall 269 Accused Products; providing technical documentation for the Hall 269 Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Hall 269 Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Hall 269 Accused Products, including live training and video.

115. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement of the Hall 269 Patent, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

116. TI's infringement of the Hall 269 Patent is and has been knowing, deliberate, and willful. TI learned of its infringement of the Hall 269 Patent no later than August 30, 2019. As detailed above, Bell Semic sent letters to TI on August 30, 2019 and January 10, 2020 identifying the Hall 269 Patent as being infringed by TI's exemplary TLK10034AAJ product. TI

did not respond to either of these letters. Despite these efforts, and knowing that it was willfully infringing the Hall 269 Patent, TI continued, and continues, to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Hall 269 Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Hall 269 Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 3

Willful Infringement of U.S. Patent No. 7,566,964 (Kang Patent)

117. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

118. The Kang Patent is generally related to an integrated circuit device structure and process for fabricating the structure wherein a power bus interconnect structure is formed in the aluminum pad or contact layer. An interconnect structure for interconnecting underlying levels of interconnect can also be formed in the aluminum pad layer. (*See* Kang Patent, Abstract.)

119. Power buses are required in interconnect systems within integrated circuits in order to supply power to the various device elements. In prior interconnect systems, power buses were formed as an additional interconnect layer. The formation of this additional interconnect layer increased fabrication cost due to the increased number of mask steps, mask layers, and process steps involved. The additional process steps also lowered device yield as they presented more opportunities for processing defects to occur. Furthermore, because this power bus interconnect layer conducted a relatively high current, it generally had a greater width, thickness,

and pitch than the signal interconnect layers, and was also a source of noise and parasitic capacitance that could disrupt the performance of proximate devices and interconnect structures. To overcome this problem, the power bus could be isolated from other device structures, but this isolation would correspondingly consume more device area. The interconnect system and power bus taught in the Kang Patent solves these problems by teaching the formation of the power bus in the same aluminum-copper alloy layer as the bond pad. In doing so, the same masking, patterning, and etching steps that are used to form the aluminum bond pad layer were also used to form the power bus in the aluminum layer. Thus, an entire metallization layer can be eliminated, including the associated process steps and mask requirements.

120. The Kang Patent contains 1 independent claim and 7 total claims, covering various integrated circuit devices. Claim 1 reads:

> An integrated circuit device comprising:
>
> a metallization interconnect system overlying a semiconductor substrate, the metallization interconnect system including at least a first and a second interconnect feature located within a dielectric layer;
>
> a power bus located over the metallization interconnect system, the power bus comprising an alloy of aluminum and copper, and further wherein the power bus includes a first contact pad region configured for connection external to the integrated circuit device that is in contact with the first interconnect feature, and a second region in contact with the second interconnect feature; and
>
> a passivation layer overlying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.

121. TI has directly infringed, and continues to directly infringe, one or more claims of the Kang Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Kang Patent (*e.g.*, claims 1-4 and 6-7), including, but not limited to:

- TI's copper-based products that have a metallization interconnect system and a top-level aluminum power distribution layer;
- TI's TM4C123GH6PGEI 32-bit ARM® Cortex®-M4F based microcontroller intended for developers of a range of industrial applications including remote monitoring, electronic point-of-sale machines, test and measurement equipment, network appliances and switches, factory automation, HVAC and building control, gaming equipment, motion control, transportation, and fire and security;
- TI's Hercules RM48L952 16/32-Bit RISC flash microcontroller intended for industrial safety applications such as industrial automation, safe PLCs, power generations and distribution, windmills and turbines, and elevators and escalators and medical applications such as ventilators, defibrillators, infusion and insulin pumps, radiation therapy, and robotic surgery; and
- TI's devices that are variants of the above-identified products;

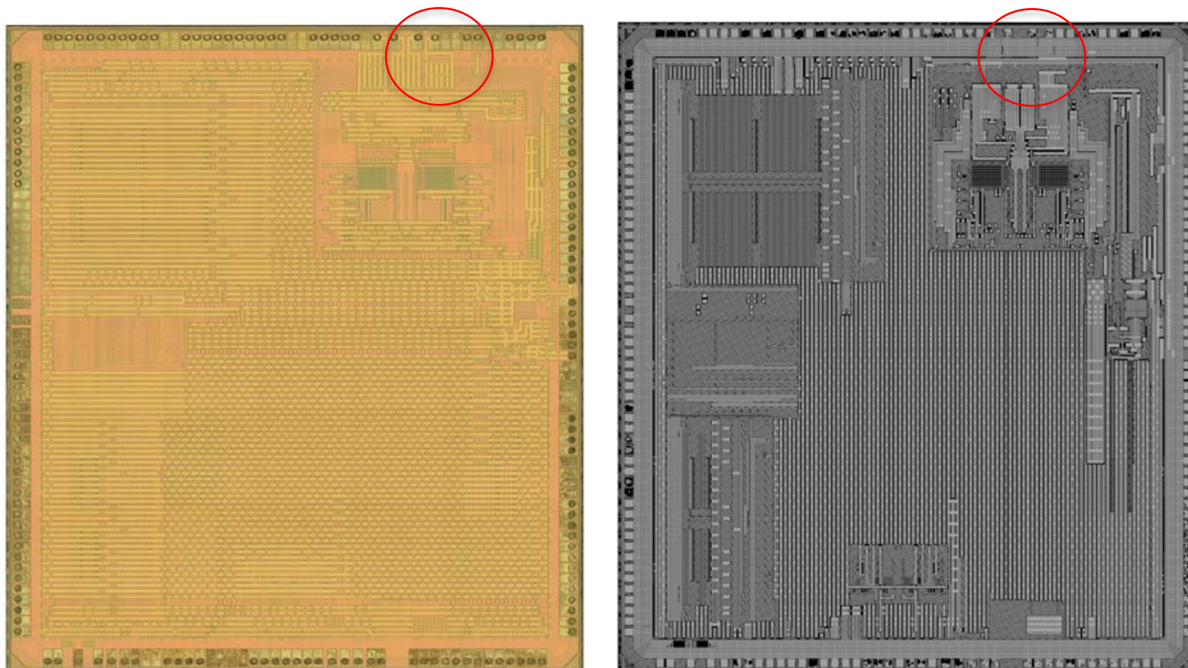
(collectively "Kang Accused Products").

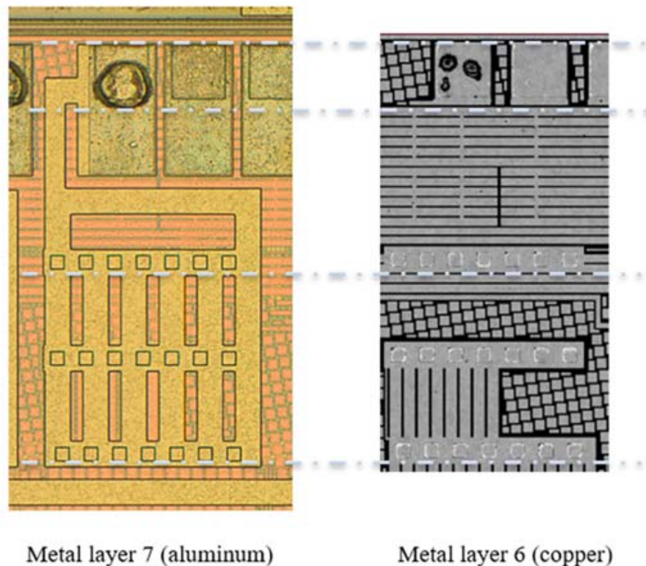
122. By way of non-limiting example only, TI's TM4C123GH6PGEI infringes claim 1 of the Kang Patent because it is an integrated circuit device that has (1) a metallization interconnect system overlying a semiconductor substrate, the metallization interconnect system including at least a first and a second interconnect feature located within a dielectric layer; (2) a power bus located over the metallization interconnect system, the power bus comprising an alloy of aluminum and copper, and further wherein the power bus includes a first contact pad region configured for connection external to the integrated circuit device that is in contact with the first interconnect feature, and a second region in contact with the second interconnect feature; and (3)

a passivation layer overlaying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.

123. As shown below, the TI TM4C123GH6PGEI is an integrated circuit device.

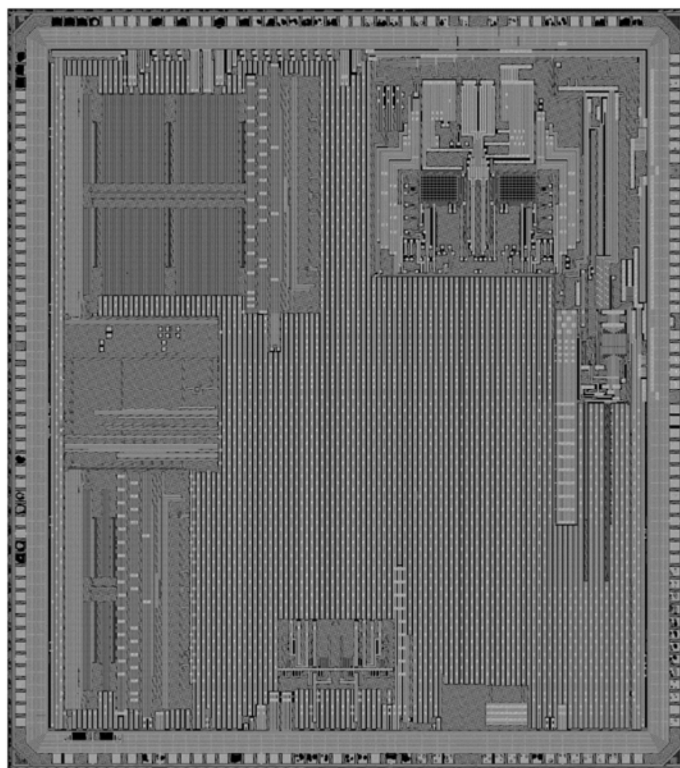
124. The TI TM4C123GH6PGEI has multiple layers, including the layers below.



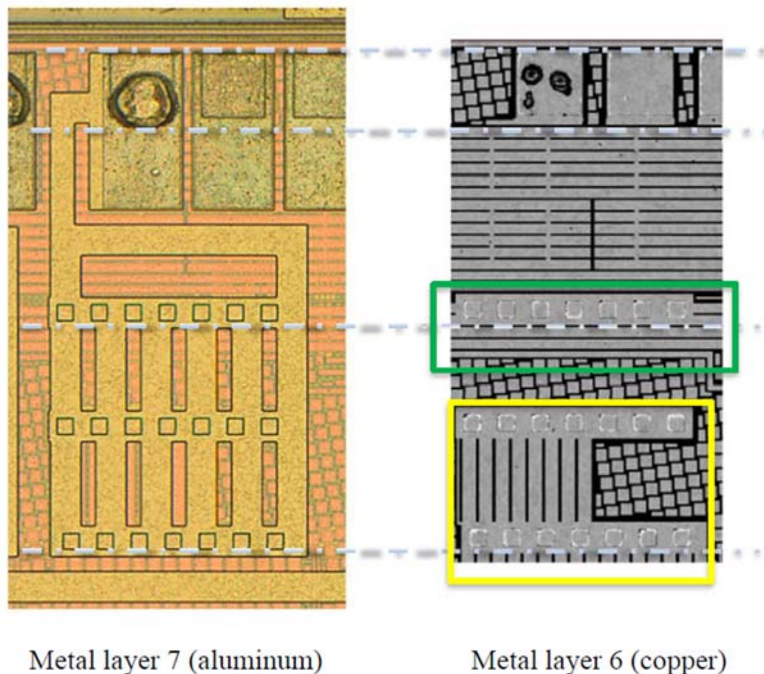


Metal layer 7 (aluminum) Metal layer 6 (copper)

125. The TI TM4C123GH6PGEI has a metallization interconnect system overlying a semiconductor substrate.

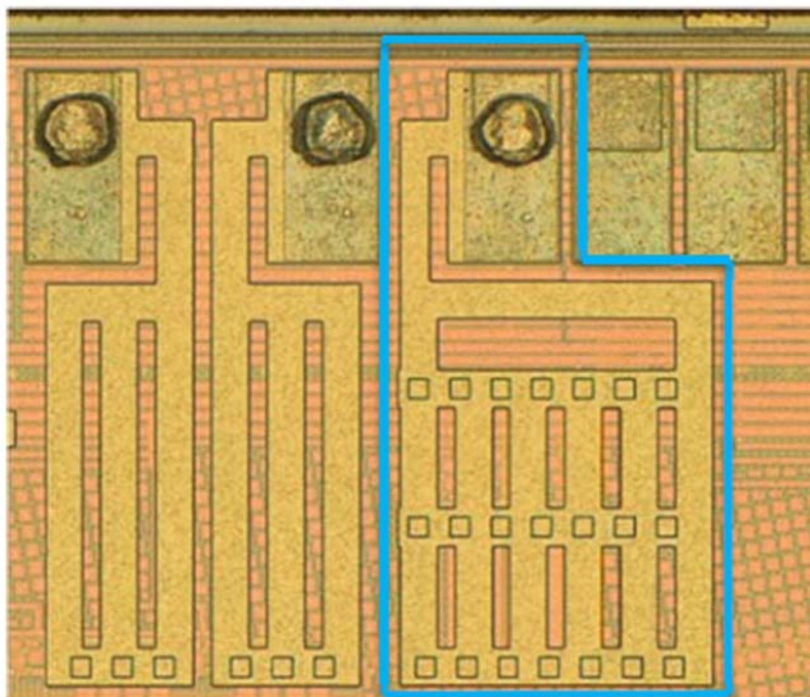


126. The metallization interconnect system (i.e., copper layers 1-6) in the TI TM4C123GH6PGEI includes at least a first and a second interconnect feature (*e.g.,* features in green and yellow below, respectively) located within a dielectric layer.

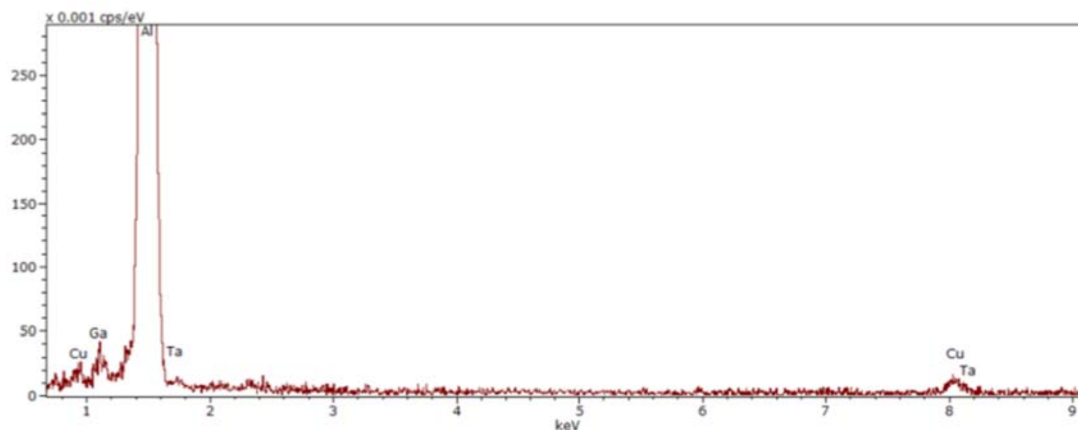


Metal layer 7 (aluminum)   Metal layer 6 (copper)

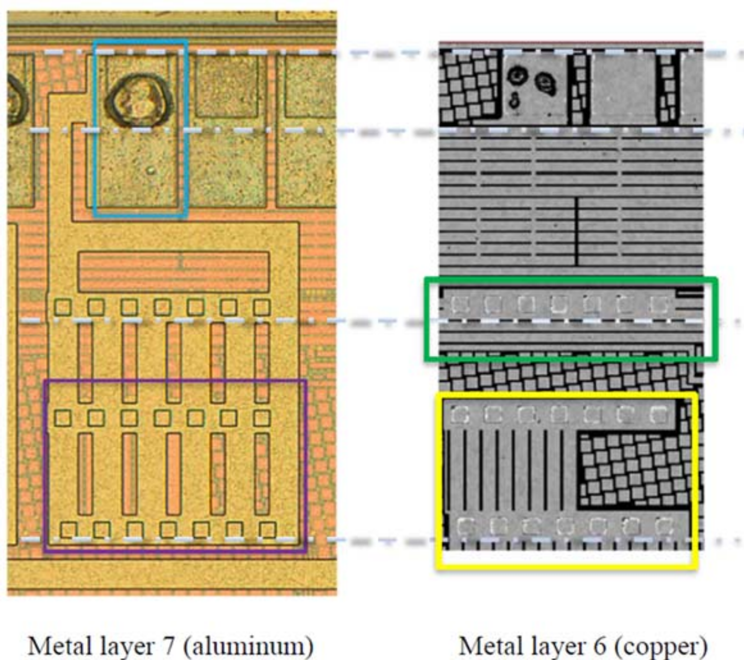
127. The TI TM4C123GH6PGEI also has a power bus (*e.g.,* in blue below) located over the metallization interconnect system.



128. The power bus comprises an alloy of aluminum and copper. *See, e.g.,* Energy Dispersive Spectroscopic analysis below evidencing an alloy of aluminum and copper.

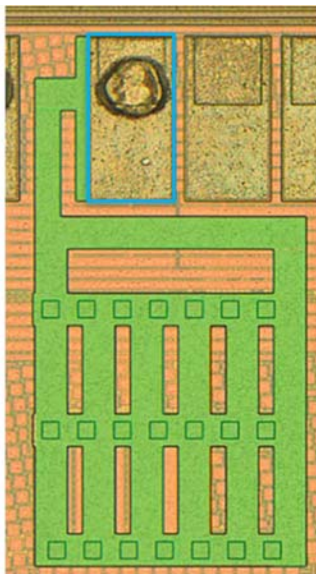


129. The power bus also includes a first contact pad region (*e.g.,* blue below) configured for connection external to the integrated circuit device that is in contact with the first interconnect feature (*e.g.,* green below), and a second region (*e.g.,* purple below) in contact with the second interconnect feature (*e.g.,* yellow below).



Metal layer 7 (aluminum) Metal layer 6 (copper)

130. The TI TM4C123GH6PGEI also has a passivation layer (*e.g.,* shaded green below) overlying at least a portion of the power bus to expose at least a portion of the first contact pad region and protect the second region.



Metal layer 7 (aluminum)

131. Claim 1 of the Kang Patent applies to each Kang Accused Product at least because each of those products contain the same or similar copper-based metallization interconnect system and a top-level aluminum power distribution layer as the TI TM4C123GH6PGEI.

132. On information and belief, each of the Kang Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

133. By way of example only, the TI TM4C123GH6PGEI has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:

TM4C123GH6PGE ACTIVE

In English ▼ | Alert me

High performance 32-bit ARM® Cortex®-M4F based MCU

DATASHEET

Tiva C Series TM4C123GH6PGE Microcontroller Data Sheet datasheet (Rev. E)

Download

ERRATA

Corrections to Tiva™ TM4C123x/TM4C129x Data Sheets Manual Update Sheet

Tiva C Series TM4C123x Microcontrollers Silicon Revisions 6 and 7 Errata (Rev. F)

ARM® Cortex™-M4F Errata (v3)

Description & parametrics | Technical documentation | Design & development | Order now | Quality & packaging | Support & training

Order Now

Part#	Buy from TI store	TI store Inventory	Price | QTY	Buy from Distributors	Distributor Inventory	Package | Pins	Package QTY | Carrier	Status	Preproduction / Production Material	Temp(C)	Device Marking
TM4C123GH6PGEI7	Add to cart	4111	5.24 | 1ku	Distributors	337	LQFP (PGE) | 144	60	ACTIVE	Production	-40 to 85	View

×

Americas (In stock) | Asia (In stock) | Europe (In stock) | Overstock * (0 stock)

Distributor	Stock	Buy from Distributor
Avnet	No Stock	
Digi-Key	303 Global Stock	Buy from Digi-Key
Mouser Electronics	34 Global Stock	Buy from Mouser Electronics
Arrow	No Stock	

See https://www.ti.com/product/TM4C123GH6PGE/samplebuy (last visited February 15, 2020).

134. TI has known of the Kang Patent's disclosure since at least April 2008, when TI and its Deputy General Patent Counsel, Warren L. Franz received an International Search Report specifically citing Kang's disclosure as relevant to TI's International Patent Application WO 2007/027994A3, and TI was made further aware of the Kang Patent and has been on notice of its infringement of the Kang Patent since at least January 10, 2020, when Bell Semic identified the TI TM4C123GH6PGEI as infringing and exemplary of TI's infringement of the Kang Patent. TI did not respond to this letter.

135. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Kang Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

136. TI, knowing its products infringe the Kang Patent and with specific intent for others to infringe the Kang Patent, has induced infringement, and continues to induce infringement, of one or more claims of the Kang Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Kang Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Kang Accused Products in the United States. TI knows, and has known since at least January 10, 2020, that the Kang Accused Products infringe the Kang Patent, and purposefully and knowingly sells and offers to sell the Kang Accused Products to its customers with the knowledge and expectation that the Kang Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

137. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Kang Accused Products and/or products incorporating the Kang Accused Products in the United States by marketing the Kang Accused Products in the United States; providing information such as detailed datasheets supporting use of the Kang Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Kang Accused Products; providing

technical documentation for the Kang Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Kang Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Kang Accused Products, including live training and video.

138. TI has contributed to the infringement of, and continue to contribute to the infringement of, one or more claims of the Kang Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Kang Accused Products, which constitute a material part of the invention of the Kang Patent, knowing the Kang Accused Products to be especially made or especially adapted for use in infringement of the Kang Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

139. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

140. TI's infringement of the Kang Patent is and has been knowing, deliberate, and willful. TI has known of the Kang Patent's disclosure since April 2008. TI learned of its infringement of the Kang Patent from Bell Semic no later than January 10, 2020. As detailed above, Bell Semic sent a letter to TI on January 10, 2020 identifying the Kang Patent as being

infringed by TI's exemplary TM4C123GH6PGEI product. TI did not respond to this letter. Despite these efforts, and knowing that it was willfully infringing the Kang Patent, TI continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Kang Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Kang Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 4

Willful Infringement of U.S. Patent No. 6,281,129 (Merchant Patent)

141. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

142. The Merchant Patent is generally related to methods of manufacturing a semiconductor device by using a polishing apparatus with a polishing pad conditioning wheel that has a conditioning head, a setting alloy, an abrasive material, and a corrosion resistant coating. The conditioning head has opposing first and second faces with the first face coupleable to the polishing apparatus. The setting alloy is coupled to the conditioning head at the second face, and the abrasive material is embedded in the setting alloy, which is substantially covered by the corrosion resistant coating. (*See* Merchant Patent, Abstract.)

143. Chemical mechanical planarization (CMP) is used in the manufacture of semiconductor devices in order to create dielectric and metal layers that are extremely flat and of a precise thickness needed to pattern the features that comprise a semiconductor device. CMP

involves the polishing of a wafer using a polishing pad and a chemical/mechanical slurry. The polishing process results in pad material and slurry residues collecting in pores of the polishing pad, requiring that the polishing pad be conditioned using a conditioning wheel. During conditioning, the conditioning wheel comes into contact with residue of the chemical/mechanical slurry from the polishing pad, which attacks the setting alloy that holds the abrasive materials on the conditioning wheel. As a result, over time, the abrasive materials loosen from the conditioning wheel, reducing the effective surface area of the conditioning wheel and slowing the conditioning process. The Merchant Patent addresses this problem by teaching the use of a corrosion resistant coating and a hard-facing metal alloy, such as a nickel / chromium / iron alloy, as the setting alloy in the conditioning wheel. Due to the corrosion resistant coating and the use of the hard-facing metal alloy, which is significantly resistive to the corrosive effects of the materials used in chemical/mechanical slurries, the usable lifetime of the conditioning head is improved.

144. The Merchant Patent contains 2 independent claims and 9 total claims, covering various methods. Claim 5 depends from independent claim 1 and reads:

> [A method of manufacturing a semiconductor device, comprising:
>
> polishing a semiconductor wafer with a chemical/mechanical slurry against a polishing pad, the polishing forming variations in a polishing surface of the polishing pad; and
>
> conditioning the polishing surface with a polishing pad conditioning wheel comprising:
>
> a conditioning head having opposing first and second faces, the first face coupleable to a polishing apparatus;
>
> a setting alloy coupled to the conditioning head at the second face;
>
> abrasive material embedded in the setting alloy; and
>
> a corrosion resistant coating affixed to the setting alloy],

wherein conditioning includes conditioning with a polishing pad conditioning wheel wherein the setting alloy comprises a hard facing metal alloy.

145. TI has directly infringed one or more claims of the Merchant Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Merchant Patent, and/or TI has directly infringed one or more claims of the Merchant Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Merchant Patent (*e.g.*, claims 5-7). Such products manufactured using these infringing methods include, but are not limited to:

- TI products manufactured using a chemical-mechanical polishing process to polish metals including tungsten and copper;
- TI's AWR1642 integrated single-chip automotive radar sensor using TI's mmWave sensor technology intended as a complete platform solution for the automotive space;
- TI's DM3725CUS digital media processor intended to provide ARM and graphics performance with low power consumption for applications including portable data terminals, navigation, auto infotainment, gaming, medical imaging, home automation, human interface, industrial control, test and measurement, and single board computers;
- TI's WL1807MOD certified WiLink 8 module with high throughput and extended range along with Wi-Fi and Bluetooth coexistence in a power-optimized design for applications including the internet of things (IoT), multimedia, home electronics, home appliances and white goods, industrial and home automation, smart gateway and metering, video conferencing video camera and security;

- TI's Hercules RM48L952 16/32-Bit RISC flash microcontroller intended for industrial safety applications such as industrial automation, safe PLCs, power generations and distribution, windmills and turbines, and elevators and escalators and medical applications such as ventilators, defibrillators, infusion and insulin pumps, radiation therapy, and robotic surgery;
- TI's TM4C123GH6PGEI 32-bit ARM® Cortex®-M4F based microcontroller intended for developers of a range of industrial applications including remote monitoring, electronic point-of-sale machines, test and measurement equipment, network appliances and switches, factory automation, HVAC and building control, gaming equipment, motion control, transportation, and fire and security;
- TI's TMS320DM6467 digital media SoC supporting a range of encode, decode, and transcode operations making it suitable for digital media and video applications;
- TI's TLK10034AAJ quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems;
- TI's DRV2624 haptic driver for mobile phones and tablets;
- TI's DLP3010AFQK digital micromirror device;
- TI's TPD12S015A integrated HDMI companion chip solution for HDMI 1.3/1.4 interfaces, for both portable and non-portable electronics applications;
- TI's TPS65912 power management IC intended for use in data cards, smart phones, wireless routers and switches, tablets, industrial applications, LTE modems, and GPS;
- TI's BQ24725 high-efficiency, synchronous battery charger, with low component count for space-constraint, multi-chemistry battery charging applications;

- TI's TPS65632 AMOLED (Active Matrix Organic Light Emitting Diode) display power supply solution designed to drive AMOLED displays requiring three supply rails;
- TI's ADS1261 high-accuracy, single-chip analog-to-digital converter solution for measurements, for example, weigh scales and resistance temperature detectors;
- TI's TPA3110D2 stereo amplifier (15 watts per channel) used in televisions and consumer audio equipment;
- TI's TSC2004 very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on advanced low-voltage processors;
- TI's TPS92661 compact, highly-integrated LED matrix manager for shunt FET dimming for large arrays of high-brightness LEDs in applications such as automotive headlights;
- TI's AWR1443FQIGABYA60E integrated single-chip automotive radar sensor using TI's mmWave sensor technology used as a radar system for the automotive space;
- TI's IWR1642AQAGABLR integrated single-chip industrial radar sensor using TI's mmWave sensor technology used as a low-power, self-monitored, and ultra-accurate radar systems for use in industrial applications such as building automation, factory automation, drones, material handling, traffic monitoring, and surveillance; and
- TI's devices that are variants of the above-identified products;

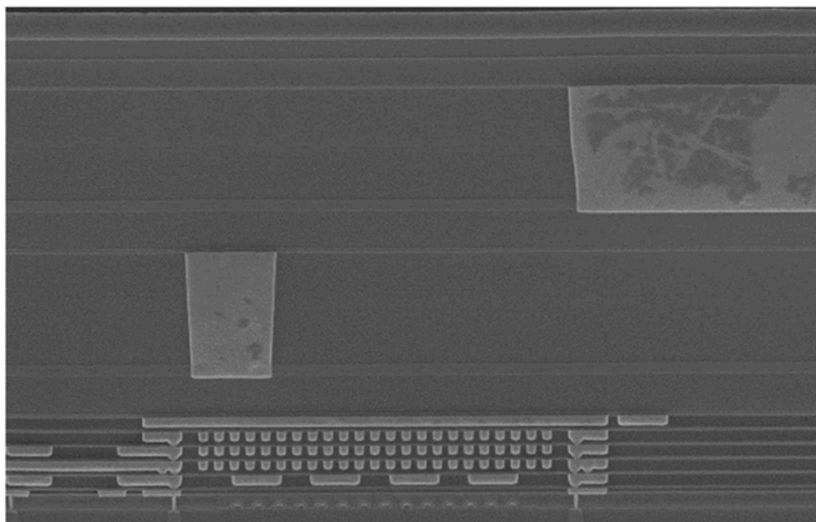
(collectively "Merchant Accused Products").

146. By way of non-limiting example only, the process of manufacturing the TI AWR1642 meets all the steps of claim 5 of the Merchant Patent including the steps of (1) polishing a semiconductor wafer with a chemical/mechanical slurry against a polishing pad, the

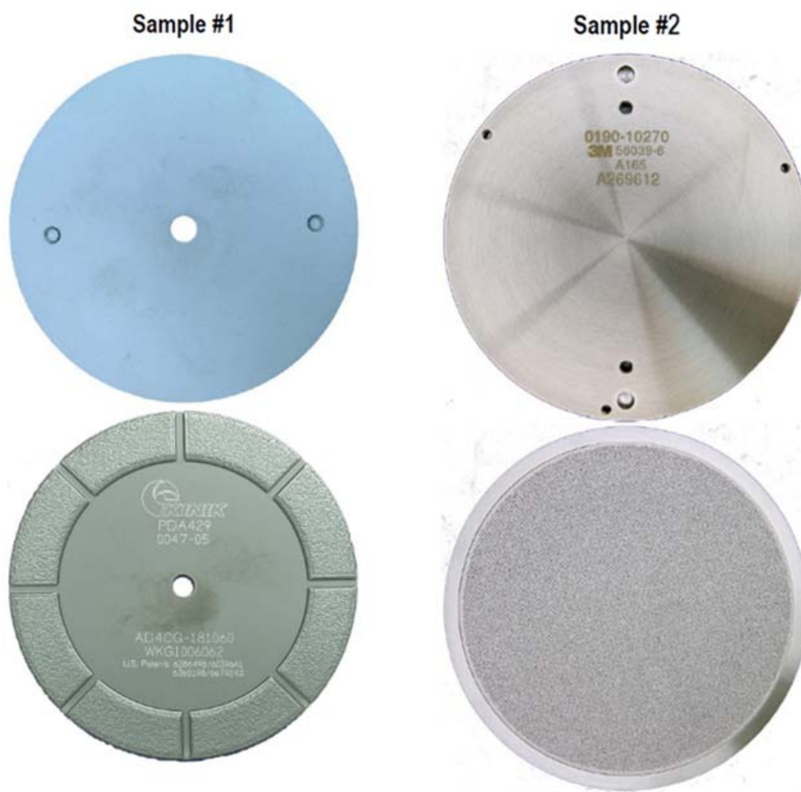
polishing forming variations in a polishing surface of the polishing pad; and (2) conditioning the polishing surface with a polishing pad conditioning wheel that has (i) a conditioning head with opposing first and second faces, where the first face is coupleable to a polishing apparatus; (ii) a setting alloy coupled to the conditioning head at the second face; (iii) abrasive material embedded in the setting alloy; and (iv) a corrosion resistant coating affixed to the setting alloy, and the setting alloy comprises a hard-facing metal alloy.

147. As shown below, the TI AWR1642 is a semiconductor device.

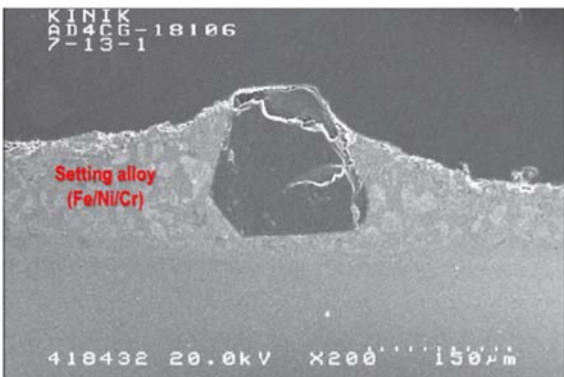
148. On information and belief, the TI AWR1642 is manufactured using a chemical mechanical planarization step to create an extremely flat and precise thickness that is necessary to manufacture a functioning device. The chemical mechanical planarization process includes the polishing of a semiconductor wafer with a chemical/mechanical slurry against a polishing pad. The polishing process inherently causes the polishing pad to become clogged with pad material and slurry residue, making it necessary to condition the polishing pad to restore its full functionality.



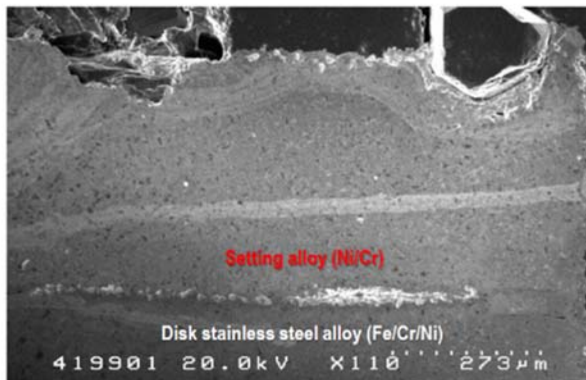
149. On information and belief, this polishing included the use of an industry standard polishing pad conditioning wheel, such as the two sample conditioning wheels below. The top picture of each sample shows a first face that can be coupled to a polishing apparatus.



150. These sample conditioning wheels each have a setting alloy coupled to the conditioning head at the second face.

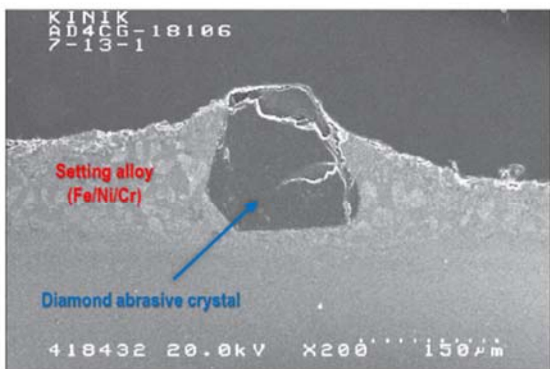


Sample #1

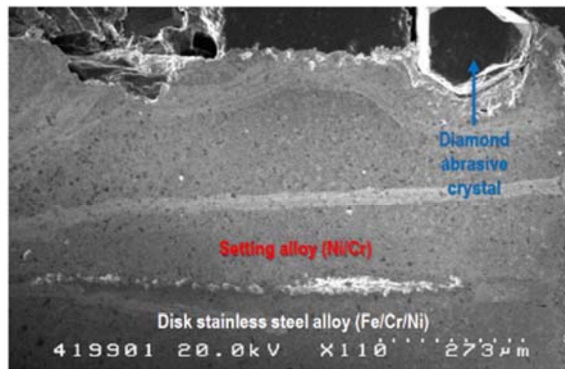


Sample #2

151. These sample conditioning wheels further have abrasive material embedded in the setting alloy.

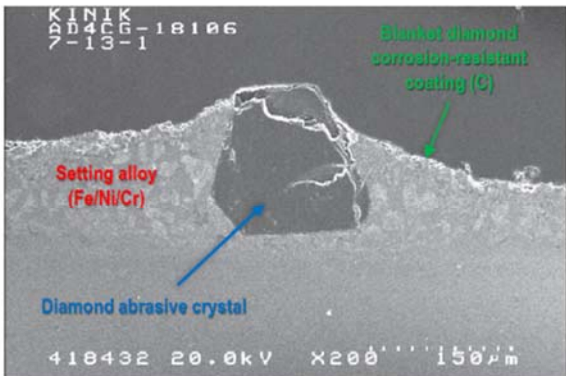


Sample #1

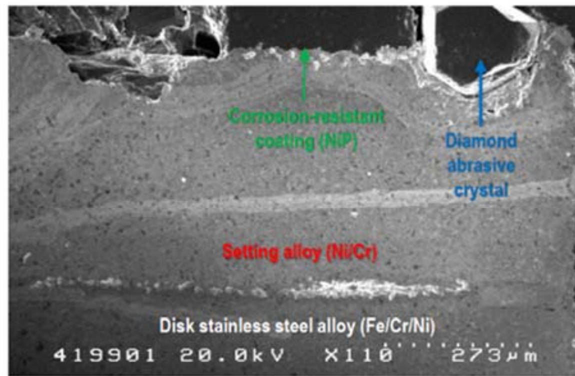


Sample #2

152. These sample conditioning wheels further have a corrosion resistant coating affixed to the setting alloy.

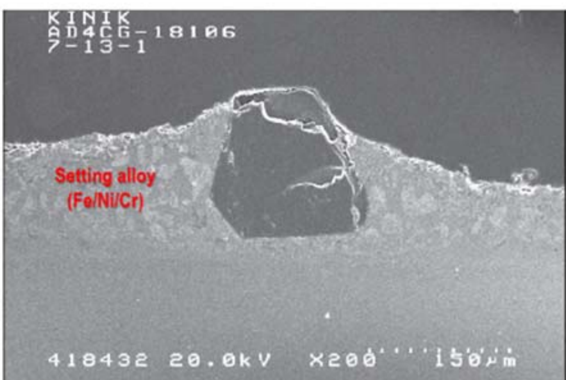


Sample #1

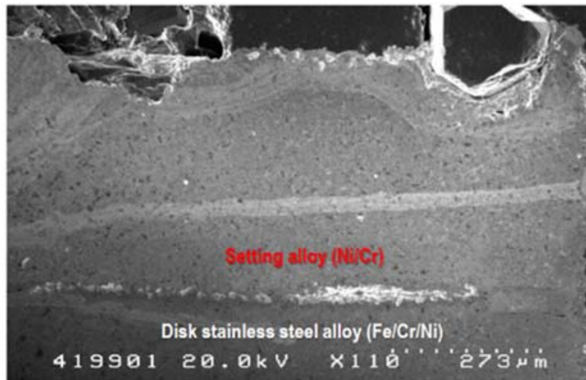


Sample #2

153. The setting alloy used in these sample conditioning wheels is a hard facing metal alloy, *i.e.,* iron nickel chromium and nickel chromium alloys, respectively.



Sample #1

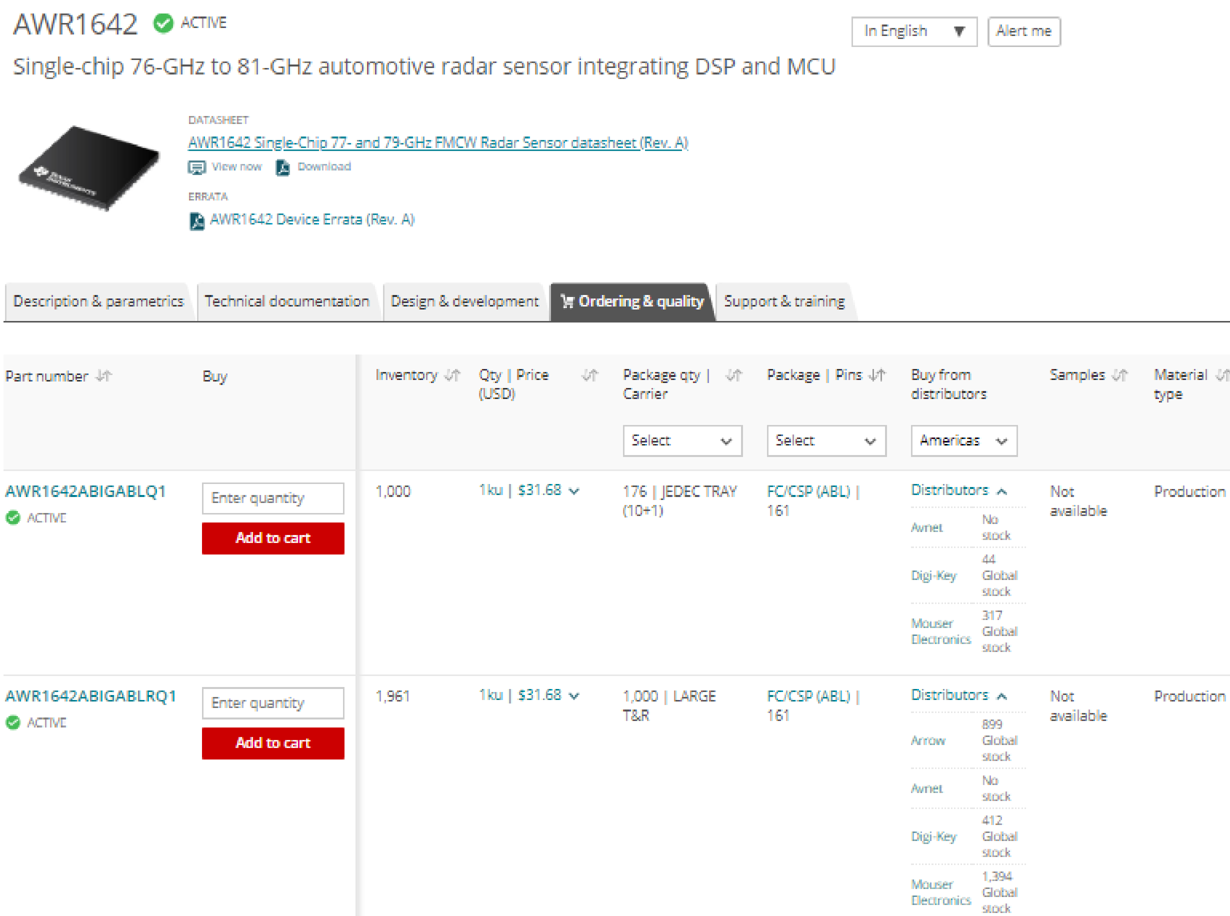


Sample #2

154. Claim 5 of the Merchant Patent applies to each Merchant Accused Product at least because each of those products are manufactured using the same or similar CMP process to polish metals including tungsten and copper as the TI AWR1642.

155. On information and belief, each of the Merchant Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

156. By way of example only, the TI AWR1642 has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



See http://www.ti.com/product/AWR1642/samplebuy (last visited February 15, 2020).

157. TI has known of the Merchant Patent and has been on notice of its infringement of Merchant Patent since at least August 30, 2019, when Bell Semic first identified the AWR1642, DM3725CUS, WL1807MOD, RM48L952, TM4C123GH6PGEI, TMS320DM6467, TLK10034AAJ, DRV2624, DLP3010AFQK, TPD12S015A, TPS65912, BQ24725, TPS65632, ADS1261, TPA3110D2, TSC2004, and TPS92661 as infringing the Merchant Patent. After TI did not respond to that letter, Bell Semic sent another letter to TI on January 10, 2020, again

identifying the aforementioned TI products as infringing and further identified the AWR1443FQIGABYA60E and IWR1642AQAGABLR as infringing the Merchant Patent. TI also did not respond to that letter.

158. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Merchant Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

159. TI, knowing that the process of manufacturing its Accused Merchant Products infringed the Merchant Patent and with specific intent for others to infringe the Merchant Patent, induced infringement of one or more claims of the Merchant Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least (1) by actively inducing others to make in the United States without authorization the Merchant Accused Products; and/or (2) by actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Merchant Accused Products, and products incorporating the same.

160. TI has known since at least August 30, 2019 that the process of manufacturing the Merchant Accused Products infringed the Merchant Patent. Despite this knowledge, TI knowingly and intentionally instructed its OEMs and foundry suppliers to infringe the Merchant Patent through the unlicensed manufacture of the Merchant Accused Products with the expectation that such products would be used, sold, offered for sale, and/or imported in or into the United States. TI further knowingly and intentionally aided and abetted infringement of the Merchant Patent by its customers', distributors', and/or other third parties' sale and distribution of the Merchant Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. TI further knowing and intentionally aided and abetted infringement of the

Merchant Patent through the use, sale, offers for sale and/or importing in or into the United States of the Merchant Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website.

161. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Merchant Accused Products and/or products incorporating the Merchant Accused Products in the United States by marketing the Merchant Accused Products in the United States; providing information such as detailed datasheets supporting use of the Merchant Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Merchant Accused Products; providing technical documentation for the Merchant Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Merchant Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Merchant Accused Products, including live training and video.

162. Bell Semic has sustained and is entitled to recover damages as a result of TI's past infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

163. TI's infringement of the Merchant Patent was knowing, deliberate, and willful. TI learned of its infringement of the Merchant Patent no later than August 30, 2019. As detailed above, Bell Semic sent a letter to TI on August 30, 2019 identifying the Merchant Patent as being infringed by several TI products. TI did not respond to this letter. Despite these efforts, and knowing that it was willfully infringing the Merchant Patent, TI continued to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Merchant Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct was egregious. TI's knowing, deliberate, and willful infringement of the Merchant Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 5

Willful Infringement of U.S. Patent No. 6,879,046 (Gibson Patent)

164. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

165. The Gibson Patent is generally related to a split barrier layer that enables copper interconnect wires to be used in conjunction with low-k dielectric films by preventing the diffusion of N—H base groups into photoresists where they can render the photoresist insoluble. The split barrier layer is disposed between the copper and the low-k dielectric, and including a nitrogen-containing, oxygen-free film which contacts the copper, and an oxygen-containing, nitrogen-free film which contacts the low-k dielectric film. The nitrogen-containing film

prevents the diffusion of N—H base groups into the low-k dielectric films. (*See* Gibson Patent, Abstract.)

166. During the fabrication of semiconductor devices, the lithography process uses chemically amplified deep ultra-violet (DUV) photoresists to improve the performance of the lithography system and improve device feature resolution. Low dielectric constant (low-k) dielectrics and copper interconnect schemes are favored manufacturing techniques because they increase device speed, provide lower cost processing, and improve level-to-level alignment, which provide for tighter design rules and improve performance. However, during the patterning of the low-k dielectric material to form the damascene or dual-damascene structures, this combination causes base groups such as N—H base groups to diffuse into porous regions of the low-k dielectric materials, rendering any exposed photoresist that interacted with the N—H base group insoluble to developer solution. The N—H base groups are formed during the dual damascene process, where the etch stop layers and barrier films contain nitrogen and N—H base groups are formed. Additionally, ammonia compounds are used to clean or treat copper surfaces to remove any oxides that may have formed and to remove any organic corrosion inhibitor. These ammonia containing chemistries also produce the N—H base group. The Gibson Patent solves this problem by providing a method and structure for isolating copper surfaces and nitrogen-containing layers and films, from low-k dielectric materials. The Gibson Patent teaches isolating of these layers by forming a split barrier layer that is disposed between the copper and the low-k dielectric, and including a nitrogen-containing, oxygen-free film which contacts the copper, and an oxygen-containing, nitrogen-free film which contacts the low-k dielectric film. The oxygen-containing film prevents the diffusion of N—H base groups into the low-k dielectric films.

167. The Gibson Patent contains 4 independent claims and 13 total claims, covering various semiconductor products. Claim 1 reads:

> A semiconductor product comprising a barrier layer disposed between a copper-containing structure and a low-k dielectric film, said barrier layer comprising a composite film structure including a nitrogen-containing, substantially oxygen-free first film forming a boundary with said copper containing structure and an oxygen-containing, substantially nitrogen-free second film forming a boundary with said low-k dielectric film in which said first film comprises nitrogen-doped silicon carbide and said second film comprises oxygen-doped silicon carbide.

168. TI has directly infringed, and continues to directly infringe, one or more claims of the Gibson Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Gibson Patent (*e.g.*, claims 1-3 and 7), including, but not limited to:

- TI products with a split barrier layer that enables copper interconnect wires to be used in conjunction with low-k dielectric films;
- TI's WL1807MOD certified WiLink 8 module with high throughput and extended range along with Wi-Fi and Bluetooth coexistence for applications including the internet of things (IoT), multimedia, home electronics, home appliances and white goods, industrial and home automation, smart gateway and metering, video conferencing video camera and security;
- TI's AWR1642 integrated single-chip automotive radar sensor using TI's mmWave sensor technology intended as a complete platform solution for the automotive space;
- TI's devices that are variants of the above-identified products; and

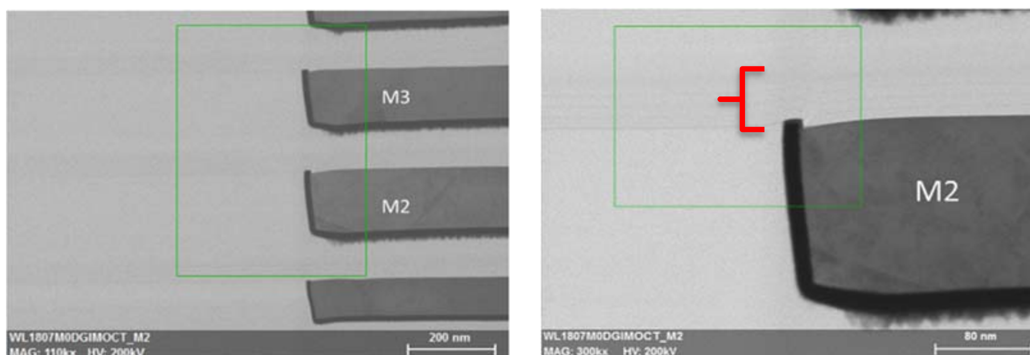
- all other TI semiconductor devices, integrated circuits, and products that have copper interconnects and are manufactured using chemically amplified photoresists which use the infringing technology;

(collectively "Gibson Accused Products").

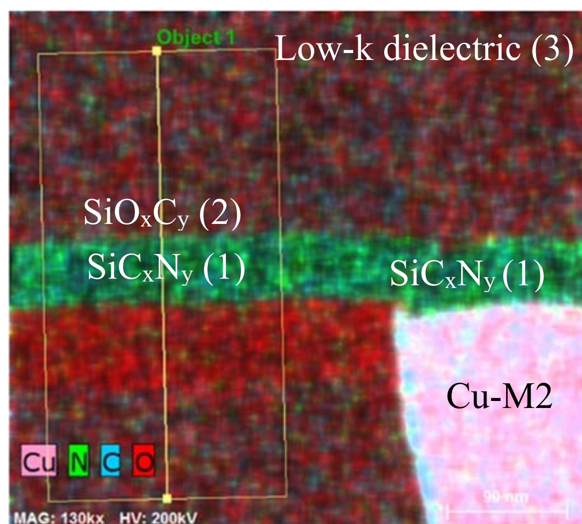
169. By way of non-limiting example only, TI's WL1807MOD infringes claim 1 of the Gibson Patent because it is a semiconductor product that has a barrier layer disposed between a copper-containing structure and a low-k dielectric film, where the barrier layer comprises a composite film structure with (1) a nitrogen-containing, substantially oxygen-free first film forming a boundary with the copper-containing structure and (2) an oxygen-containing, substantially nitrogen-free second film forming a boundary with the low-k dielectric film, where the first film comprises nitrogen-doped silicon carbide and the second film comprises oxygen-doped silicon carbide.

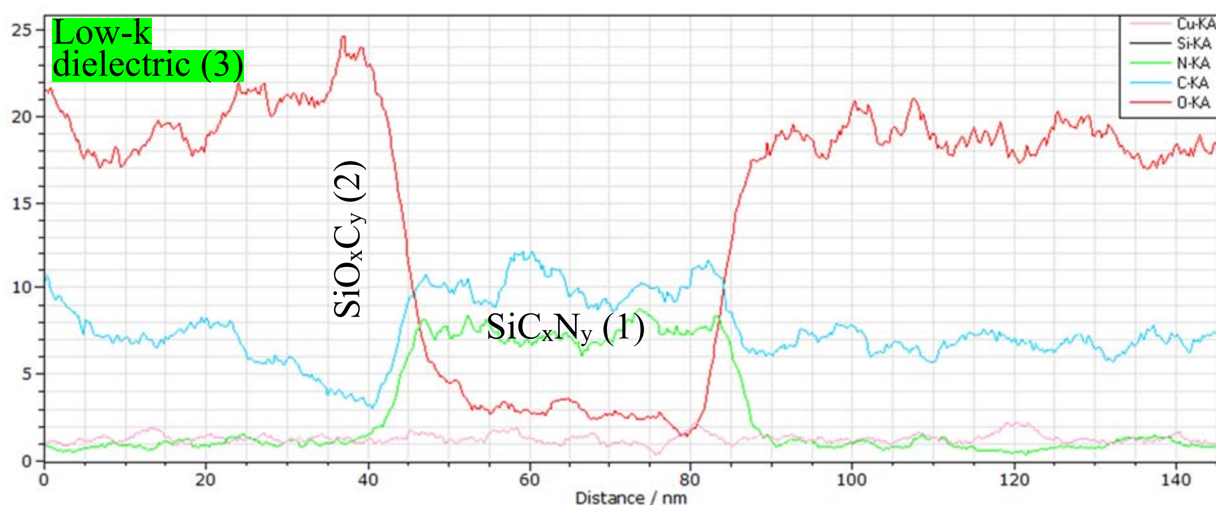
170. As shown below, the WL1807MOD is a semiconductor product:

171. The WL1807MOD has a barrier layer (indicated in red below) between a copper containing structure (designated M2 below) and a low-k dielectric film disposed above the barrier layer:



172. The barrier layer in the WL1807MOD comprises a composite film structure with a nitrogen-containing, substantially oxygen-free first film (SiC_xN_y in the barrier layer) forming a boundary with the copper-containing structure(Cu-M2) and an oxygen-containing, substantially nitrogen-free second film (SiO_xC_y in the barrier layer) forming a boundary with the low-k dielectric film above the barrier layer. The first film comprises nitrogen-doped silicon carbide (SiC_xN_y) and the second film comprises oxygen-doped silicon carbide (SiO_xC_y).

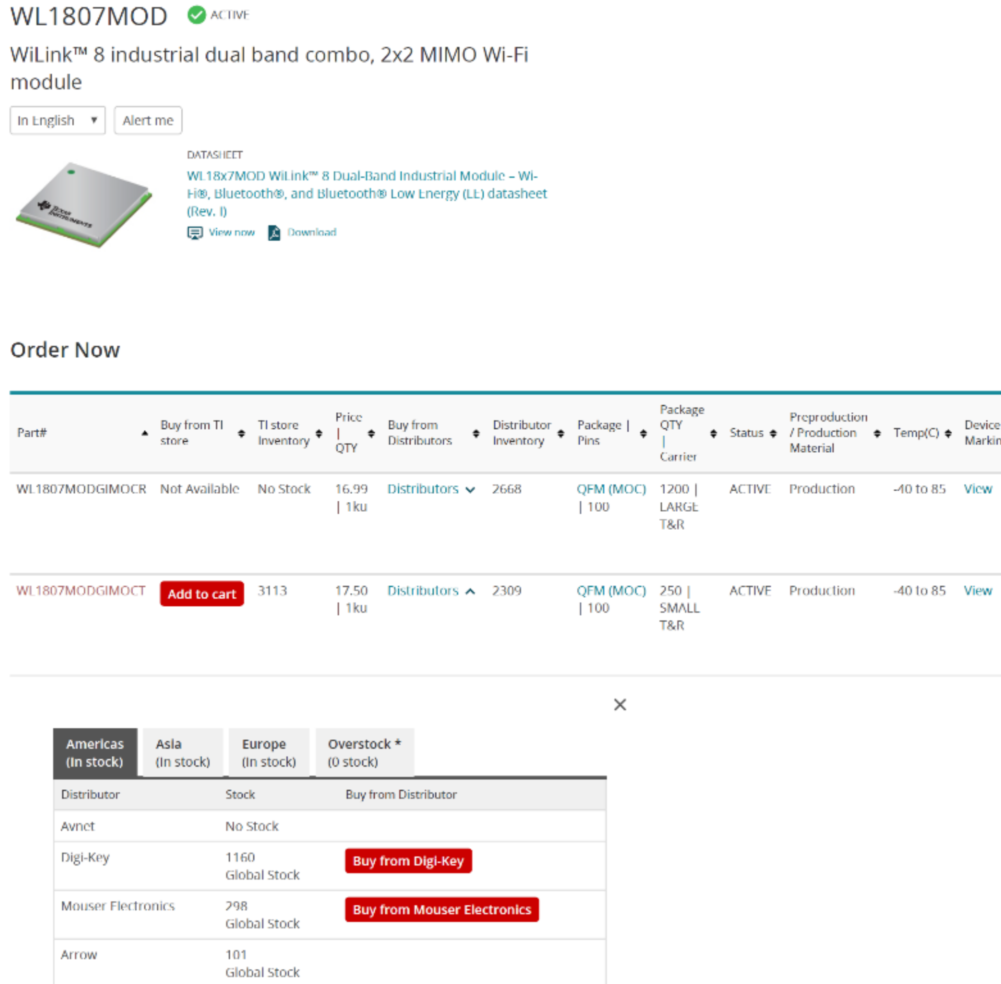




173. Claim 1 of the Gibson Patent applies to each Gibson Patent Accused Product at least because each of those products contain the same or similar copper interconnects as the TI WL1807MOD, and are manufactured using chemically amplified photoresists.

174. On information and belief, each of the Gibson Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

175. By way of example only, the TI WL1807MOD has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



WL1807MOD ACTIVE

WiLink™ 8 industrial dual band combo, 2x2 MIMO Wi-Fi module

In English | Alert me

DATASHEET

WL18x7MOD WiLink™ 8 Dual-Band Industrial Module – Wi-Fi®, Bluetooth®, and Bluetooth® Low Energy (LE) datasheet (Rev. I)

View now | Download

Order Now

Part#	Buy from TI store	TI store Inventory	Price | QTY	Buy from Distributors	Distributor Inventory	Package | Pins	Package QTY | Carrier	Status	Preproduction / Production Material	Temp(C)	Device Markin
WL1807MODGIMOCR	Not Available	No Stock	16.99 | 1ku	Distributors	2668	QFM (MOC) | 100	1200 | LARGE T&R	ACTIVE	Production	-40 to 85	View
WL1807MODGIMOCT	Add to cart	3113	17.50 | 1ku	Distributors	2309	QFM (MOC) | 100	250 | SMALL T&R	ACTIVE	Production	-40 to 85	View

Americas (In stock) | Asia (In stock) | Europe (In stock) | Overstock * (0 stock)

Distributor	Stock	Buy from Distributor
Avnet	No Stock	
Digi-Key	1160 Global Stock	Buy from Digi-Key
Mouser Electronics	298 Global Stock	Buy from Mouser Electronics
Arrow	101 Global Stock	

See https://www.ti.com/product/WL1807MOD/samplebuy (last visited January 31, 2020).

176. TI has known of the Gibson Patent's disclosure since no later than January 15, 2003, when U.S. patent examiner cited Gibson's disclosure to reject pending claims in TI's published U.S. patent application 2003/0170992A1, which TI ultimately abandoned. TI learned of Gibson's disclosure again in May 17, 2004, when a U.S. patent examiner cited Gibson's disclosure during prosecution of TI's application that issued as U.S. Patent No. 6,774,031. TI

learned of Gibson's disclosure again October 9, 2008, when a U.S. patent examiner cited Gibson's disclosure to reject pending claims in TI's published patent application 2008/0014739A1—and on January 9, 2009, TI submitted a response describing and citing Gibson's disclosure. TI ultimately abandoned the application. TI has been on notice of its infringement of the Gibson Patent by Bell Semic since at least January 10, 2020, when Bell Semic sent a letter identifying the WL1807MOD as infringing and exemplary of TI's infringement of the Gibson Patent. TI did not respond to this letter.

177. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Gibson Patent because Bell Semic provided TI with written notice of its infringement as detailed above.

178. TI, knowing its products infringe the Gibson Patent and with specific intent for others to infringe the Gibson Patent, have induced infringement of, and continue to induce infringement of, one or more claims of the Gibson Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, distributors, customers, end-users, and other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Gibson Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Gibson Accused Products in the United States. TI knows, and has known since at least January

10, 2020, that the Gibson Patent Accused Products infringe the Gibson Patent, and purposefully and knowingly sells and offers to sell the Gibson Patent Accused Products to its customers with the knowledge and expectation that the Gibson Patent Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors

179. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Gibson Accused Products and/or products incorporating the Gibson Accused Products in the United States by marketing the Gibson Accused Products in the United States; providing information such as detailed datasheets supporting use of the Gibson Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Gibson Accused Products; providing technical documentation for the Gibson Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Gibson Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Gibson Accused Products, including live training and video.

180. TI has contributed to the infringement of, and continue to contribute to the infringement of, one or more claims of the Gibson Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or

importing in or into the United States the Gibson Accused Products, which constitute a material part of the invention of the Gibson Patent, knowing the Gibson Accused Products to be especially made or especially adapted for use in infringement of the Gibson Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

181. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

182. TI's infringement of the Gibson Patent is and has been knowing, deliberate, willful. TI learned of its infringement of the Gibson Patent no later than January 10, 2020. As detailed above, Bell Semic sent a letter to TI January 10, 2020, identifying the Gibson Patent as being infringed by TI's exemplary WL1807MOD product. TI did not respond to the letter. Despite these efforts, and knowing that it was willfully infringing the Gibson Patent, TI continued and continuous to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Gibson Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Gibson Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 6

Willful Infringement of U.S. Patent No. 6,707,132 (Banerjee Patent)

183. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

184. The Banerjee Patent is generally related to methods for selectively improving carrier mobility in the surface channel of semiconductor devices, such as a semiconductor device wherein some parts of a circuit are disposed on Si—Ge regions and others are implemented in Silicon substrate regions of the chip. A method of making such a semiconductor device also is provided and includes steps of forming a thermal oxide layer on a Silicon substrate, masking at least a portion of the thermal oxide layer, removing at least a portion of the thermal oxide layer in order to expose a portion of the Silicon substrate, epitaxially growing a Si—Ge layer on the exposed portion of the Silicon substrate, and continuing manufacture of the device by forming a circuit on the Si—Ge regions and non-Si—Ge regions of the semiconductor device. (*See* Banerjee Patent, Abstract.)

185. The semiconductor industry is ever scaling transistors to smaller dimensions to reduce die size, increase logic functionality, and reduce power. However, this scaling has decreased drive currents, reducing performance and increasing dynamic power consumption of semiconductor devices. The drop in drive current results from a decrease in the mobility of carriers due to increased surface and impurity scattering in the surface channel of the semiconductor device. The formation of Si—Ge regions in silicon improves mobility of carriers of a semiconductor device. To that end, the Banerjee Patent teaches the formation of both Si-Ge regions and non-Si—Ge regions all on the same semiconductor chip. To do so, the Banerjee Patent teaches forming a Si—Ge region through the masking and subsequent removal of a

portion of the thermal oxide layer disposed over a silicon substrate, wherein a Si—Ge layer is epitaxially grown or deposited.

186. The Banerjee Patent contains 2 independent claims and 18 total claims, covering various semiconductor devices and methods. Claim 5 reads:

> A method of making a semiconductor device comprising:
>
> providing a Silicon substrate; and
>
> depositing Si—Ge on the Silicon substrate;
>
> further comprising forming a thermal oxide layer on the Silicon substrate;
>
> further comprising masking at least a portion of the thermal oxide layer which is disposed on the Silicon substrates;
>
> further comprising removing at least a portion of the thermal oxide layer which is disposed on the Silicon substrate in order to expose a portion of the Silicon substrate;
>
> further comprising forming a Si—Ge layer on the exposed portion of the Silicon substrate.

187. TI has directly infringed, and continues to directly infringe, one or more claims of the Banerjee Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Banerjee Patent, and/or TI has directly infringed, and continues to directly infringe, one or more claims of the Banerjee Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products made by a process using one or more claims of the Banerjee Patent (*e.g.*, claims 5, 12, and 14). Such products manufactured using these infringing methods include, but are not limited to:

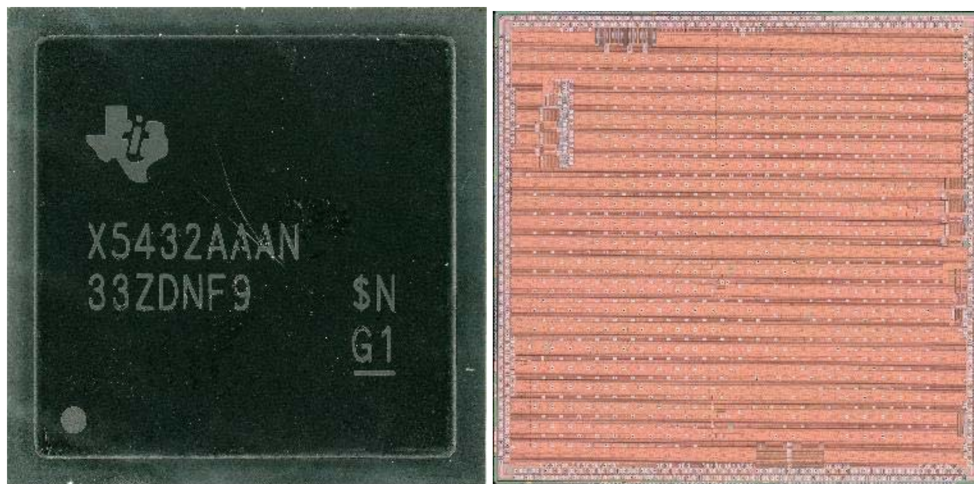
- TI products containing circuits or circuit elements on both Si—Ge regions and non-Si—Ge regions;

- TI's OMAP5432 high-performance multimedia application device designed to provide best-in-class CPU performance, video, image, and graphics processing; and
- TI's devices that are variants of the above-identified products or that are manufactured using the same or similar processes;

(collectively "Banerjee Accused Products").

188. By way of non-limiting example only, the process of manufacturing the TI OMAP5432 meets all the steps of claim 5 of the Banerjee Patent including: (1) providing a Silicon substrate; and (2) depositing Si—Ge on the Silicon Substrate, including the steps of (i) forming a thermal oxide layer on the Silicon substrate; (ii) masking at least a portion of the thermal oxide layer which is disposed on the Silicon substrate; (iii) further comprising removing at least a portion of the thermal oxide layer which is disposed on the Silicon substrate in order to expose a portion of the Silicon substrate; and (iv) forming a Si—Ge layer on the exposed portion of the Silicon Substrate.

189. The TI OMAP5432 (part no. X5432AAAN) is a semiconductor device:



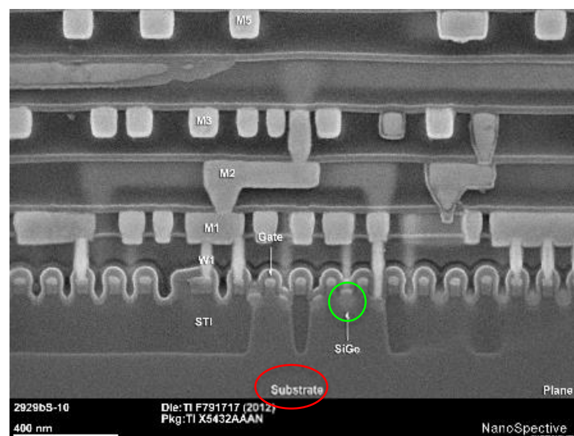
190. The TI OMAP5432 is manufactured on a 28-nm technology Node:

OMAP5432 ES2.0 Processor

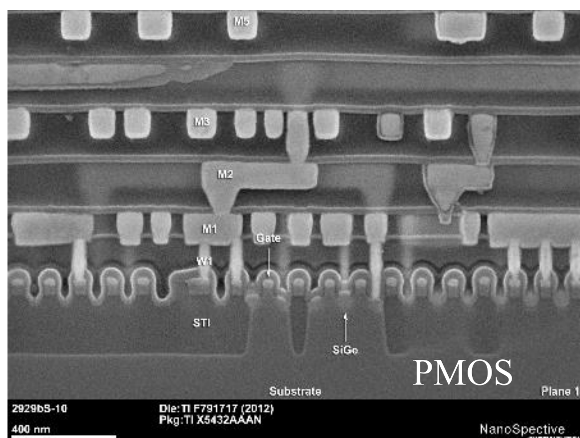
The heart of OMAP5432 EVM is the OMAP5432 ES2.0 processor. The OMAP5432 high-performance multimedia application device is based on enhanced OMAP™ architecture and uses 28-nm technology. The architecture is designed to provide best-in-class CPU performance, video, image, and graphics processing.

See http://www.ti.com/lit/ug/swcu130/swcu130.pdf at pg. 14 (last visited February 5, 2020). *See also* https://www.eetimes.com/upset-ti-slams-samsungs-foundry-efforts/ (last visited February 5, 2020).

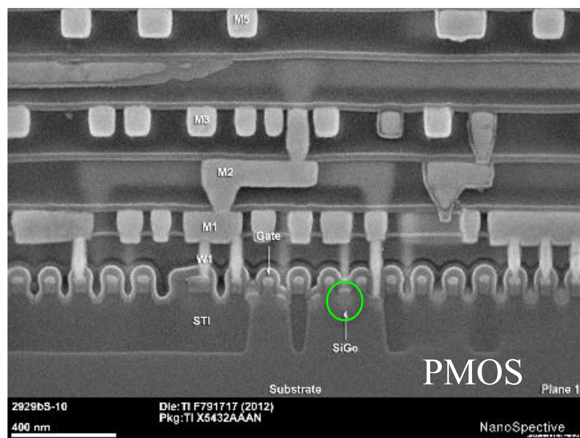
191. The TI OMAP5432 is manufactured to include a Silicon substrate (red circle) and Si-Ge deposited on the Silicon Substrate (green circle shows one of many areas with Si-Ge deposited):



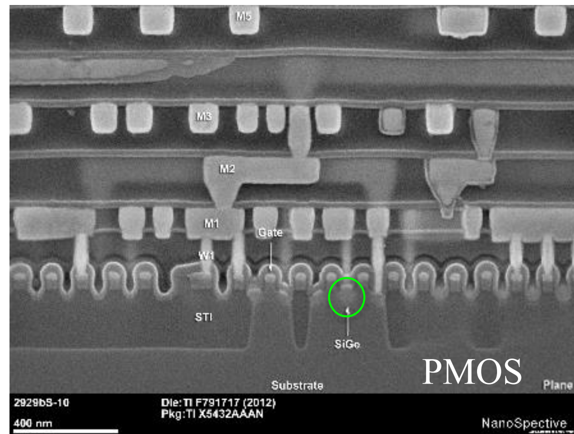
192. The TI OMAP5432 is further manufactured to include a thermal oxide layer (the gate oxide) across the Silicon substrate, including the source and drain areas of the p-channel metal-oxide-semiconductor (PMOS) transistors:



193. During manufacture of the TI OMAP5432, a portion of the thermal oxide layer over the TI OMAP5432's transistors were masked and then removed, including over PMOS source and drain Silicon regions (green circle):



194. Subsequently, a Si—Ge region is formed in the exposed portion of the PMOS source and drain Silicon region (green circle):



195. Claim 5 of the Banerjee Patent applies to each Banerjee Accused Product at least because each of those products are manufactured on the same or similar technology node as the TI OMAP5423 or are manufactured on other technology nodes that contain circuits or circuit elements on both Si—Ge regions and non-Si—Ge regions.

196. On information and belief, each of the Banerjee Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

197. TI has known of the Banerjee Patent since at least February 28, 2005. On February 28, 2005 during the prosecution of TI's patent application 10/691,843 (which issued as U.S. Patent No. 6,917,903), the Patent Examiner cited the Banerjee Patent in a Notice of References Cited. On this same day, the Patent Examiner conducted an interview to discuss the prior art cited, and issued reasons for allowance citing and discussing the Banerjee Patent. On June 3, 2005, TI filed Comments on the Examiner's Reasons for Allowance, and specifically discussed the details of the Banerjee Patent's disclosure.

198. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Banerjee Patent at least because Bell Semic provided TI with written notice of its infringement as of the filing of the original Complaint on February 21, 2020.

199. TI, knowing that the process of manufacturing its Accused Banerjee Products infringes the Banerjee Patent and with specific intent for others to infringe the Banerjee Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Banerjee Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others (1) actively inducing others to make in the United States without authorization the Banerjee Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Banerjee Accused Product, as well as products incorporating the same.

200. TI knows, and has known since at least February 28, 2005, that the process of manufacturing the Banerjee Accused Products infringes the Banerjee Patent. Despite this knowledge, TI knowingly and intentionally instructed, and continues to instruct, its OEMs and foundry suppliers to infringe the Banerjee Patent through the unlicensed manufacture of the Banerjee Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States market. TI further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Banerjee Patent by its customers', distributors', and/or other third parties' sale and distribution of the Banerjee Accused Products with the expectation that such products, and/or products incorporating the same, will be used, sold, offered for sale, and/or imported in or into the United States. TI further knowing and intentionally aided and abetted, and continues to aid and abet, infringement of the Banerjee Patent through the use, sale, offers for sale, and/or importation in or into the United States of the

Banerjee Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website.

201. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Banerjee Accused Products and/or products incorporating the Banerjee Accused Products in the United States by marketing the Banerjee Accused Products in the United States; providing information such as detailed datasheets supporting use of the Banerjee Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Banerjee Accused Products; providing technical documentation for the Banerjee Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Banerjee Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Banerjee Accused Products, including live training and video.

202. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

203. TI's infringement of the Banerjee Patent is and has been knowing, deliberate, and willful. TI learned of the Banerjee Patent no later than February 28, 2005. However, despite

knowing that it was willfully infringing the Banerjee Patent, TI continued, and continues, to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Banerjee Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Banerjee Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 7

Willful Infringement of U.S. Patent No. 6,544,907 (Ma Patent)

204. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

205. The Ma Patent is generally related to methods for manufacturing a high-quality gate oxide layer having a uniform thickness, including providing a semiconductor substrate, and forming an oxide layer having a substantially uniform thickness on the semiconductor substrate, and in a zone of pressure of less than about 4 Torr or greater than about 25 Torr. (*See* Ma Patent, Abstract.)

206. During the manufacture of metal-oxide-semiconductor transistors, a gate oxide layer is formed. The thickness and uniformity of the gate oxide layer can significantly impact the overall operation of the device being formed. As transistors have shrunk in size, the thickness of the gate oxide has correspondingly shrunk. And, as the thickness has continued to decrease, the thickness uniformity of the gate oxide layer becomes increasingly important. Prior to the Ma Patent, gate oxide layer manufacturing was performed at pressures ranging from 10 Torr to about

15 Torr, however, forming gate oxides within such pressure ranges produces very non-uniform gate oxides. The Ma Patent provided a solution to these non-uniform gate oxides by teaching the formation of gate oxide layers at pressures of less than about 4 Torr or greater than about 25 Torr, which can be used to form a substantially uniform gate oxide layer, such as one that has a thickness that varies by less than about 0.2 nm.

207. The Ma Patent contains 4 independent claims and 17 total claims, covering various semiconductor devices and methods. Claim 1 reads:

> A method for manufacturing a high quality oxide layer having a uniform thickness, comprising:
>
> providing a semiconductor substrate, and
>
> forming a gate oxide layer having a substantially uniform thickness on the semiconductor substrate, the gate oxide layer having a range of thicknesses that varies by less than about 0.2 nm.

208. TI has directly infringed, and continues to directly infringe, one or more claims of the Ma Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Ma Patent, and/or TI has directly infringed, and continues to directly infringe, one or more claims of the Ma Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Ma Patent (*e.g.*, claims 1, 2, 7, 9, 14, and 15). Such products manufactured using these infringing methods include, but are not limited to:

- TI products with a high quality oxide layer having a substantially uniform thickness,
- TI's AWR1642 integrated single-chip automotive radar sensor using TI's mmWave sensor technology intended as a complete platform solution for the automotive space;

- TI's DM3725CUS digital media processor intended to provide ARM and graphics performance with low power consumption for applications including portable data terminals, navigation, auto infotainment, gaming, medical imaging, home automation, human interface, industrial control, test and measurement, and single board computers;
- TI's WL1807MOD WiLink 8 module with high throughput and extended range along with Wi-Fi and Bluetooth coexistence for applications including the internet of things (IoT), multimedia, home electronics, home appliances and white goods, industrial and home automation, smart gateway and metering, video conferencing video camera and security;
- TI's Hercules RM48L952 16/32-Bit RISC flash microcontroller intended for industrial safety applications such as industrial automation, safe PLCs, power generations and distribution, windmills and turbines, and elevators and escalators and medical applications such as ventilators, defibrillators, infusion and insulin pumps, radiation therapy, and robotic surgery;
- TI's TM4C123GH6PGEI 32-bit ARM® Cortex®-M4F based microcontroller intended for developers of a range of industrial applications including remote monitoring, electronic point-of-sale machines, test and measurement equipment, network appliances and switches, factory automation, HVAC and building control, gaming equipment, motion control, transportation, and fire and security,
- TI's TLK10034AAJ quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems;

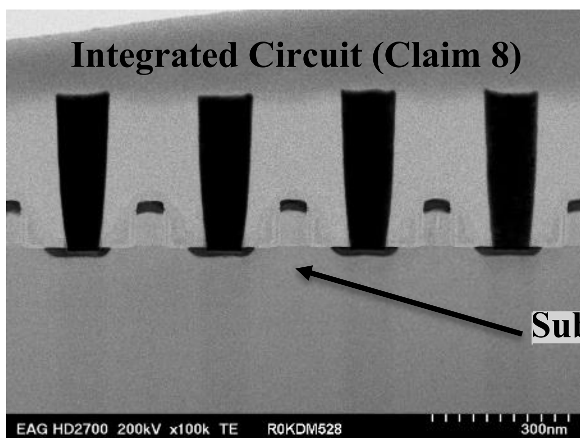
- TI's AWR1443FQIGABYA60E integrated single-chip automotive radar sensor using TI's mmWave sensor technology used as a radar system for the automotive space;
- TI's IWR1642AQAGABLR integrated single-chip industrial radar sensor using TI's mmWave sensor technology used as a radar system for use in industrial applications such as building automation, factory automation, drones, material handling, traffic monitoring, and surveillance; and
- TI's devices that are variants of the above-identified products;

(collectively "Ma Accused Products").

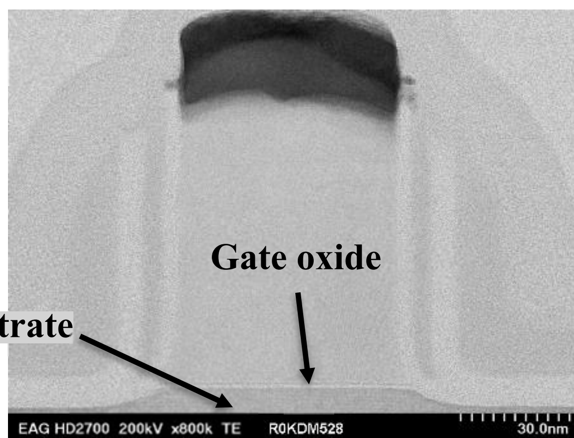
209. By way of non-limiting example only, the process of manufacturing the TI RM48L952 meets all the steps of claim 1 of the Ma Patent including forming a gate oxide layer having a substantially uniform thickness on the semiconductor substrate, wherein the gate oxide layer has a range of thicknesses that varies by less than about 0.2 nm.

210. As shown below, the TI RM48L952 is a semiconductor device:

211. The TI RM48L952 is manufactured to have a gate oxide layer formed that has a substantially uniform thickness on a semiconductor substrate:

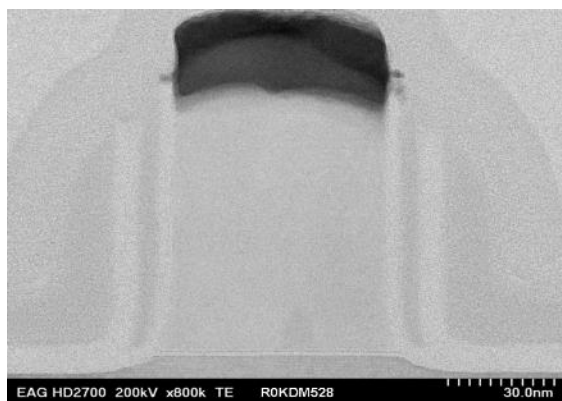


RM48L952DZWTT

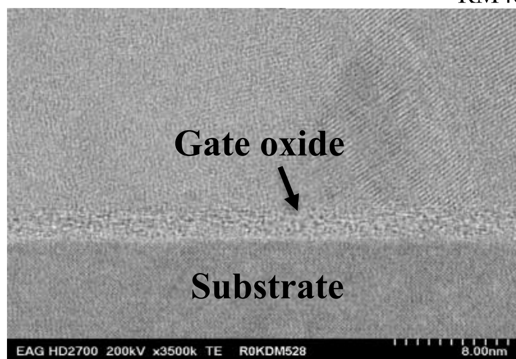


RM48L952DZWTT

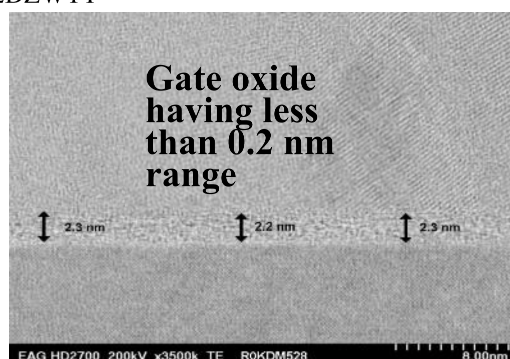
212. As shown below, the TI RM48L952 has a substantially uniform thickness that varies less than 0.2 nm:



RM48L952DZWTT



RM48L952DZWTT



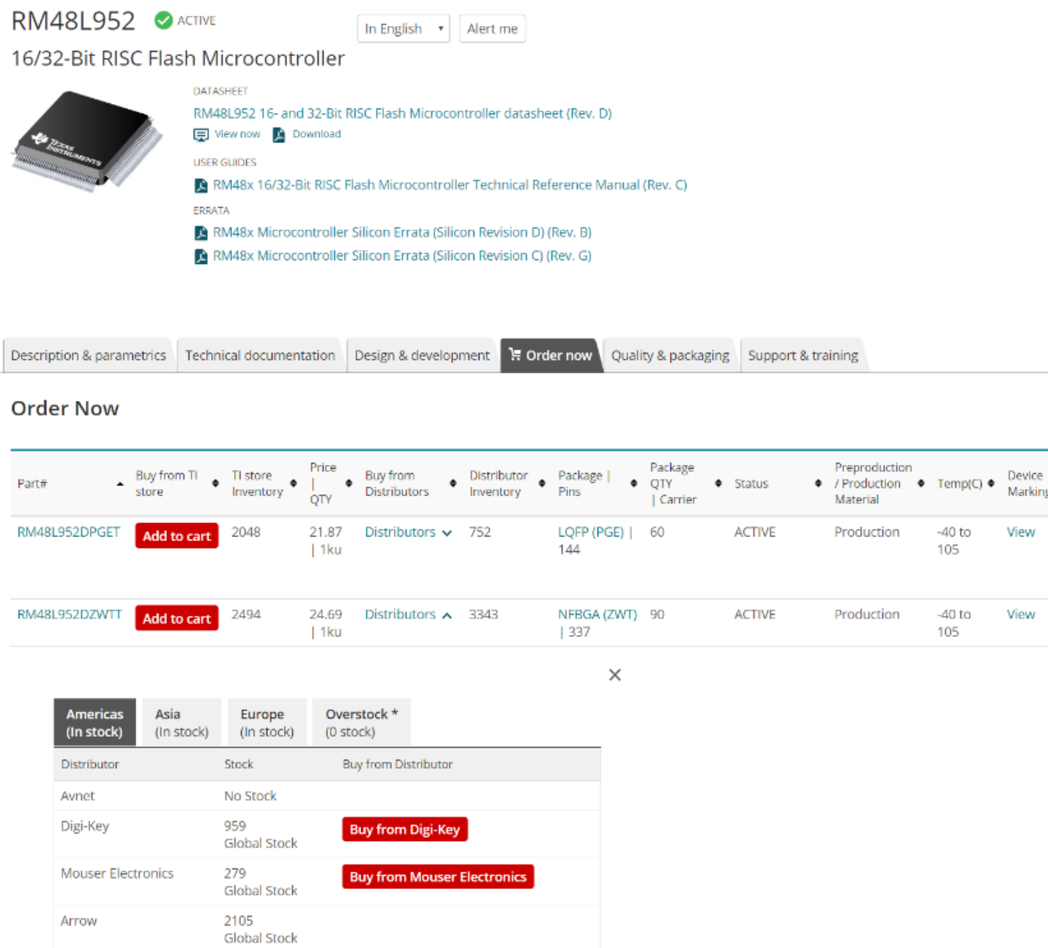
RM48L952DZWTT

213. Claim 1 of the Ma Patent applies to each Ma Accused Product at least because each of those products are manufactured on the same technology nodes (Technology Nodes 65

nm through 40 nm) as the above-identified products or other technology nodes using similar processes.

214. On information and belief, each of the Ma Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

215. By way of example only, the TI RM48L952 has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



See http://www.ti.com/product/RM48L952/samplebuy (last visited February 4, 2020).

216. TI has known of the Ma Patent and has been on notice of its infringement of the Ma Patent since at least January 10, 2020, when Bell Semic sent a letter to TI identifying the RM48L952, WL1807MOD, AWR1642, TM4C123GH6PGEI, TLK10034AAJ, DM3725CUS, AWR1443FQIGABLQ, and IWR1642AQAGABLR as infringing the Ma Patent. TI did not respond to this letter.

217. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Ma Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

218. TI, knowing that the process of manufacturing its Accused Ma Products infringes the Ma Patent and with specific intent for others to infringe the Ma Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Ma Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Ma Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Ma Accused Products, and products incorporating same.

219. TI knows, and has known since at least January 10, 2020, that the process of manufacturing the Ma Accused Products infringes the Ma Patent. Despite this knowledge, TI knowingly and intentionally instructed, and continues to instruct, its OEMs, package assemblers, and foundry suppliers to infringe the Ma Patent through the unlicensed manufacture and assembly of the Ma Accused Products with the expectation that such products will be used, sold, offered for sale, and/or imported in or into the United States. TI further knowingly and intentionally aided and abetted, and continues to aid and abet, infringement of the Ma Patent by its customers', distributors', and/or other third parties' sale and distribution of the Ma Accused

Products with the expectation that such products, and/or products incorporating the same, will be imported into the United States market where they will be used, sold, and/or offered for sale. TI further knowing and intentionally aided and abetted, and continues to aid and abet, infringement of the Ma Patent through the use, sale, offers for sale, and/or importation in or into the United States the Ma Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website.

220. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Ma Accused Products and/or products incorporating the Ma Accused Products in the United States by marketing the Ma Accused Products in the United States; providing information such as detailed datasheets supporting use of the Ma Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Ma Accused Products; providing technical documentation for the Ma Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Ma Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Ma Accused Products, including live training and video.

221. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement of the Ma Patent, in an amount adequate to compensate for TI's

infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

222. TI's infringement of the Ma Patent is and has been knowing, deliberate, and willful. TI learned of its infringement of the Ma Patent no later than January 10, 2020. As detailed above, Bell Semic sent a letter to TI on January 10, 2020, identifying the Ma Patent as being infringed by several TI products. TI did not respond to the letter. Despite these efforts, and knowing that it was willfully infringing the Ma Patent, TI continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Ma Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Ma Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 8
Willful Infringement of U.S. Patent No. 6,492,712 (Chen)

223. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

224. The Chen Patent is generally related to an oxide for use in integrated circuits that is substantially stress-free both in the bulk and at the interface between the substrate and the oxide. The interface is planar and has a low interface trap density. The oxide has a low defect density and may have a thickness of less than 1.5 nm or less. (*See* Chen Patent, Abstract.)

225. During the manufacture of metal-oxide-semiconductor transistors, an oxide layer is formed. As the size of the devices within an integrated circuit decrease, the various elements of such devices, including the oxide layer, must also be reduced proportionally. As these oxide layers are made thinner, the oxide quality degrades and the reliability of the dielectric material may be affected by oxide stress and the planarity of the oxide-substrate interface. Resulting problems, such as device parameter drift and time dependent dielectric breakdown, can cause the device to fail. The Chen Patent provides a solution to reduce these issues by teaching an oxide layer with two portions, resulting in improved interfacial planarity and a reduction in the stress in the oxide and the interface between the oxide and the substrate.

226. The Chen Patent contains 4 independent claims and 15 total claims, covering various integrated circuit elements. Claim 15 reads:

> An integrated circuit element, comprising:
>
> a substrate;
>
> an oxide layer having a first portion and a second portion disposed over said substrate, said first portion being disposed over said second portion, wherein said oxide layer has a thickness of 2.5 nm or less, and wherein said substrate and said oxide layer form an interface and said interface has a surface roughness of 3 Å or less.

227. TI has directly infringed, and continues to directly infringe, one or more claims of the Chen Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Chen Patent (*e.g.*, claims 12-15) including, but not limited to:

- TI products with a low defect density oxide and a thickness of 2.5 nm or less;

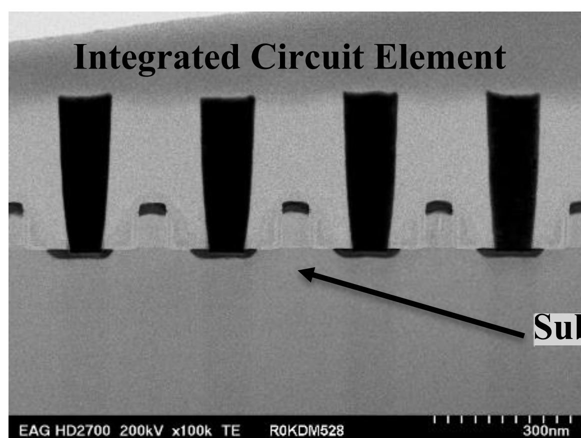
- TI's AWR1642 integrated single-chip automotive radar sensor using TI's mmWave sensor technology intended as a complete platform solution for the automotive space;
- TI's DM3725CUS digital media processor with low power consumption for applications including portable data terminals, navigation, auto infotainment, gaming, medical imaging, home automation, human interface, industrial control, test and measurement, and single board computers;
- TI's WL1807MOD WiLink 8 module with high throughput and extended range along with Wi-Fi and Bluetooth coexistence for applications including the internet of things (IoT), multimedia, home electronics, home appliances and white goods, industrial and home automation, smart gateway and metering, video conferencing video camera and security;
- TI's Hercules RM48L952 16/32-Bit RISC flash microcontroller intended for industrial safety applications such as industrial automation, safe PLCs, power generations and distribution, windmills and turbines, and elevators and escalators and medical applications such as ventilators, defibrillators, infusion and insulin pumps, radiation therapy, and robotic surgery;
- TI's TM4C123GH6PGEI 32-bit ARM® Cortex®-M4F based microcontroller intended for developers of a range of industrial applications including remote monitoring, electronic point-of-sale machines, test and measurement equipment, network appliances and switches, factory automation, HVAC and building control, gaming equipment, motion control, transportation, and fire and security,
- TI's TLK10034AAJ quad-channel multi-rate transceiver intended for use in high-speed bi-directional point-to-point data transmission systems;

- TI's AWR1443FQIGABYA60E integrated single-chip automotive radar sensor using TI's mmWave sensor technology use as a radar system for the automotive space;
- TI's IWR1642AQAGABLR integrated single-chip industrial radar sensor using TI's mmWave sensor technology used as a radar system in industrial applications such as building automation, factory automation, drones, material handling, traffic monitoring, and surveillance; and
- TI's devices that are variants of the above-identified products;

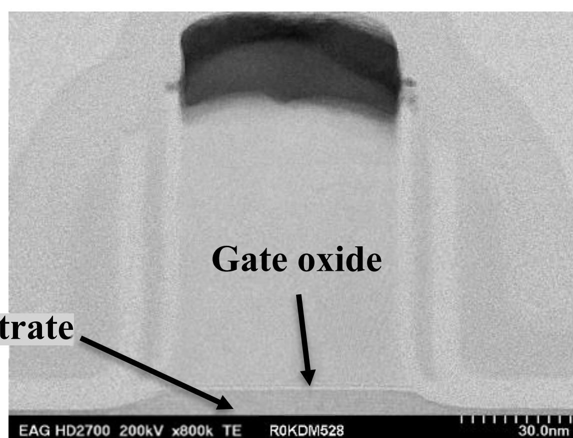
(collectively "Chen Accused Products").

228. By way of example only, the RM48L952 infringes claim 15 of the Chen Patent and has an integrated circuit element comprising a substrate and an oxide layer having a first portion and a second portion disposed over the substrate, where (1) the first portion is disposed over the second portion, (2) the oxide layer has a thickness of 2.5 nm or less, and (3) the substrate and oxide layer form an interface with a surface roughness of 3 Å or less.

229. As shown below, the TI RM48L952 has an integrated circuit element comprising a substrate and an oxide layer:

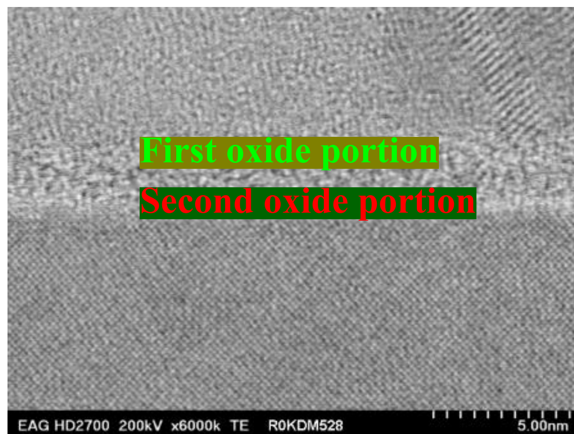


RM48L952DZWTT



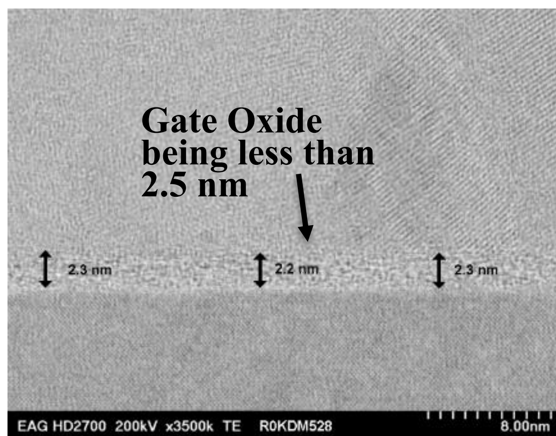
RM48L952DZWTT

230. The oxide layer of the TI RM48L952 has a first portion disposed over the second portion:



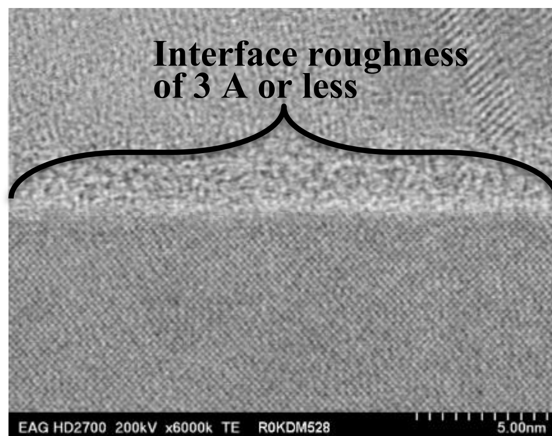
RM48L952DZWTT

231. The oxide layer of the TI RM48L952 has a thickness of 2.5 nm or less:



RM48L952DZWTT

232. The substrate and oxide layer form an interface where the interface has, on information and belief, a surface roughness of 3 Å or less:



RM48L952DZWTT

233. Claim 15 of the Chen Patent applies to each Chen Accused Product at least because each of those products are manufactured on the same technology nodes (Technology Nodes 65-nm through 40-nm) as the above-identified products or other technology nodes using similar processes.

234. On information and belief, each of the Chen Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

235. By way of example only, the RM48L952 has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:

RM48L952 ACTIVE

In English | Alert me

16/32-Bit RISC Flash Microcontroller

DATASHEET

RM48L952 16- and 32-Bit RISC Flash Microcontroller datasheet (Rev. D)

View now | Download

USER GUIDES

RM48x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual (Rev. C)

ERRATA

RM48x Microcontroller Silicon Errata (Silicon Revision D) (Rev. B)

RM48x Microcontroller Silicon Errata (Silicon Revision C) (Rev. G)

Description & parametrics | Technical documentation | Design & development | Order now | Quality & packaging | Support & training

Order Now

Part#	Buy from TI store	TI store Inventory	Price | QTY	Buy from Distributors	Distributor Inventory	Package | Pins	Package QTY | Carrier	Status	Preproduction / Production Material	Temp(C)	Device Marking
RM48L952DPGET	Add to cart	2048	21.87 | 1ku	Distributors	752	LQFP (PGE) | 144	60	ACTIVE	Production	-40 to 105	View
RM48L952DZWTT	Add to cart	2494	24.69 | 1ku	Distributors	3343	NFBGA (ZWT) | 337	90	ACTIVE	Production	-40 to 105	View

Americas (In stock) | Asia (In stock) | Europe (In stock) | Overstock * (0 stock)

Distributor	Stock	Buy from Distributor
Avnet	No Stock	
Digi-Key	959 Global Stock	Buy from Digi-Key
Mouser Electronics	279 Global Stock	Buy from Mouser Electronics
Arrow	2105 Global Stock	

See http://www.ti.com/product/RM48L952/samplebuy (last visited February 4, 2020).

236. TI has known of the Chen Patent and has been on notice of its infringement of the Chen Patent since at least January 10, 2020, when Bell Semic sent a letter to TI identifying the RM48L952, WL1807MOD, AWR1642, TM4C123GH6PGEI, TLK10034AAJ, DM3725CUS, AWR1443FQIGABLQ, and IWR1642AQAGABLR as infringing the Chen Patent. TI did not respond to this letter.

237. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Chen Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

238. TI, knowing its products infringe the Chen Patent and with specific intent for others to infringe the Chen Patent, have induced infringement of, and continue to induce infringement of, one or more claims of the Chen Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its customers, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Chen Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Chen Accused Products in the United States. TI knows, and has known since at least January 10, 2020, that the Chen Accused Products infringe the Chen Patent, and purposefully and knowingly sells and offers to sell the Chen Accused Products to its customers with the knowledge and expectation that the Chen Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors

239. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Chen Accused Products and/or products incorporating the Chen Accused Products in the United States by marketing the Chen Accused

Products in the United States; providing information such as detailed datasheets supporting use of the Chen Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Chen Accused Products; providing technical documentation for the Chen Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Chen Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Chen Accused Products, including live training and video.

240. TI's infringement of the Chen Patent is and has been knowing, deliberate, and willful. TI learned of its infringement of the Chen Patent no later than January 10, 2020, when Bell Semic sent a letter to TI identifying the Chen Patent as being infringed by several TI products. TI did not respond to the letter. Despite these efforts, and knowing that it was willfully infringing the Chen Patent, TI continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Chen Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Chen Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 9

Willful Infringement of U.S. Patent No. 7,319,272 (Ramakrishnan Patent)

241. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

242. The Ramakrishnan Patent is generally related to a pattern of contacts that includes high speed transmitter contacts disposed in differential pairs in a first portion of the pattern, high speed receiver contacts disposed in differential pairs in a second portion of the pattern, and at least one unbroken line of other contacts disposed between the first and second portions of the pattern. Low speed IO contacts are disposed in a third portion of the pattern in an interior portion of the pattern relative to the first and second portions. Substantially all of the contacts are disposed at a first pitch from another on a single contact surface. (*See* Ramakrishnan Patent, Abstract.)

243. To ensure performance of high-speed integrated circuits, isolation of transmitter and receiver pairs of high-speed signals, and between high-speed signals and other signals, in integrated circuits, package substrate, and circuit board are critical factors to consider. It is advantageous to route integrated circuits so that high-speed signals are adequately isolated in the package substrate and also in the printed circuit board. Additionally, routing of high-speed signals in the lowest possible number of printed circuit board layers reduces the overall cost of the system. By configuring the contact pattern, as taught by the Ramakrishnan Patent, better separation between the high-speed transmitter contacts and the high-speed receiver contacts is achieved, and the high-speed signals are more easily routed out of the pattern.

244. The Ramakrishnan Patent contains 3 independent claims and 20 total claims, covering various integrated circuit package substrates. Claim 17 reads:

A package substrate having a pattern of contacts comprising:

> high speed transmitter contacts disposed in a first portion of the pattern, where the high speed transmitter contacts are disposed in transmitter differential pairs,
>
> high speed receiver contacts disposed in a second portion of the pattern, where the first portion of the pattern is not interspersed with the second portion of the pattern, and the high speed receiver contacts are disposed in receiver differential pairs,
>
> at least one unbroken line of other contacts disposed between the first portion of the pattern and the second portion of the pattern, where the other contacts do not contain any high speed transmitter contacts and high speed receiver contacts, and
>
> low speed IO contacts disposed in a third portion of the pattern, where a part of the third portion of the pattern is disposed in an interior portion of the pattern relative to both the first portion of the pattern and the second portion of the pattern,
>
> where substantially all of the contacts are disposed at a first pitch from one another on a single contact surface.

245. TI has directly infringed, and continues to directly infringe, one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Ramakrishnan Patent (*e.g.*, claims 1-4 and 17-19), including, but not limited to:

- TI products that have transmitter and receiver contacts in differential pairs with an unbroken line of other contacts between them, and I/O contacts in the interior portion of the contacts relative to the transmitter and receiver contacts;
- TI's DS280DF810, a 28 Gbps multi-rate 8-channel retimer;
- TI's DS110DF1610, an 8.5 to 11.3 Gbps 16-channel retimer;
- TI's DS125DF1610, a 9.8 to 12.5 Gbps 16-channel retimer;
- TI's DS150DF1610, a 12.5 to 15 Gbps 16-channel retimer;
- TI's DS250DF230, a 25 Gbps multi-rate 2-channel retimer;
- TI's DS250DF410, a 25 Gbps multi-rate 4-channel retimer;

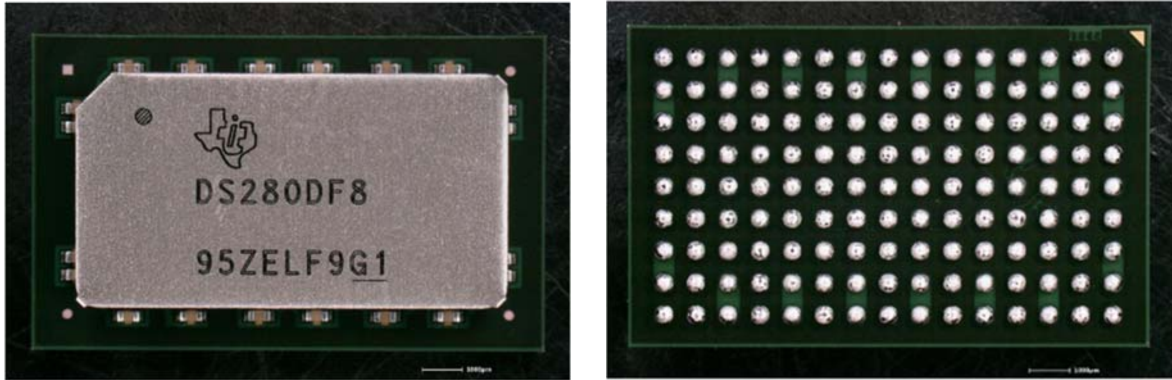
- TI's DS250DF810, a 25 Gbps multi-rate 8-channel retimer;
- TI's DS280MB810, a 28 Gbps 8-channel linear repeater;
- TI's DS280BR810, a 28 Gbps 8-channel linear repeater;
- TI's DS280BR820, a 28 Gbps 8-channel linear repeater;
- TI's ADC08DJ3200, a 6.4 GSPS single-channel or 3.2 GSPS dual-channel analog-to-digital converter;
- TI's ADC09QJ1300-Q1, a 1.3 GSPS quad-channel analog-to-digital converter;
- TI's ADC12DJ2700, a 5.4 GSPS single-channel or 2.7 GSPS dual-channel analog-to-digital converter;
- TI's ADC12DJ3200, a 6.4 GSPS single-channel or 3.2 GSPS dual-channel analog-to-digital converter;
- TI's ADC12DJ5200RF, a 10.4 GSPS single-channel or 5.2 GSPS dual-channel analog-to-digital converter;
- TI's ADC12DL3200, a 6.4 GSPS single-channel or 3.2 GSPS dual-channel analog-to-digital converter;
- TI's ADC12QJ1600-Q1, a 1.6 GSPS quad-channel analog-to-digital converter;
- TI's DAC37J82, a 1.6 GSPS dual-channel digital-to-analog converter;
- TI's DAC38J82, a 2.5 GSPS dual-channel digital-to-analog converter;
- TI's DAC37J84, a 1.6 GSPS dual-channel digital-to-analog converter;
- TI's DAC38J84, a 2.5 GSPS dual-channel digital-to-analog converter;
- TI's DAC38RF82, a 9 GSPS dual-channel digital-to-analog converter;
- TI's DAC38RF89, a 9 GSPS dual-channel digital-to-analog converter;
- TI's DAC38RF83, a 9 GSPS dual-channel digital-to-analog converter;

- TI's DAC38RF93, a 9 GSPS dual-channel digital-to-analog converter;
- TI's DAC38RF85, a 9 GSPS dual-channel digital-to-analog converter;
- TI's DAC39J82, a 2.8 GSPS dual-channel digital-to-analog converter;
- TI's DAC39J84, a 2.8 GSPS quad-channel digital-to-analog converter; and
- TI's devices that are variants of the above-identified products;

(collectively, the "Ramakrishnan Accused Products").

246. By way of non-limiting example only, TI's DS280DF810 infringes claim 17 of the Ramakrishnan Patent because it is an integrated circuit with a package substrate having a pattern of contacts that has (1) high-speed transmitter contacts disposed in a first portion of the pattern that are disposed in transmitter differential pairs; (2) high-speed receiver contacts disposed in a second portion of the pattern where the first portion of the pattern is not interspersed with the second portion of the pattern and the high-speed receiver contacts are disposed in receiver differential pairs; (3) an unbroken line of other contacts disposed between the first and second portions of the pattern, where the other contacts do not contain any highspeed transmitter contacts and high-speed receiver contacts; and (4) low speed IO contacts disposed in a third portion of the pattern that has a part of it disposed in an interior portion of the pattern relative to both the first and second portions of the pattern. Substantially all of the contacts in the TI DS280DF810 are also disposed at a first pitch one from another on a single contact surface.

247. As shown below, TI's DS280DF810 is an integrated circuit with a package substrate having a pattern of contacts.



248. The data sheet for the TI DS280DF810 provides a top view of the pinout:

135-pin fcBGA, 0.8 mm BGA pin pitch
Top View

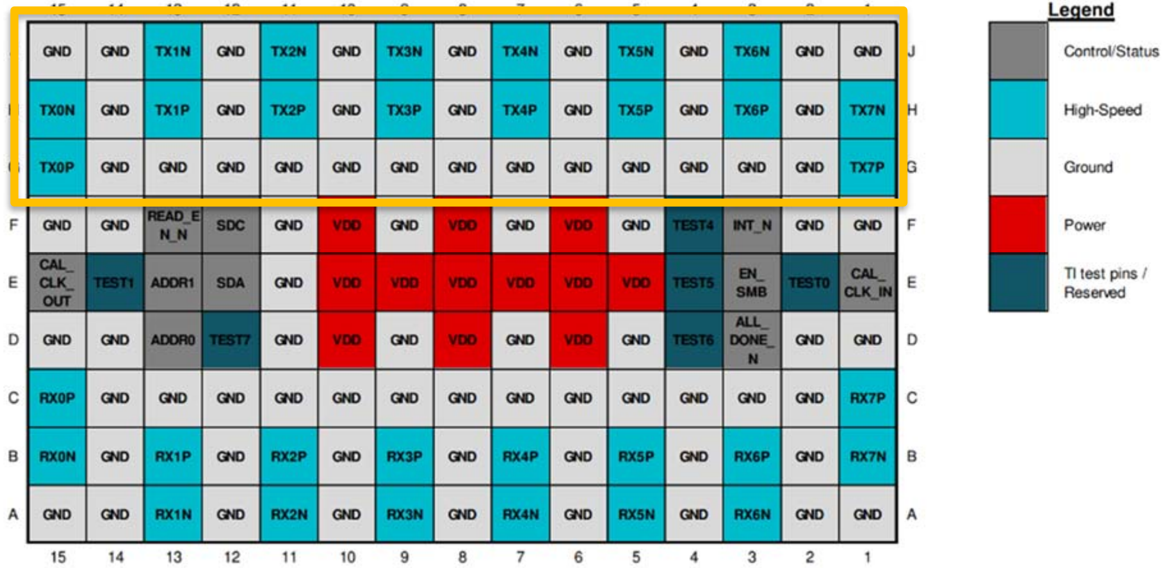
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
J	GND	GND	TX1N	GND	TX2N	GND	TX3N	GND	TX4N	GND	TX5N	GND	TX6N	GND	GND	J
H	TX0N	GND	TX1P	GND	TX2P	GND	TX3P	GND	TX4P	GND	TX5P	GND	TX6P	GND	TX7N	H
G	TX0P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TX7P	G
F	GND	GND	READ_EN_N	SDC	GND	VDD	GND	VDD	GND	VDD	GND	TEST4	INT_N	GND	GND	F
E	CAL_CLK_OUT	TEST1	ADDR1	SDA	GND	VDD	VDD	VDD	VDD	VDD	VDD	TEST5	EN_SMB	TEST0	CAL_CLK_IN	E
D	GND	GND	ADDR0	TEST7	GND	VDD	GND	VDD	GND	VDD	GND	TEST6	ALL_DONE_N	GND	GND	D
C	RX0P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RX7P	C
B	RX0N	GND	RX1P	GND	RX2P	GND	RX3P	GND	RX4P	GND	RX5P	GND	RX6P	GND	RX7N	B
A	GND	GND	RX1N	GND	RX2N	GND	RX3N	GND	RX4N	GND	RX5N	GND	RX6N	GND	GND	A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Legend

- Control/Status
- High-Speed
- Ground
- Power
- TI test pins / Reserved

249. The TI DS280DF810 has high speed transmitter contacts disposed in a first portion (circled in orange below) of the pattern of contacts, where the high speed transmitter contacts are disposed in transmitter differential pairs (TX0P-TX0N, TX1P-TX1N, etc.).

135-pin fcBGA, 0.8 mm BGA pin pitch
Top View

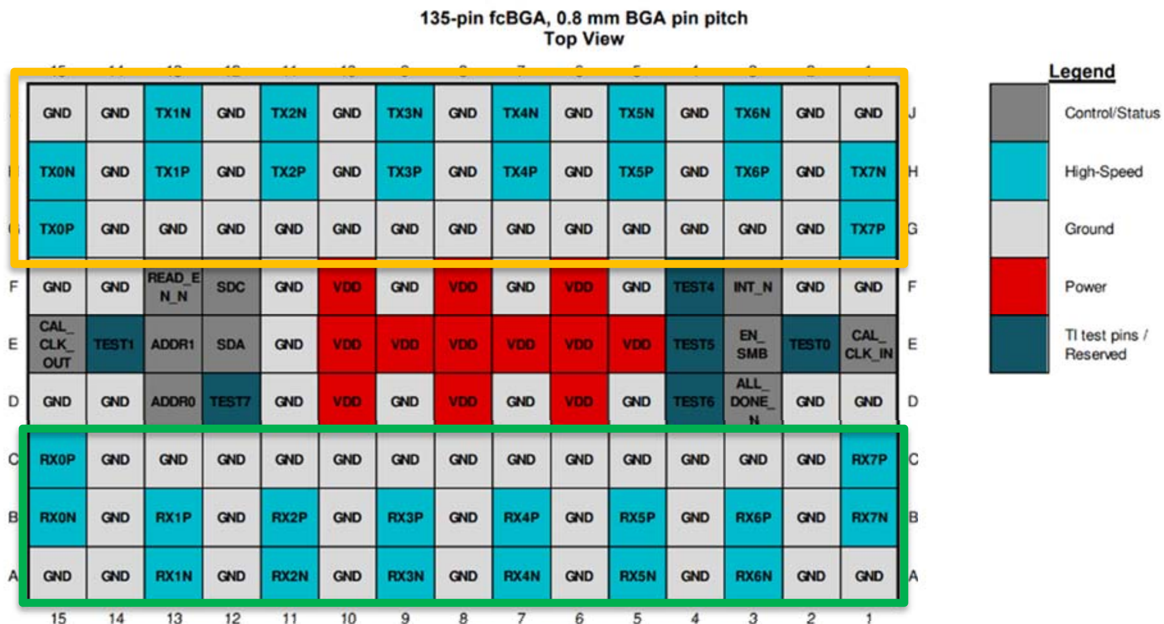


Pin Functions

PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
HIGH SPEED DIFFERENTIAL I/Os				
RX0P	C15	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX0N	B15	Input	None	
RX1P	B13	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX1N	A13	Input	None	
RX2P	B11	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX2N	A11	Input	None	
RX3P	B9	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX3N	A9	Input	None	
RX4P	B7	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX4N	A7	Input	None	
RX5P	B5	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX5N	A5	Input	None	
RX6P	B3	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX6N	A3	Input	None	
RX7P	C1	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX7N	B1	Input	None	
TX0P	G15	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX0N	H15	Output	None	

TX1P	H13	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX1N	J13	Output	None	
TX2P	H11	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX2N	J11	Output	None	
TX3P	H9	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX3N	J9	Output	None	
TX4P	H7	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX4N	J7	Output	None	
TX5P	H5	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX5N	J5	Output	None	
TX6P	H3	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX6N	J3	Output	None	
TX7P	G1	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX7N	H1	Output	None	

250. The TI DS280DF810 has high speed receiver contacts disposed in a second portion (circled in green below) of the pattern of contacts, where the first portion of the pattern (circled in orange below) is not interspersed with the second portion of the pattern, and the high speed receiver contacts are disposed in receiver differential pairs (RX0P-RX0N, RX1P-RX1N, etc.).



Pin Functions

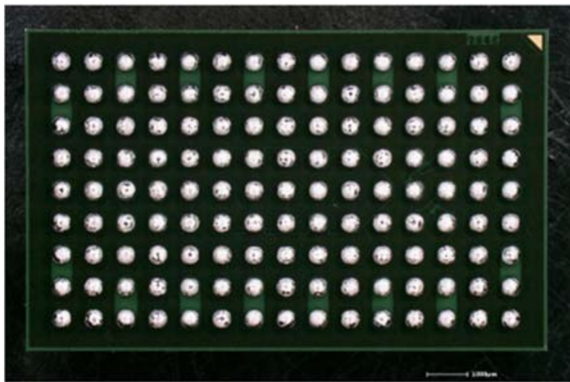
PIN		TYPE	INTERNAL PULL-UP/ PULL-DOWN	DESCRIPTION
NAME	NO.			
HIGH SPEED DIFFERENTIAL I/Os				
RX0P	C15	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX0N	B15	Input	None	
RX1P	B13	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX1N	A13	Input	None	
RX2P	B11	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX2N	A11	Input	None	
RX3P	B9	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX3N	A9	Input	None	
RX4P	B7	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX4N	A7	Input	None	
RX5P	B5	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX5N	A5	Input	None	
RX6P	B3	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX6N	A3	Input	None	
RX7P	C1	Input	None	Inverting and non-inverting differential inputs to the equalizer. An on-chip 100-Ω termination resistor connects RXP to RXN. These inputs are AC coupled on-chip with physical 220 nF capacitors.
RX7N	B1	Input	None	
TX0P	G15	Output	None	Inverting and non-inverting 50 Ω driver outputs. These outputs are AC coupled on-chip with physical 220 nF capacitors.
TX0N	H15	Output	None	

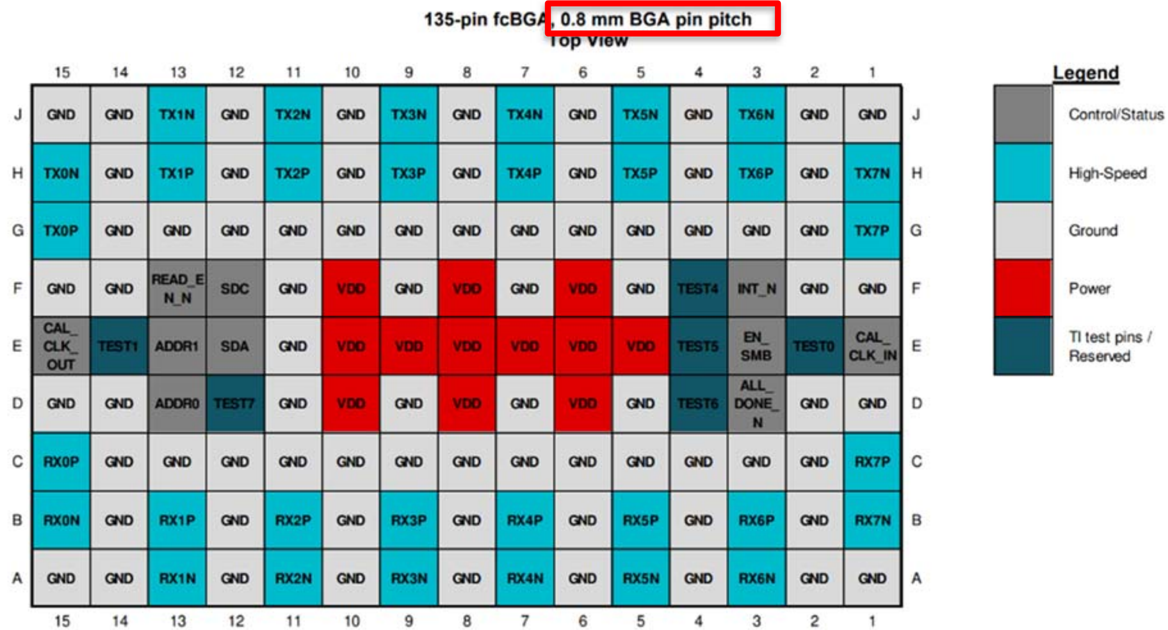
251. The TI DS280DF810 has at least one unbroken line of other contacts (*e.g.,* three lines of contacts circled in yellow below) disposed between the first portion of the pattern and the second portion of the pattern, where the other contacts do not contain any high speed transmitter contacts and high speed receiver contacts.

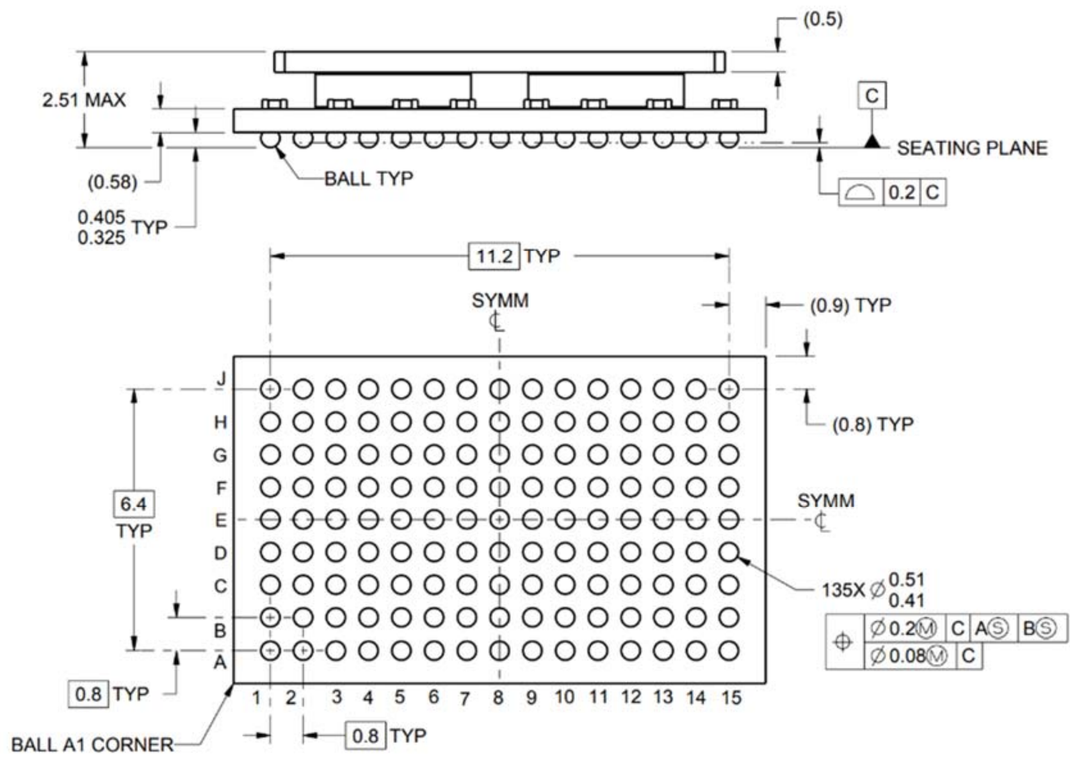
252. The TI DS280DF810 has low speed IO contacts (*e.g.*, "SDC" and "SDA" contacts) disposed in a third portion (circled in purple below) of the pattern, where a part of the third portion of the pattern is disposed in an interior portion of the pattern relative to both the first portion of the pattern and the second portion of the pattern

SYSTEM MANAGEMENT BUS (SMBUS) PINS				
ADDR0	D13	Input, 4-level	None	4-level strap pins used to set the SMBus address of the device. The pin state is read on power-up. The multi-level nature of these pins allows for 16 unique device addresses. The four strap options include: 0: 1 kΩ to GND R: 10 kΩ to GND F: Float 1: 1 kΩ to VDD Refer to Device SMBus Address for more information.
ADDR1	E13	Input, 4-level	None	
EN_SMB	E3	Input, 4-level	None	Four-level 2.5 V input used to select between SMBus master mode (float) and SMBus slave mode (high). The four defined levels are: 0: 1 kΩ to GND - RESERVED, TI test mode. R: 10 kΩ to GND - RESERVED, TI test mode F: Float - SMBus Master Mode 1: 1 kΩ to VDD - SMBus Slave Mode
SDA	E12	I/O, 3.3 V LVCMOS, Open Drain	None	SMBus data input and open drain output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.
SDC	F12	I/O, 3.3 V LVCMOS, Open Drain	None	SMBus clock input and open drain clock output. External 2 kΩ to 5 kΩ pull-up resistor is required as per SMBus interface standard. This pin is 3.3 V LVCMOS tolerant.

253. Substantially all of the contacts of the TI DS280DF810 are disposed at a first pitch (0.8 mm) from one another on a single contact surface.





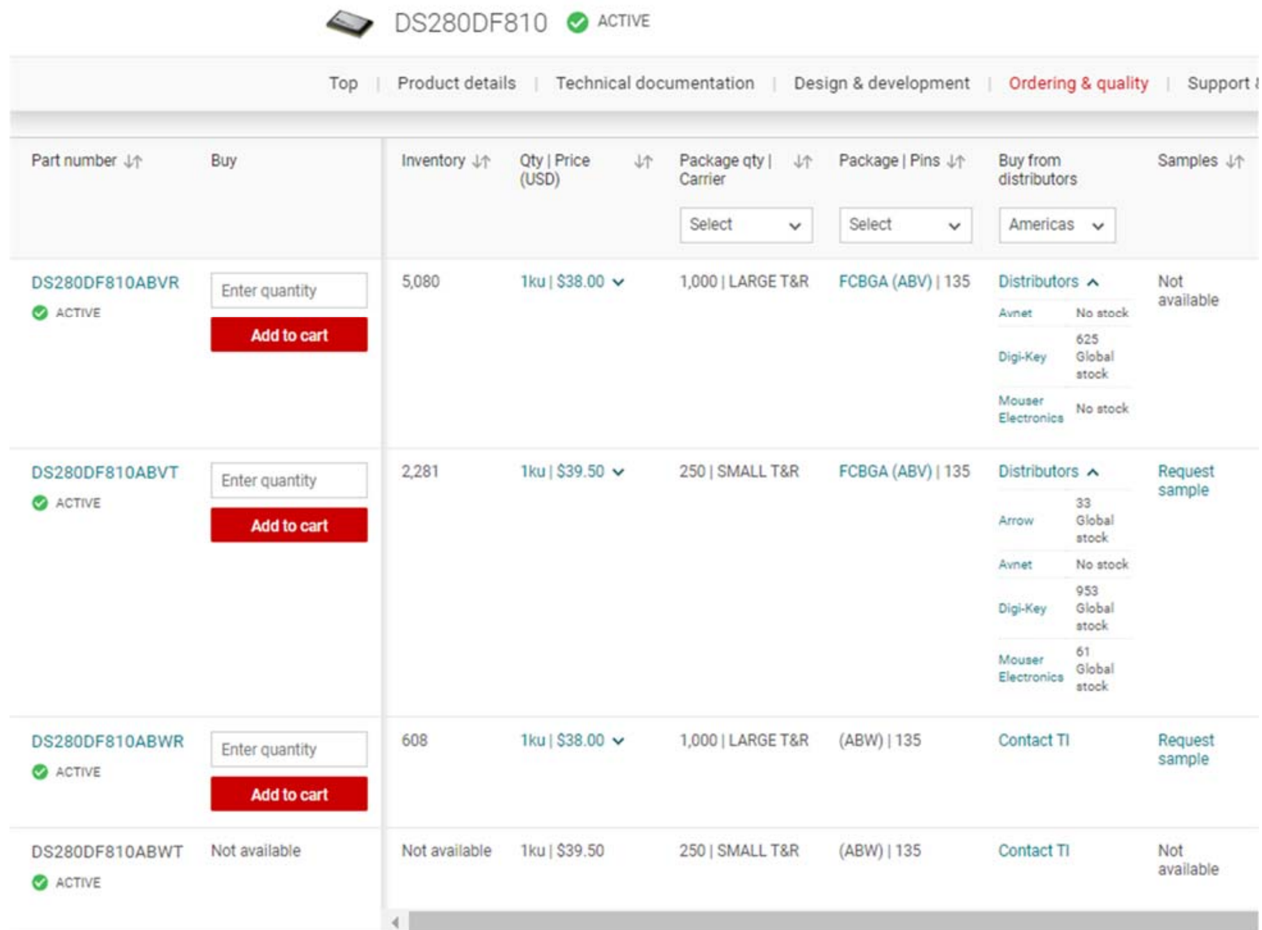


254. Claim 17 of the Ramakrishnan Patent applies to each Ramakrishnan Accused Product at least because each of those products has transmitter and receiver contacts in differential pairs with an unbroken line of other contacts between them, and I/O contacts in the

interior portion of the contacts relative to the transmitter and receiver contacts, like the TI DS280DF810.

255. On information and belief, each of the Ramakrishnan Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

256. By way of example only, the TI DS280DF810 has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:



DS280DF810 ACTIVE

Top | Product details | Technical documentation | Design & development | Ordering & quality | Support &

Part number	Buy	Inventory	Qty | Price (USD)	Package qty | Carrier Select	Package | Pins Select	Buy from distributors Americas	Samples
DS280DF810ABVR ACTIVE	Enter quantity Add to cart	5,080	1ku | $38.00	1,000 | LARGE T&R	FCBGA (ABV) | 135	Distributors Avnet: No stock Digi-Key: 625 Global stock Mouser Electronics: No stock	Not available
DS280DF810ABVT ACTIVE	Enter quantity Add to cart	2,281	1ku | $39.50	250 | SMALL T&R	FCBGA (ABV) | 135	Distributors Arrow: 33 Global stock Avnet: No stock Digi-Key: 953 Global stock Mouser Electronics: 61 Global stock	Request sample
DS280DF810ABWR ACTIVE	Enter quantity Add to cart	608	1ku | $38.00	1,000 | LARGE T&R	(ABW) | 135	Contact TI	Request sample
DS280DF810ABWT ACTIVE	Not available	Not available	1ku | $39.50	250 | SMALL T&R	(ABW) | 135	Contact TI	Not available

See https://www.ti.com/product/DS280DF810#order-quality (last visited July 14, 2020).

257. TI has known of the Ramakrishnan Patent and has been on notice of its infringement of Ramakrishnan Patent since at least as of the filing of this First Amended Complaint.

258. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Ramakrishnan Patent at least because Bell Semic provided TI with written notice of its infringement as of the filing of this First Amended Complaint.

259. TI, knowing its products infringe the Ramakrishnan Patent and with specific intent for others to infringe the Ramakrishnan Patent, induces infringement of one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMS, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Ramakrishnan Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Ramakrishnan Accused Products in the United States. TI knows that the Ramakrishnan Accused Products infringe the Ramakrishnan Patent, and purposefully and knowingly sells and offers to sell the Ramakrishnan Accused Products to its customers with the knowledge and expectation that the Ramakrishnan Accused Products will enter the United States

market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

260. TI further induces infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Ramakrishnan Accused Products and/or products incorporating the Ramakrishnan Accused Products in the United States by marketing the Ramakrishnan Accused Products in the United States; providing information such as detailed datasheets supporting use of the Ramakrishnan Accused Products that promote their features, specifications, and applications; providing design, layout, and power requirements for the Ramakrishnan Accused Products; providing technical documentation for the Ramakrishnan Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Ramakrishnan Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Ramakrishnan Accused Products, including live training and video.

261. Further, TI, knowing that the printed circuit boards (PCBs) used in conjunction with the Ramakrishnan Accused Products infringe at least claims 11-13 of the Ramakrishnan Patent and with specific intent for others to infringe the Ramakrishnan Patent, further induces infringement of at least claims 11-13 of the Ramakrishnan Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including the manufacturers of the corresponding PCBs, customers, distributors, end-users,

and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the PCBs that are used in conjunction with the Ramakrishnan Accused Products, as well as products containing the same. In order for the Ramakrishnan Accused Products to be functional, the pin layout of the Ramakrishnan Accused Products must match the pin layout on the PCB to ensure proper performance of the Ramakrishnan Accused Products. Accordingly, TI knowingly and intentionally designs and specifies the pin layouts for the Ramakrishnan Accused Products, with the knowledge and intent that the manufacturers of the corresponding PCBs must match the pin layout of the PCBs to the pin layout of the Ramakrishnan Accused Products to ensure proper performance of the Ramakrishnan Accused Products, and thus, the PCB manufacturers directly infringe at least claims 11-13 of the Ramakrishnan Patent. Further, through its design and specification of the pin layouts for the Ramakrishnan Accused Products, TI knowingly and intentionally induces the direct infringement of at least claims 11-13 of the Ramakrishnan Patent by its customers, distributors, end-users, and/or other third parties who use, sell, offer to sell, and/or import in or into the United States, in addition to their infringement of one or more other claims of the Ramakrishnan Patent through the use, sale, offers to sell, and/or importation in or into the United States of the Ramakrishnan Accused Products.

262. TI has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Ramakrishnan Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Ramakrishnan Accused Products, which constitute a material part of the invention of the Ramakrishnan Patent, knowing the Ramakrishnan Accused Products to be especially made or especially adapted for use in infringement of the

Ramakrishnan Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

263. Bell Semic has sustained and is entitled to recover damages as a result of TI's infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

264. TI's infringement of the Ramakrishnan Patent is knowing, deliberate, and willful. TI learned of its infringement of the Ramakrishnan Patent no later than the filing of this Amended Complaint. Despite knowing that it was infringing the Ramakrishnan Patent, TI continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Ramakrishnan Patent, despite a risk of infringement that is known or so obvious that it should be known to TI, and/or even though TI otherwise should know that its actions constitute an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is egregious. TI's knowing, deliberate, and willful infringement of the Ramakrishnan Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 10

Willful Infringement of U.S. Patent No. 6,441,499 (Nagarajan Patent)

265. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

266. The Nagarajan Patent is generally related to a flip chip ball grid array (BGA) package that includes a die that was thinned for matching a composite coefficient of thermal expansion to that of a second level board. (*See* Nagarajan Patent, Abstract.)

267. The composite coefficient of thermal expansion (CTE) of a standard BGA package was typically lower than the CTE of the second level board because the die within the BGA package typically had a CTE several times lower than that of the second level board. This difference in CTEs could cause cracking of the solder balls that connect the substrate to the second level board and result in poor second level package reliability. The Nagarajan Patent provided a solution to this issue by thinning the die, which thus has a smaller effect on the composite CTE of the BGA package so that the CTE of the BGA package matches more closely to the CTE of the second level board.

268. The Nagarajan Patent contains 1 independent claim and 7 total claims, covering flip chip BGA packages. Claim 2 reads:

> [A flip chip ball grid array package comprising a thin die having a die thickness for matching a composite coefficient of thermal expansion to that of a second level board],
>
> wherein the die thickness is within a range from about 127 microns to about 381 microns.

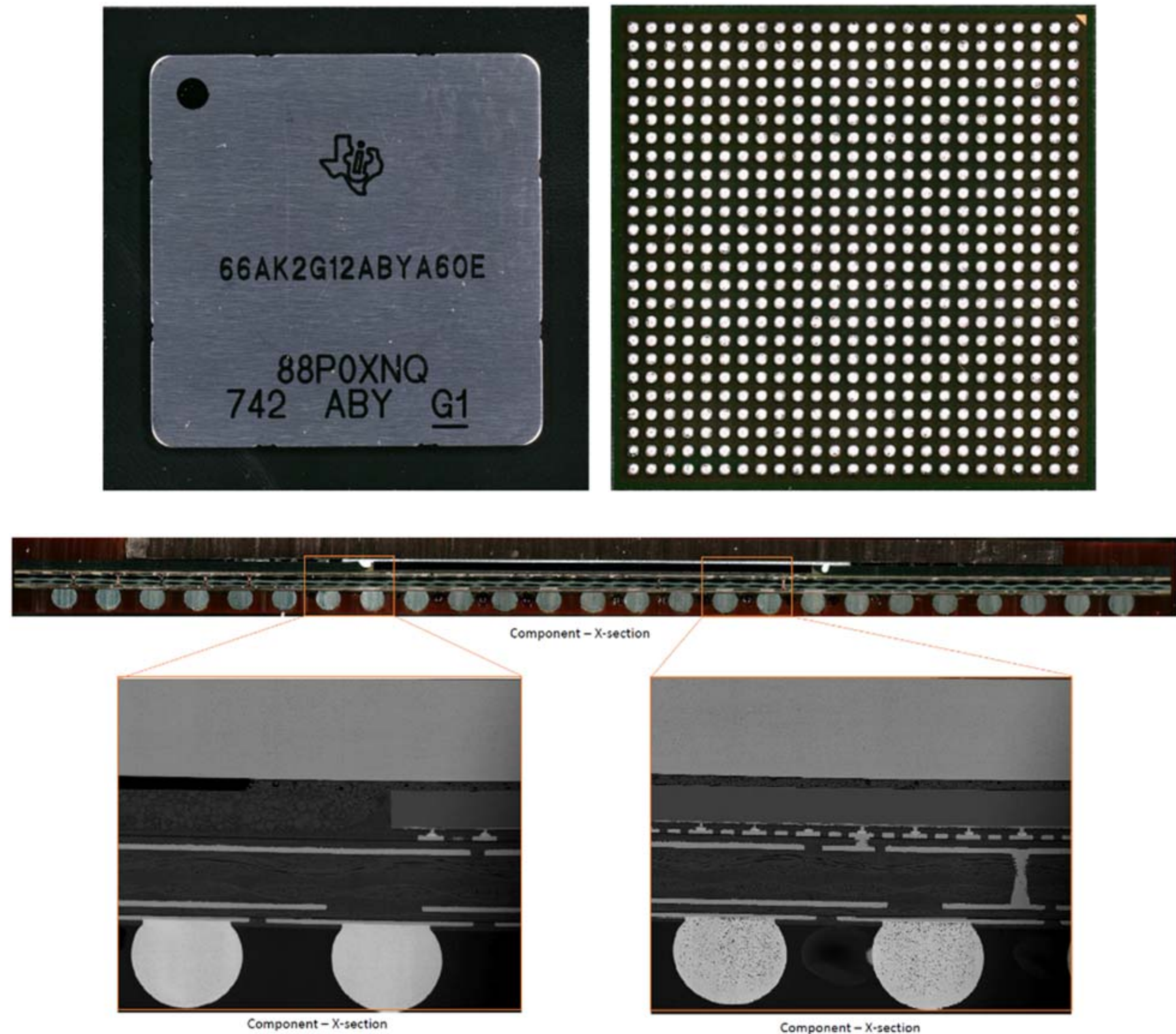
269. TI has directly infringed, and continues to directly infringe, one or more claims of the Nagarajan Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Nagarajan Patent (*e.g.*, claims 1-5), including, but not limited to:

- TI products with a flip chip BGA package with a die having a thickness of 381 microns or less;
- TI's 66AK2G12ABYA60E, a multicore SoC based on TI's Keystone II architecture; and
- TI's devices that are variants of the above-identified products;

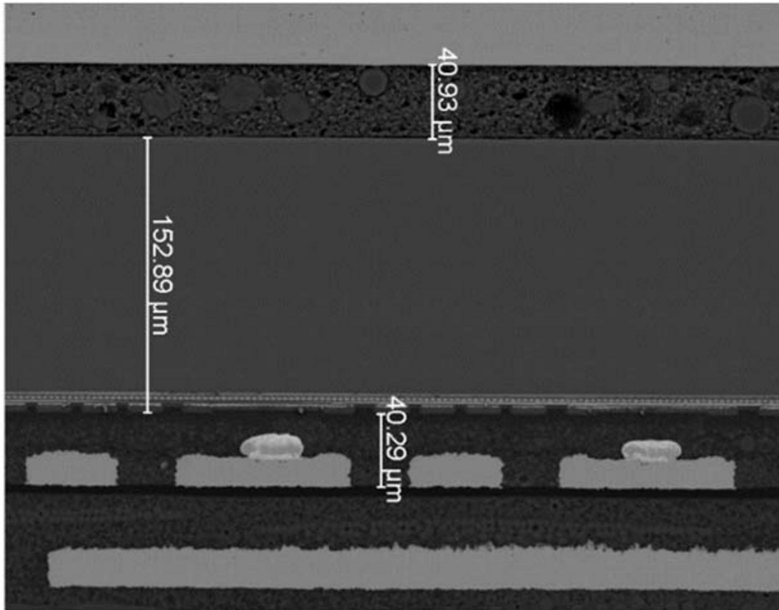
(collectively, the "Nagarajan Accused Products").

270. By way of non-limiting example only, TI's 66AK2G12ABYA60E infringes claim 2 of the Nagarajan Patent because it is a flip chip ball grid array package that has a thin die having a die thickness for matching a composite coefficient of thermal expansion to that of a second level board, and has a die thickness within a range from about 127 microns to about 381 microns.

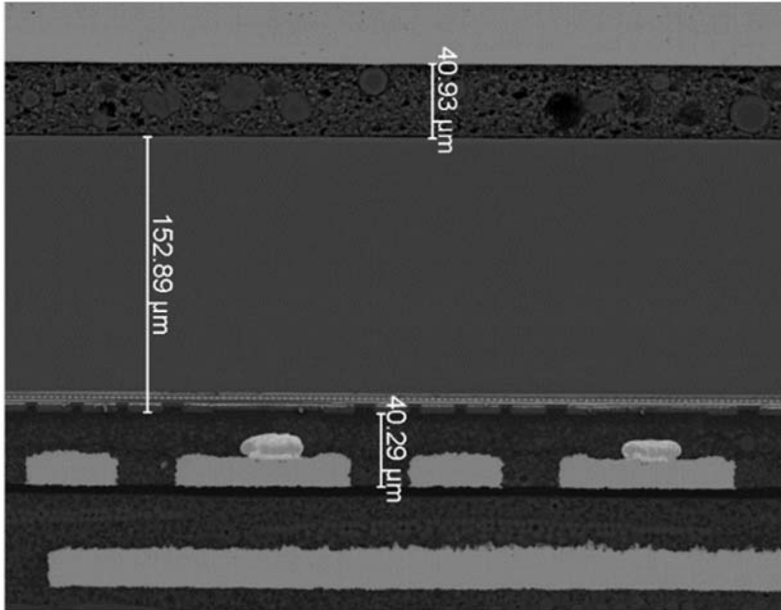
271. As shown below, TI's 66AK2G12ABYA60E is an integrated circuit with a flip chip ball grid array package.



272. The TI 66AK2G12ABYA60E has a thin die, here 152.89 µm. On information and belief, the thin die of the TI 66AK2G12ABYA60E was thinned so that the composite CTE of the BGA package would match more closely to the CTE of the intended second level boards. On information and belief, the composite CTE of the BGA package is between 10-11 ppm/ºC, while the typical CTE of a BGA package with a non-thinned die is around 6 ppm/ºC.



273. The thickness of the die in the TI 66AK2G12ABYA60E is within a range from about 127 microns to about 381 microns, here, 152.89 µm (microns).



274. Claim 2 of the Nagarajan Patent applies to each Nagarajan Accused Product at least because each of those products have a BGA package and a die having a thickness from about 127-381 microns, like the TI 66AK2G12ABYA60E.

275. On information and belief, each of the Nagarajan Accused Products have been available for purchase in the United States, including but not limited to, directly from TI, through TI's website, and/or through TI-authorized Americas distributors.

276. By way of example only, the TI 66AK2G12ABYA60E has been available for purchase in the United States, including but not limited to through TI's website, either directly from TI or through at least three TI-authorized Americas distributors:

66AK2G12 ACTIVE | Data sheet | Order now

Top | Product details | Technical documentation | Design & development | Ordering & quality | Support & training

Part number	Buy	Inventory	Qty | Price (USD)	Package qty | Carrier	Package | Pins	Buy from distributors	Samples	Material type	Operating temperature range (°C)	Device marking	Lead finish/Ball material
				Select	Select	Americas					
66AK2G12ABY60 ACTIVE	Enter quantity Add to cart	299	1ku | $19.36	60 | JEDEC TRAY (5+1)	FCBGA (ABY) | 625	Distributors	Not available	Production	0 to 90	View	SNAGCU
66AK2G12ABYA100 ACTIVE	Not available	Not available	1ku | $27.98	60 | JEDEC TRAY (5+1)	FCBGA (ABY) | 625	Distributors	Not available	Production	-40 to 105	View	SNAGCU
66AK2G12ABYA100E ACTIVE	Not available	Not available	1ku | $30.88	60 | JEDEC TRAY (5+1)	FCBGA (ABY) | 625	Distributors	Not available	Production	-40 to 105	View	SNAGCU
66AK2G12ABYA60 ACTIVE	Enter quantity Add to cart	80	1ku | $22.26	60 | JEDEC TRAY (5+1)	FCBGA (ABY) | 625	Distributors Arrow 2 Global stock Avnet No stock Digi-Key No stock Mouser Electronics No stock	Not available	Production	-40 to 105	View	SNAGCU
66AK2G12ABYA60E ACTIVE	Not available	Not available	1ku | $25.17	60 | JEDEC TRAY (5+1)	FCBGA (ABY) | 625	Distributors Arrow 8 Global stock Avnet No stock Digi-Key No stock Mouser Electronics 30 Global stock	Not available	Production	-40 to 105	View	SNAGCU

See https://www.ti.com/product/66AK2G12#order-quality (last visited July 14, 2020).

277. TI has known of the Nagarajan Patent and has been on notice of its infringement of Nagarajan Patent since at least March 18, 2005. On March 18, 2005, during prosecution of TI's U.S. patent application 10/737,682, which published as US 2005/0127484, the examiner cited the Nagarajan Patent as pertinent to the applicant's disclosure. On August 30, 2019, Bell Semic identified the TI 66AK2G12ABYA60E as infringing and exemplary of TI's infringement of the Nagarajan Patent. After TI did not respond to that letter, Bell Semic sent another letter to TI on January 10, 2020, again identifying the TI 66AK2G12ABYA60E as infringing and exemplary of TI's infringement. TI also did not respond to that letter.

278. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Nagarajan Patent at least because Bell Semic provided TI with written notice of its infringement as detailed above.

279. TI, knowing its products infringe the Nagarajan Patent and with specific intent for others to infringe the Nagarajan Patent, has induced infringement of, and continue to induce infringement of, one or more claims of the Nagarajan Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, package assemblers, distributors, customers, end-users, and/or other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Nagarajan Accused Products, as well as products containing the same. TI knowingly and intentionally instructs its customers, OEMs, foundry suppliers, package assemblers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on TI's website. TI actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Nagarajan Accused Products in the United States. TI knows, and has known since at least August 30, 2019, that the Nagarajan Accused Products infringe the Nagarajan Patent, and purposefully and knowingly sells and offers to sell the Nagarajan Accused Products to its customers with the knowledge and expectation that the Nagarajan Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

280. TI further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Nagarajan Accused Products and/or products incorporating the Nagarajan Accused Products in the United States by marketing the Nagarajan Accused Products in the United States; providing information such as detailed datasheets supporting use of the Nagarajan Accused Products that promote their features, specifications, and

applications; providing design, layout, and power requirements for the Nagarajan Accused Products; providing technical documentation for the Nagarajan Accused Products including application notes, technical articles, and user guides describing how to implement, optimize, and test applications; providing design and development tools (such as circuit design and simulation tools); providing support and training through TI E2E Support; and by promoting the incorporation of the Nagarajan Accused Products into end-user products by providing for its customers reference designs; complimentary design review services; hardware, software, and development tools; and robust customer support. In addition to these resources, TI also provides numerous support resources for the customers of its Nagarajan Accused Products, including live training and video.

281. TI has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Nagarajan Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Nagarajan Accused Products, which constitute a material part of the invention of the Nagarajan Patent, knowing the Nagarajan Accused Products to be especially made or especially adapted for use in infringement of the Nagarajan Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

282. Bell Semic has sustained and is entitled to recover damages as a result of TI's past and continuing infringement, in an amount adequate to compensate for TI's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

283. TI's infringement of the Nagarajan Patent is and has been knowing, deliberate, and willful. TI learned of its infringement of the Nagarajan Patent no later than March 18, 2005.

As detailed above, on March 18, 2005 the examiner cited the Nagarajan Patent during prosecution of TI's U.S patent application no. 10/737,682. Bell Semic further sent letters to TI on August 30, 2019 and January 10, 2020 identifying the Nagarajan Patent as being infringed by TI's exemplary 66AK2G12ABYA60E product. TI did not respond to either of these letters. Despite these efforts, and knowing that it was willfully infringing the Nagarajan Patent, TI continued and continues to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Nagarajan Patent, despite a risk of infringement that was known or so obvious that it should have been known to TI, and/or even though TI otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, TI's conduct is and has been egregious. TI's knowing, deliberate, and willful infringement of the Nagarajan Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Bell Semic prays for the following relief:

A. A judgment that TI has infringed one or more claims of each Asserted Patent;

B. An award of damages resulting from TI's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order requiring TI to provide accountings and to pay supplemental damages to Bell Semic, including, without limitation, additional damages for any infringing sales not presented at trial, and prejudgment and post-judgment interest;

D. A judgment and order finding that TI's acts of infringement were willful and egregious and trebling damages under 35 U.S.C. § 284;

E. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Bell Semic its reasonable attorneys' fees against TI.

F. A permanent injunction enjoining TI and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in active concert or participation with TI, from infringing the Hall 340, Hall 269, Kang, Gibson, Banerjee, Ma, Chen, Ramakrishnan, and Nagarajan Patents;

G. If a permanent injunction preventing further infringement of the Hall 340, Hall 269, Kang, Gibson, Banerjee, Ma, Chen, Ramakrishnan, and Nagarajan Patents is not granted, a compulsory ongoing licensing fee for any such further infringement; and

H. Any and all other relief to which Plaintiff may show itself to be entitled.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Dated: July 31, 2020

/s/ *Paul J. Skiermont*
Paul J. Skiermont (TX Bar No. 24033073)
Steven W. Hartsell (TX Bar No. 24040199)
Jaime K. Olin (TX Bar No. 24070363)
Joseph M. Ramirez (TX Bar No. 24108257)
SKIERMONT DERBY LLP
1601 Elm St., Ste. 4400
Dallas, TX 75201
Phone: (214) 978-6600
Fax: (214) 978-6601
pskiermont@skiermontderby.com
shartsell@skiermontderby.com
jolin@skiermontderby.com
jramirez@skiermontderby.com

Charles C. Koole (CA Bar No. 259997)
SKIERMONT DERBY LLP
800 Wilshire Blvd., Ste. 1450
Los Angeles, CA 90017
Phone: (213) 788-4500
Fax: (213)788-4545
ckoole@skiermontderby.com

Attorneys for Plaintiff
BELL SEMICONDUCTOR, LLC