UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

TELEPUTERS, LLC, Plaintiff v. RENESAS ELECTRONICS AMERICA, INC. AND RENESAS ELECTRONICS CORPORATION, Defendants	**Case No. 6:20-cv-599** **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Teleputers, LLC ("Plaintiff" or "Teleputers") hereby files this First Amended Complaint for Patent Infringement against Defendants Renesas Electronics America, Inc. and Renesas Electronics Corporation (collectively "Defendants" or "Defendant" or "Renesas"), and alleges, on information and belief, as follows:

THE PARTIES

1. Teleputers, LLC is a limited liability company organized and existing under the laws of the State of New Jersey with its principal place of business in Princeton, New Jersey.

2. On information and belief, Defendant Renesas Electronics America, Inc. is a California corporation with its principal place of business at 1001 Murphy Ranch Road, Milpitas, California 95035. Renesas Electronics America, Inc. may be served through its registered agent, Corporation Service Company (which will do business in California as CSC - Lawyers Incorporating Service, 251 Little Falls Drive, Wilmington, Delaware 19808.

3. On information and belief, Defendant Renesas Electronics Corporation is a company organized under the laws of Japan with its principal place of business at TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan. Renesas Electronics Corporation may be served through its U.S. subsidiary, Renesas Electronics America, Inc.

JURISDICTION AND VENUE

4. This action arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. Defendants have committed acts of infringement in this judicial district.

6. On information and belief, Defendants maintain regular and systematic business interests in this district and throughout the State of Texas including through their representatives, employees and physical facilities.

7. On information and belief, the Court has personal jurisdiction over Defendants because Defendants have committed, and continue to commit, acts of infringement in the State of Texas, have conducted business in the State of Texas, and/or have engaged in continuous and systematic activities in the State of Texas. On information and belief, Defendants' accused instrumentalities that are alleged herein to infringe were and continue to be used, imported, offered for sale, and/or sold in the Western District of Texas.

8. On information and belief, Defendants voluntarily conduct business and solicit customers in the State of Texas and within this District, including, but not limited to, its offices located at 900 S. Capital of Texas Highway, Las Cimas IV, Suite 250, Austin, Texas 78746. *See, e.g.:*

Global Locations | Renesas Electronics Europe

Design Centers 1

Company	Phone	Fax	Email	Notes
TX Design Center 900 S. Capital of Texas Hwy Las Cimas IV, Suite 250 Austin, TX 78746	--	--	--	

Renesas website as visited on June 23, 2020 at: https://www.renesas.com/us/en/support/contact/locations.html?region=United States&subregion=Texas.

9. On information and belief, Defendants generate substantial revenue within this District and from the acts of infringement as carried out in this District. As such, the exercise of jurisdiction over Defendants would not offend the traditional notions of fair play and substantial justice.

10. Venue is proper in the Western District of Texas pursuant to 28 U.S.C. § 1400(b) and 28 U.S.C. § 1391(c)(3).

NOTICE OF TELEPUTERS' PATENTS

11. Teleputers is owner by assignment of U.S. Patent No. 6,922,472 ("the '472 Patent") entitled "Method and system for performing permutations using permutation instructions based on butterfly networks." A copy may be obtained at: https://patents.google.com/patent/US6922472B2/en.

12. Teleputers is owner by assignment of U.S. Patent No. 6,952,478B2 ("the '478 Patent") entitled "Method and system for performing permutations using permutation instructions based on modified omega and flip stages." A copy may be obtained at: https://patents.google.com/patent/US6952478B2/en.

13. Teleputers is owner by assignment of U.S. Patent No. 7,092,526B2 ("the '526 Patent" and collectively with the '478 Patent, "the Patents-in-Suit") entitled "Method and system for performing subword permutation instructions for use in two-dimensional multimedia processing." A copy may be obtained at: https://patents.google.com/patent/US7092526B2/en.

14. Teleputers is owner by assignment of U.S. Patent No. 7,174,014B2 ("the '014 Patent") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at: https://patents.google.com/patent/US7174014B2/en.

15. Teleputers is owner by assignment of U.S. Patent No. 7,519,795B2 ("the '795 Patent") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at: https://patents.google.com/patent/US7519795B2/en.

16. The foregoing Patents, namely the '014 Patent, the '526 Patent, the '478 Patent, the '472 Patent, and the '795 Patent are collectively referred to as "the Teleputers Patents."

17. Teleputers is the owner of all right, title, and interest in each of the Teleputers Patents. None of the Teleputers Patents, nor any of the claimed subject matter in any such Teleputers Patents, has been otherwise assigned to any person or entity other than Teleputers. Teleputers therefore has complete and unfettered standing to assert and seek money damages for the infringement of each and every one of the Teleputers Patents.

18. No entity other than Teleputers presently claims any ownership interest, valid or otherwise, in any of the Teleputers Patents. Teleputers possesses full legal title to each of the Teleputers Patents.

19. The records at the United States Patent and Trademark Office indicate duly recorded assignments of the Teleputers Patents from the inventors (Lee, Shi, Yang, and/or Vachharajani) to Teleputers, LLC, executed on February 14, 2005. No other assignments of interest in any

Teleputers Patent have been recorded with the United States Patent and Trademark Office, and no such assignments exist. Indeed, the face of each Teleputers Patent properly identifies Teleputers LLC as the legal assignee. As such, because each of the Teleputers Patents were issued to the inventors, and because the inventors assigned the Teleputers Patents to Teleputers LLC and filed copies of such assignments with the Patent and Trademark Office, Plaintiff presumptively has proper standing to bring these causes of action. By operation of law, legal title vests in the inventors, and passes to another only by way of assignment or effective legal transfer.

20. To the extent Princeton University possessed any rights whatsoever in any Teleputers Patent, such rights were equitable in nature and non-exclusive to the rights of the inventors. The Verified Statement Claiming Small Entity Status (dated March 5, 2000) in the certain Provisional Patent Application Number 60/202,250 states only that certain unidentified "rights under contract or law" were, at the time, allegedly possessed by The Trustees of Princeton University. The Verified Statement further made clear that the named inventors possessed legal rights to the inventions. At best, such rights possessed by Princeton were equitable, and were in any event limited to the *inventions*, not to the issued *patents*. Further, the written policies of Princeton University relating to inventions (*see* https://dof.princeton.edu/policies-procedure/policies/patents) expressly call for the outright assignment of inventions to the inventors or the transfer of the inventions to a patent management company. Having not transferred any of the Teleputers Patents to any patent management company, the historical actions of Princeton reflect an abandonment of equitable rights and an assignment of all rights (equitable and legal) to the inventors. Stated differently, the conduct of the parties (Princeton and the inventors) evidences an abandonment of rights on the part of Princeton, and full equitable and legal title in the inventors.

In any event, the "rights" allegedly possessed by Princeton in the '250 Application do not carry over to the inventions described and claimed in the Teleputers Patents.

21. The Teleputers Patents are valid, enforceable, and were duly issued in full compliance with Title 35 of the United States Code.

22. Defendants, at least by the date of this Original Complaint, are on notice of the Teleputers Patents.

23. Each of the aforementioned Teleputers Patents are directed to, and claim, patent eligible subject matter, and each is presumed to be valid and patent-eligible.

24. The '472 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. The permute instructions are based on a Benes network comprising two butterfly networks of the same size connected back-to-back. Intermediate sequences of bits are defined that an initial sequence of bits from a source register are transformed into. Each intermediate sequence of bits is used as input to a subsequent permutation instruction. Permutation instructions are determined for permitting the initial source sequence of bits into one or more intermediate sequence of bits until a desired sequence is obtained. The intermediate sequences of bits are determined by configuration bits. The permutation instructions form a permutation instruction sequence of at least one instruction. At most 21 gr/m permutation instructions are used in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted, and m is the number of network stages executed in one instruction. The permutation instructions can be used to permute k-bit subwords packed into an n-bit word, where k can be 1, 2, . . . , or n bits, and k*r=n. *See* Abstract, '472 Patent.

25. The claims of the '472 Patent claim priority to at least May 5, 2000.

26. The claims of the '472 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

27. Further, the claims of the '472 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

28. Further, the claims of the '472 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '472 Patent at 1:17-3:15.

29. For example, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '472 Patent at 3:17-21.

30. Further, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '472 Patent at 3:24-37.

31. Further, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '472 Patent at 3:42-47.

32. The foregoing improvements and technological solutions, as captured in the claims of the '472 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

33. Further, the claims of the '472 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

34. Consequently, the claims of the '472 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

35. The '472 Patent was examined by Primary United States Patent Examiner Gilberto Barron, Jr, with Assistant Examiner Grigory Gurshman. During the examination of the '472 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/37, 28, 1.

36. After conducting a search for prior art during the examination of the '472 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US5495476A; (ii) US5546393A; (iii) US6381690B1; (iv) US6446198B1; (v) US6629115B1; (vi) US6108311A; and (vii) US5940389A.

37. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '472 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner

properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

38. The '478 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. The permute instructions are based on an omega-flip network comprising at least two stages in which each stage can perform the function of either an omega network stage or a flip network stage. Intermediate sequences of bits are defined that an initial sequence of bits from a source register are transformed into. Each intermediate sequence of bits is used as input to a subsequent permutation instruction. Permutation instructions are determined for permuting the initial source sequence of bits into one or more intermediate sequence of bits until a desired sequence is obtained. The intermediate sequences of bits are determined by configuration bits. The permutation instructions form a permutation instruction sequence, of at least one instruction. At most 21 gr/m permutation instructions are used in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted, and m is the number of network stages executed in one instruction. The permutation instructions can be used to permute k-bit subwords packed into an n-bit word, where k can be 1, 2, . . . , or n bits, and k*r=n. *See* Abstract, '478 Patent.

39. The claims of the '478 Patent claim priority to at least May 5, 2000.

40. The claims of the '478 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

41. Further, the claims of the '478 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

42. Further, the claims of the '478 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '478 Patent at 1:17-3:15.

43. For example, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '478 Patent at 3:17-21.

44. Further, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '478 Patent at 3:24-37.

45. Further, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '478 Patent at 3:42-47.

46. The foregoing improvements and technological solutions, as captured in the claims of the '478 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

47. Further, the claims of the '478 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

48. Consequently, the claims of the '478 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

49. The '478 Patent was examined by Primary United States Patent Examiner Thomas Peeso, with Assistant Examiner Grigory Gurshman. During the examination of the '478 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/37, 28, 1, 380/26.

50. After conducting a search for prior art during the examination of the '478 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US5495476A; (ii) US5546393A; (iii) US6381690B1; (iv) US6446198B1; and (v) US6629115B1.

51. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '478 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

52. The '526 Patent relates generally to methods and systems for providing provides a set of permutation primitives for current and future 2-D multimedia programs which are based on decomposing images and objects into atomic units, then finding the permutations desired for the atomic units. The subword permutation instructions for these 2-D building blocks are also defined

for larger subword sizes at successively higher hierarchical levels. The atomic unit can be a 2×2 matrix and four triangles contained within the 2×2 matrix. Each of the elements in the matrix can represent a subword of one or more bits. The permutations provide vertical, horizontal, diagonal, rotational, and other rearrangements of the elements in the atomic unit. *See* Abstract, '526 Patent.

53. The claims of the '526 Patent claim priority to at least May 7, 2001.

54. The claims of the '526 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

55. Further, the claims of the '526 Patent overcome deficiencies in the prior art, including but not limited to those deficiencies embodied in subword parallelism, shift-and-rotate instructions, extract-and-deposit instructions, and mix-and-permute. The prior art was deficient in its ability to permute more than 16 elements. *See* '526 Patent at 1:15-2:23.

56. Further, the claims of the '526 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

57. For example, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, and provide for efficient subword permutation instructions that can be used for parallel execution, for example in 2-D multimedia processing. *See* '526 Patent at 2:50-53.

58. Further, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, and provide for single-cycle instructions, which can be used to construct any type of permutations needed in two-dimensional (2-D) multimedia processing. The instructions can be used in a programmable processor, such as a digital signal processor, video

signal processors, media processors, multimedia processors, cryptographic processors and programmable System-on-a-Chips (SOCs). *See* '526 Patent at 2:56-62.

59. Further, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, wherein the subword permutation primitives enhance the use of subword parallelism by allowing in-place rearrangement of packed subwords across multiple registers, reducing the need for memory accesses with potentially costly cache misses. The alphabet of permutation primitives of the invention is easy to implement and is useful for 2-D multimedia processing and for other data-parallel computations using subword parallelism. *See* '526 Patent at 3:40-47.

60. The foregoing improvements and technological solutions, as captured in the claims of the '526 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

61. Further, the claims of the '526 Patent do not preempt all methods and systems for providing permutation primitives.

62. Consequently, the claims of the '526 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

63. The '526 Patent was examined by Primary United States Patent Examiner Hosuk Song. During the examination of the '526 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 708/100, 708/520, 712/1, 10, 20, 16, 24, 200, 380/28, 380/37, 42-47.

64. After conducting a search for prior art during the examination of the '526 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art

references found during the search: (i) US4751733A; (ii) US4845668A; (iii) US5113516A; (iv) US5423010A; and (v) US5673321A.

65. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '526 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

66. The '014 Patent relates generally to methods and systems for providing permutation instructions usable in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. PPERM and PPERM3R instructions are defined to perform permutations by a sequence of instructions with each sequence specifying the position in the source for each bit in the destination. In the PPERM instruction bits in the destination register that change are updated and bits in the destination register that do not change are set to zero. In the PPERM3R instruction bits in the destination register that change are updated and bits in the destination register that do not change are copied from intermediate result of previous PPERM3R instructions. Both PPERM and PPERM3R instructions can individually do permutation with bit repetition. Both PPERM and PPERM3R instructions can individually do permutation of bits stored in more than one register. In an alternate embodiment, a GRP instruction is defined to perform permutations. *See* Abstract, '014 Patent.

67. The claims of the '014 Patent claim priority to at least May 7, 2001.

68. The claims of the '014 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

69. Further, the claims of the '014 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

70. Further, the claims of the '014 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '014 Patent at 1:14-2:67.

71. For example, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '014 Patent at 3:1-5.

72. Further, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '014 Patent at 3:9-21.

73. Further, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '014 Patent at 3:26-31.

74. The foregoing improvements and technological solutions, as captured in the claims of the '014 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

75. Further, the claims of the '014 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

76. Consequently, the claims of the '014 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

77. The '014 Patent was examined by Primary United States Patent Examiner Emmanuel L. Moise, with Assistant Examiner Paul Callahan. During the examination of the '014 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/44, 380/265, 28, 377/54, 60, 75, 67, 81, 711/109, 340/825.68, 365/73, 78, 712/1, 24, 10, 712/223.

78. After conducting a search for prior art during the examination of the '014 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US5524256A; (ii) US5734721A; (iii) US6865272B2; (iv) US4907233A; (v) JP2863597B2; (vi) US5734334A; (vii) US5422705A; (viii) GB9617553D0; (ix) US5996104A; (x) US6275965B1; (xi) US6233671B1; (xii) US6483543B1; (xiii) EP0992916A1; (xiv) US7174014B2; and (xv) Zhijie Shi, Ruby B. Lee: "Bit Permutation Instructions for Accelerating Software Cryptography", in Proc. IEEE Intl. Conf. Application-Specific Systems, Architectures and Processors, pp. 138-148, Jul. 2000.

79. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United

States Patent Examiner(s) allowed all of the claims of the '014 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

80. The '795 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. PPERM and PPERM3R instructions are defined to perform permutations by a sequence of instructions with each sequence specifying the position in the source for each bit in the destination. In the PPERM instruction bits in the destination register that change are updated and bits in the destination register that do not change are set to zero. In the PPERM3R instruction bits in the destination register that change are updated and bits in the destination register that do not change are copied from intermediate result of previous PPERM3R instructions. Both PPERM and PPERM3R instruction can individually do permutation with bit repetition. Both PPERM and PPERM3R instruction can individually do permutation of bits stored in more than one register. In an alternate embodiment, a GRP instruction is defined to perform permutations. The GRP instruction divides the initial sequence in the source register into two groups depending on control bits. The first group is combined with the second group to form an intermediate sequence toward the desired final permutation. The total number of GRP instructions for a bit level permutation of n bits is not greater than 1gn. The GRP instruction can be used to permute k-bit subwords packed into an n bits word, where k can be 1, 2, . . . , or n bits, and k*r=n. At most 1gr permutation instructions are used

in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted. The GRP instruction can also be used to permute 2n bits stored in two n-bit registers. The total number of instructions for bit permutation of 2n bits is 21gn+4, and two of those instructions are SHIFT PAIR instruction. *See* Abstract, '795 Patent.

81. The claims of the '795 Patent claim priority to at least May 5, 2000.

82. The claims of the '795 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

83. Further, the claims of the '795 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

84. Further, the claims of the '795 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '795 Patent at 1:19-2:65.

85. For example, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '795 Patent at 2:66-3:3.

86. Further, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '795 Patent at 3:7-19.

87. Further, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '795 Patent at 3:17-28.

88. The foregoing improvements and technological solutions, as captured in the claims of the '795 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

89. Further, the claims of the '795 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

90. Consequently, the claims of the '795 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

91. The '795 Patent was examined by Primary United States Patent Examiner Eric Coleman. During the examination of the '795 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 712/223, 380/28.

92. After conducting a search for prior art during the examination of the '795 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US4907233A; (ii) US5126831A; (iii) US5546393A; (iv) US5673321A; (v) US5734334A; (vi) US5996104A; (vii) US6119224A; (viii) US6233671B1; (ix) US6275965B1; (x) US6278709B1; (xi) US6483543B1; (xii) US6658578B1; (xiii) US6865272B2; and (xiv) US5422705A.

93. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United

States Patent Examiner(s) allowed all of the claims of the '795 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

ACCUSED INSTRUMENTALITIES

94. On information and belief, Defendants make, use, import, sell, and/or offer for sale a multitude of products and services as systems on chips ("SoC") that employ Arm Neon technology supporting the infringing instructions including, but not limited to: the R-Car Hxx, R-Car Mxx, R-Car Exx, R-Car V3M, EMMA Mobile/EV2, R-Mobile A1, RZ/A1xx, RZ/A2M, RZ/G2xx, RZ/G1xx, GR-PEACH, GR-LYCHEE, emCON-RZ_G1x, and DIMM-RZ/A1H (individually and collectively, the "Accused Instrumentalities"). On information and belief, the Accused Instrumentalities are made, used, sold, offered for sale, and/or imported in the United States by Defendants.

COUNT I
(Infringement of U.S. Patent No. 7,092,526B2)

95. Teleputers incorporates the above paragraphs by reference.

96. Defendants have been on notice of the '526 Patent at least as early as the date it received service of this Original Complaint.

97. On information and belief, Defendants have directly infringed and continue to infringe the '526 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

98. On information and belief, Defendants, at least as of the date of service of the Original Complaint in this matter, and with knowledge of the '526 Patent, indirectly infringe the '526 Patent by inducing others to infringe the '526 Patent. In particular, Defendants have or will intend to induce customers to infringe the '526 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

99. On information and belief, Defendants also have or will induce others, including its customers, to infringe the '526 Patent by providing technical support for the use of the Accused Instrumentalities.

100. On information and belief, at all times Defendants own and control the operation of the Accused Instrumentalities in accordance with an end user license agreement.

101. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the '526 Patent when used as intended.

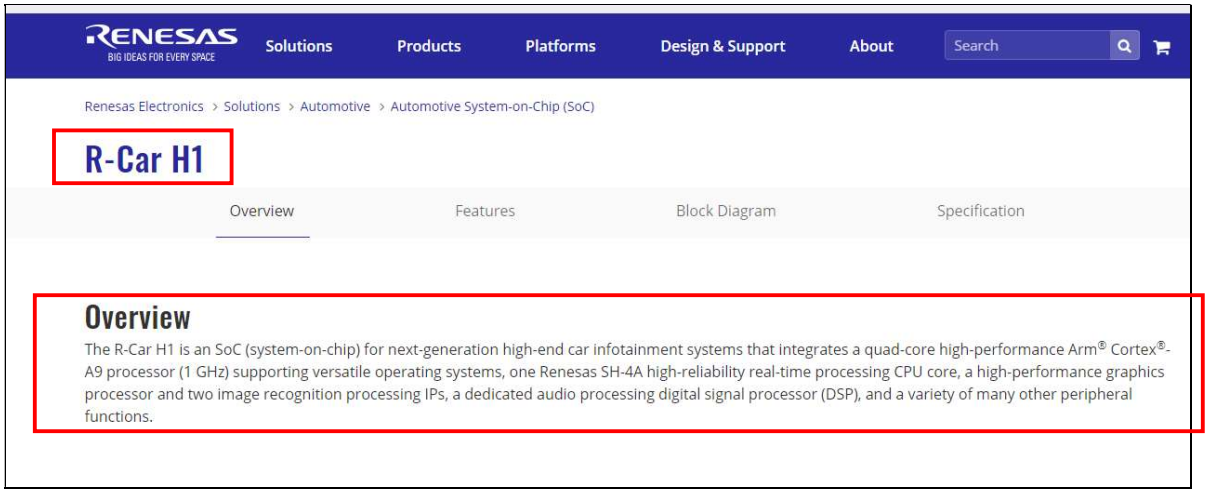
102. On information and belief, the Accused Instrumentalities infringe at least Claim 1 of the '526 Patent by providing and practicing a method for permuting two-dimensional (2-D) data in a programmable processor. For example, Defendants provide a system-on-chip (including but not limited to R-Car Hxx, R-Car Mxx, R-Car Exx, R-Car V3M, EMMA Mobile/EV2, R-Mobile A1, RZ/A1xx, RZ/A2M, RZ/G2xx, RZ/G1xx, GR-PEACH, GR-LYCHEE, emCON-RZ_G1x, and DIMM-RZ/A1H) solutions for parallel data processing.

103. For example, Defendants' R-Car H1 SoC (used herein as an exemplary product) is used for car infotainment systems. The R-Car H1 includes a quad-core Arm Cortex-A9 processor (1 GHz), a Renesas SH-4A real-time processing CPU core, a graphics processor and two image recognition processing IPs, and/or an audio processing digital signal processor (DSP).

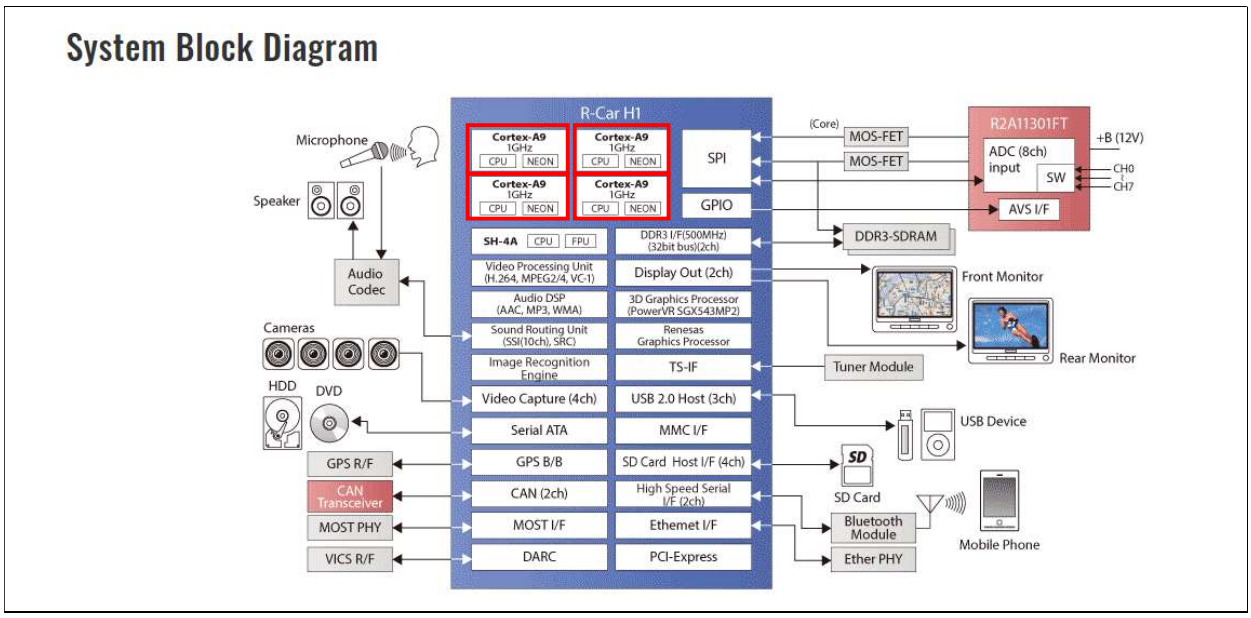
104. Further, the R-Car H1 SoC ("programmable processor") utilizes Arm Neon technology (an advanced Single Instruction Multiple Data (SIMD) architecture) for improving audio/video encoding and decoding, 2D/3D graphics ("two dimensional (2-D) data"), and/or image/video processing. ARM Neon SIMD architecture provides permutation instructions to rearrange individual elements present in 2D/3D graphics.

105. Further, on information and belief, Defendants directly infringe the claim at least when it tests its SoCs. During such tests, on information and belief, Defendants utilize the SoCs to perform permutation on the input data using permutation instructions available in ARM Neon SIMD ISA (Instruction Set Architecture).

106. Further, since at least the date of service of the Original Complaint in this matter, Defendants have and will indirectly infringe one or more claims of the '526 Patent at least when Defendants' customers (such as device manufacturers which use Defendants' SoCs in their products) perform the method while testing their devices and when the devices are operated as designed, intended, and instructed, by end-users.



Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.

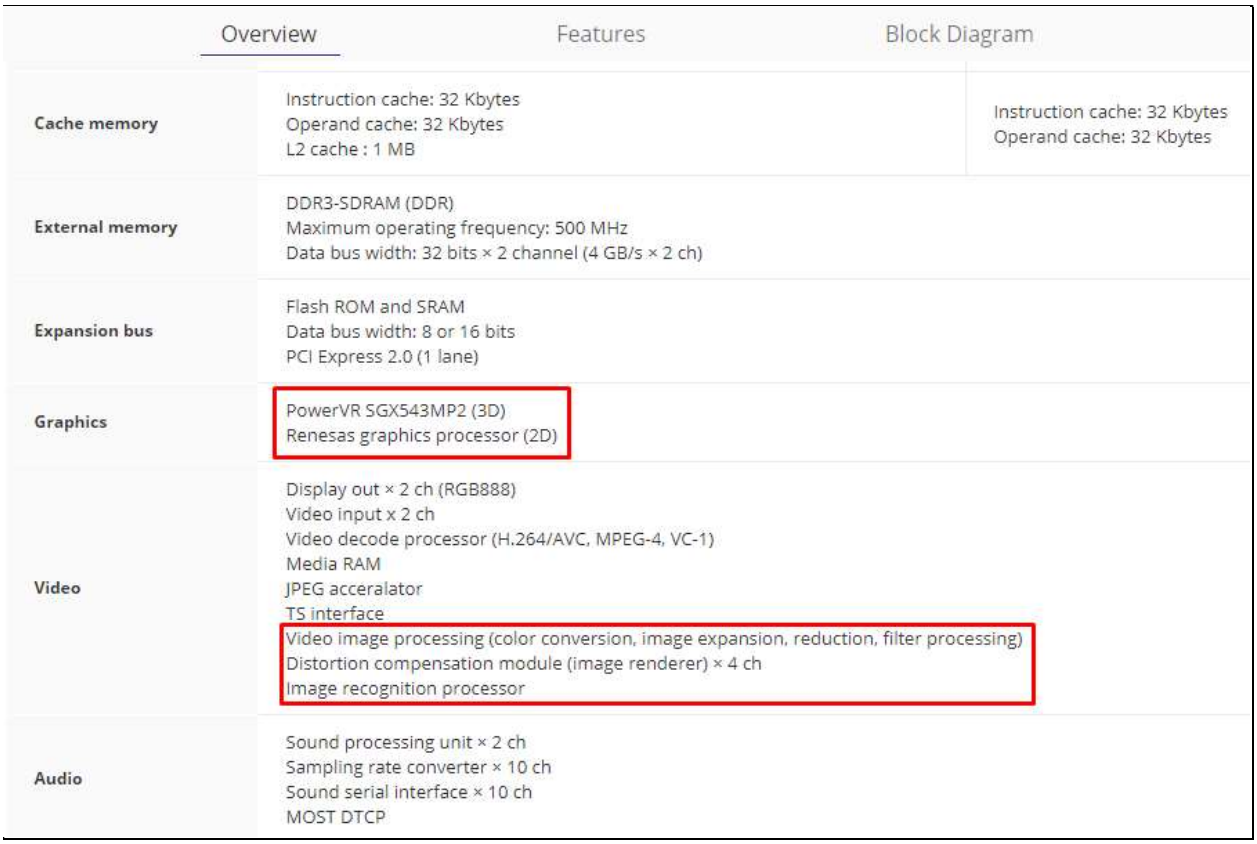


Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.

Specification

Item	R-Car H1 Specifications	
Product No.	R-Car H1 (R8A77790)	
Power supply voltage	3.3 V (IO), 1.5 V (DDR3), 1.2 V (Core), 2.5 V (PCIe, MLB), 1.8 V (SDIF UHS-I)	
CPU core	Arm® Cortex®-A9 Quad (with NEON™)	SH-4A core
Maximum operating frequency	1000 MHz	800 MHz
Processing performance	10000 DMIPS	1760DMIPS(Effective), 5600MFLOP
Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes

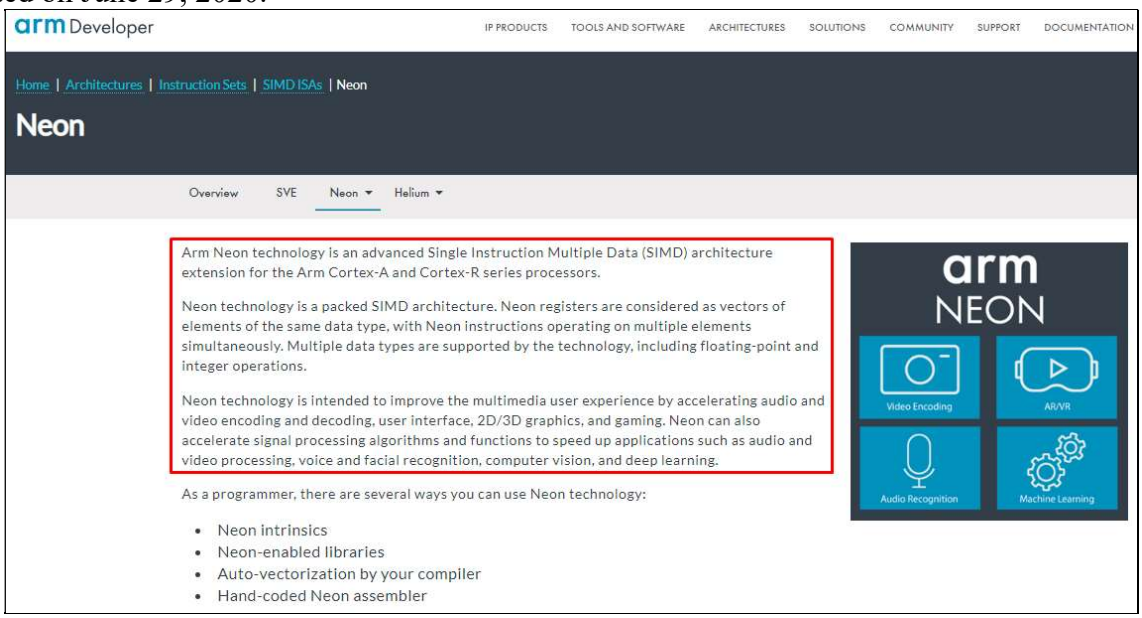
Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



Overview | Features | Block Diagram

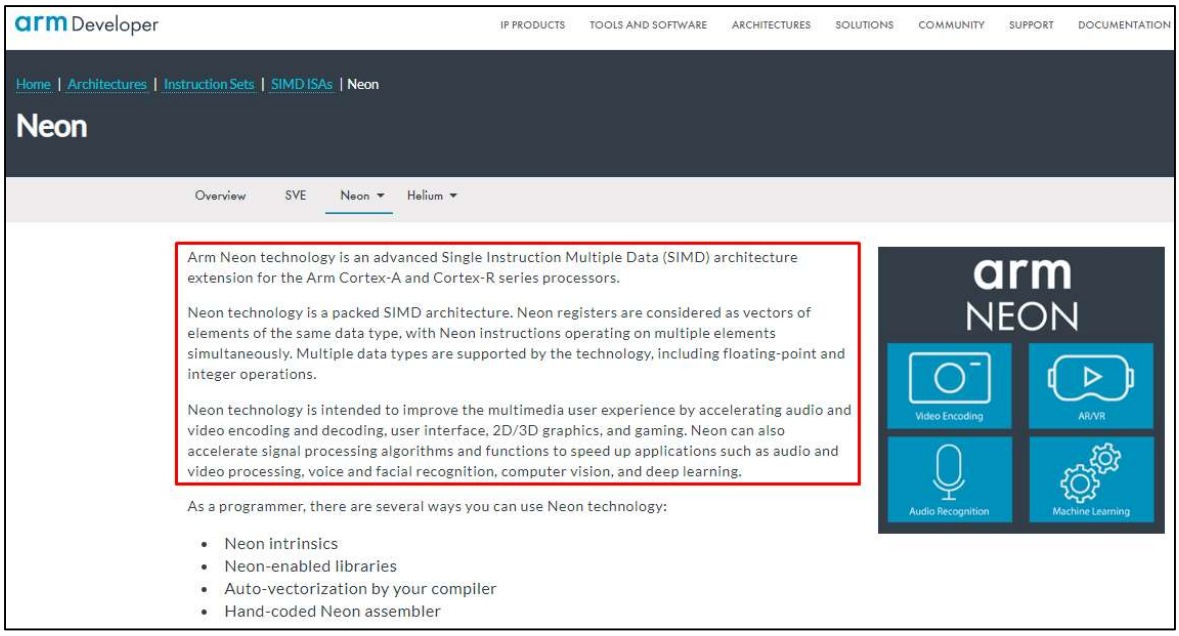
Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes
External memory	DDR3-SDRAM (DDR) Maximum operating frequency: 500 MHz Data bus width: 32 bits × 2 channel (4 GB/s × 2 ch)	
Expansion bus	Flash ROM and SRAM Data bus width: 8 or 16 bits PCI Express 2.0 (1 lane)	
Graphics	PowerVR SGX543MP2 (3D) Renesas graphics processor (2D)	
Video	Display out × 2 ch (RGB888) Video input x 2 ch Video decode processor (H.264/AVC, MPEG-4, VC-1) Media RAM JPEG acceralator TS interface Video image processing (color conversion, image expansion, reduction, filter processing) Distortion compensation module (image renderer) × 4 ch Image recognition processor	
Audio	Sound processing unit × 2 ch Sampling rate converter × 10 ch Sound serial interface × 10 ch MOST DTCP	

Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.

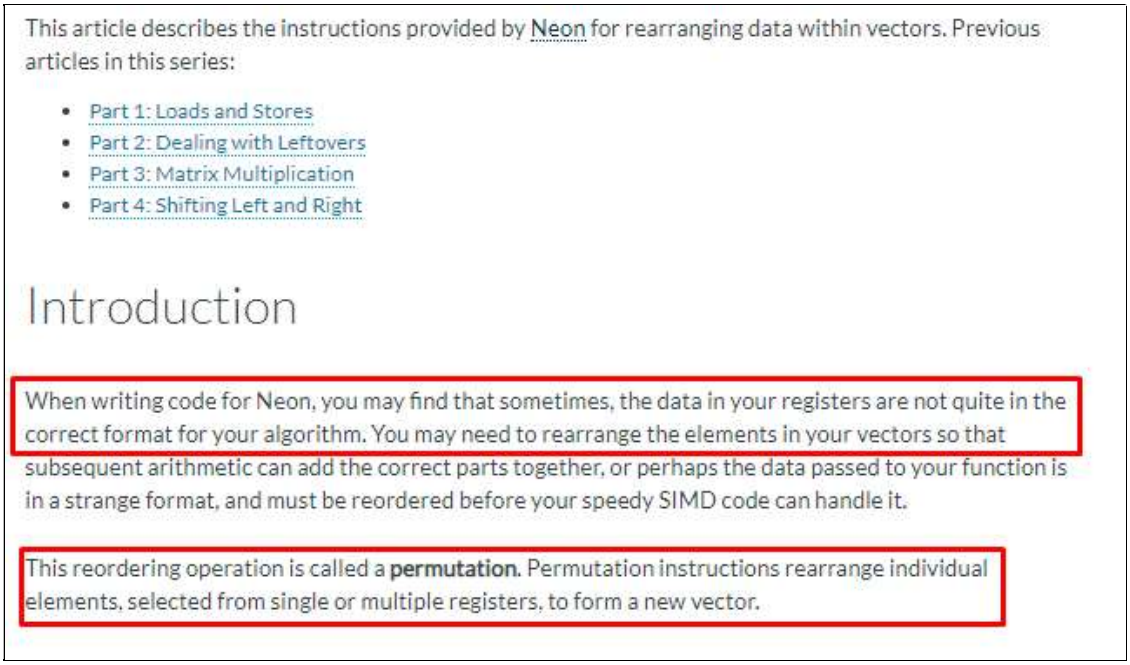


Source: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon, as visited on

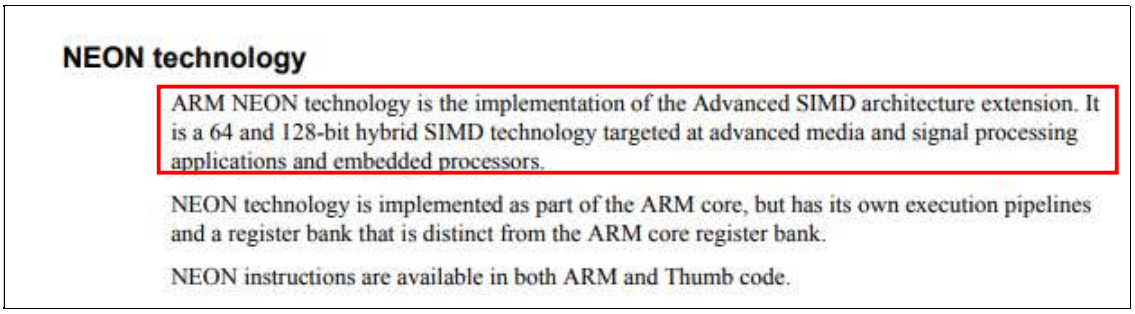
June 29, 2020.



Source: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon, as visited on June 29, 2020.



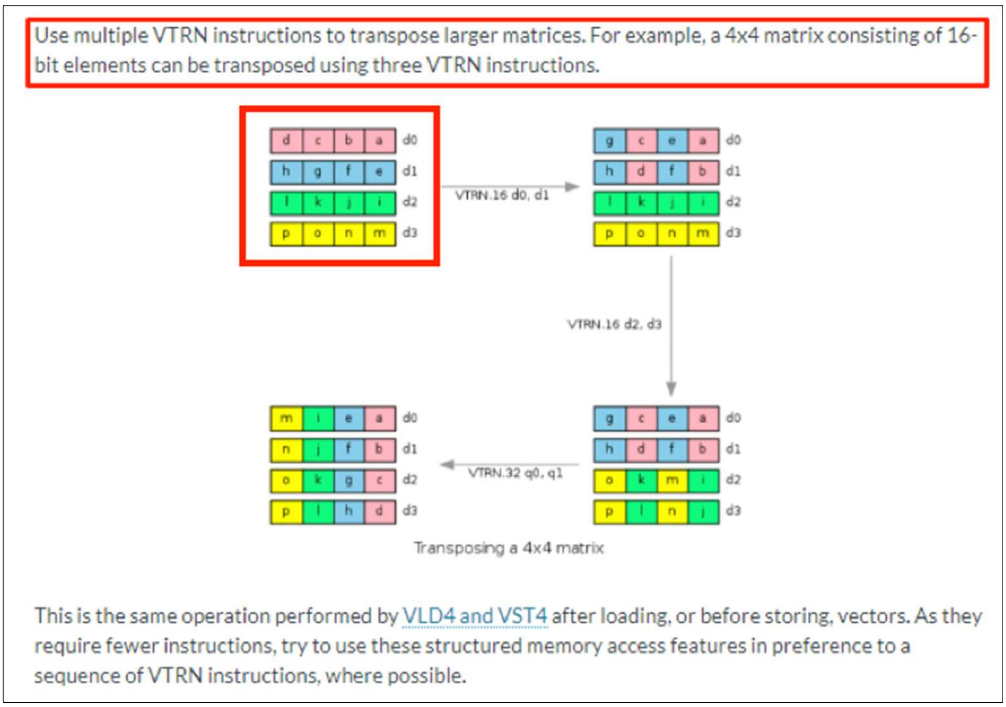
Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



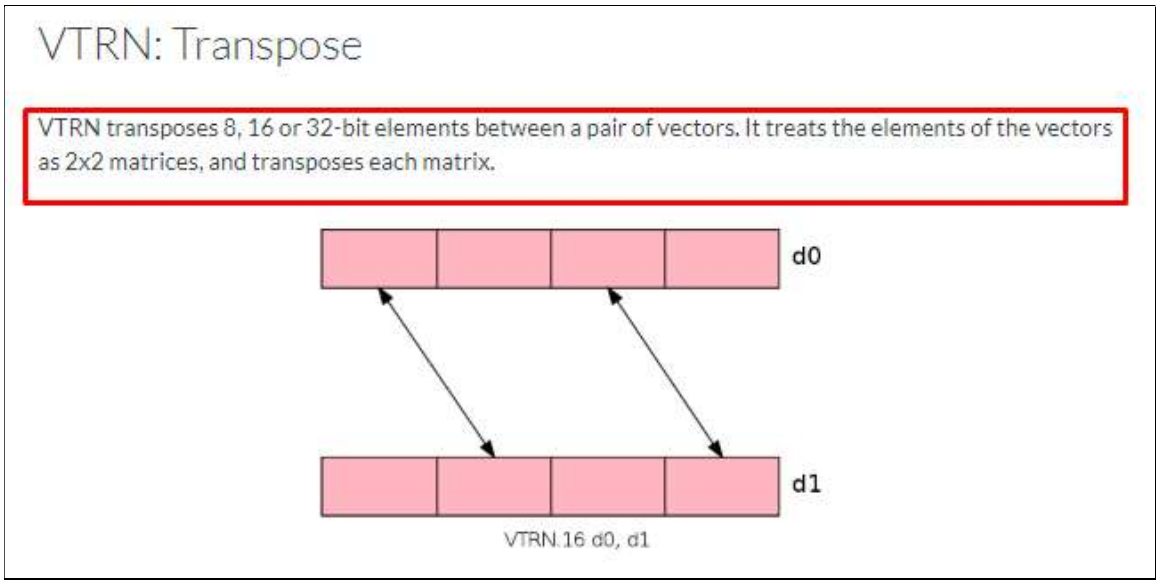
Source: http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 40, as visited on June 29, 2020.

107. Further, Defendants perform and have or will induce others to perform the step of decomposing said two-dimensional data into at least one atomic element said two dimensional data being located in at least one source register said at least one atomic element of said two dimensional data is a 2×2 matrix and said two dimensional data is decomposed into data elements in said matrix.

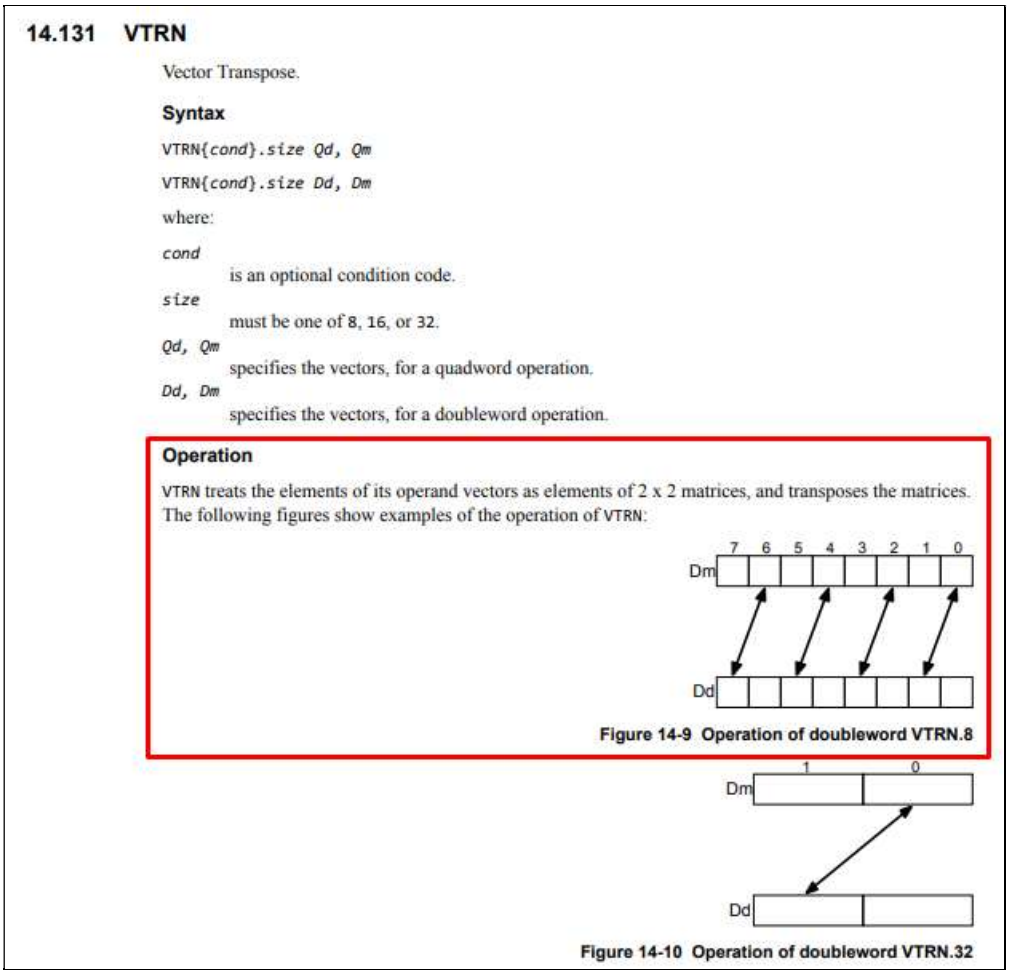
108. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and decomposes two-dimensional data (in the form of 4x4 matrix) into a 2x2 matrix. The 4x4 matrix consists of 16-bit elements ("atomic element"). The permutation instruction transposes 8, 16 or 32-bit elements between a pair of vectors. The permutation instruction is applied on the elements of the vectors by dividing it into 2x2 matrices. The two dimensional data is stored in at least one of the d0 and d1 vectors ("source registers").



Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



14.131 VTRN

Vector Transpose.

Syntax

`VTRN{cond}.size Qd, Qm`

`VTRN{cond}.size Dd, Dm`

where:

cond
is an optional condition code.

size
must be one of 8, 16, or 32.

Qd, Qm
specifies the vectors, for a quadword operation.

Dd, Dm
specifies the vectors, for a doubleword operation.

Operation

VTRN treats the elements of its operand vectors as elements of 2 x 2 matrices, and transposes the matrices. The following figures show examples of the operation of VTRN:

Figure 14-9 Operation of doubleword VTRN.8

Figure 14-10 Operation of doubleword VTRN.32

Source:
http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 734, as visited on June 29, 2020.

109. Further, Defendants perform and have or will induce others to perform the step of determining at least one permutation instruction for rearrangement of said data in said atomic element.

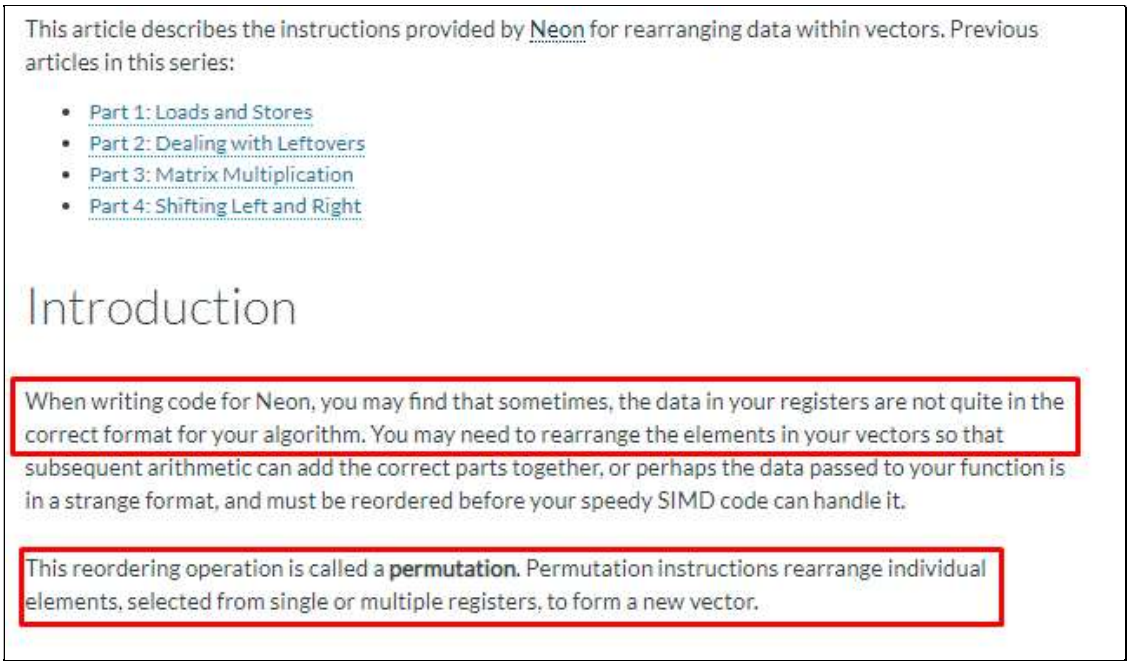
110. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and decomposes two-dimensional data (in the form of 4x4 matrix) into a 2x2 matrix. The permutation instruction transposes ("rearrangement") 8, 16 or 32-bit elements between a pair of vectors. The permutation instruction is applied on the elements of the vectors by dividing it into 2x2 matrices.

111. Further, Defendants perform and have or will induce others to perform the step of said data elements being rearranged by said at least one permutation instruction, each of said data elements representing a subword having one or more bits.

112. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and transposes ("rearrange") 8, 16 or 32- bit elements ("subwords") of the 2x2 matrix. The permutation instruction performs subword permutation on each element.

113. Further, Defendants perform and have or will induce others to perform the step of applying said permutation instructions to said subwords and placing said permutated subwords into a destination register.

114. For example, the R-Car H1 SoC uses a permutation instruction (such as a VTRN instruction) and transposes 2x2 matrix elements to form a new vector ("placing said permutated subword into a destination register").



This article describes the instructions provided by Neon for rearranging data within vectors. Previous articles in this series:

- Part 1: Loads and Stores
- Part 2: Dealing with Leftovers
- Part 3: Matrix Multiplication
- Part 4: Shifting Left and Right

Introduction

When writing code for Neon, you may find that sometimes, the data in your registers are not quite in the correct format for your algorithm. You may need to rearrange the elements in your vectors so that subsequent arithmetic can add the correct parts together, or perhaps the data passed to your function is in a strange format, and must be reordered before your speedy SIMD code can handle it.

This reordering operation is called a **permutation**. Permutation instructions rearrange individual elements, selected from single or multiple registers, to form a new vector.

Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.

115. Teleputers has been damaged by Defendants' infringement of the '526 Patent.

COUNT II
(Infringement of U.S. Patent No. 6,952,478B2)

116. Teleputers incorporates the above paragraphs by reference.

117. Defendants have been on notice of the '478 Patent at least as early as the date it received service of this Original Complaint.

118. On information and belief, Defendants have infringed and continue to infringe the '478 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

119. On information and belief, Defendants, at least as of the date of service of the Original Complaint in this matter, and with knowledge of the '478 Patent, indirectly infringe the '478 Patent by inducing others to infringe the '478 Patent. In particular, Defendants have or will intend to induce customers to infringe the '478 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

120. On information and belief, Defendants also have or will induce others, including customers, to infringe the '478 Patent by providing technical support for the use of the Accused Instrumentalities.

121. On information and belief, at all times Defendants own and control the operation of the Accused Instrumentalities in accordance with an end user license agreement.

122. On information and belief, the Accused Instrumentalities necessarily infringe one or more claims of the '478 Patent when used as intended.

123. On information and belief, the Accused Instrumentalities infringe the '478 Patent by providing and practicing a method for performing an arbitrary permutation of a source sequence of bits by defining an intermediate sequence of bits. For example, Defendants infringe at least Claim 1 of the '478 Patent using a permutation instruction, the source sequence of bits are

transformed into intermediate sequence of bits. This is repeated using the intermediate sequence of bits as source sequence of bits until a desired sequence of bits is obtained and the permutation instructions form a sequence of instructions. For example, Defendants provide system-on-chip (including but not limited to R-Car Hxx, R-Car Mxx, R-Car Exx, R-Car V3M, EMMA Mobile/EV2, R-Mobile A1, RZ/A1xx, RZ/A2M, RZ/G2xx, RZ/G1xx, GR-PEACH, GR-LYCHEE, emCON-RZ_G1x, and DIMM-RZ/A1H) solutions for parallel data processing.

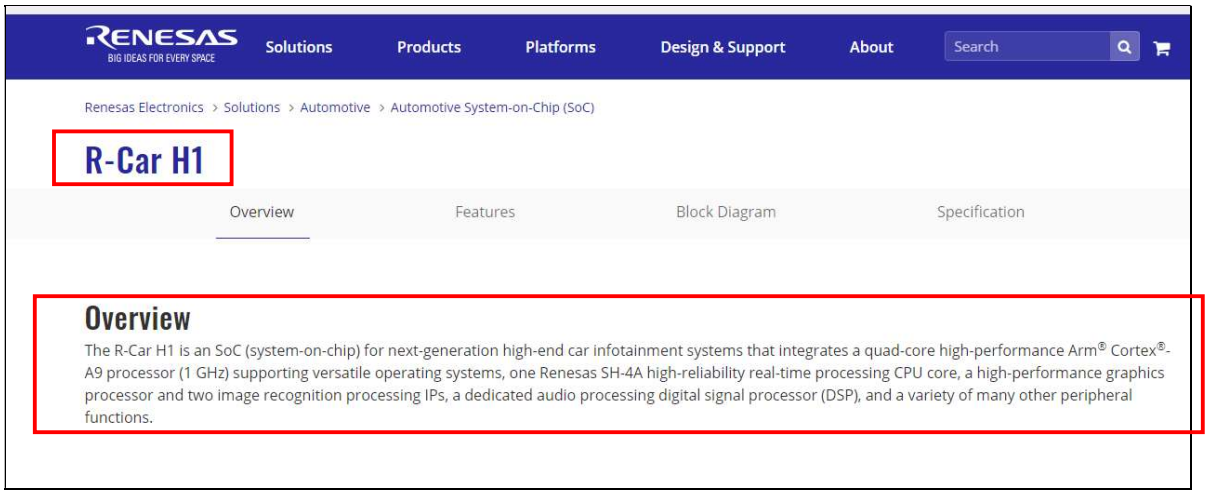
124. For example, Defendants' R-Car H1 SoC (used herein as an exemplary product) is used for car infotainment systems. The R-Car H1 includes a quad-core Arm Cortex-A9 processor (1 GHz), a Renesas SH-4A real-time processing CPU core, a graphics processor and two image recognition processing IPs, and/or an audio processing digital signal processor (DSP).

125. Further, the R-Car H1 SoC ("programmable processor") utilizes Arm Neon technology (an advanced Single Instruction Multiple Data (SIMD) architecture) for improving audio/video encoding and decoding, 2D/3D graphics ("source sequence of bits"), and/or image/video processing. ARM Neon SIMD architecture provides permutation instructions to rearrange individual elements present in 2D/3D graphics.

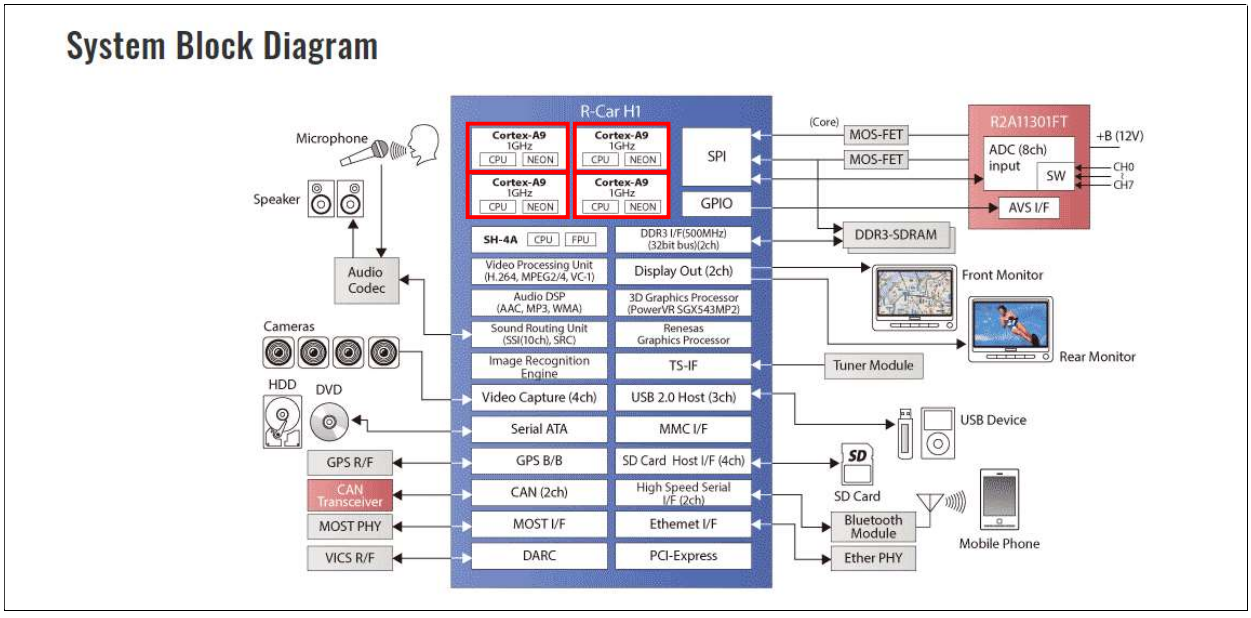
126. Further, on information and belief, Defendants directly infringe the claim at least when it tests its SoCs. During such tests, Defendants utilize the SoCs to perform permutation on the input data using permutation instructions available in ARM Neon SIMD ISA (Instruction Set Architecture).

127. Further, Defendants directly infringe the claim at least when they test their SoCs. During such tests, on information and belief, Defendants utilize the SoCs to perform permutation on the input data using permutation instructions available in ARM Neon SIMD ISA (Instruction Set Architecture).

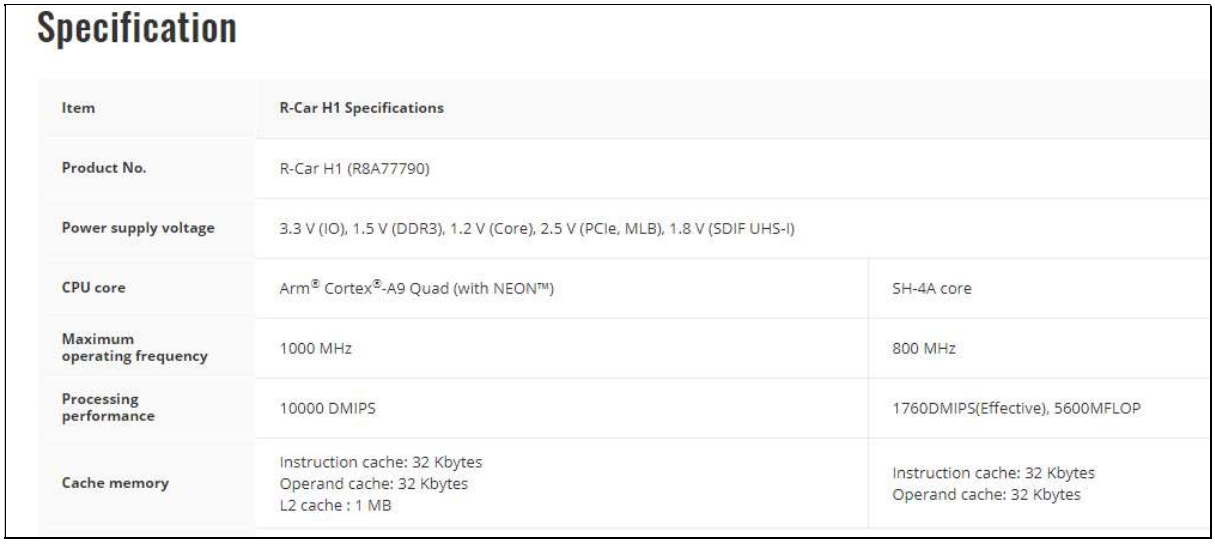
128. Further, since at least the date of service of the Original Complaint in this matter, Defendants have and will indirectly infringe one or more claims of the '478 Patent at least when Defendants' customers (such as device manufacturers which use Defendants' SoCs in their products) perform the method while testing their devices and when the devices are operated as designed, intended, and instructed, by end-users.



Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



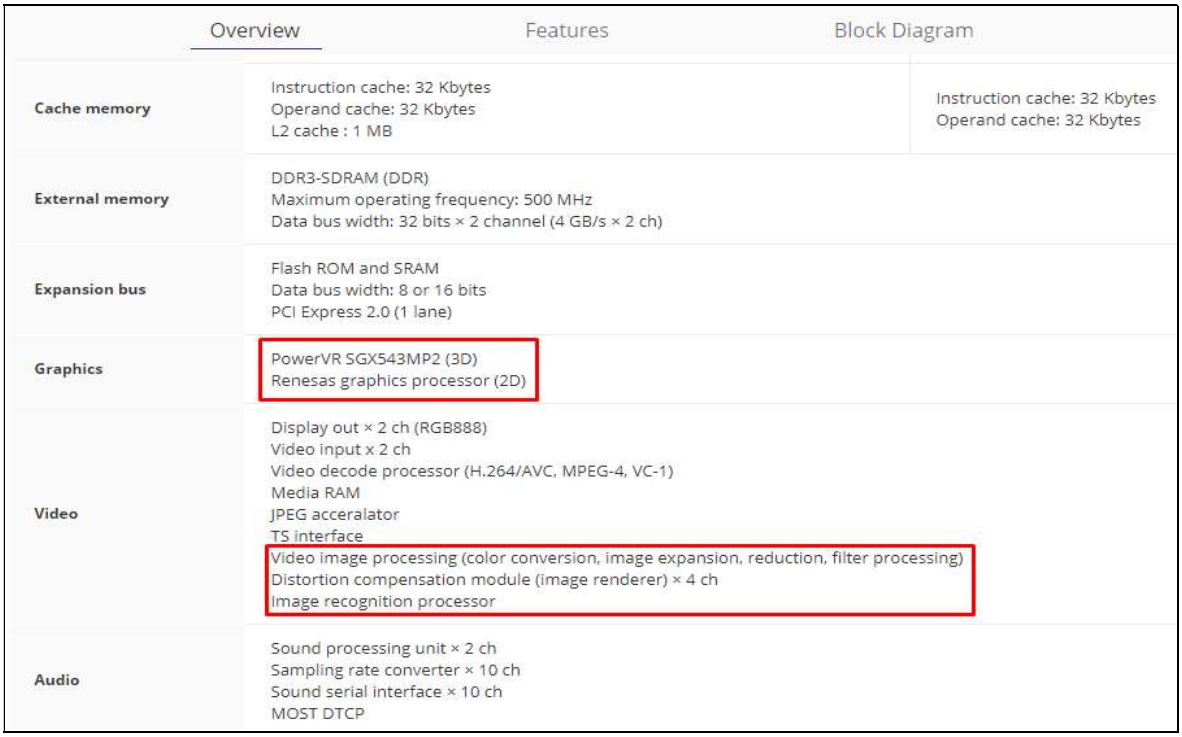
Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.



Specification

Item	R-Car H1 Specifications	
Product No.	R-Car H1 (R8A77790)	
Power supply voltage	3.3 V (IO), 1.5 V (DDR3), 1.2 V (Core), 2.5 V (PCIe, MLB), 1.8 V (SDIF UHS-I)	
CPU core	Arm® Cortex®-A9 Quad (with NEON™)	SH-4A core
Maximum operating frequency	1000 MHz	800 MHz
Processing performance	10000 DMIPS	1760DMIPS(Effective), 5600MFLOP
Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes

Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as visited on June 29, 2020.

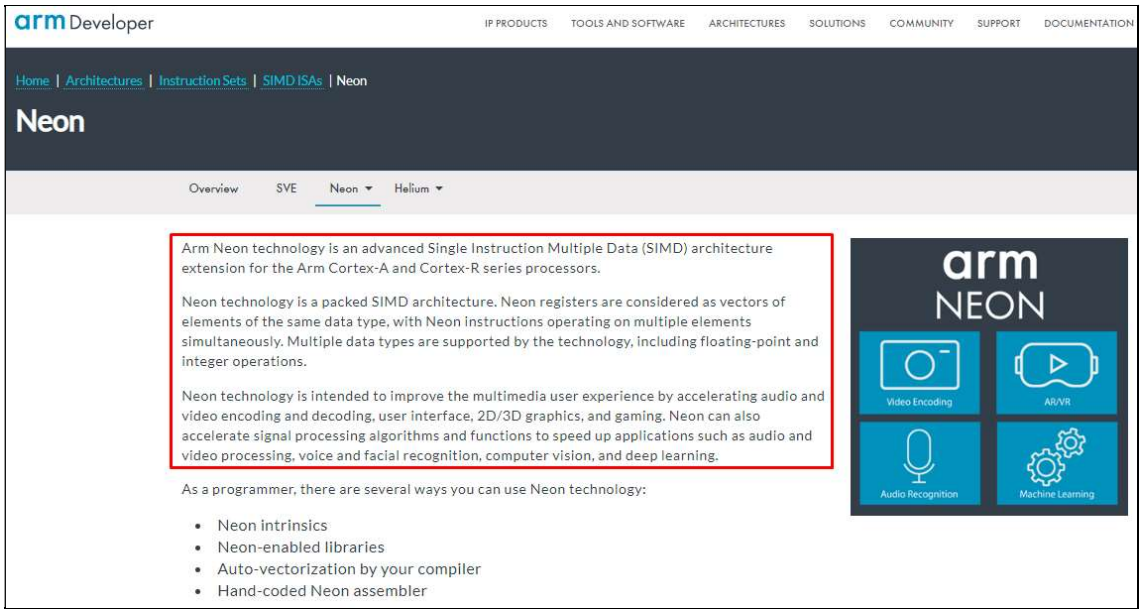


Overview Features Block Diagram

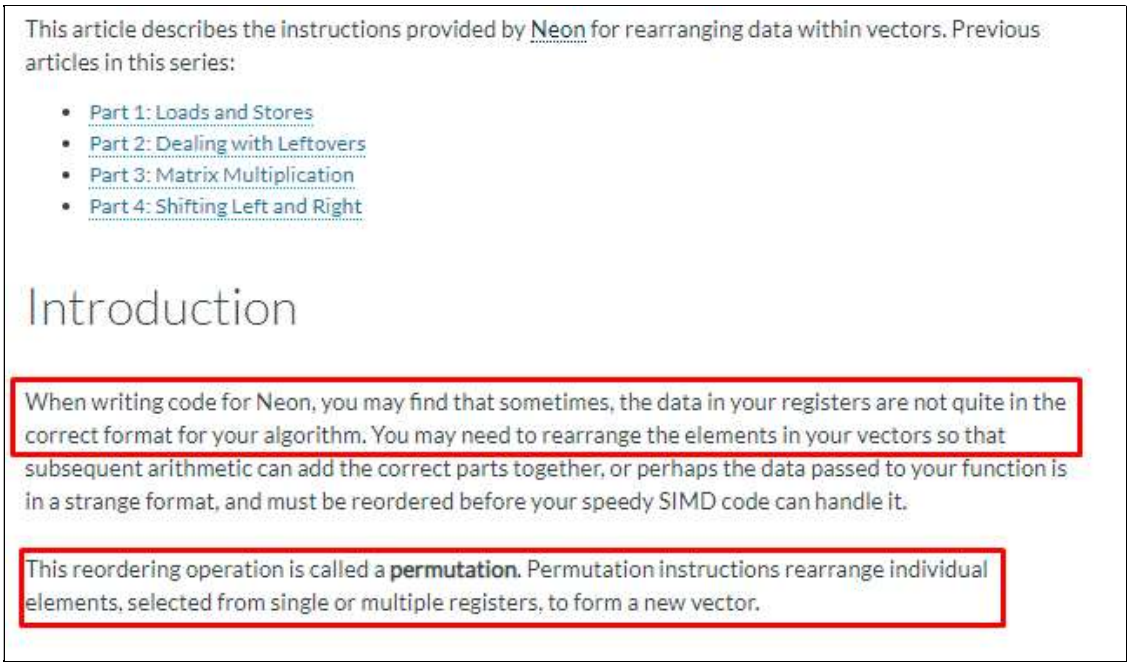
Cache memory	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes L2 cache : 1 MB	Instruction cache: 32 Kbytes Operand cache: 32 Kbytes
External memory	DDR3-SDRAM (DDR) Maximum operating frequency: 500 MHz Data bus width: 32 bits × 2 channel (4 GB/s × 2 ch)	
Expansion bus	Flash ROM and SRAM Data bus width: 8 or 16 bits PCI Express 2.0 (1 lane)	
Graphics	PowerVR SGX543MP2 (3D) Renesas graphics processor (2D)	
Video	Display out × 2 ch (RGB888) Video input x 2 ch Video decode processor (H.264/AVC, MPEG-4, VC-1) Media RAM JPEG acceralator TS interface Video image processing (color conversion, image expansion, reduction, filter processing) Distortion compensation module (image renderer) × 4 ch Image recognition processor	
Audio	Sound processing unit × 2 ch Sampling rate converter × 10 ch Sound serial interface × 10 ch MOST DTCP	

Source: https://www.renesas.com/us/en/solutions/automotive/soc/r-car-h1.html#overview, as

visited on June 29, 2020.

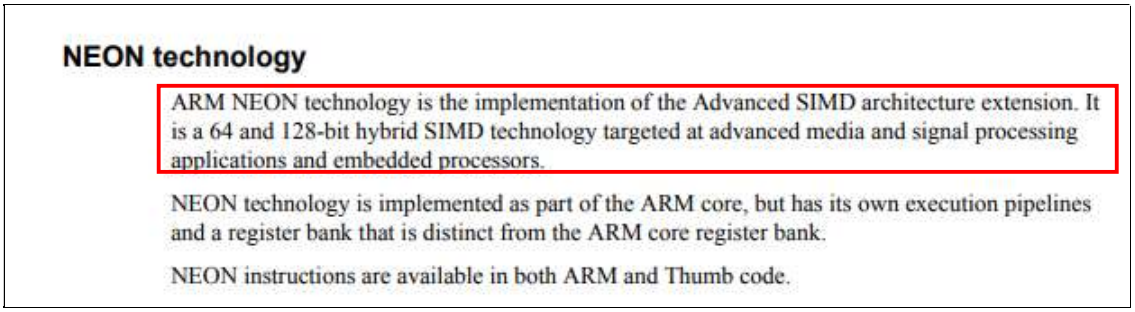


Source: https://developer.arm.com/architectures/instruction-sets/simd-isas/neon, as visited on June 29, 2020.



Source: https://community.arm.com/developer/ip-products/processors/b/processors-ip-

blog/posts/coding-for-neon---part-5-rearranging-vectors, as visited on June 29, 2020.



NEON technology

ARM NEON technology is the implementation of the Advanced SIMD architecture extension. It is a 64 and 128-bit hybrid SIMD technology targeted at advanced media and signal processing applications and embedded processors.

NEON technology is implemented as part of the ARM core, but has its own execution pipelines and a register bank that is distinct from the ARM core register bank.

NEON instructions are available in both ARM and Thumb code.

Source:

http://infocenter.arm.com/help/topic/com.arm.doc.dui0473j/DUI0473J_armasm_user_guide.pdf, page 40, as visited on June 29, 2020.

129. Teleputers has been damaged by Defendants' infringement of the '478 Patent.

PRAYER FOR RELIEF

WHEREFORE, Teleputers respectfully requests the Court enter judgment against Defendants:

1. declaring that the Defendants have infringed each of the Patents-in-Suit;

2. awarding Teleputers its damages suffered as a result of Defendants' infringement of the Patents-in-Suit;

3. awarding Teleputers its costs, attorneys' fees, expenses, and interest;

4. awarding Teleputers ongoing post-trial royalties; and

5. granting Teleputers such further relief as the Court finds appropriate.

JURY DEMAND

Teleputers demands trial by jury, under Fed. R. Civ. P. 38.

Dated: September 24, 2020

Respectfully Submitted

/s/ M. Scott Fuller

M. Scott Fuller
Texas Bar No. 24036607
sfuller@ghiplaw.com
Thomas G. Fasone III
Texas Bar No. 00785382
tfasone@ghiplaw.com
GARTEISER HONEA, PLLC
119 W. Ferguson Street
Tyler, Texas 75702
Telephone: (903) 705-7420
Facsimile: (888) 908-4400

Raymond W. Mort, III
Texas State Bar No. 00791308
raymort@austinlaw.com
THE MORT LAW FIRM, PLLC
100 Congress Ave, Suite 2000
Austin, Texas 78701
Tel/Fax: (512) 865-7950

ATTORNEYS FOR PLAINTIFF TELEPUTERS LLC