**UNITED STATES DISTRICT COURT**
**FOR THE WESTERN DISTRICT OF TEXAS**
**WACO DIVISION**

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| TELEPUTERS, LLC,<br><br>Plaintiff<br><br>v.<br><br>ORACLE CORPORATION AND SUN MICROSYSTEMS, INC.,<br><br>Defendants | **Case No. 6:20-cv-00600**<br><br>**JURY TRIAL DEMANDED** |

**FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff Teleputers, LLC ("Plaintiff" or "Teleputers") hereby files this First Amended Complaint for Patent Infringement against Defendant Oracle Corporation and Sun Microsystems, Inc. (collectively "Defendants" or "Defendant" or collectively as "Oracle"), and alleges, on information and belief, as follows:

**THE PARTIES**

1. Teleputers, LLC is a limited liability company organized and existing under the laws of the State of New Jersey with its principal place of business in Princeton, New Jersey.

2. On information and belief, Defendant Oracle Corporation is a California corporation with its principal place of business at 500 Oracle Parkway, Redwood Shores, California 94065. Oracle Corporation may be served through its registered agent, Corporation Service Company d/b/a CSC – Lawyers Incorporating Service Company, 211 East 7th Street, Suite 620, Austin, Texas 78701.

3. On information and belief, Defendant Sun Microsystems, Inc. was a California corporation and was acquired by Oracle Corporation in January 2010 for $7.4 Billon. Sun Microsystems, Inc. may be served through its current parent/owner, Oracle Corporation.

## JURISDICTION AND VENUE

4. This action arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. Defendants have committed acts of infringement in this judicial district.

6. On information and belief, Defendants maintain regular and systematic business interests in this district and throughout the State of Texas including through their representatives, employees and physical facilities.

7. On information and belief, the Court has personal jurisdiction over Defendants because Defendants have committed, and continue to commit, acts of infringement in the State of Texas, have conducted business in the State of Texas, and/or have engaged in continuous and systematic activities in the State of Texas. On information and belief, Defendants' accused instrumentalities that are alleged herein to infringe were and continue to be used, imported, offered for sale, and/or sold in the Western District of Texas.

8. On information and belief, Defendants voluntarily conduct business and solicit customers in the State of Texas and within this District, including, but not limited to, its offices located at 2300 Cloud Way, Austin, Texas 78741.

| Austin | Austin | Frisco | Houston |
|---|---|---|---|
| 2300 Oracle Way | 5300 Riata Park | 7460 Warren | Two Allen Center |
| Austin, TX 78741<br>Phone: | Court<br>Building B | Parkway<br>Suite 300 | 1200 Smith St.<br>Suite 1500 |

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|---|---|---|---|
| +1.737.867.1000 | Austin, TX 78727<br>Phone:<br>+1.512.401.1000<br><br>Fax:<br>+1.512.401.1001 | Frisco, TX<br>75034<br>Phone:<br>+1.972.963.2300<br><br>Fax:<br>+1.972.963.2301 | Houston, TX<br>77002 Phone:<br>+1.713.654.0919<br><br>Fax:<br>+1.713.654.8743 |

Source: Oracle website https://www.oracle.com/corporate/contact/field-offices.html, as visited on June 23, 2020.

9. Defendants also have engineers and actively recruit for employees to work in Austin, Texas.

> Oracle today announced the opening of the Oracle Startup Cloud Accelerator in Austin, Texas, the global program's first U.S. location and part of the Oracle Global Startup Ecosystem. The new accelerator provides statewide startups with access to a network of more than 430,000 Oracle customers, technical and business mentors, state-of-the art technology, co-working space at Capital Factory, introductions to partners, talent, and investors, and free Oracle Cloud credits. In addition to local expertise, the program offers an ever-expanding global community of startup peers and program alumni.

Source: Oracle website https://www.oracle.com/corporate/pressrelease/expanded-oracle-accelerator-gives-texas-startups-a-boost-062218.html, as visited on June 22, 2020.

10. On information and belief, Defendants generate substantial revenue within this District and from the acts of infringement as carried out in this District. As such, the exercise of jurisdiction over Defendants would not offend the traditional notions of fair play and substantial justice.

11. Venue is proper in the Western District of Texas pursuant to 28 U.S.C. § 1400(b).

## NOTICE OF TELEPUTERS' PATENTS

12. Teleputers is owner by assignment of U.S. Patent No. 6,922,472 ("the '472 Patent") entitled "Method and system for performing permutations using permutation instructions based on butterfly networks." A copy may be obtained at:

https://patents.google.com/patent/US6922472B2/en.

13. Teleputers is owner by assignment of U.S. Patent No. 6,952,478B2 ("the '478 Patent") entitled "Method and system for performing permutations using permutation instructions based on modified omega and flip stages." A copy may be obtained at:

https://patents.google.com/patent/US6952478B2/en.

14. Teleputers is owner by assignment of U.S. Patent No. 7,092,526B2 ("the '526 Patent") entitled "Method and system for performing subword permutation instructions for use in two-dimensional multimedia processing." A copy may be obtained at:

https://patents.google.com/patent/US7092526B2/en.

15. Teleputers is owner by assignment of U.S. Patent No. 7,174,014B2 ("the '014 Patent" and "the Patents-in-Suit") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at:

https://patents.google.com/patent/US7174014B2/en.

16. Teleputers is owner by assignment of U.S. Patent No. 7,519,795B2 ("the '795 Patent") entitled "Method and system for performing permutations with bit permutation instructions." A copy may be obtained at:

https://patents.google.com/patent/US7519795B2/en.

17. The foregoing Patents, namely the '014 Patent, the '526 Patent, the '478 Patent, the '472 Patent, and the '795 Patent are collectively referred to as "the Teleputers Patents."

18. Teleputers is the owner of all right, title, and interest in each of the Teleputers Patents. None of the Teleputers Patents, nor any of the claimed subject matter in any such Teleputers Patents, has been otherwise assigned to any person or entity other than Teleputers. Teleputers therefore has complete and unfettered standing to assert and seek money damages for the infringement of each and every one of the Teleputers Patents.

19. No entity other than Teleputers presently claims any ownership interest, valid or otherwise, in any of the Teleputers Patents. Teleputers possesses full legal title to each of the Teleputers Patents.

20. The records at the United States Patent and Trademark Office indicate duly recorded assignments of the Teleputers Patents from the inventors (Lee, Shi, Yang, and/or Vachharajani) to Teleputers, LLC, executed on February 14, 2005. No other assignments of interest in any Teleputers Patent have been recorded with the United States Patent and Trademark Office, and no such assignments exist. Indeed, the face of each Teleputers Patent properly identifies Teleputers LLC as the legal assignee. As such, because each of the Teleputers Patents were issued to the inventors, and because the inventors assigned the Teleputers Patents to Teleputers LLC and filed copies of such assignments with the Patent and Trademark Office, Plaintiff presumptively has proper standing to bring these causes of action. By operation of law, legal title vests in the inventors, and passes to another only by way of assignment or effective legal transfer.

21. To the extent Princeton University possessed any rights whatsoever in any Teleputers Patent, such rights were equitable in nature and non-exclusive to the rights of the inventors. The Verified Statement Claiming Small Entity Status (dated March 5, 2000) in the certain Provisional Patent Application Number 60/202,250 states only that certain unidentified "rights under contract or law" were, at the time, allegedly possessed by The Trustees of Princeton University. The

Verified Statement further made clear that the named inventors possessed legal rights to the inventions. At best, such rights possessed by Princeton were equitable, and were in any event limited to the *inventions*, not to the issued *patents*. Further, the written policies of Princeton University relating to inventions (*see* https://dof.princeton.edu/policies-procedure/policies/patents) expressly call for the outright assignment of inventions to the inventors or the transfer of the inventions to a patent management company. Having not transferred any of the Teleputers Patents to any patent management company, the historical actions of Princeton reflect an abandonment of equitable rights and an assignment of all rights (equitable and legal) to the inventors. Stated differently, the conduct of the parties (Princeton and the inventors) evidences an abandonment of rights on the part of Princeton, and full equitable and legal title in the inventors. In any event, the "rights" allegedly possessed by Princeton in the '250 Application do not carry over to the inventions described and claimed in the Teleputers Patents.

22. The Teleputers Patents are valid, enforceable, and were duly issued in full compliance with Title 35 of the United States Code.

23. Defendants, at least by the date of this Original Complaint, are on notice of the Teleputers Patents.

24. Each of the aforementioned Teleputers Patents are directed to, and claim, patent eligible subject matter, and each is presumed to be valid and patent-eligible.

25. The '472 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. The permute instructions are based on a Benes network comprising two butterfly networks of the same size connected back-to-back. Intermediate sequences of bits are defined that an initial sequence of bits

from a source register are transformed into. Each intermediate sequence of bits is used as input to a subsequent permutation instruction. Permutation instructions are determined for permitting the initial source sequence of bits into one or more intermediate sequence of bits until a desired sequence is obtained. The intermediate sequences of bits are determined by configuration bits. The permutation instructions form a permutation instruction sequence of at least one instruction. At most 21 gr/m permutation instructions are used in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted, and m is the number of network stages executed in one instruction. The permutation instructions can be used to permute k-bit subwords packed into an n-bit word, where k can be 1, 2, . . . , or n bits, and k*r=n. *See* Abstract, '472 Patent.

26. The claims of the '472 Patent claim priority to at least May 5, 2000.

27. The claims of the '472 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

28. Further, the claims of the '472 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

29. Further, the claims of the '472 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '472 Patent at 1:17-3:15.

30. For example, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform

arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '472 Patent at 3:17-21.

31. Further, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '472 Patent at 3:24-37.

32. Further, the claims of the '472 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '472 Patent at 3:42-47.

33. The foregoing improvements and technological solutions, as captured in the claims of the '472 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

34. Further, the claims of the '472 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

35. Consequently, the claims of the '472 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

36. The '472 Patent was examined by Primary United States Patent Examiner Gilberto Barron, Jr, with Assistant Examiner Grigory Gurshman. During the examination of the '472 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/37, 28, 1.

37. After conducting a search for prior art during the examination of the '472 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art

references found during the search: (i) US5495476A; (ii) US5546393A; (iii) US6381690B1; (iv) US6446198B1; (v) US6629115B1; (vi) US6108311A; and (vii) US5940389A.

38. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '472 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

39. The '478 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. The permute instructions are based on an omega-flip network comprising at least two stages in which each stage can perform the function of either an omega network stage or a flip network stage. Intermediate sequences of bits are defined that an initial sequence of bits from a source register are transformed into. Each intermediate sequence of bits is used as input to a subsequent permutation instruction. Permutation instructions are determined for permuting the initial source sequence of bits into one or more intermediate sequence of bits until a desired sequence is obtained. The intermediate sequences of bits are determined by configuration bits. The permutation instructions form a permutation instruction sequence, of at least one instruction. At most 21 gr/m permutation instructions are used in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted, and m is the number of network stages executed in one instruction. The

permutation instructions can be used to permute k-bit subwords packed into an n-bit word, where k can be 1, 2, . . . , or n bits, and k*r=n. *See* Abstract, '478 Patent.

40. The claims of the '478 Patent claim priority to at least May 5, 2000.

41. The claims of the '478 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

42. Further, the claims of the '478 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

43. Further, the claims of the '478 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '478 Patent at 1:17-3:15.

44. For example, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '478 Patent at 3:17-21.

45. Further, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '478 Patent at 3:24-37.

46. Further, the claims of the '478 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors

which can be efficient for both cryptography and multimedia software. *See* '478 Patent at 3:42-47.

47. The foregoing improvements and technological solutions, as captured in the claims of the '478 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

48. Further, the claims of the '478 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

49. Consequently, the claims of the '478 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

50. The '478 Patent was examined by Primary United States Patent Examiner Thomas Peeso, with Assistant Examiner Grigory Gurshman. During the examination of the '478 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/37, 28, 1, 380/26.

51. After conducting a search for prior art during the examination of the '478 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US5495476A; (ii) US5546393A; (iii) US6381690B1; (iv) US6446198B1; and (v) US6629115B1.

52. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '478 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further

presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

53. The '526 Patent relates generally to methods and systems for providing provides a set of permutation primitives for current and future 2-D multimedia programs which are based on decomposing images and objects into atomic units, then finding the permutations desired for the atomic units. The subword permutation instructions for these 2-D building blocks are also defined for larger subword sizes at successively higher hierarchical levels. The atomic unit can be a 2×2 matrix and four triangles contained within the 2×2 matrix. Each of the elements in the matrix can represent a subword of one or more bits. The permutations provide vertical, horizontal, diagonal, rotational, and other rearrangements of the elements in the atomic unit. *See* Abstract, '526 Patent.

54. The claims of the '526 Patent claim priority to at least May 7, 2001.

55. The claims of the '526 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

56. Further, the claims of the '526 Patent overcome deficiencies in the prior art, including but not limited to those deficiencies embodied in subword parallelism, shift-and-rotate instructions, extract-and-deposit instructions, and mix-and-permute. The prior art was deficient in its ability to permute more than 16 elements. *See* '526 Patent at 1:15-2:23.

57. Further, the claims of the '526 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

58. For example, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, and provide for efficient subword permutation instructions that can be used for parallel execution, for example in 2-D multimedia processing. *See* '526 Patent at 2:50-53.

59. Further, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, and provide for single-cycle instructions, which can be used to construct any type of permutations needed in two-dimensional (2-D) multimedia processing. The instructions can be used in a programmable processor, such as a digital signal processor, video signal processors, media processors, multimedia processors, cryptographic processors and programmable System-on-a-Chips (SOCs). *See* '526 Patent at 2:56-62.

60. Further, the claims of the '526 Patent recite and are drawn to improvements in existing computational technologies, wherein the subword permutation primitives enhance the use of subword parallelism by allowing in-place rearrangement of packed subwords across multiple registers, reducing the need for memory accesses with potentially costly cache misses. The alphabet of permutation primitives of the invention is easy to implement and is useful for 2-D multimedia processing and for other data-parallel computations using subword parallelism. *See* '526 Patent at 3:40-47.

61. The foregoing improvements and technological solutions, as captured in the claims of the '526 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

62. Further, the claims of the '526 Patent do not preempt all methods and systems for providing permutation primitives.

63. Consequently, the claims of the '526 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

64. The '526 Patent was examined by Primary United States Patent Examiner Hosuk Song. During the examination of the '526 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 708/100, 708/520, 712/1, 10, 20, 16, 24, 200, 380/28, 380/37, 42-47.

65. After conducting a search for prior art during the examination of the '526 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US4751733A; (ii) US4845668A; (iii) US5113516A; (iv) US5423010A; and (v) US5673321A.

66. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '526 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

67. The '014 Patent relates generally to methods and systems for providing permutation instructions usable in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. PPERM and PPERM3R instructions are defined to perform permutations by a sequence of instructions with each sequence specifying the position

in the source for each bit in the destination. In the PPERM instruction bits in the destination register that change are updated and bits in the destination register that do not change are set to zero. In the PPERM3R instruction bits in the destination register that change are updated and bits in the destination register that do not change are copied from intermediate result of previous PPERM3R instructions. Both PPERM and PPERM3R instructions can individually do permutation with bit repetition. Both PPERM and PPERM3R instructions can individually do permutation of bits stored in more than one register. In an alternate embodiment, a GRP instruction is defined to perform permutations. *See* Abstract, '014 Patent.

68. The claims of the '014 Patent claim priority to at least May 7, 2001.

69. The claims of the '014 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

70. Further, the claims of the '014 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

71. Further, the claims of the '014 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '014 Patent at 1:14-2:67.

72. For example, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '014 Patent at 3:1-5.

73. Further, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '014 Patent at 3:9-21.

74. Further, the claims of the '014 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '014 Patent at 3:26-31.

75. The foregoing improvements and technological solutions, as captured in the claims of the '014 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

76. Further, the claims of the '014 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

77. Consequently, the claims of the '014 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

78. The '014 Patent was examined by Primary United States Patent Examiner Emmanuel L. Moise, with Assistant Examiner Paul Callahan. During the examination of the '014 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 380/44, 380/265, 28, 377/54, 60, 75, 67, 81, 711/109, 340/825.68, 365/73, 78, 712/1, 24, 10, 712/223.

79. After conducting a search for prior art during the examination of the '014 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US5524256A; (ii) US5734721A; (iii) US6865272B2; (iv)

US4907233A; (v) JP2863597B2; (vi) US5734334A; (vii) US5422705A; (viii) GB9617553D0; (ix) US5996104A; (x) US6275965B1; (xi) US6233671B1; (xii) US6483543B1; (xiii) EP0992916A1; (xiv) US7174014B2; and (xv) Zhijie Shi, Ruby B. Lee: "Bit Permutation Instructions for Accelerating Software Cryptography", in Proc. IEEE Intl. Conf. Application-Specific Systems, Architectures and Processors, pp. 138-148, Jul. 2000.

80. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '014 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

81. The '795 Patent relates generally to methods and systems for providing permutation instructions which can be used in software executed in a programmable processor for solving permutation problems in cryptography, multimedia and other applications. PPERM and PPERM3R instructions are defined to perform permutations by a sequence of instructions with each sequence specifying the position in the source for each bit in the destination. In the PPERM instruction bits in the destination register that change are updated and bits in the destination register that do not change are set to zero. In the PPERM3R instruction bits in the destination register that change are updated and bits in the destination register that do not change are copied from intermediate result of previous PPERM3R instructions. Both PPERM and PPERM3R instruction can individually do permutation with bit repetition. Both PPERM and PPERM3R instruction can

individually do permutation of bits stored in more than one register. In an alternate embodiment, a GRP instruction is defined to perform permutations. The GRP instruction divides the initial sequence in the source register into two groups depending on control bits. The first group is combined with the second group to form an intermediate sequence toward the desired final permutation. The total number of GRP instructions for a bit level permutation of n bits is not greater than 1gn. The GRP instruction can be used to permute k-bit subwords packed into an n bits word, where k can be 1, 2, . . . , or n bits, and k*r=n. At most 1gr permutation instructions are used in the permutation instruction sequence, where r is the number of k-bit subwords to be permuted. The GRP instruction can also be used to permute 2n bits stored in two n-bit registers. The total number of instructions for bit permutation of 2n bits is 21gn+4, and two of those instructions are SHIFT PAIR instruction. *See* Abstract, '795 Patent.

82. The claims of the '795 Patent claim priority to at least May 5, 2000.

83. The claims of the '795 Patent are not drawn to laws of nature, natural phenomena, or abstract ideas. Although the systems and methods claimed in the Asserted Patents are ubiquitous now (and, as a result, are widely infringed), the specific combinations of elements, as recited in the claims, was not conventional or routine at the time of the invention.

84. Further, the claims of the '795 Patent contain inventive concepts which transform the underlying non-abstract aspects of the claims into patent-eligible subject matter.

85. Further, the claims of the '795 Patent overcome deficiencies in the prior art, including but not limited to those relating to secure use of the Internet, symmetric key cryptography, bit-level permutations, table lookup methods, and methods requiring excessive memory requirements. *See* '795 Patent at 1:19-2:65.

86. For example, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide significantly faster and more economical ways to perform arbitrary permutations of n bits, without any need for table storage, which can be used for encrypting large amounts of data for confidentiality or privacy. *See* '795 Patent at 2:66-3:3.

87. Further, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide improved and more efficient cryptography, which provides for improved multimedia processing. *See* '795 Patent at 3:7-19.

88. Further, the claims of the '795 Patent recite and are drawn to improvements in existing computational technologies, and provide a basis for the design of new processors or coprocessors which can be efficient for both cryptography and multimedia software. *See* '795 Patent at 3:17-28.

89. The foregoing improvements and technological solutions, as captured in the claims of the '795 Patent, enable prior art systems to perform better than they previously could by implementing unconventional methodologies.

90. Further, the claims of the '795 Patent do not preempt all methods and systems for solving permutation problems in cryptography.

91. Consequently, the claims of the '795 Patent recite systems and methods resulting in improved functionality of the claimed systems and represent technological improvements to the operation of computers.

92. The '795 Patent was examined by Primary United States Patent Examiner Eric Coleman. During the examination of the '795 Patent, the United States Patent Examiner(s) searched for prior art in the following US Classifications: 712/223, 380/28.

93. After conducting a search for prior art during the examination of the '795 Patent, the United States Patent Examiner(s) identified and cited the following as the most relevant prior art references found during the search: (i) US4907233A; (ii) US5126831A; (iii) US5546393A; (iv) US5673321A; (v) US5734334A; (vi) US5996104A; (vii) US6119224A; (viii) US6233671B1; (ix) US6275965B1; (x) US6278709B1; (xi) US6483543B1; (xii) US6658578B1; (xiii) US6865272B2; and (xiv) US5422705A.

94. After giving full proper credit to the prior art and having conducted a thorough search for all relevant art and having fully considered the most relevant art known at the time, the United States Patent Examiner(s) allowed all of the claims of the '795 Patent to issue. In so doing, it is presumed that the Examiner(s) used his or her knowledge of the art when examining the claims. *K/S Himpp v. Hear-Wear Techs., LLC,* 751 F.3d 1362, 1369 (Fed. Cir. 2014). It is further presumed that the Examiner has experience in the field of the invention, and that the Examiner properly acted in accordance with a person of ordinary skill. *In re Sang Su Lee,* 277 F.3d 1338, 1345 (Fed. Cir. 2002).

## ACCUSED INSTRUMENTALITIES

95. On information and belief, Defendants make, use, import, sell, and/or offer for sale a multitude of products and services as systems on chips ("SoC") that employ technology supporting the infringing instructions including, but not limited to: the Oracle Solaris 11 Operating System (including Oracle SPARC and Oracle x86 Servers shipped with Oracle Solaris 11) (individually and collectively, the "Accused Instrumentalities"). On information and belief, the Accused Instrumentalities are made, used, sold, offered for sale, and/or imported in the United States by Defendants.

**COUNT I**
**(Infringement of U.S. Patent No. 7,174,014B2)**

96. Teleputers incorporates the above paragraphs by reference.

97. Defendants have been on notice of the ’014 Patent at least as early as the date it received service of this Original Complaint.

98. On information and belief, Defendants have directly infringed and continue to infringe the ’014 Patent by making, using, importing, selling, and/or, offering for sale the Accused Instrumentalities in the United States.

99. On information and belief, Defendants, at least as of the date of service of the Original Complaint in this matter, and with knowledge of the ‘014 Patent, indirectly infringe the ‘014 Patent by inducing others to infringe the ‘014 Patent. In particular, Defendants have or will intend to induce customers to infringe the ‘014 Patent by encouraging customers to use the Accused Instrumentalities in a manner that results in infringement.

On information and belief, Defendants also have or will induce others, including its customers, to infringe the ‘014 Patent by providing technical support for the use of the Accused Instrumentalities.

100. Further, since at least the date of service of the Original Complaint in this matter, Defendants have and will indirectly infringe one or more claims of the ‘014 Patent at least when Defendants’ customers (such as device manufacturers which use Defendants’ SoCs in their products) perform the method while testing their devices and when the devices are operated as designed, intended, and instructed, by end-users.

101. On information and belief, the Accused Instrumentalities infringe at least Claim 33 of the ’014 Patent by providing and practicing a computer implemented method for performing an arbitrary permutation of a sequence of bits. Defendants provide a Solaris operating system

(including but not limited to Solaris 11.2, Solaris 11.3 and Solaris 11.4) which supports permutation instructions to permute an input sequence of data. Oracle Solaris is an enterprise operating system for Oracle Database, Oracle Cloud Infrastructure, Oracle IT Infrastructure (enterprise servers and storage solutions) and Java applications.

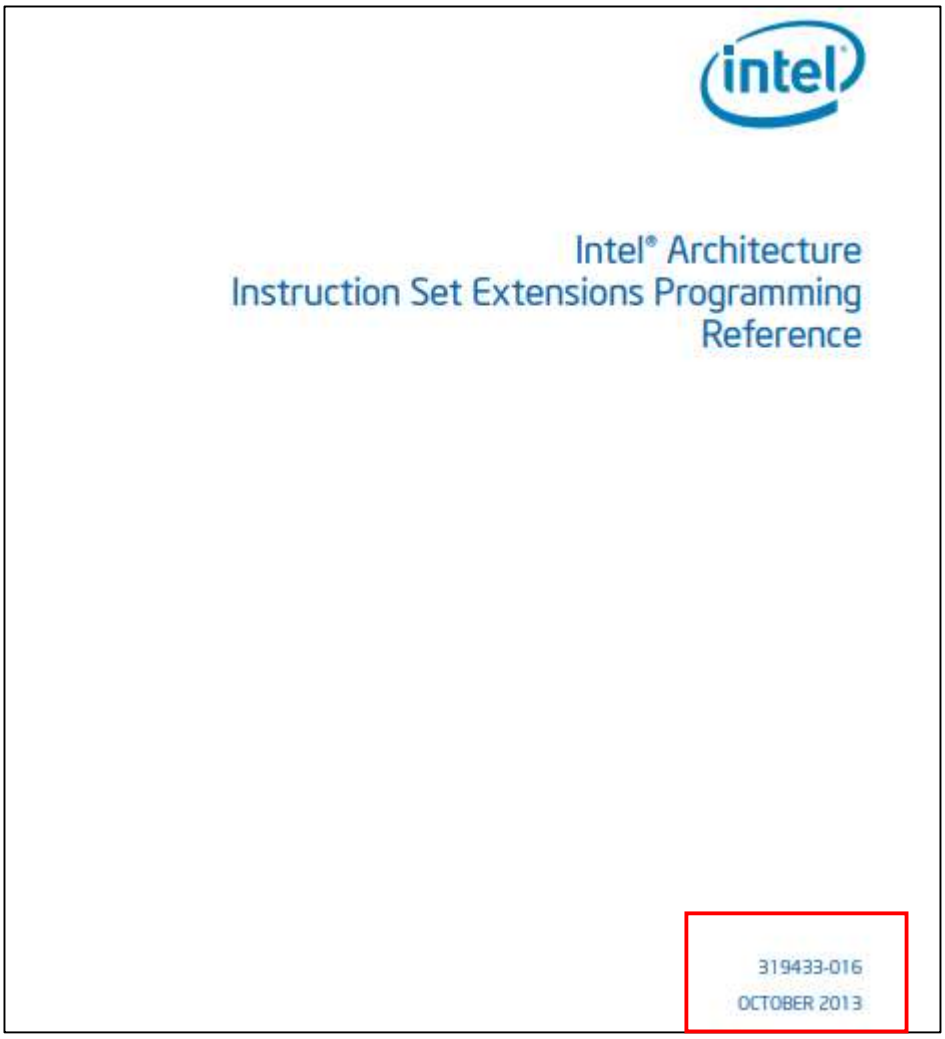
102. Defendants' Solaris 11.2 (used herein as an exemplary product) supports and performs permutation instructions to permute an input sequence of data. Defendants have taken reference from Intel's 64 and IA-32 architecture instruction set for the permutation instructions in Solaris.

103. Further, on information and belief, Defendants directly infringe the claim at least when it tests its operating system Solaris 11. During such tests, on information and belief, Defendants perform permutation on the input data using permutation instructions.


Source: https://www.oracle.com/solaris/solaris11/, as visited on June 23, 2020.

| | | | |
|---|---|---|---|
| vinsertf128 | VINSERTF128<br>VINSERTF32x4<br>VINSERTF64x4 | Insert Packed Floating-Point Values | page 5-305 (319433-016/Oct. 2013) |
| vmaskmov(pd\|ps) | VMASKMOV | Conditional SIMD Packed Loads and Stores | page 4-506 (253667-048US/ Sep.2013) |
| vperm2f128 | VPERM2F128 | Permute Floating-Point Values | page 4-527 (253667-048US/ Sep.2013) |
| vpermilpd | VPERMILPD | Permute Double-Precision Floating-Point Values | page 5-445 (319433-016/Oct. 2013) |
| vpermilps | VPERMILPS | Permute Single-Precision Floating-Point Values | page 5-450 (319433-016/Oct. 2013) |

Source: https://docs.oracle.com/cd/E36784_01/pdf/E36859.pdf , page 73, as visited on June 23, 2020.




Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf (front page), as visited on June 23, 2020.

**VPERMILPD—Permute Double-Precision Floating-Point Values**

| Opcode/ Instruction | Op / En | 64/32 bit Mode Support | CPUID Feature Flag | Description |
|---|---|---|---|---|
| VEX.NDS.128.66.0F38.W0 0D /r<br>VPERMILPD xmm1, xmm2, xmm3/m128 | RVM | V/V | AVX | Permute double-precision floating-point values in xmm2 using controls from xmm3/m128 and store result in xmm1. |
| VEX.NDS.256.66.0F38.W0 0D /r<br>VPERMILPD ymm1, ymm2, ymm3/m256 | RVM | V/V | AVX | Permute double-precision floating-point values in ymm2 using controls from ymm3/m256 and store result in ymm1. |
| EVEX.NDS.512.66.0F38.W1 0D /r<br>VPERMILPD zmm1 {k1}{z}, zmm2, zmm3/m512/m64bcst | FV-RVM | V/V | AVX512F | Permute double-precision floating-point values in zmm2 using control from zmm3/m512/m64bcst and store the result in zmm1 using writemask k1. |
| VEX.128.66.0F3A.W0 05 /r ib<br>VPERMILPD xmm1, xmm2/m128, imm8 | RM | V/V | AVX | Permute double-precision floating-point values in xmm2/m128 using controls from imm8. |
| VEX.256.66.0F3A.W0 05 /r ib<br>VPERMILPD ymm1, ymm2/m256, imm8 | RM | V/V | AVX | Permute double-precision floating-point values in ymm2/m256 using controls from imm8. |
| EVEX.512.66.0F3A.W1 05 /r ib<br>VPERMILPD zmm1 {k1}{z}, zmm2/m512/m64bcst, imm8 | FV-RM | V/V | AVX512F | Permute double-precision floating-point values in zmm2/m512/m64bcst using controls from imm8 and store the result in zmm1 using writemask k1. |

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-445, as visited on June 23, 2020.

104. Further, Defendants perform the step of inputting a source sequence of bits into a source register. For example, the Solaris 11.2 uses a permutation instruction (such as VPERMILPD instruction) to obtain data bits from a first source operand ("source register") and permute the data bits.

**VPERMILPD—Permute Double-Precision Floating-Point Values**

| Opcode/ Instruction | Op / En | 64/32 bit Mode Support | CPUID Feature Flag | Description |
|---|---|---|---|---|
| VEX.NDS.128.66.0F38.W0 0D /r<br>VPERMILPD xmm1, xmm2, xmm3/m128 | RVM | V/V | AVX | Permute double-precision floating-point values in xmm2 using controls from xmm3/m128 and store result in xmm1. |
| VEX.NDS.256.66.0F38.W0 0D /r<br>VPERMILPD ymm1, ymm2, ymm3/m256 | RVM | V/V | AVX | Permute double-precision floating-point values in ymm2 using controls from ymm3/m256 and store result in ymm1. |
| EVEX.NDS.512.66.0F38.W1 0D /r<br>VPERMILPD zmm1 {k1}{z}, zmm2, zmm3/m512/m64bcst | FV-RVM | V/V | AVX512F | Permute double-precision floating-point values in zmm2 using control from zmm3/m512/m64bcst and store the result in zmm1 using writemask k1. |
| VEX.128.66.0F3A.W0 05 /r ib<br>VPERMILPD xmm1, xmm2/m128, imm8 | RM | V/V | AVX | Permute double-precision floating-point values in xmm2/m128 using controls from imm8. |
| VEX.256.66.0F3A.W0 05 /r ib<br>VPERMILPD ymm1, ymm2/m256, imm8 | RM | V/V | AVX | Permute double-precision floating-point values in ymm2/m256 using controls from imm8. |
| EVEX.512.66.0F3A.W1 05 /r ib<br>VPERMILPD zmm1 {k1}{z}, zmm2/m512/m64bcst, imm8 | FV-RM | V/V | AVX512F | Permute double-precision floating-point values in zmm2/m512/m64bcst using controls from imm8 and store the result in zmm1 using writemask k1. |

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-445, as visited on June 23, 2020.

105. Further, Defendants perform the step of defining bit positions in said source sequence of bits to be permuted in said source register for a group of bits in a destination register.

106. For example, the Solaris 11.2 implements a permutation instruction (such as a VPERMILPD instruction) to permute the data bits. The data bits in the first source operand ("source register") are permuted based on the data bits in the second source operand. Therefore, second source operand defines the data bits in the first source operand that will be permuted and moved to the destination operand ("destination register"). If the 0th bit in second source operand (imm8) is 0, then [63-0] bits of first source operand (SRC1) will be moved to [63-0] bit positions in the destination operand (DEST). If the 0th bit in second source operand (imm8) is 1, then [127-64] bits of the first source operand (SRC1) will be moved to [63-0] bit positions in the destination

operand (DEST). Therefore, bits in the second source operand (imm8) define the bit positions for the bits in the first source operand (SRC1) to be permuted.

**Description**

(variable control version)

Permute double-precision floating-point values in the first source operand (second operand) using 8-bit control fields in the low bytes of the second source operand (third operand) and store results in the destination operand (first operand). The destination and the first source operand are vector register.

There is one control byte per destination double-precision element. Each control byte is aligned with the low 8 bits of the corresponding double-precision destination element. Each control byte contains a 1-bit select field (see Figure 5-30) that determines which of the source elements are selected. Source elements are restricted to lie in the same source 128-bit region as the destination.

EVEX.512 version: The second source operand (third operand) is a ZMM register, a 512-bit memory location or a 512-bit vector broadcasted from a 64-bit memory location. Permuted results are written to the destination under the writemask.

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-445, as visited on June 23, 2020.

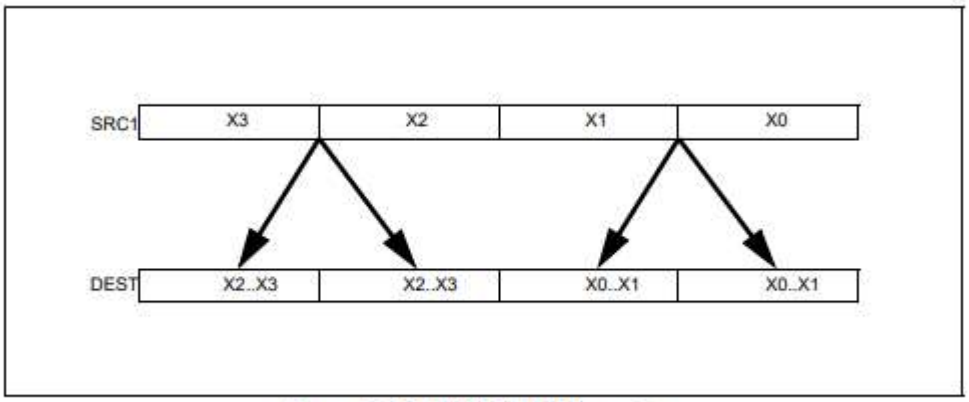



Figure 5-29. VPERMILPD Operation

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-446, as visited on June 23, 2020.

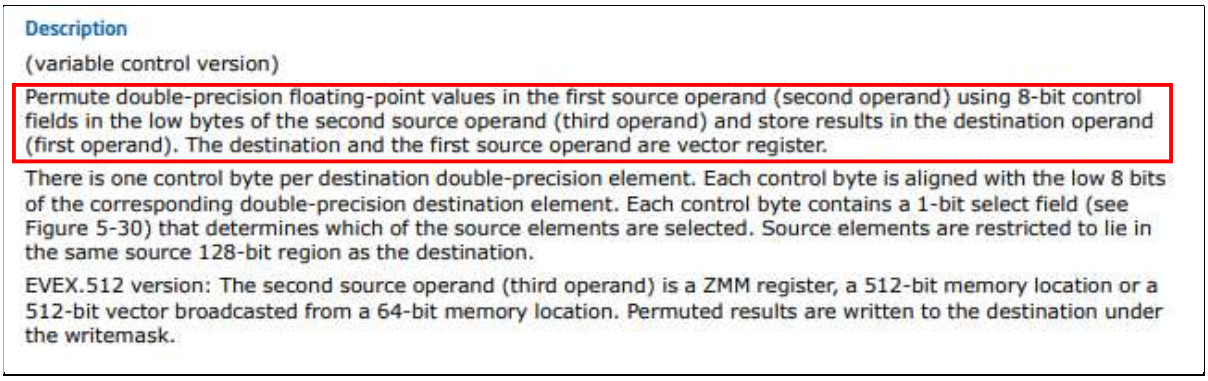
**VPERMILPD (256-bit immediate version)**

IF (imm8[0] = 0) THEN DEST[63:0]←SRC1[63:0]
IF (imm8[0] = 1) THEN DEST[63:0]←SRC1[127:64]
IF (imm8[1] = 0) THEN DEST[127:64]←SRC1[63:0]
IF (imm8[1] = 1) THEN DEST[127:64]←SRC1[127:64]
IF (imm8[2] = 0) THEN DEST[191:128]←SRC1[191:128]
IF (imm8[2] = 1) THEN DEST[191:128]←SRC1[255:192]
IF (imm8[3] = 0) THEN DEST[255:192]←SRC1[191:128]
IF (imm8[3] = 1) THEN DEST[255:192]←SRC1[255:192]

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-447, as visited on June 23, 2020.

107. Further, Defendants perform the step of in response to a PPERM instruction inserting bits from said source sequence into said destination register as determined by said bit positions.

108. For example, the Solaris 11.2 performs the VPERMILPD permutation instruction (equivalent to the PPERM instruction) and in response to the VPERMILPD permutation instruction, the data bits in first source operand ("source sequence") are moved to the destination operand ("destination register") according to the bit positions defined by second source operand.



**Description**

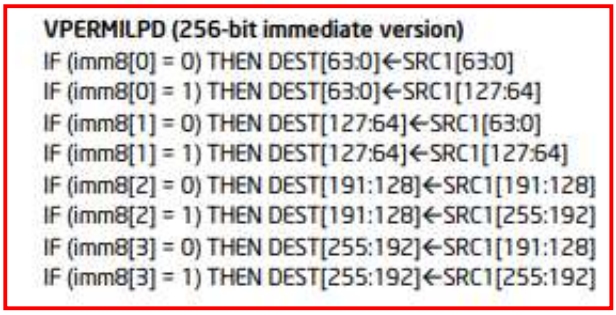
(variable control version)

Permute double-precision floating-point values in the first source operand (second operand) using 8-bit control fields in the low bytes of the second source operand (third operand) and store results in the destination operand (first operand). The destination and the first source operand are vector register.

There is one control byte per destination double-precision element. Each control byte is aligned with the low 8 bits of the corresponding double-precision destination element. Each control byte contains a 1-bit select field (see Figure 5-30) that determines which of the source elements are selected. Source elements are restricted to lie in the same source 128-bit region as the destination.

EVEX.512 version: The second source operand (third operand) is a ZMM register, a 512-bit memory location or a 512-bit vector broadcasted from a 64-bit memory location. Permuted results are written to the destination under the writemask.

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-445, as visited on June 23, 2020.



**VPERMILPD (256-bit immediate version)**

IF (imm8[0] = 0) THEN DEST[63:0]←SRC1[63:0]
IF (imm8[0] = 1) THEN DEST[63:0]←SRC1[127:64]
IF (imm8[1] = 0) THEN DEST[127:64]←SRC1[63:0]
IF (imm8[1] = 1) THEN DEST[127:64]←SRC1[127:64]
IF (imm8[2] = 0) THEN DEST[191:128]←SRC1[191:128]
IF (imm8[2] = 1) THEN DEST[191:128]←SRC1[255:192]
IF (imm8[3] = 0) THEN DEST[255:192]←SRC1[191:128]
IF (imm8[3] = 1) THEN DEST[255:192]←SRC1[255:192]

Source: http://kib.kiev.ua/x86docs/Intel/ISAFuture/319433-016.pdf, page 5-447, as visited on June 23, 2020.

## PRAYER FOR RELIEF

WHEREFORE, Teleputers respectfully requests the Court enter judgment against Defendants:

1. declaring that the Defendants have infringed each of the Patents-in-Suit;

2. awarding Teleputers its damages suffered as a result of Defendants' infringement of the Patents-in-Suit;

3. awarding Teleputers its costs, attorneys' fees, expenses, and interest;

4. awarding Teleputers ongoing post-trial royalties; and

5. granting Teleputers such further relief as the Court finds appropriate.

## JURY DEMAND

Teleputers demands trial by jury, under Fed. R. Civ. P. 38.

Dated: September 24, 2020

Respectfully Submitted

*/s/ M. Scott Fuller*

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