IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

HD SILICON SOLUTIONS LLC, Plaintiff, v. MICROCHIP TECHNOLOGY INC., Defendant.	Civil Action No. 6:20-cv-1092 **PATENT CASE** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

This is an action for patent infringement in which plaintiff HD Silicon Solutions LLC ("HDSS"), makes the following allegations against defendant Microchip Technology Inc. ("MTI"):

BACKGROUND

1. This lawsuit asserts causes of action for infringement of HDSS's patents referenced in Counts One through Seven herein (collectively, the "Asserted Patents").

2. The Asserted Patents address various core technologies in modern semiconductors, including microcontrollers, microprocessors, and programmable gate arrays.

THE PARTIES

3. Plaintiff HDSS is an intellectual property licensing company. HDSS is organized and existing as a limited liability company under the laws of Texas with a principal place of business at 5900 Balcones Drive, Suite 100, Austin, Texas 78731.

4. Defendant MTI is a corporation organized and existing under the laws of Delaware, with a principal place of business at 2355 West Chandler Boulevard, Chandler, Arizona 85224. MTI is doing business, either directly or through its agents, on an ongoing basis

in this judicial district and elsewhere in the United States, and has a regular and established place of business in this judicial district. MTI may be served through its registered agent The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801.

JURISDICTION AND VENUE

5. This action arises under the patent laws of the United States, Title 35 of the United States Code, including in particular 35 U.S.C. § 271.

6. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

7. This Court has personal jurisdiction over MTI because MTI has minimum contacts with Texas and this district such that this venue is a fair and reasonable one. MTI conducts substantial business in this forum, including (i) engaging in the infringing conduct alleged herein and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct, and/or deriving substantial revenue from goods and services provided to companies and individuals in Texas and in this district.

8. Venue in the Western District of Texas is proper under 28 U.S.C. §§ 1391(b) and (c) and 1400(b).

9. Upon information and belief, MTI has committed infringing acts in this judicial district by making, using, offering for sale, selling, or importing products or services that infringe the Asserted Patents, or by inducing others to infringe the Asserted Patents. On information and belief, MTI maintains a "regular and established" place of business in this district, including by maintaining and operating one or more places in this district where research, development, or sales are conducted or where customer service is provided.

10. On information and belief, MTI has a regular and established physical presence in the district, including but not limited to, ownership of or control over property, equipment, or

inventory. For example, MTI has an office located at 8601 Ranch Road 2222, Park Centre Building 3, Austin, Texas 78730, which lies within this federal judicial district.

11. In other recent actions, MTI has either admitted or not contested that this federal judicial district is a proper venue for patent infringement actions against it. *See, e.g.*, Answer to 1st Am. Compl. ¶ 14, *Vantage Micro LLC v. Microchip Tech. Inc.*, No. W-19-cv-581 (W.D. Tex. Feb. 18, 2020), ECF No. 22, *answering* 1st Am. Compl. ¶ 14, ECF No. 16 (Feb. 4, 2020); Answer ¶ 5, *Far North Patents, LLC v. Microchip Tech. Inc.*, No. 6:20-cv-221 (W.D. Tex. Jun. 23, 2020), ECF No. 17, *answering* Compl. ¶ 5, ECF. No. 1 (Mar. 25, 2020). MTI has also admitted or failed to contest that it has transacted business in this district. *See, e.g.*, Answer to 1st Am. Compl. ¶ 13, *Vantage Micro LLC v. Microchip Tech. Inc.*, No. W-19-cv-581 (W.D. Tex. Feb. 18, 2020), ECF No. 22, *answering* 1st Am. Compl. ¶ 13, ECF No. 16 (Feb. 4, 2020).

COUNT ONE
Infringement of U.S. Patent No. 7,260,731

12. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

13. On August 21, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,260,731 B1 ("the '731 Patent"), entitled "Saving power when in or transitioning to a static mode of a processor." A true and correct copy of that patent is attached as Exhibit 1.

14. HDSS is the owner by assignment of the '731 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

15. Claim 6 of the '731 Patent recites:

> 6. A method for reducing power utilized by a system having a least a processor, comprising the steps of:

> determining that the processor is transitioning from a computing mode to a mode in which a system clock to the processor is disabled,
>
> reducing core voltage being furnished by a voltage regulator to the processor to a value sufficient to maintain state during the mode in which the system clock is disabled, and
>
> transferring operation of the voltage regulator furnishing core in a mode in which power is dissipated during a voltage transition in reduction in core voltage to a mode in which power is saved during said voltage transition in the reduction in core voltage when it is determined that the processor is transitioning from the computing mode to the mode in which the system clock to the processor is disabled.

16. By way of example, MTI's PIC24 family of 16-bit microcontroller chips utilize what MTI refers to as "eXtreme Low-Power or XLP Technology."[1] This XLP Technology provides different power management modes, including a "Low-Voltage/Retention Sleep" mode at a reduced voltage level, to reduce power consumption by the chip's processor. In this mode, the core voltage drops from an operating voltage of 1.8V (or more) to 1.2V and the main CPU clock is shut down, but device state is maintained.[2]

17. The "'731 Accused Chips" include at least each of the aforementioned chips as well as any other MTI chips utilizing XLP Technology supporting a Low-Voltage/Retention Sleep mode.

18. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 6, of the '731 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, using, offering to sell, or selling in the United States or importing into the United States the '731 Accused Chips.

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[1] eXtreme Low-Power (XLP) PIC Microcontrollers: An Introduction to Microchip's Low-Power Devices, AN1267, at 1 (2017), http://ww1.microchip.com/downloads/en/AppNotes/00001267b.pdf.
[2] *Id.* at 4–5.

19. For example, the ’731 Accused Chips implement a method for reducing power utilized by the processor. The method utilizes an on-board voltage regulator that, according to MTI, “has the ability to alter functionality to provide power savings.” The voltage regulator includes “two basic modules: the Voltage Regulator (VREG) and the Retention Regulator (RETREG).” In the regular operating “Run” mode of the ’731 Accused Chips, “the main VREG is providing a regulated voltage with enough current to supply a device running at full speed.” In this mode, the RETREG “may or may not be running, but is unused.” In the Low-Voltage/Retention Sleep mode, “the device is in Sleep and all regulated voltage is provided solely by the Retention Regulator.”[3]

20. When the ’731 Accused Chips determine that the processor is transitioning from Run mode to Low-Voltage/Retention Sleep mode, the voltage regulator transitions the core voltage to the processor down to 1.2V and during the transition turns off the VREG and provides voltage solely with the RETREG (also known the “low-voltage/retention regulator”). This changes the voltage regulator from a regulation mode in which power is dissipated to one in which power is saved during the voltage transition.

21. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’731 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the ’731 Accused Chips and the creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including

[3] PIC24FV32KA304 Family Datasheet, DS30009995E, at 133 (2017), http://ww1.microchip.com/downloads/en/DeviceDoc/30009995e.pdf.

the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the ’731 Patent.

22. For example, MTI took active steps to encourage end users to use the ’731 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims, including at least claim 6, of the ’731 Patent, including by selling the chips and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-identified active steps after receiving notice of the ’731 Patent and how those steps induce infringement of that patent.

23. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’731 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the ’731 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

24. For example, MTI is aware that the functionality included in the ’731 Accused Chips enables such chips to reduce power consumption as described above and that such functionality infringes the ’731 Patent, including at least claim 6. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the ’731 Patent and how the chips’ functionality infringes that patent.

25. The infringing aspects of the ’731 Accused Chips can be used only in a manner that infringes the ’731 Patent and thus have no substantial non-infringing uses. The infringing

aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

26. MTI's acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI's infringement of HDSS's rights under the '731 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT TWO
Infringement of U.S. Patent No. 7,870,404

27. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

28. On January 11, 2011, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,870,404 B2 ("the '404 Patent"), entitled "Transitioning to and from a sleep state of a processor." A true and correct copy of that patent is attached as Exhibit 2.

29. HDSS is the owner by assignment of the '404 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

30. Claim 1 of the '404 Patent recites:

> 1. A computer system comprising:
>
> a processing unit;
>
> circuitry coupled to the processing unit, said circuitry configured to provide to said processing unit:
>
> a sleep voltage;
>
> a first operating voltage; and

a second operating voltage that is less than the first operating voltage;

wherein said computer system has a first transition time for transitioning from said sleep voltage to said first operating voltage;

wherein said computer system has a second transition time for transitioning from said sleep voltage to said second operating voltage;

wherein said second transition time is within an allowed time for transitioning from a sleep state to an operating state; and

wherein said first transition time is greater than said allowed time.

31. By way of example, MTI's PIC24FV32KA304 and other members of MTI's PIC24 family of 16-bit microcontroller chips utilize "eXtreme Low-Power" (XLP) technology providing for "sleep" and "low-voltage/retention sleep" power-saving modes. The "'404 Accused Chips" include at least each of the aforementioned chips as well as any other MTI chips utilizing XLP technology.

32. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 1, of the '404 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, offering to sell, or selling in the United States or importing into the United States the '404 Accused Chips.

33. The '404 Accused Chips include a CPU processor and an adjustable voltage supply for the processor in the form of "a Voltage Regulator that has the ability to alter functionality to provide power savings" or "VREG." The adjustable voltage supply also includes a "Retention Regulator (RETREG)." According to MTI, "[w]ith the combination of VREG and RETREG," several power modes are available.[4]

[4] DS30009995E, *supra* note 3, at 1, 133.

34. The voltage regulator of the '404 Accused Chips is configured to output various operating voltages ranging from, for example, 2.0V at the low end to 3.2V–5.5V at the high end. According to MTI, the figure below shows a "PIC24FV32KA304 voltage-frequency graph (industrial and extended)."[5] As shown in the figure, the various operating voltages have corresponding supported operating frequencies.

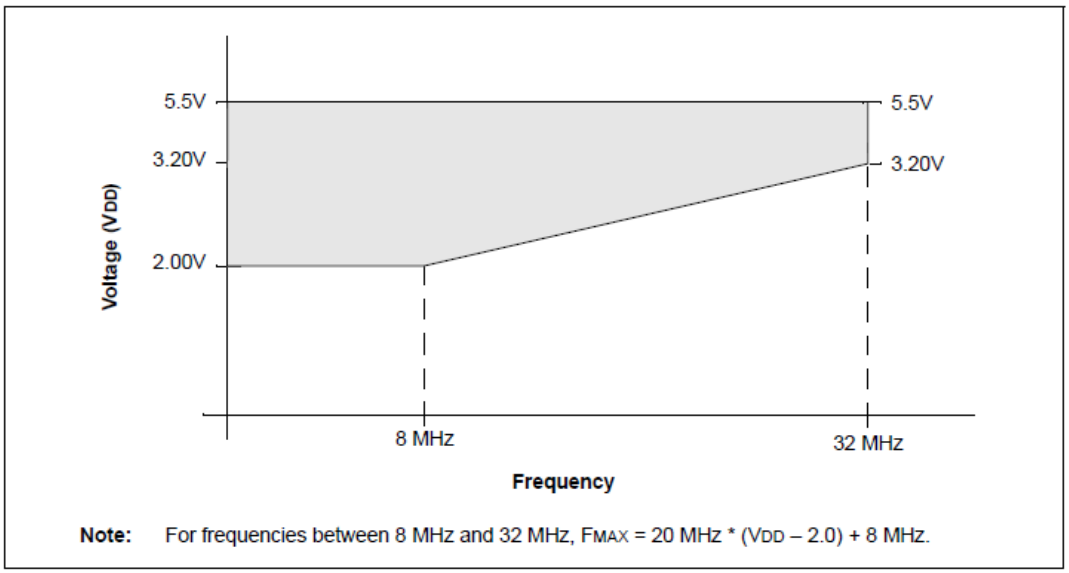

Figure 1

35. These operating voltages support the chips' "Run Mode." According to MTI, "In Run mode, the main VREG is providing a regulated voltage with enough current to supply a device running at full speed."[6]

36. The voltage regulator of the '404 Accused Chips is also configured to output a sleep voltage, which is the voltage supporting the mode that MTI describes as "Retention Sleep mode." According to MTI, "In Retention Sleep mode, the device is in Sleep and all regulated voltage is provided solely by the Retention Regulator. Consequently, this mode has lower power consumption than regular Sleep mode, but is also limited in terms of how much functionality can

[5] *Id.* at 264 & Fig. 29-1.
[6] *Id.* at 264; AN1267, *supra* note 1, at 133.

be enabled."[7] According to MTI, "Low-Voltage/Retention Sleep mode is similar to Sleep mode" except that "the low-voltage/retention regulator allows the core digital logic voltage (VCORE) to drop to 1.2V. This permits an incremental reduction in power consumption over what would be required if VCORE was maintained at [an operating] level."[8] When the processor transitions from "Low-Voltage/Retention Sleep mode" into "Run mode," the voltage regulator returns to outputting an operating voltage.

37. On information and belief, the adjustable voltage supply transitions from "Low-Voltage/Retention Sleep mode" to a higher operating voltage in a time period greater than the time period allowed for transition to a lower operating voltage. According to MTI, "Low-Voltage Sleep mode requires a longer wake-up time than Sleep mode, due to the additional time required to bring [the core voltage] back to [an operating voltage]."[9] The transition to 3.2V, for example, takes longer than the transition to 2.0V because, among other reasons, the frequency must be increased, as shown in Figure 1 above, from 8 Mhz to 32 Mhz, which is done over a period of additional time.

38. In addition, MTI has indirectly infringed and continues to indirectly infringe the '404 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the '404 Accused Chips and the creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including

[7] DS30009995E, *supra* note 3, at 133.
[8] AN1267, *supra* note 1, at 5.
[9] AN1267, *supra* note 1, at 5.

the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the ’404 Patent.

39. For example, MTI took active steps to encourage end users to use the ’404 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims of the ’404 Patent, including by selling the chips and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-identified active steps after receiving notice of the ’404 Patent and how those steps induce infringement of that patent.

40. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’404 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the ’404 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

41. For example, MTI is aware that the functionality included in the ’404 Accused Chips enables such chips to transition between voltages as described above and that such functionality infringes the ’404 Patent. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the ’404 Patent and how the chips’ functionality infringes that patent.

42. The infringing aspects of the ’404 Accused Chips can be used only in a manner that infringes the ’404 Patent and thus have no substantial non-infringing uses. The infringing

aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

43. MTI's acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI's infringement of HDSS's rights under the '404 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT THREE
Infringement of U.S. Patent No. 7,810,002

44. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

45. On October 5, 2010, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,810,002 B2 ("the '002 Patent"), entitled "Providing trusted access to a JTAG scan interface in a microprocessor." A true and correct copy of that patent is attached as Exhibit 3.

46. The '002 Patent teaches a method for securing access to the trusted resources of a secure processor. Such processors contain secret information, such as cryptographic keys, authentication information, or runtime register states, that normally should not leave the secure processor. However, it is often useful to have an interface that provides access to such information for purposes of debugging, profiling, aiding the manufacturing process, testing, or diagnosing defects of a chip. Some preexisting processors allowed entirely unsecured access to such information from outside the chip, such as through a documented software or scan chain interface, whereas others may have allowed access through an undocumented hardware interface, relying on the absence of public documentation as the sole basis for security.

47. The ’002 Patent teaches the use of a trusted software layer in conjunction with a secure processor, such that only the trusted software layer, and not any untrusted software, has access to the ability to enable the scan chain interface providing access to the internal secrets. At the time of the invention and at the time of the filing of the application leading to the ’002 Patent, the use of such a trusted software layer in conjunction with a secure processor was unconventional, uncommon, and not well-understood in the industry.

48. The trusted software is in a unique position to be able to securely authenticate the validity of a request to allow access to the scan chain interface and, if the request is valid, enable access to the scan chain interface. The use of such a trusted software layer in conjunction with a secure processor prevents untrusted software from enabling access to the internal secrets of the processor. This provides a level of security unavailable in prior processors. In addition, the performance of authentication operations at the trusted software layer, instead of in hardware, minimizes the number of hardware components necessary in the secure processor to support the authentication process. This also potentially allows the authentication operation to occur even though portions of a chip or processor may be malfunctioning, as may often be the case when the purpose of accessing the interface is to diagnose defects. Furthermore, because the authentication operation occurs in software, it is more easily modified, enhanced, or patched than any hardware-based solution.

49. HDSS is the owner by assignment of the ’002 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

50. Claim 1 of the ’002 Patent recites:

> 1. A method for securing a scan chain architecture, said method comprising:

> disabling a scan interface in a system comprising a secure processor and a software layer, wherein said software layer is authorized to access trusted resources in said secure processor;
>
> receiving authentication information at the software layer, wherein said authentication information if valid provides access to said scan interface;
>
> verifying whether said authentication information is valid using said software layer; and
>
> allowing access to said scan interface if said authentication information is valid.

51. Claim 17 of the ’002 Patent recites:

> 17. A computer-readable medium having stored thereon, computer-executable instructions that, responsive to execution by a computing device, cause the computing device to perform operations comprising:
>
> disabling a scan interface of a system comprising a secure processor and a software layer, wherein said software layer is authorized to access trusted resources in said secure processor;
>
> receiving authentication information at the software layer, wherein said authentication information if valid provides access to said scan interface;
>
> verifying whether said authentication information is valid using said software layer; and
>
> allowing access to said scan interface if said authentication information is valid.

52. By way of example, MTI’s SAM L11 family of microcontroller chips utilize TrustZone technology to provide access control for debug functionality. The “’002 Accused Chips” include at least each of the aforementioned chips as well as any other MTI chips that provide access control for debug functionality in a substantially similar manner.

53. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 17, of the ’002 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, offering to sell, or selling in the United States or importing into the United

States the '002 Accused Chips. In addition, on information and belief, MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 1, of the '002 Patent in violation of 35 U.S.C. § 271(a) by, without authority, using in the United States the claimed method for accessing the scan interface on the '002 Accused Chips, including for purposes of developing, debugging, profiling, aiding the manufacturing process, testing, or diagnosing defects of such chips.

54. For example, the '002 Accused Chips include an "Arm Cortex-M23" microprocessor.[10] Arm is a technology provider that licenses processor and system-on-chip designs to chip providers such as MTI.

55. The '002 Accused Chips include "Arm TrustZone technology" providing for "integrated hardware security" including "secure debug" functionality, resulting in a secure processor.[11] This debug functionality is provided across a "Serial Wire Debug (SWD)" scan interface.[12]

56. The '002 Accused Chips include a computer-readable memory coupled to the processor in the form of an internal ROM containing program instructions including for "Secure Boot."[13]

57. According to MTI, "TrustZone for an ARMv8-M device is based on a specific hardware that is implemented in the Cortex-M23 core, which is combined with a dedicated secure instructions set. It enables creating multiple software security domains that restricts access

[10] Microchip SAM L10/L11 Family Datasheet, DS60001513F, at 1, 53 (2020), https://ww1.microchip.com/downloads/en/DeviceDoc/SAM-L10L11-Family-DataSheet-DS60001513F.pdf.
[11] https://www.microchip.com/design-centers/32-bit/sam-32-bit-mcus/sam-l-mcus/sam-l10-and-l11-microcontroller-family
[12] DS60001513F, *supra* note 10, at 3.
[13] *Id.* at 17.

to selected memory, peripherals, and I/O to trusted software without compromising the system performances."[14] The secure instructions including those in secure boot ROM are a software layer authorized to access trusted resources in the processor.

58. According to MTI, the '002 Accused Chips provide several "debug access levels (DAL), which restrict programming and debug access to Secure and Non-Secure resources in the system." In DAL0, which is the lowest level of access, "No access is authorized except with a debugger using the Boot ROM Interactive mode." In DAL1, "Access is limited to the Non-Secure memory regions. Secure memory region accesses are forbidden." DAL2 provides "Debug access with no restrictions in terms of memory and peripheral accesses."[15]

59. According to MTI, "For security reasons, while the Boot ROM is executing, no debug is possible except when entering a specific Boot ROM mode called CPU Park mode."[16] As a result, the scan interface is initially disabled.

60. Accessing higher DAL levels requires submitting authentication information in the form of a secret "ChipErase" key to the trusted software layer. According to MTI, "The chip erase commands allow to erase memories of the device and provide secure transitions between the different Debug Access Levels." In particular, as reflected in the MTI figure below depicting "SAM L11 Debug Access Levels Transitions," the "CEKEY2" key enables a transition to DAL2.[17] According to MTI, "The various chip erase operations are managed by the boot ROM

[14] Microchip SAM L11 Security Reference Guide, AN5365, DS70005365B, at 3 (2019), http://ww1.microchip.com/downloads/en/Appnotes/SAML11-Security-Reference-Guide-DS70005365B.pdf.
[15] AN5365, *supra* note 14, at 13.
[16] DS60001513F, *supra* note 10, at 67.
[17] *Id.* at 75.

code."[18] The trusted software layer verifies whether the CEKEY2 is correct and, if so, allows DAL2 access to the scan interface.

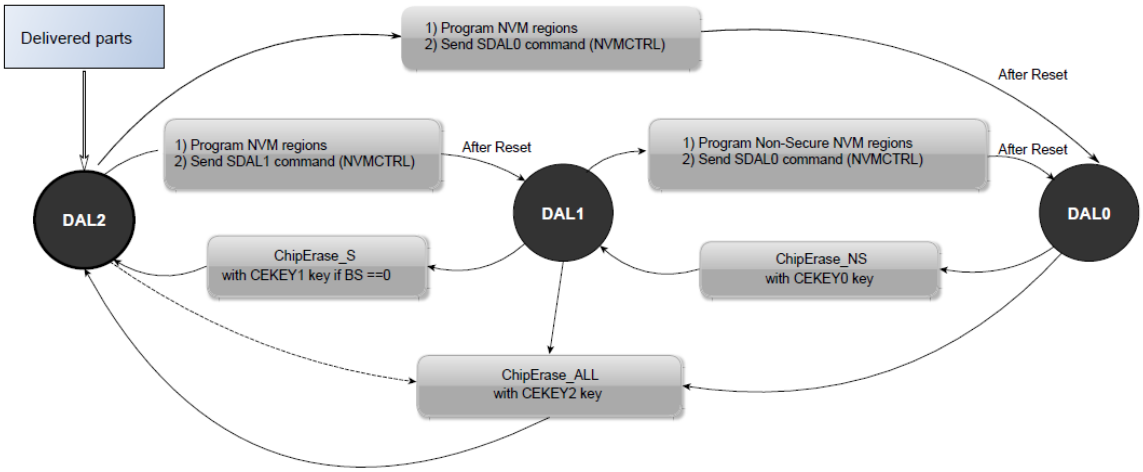

Figure 2

61. In addition, MTI has indirectly infringed and continues to indirectly infringe the '002 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the '002 Accused Chips and the creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the '002 Patent.

62. For example, MTI took active steps to encourage end users to use the '002 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims, including at least claim 1, of the '002 Patent, including by selling the chips

[18] *Id.* at 512.

and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-identified active steps after receiving notice of the '002 Patent and how those steps induce infringement of that patent.

63. In addition, MTI has indirectly infringed and continues to indirectly infringe the '002 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the '002 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

64. For example, MTI is aware that the functionality included in the '002 Accused Chips enables such chips to secure the scan interface as described above and that such functionality infringes the '002 Patent, including at least claim 1. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the '002 Patent and how the chips' functionality infringes that patent.

65. The infringing aspects of the '002 Accused Chips can be used only in a manner that infringes the '002 Patent and thus have no substantial non-infringing uses. The infringing aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

66. MTI's acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI's infringement of HDSS's rights under

the ’002 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT FOUR
Infringement of U.S. Patent No. 6,748,577

67. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

68. On June 8, 2004, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,748,577 B2 (“the ’577 Patent”), entitled “System for simplifying the programmable memory to logic interface in FPGA.” A true and correct copy of that patent is attached as Exhibit 4.

69. HDSS is the owner by assignment of the ’577 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

70. Claim 1 of the ’577 Patent recites:

> 1. A programmable gate array (PGA) comprising:
>
> at least one embedded memory having a plurality of address lines, data lines, and control lines connected thereto;
>
> a plurality of programmable logic blocks (PLBs);
>
> a plurality of input/outputs (I/Os);
>
> a plurality of routing lines interconnecting said at least one embedded memory, said PLBs, and said I/Os;
>
> an interface for isolating the routing lines from said address lines, data lines, and control lines; and
>
> a plurality of dedicated connections for connecting said PLBs and said I/Os to said at least one embedded memory.

71. By way of example, MTI’s AT40K family of products sold under MTI’s Atmel brand are field-programmable gate array chips. The “’577 Accused Chips” include at least each

of the aforementioned chips as well as any other MTI programmable gate array chips that provide connections to embedded memory in a substantially similar manner.

72. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 1, of the '577 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, offering to sell, or selling in the United States or importing into the United States the '577 Accused Chips.

73. For example, the '577 Accused Chips have a plurality of inputs/outputs in the form of "128 – 384 PCI Compliant I/Os." The chips include embedded memory in the form of "FreeRAM."[19] According to MTI, "32 x 4 dual-ported RAM blocks are dispersed throughout the array." "RAM" refers to "random access memory." Such memory blocks have address lines, data lines, and control lines.[20]

74. The chips include thousands of programmable logic blocks in the form of cells with, according to MTI, "configurable logic block[s] based around two 3-input LUTs . . . , which can be combined to produce one 4-input LUT. This means any core cell can implement two functions of three inputs or one function of four inputs."[21]

75. According to MTI, the figure below depicts a "cell" in '577 Accused Chips, including the two aforementioned LUTs that make up a programmable logic block.[22]

[19] Atmel AT40K05AL, AT40K10AL, AT40K20AL, AT40K40AL Datasheet at 1 (2013), http://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-2818-FPGA-AT40KAL-Series-Datasheet.pdf.
[20] *Id.* at 11.
[21] *Id.* at 9.
[22] *Id.* at 9 & Fig. 5-1.

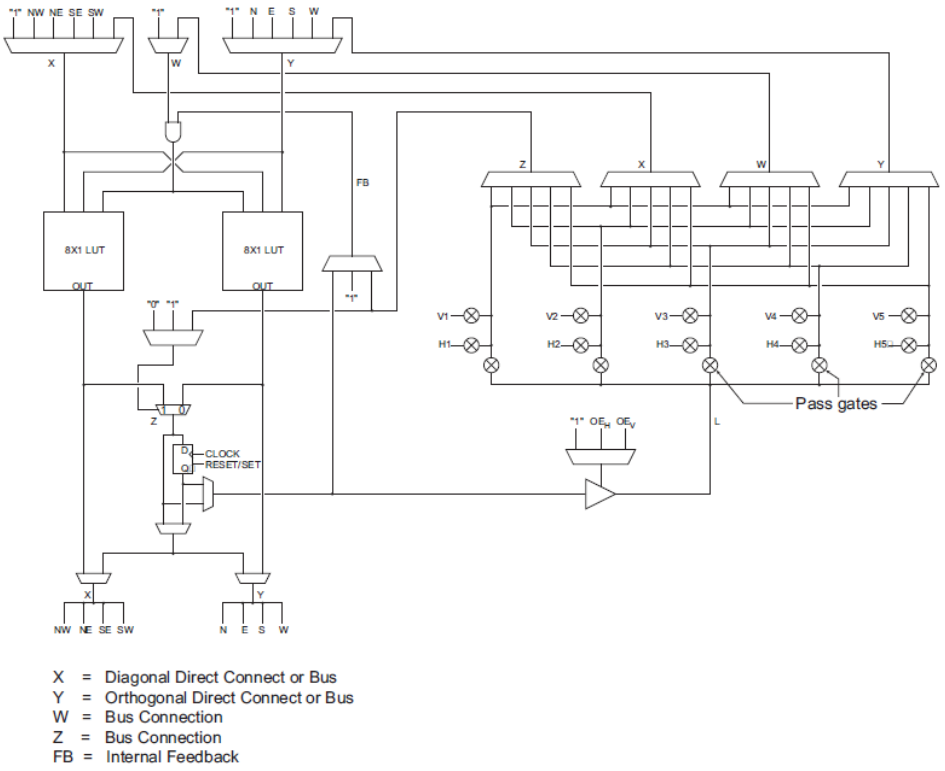

Figure 3

76. According to MTI, the figure below depicts connections to I/Os for exemplary "West Primary I/O" cells. The box labeled "PAD" refers to an "I/O pad . . . that connects the I/O to the outside world." As shown in the figure, the I/Os are connected directly to certain cells (in the figure, the middle cell) as well as indirectly to certain cells via routing lines. Other I/O cells throughout the chip, described by MTI using other compass-directional names, are connected through corresponding configurations depending on their location on the chip that achieve the same result.[23]

[23] *Id.* at 19–21 & Fig. 9-1.

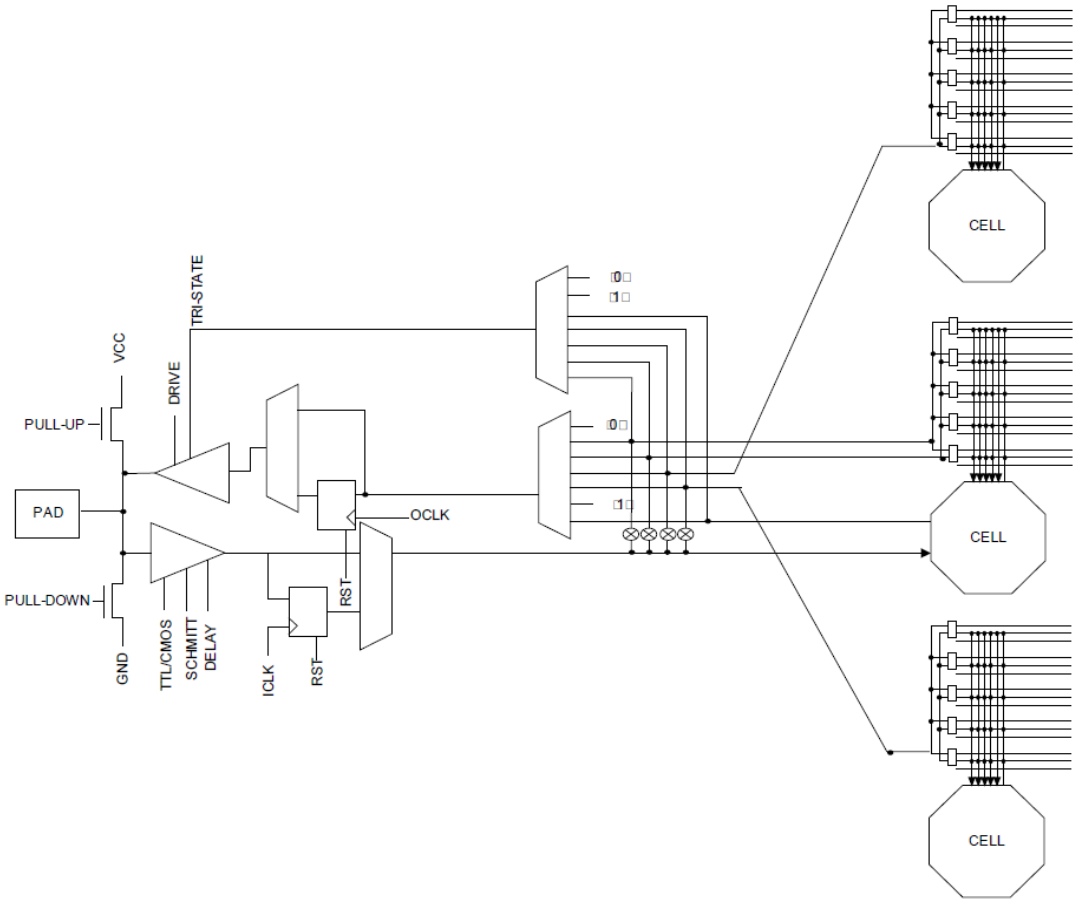

Figure 4

77. According to MTI, the figure below depicts "RAM Connections" for "One Ram Block" in '577 Accused Chips.[24]

[24] *Id.* at 11 & Fig. 6-1.

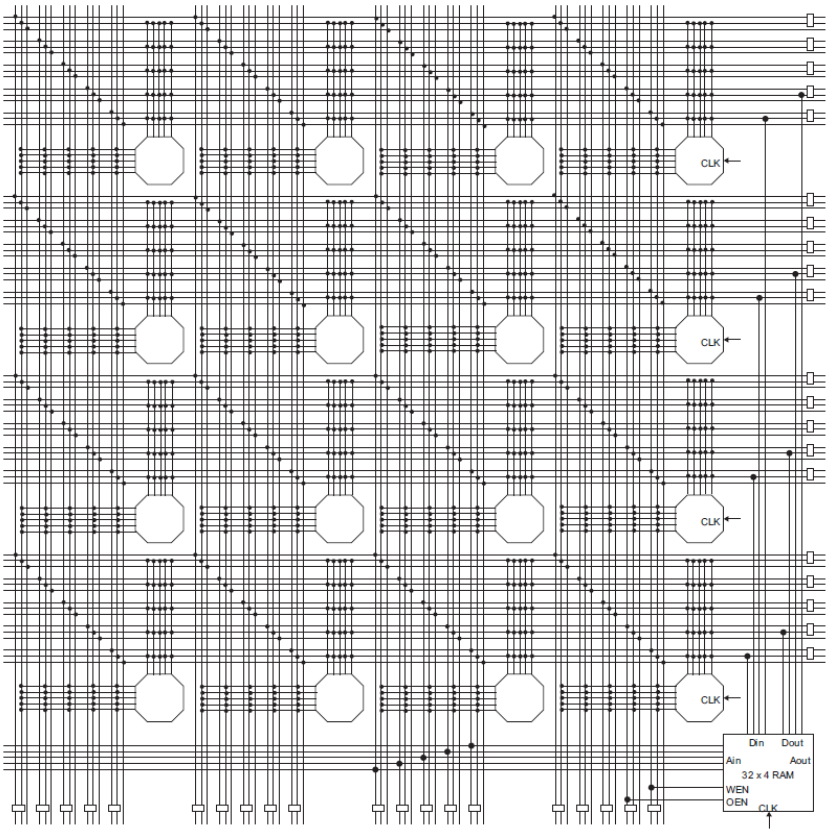

Figure 5

78. Figure 5 shows routing lines interconnecting a "32 x 4 RAM" (in the lower right corner) with cells (shown as octagons), and thereby with the programmable logic blocks and inputs/outputs, in '577 Accused Chips.[25] According to MTI, Figure 6 below "depicts the connections between a cell and five horizontal local buses (one per busing plane) and five vertical local buses (one per busing plane)" in '577 Accused Chips.[26] The connections labeled variously as "W," "X," "Y," and "Z" correspond to the connections shown in Figure 3 above, which interconnect with the programmable logic blocks and inputs/outputs.

[25] *Id.* at 11.
[26] *Id.* at 8 & Fig. 4-1(b).

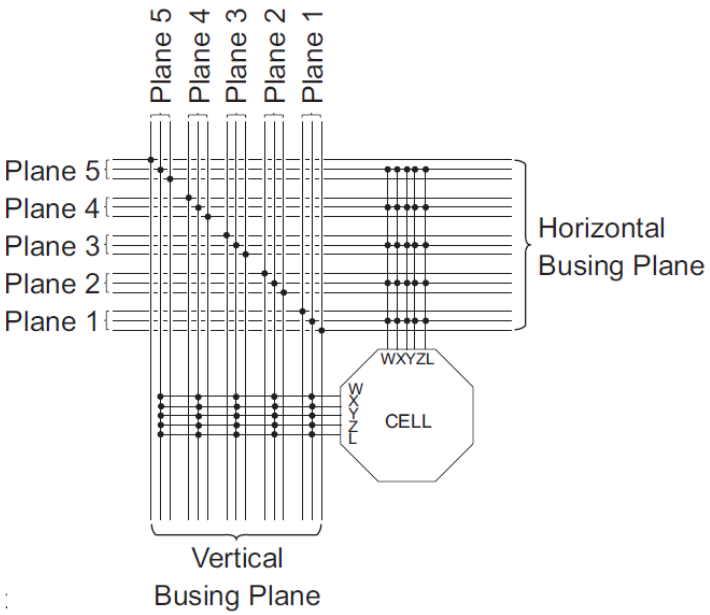

Figure 6

79. The '577 Accused Chips include an interface for isolating the aforementioned routing lines from the address lines, data lines, and control lines. For example, Figure 5 above shows that the various hard connections (the large dots along the bottom and right side of the figure) to the address lines, data lines, and control lines of the embedded memory may be isolated from the routing lines using an isolating interface in the form of programmable transistors (the small dots along various diagonals).

80. The aforementioned hard connections result in dedicated connections from the programmable logic blocks and inputs/outputs to the embedded memory. For example, according to MTI, Figure 7 below depicts a "RAM Example" for "128 x 8 Dual-ported RAM (Asynchronous)" in '577 Accused Chips.[27] As indicated in the figure, "Dedicated Connections" connect the programmable logic blocks and inputs/outputs in the cells (shown as octagons) to embedded memory (shown in eight squares) in '577 Accused Chips.

[27] *Id.* at 12 & Fig. 6-3.

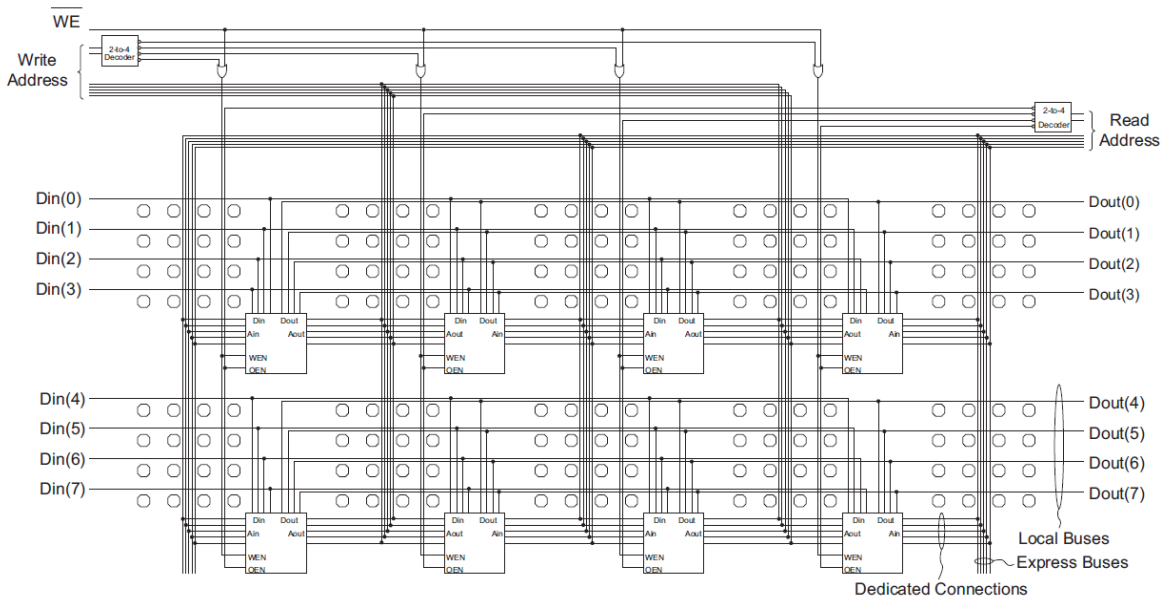

Figure 7

81. In addition, MTI has indirectly infringed and continues to indirectly infringe the '577 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the '577 Accused Chips and the creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the '577 Patent.

82. For example, MTI took active steps to encourage end users to use the '577 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims of the '577 Patent, including by selling the chips and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-

identified active steps after receiving notice of the ’577 Patent and how those steps induce infringement of that patent.

83. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’577 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the ’577 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

84. For example, MTI is aware that the functionality included in the ’577 Accused Chips enables such chips to provide connections as described above and that such functionality infringes the ’577 Patent. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the ’577 Patent and how the chips’ functionality infringes that patent.

85. The infringing aspects of the ’577 Accused Chips can be used only in a manner that infringes the ’577 Patent and thus have no substantial non-infringing uses. The infringing aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

86. MTI’s acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI’s infringement of HDSS’s rights under the ’577 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT FIVE
Infringement of U.S. Patent No. 7,154,299

87. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

88. On December 26, 2006, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,154,299 B2 ("the '299 Patent"), entitled "Architecture for programmable logic device." A true and correct copy of that patent is attached as Exhibit 5.

89. HDSS is the owner by assignment of the '299 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

90. Claim 14 of the '299 Patent recites:

> 14. An integrated circuit comprising:
>
> programmable logic blocks; and
>
> routing resources adjacent to one of the programmable logic blocks and including a sequential logic element having an input and an output, the routing resources operable to couple the input of the sequential logic element to one of the logic blocks via no circuit element other than one or more pass gates and to simultaneously couple the output of the sequential logic element to one of the programmable logic blocks;
>
> wherein the routing resources are operable to allow bidirectional communication via the sequential logic element between the logic block coupled to the input of the sequential logic element and the logic block coupled to the output of the sequential logic element.

91. By way of example, MTI's PolarFire family of field-programmable gate array chips sold under MTI's Microsemi brand are integrated circuits. The "'299 Accused Chips" include at least each of the aforementioned chips as well as any other MTI programmable gate array chips that provide routing resources that operate in a substantially similar manner.

92. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 14, of the '299 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, offering to sell, or selling in the United States or importing into the United States the '299 Accused Chips.

93. For example, the '299 Accused Chips include programmable logic blocks in the form of look-up tables. According to MTI, the chips have "[u]p to 481K logic elements consisting of a 4-input look-up table (LUT),"[28] and this "4-input LUT with carry chain can be configured to implement any 4-input combinatorial logical function or arithmetic function."[29]

94. These programmable logic blocks have routing resources adjacent to them. According to MTI, the figure below depicts a "Functional Block Diagram of Logic Element" in '299 Accused Chips.[30] The routing resources include a sequential logic element in the form of a D-type flip-flop (designated "Flip-Flop" in the figure) with a data input ("D") and an output ("Q").

[28] Microchip PolarFire FPGAs Brochure at 3 (2019), https://www.microsemi.com/document-portal/doc_download/136519-ds0141-polarfire-fpga-datasheet.
[29] UG0680 User Guide PolarFire FPGA Fabric, Rev. 6.0, at 10 (2020), https://www.microsemi.com/document-portal/doc_download/136522-ug0680-polarfire-fpga-fabric-user-guide.
[30] *Id.* at 10.

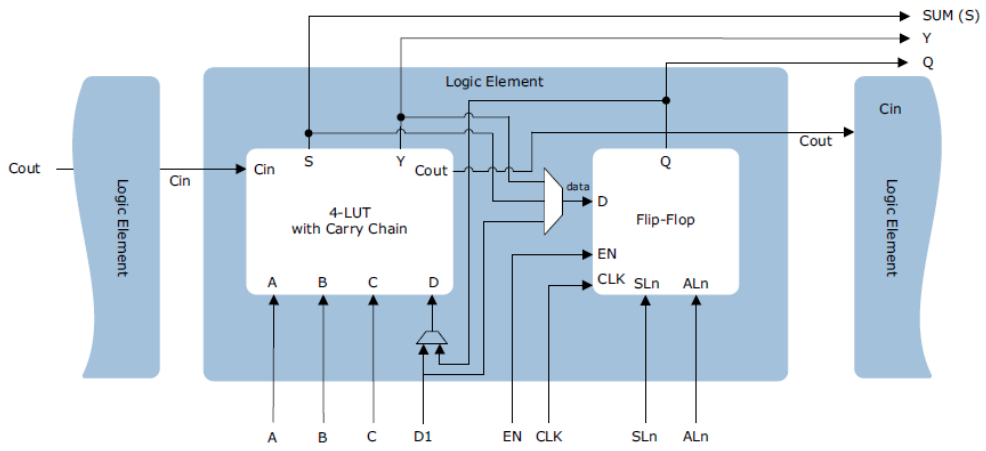

Figure 8

95. As shown in the figure, the routing resources include connections operable to couple the flip-flop input "D" to one of the logic blocks represented by the incoming routing interface connection "D1," where this coupling is via a pass gate in the form of a multiplexer (shown as a trapezoidal figure) outputting the "data" signal and via no circuit element other than one or more pass gates (including the multiplexer). Simultaneously, the routing resources include connections operable to couple the flip-flop output "Q" to the programmable logic block shown in the figure as the right-side input to another multiplexer and thereby into the "D" input of the LUT.

96. According to MTI, "The logic elements in the PolarFire FPGA are organized in clusters." Figure 9 below "shows the logic cluster with its routing interface" in '299 Accused Chips.[31]

[31] *Id.* at 12 & Fig. 8.

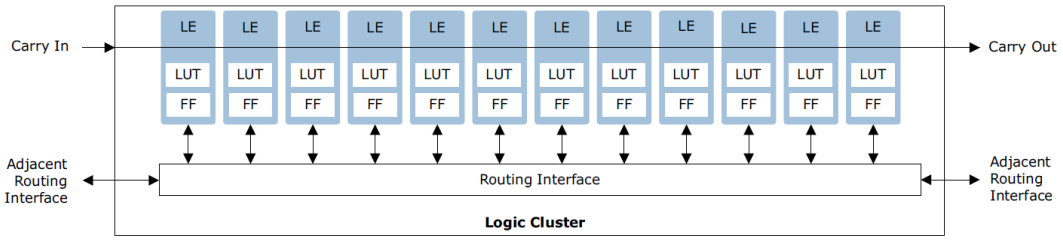

Figure 9

97. As shown in the figure, the logic cluster includes a "Routing Interface" allowing bidirectional communication among the logic elements in the cluster. The routing resources further include this "Routing Interface." The routing resources are operable to allow bidirectional communication between the LUTs of different cells via the flip-flop sequential logic element.

98. For example, with reference to Figure 8, signals coming in at flip-flop input "D," which connects through the incoming routing interface connection "D1" to the output of the LUT of another cell, can be sent through the flip-flip output "Q" through the multiplexer that provides the LUT input "D," thereby allowing communication from another LUT to the depicted LUT. Likewise, signals from the depicted LUT output "Y" can be sent to the depicted flip-flop input "D" via the "data" multiplexer and output as flip-flop output "Q," which connects through the routing interface to the "D" input of the other LUT via that other LUT's multiplexer and its incoming signal "D1." Thus, the routing resources allow bidirectional communication via the sequential logic element between the logic block coupled to the input of the sequential logic element and the logic block coupled to the output of the sequential logic element.

99. In addition, MTI has indirectly infringed and continues to indirectly infringe the '299 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the '299 Accused Chips and the

creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the ’299 Patent.

100. For example, MTI took active steps to encourage end users to use the ’299 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims of the ’299 Patent, including by selling the chips and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-identified active steps after receiving notice of the ’299 Patent and how those steps induce infringement of that patent.

101. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’299 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the ’299 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

102. For example, MTI is aware that the functionality included in the ’299 Accused Chips enables such chips to provide communication as described above and that such functionality infringes the ’299 Patent. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the ’299 Patent and how the chips’ functionality infringes that patent.

103. The infringing aspects of the ’299 Accused Chips can be used only in a manner that infringes the ’299 Patent and thus have no substantial non-infringing uses. The infringing aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

104. MTI’s acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI’s infringement of HDSS’s rights under the ’299 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT SIX
Infringement of U.S. Patent No. 7,302,619

105. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

106. On November 27, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,302,619 B1 (“the ’619 Patent”), entitled “Error correction in a cache memory.” A true and correct copy of that patent is attached as Exhibit 6.

107. HDSS is the owner by assignment of the ’619 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

108. Claim 21 of the ’619 Patent recites:

> 21. A system for instruction error correction, comprising:
>
> an instruction cache;
>
> a processor operatively coupled to the instruction cache, the processor being configured to fetch a plurality of instructions stored in the instruction cache, each of the instructions being fetched during a respective one of a plurality of instruction cycles; and

> circuitry configured to detect an error in each of the instructions concurrently with the fetching of a respective one of the instructions.

109. By way of example, MTI's PIC32MZ DA, PIC32MZ EF, and PIC32MK families of microcontrollers utilize an L1 CPU cache with a prefetch module providing error detection and correction. The "'619 Accused Chips" include at least each of the aforementioned chips as well as any other MTI chips that utilize an L1 CPU cache with a prefetch module providing error detection and correction.

110. MTI has directly infringed and continues to directly infringe one or more claims, including at least claim 21, of the '619 Patent in violation of 35 U.S.C. § 271(a) by, without authority, making, offering to sell, or selling in the United States or importing into the United States the '619 Accused Chips.

111. The '619 Accused Chips include a system for instruction error correction as recited in claim 21 and in operation perform the method for error correction as recited in claim 1. The '619 Accused Chips include a processor in the form of their "CPU" and an instruction cache in the form of a "Prefetch module" operating with the "L1 CPU Cache," which includes a "line for CPU instructions," as described in Microchip's PIC32 Family Reference Manual. According to MTI, the PFM includes "Error detection and correction."[32]

112. According to MTI, "The Prefetch module is a performance enhancing module included in PIC32 devices with L1 CPU caches. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of

[32] Microchip PIC32 Family Reference Manual at 41-2 (2013), http://ww1.microchip.com/downloads/en/DeviceDoc/60001183B.pdf.

the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly."[33]

113. In the '619 Accused Chips, the prefetched instructions are placed in a "temporary holding area" depicted as the lowest row of "Data" fields in MTI's "Prefetch Module Block Diagram" shown as Figure 10 below. This instruction cache is operatively coupled to the "System Bus/CPU" as shown in the diagram.[34]

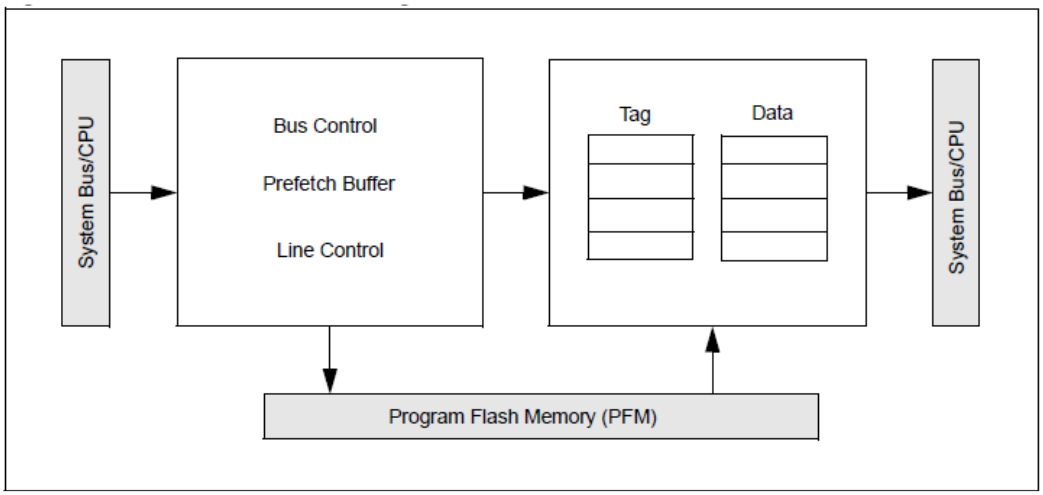

Figure 10

114. In the '619 Accused Chips, the CPU fetches instructions for execution from the PFM. According to MTI, in normal operation the "CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations."[35] This results in each instruction being fetched from the PFM during a respective one of the instruction cycles.

[33] *Id.* at 41-3.
[34] *Id.* at 41-3.
[35] Microchip PIC32MZ Graphics (DA) Family Datasheet at 51 (2019), http://ww1.microchip.com/downloads/en/DeviceDoc/PIC32MZ_DA%20_Family%20Datasheet_DS60001361H.pdf.

115. In the ’619 Accused Chips, error detection for each instruction is performed concurrently with the fetching of instructions by circuitry configured to perform such error detection. Specifically, according to MTI, “The Prefetch module handles and reports information about two error types: ECC Double-bit Error Detected (DED) and ECC Single-bit Error Corrected (SEC).” Further, according to MTI, “A read from the Flash memory that results in a PFM ECC DED causes the Prefetch module to return a bus exception error to the initiator. If that initiator is the CPU, it recognizes the bus exception error, prevents the instruction from executing, or read data from loading, and generates an exception using the bus exception error vector.”[36]

116. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’619 Patent in violation of 35 U.S.C. § 271(b) by taking active steps to encourage and facilitate direct infringement by others, including OEMs, agent-subsidiaries, affiliates, partners, service providers, manufacturers, importers, resellers, customers, and/or end users, in this district and elsewhere in the United States, through the dissemination of the ’619 Accused Chips and the creation and dissemination of promotional and marketing materials, supporting materials, instructions, product manuals, and/or technical information relating to such products (including the materials previously cited) with knowledge and the specific intent that its efforts will result in the direct infringement of the ’619 Patent.

117. For example, MTI took active steps to encourage end users to use the ’619 Accused Chips in the United States in a manner it knows will directly infringe each element of one or more claims of the ’619 Patent, including by selling the chips and promoting and instructing on their use despite knowing of the patent and the fact that such acts will cause the

[36] Microchip PIC32 Family Reference Manual, *supra* note 32, at 41-10.

user to use the chip in a manner that infringes the patent. MTI continues to undertake the above-identified active steps after receiving notice of the ’619 Patent and how those steps induce infringement of that patent.

118. In addition, MTI has indirectly infringed and continues to indirectly infringe the ’619 Patent in violation of 35 U.S.C. § 271(c) by selling or offering to sell in the United States, or importing into the United States, the ’619 Accused Chips with knowledge that they are especially designed or adapted to operate in a manner that infringes that patent and despite the fact that the infringing technology or aspects of the chips are not a staple article of commerce suitable for substantial non-infringing use.

119. For example, MTI is aware that the functionality included in the ’619 Accused Chips enables such chips to perform error correction as described above and that such functionality infringes the ’619 Patent. MTI continues to sell and offer to sell such chips in the United States after receiving notice of the ’619 Patent and how the chips’ functionality infringes that patent.

120. The infringing aspects of the ’619 Accused Chips can be used only in a manner that infringes the ’619 Patent and thus have no substantial non-infringing uses. The infringing aspects of those instrumentalities otherwise have no meaningful use, let alone any meaningful non-infringing use.

121. MTI’s acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those wrongful acts in an amount subject to proof at trial. MTI’s infringement of HDSS’s rights under the ’619 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

COUNT SEVEN
Infringement of U.S. Patent No. 6,774,033

122. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

123. On August 10, 2004, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 6,774,033 B1 ("the '033 Patent"), entitled "Metal stack for local interconnect layer." A true and correct copy of that patent is attached as Exhibit 7.

124. HDSS is the owner by assignment of the '033 Patent and holds all substantial rights in that patent, including the sole and exclusive right to sue and recover for any and all infringement.

125. Claim 1 of the '033 Patent recites:

> 1. A method of forming a local interconnect layer in an integrated circuit, the method comprising:
>
> depositing a first film over an oxide layer, the first film comprising titanium nitride; and
>
> depositing a second film over the first film, the second film comprising tungsten, the first film and the second film forming a metal stack of the local interconnect layer.

126. Claim 5 of the '033 Patent recites:

> 5. The method of claim 1 wherein the first film is deposited to a thickness equal to or less than about 300 Angstroms.

127. By way of example, MTI's PolarFire family of field-programmable gate array chips (sold under MTI's Microsemi brand) include interconnect layers formed by metal stacks of titanium nitride and tungsten. The "'033 Accused Chips" include at least each of the aforementioned chips as well as any other MTI chips manufactured using a substantially similar process.

128. MTI has directly infringed and continues to directly infringe one or more claims, including at least claims 1 and 5, of the ’033 Patent in violation of 35 U.S.C. § 271(a) and/or (g) by using in the United States, without authority, the claimed processes to manufacture the ’033 Accused Chips and/or by importing into the United States, without authority, the ’033 Accused Chips which are made using the claimed processes.

129. For example, the ’033 Accused Chips are integrated circuits that contain static random access memory (SRAM) circuits that have local interconnect layers used to connect transistors. Examples of the local interconnect layers are shown in Figure 11 below, which shows a tunneling-electron microscopic image of the SRAM of a PolarFire MPF100T chip with two examples of interconnects circled.

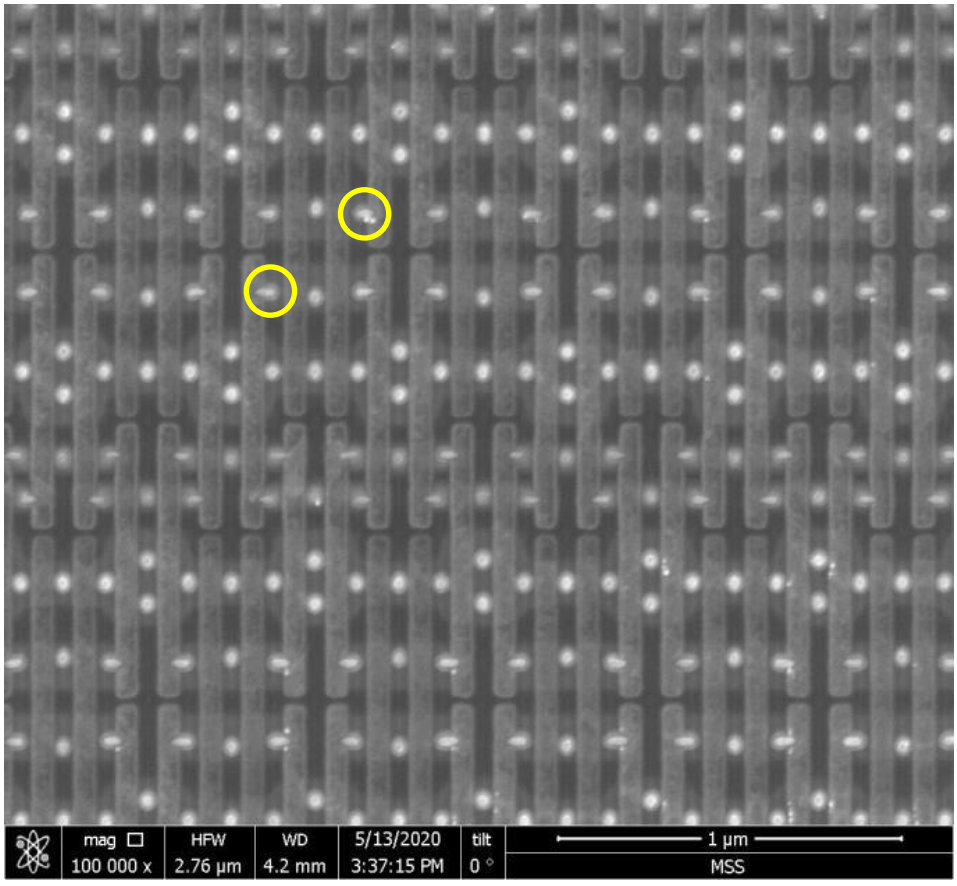

Figure 11

130. An example of the metal stack of an interconnect is shown in Figure 12 below, which shows a tunneling-electron microscopic image of the cross-section view of a transistor (the dark block at the bottom) with connectors through a local interconnect layer in a PolarFire MPF100T chip.

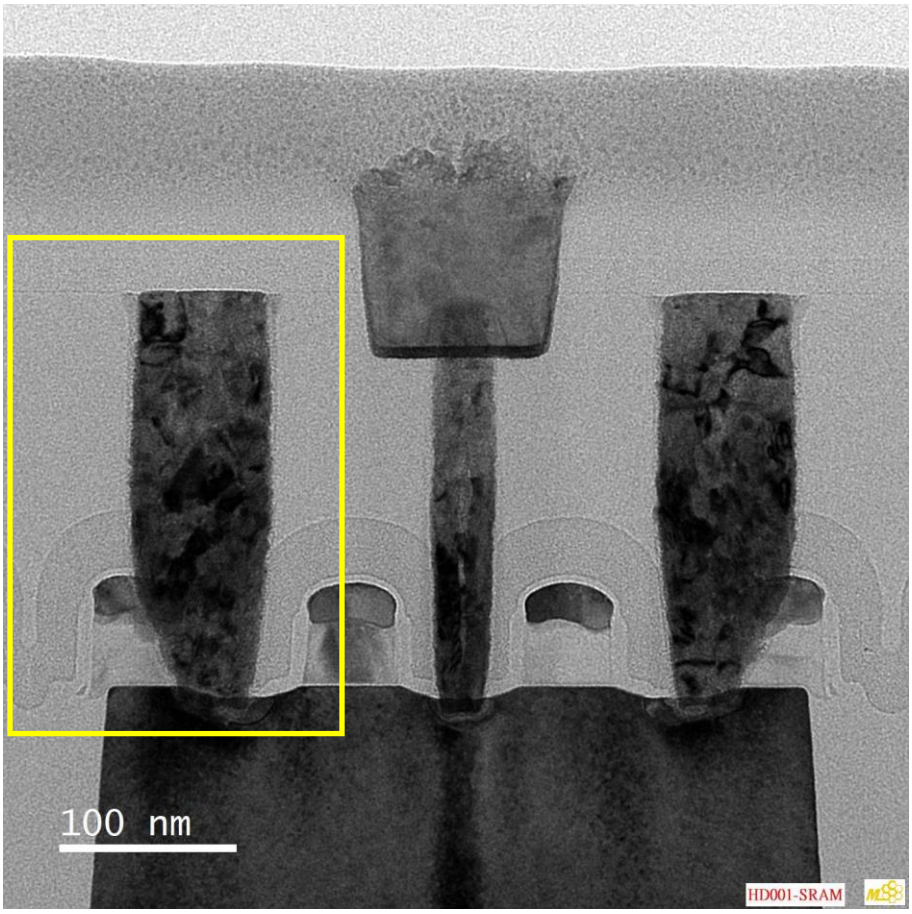

Figure 12

131. Figure 13 below is an enlargement of the yellow-highlighted portion of the above figure with an overlay showing the material composing certain layers.

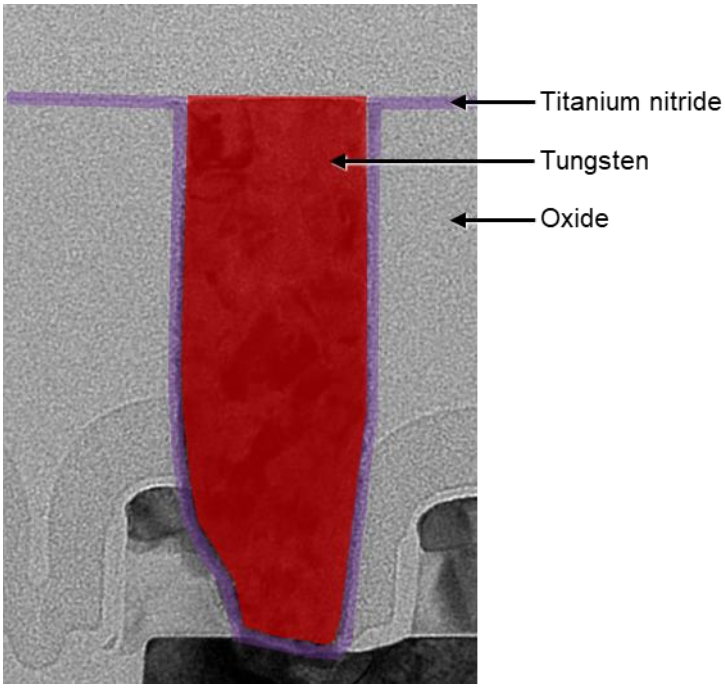

Figure 13

132. As shown in Figure 13 above, the interconnect layers consist of a metal stack of titanium nitride and tungsten layers on top of an oxide layer.

133. As evidenced by the scale in Figure 12 above, the titanium nitride layer is roughly 10 nanometers, and well under 30 nanometers (300 Angstroms), in thickness.

134. Upon information and belief, these interconnect layers are formed by depositing a first film comprising titanium nitride to a thickness less than 300 Angstroms on top of an oxide layer, and then depositing a second film comprising tungsten over the first film. Trenches in the surface, such as that shown in Figure 13, during depositions fill from the outer surfaces inwards, and excess tungsten deposited above the surface of the trench is subsequently removed through grinding and/or polishing. The titanium nitride and tungsten layers form a metal stack of the local interconnect layer.

135. MTI's acts of infringement have caused and continue to cause damage to HDSS, and HDSS is entitled to recover from MTI the damages it has sustained as a result of those

wrongful acts in an amount subject to proof at trial. MTI's infringement of HDSS's rights under the '033 Patent will continue to damage HDSS, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

DEMAND FOR JURY TRIAL

136. HDSS hereby demands a jury trial pursuant to Federal Rule of Civil Procedure 38.

FEES AND COSTS

137. To the extent that MTI's litigation conduct supports a finding that this is an "exceptional case," an award of attorneys' fees and costs to HDSS is justified pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, HDSS prays for relief against MTI as follows:

a. Declaring that MTI has infringed the Asserted Patents, contributed to the infringement of the Asserted Patents, and/or induced the infringement of the Asserted Patents;

b. Awarding HDSS damages arising out of this infringement of the Asserted Patents, including enhanced damages pursuant to 35 U.S.C. § 284 and prejudgment and post-judgment interest, in an amount according to proof;

c. Permanently enjoining MTI, and its respective officers, agents, servants, employees, and those acting in privity with it, from further infringement, including inducing infringement and contributory infringement, of the Asserted Patents;

d. Awarding attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law; and

e. Awarding to HDSS such other costs and further relief as the Court deems just and proper.

DATED: November 30, 2020 Respectfully submitted,

By: */s/ Max L. Tribble Jr.*

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