IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

LIBERTY PATENTS, LLC, Plaintiff, v. ANALOG DEVICES, INC., Defendant.	CIVIL ACTION NO. 6:21-cv-60 ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Liberty Patents, LLC ("Liberty Patents" or "Plaintiff") files this original complaint against Defendant Analog Devices, Inc. ("ADI" or "Defendant"), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

PARTIES

1. Liberty Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas 75703.

2. Defendant Analog Devices, Inc. is a company organized and existing under the laws of the Commonwealth of Massachusetts. Analog Devices, Inc. may be served with process through its registered agent, Corporation Service Company d/b/a/ CSC-Lawyers Incorporating Service Company at 211 East 7th Street, Suite 620, Austin, Texas, 78701-3218.

3. ADI describes itself as "a world leader in the design, manufacture, and marketing of a broad portfolio of high performance analog, mixed-signal, and digital signal processing (DSP) integrated circuits (ICs) used in virtually all types of electronic equipment."[1] ADI's

[1] https://www.analog.com/en/about-adi/corporate-information.html.

products are used by over 100,000 customers worldwide and include "data converters, amplifiers and linear products, radio frequency (RF) ICs, power management products, sensors based on microelectromechanical systems (MEMS) technology and other sensors, and processing products, including DSP and other processors."[2]

JURISDICTION AND VENUE

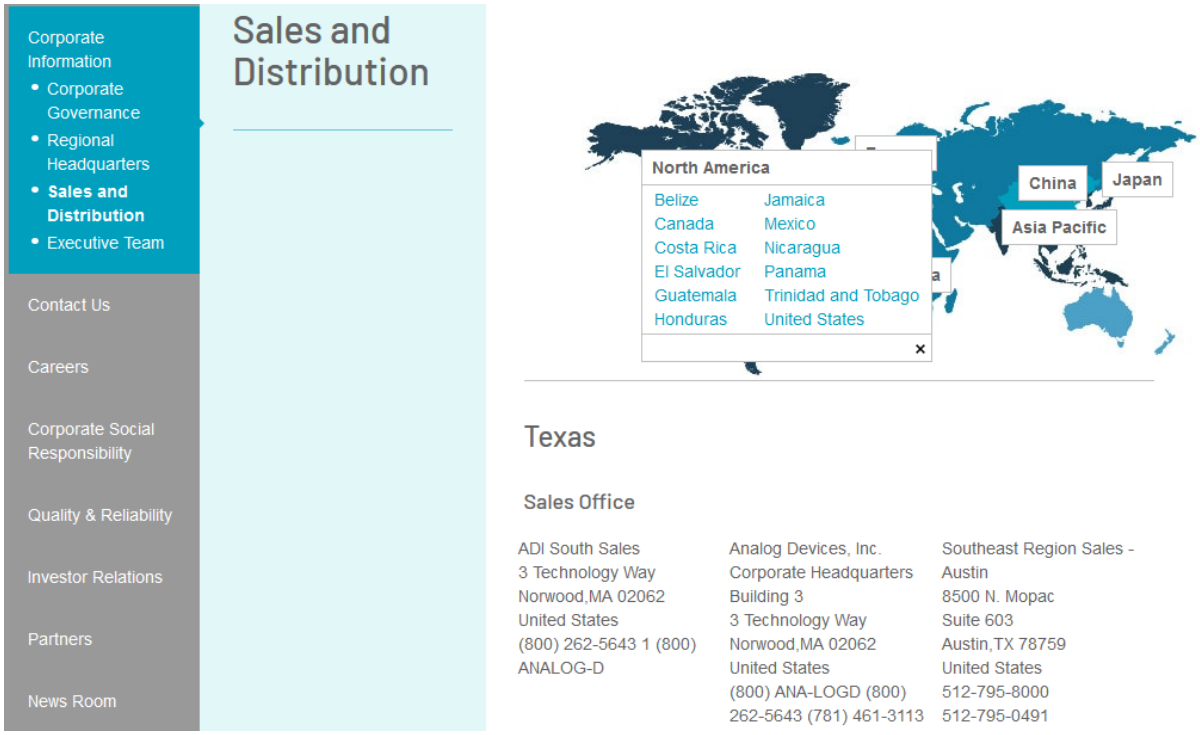
4. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

5. This Court has personal jurisdiction over ADI pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) ADI has done and continues to do business in Texas; (ii) ADI has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing a least a portion of any other infringements alleged herein in Texas, and (iii) ADI is registered to do business in Texas.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). Venue is further proper because ADI has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a portion of any other infringements alleged herein in this district.

[2] *Id*.

7. ADI also has a regular and established places of business in this district, including at least at 8500 N. Mopac, Suite 603, Austin, Texas, 78759:



Source: www.analog.com/en/about-adi/corporate-information/sales-distribution.html

BACKGROUND

8. The patents-in-suit generally relate to zero delay buffer (ZDB) technology. In particular, they teach ZDB technology with multiple output clock signals—instantiations of a reference input clock signal—with predicted delay. The inventions of the patents-in-suit afforded the industry with numerous enhancements, some of which included product robustness, multiplexed feedback, minimization of delay between output clock signals, programmability, and approximating a closed-loop system to mitigate variations in temperature, supply voltage, supply ground, and/or output loading effects.

9. The patented technology was developed by engineers at Cypress Semiconductor Corp., which is one of the preeminent semiconductor design and manufacturing companies in the

world today. In the early 2000s, when the patents-in-suit were filed, Cypress Semiconductor was a world leader in timing-technology solutions and specifically, was leading all other companies in the clock distribution arena.[3]

10. Cypress Semiconductor is a pioneer in the area of programmable clocks, having been in the "Timing Solutions" industry since the late 1990s.[4] Indeed, Cypress Semiconductor invented the world's first programmable IC for crystal oscillators in 1996, the world's first programmable clock generator in 1995, and the world's first programmable skew buffer in 1998.[5] In its Annual Report discussing the 2001 fiscal year—the year in which the initial patent application was filed—Cypress Semiconductor noted that it was a "leader in the timing technology device market primarily due to [its] clocks and clock distribution circuits."[6] It explained that these circuits were "widely used" in personal computers, disk drives, modems, small office/home office network routers and hubs, digital video disks, and home video games.[7] At that time, Cypress Semiconductor was "the only supplier offering true field-programmable clocks," which had resulted in "clock outputs hav[ing] the desired characteristics of high drive, low jitter, low electro-magnetic interference and low skew."[8]

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[3] *See, e.g.*, https://www.businesswire.com/news/home/20030421005075/en/Cypress-Announces-Field-Programmable-Zero-Delay-Buffer; https://www.businesswire.com/news/home/20030930005313/en/Cypress-Announces-Industrys-Lowest-Total-Timing-Budget.

[4] *See* https://www.cypress.com/products/timing-solutions.

[5] *See id*.

[6] *See* Cypress Semiconductor Annual Report (2002) at 6, http://investors.cypress.com/node/7026/html.

[7] *Id*.

[8] *Id*.

11. The pioneering nature of the patented technology is attested to by the number of companies that have cited to the patents-in-suit: Agere Systems (now part of Broadcom), Altera (acquired by Intel), Boeing, Canon, Integrated Device Technology (now owned by Renesas), Lattice Semiconductor, Rambus, ROHM Semiconductor, Samsung, TSMC, and UMC.

COUNT I

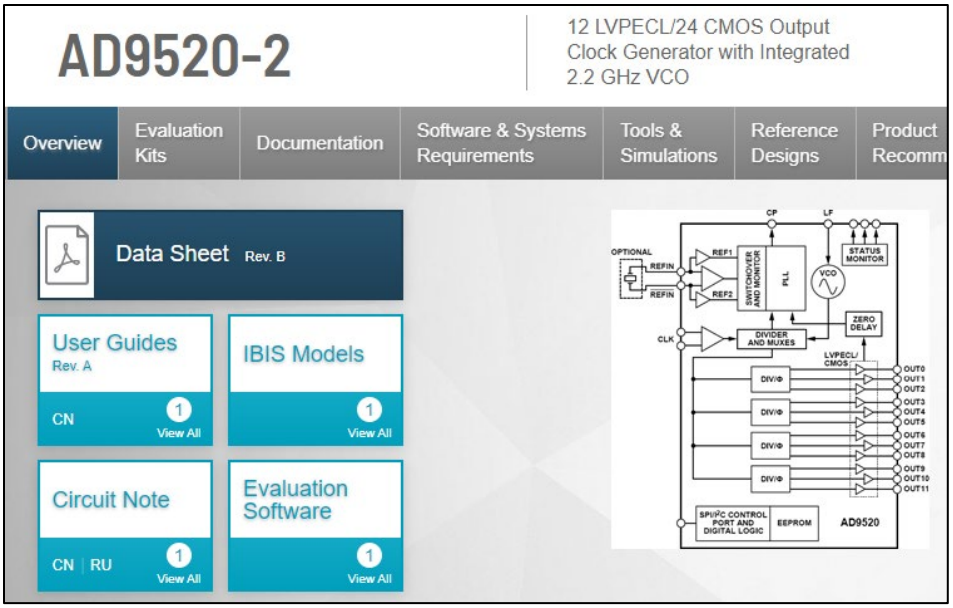
DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,608,530

12. On August 19, 2003, U.S. Patent No. 6,608,530 ("the '530 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques."

13. Liberty Patents is the owner of the '530 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '530 Patent against infringers, and to collect damages for all relevant times.

14. ADI made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its AD9520-2 clock generator and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[9] ("accused products"):

[9] *See, e.g.*, AD9520-0, AD9520-1, AD9520-3, AD9520-4, AD9522-0, AD9522-1, AD9522-2, AD9522-3, AD9522-4, AD9542, AD9543, D9544, AD9545, EVAL-AD9522-0, EVAL-AD9522-1, EVAL-AD9522-2, EVAL-AD9522-3, EVAL-AD9522-4, EVAL-AD9520-0, EVAL-AD9520-1, EVAL-AD9520-2, EVAL-AD9520-3, EVAL-AD9520-4, EVAL-AD9542, EVAL-AD9543, EVAL-AD9544, EVAL-AD9545.

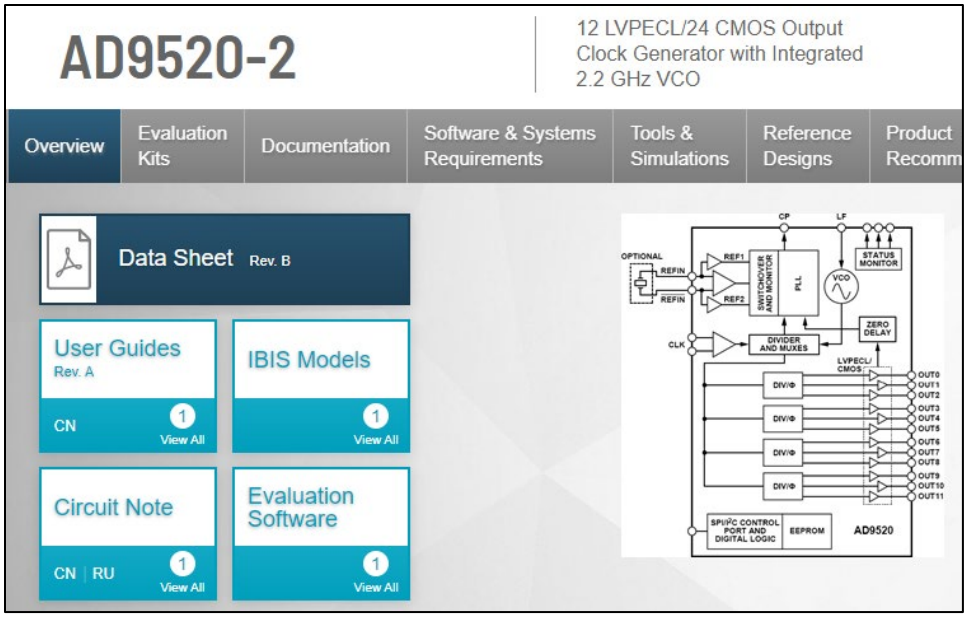


Source: https://www.analog.com/en/products/ad9520-2.html#product-overview

15. By doing so, ADI has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 15 of the '530 Patent. ADI's infringement in this regard is ongoing.

16. ADI's AD9520-2 clock generator is an exemplary product. It includes a first circuit configured to present a plurality of output clock signals in response to a reference clock signal and a feedback signal.

17. For example, ADI's AD9520-2 clock generator provides a multioutput clock distribution function with subpicosecond jitter performance. The device also provides a low output channel-to-channel skew or delay. It includes a phase locked loop (PLL) with dividers, a voltage-controlled oscillator (VCO), and filters ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The clock outputs are grouped together into four channels. Each channel consists of three LVPECL clock outputs or six CMOS clock outputs.



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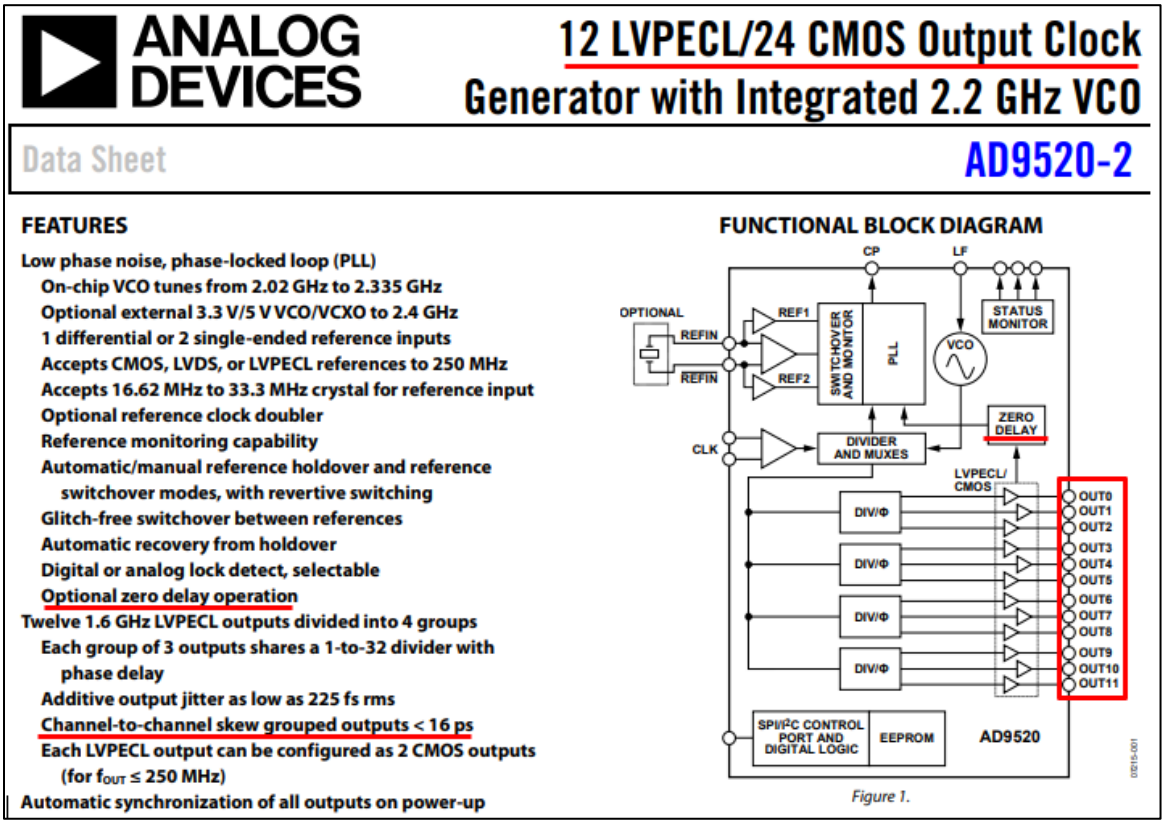

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

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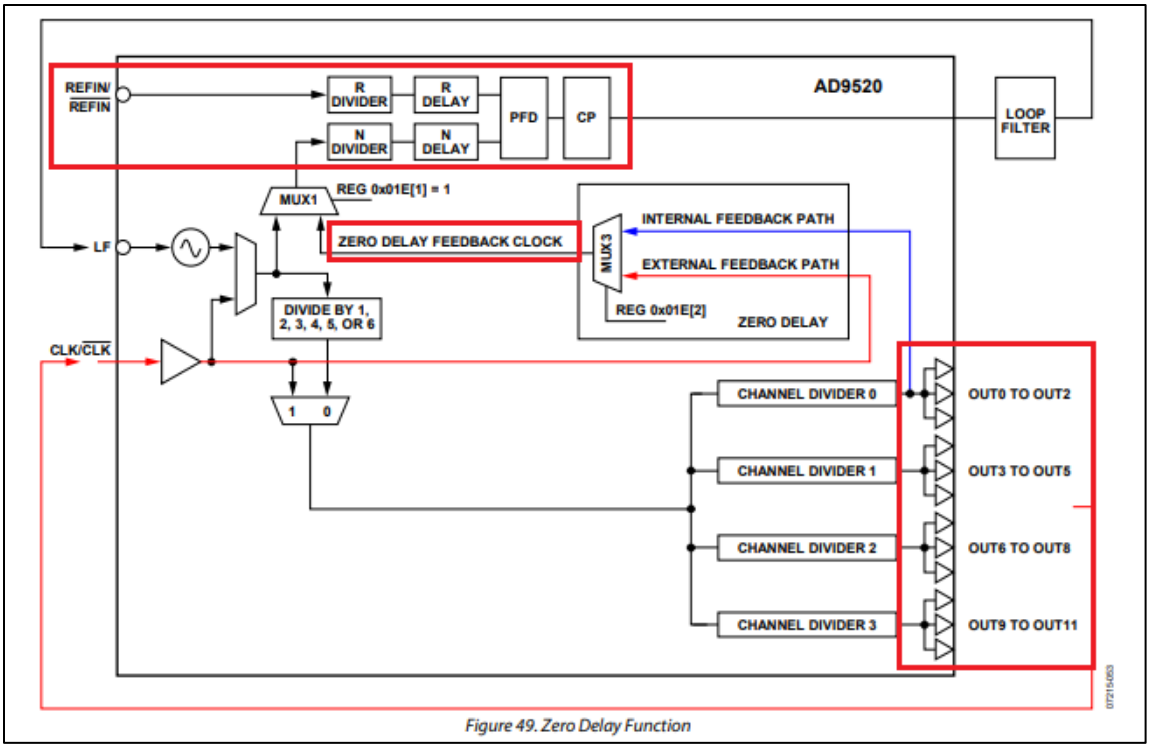

Figure 49. Zero Delay Function

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

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CLOCK DISTRIBUTION

A clock channel consists of three LVPECL clock outputs or six CMOS clock outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or CMOS at the pins.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

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External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red. Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/$\overline{\text{CLK}}$ pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

REFERENCE INPUTS Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 4)

18. ADI's AD9520-2 clock generator includes a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to a first control signal. The first control signal is configured to minimize a difference in delay between the plurality of output clock signals.

19. For example, ADI's AD9520-2 clock generator can generate multiple output clocks ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The feedback input can be internal or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal.

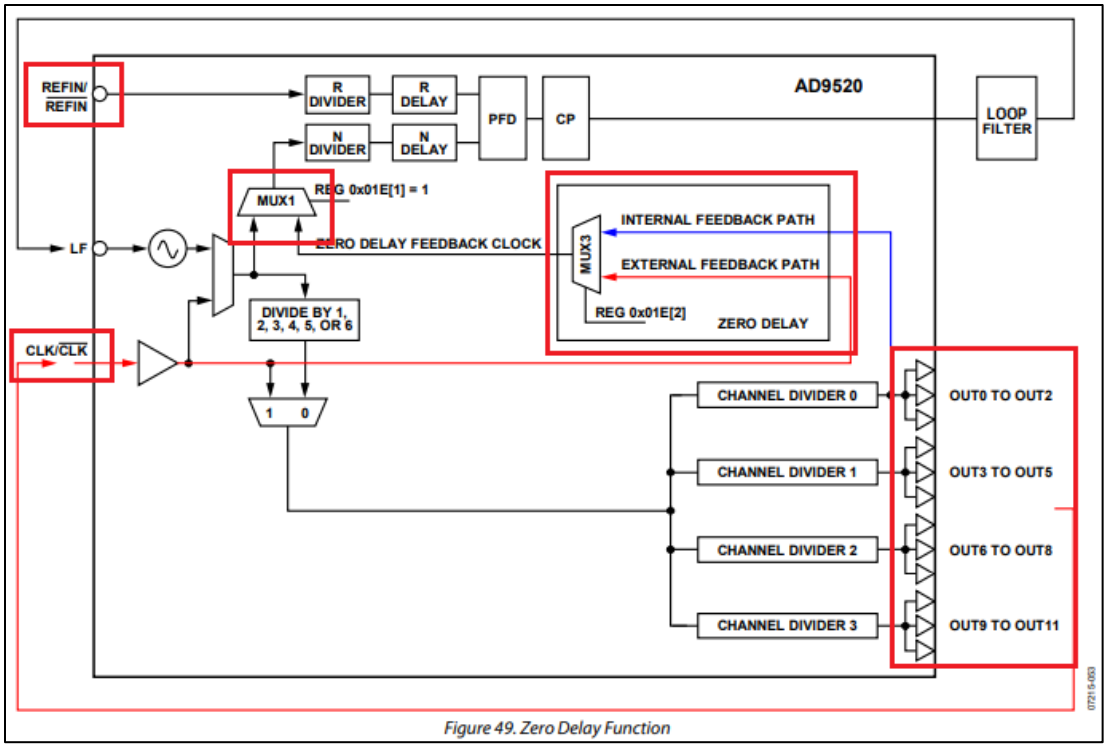
20. The user can specify which channel divider should be used for external zero delay mode using a register value (e.g., 0x01E). Based on that value, one of the channel dividers is selected for external feedback. One of the clock outputs (from the selected channel divider) is routed back as the external feedback signal. The AD9520-2 clock generator includes control logic or a control signal ("a first control signal") that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. It further includes a circuit ("a second circuit") that selects one of the clock outputs as the feedback signal based on the control signal. This second circuit is connected to all of the other divider channels and their clock outputs, and allows the AD9520-2 clock generator to operate as a closed-loop system for all the divider channels and their clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

21. The accuracy in generating the output clock signals minimizes the delay between them. Because the closed-loop configuration requires the control signal to select one of the clock outputs, the control signal is configured to minimize the delay between the output clock signals.

ZERO DELAY OPERATION

Zero delay operation aligns the phase of the output clocks with the phase of the external PLL reference input. There are two zero delay modes on the AD9520-2: internal and external.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 42)



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For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

The PLL synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the PLL components to minimize the phase offset between the feedback clock and the reference input.

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Twelve 1.6 GHz LVPECL outputs divided into 4 groups
- **Each group of 3 outputs shares a 1-to-32 divider with phase delay**
- **Additive output jitter as low as 225 fs rms**
- **Channel-to-channel skew grouped outputs < 16 ps**
- **Each LVPECL output can be configured as 2 CMOS outputs (for f_{OUT} ≤ 250 MHz)**

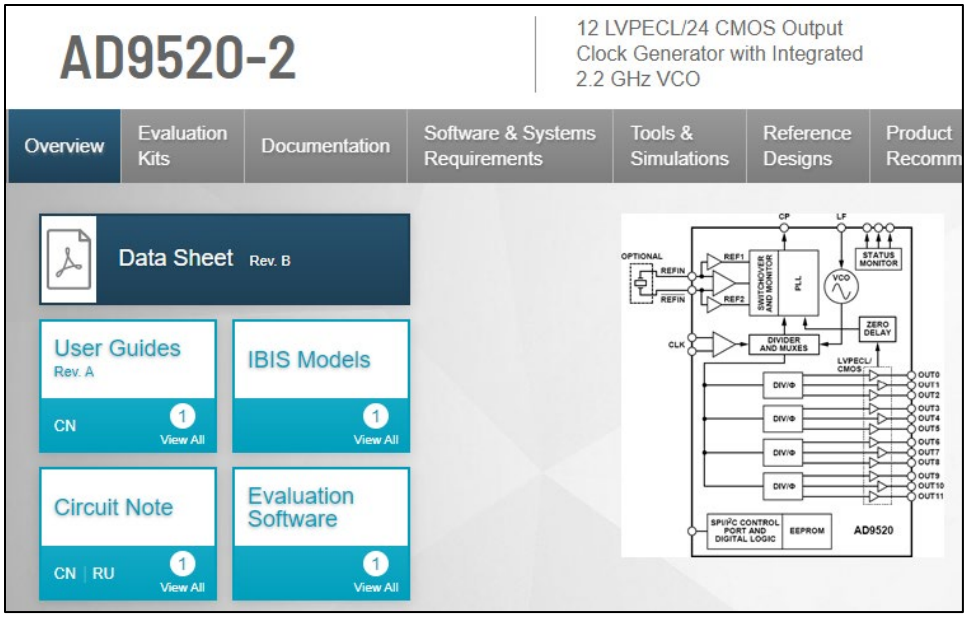
Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 1)

0x01E	[7:5]	Unused	Unused.		
	[4:3]	External zero delay feedback channel divider select	**Bit 4**	**Bit 3**	**Selection of Channel Divider for Use in the External Zero-Delay Path**
			0	0	Selects Channel Divider 0 (default).
			0	1	Selects Channel Divider 1.
			1	0	Selects Channel Divider 2.
			1	1	Selects Channel Divider 3.
	2	Enable external zero delay	Selects which zero delay mode to use. 0: enables internal zero delay mode if Register 0x01E[1] = 1 (default). 1: enables external zero delay mode if Register 0x01E[1] = 1.		

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 70)

22. ADI has infringed the '530 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of generating output clock signals in response to a reference clock signal and a feedback signal.

23. For example, ADI's AD9520-2 clock generator provides a multioutput clock distribution function with subpicosecond jitter performance. The device also provides a low output channel-to-channel skew or delay. It includes a phase locked loop (PLL) with dividers, a voltage-controlled oscillator (VCO), and filters for generating multiple clock outputs ("a plurality of output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The clock outputs are grouped together into four channels. Each channel consists of three LVPECL clock outputs or six CMOS clock outputs.



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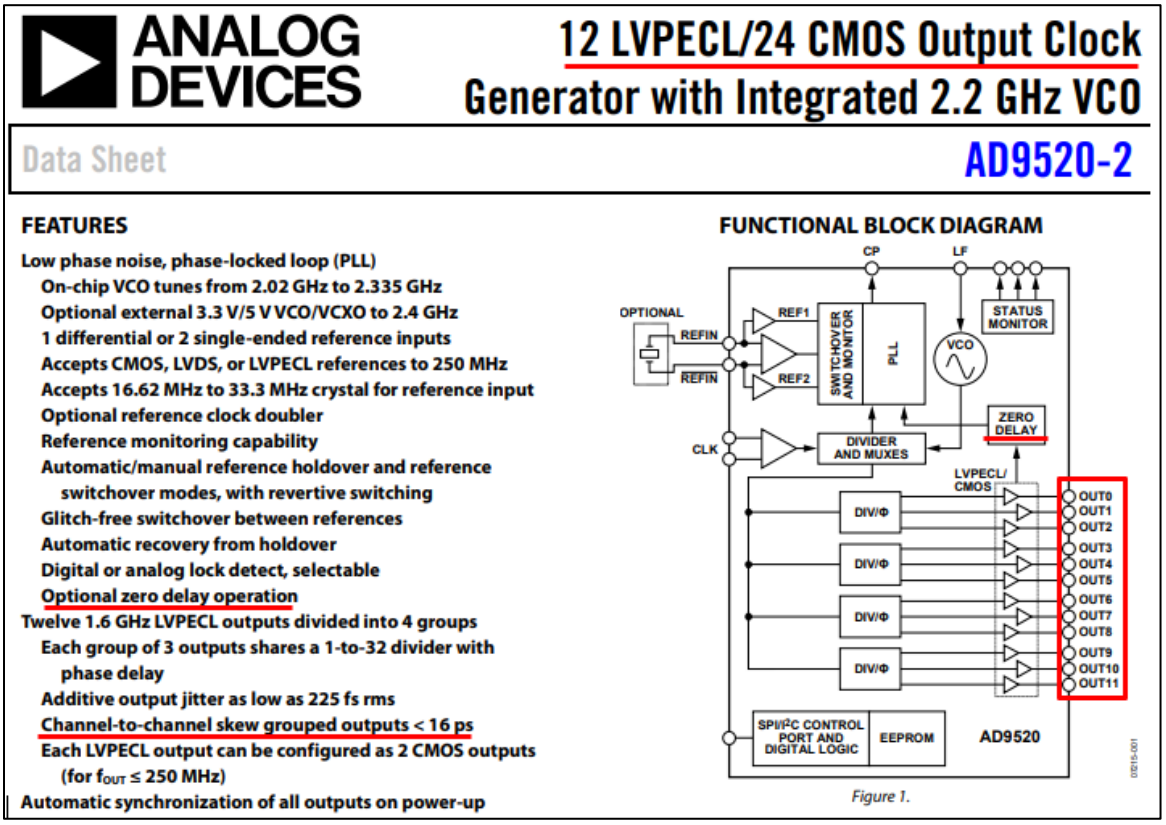

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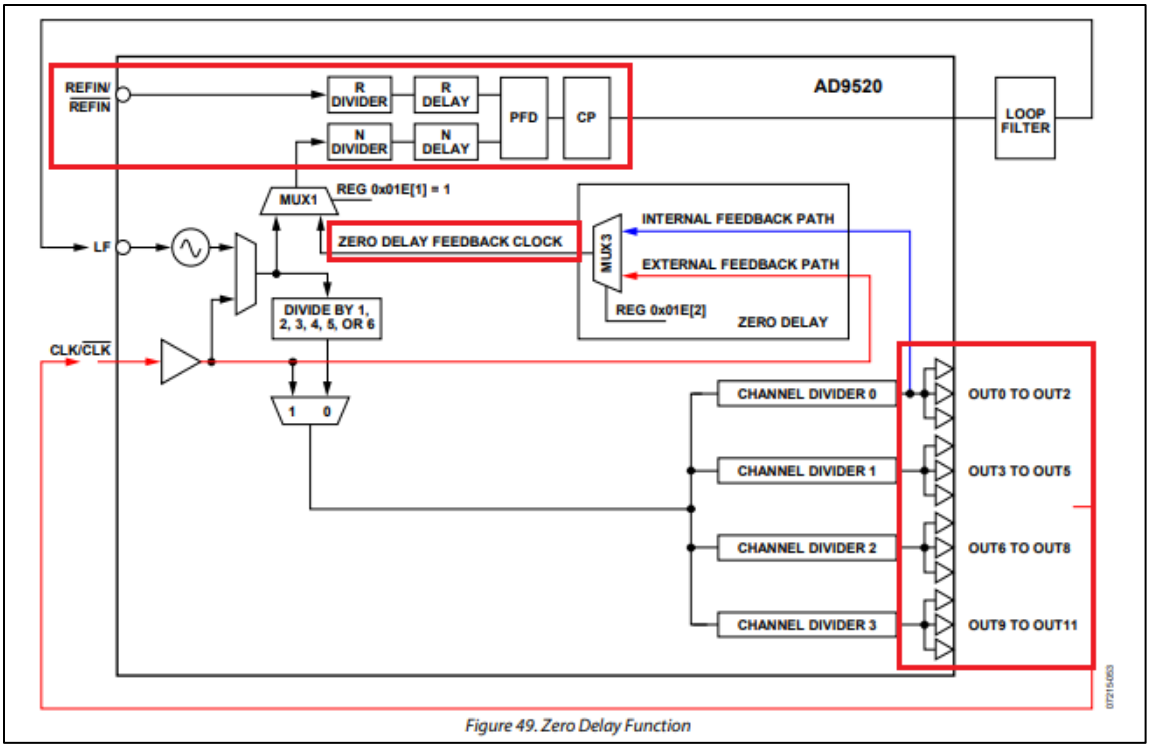

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REFERENCE INPUTS Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
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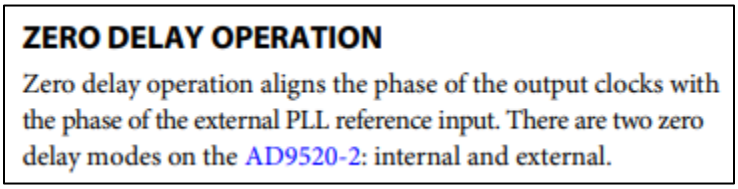
24. ADI has infringed the '530 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of selecting one of the output clock signals as the feedback signal in response to a control signal.

25. For example, ADI's AD9520-2 clock generator can generate multiple output clocks ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The feedback input can be internal or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal.

26. The user can specify which channel divider should be used for external zero delay mode using a register value (e.g., 0x01E). Based on that value, one of the channel dividers is selected for external feedback. One of the clock outputs (from the selected channel divider) is routed back as the external feedback signal. The AD9520-2 clock generator includes control logic or a control signal ("a control signal") that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. The circuit that selects one of the divider channels based on the control signal is connected to all of the other divider channels and their clock outputs. That circuit allows the AD9520-2 clock generator to operate as a closed-loop system for all the divider channels and their clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.



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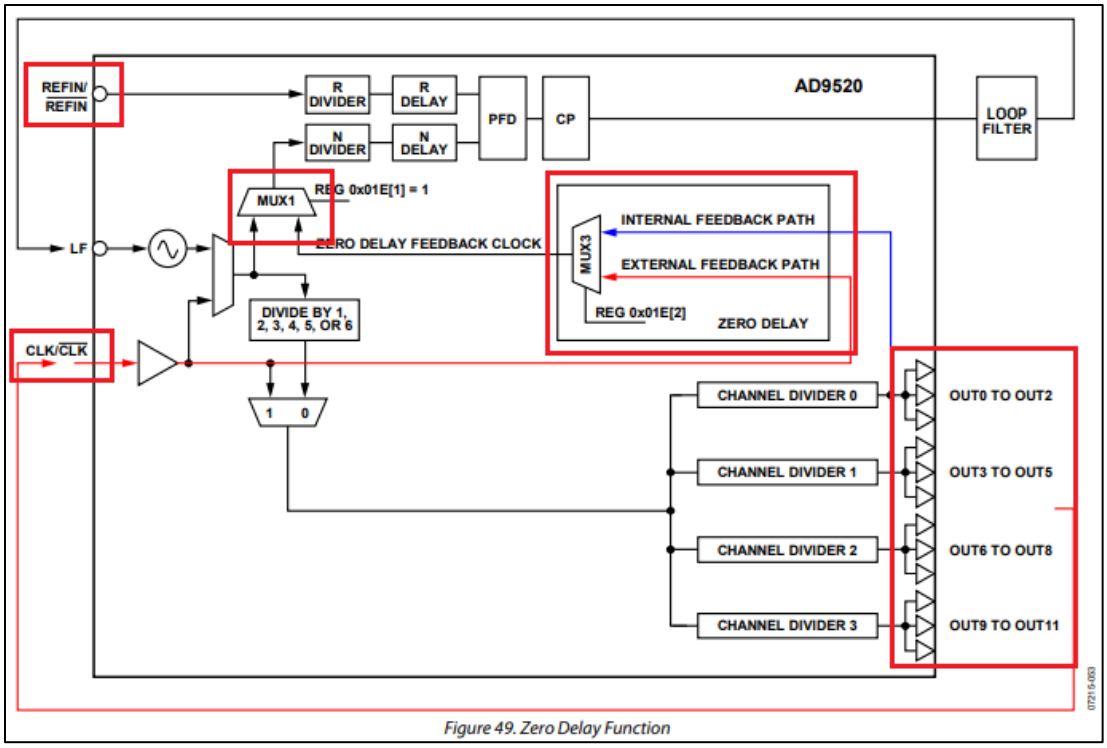

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For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

The PLL synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the PLL components to minimize the phase offset between the feedback clock and the reference input.

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(Page 43)

Twelve 1.6 GHz LVPECL outputs divided into 4 groups
- **Each group of 3 outputs shares a 1-to-32 divider with phase delay**
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- **Each LVPECL output can be configured as 2 CMOS outputs (for f_{OUT} ≤ 250 MHz)**

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Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 70)

27. ADI has had knowledge of the '530 Patent at least as of the date when it was notified of the filing of this action.

28. Liberty Patents has been damaged as a result of the infringing conduct by ADI alleged above. Thus, ADI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

29. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '530 Patent.

COUNT II

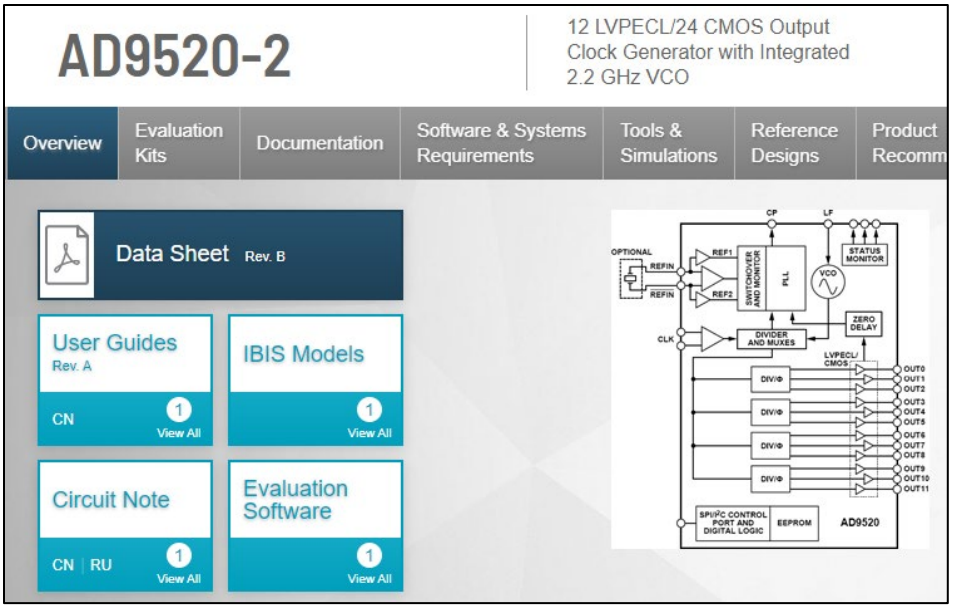
DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,734,740

30. On May 11, 2004, U.S. Patent No. 6,734,740 ("the '740 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques."

31. Liberty Patents is the owner of the '740 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '740 Patent against infringers, and to collect damages for all relevant times.

32. ADI made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its AD9520-2 clock generator and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[10] ("accused products"):

[10] *See, e.g.*, AD9520-0, AD9520-1, AD9520-3, AD9520-4, AD9522-0, AD9522-1, AD9522-2, AD9522-3, AD9522-4, AD9542, AD9543, D9544, AD9545, EVAL-AD9522-0, EVAL-AD9522-1, EVAL-AD9522-2, EVAL-AD9522-3, EVAL-AD9522-4, EVAL-AD9520-0, EVAL-AD9520-1, EVAL-AD9520-2, EVAL-AD9520-3, EVAL-AD9520-4, EVAL-AD9542, EVAL-AD9543, EVAL-AD9544, EVAL-AD9545.



Source: https://www.analog.com/en/products/ad9520-2.html#product-overview

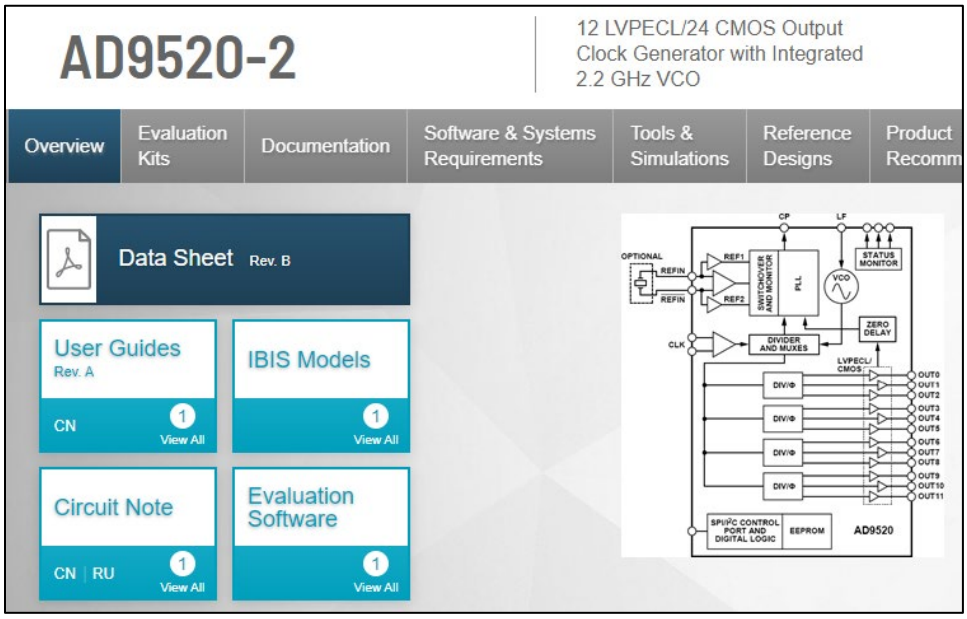
33. By doing so, ADI has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 16 of the '740 Patent. ADI's infringement in this regard is ongoing.

34. ADI's AD9520-2 is an exemplary product. It includes a first circuit configured to present a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

35. For example, ADI's AD9520-2 clock generator provides a multioutput clock distribution function with subpicosecond jitter performance. The device also provides a low output channel-to-channel skew or delay. It includes a phase locked loop (PLL) with dividers, a voltage-controlled oscillator (VCO), and filters ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal").

36. The clock outputs are grouped together into four channels. Each channel consists of three LVPECL clock outputs or six CMOS clock outputs. The feedback input can be internal

or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal using the value stored in a register (e.g., 0x01E). The AD9520-2 clock generator includes control logic or a control signal ("a first control signal") that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. The output clock signals are generated in response to the reference clock and this feedback signal. Accordingly, the control signal ("a first control signal") that selects the feedback signal is generated in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal").



Source: https://www.analog.com/en/products/ad9520-2.html#product-overview

ANALOG DEVICES

12 LVPECL/24 CMOS Output Clock Generator with Integrated 2.2 GHz VCO

Data Sheet **AD9520-2**

FEATURES

- Low phase noise, phase-locked loop (PLL)
  - On-chip VCO tunes from 2.02 GHz to 2.335 GHz
  - Optional external 3.3 V/5 V VCO/VCXO to 2.4 GHz
  - 1 differential or 2 single-ended reference inputs
  - Accepts CMOS, LVDS, or LVPECL references to 250 MHz
  - Accepts 16.62 MHz to 33.3 MHz crystal for reference input
  - Optional reference clock doubler
  - Reference monitoring capability
  - Automatic/manual reference holdover and reference switchover modes, with revertive switching
  - Glitch-free switchover between references
  - Automatic recovery from holdover
  - Digital or analog lock detect, selectable
  - Optional zero delay operation
- Twelve 1.6 GHz LVPECL outputs divided into 4 groups
  - Each group of 3 outputs shares a 1-to-32 divider with phase delay
  - Additive output jitter as low as 225 fs rms
  - Channel-to-channel skew grouped outputs < 16 ps
  - Each LVPECL output can be configured as 2 CMOS outputs (for $f_{OUT} \leq 250$ MHz)
- Automatic synchronization of all outputs on power-up

FUNCTIONAL BLOCK DIAGRAM

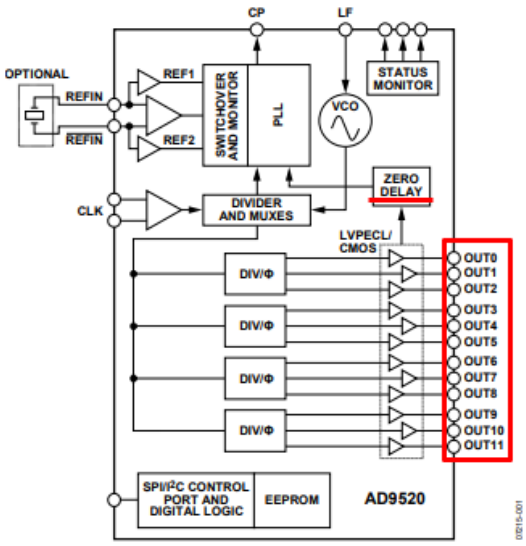


Figure 1.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 1)

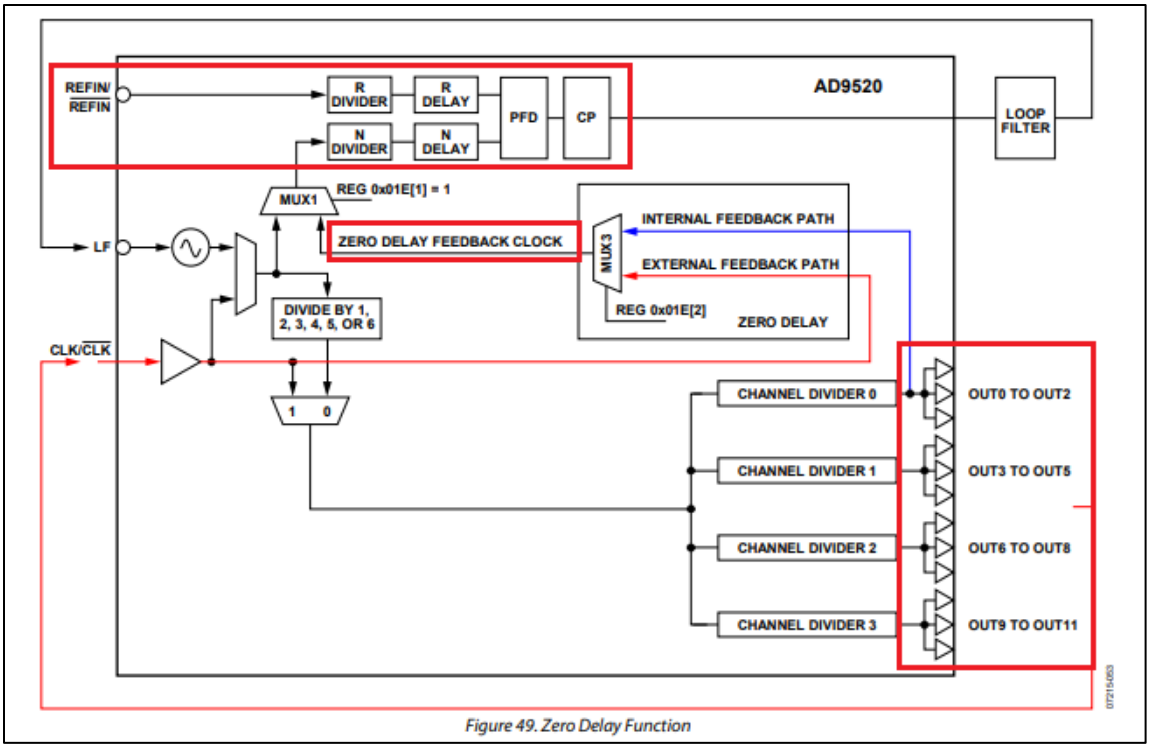


Figure 49. Zero Delay Function

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

CLOCK DISTRIBUTION

A clock channel consists of three LVPECL clock outputs or six CMOS clock outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or CMOS at the pins.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red.

Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/$\overline{\text{CLK}}$ pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43).

REFERENCE INPUTS Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 4)

37. ADI's AD9520-2 clock generator includes a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to the first control signal.

38. For example, ADI's AD9520-2 clock generator can generate multiple output clocks ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The feedback input can be internal or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal.

39. The user can specify which channel divider should be used for external zero delay mode using a register value (e.g., 0x01E). Based on that value, one of the channel dividers is selected for external feedback. One of the clock outputs (from the selected channel divider) is routed back as the external feedback signal. The AD9520-2 clock generator includes control logic or a control signal ("said first control signal") that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. It further includes a circuit ("a second circuit") that selects one of the clock outputs as the feedback signal based on the control signal. This second circuit is connected to all of the other divider channels and their clock outputs, and allows the AD9520-2 clock generator to operate as a closed-loop system for all the divider channels and their clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

40. The accuracy in generating the output clock signals minimizes the delay between them. Because the closed-loop configuration requires the control signal to select one of the clock outputs, the control signal is configured to minimize the delay between the output clock signals.

ZERO DELAY OPERATION

Zero delay operation aligns the phase of the output clocks with the phase of the external PLL reference input. There are two zero delay modes on the AD9520-2: internal and external.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 42)

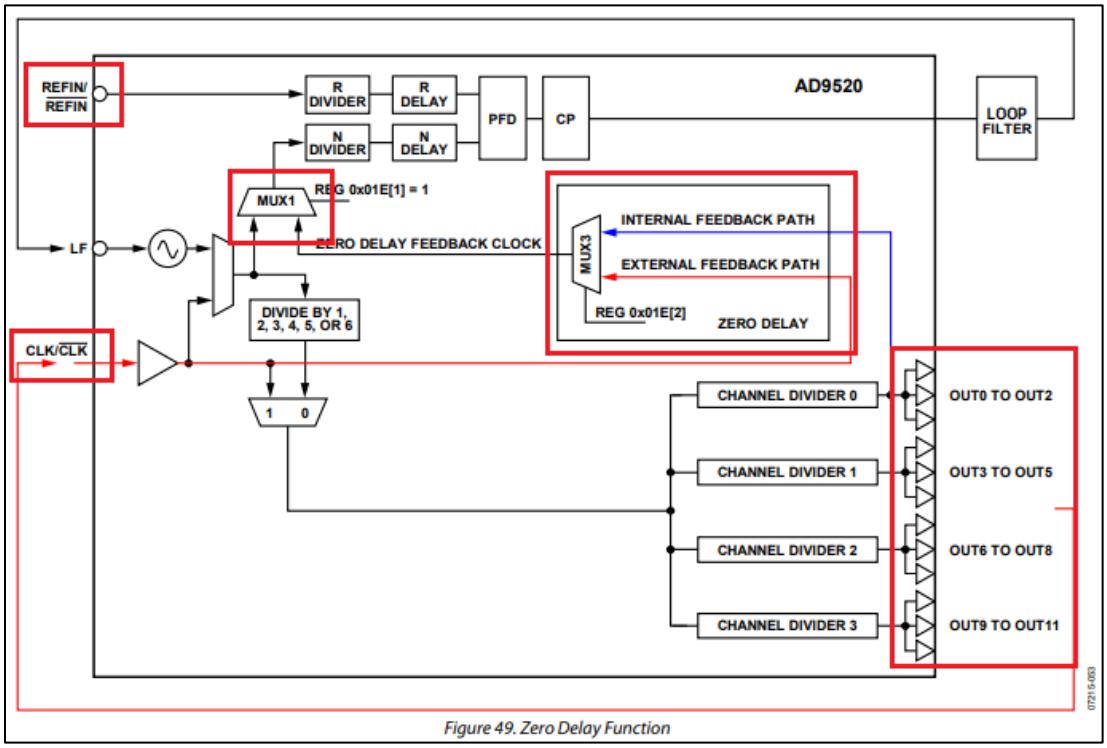


Figure 49. Zero Delay Function

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 43)

External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red.

Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/CLK pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

The PLL synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the PLL components to minimize the phase offset between the feedback clock and the reference input.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 43)

Twelve 1.6 GHz LVPECL outputs divided into 4 groups
- **Each group of 3 outputs shares a 1-to-32 divider with phase delay**
- **Additive output jitter as low as 225 fs rms**
- **Channel-to-channel skew grouped outputs < 16 ps**
- **Each LVPECL output can be configured as 2 CMOS outputs (for f_{OUT} ≤ 250 MHz)**

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 1)

0x01E	[7:5]	Unused	Unused.		
	[4:3]	External zero delay feedback channel divider select	**Bit 4**	**Bit 3**	**Selection of Channel Divider for Use in the External Zero-Delay Path**
			0	0	Selects Channel Divider 0 (default).
			0	1	Selects Channel Divider 1.
			1	0	Selects Channel Divider 2.
			1	1	Selects Channel Divider 3.
	2	Enable external zero delay	Selects which zero delay mode to use. 0: enables internal zero delay mode if Register 0x01E[1] = 1 (default). 1: enables external zero delay mode if Register 0x01E[1] = 1.		

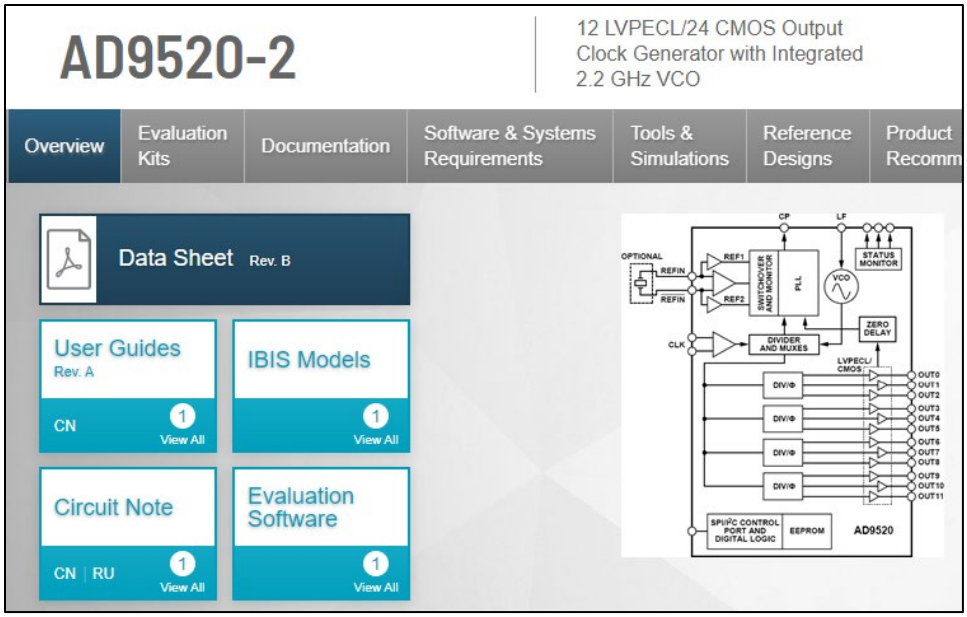
Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 70)

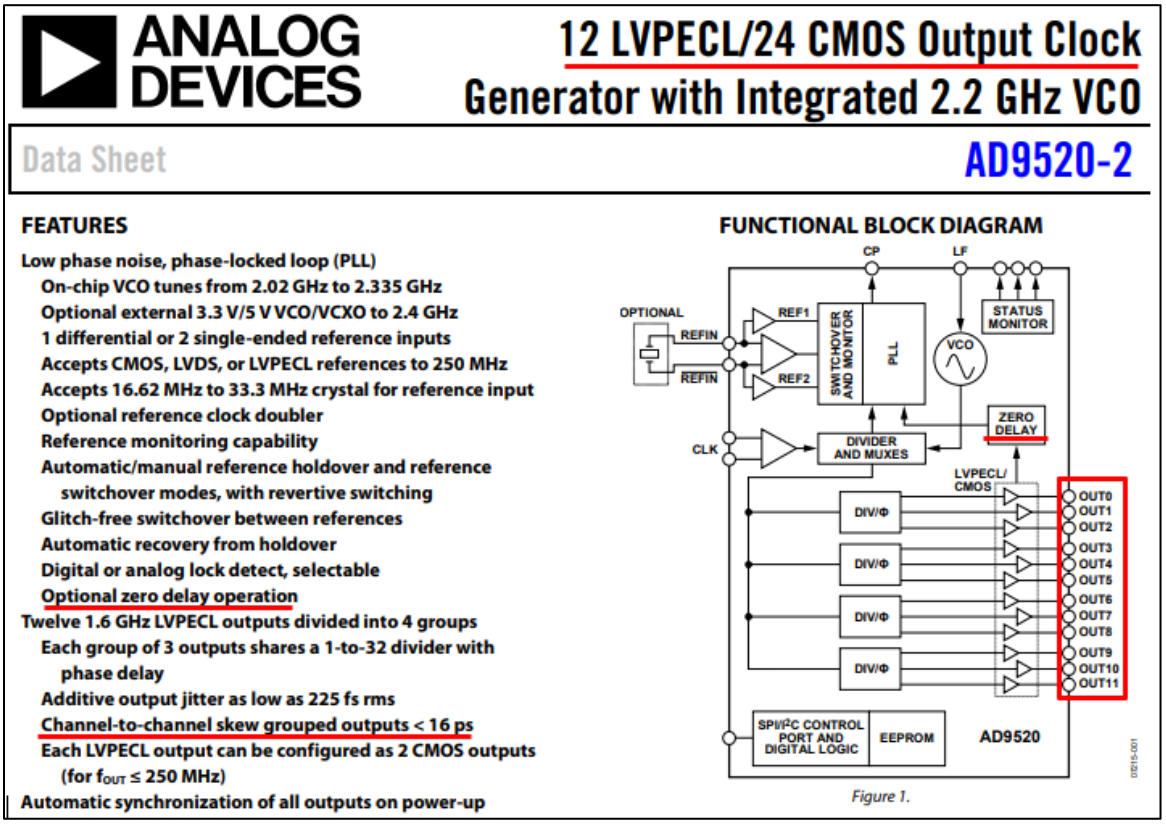
41. ADI has infringed the ’740 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of generating a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

42. For example, ADI’s AD9520-2 clock generator provides a multioutput clock distribution function with subpicosecond jitter performance. The device also provides a low output channel-to-channel skew or delay. It includes a phase locked loop (PLL) with dividers, a voltage-controlled oscillator (VCO), and filters for generating multiple clock outputs (“a plurality of output clock signals”) in response to a reference input (“a reference clock signal”) and a feedback input (“a feedback signal”). The clock outputs are grouped together into four channels. Each channel consists of three LVPECL clock outputs or six CMOS clock outputs.

43. The feedback input can be internal or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal using the value stored in a register (e.g., 0x01E). The AD9520-2 clock generator includes control logic or a control signal (“a first control signal”) that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. The output clock signals are generated in response to the reference clock and the feedback signal. Accordingly, the control signal (“a first control signal”) that selects the feedback signal is generated in response to a reference input (“a reference clock signal”) and a feedback input (“a feedback signal”).



Source: https://www.analog.com/en/products/ad9520-2.html#product-overview



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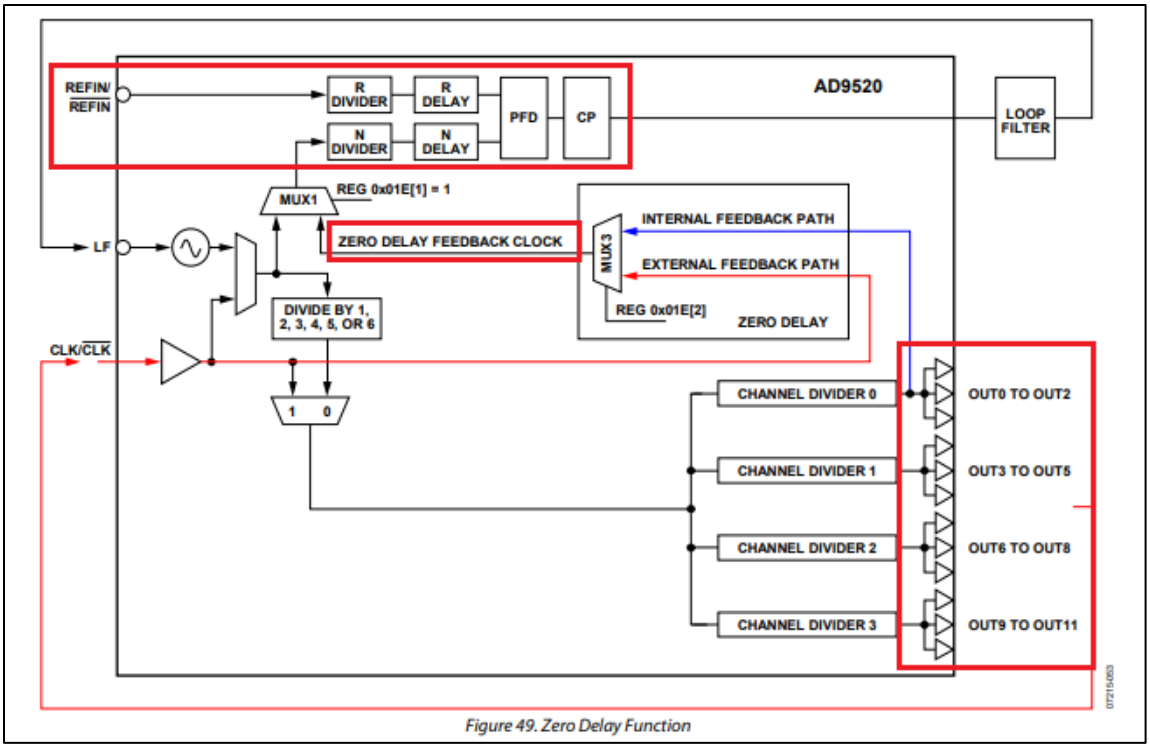

Figure 49. Zero Delay Function

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

CLOCK DISTRIBUTION

A clock channel consists of three LVPECL clock outputs or six CMOS clock outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or CMOS at the pins.

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External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red.

Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/$\overline{\text{CLK}}$ pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 43)

For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

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(Page 43).

REFERENCE INPUTS Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{OM} (self-bias voltage)
Input Sensitivity		280		mV p-p	PLL figure of merit (FOM) increases with increasing slew rate (see Figure 12); the input sensitivity is sufficient for ac-coupled LVDS and LVPECL signals
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 4)

<table>
<tr><td rowspan="6">0x01E</td><td>[7:5]</td><td>Unused</td><td colspan="3">Unused.</td></tr>
<tr><td rowspan="5">[4:3]</td><td rowspan="5">External zero delay feedback channel divider select</td><td>Bit 4</td><td>Bit 3</td><td>Selection of Channel Divider for Use in the External Zero-Delay Path</td></tr>
<tr><td>0</td><td>0</td><td>Selects Channel Divider 0 (default).</td></tr>
<tr><td>0</td><td>1</td><td>Selects Channel Divider 1.</td></tr>
<tr><td>1</td><td>0</td><td>Selects Channel Divider 2.</td></tr>
<tr><td>1</td><td>1</td><td>Selects Channel Divider 3.</td></tr>
<tr><td>2</td><td>Enable external zero delay</td><td colspan="3">Selects which zero delay mode to use.
0: enables internal zero delay mode if Register 0x01E[1] = 1 (default).
1: enables external zero delay mode if Register 0x01E[1] = 1.</td></tr>
</table>

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 70).

44. ADI has infringed the ’740 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of selecting one of the output clock signals as the feedback signal in response to the first control signal.

45. For example, ADI’s AD9520-2 clock generator can generate multiple output clocks (“said output clock signals”) in response to a reference input (“a reference clock signal”) and a feedback input (“a feedback signal”). The feedback input can be internal or external. When using the External Zero Delay mode, one of the twelve clock outputs is selected as the feedback signal.

46. The user can specify which channel divider should be used for external zero delay mode using a register value (e.g., 0x01E). Based on that value, one of the channel dividers is selected for external feedback. One of the clock outputs (from the selected channel divider) is routed back as the external feedback signal. The AD9520-2 clock generator includes control logic or a control signal (“said first control signal”) that selects the appropriate output clock signal to use as the external feedback signal based on the appropriate bits of the configuration/value in the register. The circuit that selects one of the divider channels based on the control signal is connected to all of the other divider channels and their clock outputs. That

circuit allows the AD9520-2 clock generator to operate as a closed-loop system for all the divider channels and their clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

ZERO DELAY OPERATION

Zero delay operation aligns the phase of the output clocks with the phase of the external PLL reference input. There are two zero delay modes on the AD9520-2: internal and external.

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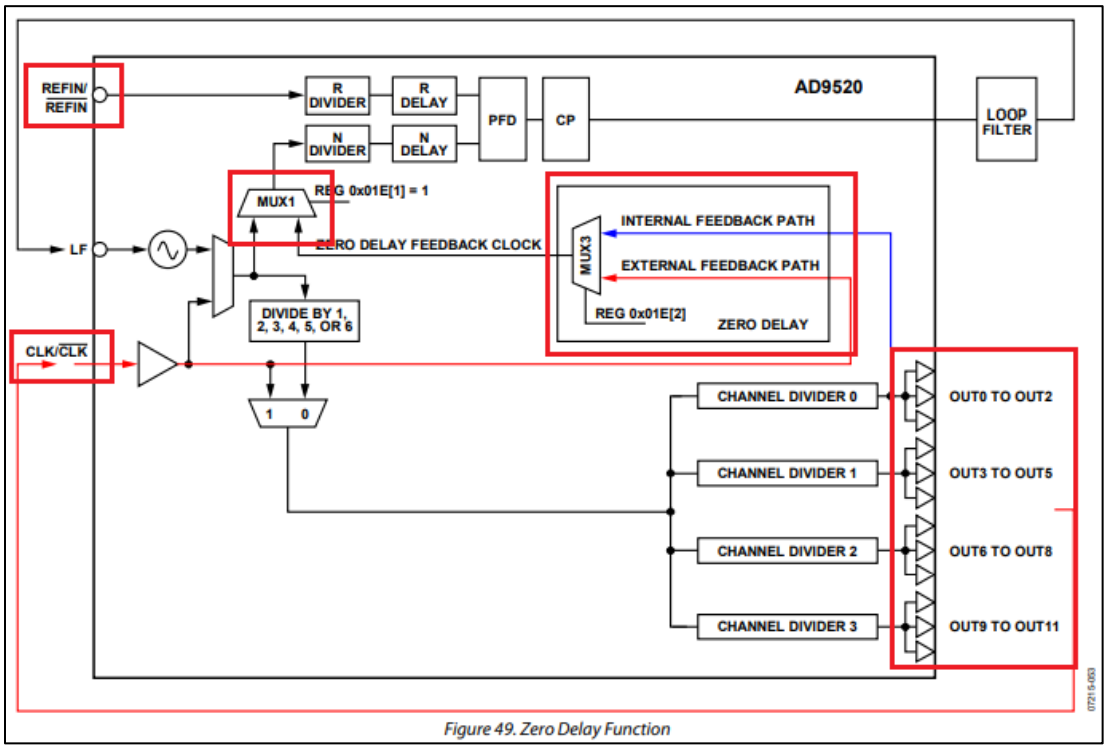

Figure 49. Zero Delay Function

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf (Page 43)

External Zero Delay Mode

The external zero delay function of the AD9520-2 is achieved by feeding one clock output back to the CLK input and ultimately back to the PLL N divider. In Figure 49, the change in signal routing for external zero delay mode is shown in red.

Set Register 0x01E[2:1] = 11b to select external zero delay mode. In external zero delay mode, one of the twelve output clocks (OUT0 to OUT11) can be routed back to the PLL (N divider) through the CLK/CLK pins and through MUX3 and MUX1. This feedback path is shown in red in Figure 49.

For VCO calibration to work correctly, the user must specify which channel divider is used for external zero delay mode. Channel Divider 0 is the default. Change the value in Register 0x01E[4:3] to select Channel Divider 1, Channel Divider 2, or Channel Divider 3 for zero delay feedback.

The PLL synchronizes the phase/edge of the feedback output clock with the phase/edge of the reference input. Because the channel dividers are synchronized to each other, the clock outputs are synchronous with the reference input. Both the R delay and the N delay inside the PLL can be programmed to compensate for the propagation delay from the PLL components to minimize the phase offset between the feedback clock and the reference input.

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(Page 43)

Twelve 1.6 GHz LVPECL outputs divided into 4 groups
- **Each group of 3 outputs shares a 1-to-32 divider with phase delay**
- **Additive output jitter as low as 225 fs rms**
- **Channel-to-channel skew grouped outputs < 16 ps**
- **Each LVPECL output can be configured as 2 CMOS outputs (for f_{OUT} ≤ 250 MHz)**

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(Page 1)

0x01E	[7:5]	Unused	Unused.		
	[4:3]	External zero delay feedback channel divider select	**Bit 4**	**Bit 3**	**Selection of Channel Divider for Use in the External Zero-Delay Path**
			0	0	Selects Channel Divider 0 (default).
			0	1	Selects Channel Divider 1.
			1	0	Selects Channel Divider 2.
			1	1	Selects Channel Divider 3.
	2	Enable external zero delay	Selects which zero delay mode to use. 0: enables internal zero delay mode if Register 0x01E[1] = 1 (default). 1: enables external zero delay mode if Register 0x01E[1] = 1.		

Source: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9520-2.pdf

(Page 70)

47. ADI has had knowledge of the ’740 Patent at least as of the date when it was notified of the filing of this action.

48. Liberty Patents has been damaged as a result of the infringing conduct by ADI alleged above. Thus, ADI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

49. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the ’740 Patent.

ADDITIONAL ALLEGATIONS REGARDING INFRINGEMENT AND PERSONAL JURISDICTION

50. ADI has also indirectly infringed the ’530 Patent and the ’740 Patent by inducing others to directly infringe the ’530 Patent and the ’740 Patent.

51. ADI has induced the end users and/or ADI’s customers to directly infringe (literally and/or under the doctrine of equivalents) the ’530 Patent and the ’740 Patent by using the accused products.

52. ADI took active steps, directly and/or through contractual relationships with others, with the specific intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

53. Such steps by ADI included, among other things, advising or directing customers and end users to use the accused products in an infringing manner; advertising and promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner.

54. ADI performed these steps, which constitute induced infringement, with the knowledge of the ’530 Patent and the ’740 Patent and with the knowledge that the induced acts constitute infringement.

55. ADI was and is aware that the normal and customary use of the accused products by ADI’s customers would infringe the ’530 Patent and the ’740 Patent. ADI’s inducement is ongoing.

56. ADI has also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates’ behalf, to directly infringe (literally and/or under the doctrine of equivalents) the ’530 Patent and the ’740 Patent by importing, selling or offering to sell the accused products.

57. ADI has a significant role in placing the accused products in the stream of commerce with the expectation and knowledge that they will be purchased by consumers in Texas and elsewhere in the United States.

58. ADI purposefully directs or controls the making of accused products and their shipment to the United States, using established distribution channels, for sale in Texas and elsewhere within the United States.

59. ADI purposefully directs or controls the sale of the accused products into established United States distribution channels, including sales to nationwide retailers. ADI’s established United States distribution channels include one or more United States based affiliates.

60. ADI purposefully directs or controls the sale of the accused products online and in nationwide retailers, including for sale in Texas and elsewhere in the United States, and expects and intends that the accused products will be so sold.

61. ADI purposefully places the accused products—whether by itself or through subsidiaries, affiliates, or third parties—into an international supply chain, knowing that the accused products will be sold in the United States, including Texas. Therefore, ADI also facilitates the sale of the accused products in Texas.

62. ADI took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the ’530 Patent and the ’740 Patent, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

63. Such steps by ADI included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing that such importation or sale would occur; and directing, facilitating, or influencing its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates’ behalf, to import, sell, or offer to sell the accused products in an infringing manner.

64. ADI performed these steps, which constitute induced infringement, with the knowledge of the ’530 Patent and the ’740 Patent, and with the knowledge that the induced acts would constitute infringement.

65. ADI performed such steps in order to profit from the eventual sale of the accused products in the United States.

66. ADI’s inducement is ongoing.

67. ADI has also indirectly infringed by contributing to the infringement of the ’530 Patent and the ’740 Patent. ADI has contributed to the direct infringement of the ’530 Patent and the ’740 Patent by the end user of the accused products.

68. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the ’530 Patent and the ’740 Patent, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

69. The special features include, for example, circuitry that reduces the delay between output clock signals in a zero delay buffer used in a manner that infringes the ’530 Patent and the ’740 Patent.

70. These special features constitute a material part of the invention of one or more of the claims of the ’530 Patent and the ’740 Patent, and are not staple articles of commerce suitable for substantial non-infringing use.

71. ADI’s contributory infringement is ongoing.

72. ADI has had actual knowledge of the ’530 Patent and the ’740 Patent at least as of the date when it was notified of the filing of this action. Since at least that time, ADI has known the scope of the claims of the ’530 Patent and the ’740 Patent, the products that practice the ’530 Patent and the ’740 Patent, and that Liberty Patents is the owner of the ’530 Patent and the ’740 Patent.

73. By the time of trial, ADI will have known and intended (since receiving such notice) that its continued actions would infringe and actively induce and contribute to the infringement of one or more claims of the ’530 Patent and the ’740 Patent.

74. Furthermore, ADI has a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of Liberty Patents’ patent rights. *See, e.g.*, M. Lemley, “Ignoring Patents,” 2008 Mich. St. L. Rev. 19 (2008).

75. ADI's actions are at least objectively reckless as to the risk of infringing valid patents, and this objective risk was either known or should have been known by ADI. ADI has knowledge of the '530 Patent and the '740 Patent.

76. ADI's customers have infringed the '530 Patent and the '740 Patent. ADI has encouraged its customers' infringement.

77. ADI's direct and indirect infringement of the '530 Patent and the '740 Patent has been, and/or continues to be willful, intentional, deliberate, and/or in conscious disregard of Liberty Patents' rights under the patents-in-suit.

78. Liberty Patents has been damaged as a result of ADI's infringing conduct alleged above. Thus, ADI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Liberty Patents hereby requests a trial by jury on all issues so triable by right.

PRAYER FOR RELIEF

Liberty Patents requests that the Court find in its favor and against ADI, and that the Court grant Liberty Patents the following relief:

a. Judgment that one or more claims of the '530 Patent and the '740 Patent have been infringed, either literally and/or under the doctrine of equivalents, by ADI and/or all others acting in concert therewith;

b. A permanent injunction enjoining ADI and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the '530 Patent and the '740 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the '530 Patent and the '740

Patent by such entities;

c. Judgment that ADI account for and pay to Liberty Patents all damages to and costs incurred by Liberty Patents because of ADI's infringing activities and other conduct complained of herein, including an award of all increased damages to which Liberty Patents is entitled under 35 U.S.C. § 284;

d. That Liberty Patents be granted pre-judgment and post-judgment interest on the damages caused by ADI's infringing activities and other conduct complained of herein;

e. That this Court declare this an exceptional case and award Liberty Patents its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285; and

f. That Liberty Patents be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: January 22, 2021

Respectfully submitted,

/s/ *Zachariah S. Harrington*

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