IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

LIBERTY PATENTS, LLC, Plaintiff, v. LATTICE SEMICONDUCTOR CORPORATION, Defendant.	CIVIL ACTION NO. 6:21-cv-61 ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Liberty Patents, LLC ("Liberty Patents" or "Plaintiff") files this original complaint against Defendant Lattice Semiconductor Corporation ("Lattice" or "Defendant"), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

PARTIES

1. Liberty Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas 75703.

2. Defendant Lattice Semiconductor Corporation is a company organized and existing under the laws of the state of Delaware. Lattice Semiconductor Corporation may be served with process through its registered agent, Corporation Service Company d/b/a/ CSC-Lawyers Incorporating Service Company at 211 East 7th Street, Suite 620, Austin, Texas, 78701-3218.

3. Lattice describes itself as a "global leader in smart connectivity solutions, providing market leading intellectual property and low-power, small form-factor devices that enable more than 8,000 global customers to quickly deliver innovative and differentiated cost

and power efficient products."[1] It is the world's largest volume supplier of FPGAs.[2] According to Lattice, "[a]n FPGA's parallel architecture enables faster processing than competing devices, such as microcontrollers, allowing for a user experience with shorter pauses and fewer delays."[3]

4. Further, Lattice states that its "FPGAs are among the lowest power consumption in the industry, enabling the application processor and other high-power components to remain dormant longer, resulting in longer battery life."[4] Lattice also states that it enables thinner end products than others in the industry.[5]

JURISDICTION AND VENUE

5. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

6. This Court has personal jurisdiction over Lattice pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) Lattice has done and continues to do business in Texas; (ii) Lattice has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas,

[1] https://ir.latticesemi.com/

[2] https://ir.latticesemi.com/static-files/1a0364e1-427b-475e-a979-092577f59207.

[3] Lattice Semiconductor Corp. Form 10-K at 5 (2019), https://ir.latticesemi.com/static-files/845b07bb-eb8f-48ff-97ba-0bcdb2b4b563.

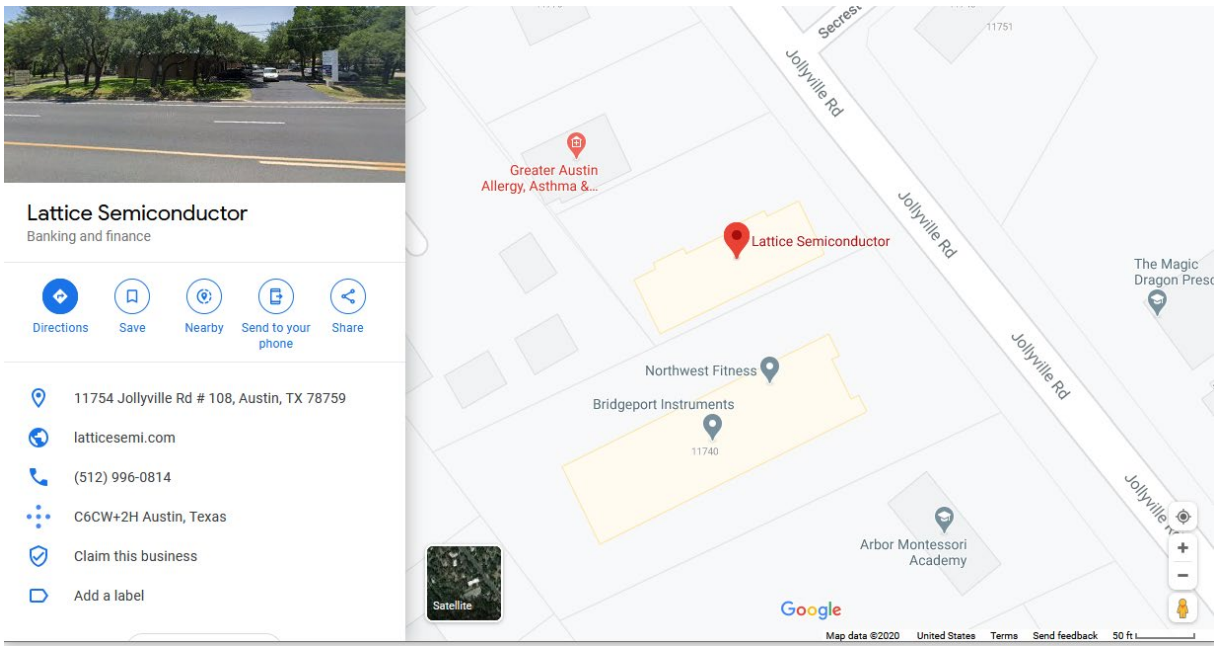
[4] *Id*.

[5] *Id*.

and/or committing a least a portion of any other infringements alleged herein in Texas, and (iii) Lattice is registered to do business in Texas.

7. Venue is proper in this district under 28 U.S.C. § 1400(b). Venue is further proper because Lattice has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a portion of any other infringements alleged herein in this district.

8. Lattice also has a regular and established places of business in this district, including at least at 11754 Jollyville Rd., #108, Austin, Texas, 78759:



Source: https://goo.gl/maps/fSg65aoPYQMH8Boa9

BACKGROUND

9. The patents-in-suit generally relate to zero delay buffer (ZDB) technology. In particular, they teach ZDB technology with multiple output clock signals—instantiations of a reference input clock signal—with predicted delay. The inventions of the patents-in-suit afforded the industry with numerous enhancements, some of which included product robustness, multiplexed feedback, minimization of delay between output clock signals, programmability, and approximating a closed-loop system to mitigate variations in temperature, supply voltage, supply ground, and/or output loading effects.

10. The patented technology was developed by engineers at Cypress Semiconductor Corp., which is one of the preeminent semiconductor design and manufacturing companies in the world today. In the early 2000s, when the patents-in-suit were filed, Cypress Semiconductor was a world leader in timing-technology solutions and specifically, was leading all other companies in the clock distribution arena.[6]

11. Cypress Semiconductor is a pioneer in the area of programmable clocks, having been in the "Timing Solutions" industry since the late 1990s.[7] Indeed, Cypress Semiconductor invented the world's first programmable IC for crystal oscillators in 1996, the world's first programmable clock generator in 1995, and the world's first programmable skew buffer in 1998.[8] In its Annual Report discussing the 2001 fiscal year—the year in which the initial patent application was filed—Cypress Semiconductor noted that it was a "leader in the timing

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[6] *See, e.g.*, https://www.businesswire.com/news/home/20030421005075/en/Cypress-Announces-Field-Programmable-Zero-Delay-Buffer; https://www.businesswire.com/news/home/20030930005313/en/Cypress-Announces-Industrys-Lowest-Total-Timing-Budget.

[7] *See* https://www.cypress.com/products/timing-solutions.

[8] *See id*.

technology device market primarily due to [its] clocks and clock distribution circuits."[9] It explained that these circuits were "widely used" in personal computers, disk drives, modems, small office/home office network routers and hubs, digital video disks, and home video games.[10] At that time, Cypress Semiconductor was "the only supplier offering true field-programmable clocks," which had resulted in "clock outputs hav[ing] the desired characteristics of high drive, low jitter, low electro-magnetic interference and low skew."[11]

12. The pioneering nature of the patented technology is attested to by the number of companies that have cited to the patents-in-suit: Agere Systems (now part of Broadcom), Altera (acquired by Intel), Boeing, Canon, Integrated Device Technology (now owned by Renesas), Lattice Semiconductor, Rambus, ROHM Semiconductor, Samsung, TSMC, and UMC.

COUNT I

DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,608,530

13. On August 19, 2003, U.S. Patent No. 6,608,530 ("the '530 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques."

14. Liberty Patents is the owner of the '530 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '530 Patent against infringers, and to collect damages for all relevant times.

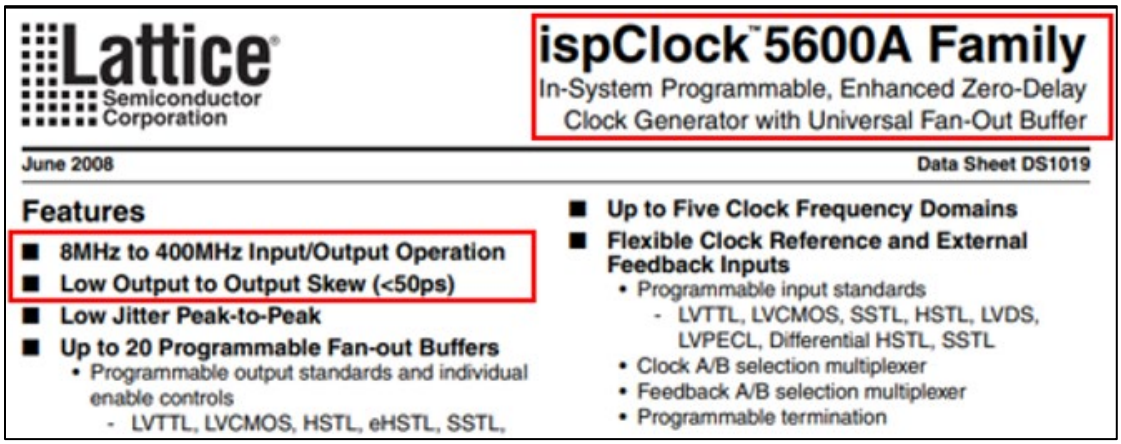
15. Lattice made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its ispClock 5600A

[9] *See* Cypress Semiconductor Annual Report (2002) at 6, http://investors.cypress.com/node/7026/html.

[10] *Id*.

[11] *Id*.

Family devices and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[12] ("accused products"):



Source: https://www.latticesemi.com/-/media/LatticeSemi/Documents/DataSheets/ispClock/ispClock5600AFamilyDataSheet.ashx?document_id=18324[13] (Page 1); https://www.fpgakey.com/lattice-family/ispclock-5500-family

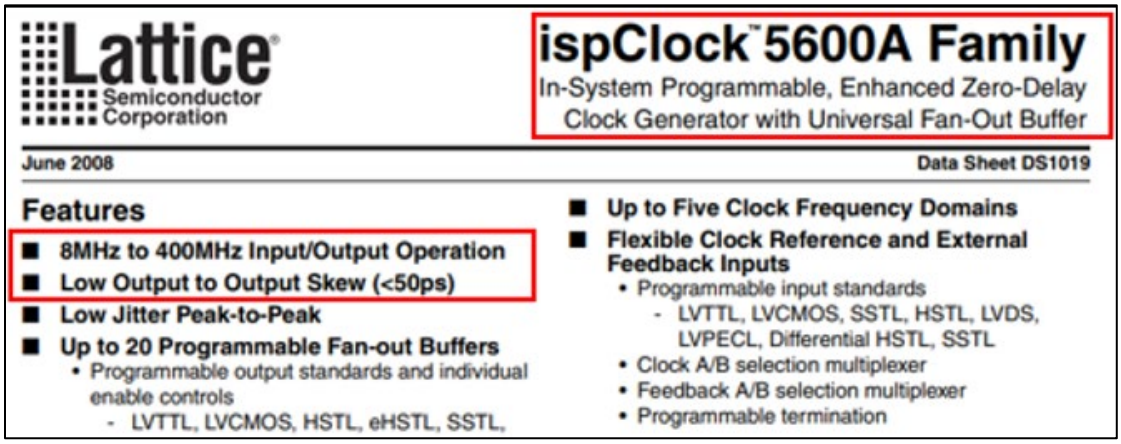
16. By doing so, Lattice has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 15 of the '530 Patent. Lattice's infringement in this regard is ongoing.

[12] *See, e.g.*, ispClock5610A, ispClock5620A, ispClock5610, ispClock5620, ispClock5510, ispClock5520, ispClock5320S, ispClock5316S, ispClock5312S, ispClock5308S, ispClock5304S, ispClock5410D, ispClock5406D, ispClock5406D, ispClock5406D, ispClock5610, ispClock5620, ispClock5620, ispClock5620A, ispClock5520, ispClock5620A, ispClock5312S, ispClock5406D, LFE5UM-25, LFE5UM-45, LFE5UM-85, LFE5UM5G-45, LFE5UM5G-25, LFE5U-12, LFE5U-25, LFE5U-45, LFE5U-85, LAE5U-12, LAE5U-25, LAE5U-45, ECP3-17, ECP3-35, ECP3-70, ECP3-95, ECP3-150, LA-ECP3-17, LA-ECP3-35.

[13] This link will be hereinafter be referred to as "Lattice ispClock5600A Family Datasheet."

17. Lattice's ispClock 5600A Family devices are exemplary products. They include a first circuit configured to present a plurality of output clock signals in response to a reference clock signal and a feedback signal.

18. For example, Lattice's ispClock 5600A Family devices are enhanced zero delay clock generators that help in minimizing the output-to-output skew or delay. These devices include a phase locked loop (PLL) with multiple divider circuits, a phase/frequency divider detector, a filter, a voltage-controller oscillator (VCO), and output drivers ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal").


Lattice Semiconductor Corporation

ispClock™5600A Family

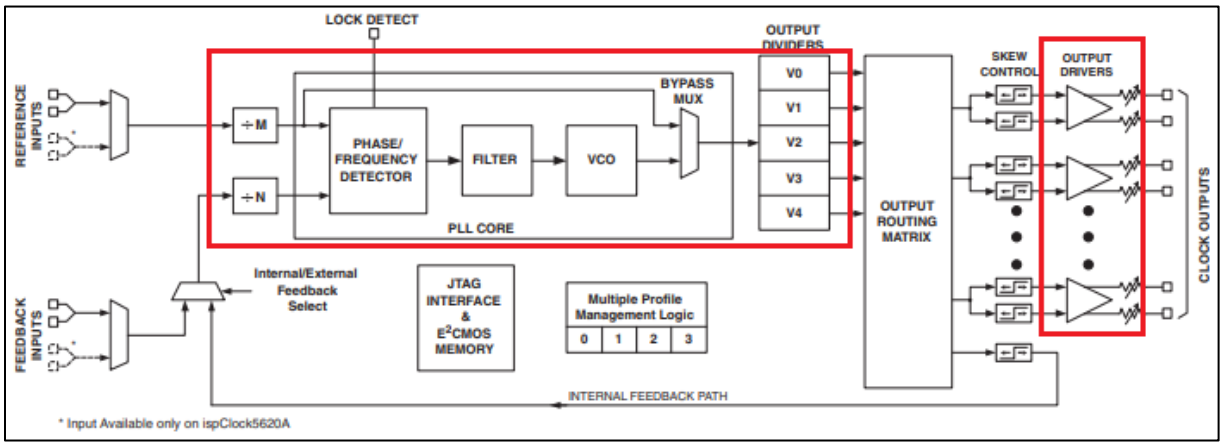
In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 Data Sheet DS1019

Features

- 8MHz to 400MHz Input/Output Operation
- Low Output to Output Skew (<50ps)
- Low Jitter Peak-to-Peak
- Up to 20 Programmable Fan-out Buffers
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL,
- Up to Five Clock Frequency Domains
- Flexible Clock Reference and External Feedback Inputs
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination

Source: Lattice ispClock5600A Family Datasheet (Page 1)



Source: Lattice ispClock5600A Family Datasheet (Page 1)

Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

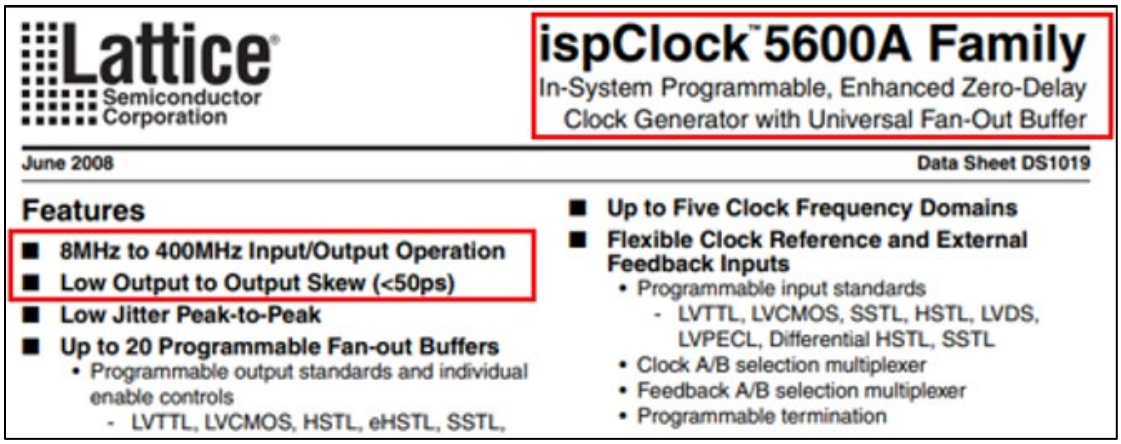
19. Lattice's ispClock 5600A Family devices include a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to a first control signal. The first control signal is configured to minimize a difference in delay between the plurality of output clock signals.

20. For example, Lattice's ispClock 5600A Family devices can generate multiple clock outputs ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The feedback input can be internal or external. When using internal feedback, one of the multiple clock outputs is selected as the feedback signal.

21. The following citations show that only one of the clock outputs is selected as the internal feedback signal, which is fed to a Feedback Skew Adjust block. The devices include

control logic or a control signal ("a first control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. They further include circuitry ("a second circuit") that selects one of the clock outputs as the feedback signal based on the control signal. This circuitry ("a second circuit") is connected to all of the clock outputs and allows the ispClock 5600A Family devices to operate as a closed-loop system for all of the clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

22. The accuracy in generating the output clock signals minimizes the delay between them. Because the closed-loop configuration requires the control signal to select one of the clock outputs, the control signal is configured to minimize the delay between the output clock signals.



Lattice Semiconductor Corporation

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Features

- 8MHz to 400MHz Input/Output Operation
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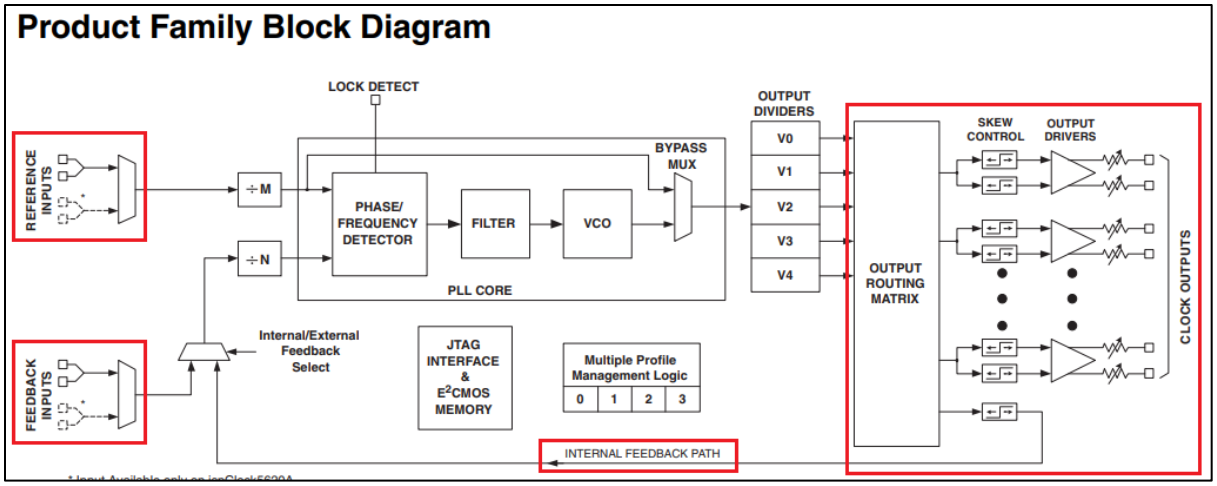
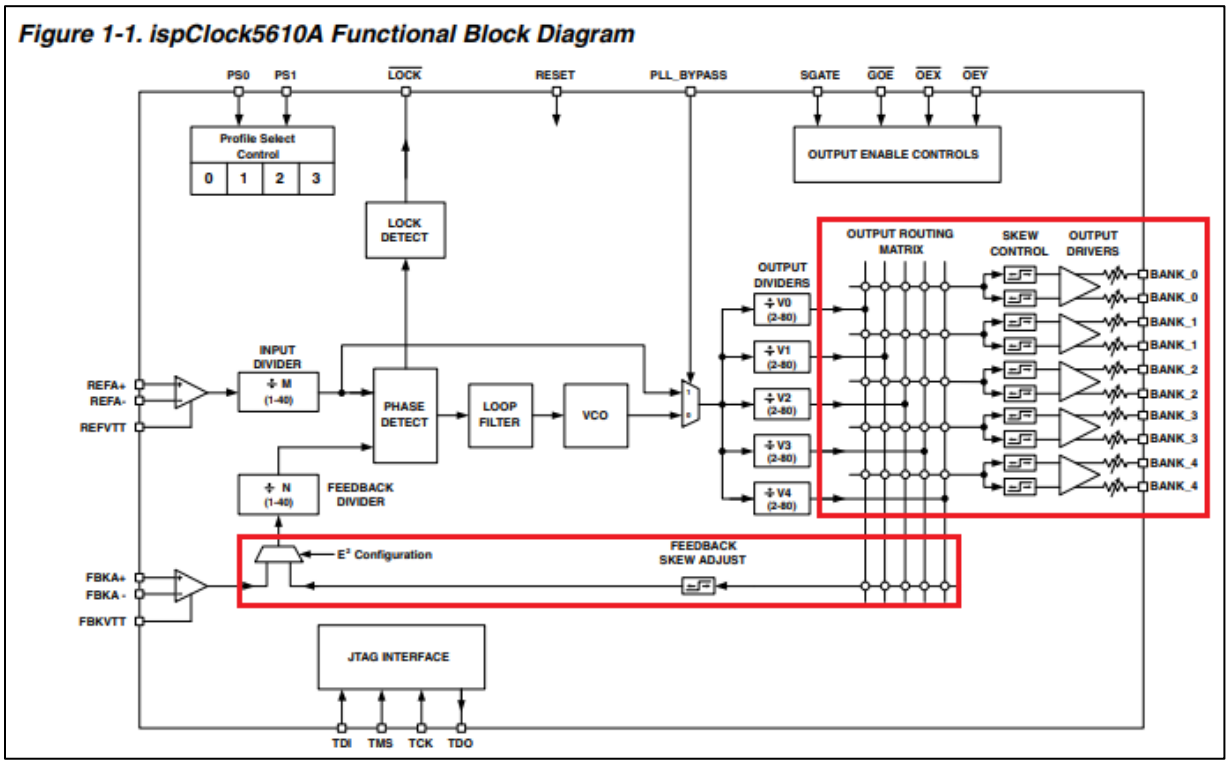
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL,
- Up to Five Clock Frequency Domains
- Flexible Clock Reference and External Feedback Inputs
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination

Source: Lattice ispClock5600A Family Datasheet (Page 1)



Source: Lattice ispClock5600A Family Datasheet (Page 1)



Source: Lattice ispClock5600A Family Datasheet (Page 2)

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Source: Lattice ispClock5600A Family Datasheet (Page 31)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Source: Lattice ispClock5600A Family Datasheet (Page 29)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

23. Lattice has infringed the '530 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of generating output clock signals in response to a reference clock signal and a feedback signal.

24. For example, Lattice's ispClock 5600A Family devices are enhanced zero delay clock generators designed for use in high performance communications and computing applications. These clock generators can output multiple clocks ("a plurality of output clock signals") and provide low output-to-output skew or delay. For instance, ispClock5610A generates 10 clock outputs, and ispClock5620A generates 20 clock outputs. The output clock signals are generated using a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The low output-to-output skew is achieved using feedback inputs.

Lattice Semiconductor Corporation

ispClock™5600A Family

In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 Data Sheet DS1019

Features

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- Low Jitter Peak-to-Peak
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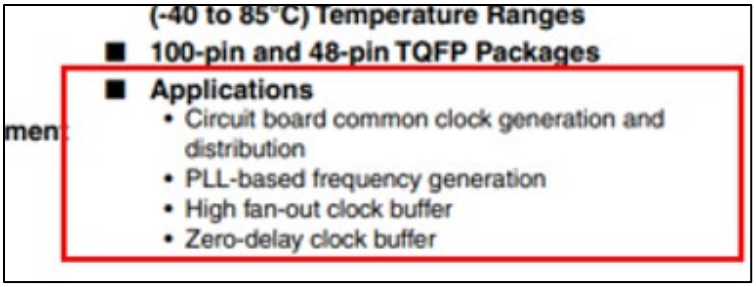
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL,
- Up to Five Clock Frequency Domains
- Flexible Clock Reference and External Feedback Inputs
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination

Source: Lattice ispClock5600A Family Datasheet (Page 1)

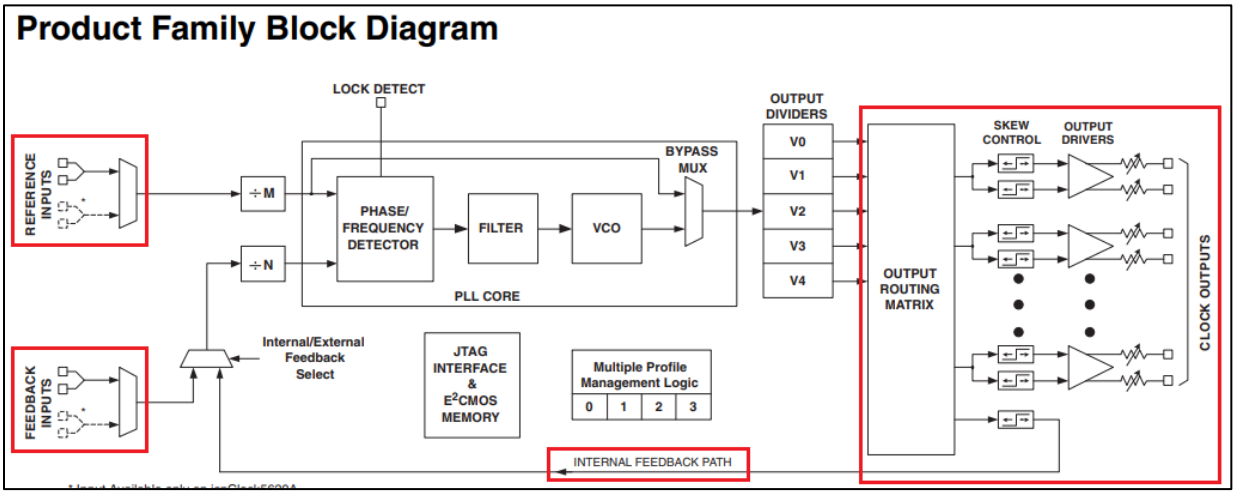


Source: Lattice ispClock5600A Family Datasheet (Page 1)

Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Source: Lattice ispClock5600A Family Datasheet (Page 2)

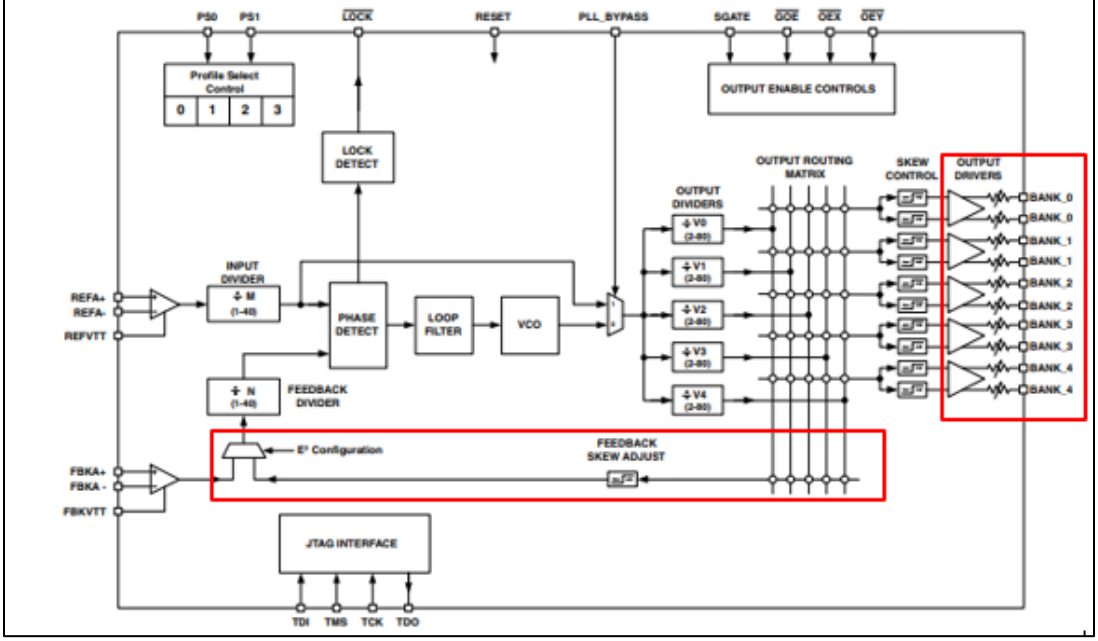


Source: Lattice ispClock5600A Family Datasheet (Page 1)

Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Figure 1-1. ispClock5610A Functional Block Diagram



Source: Lattice ispClock5600A Family Datasheet (Page 2)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

Internal Feedback Mode

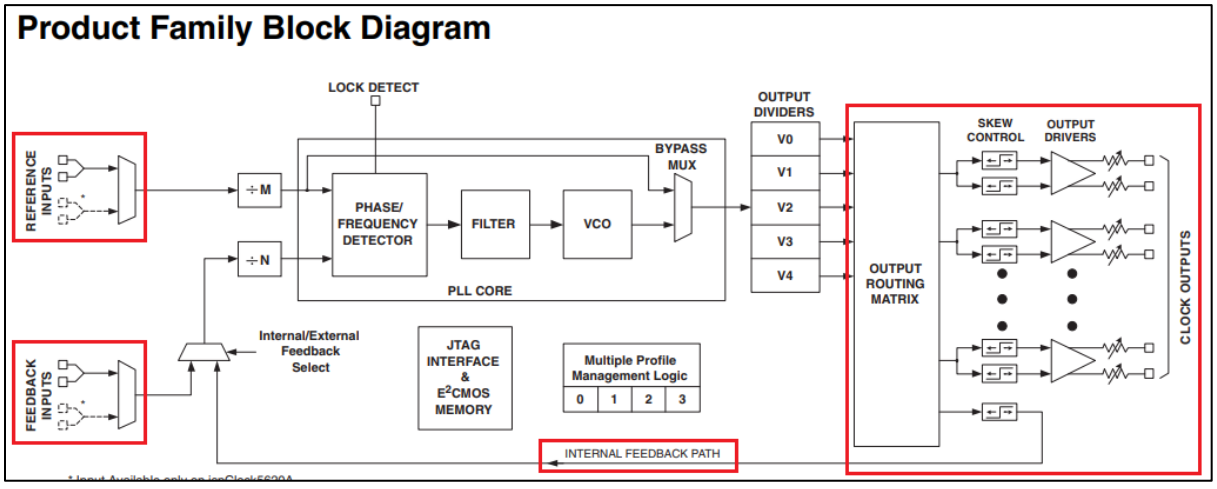
In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

25. Lattice has infringed the ’530 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of selecting one of the output clock signals as the feedback signal in response to a control signal.

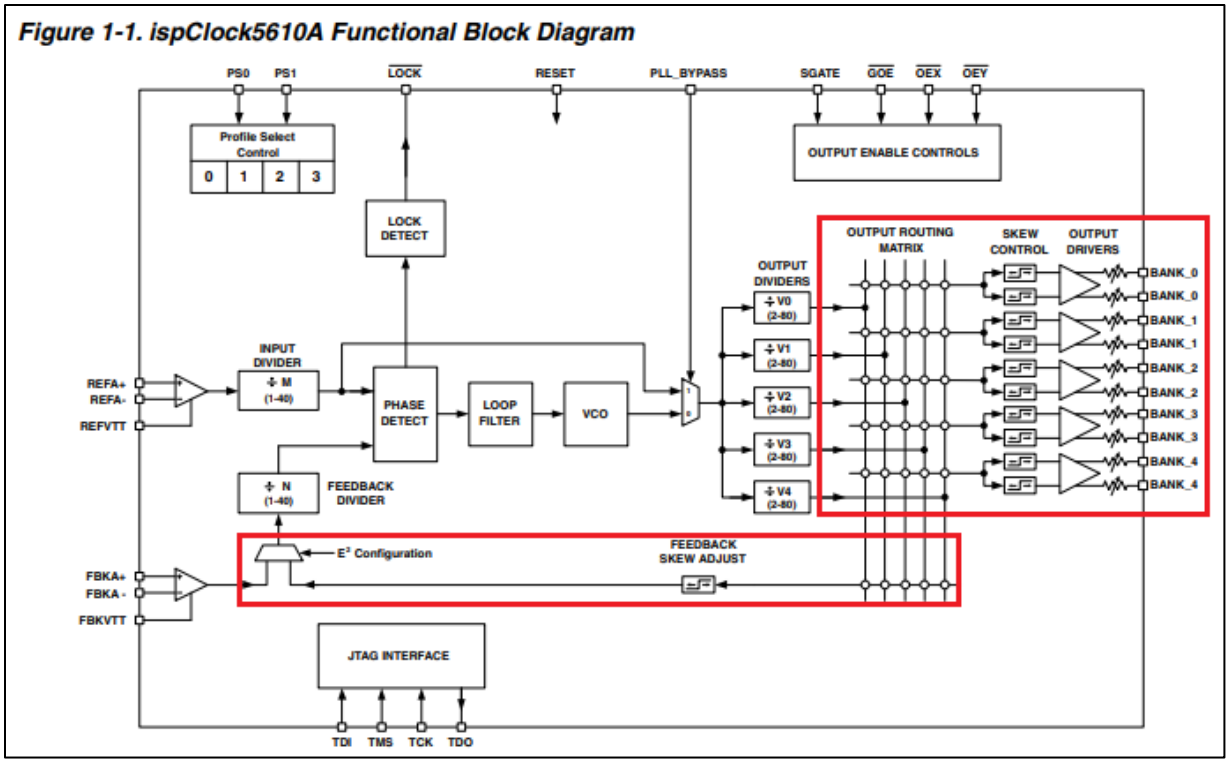
26. For example, Lattice's ispClock 5600A Family devices can generate multiple clock outputs ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). The feedback input can be internal or external. When using internal feedback, one of the multiple clock outputs is selected as the feedback signal.

27. The ispClock 5600A Family devices include control logic or a control signal ("a control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. They further include a circuit that selects one of the clock outputs as the feedback signal based on the control signal. This circuit is connected to all of the clock outputs and allows the ispClock 5600A Family devices to operate as a closed-loop system for all the clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.



Source: Lattice ispClock5600A Family Datasheet (Page 1)

28. The following citations show that only one of the clock outputs is selected as the internal feedback signal, which is fed to a Feedback Skew Adjust block.



Source: Lattice ispClock5600A Family Datasheet (Page 2)

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Source: Lattice ispClock5600A Family Datasheet (Page 31)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Source: Lattice ispClock5600A Family Datasheet (Page 29)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

29. Lattice has had knowledge of the '530 Patent at least as of the date when it was notified of the filing of this action.

30. In addition, Lattice has had knowledge of the '530 Patent at least as of February 25, 2005, when it was cited by the examiner in an office action during prosecution of U.S. Patent No. 7,132,864, which was assigned to Lattice Semiconductor Corp. The examiner rejected multiple claims in the application as anticipated by the '530 Patent. Lattice employee, Edward A. Ramsden—who was named as an inventor of U.S. Patent No. 7,132,864—and others involved in the prosecution of the patent, have had knowledge of the '530 Patent well before this lawsuit was filed.

31. Liberty Patents has been damaged as a result of the infringing conduct by Lattice alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

32. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '530 Patent.

COUNT II

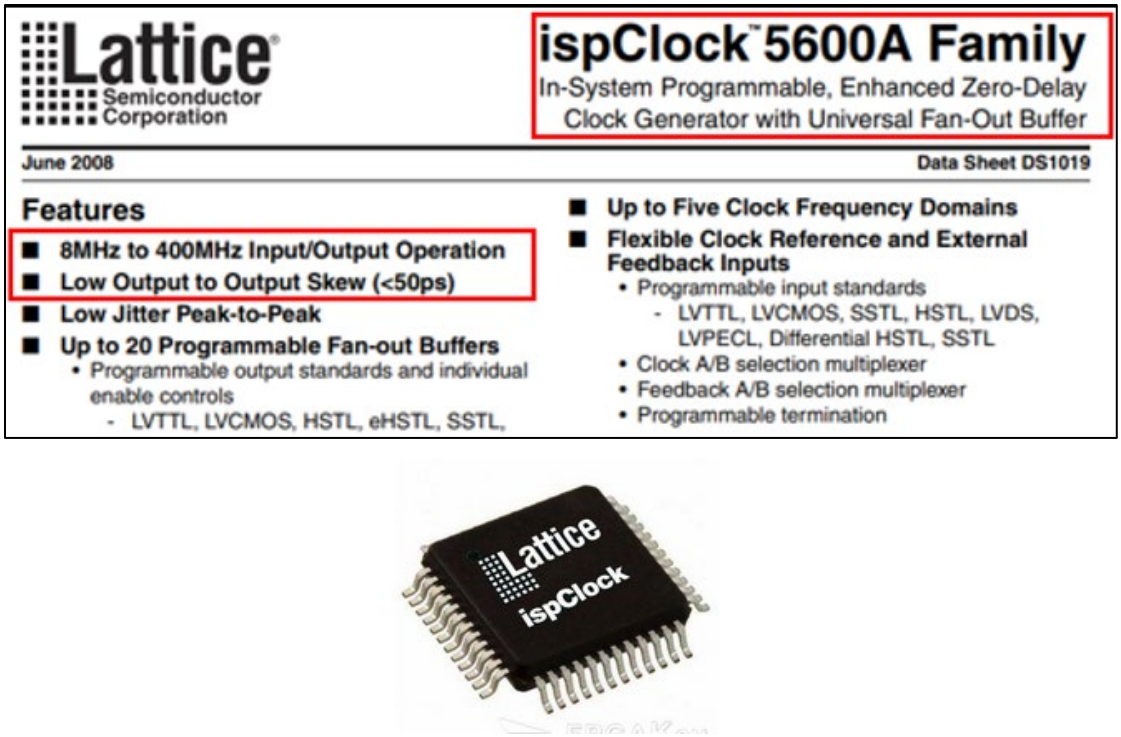
DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,734,740

33. On May 11, 2004, U.S. Patent No. 6,734,740 ("the '740 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques."

34. Liberty Patents is the owner of the '740 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '740 Patent against infringers, and to collect damages for all relevant times.

35. Lattice made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its ispClock 5600A Family devices and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[14] ("accused products"):

[14] *See, e.g.*, ispClock5610A, ispClock5620A, ispClock5610, ispClock5620, ispClock5510, ispClock5520, ispClock5320S, ispClock5316S, ispClock5312S, ispClock5308S, ispClock5304S, ispClock5410D, ispClock5406D, ispClock5406D, ispClock5406D, ispClock5610, ispClock5620, ispClock5620, ispClock5620A, ispClock5520, ispClock5620A, ispClock5312S, ispClock5406D, LFE5UM-25, LFE5UM-45, LFE5UM-85, LFE5UM5G-45, LFE5UM5G-25, LFE5U-12, LFE5U-25, LFE5U-45, LFE5U-85, LAE5U-12, LAE5U-25, LAE5U-45, ECP3-17, ECP3-35, ECP3-70, ECP3-95, ECP3-150, LA-ECP3-17, LA-ECP3-35.



Source: https://www.latticesemi.com/-/media/LatticeSemi/Documents/DataSheets/ispClock/ispClock5600AFamilyDataSheet.ashx?document_id=18324[15] (Page 1); https://www.fpgakey.com/lattice-family/ispclock-5500-family

36. By doing so, Lattice has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 16 of the '740 Patent. Lattice's infringement in this regard is ongoing.

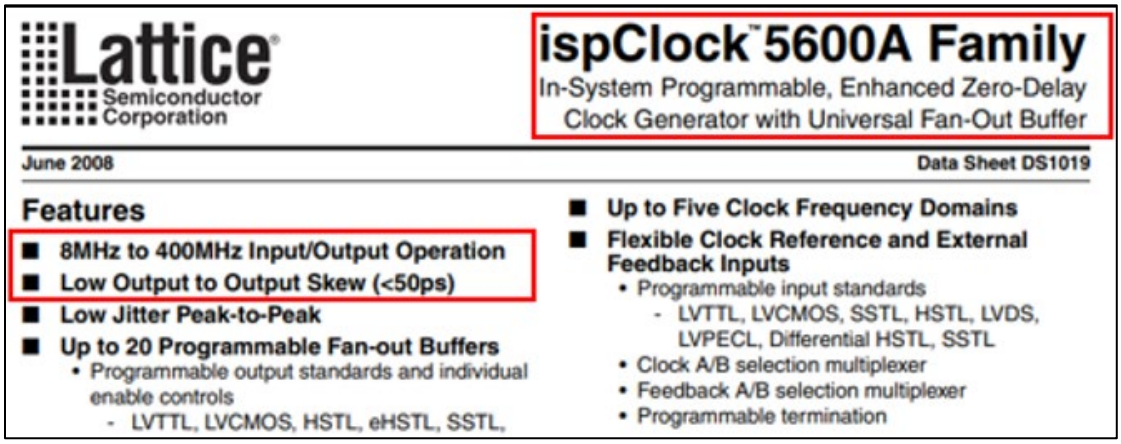
37. Lattice's ispClock 5600A Family devices are exemplary products. They include a first circuit configured to present a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

38. For example, Lattice's ispClock 5600A Family devices are enhanced zero delay clock generators that help in minimizing the output-to-output skew or delay. These devices include a phase locked loop (PLL) with multiple divider circuits, a phase/frequency divider

[15] This link will be hereinafter be referred to as "Lattice ispClock5600A Family Datasheet."

detector, a filter, a voltage-controller oscillator (VCO), and output drivers ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal").

39. One of the multiple clock outputs is selected as the feedback signal. The devices include control logic or a control signal ("a first control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. The delay between the inputs and the outputs is minimized based on the clock outputs (which are generated in response to reference clock and feedback signal). Accordingly, the control signal is generated in response to the reference clock and the feedback signal.



Lattice Semiconductor Corporation

ispClock™5600A Family

In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 — Data Sheet DS1019

Features

- **8MHz to 400MHz Input/Output Operation**
- **Low Output to Output Skew (<50ps)**
- **Low Jitter Peak-to-Peak**
- **Up to 20 Programmable Fan-out Buffers**
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL,
- **Up to Five Clock Frequency Domains**
- **Flexible Clock Reference and External Feedback Inputs**
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination

Source: Lattice ispClock5600A Family Datasheet (Page 1)

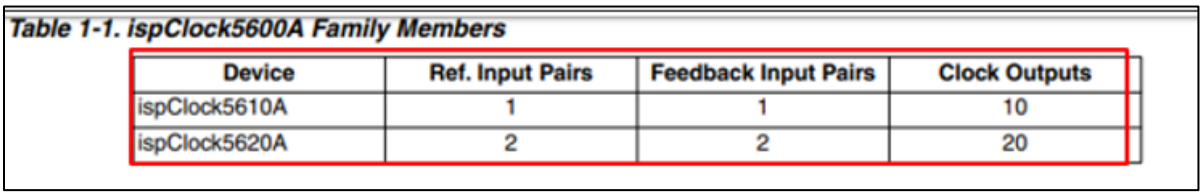
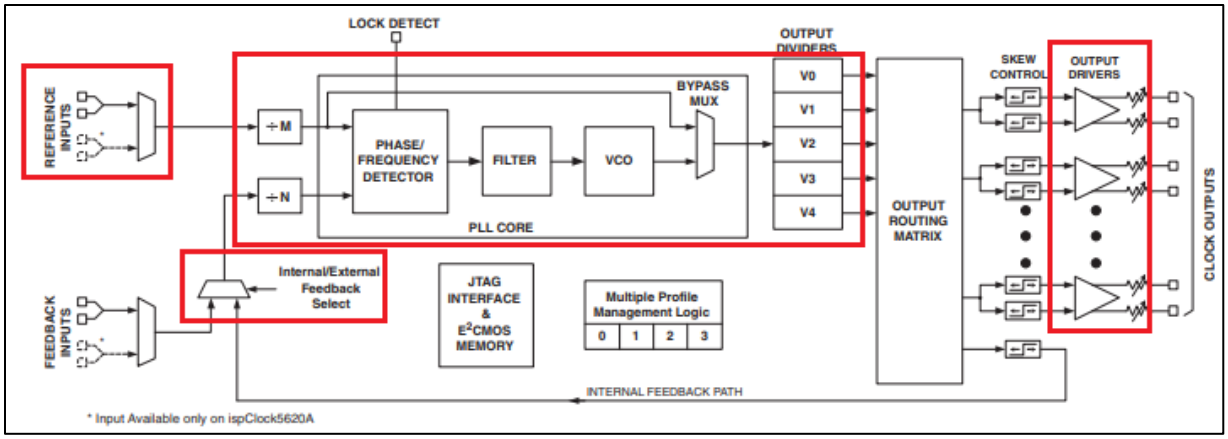


Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Source: Lattice ispClock5600A Family Datasheet (Page 2)



Source: Lattice ispClock5600A Family Datasheet (Page 1)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

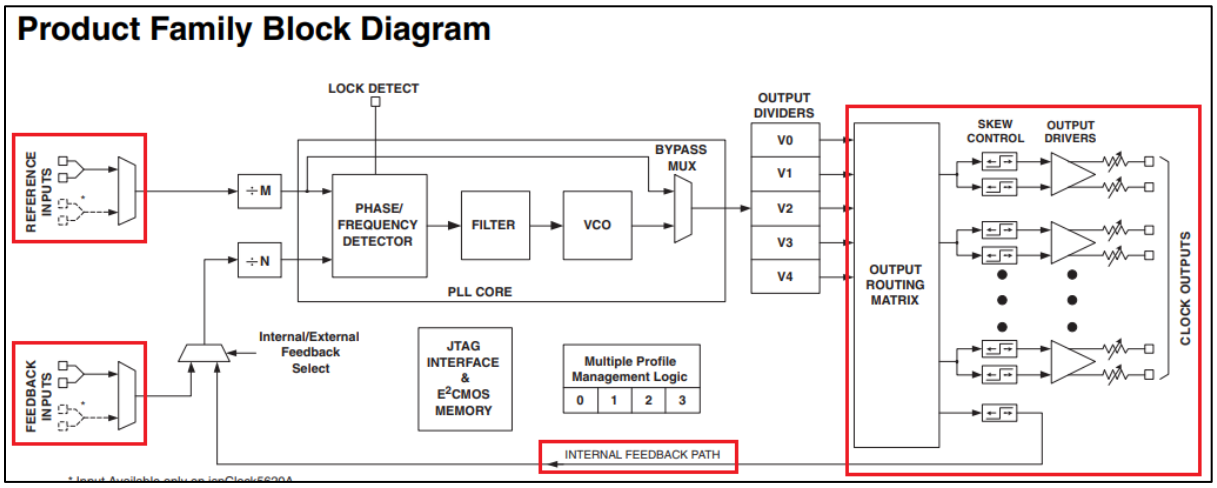
40. Lattice's ispClock 5600A Family devices include a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to the first control signal.

41. For example, Lattice's ispClock 5600A Family devices can generate multiple clock outputs ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). These devices use feedback inputs to obtain a zero delay between input and output signal. The feedback input can be internal or external.

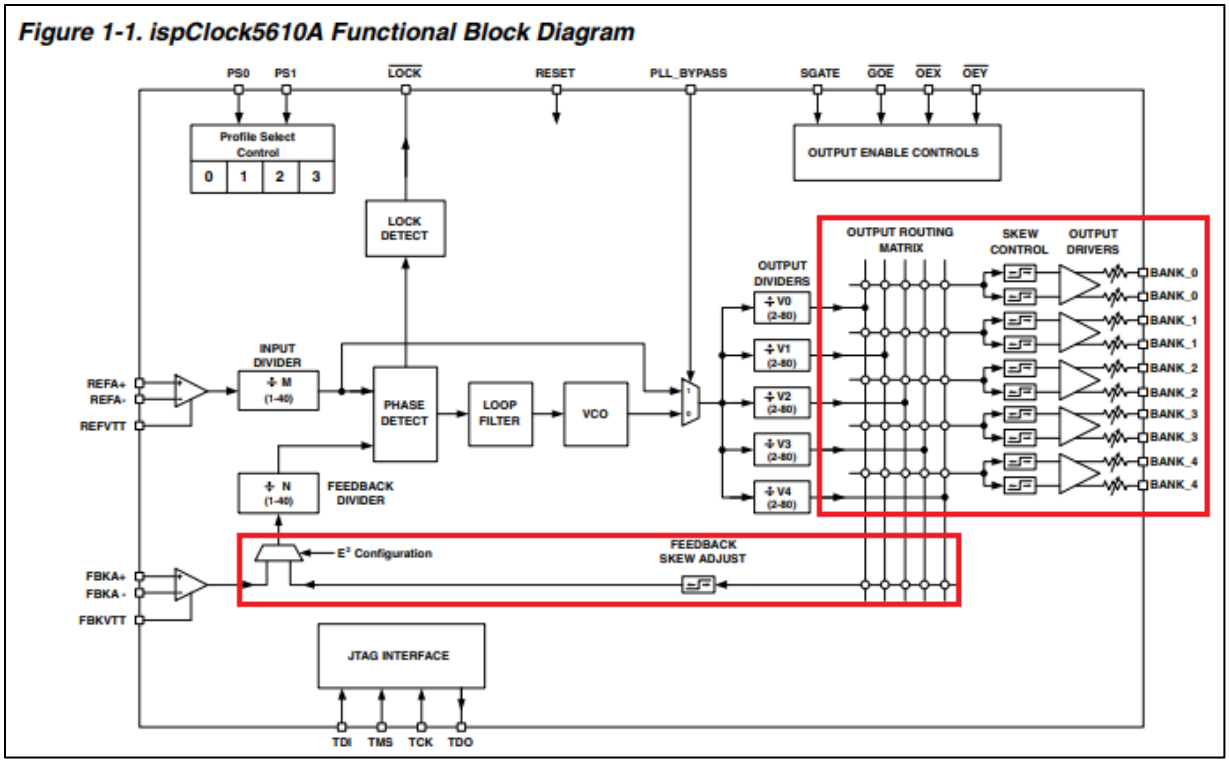
When using internal feedback, one of the multiple clock outputs is selected as the feedback signal.

42. One of the clock outputs is selected as the internal feedback signal, which is fed to a Feedback Skew Adjust block. The devices include control logic or a control signal ("said first control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. They further include circuitry ("a second circuit") that selects one of the clock outputs as the feedback signal based on the control signal. This circuitry ("a second circuit") is connected to all of the clock outputs and allows the ispClock 5600A Family devices to operate as a closed-loop system for all of the clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

43. The accuracy in generating the output clock signals minimizes the delay between them. Because the closed-loop configuration requires the control signal to select one of the clock outputs, the control signal is configured to minimize the delay between the output clock signals.



Source: Lattice ispClock5600A Family Datasheet (Page 1)



Source: Lattice ispClock5600A Family Datasheet (Page 2)

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Source: Lattice ispClock5600A Family Datasheet (Page 31)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Source: Lattice ispClock5600A Family Datasheet (Page 29)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

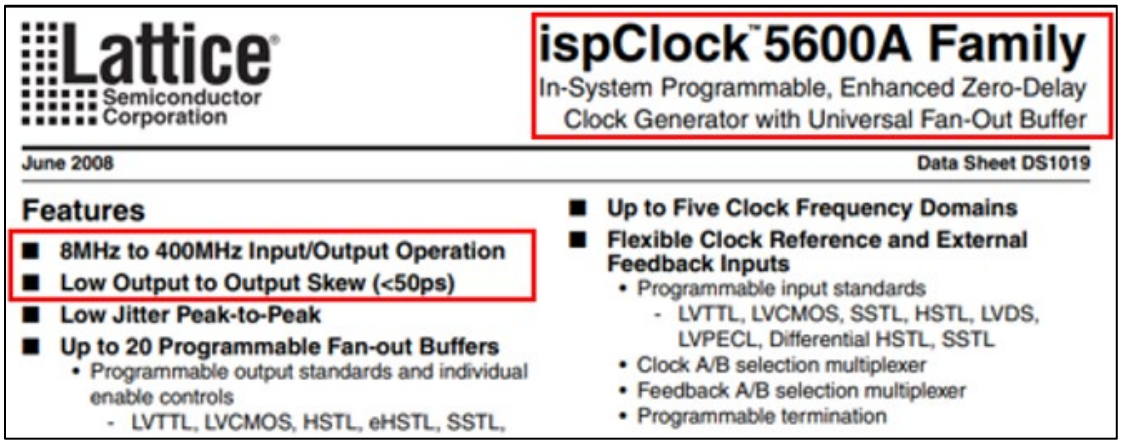
Source: Lattice ispClock5600A Family Datasheet (Page 20)

44. Lattice has infringed the '740 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of generating a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

45. For example, Lattice's ispClock 5600A Family devices are enhanced zero delay clock generators designed for use in high performance communications and computing applications. These clock generators can output multiple clocks ("a plurality of output clock signals") and provide low output-to-output skew or delay. For instance, ispClock5610A generates 10 clock outputs, and ispClock5620A generates 20 clock outputs. The output clock

signals are generated using a reference input ("a reference clock signal") and a feedback input ("a feedback signal").

46. One of the multiple clock outputs is selected as the feedback signal. The devices include control logic or a control signal ("a first control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. The delay between the inputs and the outputs is minimized based on the clock outputs (which are generated in response to reference clock and feedback signal). Accordingly, the control signal is generated in response to the reference clock and the feedback signal.


Lattice Semiconductor Corporation

ispClock™5600A Family

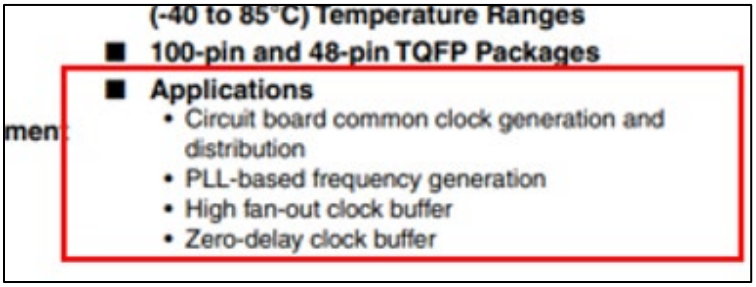
In-System Programmable, Enhanced Zero-Delay Clock Generator with Universal Fan-Out Buffer

June 2008 Data Sheet DS1019

Features

- 8MHz to 400MHz Input/Output Operation
- Low Output to Output Skew (<50ps)
- Low Jitter Peak-to-Peak
- Up to 20 Programmable Fan-out Buffers
  - Programmable output standards and individual enable controls
    - LVTTL, LVCMOS, HSTL, eHSTL, SSTL,
- Up to Five Clock Frequency Domains
- Flexible Clock Reference and External Feedback Inputs
  - Programmable input standards
    - LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL, Differential HSTL, SSTL
  - Clock A/B selection multiplexer
  - Feedback A/B selection multiplexer
  - Programmable termination

Source: Lattice ispClock5600A Family Datasheet (Page 1)


(-40 to 85°C) Temperature Ranges

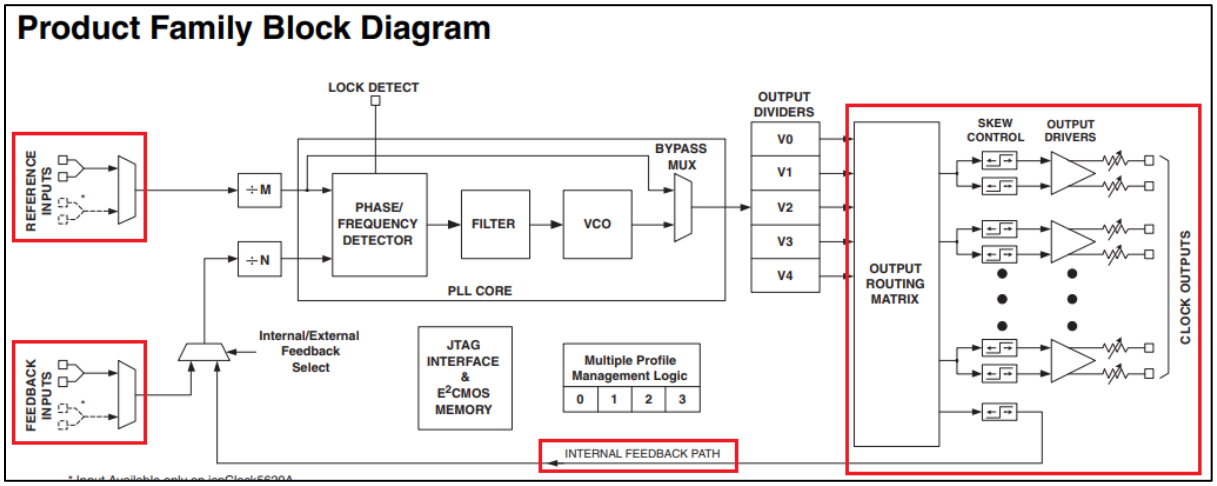
- 100-pin and 48-pin TQFP Packages
- Applications
  - Circuit board common clock generation and distribution
  - PLL-based frequency generation
  - High fan-out clock buffer
  - Zero-delay clock buffer

Source: Lattice ispClock5600A Family Datasheet (Page 1)

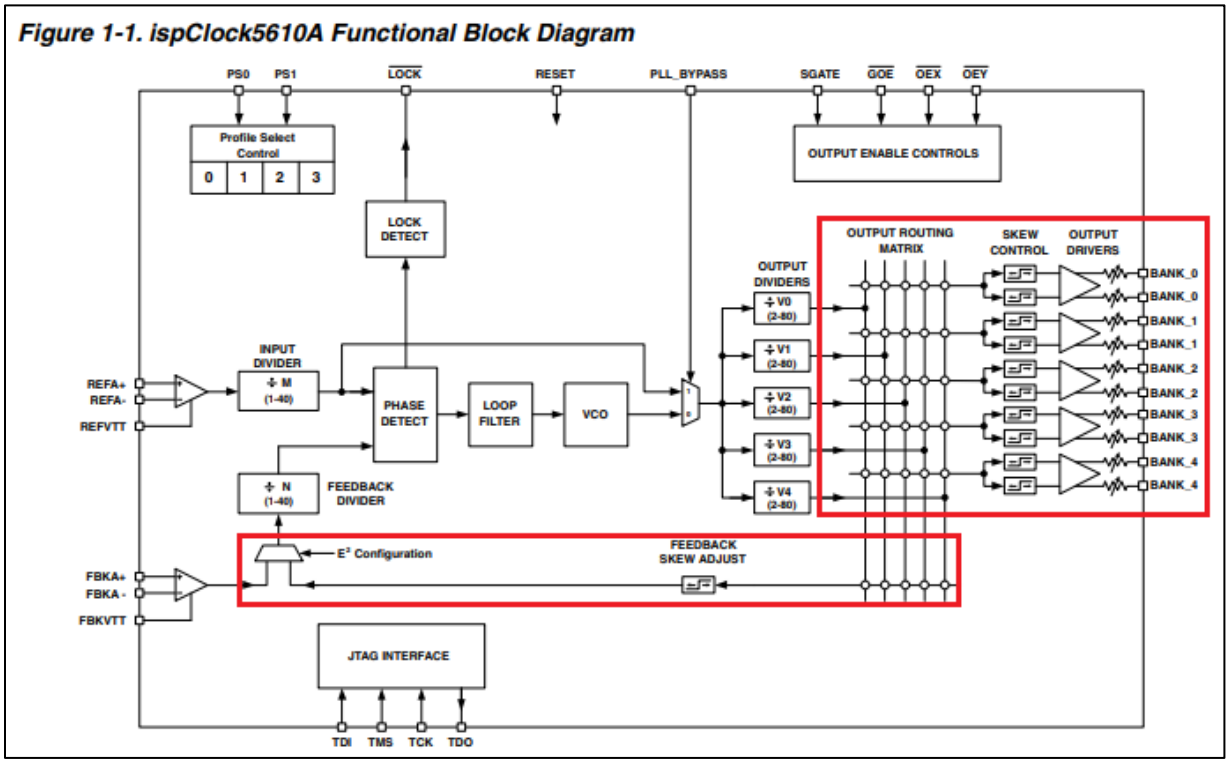
Table 1-1. ispClock5600A Family Members

Device	Ref. Input Pairs	Feedback Input Pairs	Clock Outputs
ispClock5610A	1	1	10
ispClock5620A	2	2	20

Source: Lattice ispClock5600A Family Datasheet (Page 2)



Source: Lattice ispClock5600A Family Datasheet (Page 1)



Source: Lattice ispClock5600A Family Datasheet (Page 2)

The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.

The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Source: Lattice ispClock5600A Family Datasheet (Page 31)

By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Source: Lattice ispClock5600A Family Datasheet (Page 29)

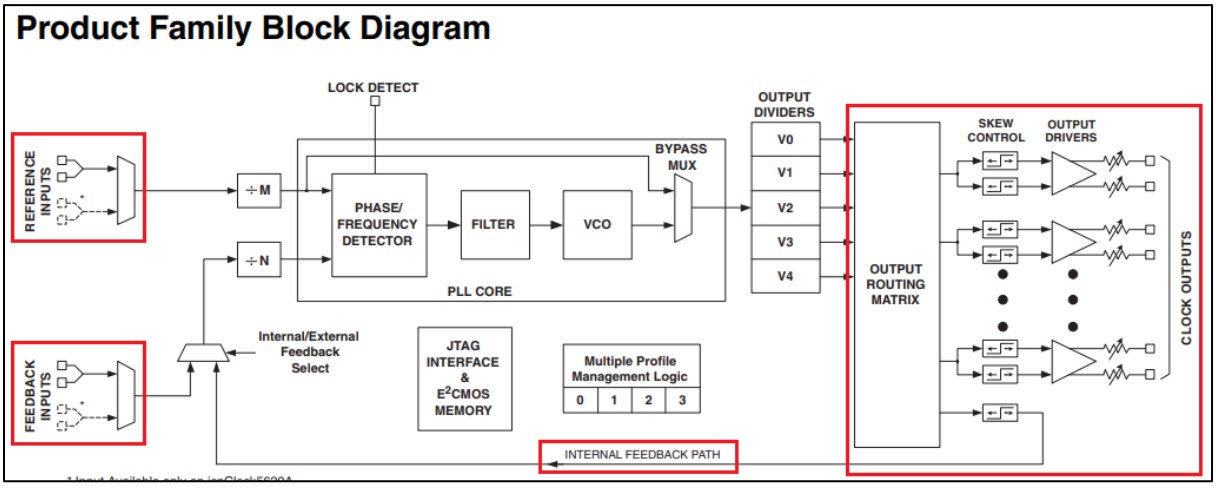
Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

47. Lattice has infringed the '740 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals. The method comprises the step of selecting one of the output clock signals as the feedback signal in response to the first control signal.

48. For example, Lattice's ispClock 5600A Family devices can generate multiple clock outputs ("said output clock signals") in response to a reference input ("a reference clock signal") and a feedback input ("a feedback signal"). These devices use feedback inputs to obtain a zero delay between input and output signals. The feedback input can be internal or external. When using internal feedback, one of the multiple clock outputs is selected as the feedback signal.

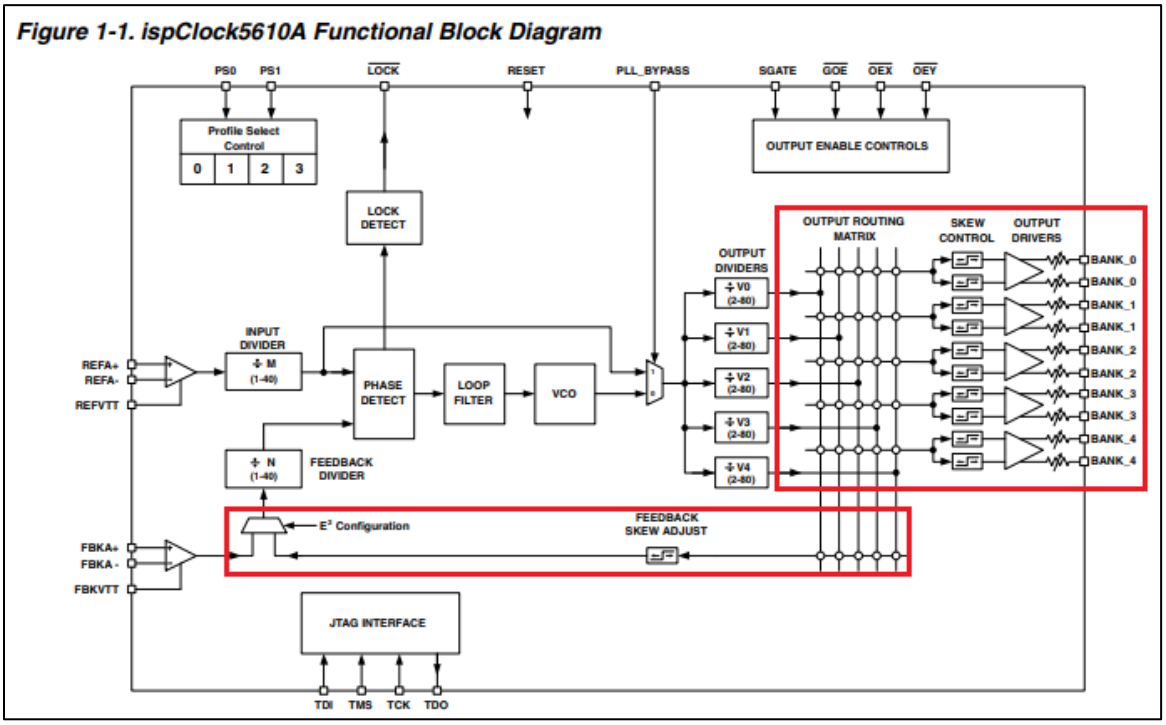


Source: Lattice ispClock5600A Family Datasheet (Page 1)

49. The following citations show that only one of the clock outputs is selected as the internal feedback signal, which is fed to a Feedback Skew Adjust block. The devices include

control logic or a control signal ("said first control signal") that selects the appropriate clock output as the feedback signal to achieve low output-to-output skew in the system. They further include circuitry that selects one of the clock outputs as the feedback signal based on the control signal. This circuitry is connected to all of the clock outputs and allows the ispClock 5600A Family devices to operate as a closed-loop system for all of the clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

Figure 1-1. ispClock5610A Functional Block Diagram



Source: Lattice ispClock5600A Family Datasheet (Page 2)

> The ispClock5600A's PLL and divider systems supports the synthesis of multiple clock frequencies derived from the reference input through the provision of programmable input and feedback dividers. A set of five post-PLL V-dividers provides additional flexibility by supporting the generation of five separate output frequencies. Loop feedback may be taken internally from the output of any of the five V-dividers, or externally through FBKA+/- or FBKB+/- pins.
>
> The core functions of all members of the ispClock5600A family are identical, the differences between devices being restricted to the number of inputs and outputs, as shown in the following table. Figures 1 and 2 show functional block diagrams of the ispClock5610A and ispClock5620A.

Source: Lattice ispClock5600A Family Datasheet (Page 2)

Static Phase Offset and Input-Output Skew

The ispClock5600A's external feedback inputs can be used to obtain near-zero effective delays from the clock reference input pins to a designated output pin. In external feedback mode (Figure 1-27) the PLL will attempt to force the output phase so that the rising edge phase ($t\phi$) at the feedback input matches the rising edge phase at the reference input. The residual error between the two is specified as the static phase error. Note that any propagation delays (t_{FBK}) in the external feedback path drive the phase of the output signal *backwards* in time as measured at the output. For this reason, if zero input-to-output delays are required in external feedback mode, the length of the signal path between the output pin and the feedback pin should be minimized.

Source: Lattice ispClock5600A Family Datasheet (Page 31)

Internal Feedback Mode

In addition to supporting the use of external feedback to close the phase-locked loop, ispClock5620A also provides the option of using an internal feedback path for this function. This feature is useful for minimizing external connections and routing in situations where one can attempt to compensate for external signal path delays using the programmable skew feature of the internal feedback path.

Source: Lattice ispClock5600A Family Datasheet (Page 32)

By using the internal feedback path, and programming a skew into the feedback skew control, it is possible to implement negative timing skews, in which the clock edge of interest appears at the ispClock5600A's output before the corresponding edge is presented at the reference input. When the feedback skew unit is used in this way, the resulting negative skew is added to whatever skew is specified for each output. For example, if the feedback skew is set to 6TU, BANK1's skew is 8TU and BANK2's skew is 3TU, then BANK1's effective output skew will be 2TU (8TU-6TU), while BANK2's effective skew will be -3TU (3TU-6TU). This negative skew will manifest itself as BANK2's outputs appearing to lead the input reference clock, appearing as a negative propagation delay.

Please note that the skew control units are only usable when the PLL is selected. In PLL bypass mode (PLL_BYPASS=1), output skew settings will be ineffective and all outputs will exhibit skew consistent with the device's propagation delay and the individual delays inherent in the output drivers consistent with the logic standard selected.

Source: Lattice ispClock5600A Family Datasheet (Page 29)

Reference and External Feedback Inputs

The ispClock5600A provides sets of configurable, internally-terminated inputs for both clock reference and feedback signals. In normal operation, one of the clock reference input pairs (REFA+/- or REFB+/-) is used as a clock input.

The external feedback inputs make it possible to compensate for input to output delay through external means. This makes it possible to provide output clocks which have very low skews in relation to the reference clock regardless of loading effects.

Source: Lattice ispClock5600A Family Datasheet (Page 20)

50. Lattice has had knowledge of the '740 Patent at least as of the date when it was notified of the filing of this action.

51. On February 25, 2005, the parent of the '740 Patent (the '530 Patent) was cited by the examiner in an office action during prosecution of U.S. Patent No. 7,132,864, which was

assigned to Lattice Semiconductor Corp. The examiner rejected multiple claims in the application as anticipated by the '530 Patent. Lattice employee, Edward A. Ramsden—who was named as an inventor of U.S. Patent No. 7,132,864—and others involved in the prosecution of the patent, have had knowledge of the '740 Patent well before this lawsuit was filed.

52. Liberty Patents has been damaged as a result of the infringing conduct by Lattice alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

53. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '740 Patent.

ADDITIONAL ALLEGATIONS REGARDING INFRINGEMENT AND PERSONAL JURISDICTION

54. Lattice has also indirectly infringed the '530 Patent and the '740 Patent by inducing others to directly infringe the '530 Patent and the '740 Patent.

55. Lattice has induced the end users and/or Lattice's customers to directly infringe (literally and/or under the doctrine of equivalents) the '530 Patent and the '740 Patent by using the accused products.

56. Lattice took active steps, directly and/or through contractual relationships with others, with the specific intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, claims 1 and 15 of the '530 Patent, and claims 1 and 16 of the '740 Patent.

57. Such steps by Lattice included, among other things, advising or directing customers and end users to use the accused products in an infringing manner; advertising and

promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner.

58. Lattice performed these steps, which constitute induced infringement, with the knowledge of the ’530 Patent and the ’740 Patent and with the knowledge that the induced acts constitute infringement.

59. Lattice was and is aware that the normal and customary use of the accused products by Lattice’s customers would infringe the ’530 Patent and the ’740 Patent. Lattice’s inducement is ongoing.

60. Lattice has also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates’ behalf, to directly infringe (literally and/or under the doctrine of equivalents) the ’530 Patent and the ’740 Patent by importing, selling or offering to sell the accused products.

61. Lattice has a significant role in placing the accused products in the stream of commerce with the expectation and knowledge that they will be purchased by consumers in Texas and elsewhere in the United States.

62. Lattice purposefully directs or controls the making of accused products and their shipment to the United States, using established distribution channels, for sale in Texas and elsewhere within the United States.

63. Lattice purposefully directs or controls the sale of the accused products into established United States distribution channels, including sales to nationwide retailers. Lattice’s established United States distribution channels include one or more United States based affiliates.

64. Lattice purposefully directs or controls the sale of the accused products online and in nationwide retailers, including for sale in Texas and elsewhere in the United States, and expects and intends that the accused products will be so sold.

65. Lattice purposefully places the accused products—whether by itself or through subsidiaries, affiliates, or third parties—into an international supply chain, knowing that the accused products will be sold in the United States, including Texas. Therefore, Lattice also facilitates the sale of the accused products in Texas.

66. Lattice took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the ’530 Patent and the ’740 Patent, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

67. Such steps by Lattice included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing that such importation or sale would occur; and directing, facilitating, or influencing its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates’ behalf, to import, sell, or offer to sell the accused products in an infringing manner.

68. Lattice performed these steps, which constitute induced infringement, with the knowledge of the ’530 Patent and the ’740 Patent, and with the knowledge that the induced acts would constitute infringement.

69. Lattice performed such steps in order to profit from the eventual sale of the accused products in the United States.

70. Lattice’s inducement is ongoing.

71. Lattice has also indirectly infringed by contributing to the infringement of the ’530 Patent and the ’740 Patent. Lattice has contributed to the direct infringement of the ’530 Patent and the ’740 Patent by the end user of the accused products.

72. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the ’530 Patent and the ’740 Patent, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

73. The special features include, for example, circuitry that reduces the delay between output clock signals in a zero delay buffer used in a manner that infringes the ’530 Patent and the ’740 Patent.

74. These special features constitute a material part of the invention of one or more of the claims of the ’530 Patent and the ’740 Patent, and are not staple articles of commerce suitable for substantial non-infringing use.

75. Lattice’s contributory infringement is ongoing.

76. Lattice has had actual knowledge of the ’530 Patent and the ’740 Patent at least as of the date when it was notified of the filing of this action. Since at least that time, Lattice has known the scope of the claims of the ’530 Patent and the ’740 Patent, the products that practice the ’530 Patent and the ’740 Patent, and that Liberty Patents is the owner of the ’530 Patent and the ’740 Patent.

77. By the time of trial, Lattice will have known and intended (since receiving such notice) that its continued actions would infringe and actively induce and contribute to the infringement of one or more claims of the ’530 Patent and the ’740 Patent.

78. Furthermore, Lattice has a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of Liberty Patents' patent rights. *See, e.g.*, M. Lemley, "Ignoring Patents," 2008 Mich. St. L. Rev. 19 (2008).

79. Lattice's actions are at least objectively reckless as to the risk of infringing valid patents, and this objective risk was either known or should have been known by Lattice. Lattice has knowledge of the '530 Patent and the '740 Patent.

80. Lattice's customers have infringed the '530 Patent and the '740 Patent. Lattice has encouraged its customers' infringement.

81. Lattice's direct and indirect infringement of the '530 Patent and the '740 Patent has been, and/or continues to be willful, intentional, deliberate, and/or in conscious disregard of Liberty Patents' rights under the patents-in-suit.

82. Liberty Patents has been damaged as a result of Lattice's infringing conduct alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Liberty Patents hereby requests a trial by jury on all issues so triable by right.

PRAYER FOR RELIEF

Liberty Patents requests that the Court find in its favor and against Lattice, and that the Court grant Liberty Patents the following relief:

a. Judgment that one or more claims of the '530 Patent and the '740 Patent have been infringed, either literally and/or under the doctrine of equivalents, by Lattice and/or all others acting in concert therewith;

b. A permanent injunction enjoining Lattice and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the '530 Patent and the '740 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the '530 Patent and the '740 Patent by such entities;

c. Judgment that Lattice account for and pay to Liberty Patents all damages to and costs incurred by Liberty Patents because of Lattice's infringing activities and other conduct complained of herein, including an award of all increased damages to which Liberty Patents is entitled under 35 U.S.C. § 284;

d. That Liberty Patents be granted pre-judgment and post-judgment interest on the damages caused by Lattice's infringing activities and other conduct complained of herein;

e. That this Court declare this an exceptional case and award Liberty Patents its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285; and

f. That Liberty Patents be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: January 22, 2021

Respectfully submitted,

/s/ *Zachariah S. Harrington*

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