IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

LIBERTY PATENTS, LLC, Plaintiff, v. TEXAS INSTRUMENTS, INC., Defendant.	CIVIL ACTION NO. 6:21-cv-62 ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Liberty Patents, LLC ("Liberty Patents" or "Plaintiff") files this original complaint against Defendant Texas Instruments, Inc. ("TI" or "Defendant"), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

PARTIES

1. Liberty Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas 75703.

2. Defendant Texas Instruments, Inc. is a company organized and existing under the laws of the state of Delaware. Texas Instruments, Inc. may be served with process through its registered agent, CT Corporation System at 1999 Bryan St., Suite 900, Dallas, Texas, 75201.

3. TI is "a global semiconductor company that designs, manufactures, tests and sells analog and embedded processing chips."[1] It "design[s], manufacture[s], test[s] and sell[s] analog and embedded semiconductors" for "nearly 100,000 customers around the globe."[2] It has a

[1] *See* https://www.ti.com/about-ti/company/overview.html.

[2] *See* https://www.ti.com/about-ti/company/what-we-do.html.

portfolio of about 80,000 products with 14 manufacturing sites worldwide, operating "10 wafer fabs, seven assembly and test factories, and multiple bump and probe facilities."[3]

JURISDICTION AND VENUE

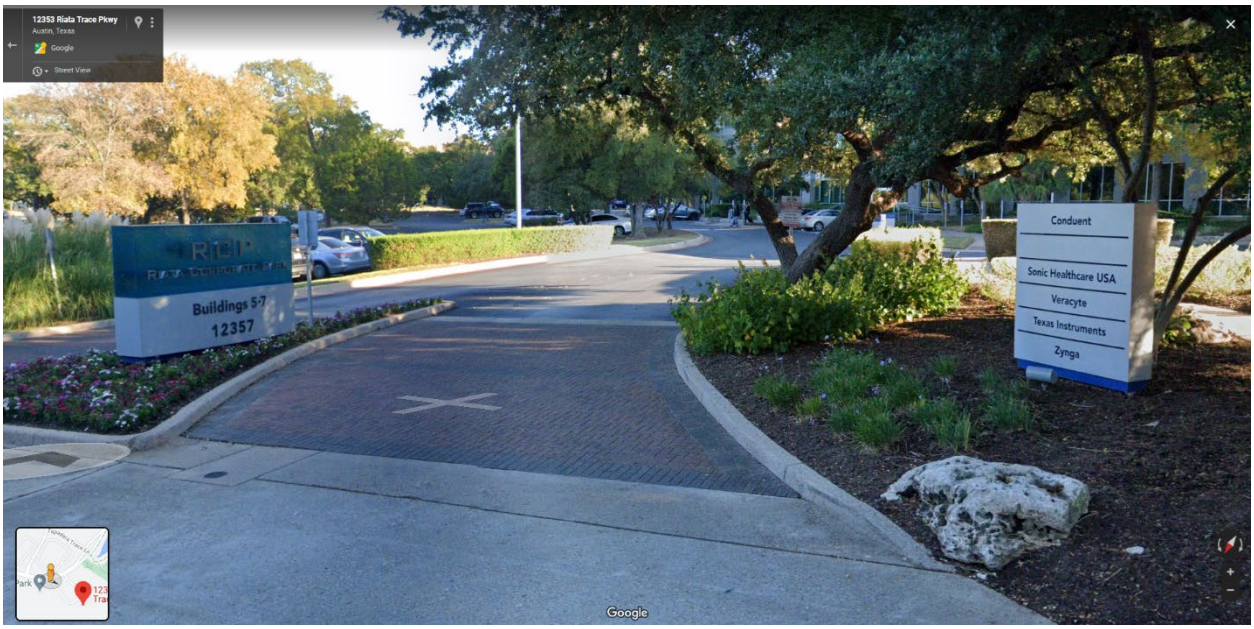
4. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

5. This Court has personal jurisdiction over TI pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) TI has done and continues to do business in Texas; (ii) TI has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing a least a portion of any other infringements alleged herein in Texas, and (iii) TI is registered to do business in Texas.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). Venue is further proper because TI has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a portion of any other infringements alleged herein in this district.

7. TI also has a regular and established places of business in this district, including at least at 12357 Riata Trace Pkwy, Suite A-130, Austin, Texas, 78727:

[3] *Id.*



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BACKGROUND

8. The patents-in-suit generally relate to zero delay buffer (ZDB) technology. In particular, they teach ZDB technology with multiple output clock signals—instantiations of a reference input clock signal—with predicted delay. The inventions of the patents-in-suit afforded the industry with numerous enhancements, some of which included product robustness,

multiplexed feedback, minimization of delay between output clock signals, programmability, and approximating a closed-loop system to mitigate variations in temperature, supply voltage, supply ground, and/or output loading effects.

9. The patented technology was developed by engineers at Cypress Semiconductor Corp., which is one of the preeminent semiconductor design and manufacturing companies in the world today. In the early 2000s, when the patents-in-suit were filed, Cypress Semiconductor was a world leader in timing-technology solutions and specifically, was leading all other companies in the clock distribution arena.[4]

10. Cypress Semiconductor is a pioneer in the area of programmable clocks, having been in the "Timing Solutions" industry since the late 1990s.[5] Indeed, Cypress Semiconductor invented the world's first programmable IC for crystal oscillators in 1996, the world's first programmable clock generator in 1995, and the world's first programmable skew buffer in 1998.[6] In its Annual Report discussing the 2001 fiscal year—the year in which the initial patent application was filed—Cypress Semiconductor noted that it was a "leader in the timing technology device market primarily due to [its] clocks and clock distribution circuits."[7] It explained that these circuits were "widely used" in personal computers, disk drives, modems, small office/home office network routers and hubs, digital video disks, and home video games.[8]

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[4] *See, e.g.*, https://www.businesswire.com/news/home/20030421005075/en/Cypress-Announces-Field-Programmable-Zero-Delay-Buffer; https://www.businesswire.com/news/home/20030930005313/en/Cypress-Announces-Industrys-Lowest-Total-Timing-Budget.

[5] *See* https://www.cypress.com/products/timing-solutions.

[6] *See id*.

[7] *See* Cypress Semiconductor Annual Report (2002) at 6, http://investors.cypress.com/node/7026/html.

[8] *Id*.

At that time, Cypress Semiconductor was "the only supplier offering true field-programmable clocks," which had resulted in "clock outputs hav[ing] the desired characteristics of high drive, low jitter, low electro-magnetic interference and low skew."[9]

11. The pioneering nature of the patented technology is attested to by the number of companies that have cited to the patents-in-suit: Agere Systems (now part of Broadcom), Altera (acquired by Intel), Boeing, Canon, Integrated Device Technology (now owned by Renesas), Lattice Semiconductor, Rambus, ROHM Semiconductor, Samsung, TSMC, and UMC.

COUNT I

DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,608,530

12. On August 19, 2003, U.S. Patent No. 6,608,530 ("the '530 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques."

13. Liberty Patents is the owner of the '530 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '530 Patent against infringers, and to collect damages for all relevant times.

14. TI made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its LMK04208 Ultra Low Noise Clock Jitter Cleaner With 6 Programmable Outputs and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[10] ("accused products"):

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[9] *Id.*

[10] *See, e.g.*, TI CDCVF25084, LMK03200, LMK04832-SP, LMK04832, LMK04828-EP, LMK05028, LMK04616, LMK04610, LMK04821, LMK04826, MK04828, LMK04816, LMK04906, LMK04803, LMK04805, LMK04806, LMK04808, LMK05028EVM, LMK03200EVAL, LMK04832EVM-CVAL, ADC12DJ3200EVMCVAL,

Source: https://www.ti.com/product/LMK04208

15. By doing so, TI has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 15 of the '530 Patent. TI's infringement in this regard is ongoing.

16. TI's LMK04208 is an exemplary accused product. It includes a first circuit configured to present a plurality of output clock signals in response to a reference clock signal and a feedback signal.

17. For example, TI's LMK04208 is a clock generator that can operate in zero delay (0-delay) mode and has a minimum output-to-output skew or delay. It includes a phase locked loop (PLL) with multiple divider circuits, a phase/frequency detector, filters, a voltage-controlled oscillator (VCO), and buffers ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to the OSCin signal ("a reference clock signal") and the FBMux signal ("a feedback signal").

ADC12DJ3200EVMCVAL-BDL, LMK04832EVM, LMK04616EVM, LMK04610EVM, LMK04208EVM, LMK04821EVM, LMK04826BEVM.

LMK04208 Low-Noise Clock Jitter Cleaner with Dual Loop PLLs

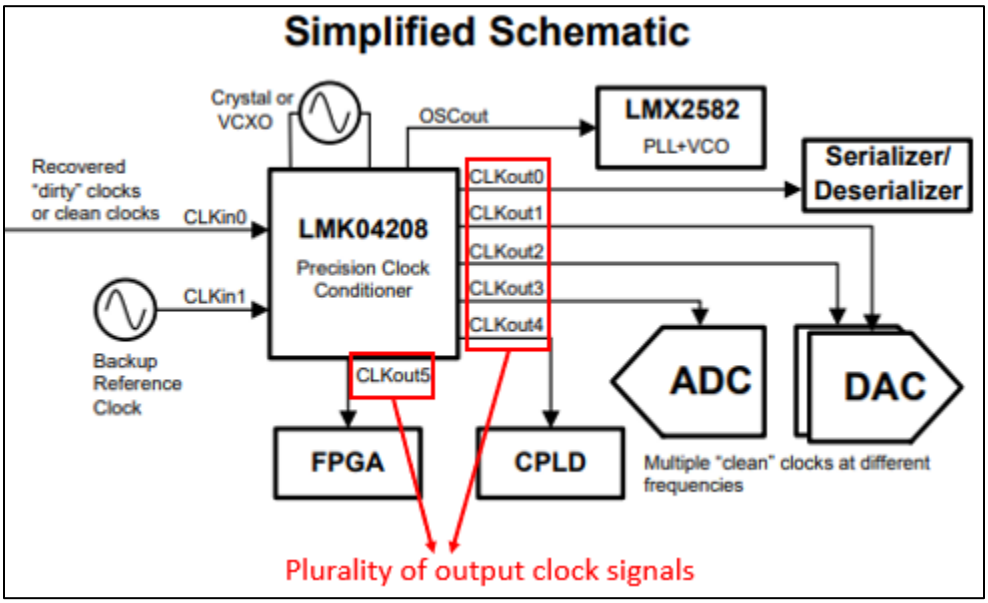
1 Features

- Ultra-Low RMS Jitter Performance
  - 111 fs, RMS Jitter (12 kHz to 20 MHz)
  - 123 fs, RMS Jitter (100 Hz to 20 MHz)
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode when Input Clocks are Lost

3 Description

The LMK04208 is a high performance clock conditioner with superior clock jitter cleaning, generation, and distribution with advanced features to meet next generation system requirements. The dual loop PLLatinum™ architecture is capable of 111 fs, RMS jitter (12 kHz to 20 MHz) using a low-noise VCXO module or sub-200 fs rms jitter (12 kHz to 20 MHz) using a low cost external crystal and varactor diode.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)



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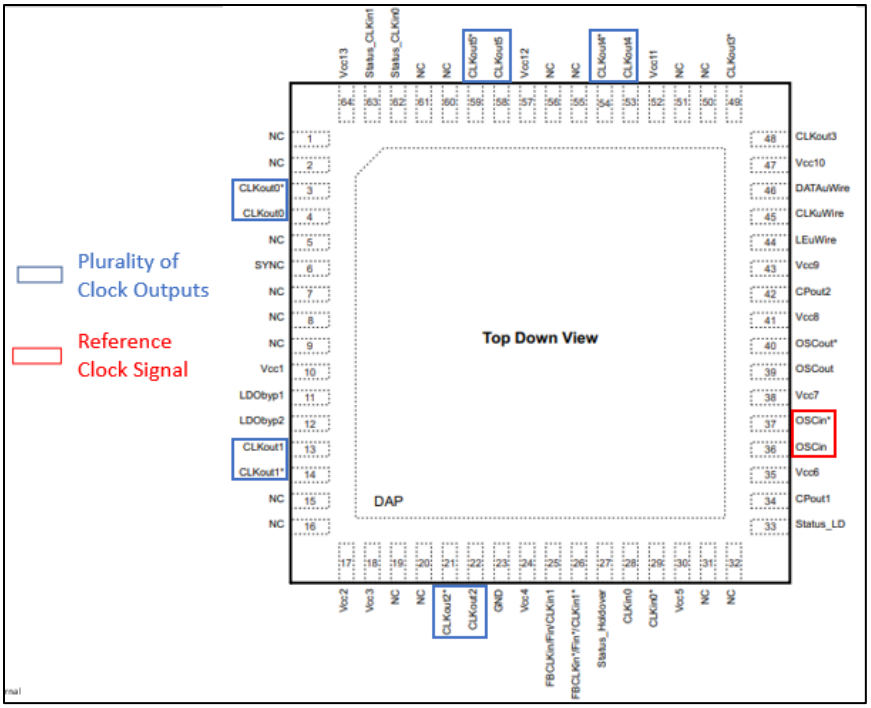

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 3)

Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SKEW and DELAY						
$\|T_{SKEW}\|$	Maximum CLKoutX to CLKoutY(4)(17)	LVDS-to-LVDS, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout(4)(17)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz.		100		
$Mixed T_{SKEW}$	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
$td_{0\text{-}DELAY}$	CLKin to CLKoutX delay(17)	MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0		1850		ps
		MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0; VCO Frequency = 2949.12 MHz Analog delay select = 0; Feedback clock digital delay = 11; Feedback clock half step = 1; Output clock digital delay = 5; Output clock half step = 0;		0		

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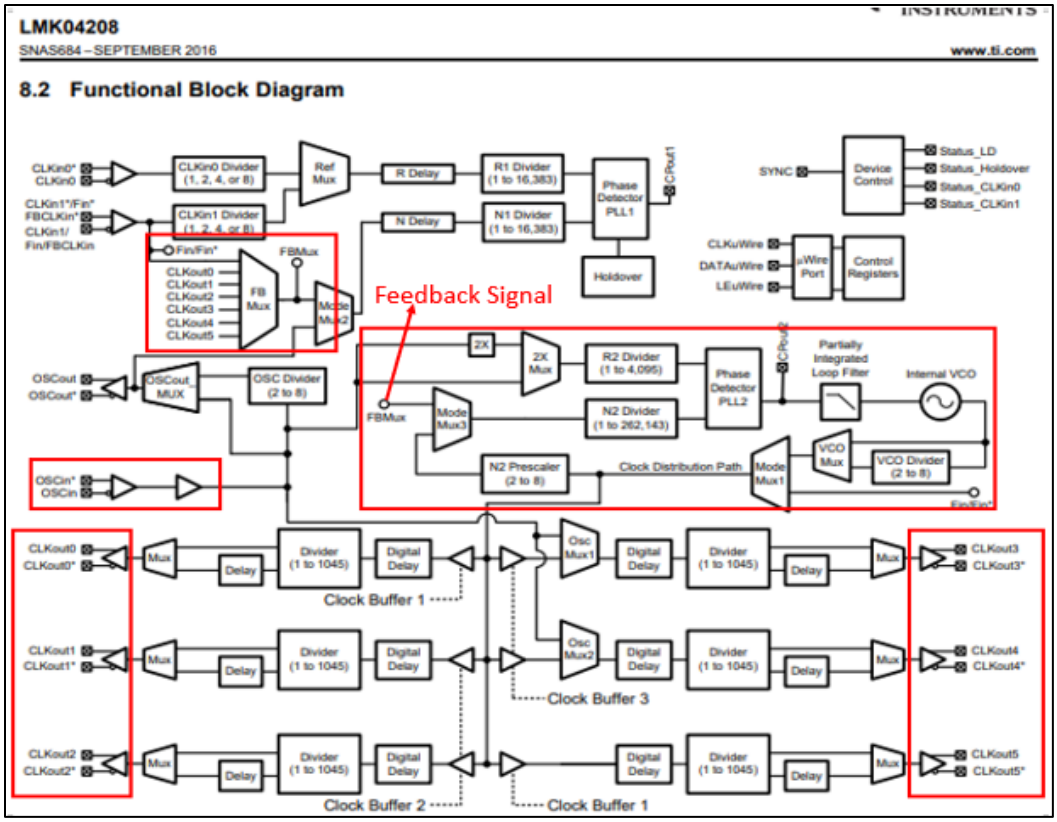


Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides low-noise jitter cleaner functionality while the second PLL (PLL2) performs the clock generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When paired with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

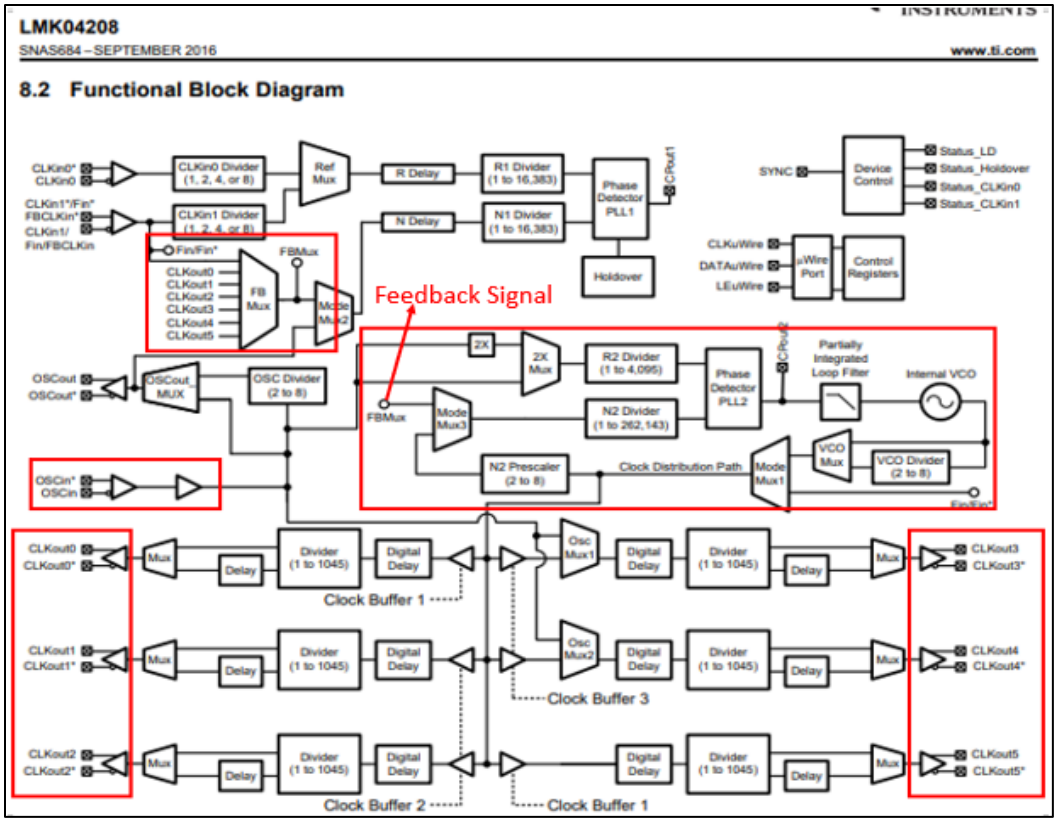
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)

18. TI's LMK04208 includes a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to a first control signal. The first

control signal is configured to minimize a difference in delay between the plurality of output clock signals.

19. For example, TI's LMK04208 is a clock generator that can generate six clock outputs ("said plurality of output clock signals") in response to the OSCin signal ("a reference clock signal") and the FBMux signal ("a feedback signal"). It provides low output-to-output skew or delay and has a 0-delay mode in which the feedback signal can be either internal or external. When the feedback is internal (during the 0-delay mode), the feedback signal is selected from the six output clock signals using a multiplexer and related circuitry ("a second circuit"). The 0-delay mode uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all of the outputs. The LMK04208 includes a control signal ("a first control signal") that indicates which output clock signal has the lowest frequency. The multiplexer, in response to the control signal ("a first control signal"), selects one of the output clock signals as the feedback signal (i.e., the lowest frequency output clock signal).

20. Further, the inputs to the multiplexer are connected to six clock outputs, and this configuration allows the LMK04208 to operate as a closed-loop system for all of the six clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals. The accuracy in generating output clock signals minimizes the delay between them. The control signal of the closed-loop configuration can select one of the outputs and is, therefore, configured to minimize the delay between output signals.



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22).

8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)

8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

Electrical Characteristics (continued)

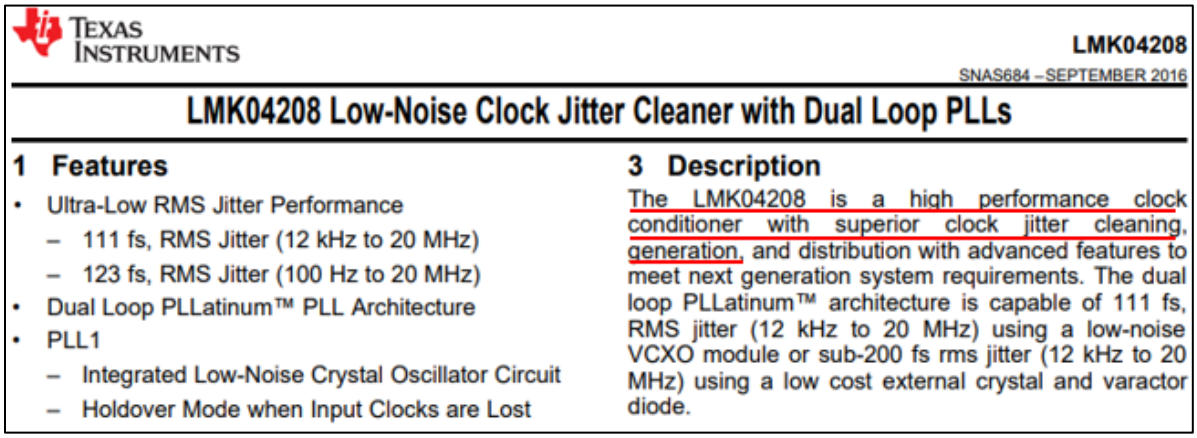
3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SKEW and DELAY						
$\|T_{SKEW}\|$	Maximum CLKoutX to CLKoutY(4)(17)	LVDS-to-LVDS, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout(4)(17)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz.		100		
$MixedT_{SKEW}$	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
$td_{0\text{-}DELAY}$	CLKin to CLKoutX delay(17)	MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0		1850		ps
		MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0; VCO Frequency = 2949.12 MHz Analog delay select = 0; Feedback clock digital delay = 11; Feedback clock half step = 1; Output clock digital delay = 5; Output clock half step = 0;		0		

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 11)

21. TI has infringed the '530 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals.

22. For example, TI's LMK04208 is a clock generator that can generate six clock outputs ("a plurality of output clock signals") and has a minimum output-to-output skew or delay.



TEXAS INSTRUMENTS

LMK04208

SNAS684 – SEPTEMBER 2016

LMK04208 Low-Noise Clock Jitter Cleaner with Dual Loop PLLs

1 Features

- Ultra-Low RMS Jitter Performance
  - 111 fs, RMS Jitter (12 kHz to 20 MHz)
  - 123 fs, RMS Jitter (100 Hz to 20 MHz)
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode when Input Clocks are Lost

3 Description

The LMK04208 is a high performance clock conditioner with superior clock jitter cleaning, generation, and distribution with advanced features to meet next generation system requirements. The dual loop PLLatinum™ architecture is capable of 111 fs, RMS jitter (12 kHz to 20 MHz) using a low-noise VCXO module or sub-200 fs rms jitter (12 kHz to 20 MHz) using a low cost external crystal and varactor diode.

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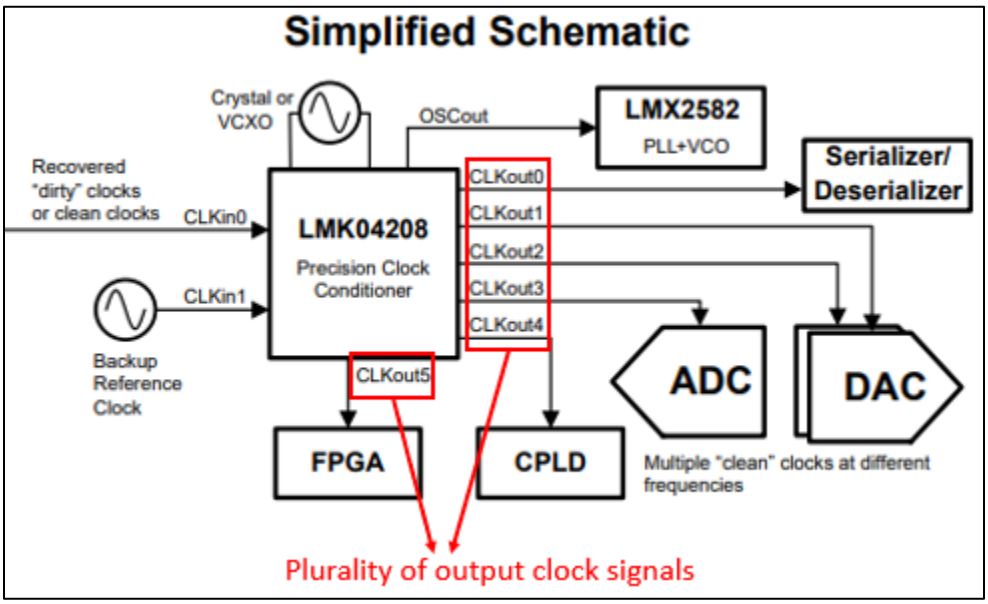

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Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SKEW and DELAY						
$\lvert T_{SKEW} \rvert$	Maximum CLKoutX to CLKoutY(4)(17)	LVDS-to-LVDS, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout(4)(17)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz.		100		
$Mixed T_{SKEW}$	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
$td_{0\text{-}DELAY}$	CLKin to CLKoutX delay(17)	MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0		1850		ps
		MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0; VCO Frequency = 2949.12 MHz Analog delay select = 0; Feedback clock digital delay = 11; Feedback clock half step = 1; Output clock digital delay = 5; Output clock half step = 0;		0		

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8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

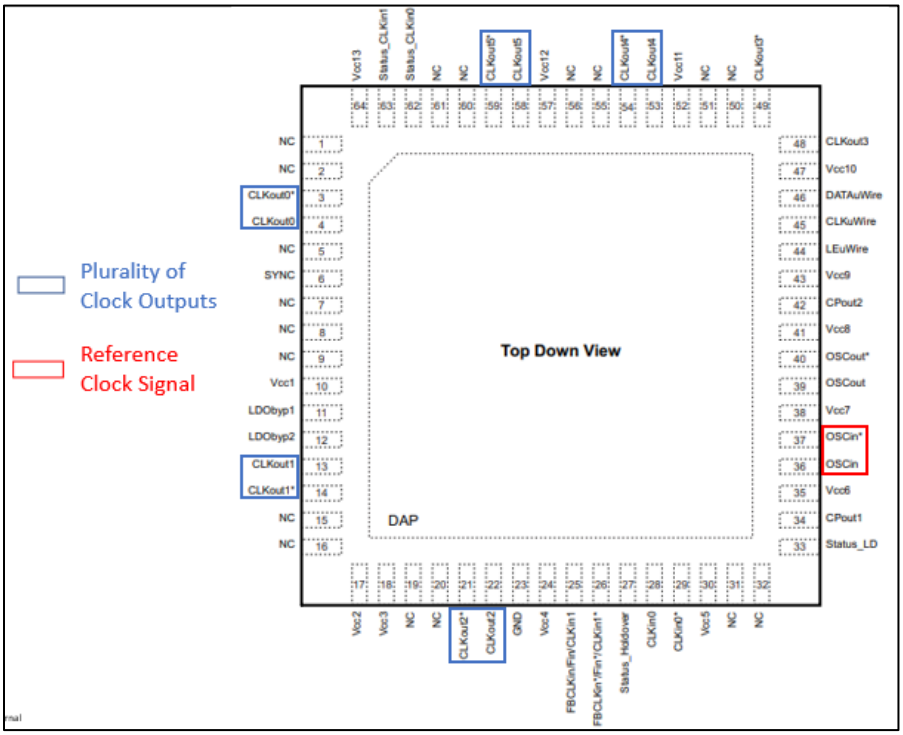
To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

23. TI has infringed the ’530 Patent by using the accused products and thereby practicing a method that includes generating output clock signals in response to a reference clock signal and a feedback signal.

24. For example, TI’s LMK04208 is a clock generator that can generate six clock outputs (“said output clock signals”) in response to the OSCin signal (“a reference clock signal”) and the FBMux signal (“a feedback signal”).



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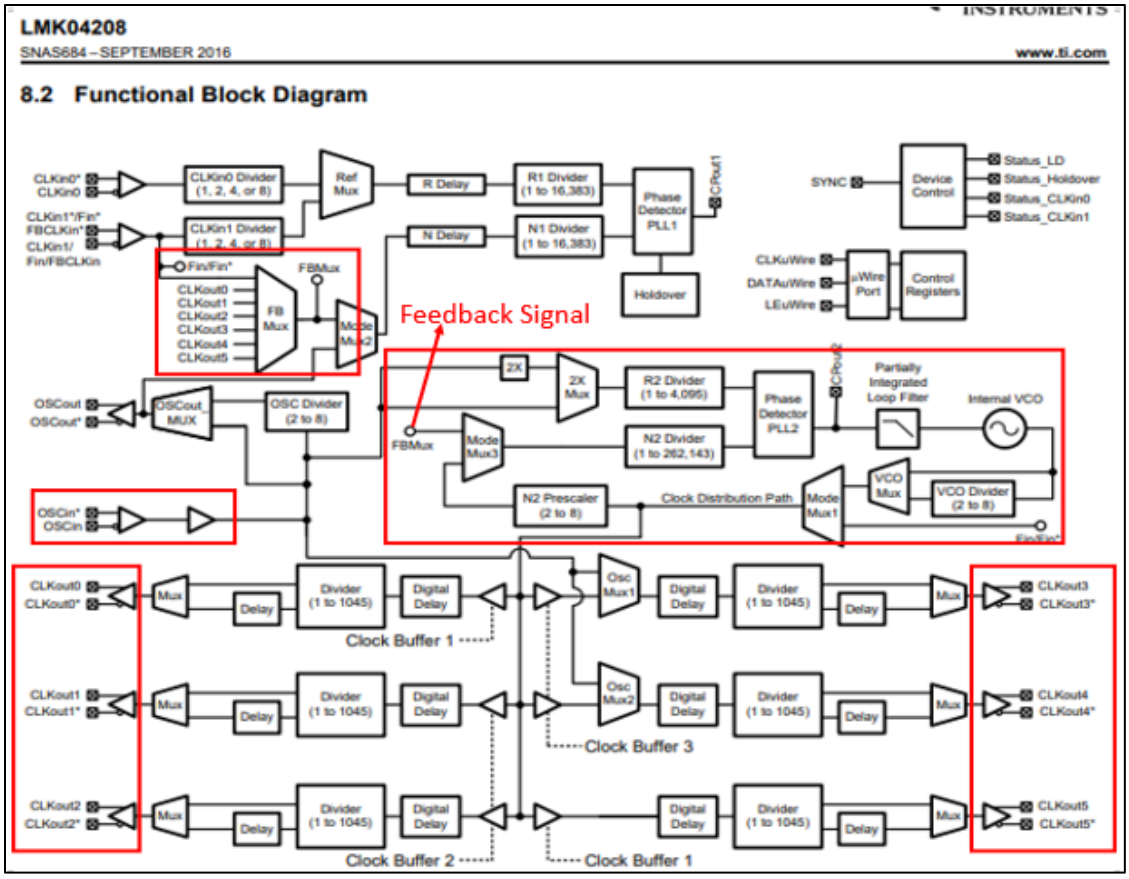
Pin Functions(1)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
36, 37	OSCin, OSCin*	I	ANLG	Feedback to PLL1, Reference input to PLL2. AC Coupled.
3, 4	CLKout0*, CLKout0	O	Programmable	Clock output 0.
13, 14	CLKout1, CLKout1*	O	Programmable	Clock output 1.
21, 22	CLKout2*, CLKout2	O	Programmable	Clock output 2.
48, 49	CLKout3, CLKout3*	O	Programmable	Clock output 3.
53, 54	CLKout4, CLKout4*	O	Programmable	Clock output 4.
58, 59	CLKout5, CLKout5*	O	Programmable	Clock output 5.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (pages 3–4)



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

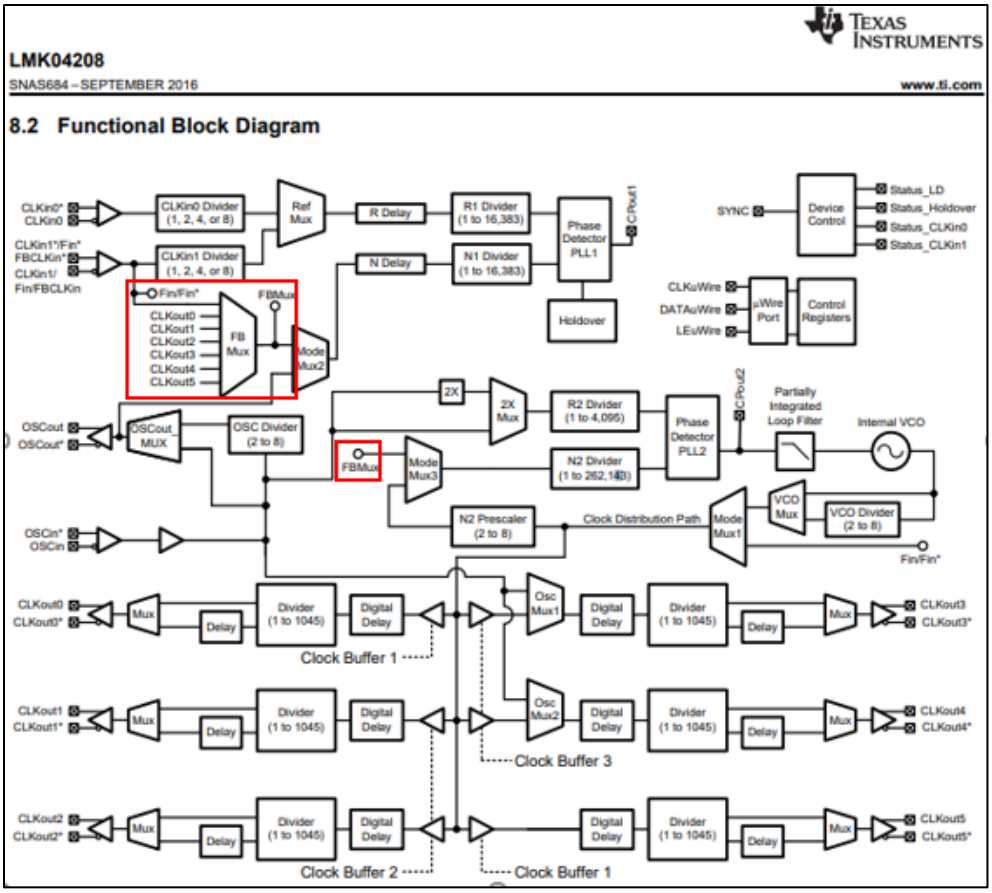
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)

25. TI has infringed the '530 Patent by using the accused products and thereby practicing a method that includes selecting one of its output clock signals as the feedback signal in response to a control signal.

26. For example, TI's LMK04208 is a clock generator that can generate six clock outputs ("said output clock signals") in response to the OSCin signal ("a reference clock signal") and the FBMux signal ("a feedback signal").

27. The LMK04208 has a 0-delay mode in which the feedback signal can be either internal or external. When the feedback is internal (during the 0-delay mode), the feedback signal is selected from the six output clock signals using a multiplexer. The 0-delay mode uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all of the outputs. The LMK04208 includes a control signal ("a control signal") that indicates which output clock signal has the lowest frequency. The multiplexer, in response to the control signal, selects one of the output clock signals as the feedback signal (i.e., the lowest frequency output clock signal).

28. Further, the inputs to the multiplexer are connected to six clock outputs, and this configuration allows the LMK04208 to operate as a closed-loop system for all of the six clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 4).

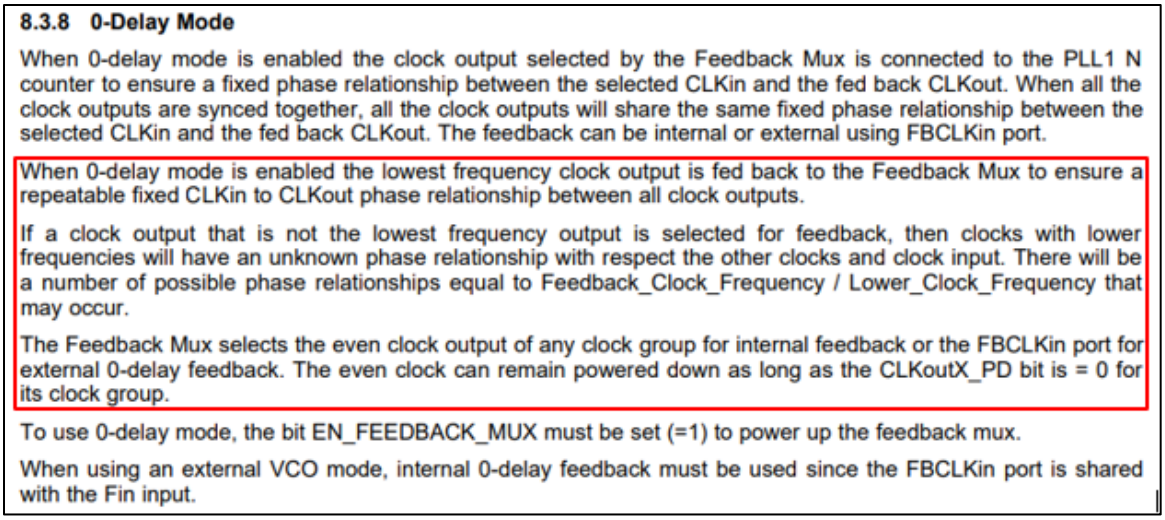
8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)



8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

29. TI has had knowledge of the ’530 Patent at least as of the date when it was notified of the filing of this action.

30. Liberty Patents has been damaged as a result of the infringing conduct by TI alleged above. Thus, TI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

31. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the ’530 Patent.

COUNT II

DIRECT INFRINGEMENT OF U.S. PATENT NO. 6,734,740

32. On May 11, 2004, U.S. Patent No. 6,734,740 (“the ’740 Patent”) was duly and legally issued by the United States Patent and Trademark Office for an invention entitled “Enhanced ZDB Feedback Methodology Utilizing Binary Weighted Techniques.”

33. Liberty Patents is the owner of the '740 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '740 Patent against infringers, and to collect damages for all relevant times.

34. TI made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, its LMK04208 Ultra Low Noise Clock Jitter Cleaner With 6 Programmable Outputs and other products with ZDB technology that can select one of the output clock signals as the feedback signal based on a control signal[11] ("accused products"):

Source: https://www.ti.com/product/LMK04208

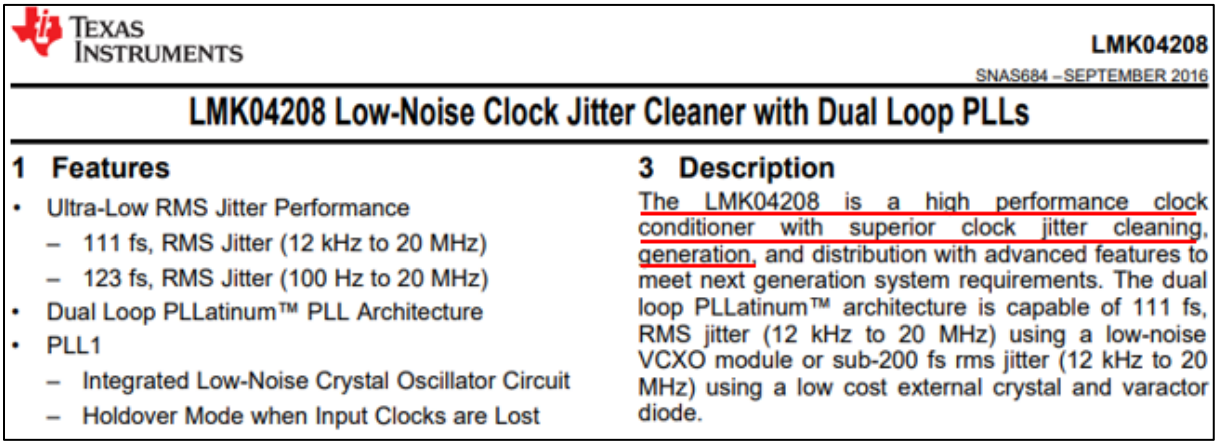
35. By doing so, TI has directly infringed (literally and/or under the doctrine of equivalents) at least Claims 1 and 16 of the '740 Patent. TI's infringement in this regard is ongoing.

[11] *See, e.g.*, TI CDCVF25084, LMK03200, LMK04832-SP, LMK04832, LMK04828-EP, LMK05028, LMK04616, LMK04610, LMK04821, LMK04826, MK04828, LMK04816, LMK04906, LMK04803, LMK04805, LMK04806, LMK04808, LMK05028EVM, LMK03200EVAL, LMK04832EVM-CVAL, ADC12DJ3200EVMCVAL, ADC12DJ3200EVMCVAL-BDL, LMK04832EVM, LMK04616EVM, LMK04610EVM, LMK04208EVM, LMK04821EVM, LMK04826BEVM.

36. TI's LMK04208 is an exemplary accused product. It includes a first circuit configured to present a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

37. For example, TI's LMK04208 is a clock generator that can generate six clock outputs and has a minimum output-to-output skew or delay. It includes a phase locked loop (PLL) with multiple divider circuits, a phase/frequency detector, filters, a voltage-controlled oscillator (VCO), and buffers ("a first circuit") for generating multiple clock outputs ("a plurality of output clock signals") in response to the OSCin signal ("a reference clock signal") and the FBMux signal ("a feedback signal").

38. The LMK04208 has a 0-delay mode that uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all of the outputs. The LMK04208 includes a control signal ("a first control signal") that indicates which output clock signal has the lowest frequency. Because the lowest frequency output clock signal is one of the plurality of output clock signals, the first control signal (which indicates the lowest frequency output clock signal) is generated in response to the OSCin signal and the FBMux signal.



TEXAS INSTRUMENTS

LMK04208

SNAS684 – SEPTEMBER 2016

LMK04208 Low-Noise Clock Jitter Cleaner with Dual Loop PLLs

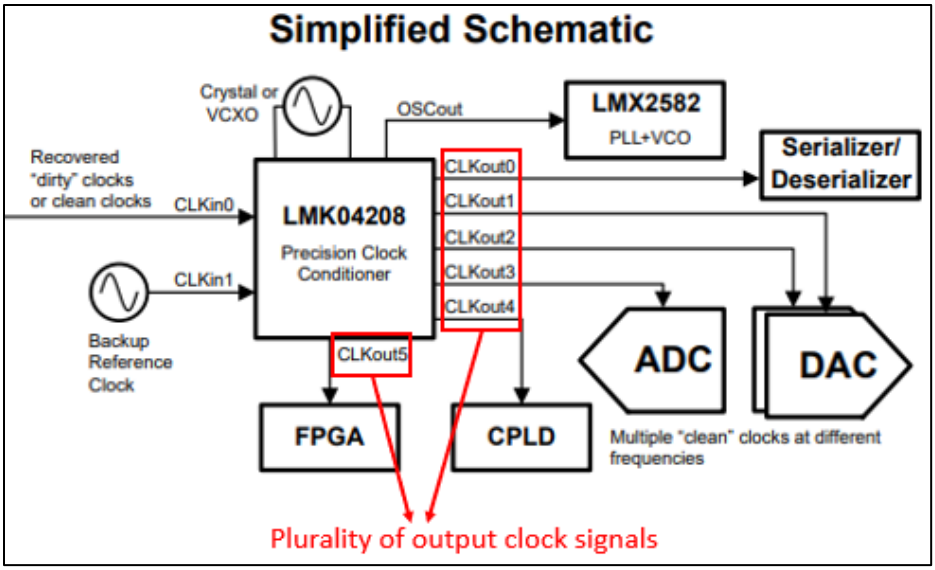
1 Features

- Ultra-Low RMS Jitter Performance
  - 111 fs, RMS Jitter (12 kHz to 20 MHz)
  - 123 fs, RMS Jitter (100 Hz to 20 MHz)
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode when Input Clocks are Lost

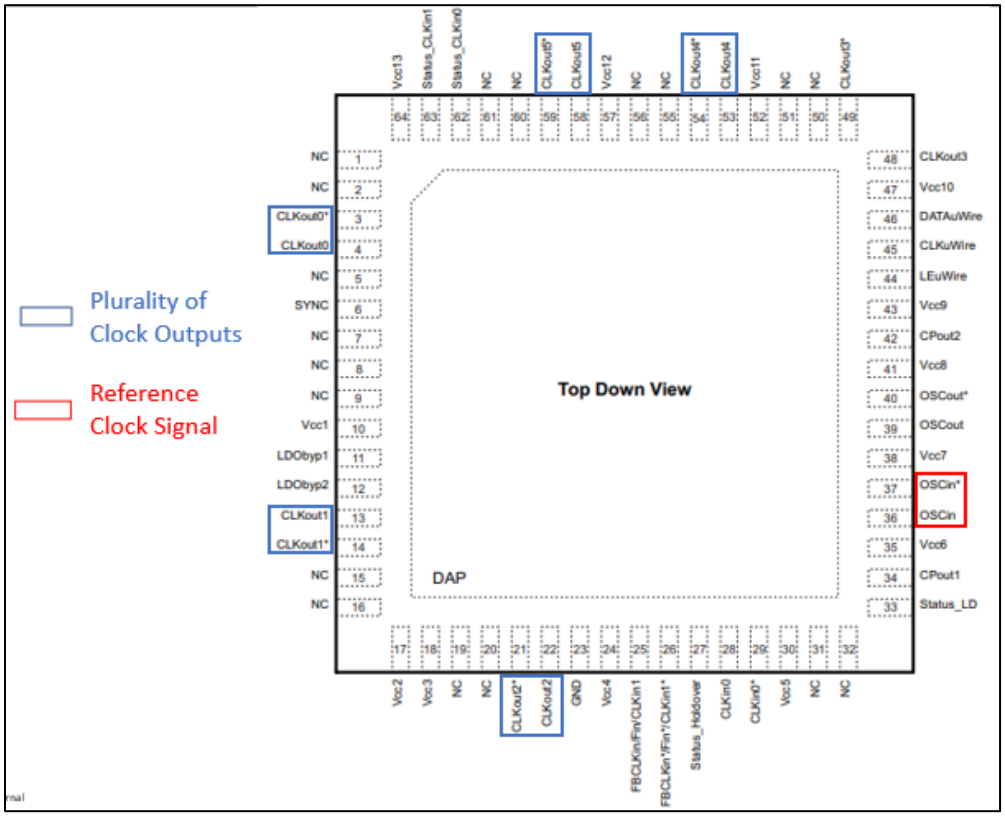
3 Description

The LMK04208 is a high performance clock conditioner with superior clock jitter cleaning, generation, and distribution with advanced features to meet next generation system requirements. The dual loop PLLatinum™ architecture is capable of 111 fs, RMS jitter (12 kHz to 20 MHz) using a low-noise VCXO module or sub-200 fs rms jitter (12 kHz to 20 MHz) using a low cost external crystal and varactor diode.

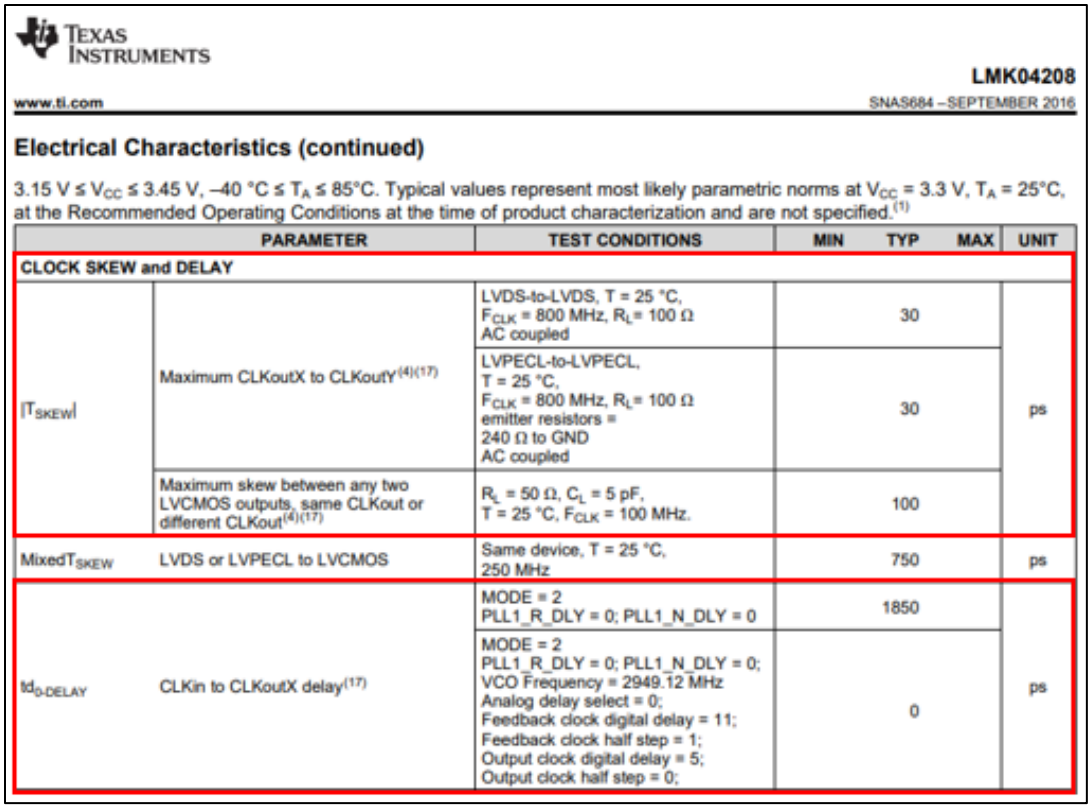
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 3)

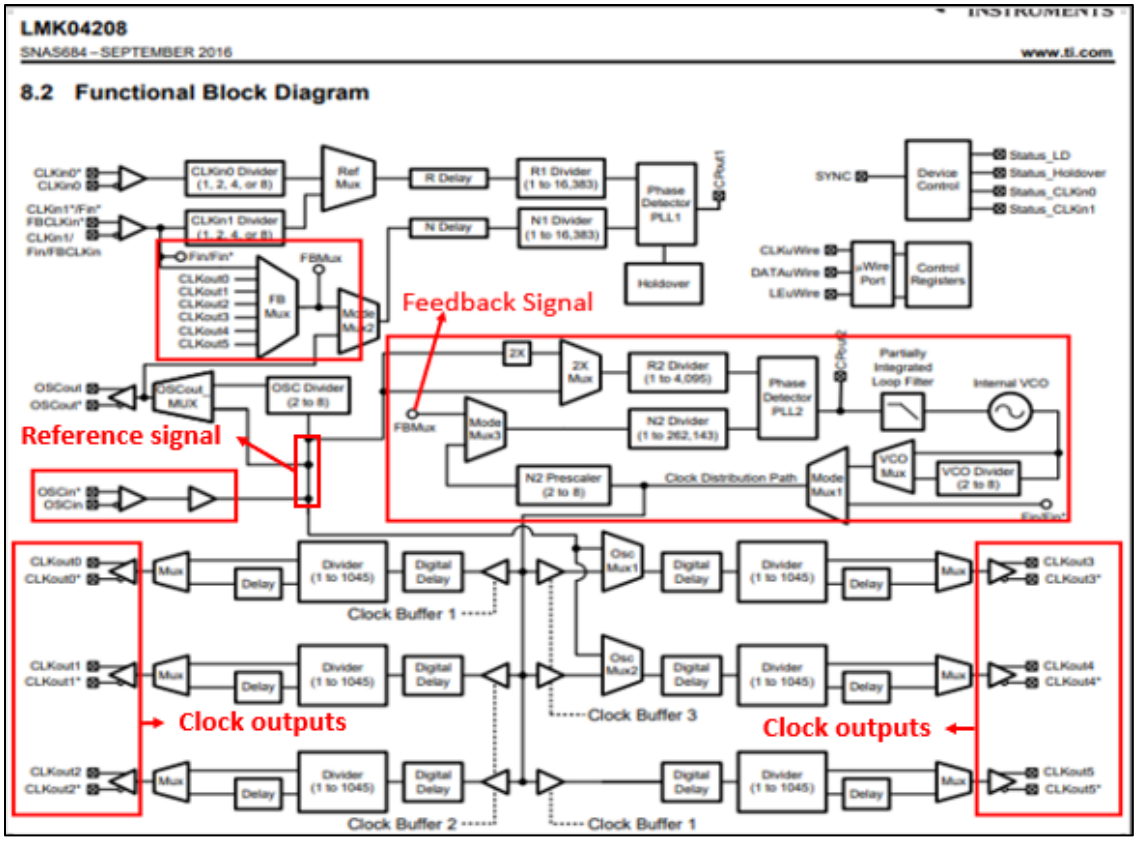


Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SKEW and DELAY						
$\lvert T_{SKEW} \rvert$	Maximum CLKoutX to CLKoutY(4)(17)	LVDS-to-LVDS, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout(4)(17)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz.		100		
$Mixed T_{SKEW}$	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
$td_{0\text{-}DELAY}$	CLKin to CLKoutX delay(17)	MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0		1850		ps
		MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0; VCO Frequency = 2949.12 MHz Analog delay select = 0; Feedback clock digital delay = 11; Feedback clock half step = 1; Output clock digital delay = 5; Output clock half step = 0;		0		

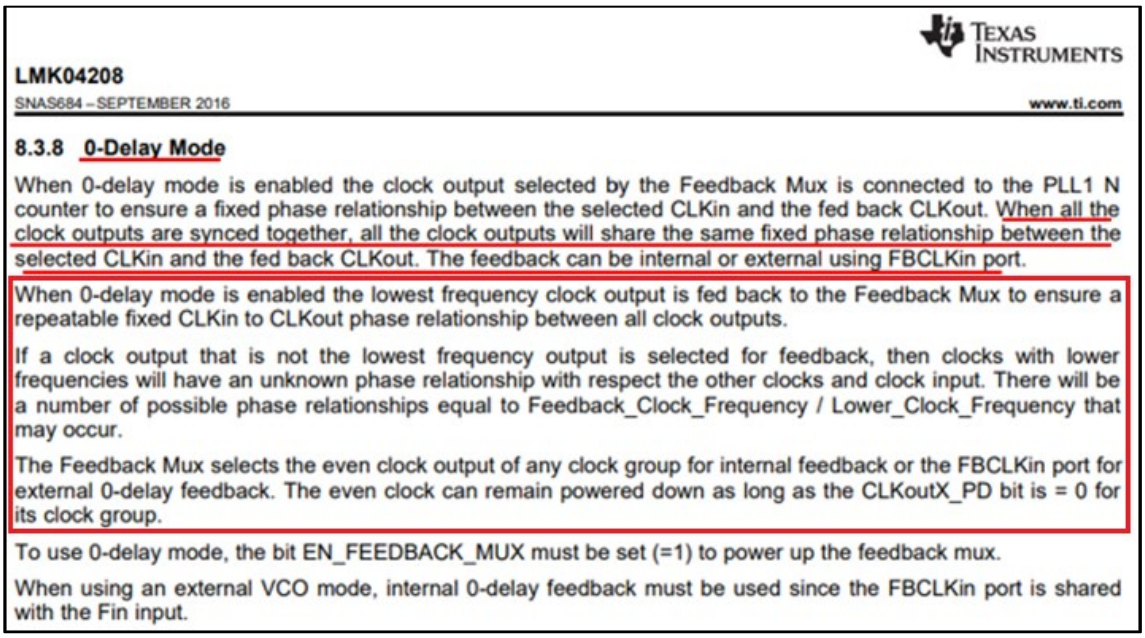
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 11)



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides low-noise jitter cleaner functionality while the second PLL (PLL2) performs the clock generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When paired with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)



LMK04208
SNAS684 – SEPTEMBER 2016
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8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

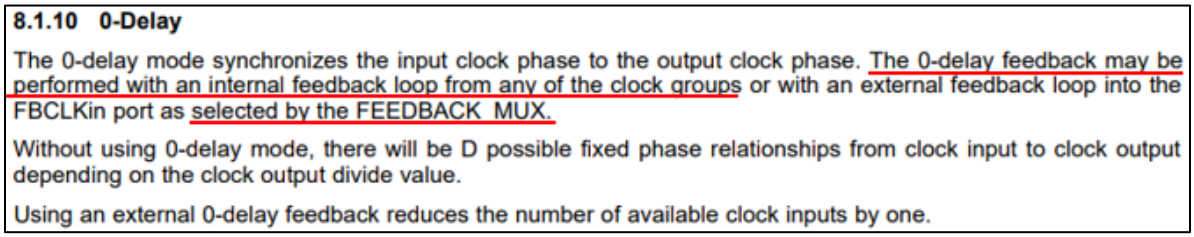
If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)



8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

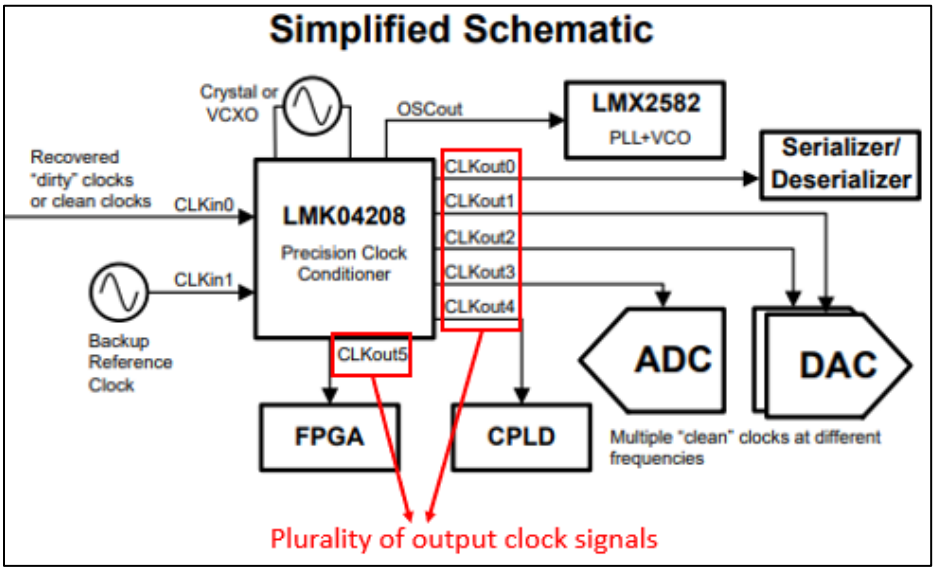
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)

39. TI's LMK04208 includes a second circuit configured to select one of the plurality of output clock signals as the feedback signal in response to the first control signal.

40. For example, TI's LMK04208 is a clock generator that can generate six clock outputs ("said plurality of output clock signals") in response to the OSCin signal ("a reference clock signal") and the FBMux signal ("a feedback signal"). The LMK04208 has a 0-delay mode in which the feedback signal can be either internal or external. When the feedback is internal (during the 0-delay mode), the feedback signal is selected from the six output clock signals using a multiplexer and related circuitry ("a second circuit"). The inputs to the multiplexer are connected to six clock outputs, and this configuration allows the LMK04208 to operate as a

closed-loop system for all of the six clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

41. The 0-delay mode uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all the outputs. The LMK04208 includes a first control signal ("said first control signal") that indicates which output clock signal has the lowest frequency. The multiplexer, in response to the first control signal, selects one of the output clock signals as the feedback signal (i.e., the lowest frequency output clock signal).



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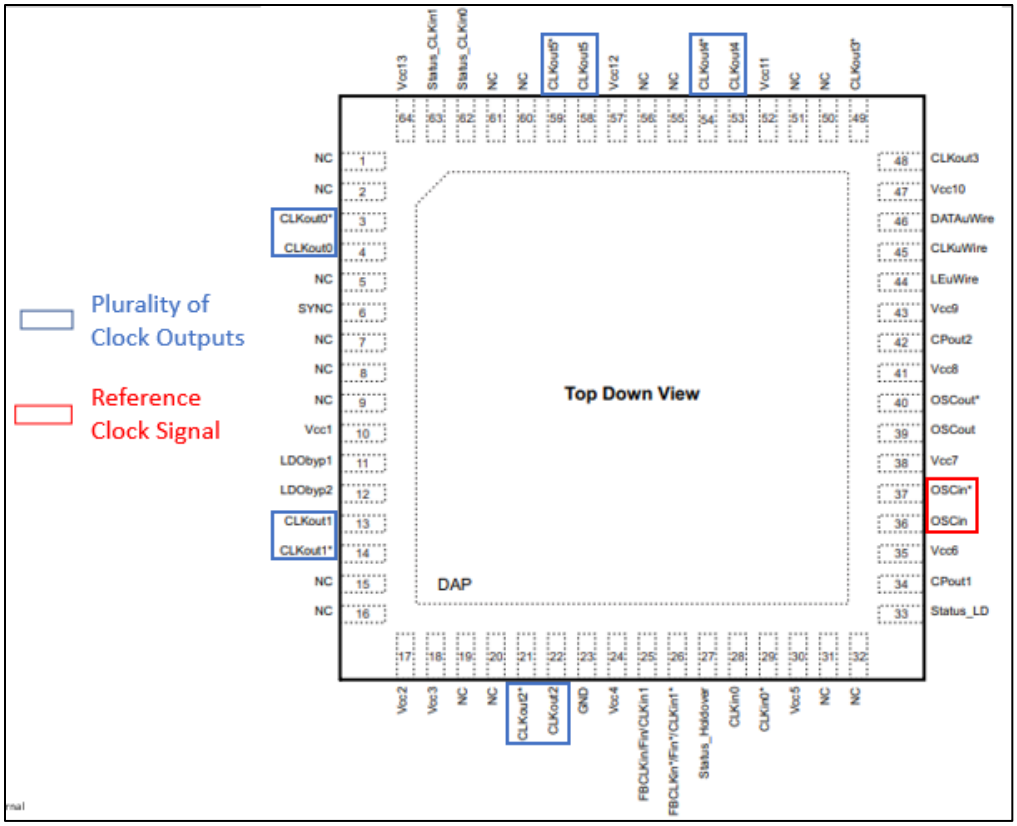

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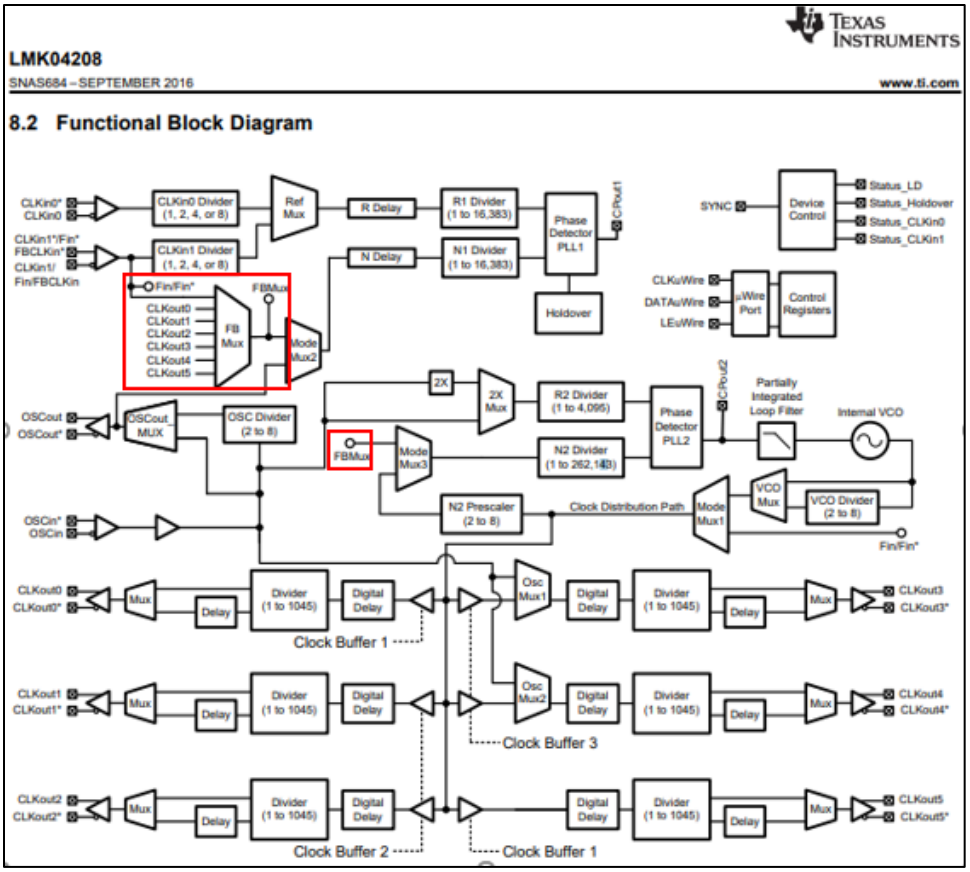

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

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8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

42. TI has infringed the ’740 Patent by using the accused products and thereby practicing a method for minimizing a difference in delay between a plurality of output clock signals.

43. For example, TI’s LMK04208 is a clock generator that generates six clock outputs (“a plurality of output clock signals”) and has a minimum output-to-output skew or delay.

TEXAS INSTRUMENTS

LMK04208

SNAS684 – SEPTEMBER 2016

LMK04208 Low-Noise Clock Jitter Cleaner with Dual Loop PLLs

1 Features

- Ultra-Low RMS Jitter Performance
  - 111 fs, RMS Jitter (12 kHz to 20 MHz)
  - 123 fs, RMS Jitter (100 Hz to 20 MHz)
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode when Input Clocks are Lost

3 Description

The LMK04208 is a high performance clock conditioner with superior clock jitter cleaning, generation, and distribution with advanced features to meet next generation system requirements. The dual loop PLLatinum™ architecture is capable of 111 fs, RMS jitter (12 kHz to 20 MHz) using a low-noise VCXO module or sub-200 fs rms jitter (12 kHz to 20 MHz) using a low cost external crystal and varactor diode.

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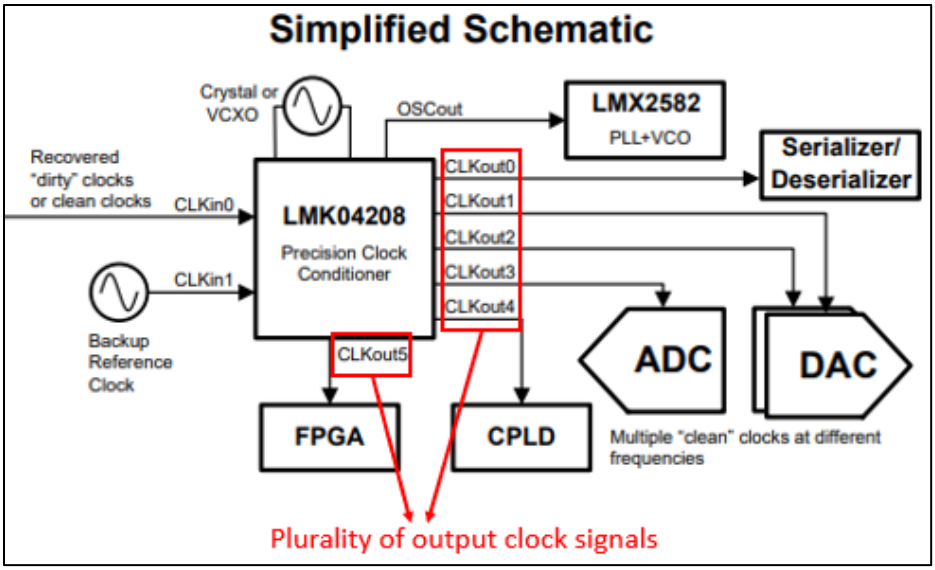

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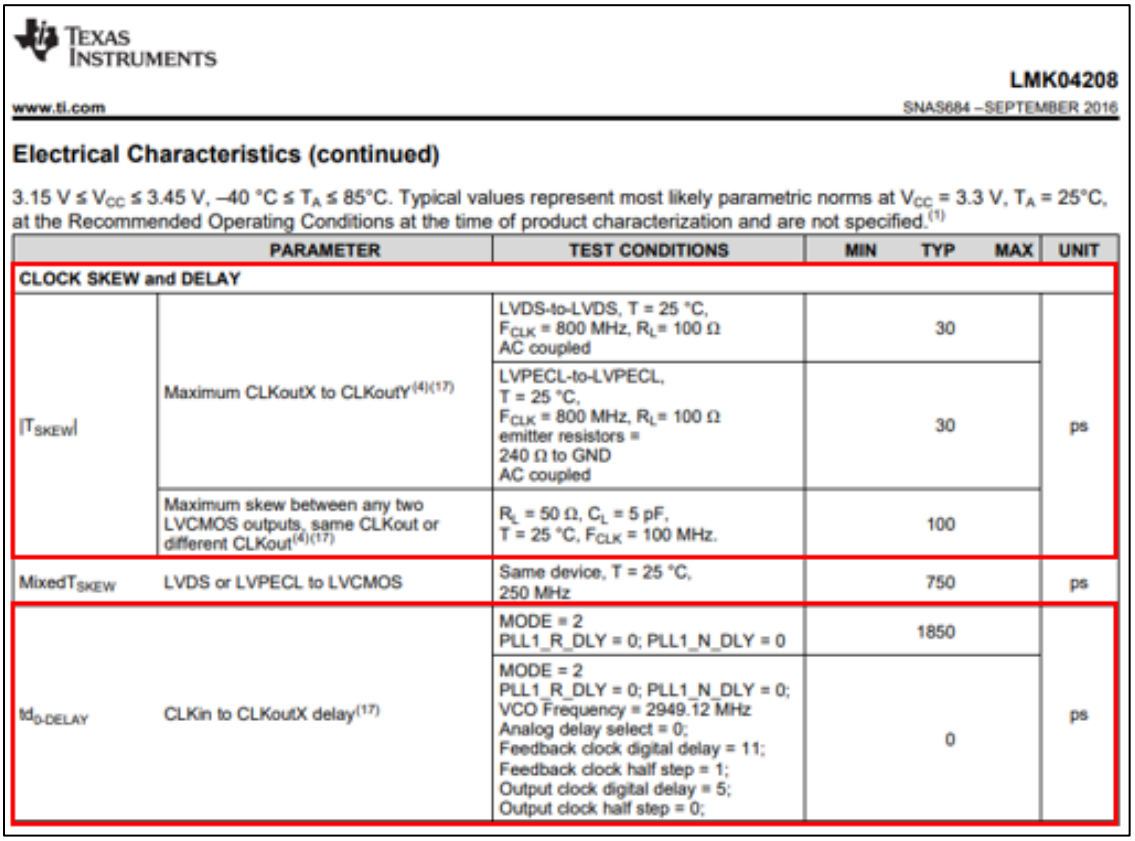

TEXAS INSTRUMENTS

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LMK04208

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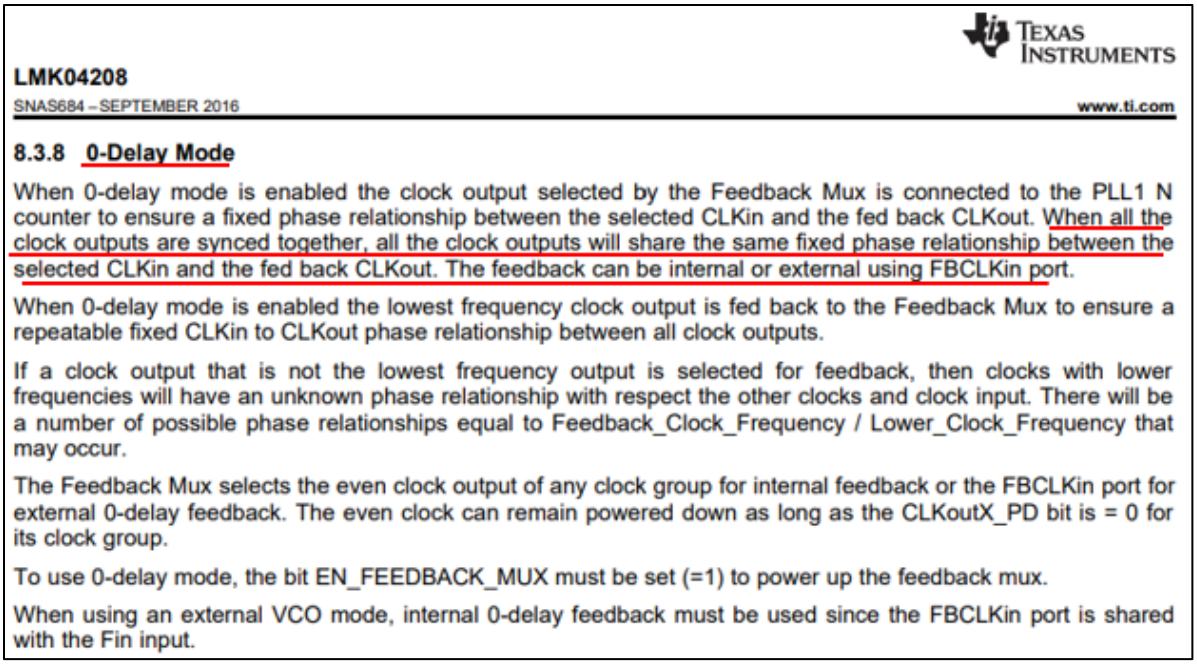
Electrical Characteristics (continued)

3.15 V ≤ V_{CC} ≤ 3.45 V, –40 °C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not specified.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK SKEW and DELAY						
$\lvert T_{SKEW} \rvert$	Maximum CLKoutX to CLKoutY(4)(17)	LVDS-to-LVDS, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω AC coupled		30		ps
		LVPECL-to-LVPECL, T = 25 °C, F_{CLK} = 800 MHz, R_L = 100 Ω emitter resistors = 240 Ω to GND AC coupled		30		
	Maximum skew between any two LVCMOS outputs, same CLKout or different CLKout(4)(17)	R_L = 50 Ω, C_L = 5 pF, T = 25 °C, F_{CLK} = 100 MHz.		100		
MixedT_{SKEW}	LVDS or LVPECL to LVCMOS	Same device, T = 25 °C, 250 MHz		750		ps
$td_{0\text{-}DELAY}$	CLKin to CLKoutX delay(17)	MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0		1850		ps
		MODE = 2 PLL1_R_DLY = 0; PLL1_N_DLY = 0; VCO Frequency = 2949.12 MHz Analog delay select = 0; Feedback clock digital delay = 11; Feedback clock half step = 1; Output clock digital delay = 5; Output clock half step = 0;		0		

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 11)



LMK04208
SNAS684 – SEPTEMBER 2016
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8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

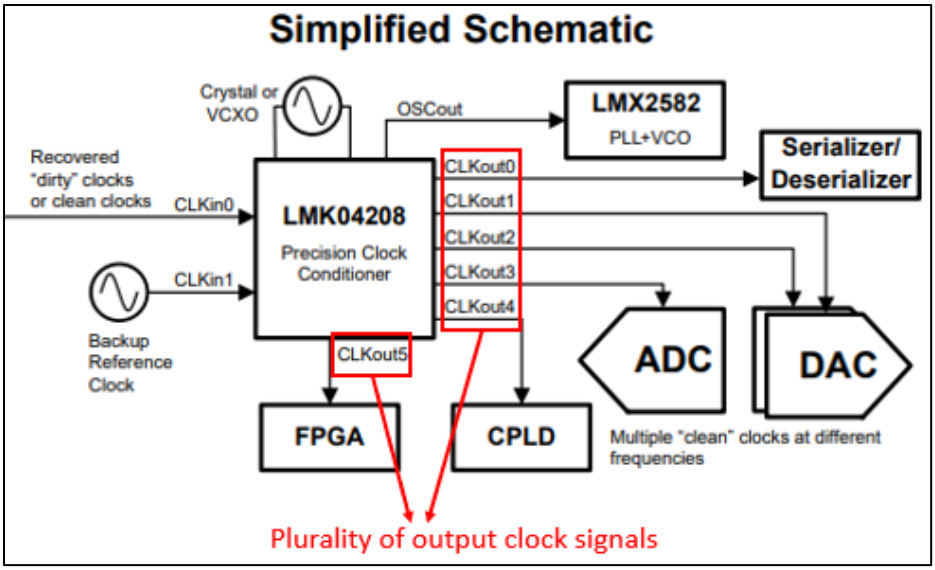
To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

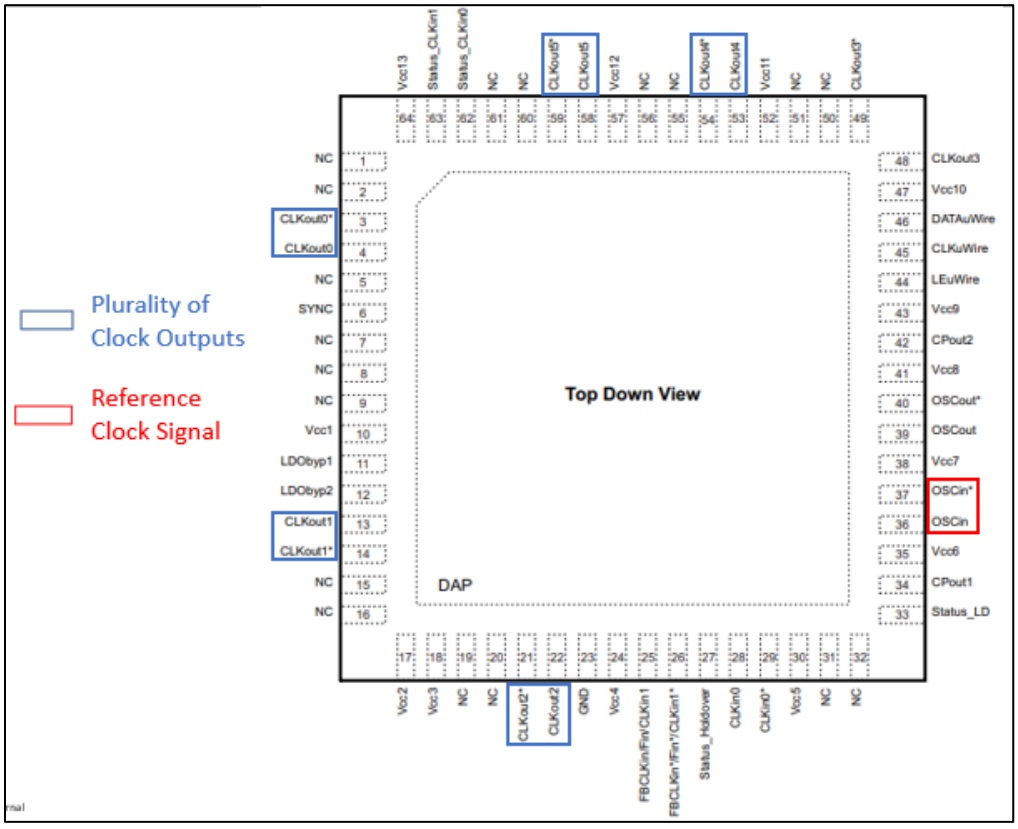
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

44. TI has infringed the ’740 Patent by using the accused products and thereby practicing a method that includes generating a plurality of output clock signals and a first control signal in response to a reference clock signal and a feedback signal.

45. For example, TI’s LMK04208 is a clock generator that can generate six clock outputs (“said plurality of output clock signals”) in response to the OSCin signal (“a reference clock signal”) and the FBMux signal (“a feedback signal”). The LMK04208 has a 0-delay mode that uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all of the outputs. The LMK04208 includes a control signal (“a first control signal”) that indicates which output clock signal has the lowest frequency. Because the lowest frequency output clock signal is one of the plurality of output clock signals, the first control signal (which indicates the lowest frequency output clock signal) is generated in response to the OSCin signal and the FBMux signal.



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 1)

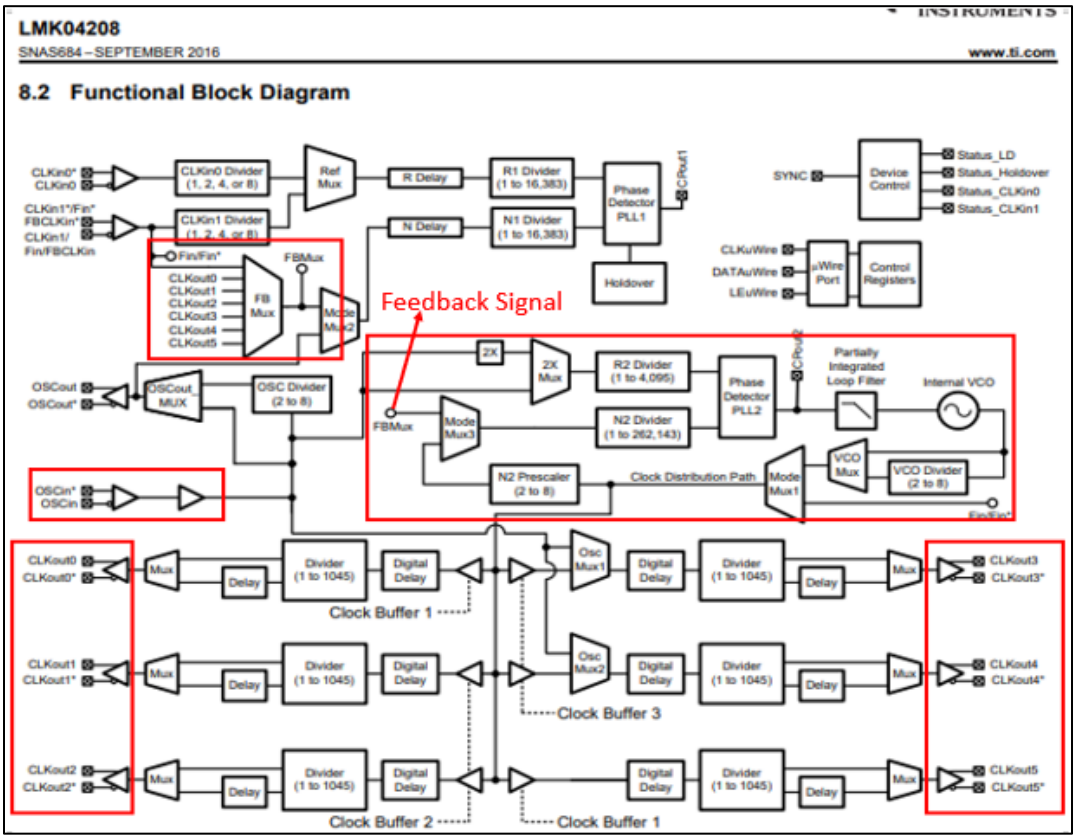


Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 3)

Pin Functions[1]

PIN NO.	PIN NAME	I/O	TYPE	DESCRIPTION
36, 37	OSCin, OSCin*	I	ANLG	Feedback to PLL1, Reference input to PLL2. AC Coupled.
3, 4	CLKout0*, CLKout0	O	Programmable	Clock output 0.
13, 14	CLKout1, CLKout1*	O	Programmable	Clock output 1.
21, 22	CLKout2*, CLKout2	O	Programmable	Clock output 2.
48, 49	CLKout3, CLKout3*	O	Programmable	Clock output 3.
53, 54	CLKout4, CLKout4*	O	Programmable	Clock output 4.
58, 59	CLKout5, CLKout5*	O	Programmable	Clock output 5.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (pages 3–4)



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

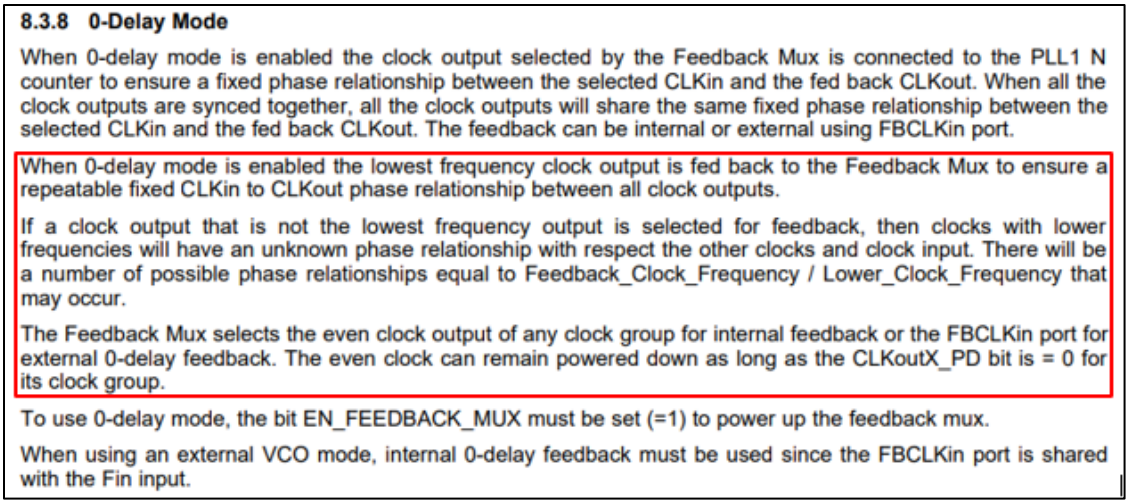
8.1.10 0-Delay

The 0-delay mode synchronizes the input clock phase to the output clock phase. The 0-delay feedback may be performed with an internal feedback loop from any of the clock groups or with an external feedback loop into the FBCLKin port as selected by the FEEDBACK_MUX.

Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)



8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

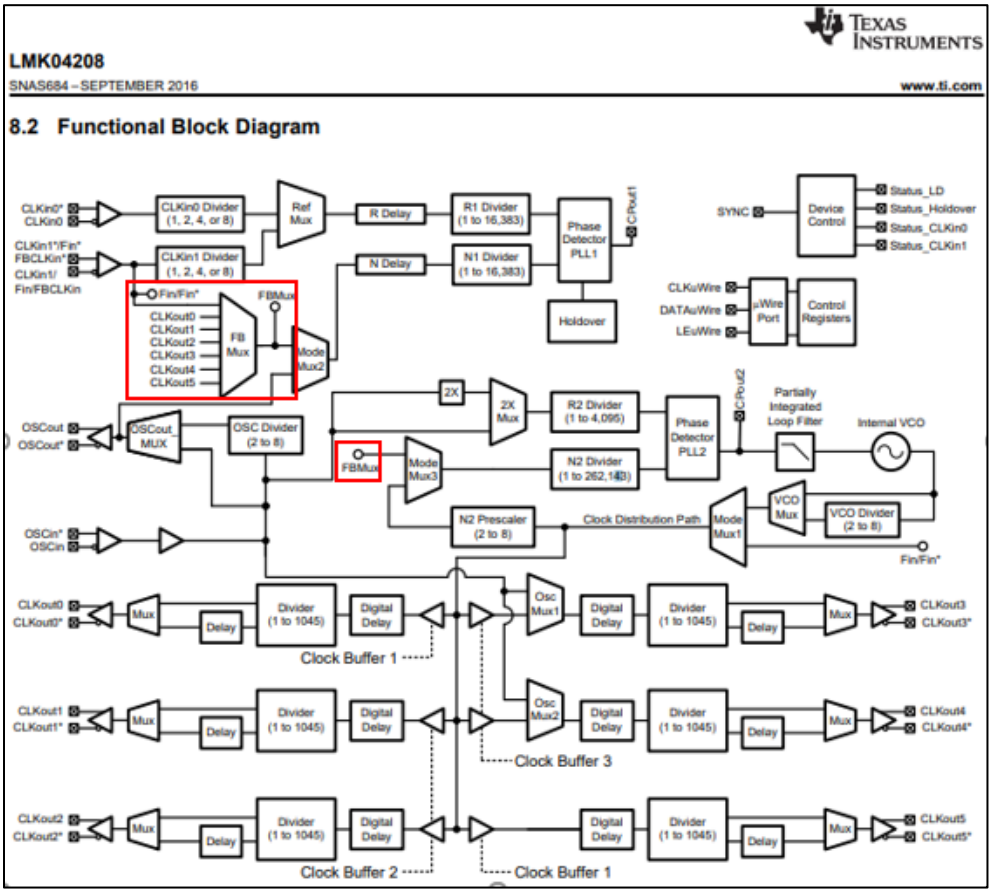
Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

46. TI has infringed the ’740 Patent by using the accused products and thereby practicing a method that includes selecting one of the output clock signals as the feedback signal in response to the first control signal.

47. For example, TI’s LMK04208 is a clock generator that can generate six clock outputs (“said output clock signals”) in response to the OSCin signal (“a reference clock signal”) and the FBMux signal (“a feedback signal”). The LMK04208 has a 0-delay mode in which the feedback signal can be either internal or external. When the feedback is internal (during the 0-delay mode), the feedback signal is selected from the six output clock signals using a multiplexer and related circuitry. The inputs to the multiplexer are connected to six clock outputs, and this configuration allows the LMK04208 to operate as a closed-loop system for all of the six clock outputs. The closed-loop system mitigates the external effects of temperature, loading, etc., and helps in generating accurate output clock signals.

48. The 0-delay mode uses the lowest frequency clock output as the feedback signal to maintain a phase relationship between all the outputs. The LMK04208 includes a first control signal (“said first control signal”) that indicates which output clock signal has the lowest

frequency. The multiplexer, in response to the first control signal, selects one of the output clock signals as the feedback signal (i.e., the lowest frequency output clock signal).



Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 22)

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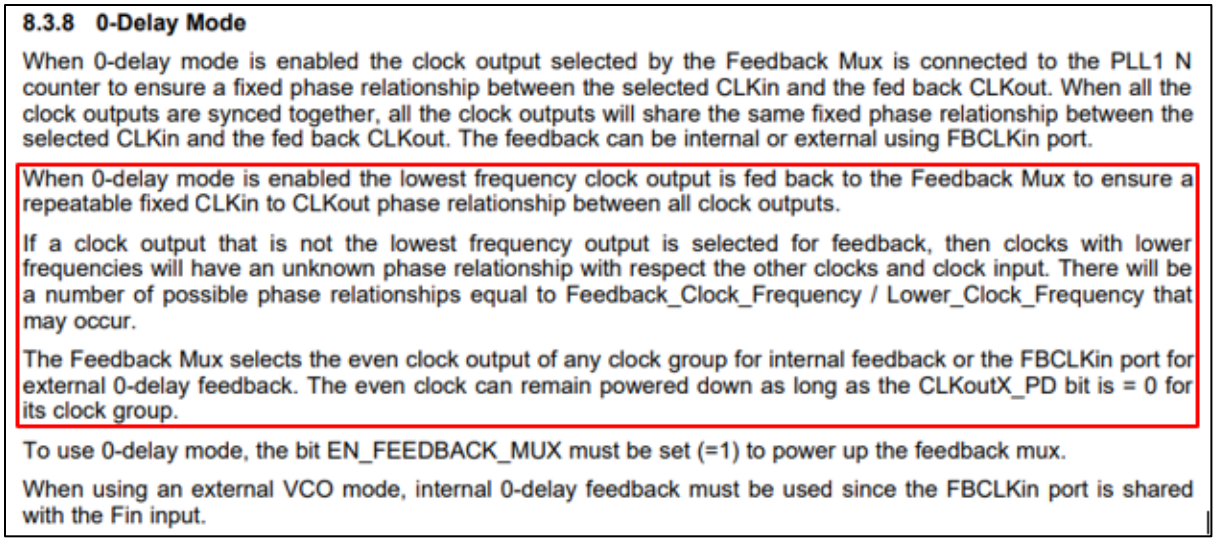
Without using 0-delay mode, there will be D possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 21)



8.3.8 0-Delay Mode

When 0-delay mode is enabled the clock output selected by the Feedback Mux is connected to the PLL1 N counter to ensure a fixed phase relationship between the selected CLKin and the fed back CLKout. When all the clock outputs are synced together, all the clock outputs will share the same fixed phase relationship between the selected CLKin and the fed back CLKout. The feedback can be internal or external using FBCLKin port.

When 0-delay mode is enabled the lowest frequency clock output is fed back to the Feedback Mux to ensure a repeatable fixed CLKin to CLKout phase relationship between all clock outputs.

If a clock output that is not the lowest frequency output is selected for feedback, then clocks with lower frequencies will have an unknown phase relationship with respect the other clocks and clock input. There will be a number of possible phase relationships equal to Feedback_Clock_Frequency / Lower_Clock_Frequency that may occur.

The Feedback Mux selects the even clock output of any clock group for internal feedback or the FBCLKin port for external 0-delay feedback. The even clock can remain powered down as long as the CLKoutX_PD bit is = 0 for its clock group.

To use 0-delay mode, the bit EN_FEEDBACK_MUX must be set (=1) to power up the feedback mux.

When using an external VCO mode, internal 0-delay feedback must be used since the FBCLKin port is shared with the Fin input.

Source: http://www.ti.com/lit/ds/symlink/lmk04208.pdf?&ts=1589467330546 (page 42)

49. TI has had knowledge of the ’740 Patent at least as of the date when it was notified of the filing of this action.

50. Liberty Patents has been damaged as a result of the infringing conduct by TI alleged above. Thus, TI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

51. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the ’740 Patent.

ADDITIONAL ALLEGATIONS REGARDING INFRINGEMENT AND PERSONAL JURISDICTION

52. TI has also indirectly infringed the ’530 Patent and the ’740 Patent by inducing others to directly infringe the ’530 Patent and the ’740 Patent.

53. TI has induced the end users and/or TI's customers to directly infringe (literally and/or under the doctrine of equivalents) the '530 Patent and the '740 Patent by using the accused products.

54. TI took active steps, directly and/or through contractual relationships with others, with the specific intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, claims 1 and 15 of the '530 Patent, and claims 1 and 16 of the '740 Patent.

55. Such steps by TI included, among other things, advising or directing customers and end users to use the accused products in an infringing manner; advertising and promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner.

56. TI performed these steps, which constitute induced infringement, with the knowledge of the '530 Patent and the '740 Patent and with the knowledge that the induced acts constitute infringement.

57. TI was and is aware that the normal and customary use of the accused products by TI's customers would infringe the '530 Patent and the '740 Patent. TI's inducement is ongoing.

58. TI has also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to directly infringe (literally and/or under the doctrine of equivalents) the '530 Patent and the '740 Patent by importing, selling or offering to sell the accused products.

59. TI has a significant role in placing the accused products in the stream of commerce with the expectation and knowledge that they will be purchased by consumers in Texas and elsewhere in the United States.

60. TI purposefully directs or controls the making of accused products and their shipment to the United States, using established distribution channels, for sale in Texas and elsewhere within the United States.

61. TI purposefully directs or controls the sale of the accused products into established United States distribution channels, including sales to nationwide retailers. TI's established United States distribution channels include one or more United States based affiliates.

62. TI purposefully directs or controls the sale of the accused products online and in nationwide retailers, including for sale in Texas and elsewhere in the United States, and expects and intends that the accused products will be so sold.

63. TI purposefully places the accused products—whether by itself or through subsidiaries, affiliates, or third parties—into an international supply chain, knowing that the accused products will be sold in the United States, including Texas. Therefore, TI also facilitates the sale of the accused products in Texas.

64. TI took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the '530 Patent and the '740 Patent, including, for example, claims 1 and 15 of the '530 Patent, and claims 1 and 16 of the '740 Patent.

65. Such steps by TI included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing that such importation or sale would occur; and directing, facilitating, or influencing its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to import, sell, or offer to sell the accused products in an infringing manner.

66. TI performed these steps, which constitute induced infringement, with the knowledge of the ’530 Patent and the ’740 Patent, and with the knowledge that the induced acts would constitute infringement.

67. TI performed such steps in order to profit from the eventual sale of the accused products in the United States.

68. TI’s inducement is ongoing.

69. TI has also indirectly infringed by contributing to the infringement of the ’530 Patent and the ’740 Patent. TI has contributed to the direct infringement of the ’530 Patent and the ’740 Patent by the end user of the accused products.

70. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the ’530 Patent and the ’740 Patent, including, for example, claims 1 and 15 of the ’530 Patent, and claims 1 and 16 of the ’740 Patent.

71. The special features include, for example, circuitry that reduces the delay between output clock signals in a zero delay buffer used in a manner that infringes the ’530 Patent and the ’740 Patent.

72. These special features constitute a material part of the invention of one or more of the claims of the ’530 Patent and the ’740 Patent, and are not staple articles of commerce suitable for substantial non-infringing use.

73. TI’s contributory infringement is ongoing.

74. TI has had actual knowledge of the ’530 Patent and the ’740 Patent at least as of the date when it was notified of the filing of this action. Since at least that time, TI has known the scope of the claims of the ’530 Patent and the ’740 Patent, the products that practice the ’530

Patent and the ’740 Patent, and that Liberty Patents is the owner of the ’530 Patent and the ’740 Patent.

75. By the time of trial, TI will have known and intended (since receiving such notice) that its continued actions would infringe and actively induce and contribute to the infringement of one or more claims of the ’530 Patent and the ’740 Patent.

76. Furthermore, TI has a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of Liberty Patents’ patent rights. *See, e.g.*, M. Lemley, “Ignoring Patents,” 2008 Mich. St. L. Rev. 19 (2008).

77. TI’s actions are at least objectively reckless as to the risk of infringing valid patents, and this objective risk was either known or should have been known by TI. TI has knowledge of the ’530 Patent and the ’740 Patent.

78. TI’s customers have infringed the ’530 Patent and the ’740 Patent. TI has encouraged its customers’ infringement.

79. TI’s direct and indirect infringement of the ’530 Patent and the ’740 Patent has been, and/or continues to be willful, intentional, deliberate, and/or in conscious disregard of Liberty Patents’ rights under the patents-in-suit.

80. Liberty Patents has been damaged as a result of TI’s infringing conduct alleged above. Thus, TI is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Liberty Patents hereby requests a trial by jury on all issues so triable by right.

PRAYER FOR RELIEF

Liberty Patents requests that the Court find in its favor and against TI, and that the Court grant Liberty Patents the following relief:

a. Judgment that one or more claims of the ’530 Patent and the ’740 Patent have been infringed, either literally and/or under the doctrine of equivalents, by TI and/or all others acting in concert therewith;

b. A permanent injunction enjoining TI and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the ’530 Patent and the ’740 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the ’530 Patent and the ’740 Patent by such entities;

c. Judgment that TI account for and pay to Liberty Patents all damages to and costs incurred by Liberty Patents because of TI’s infringing activities and other conduct complained of herein, including an award of all increased damages to which Liberty Patents is entitled under 35 U.S.C. § 284;

d. That Liberty Patents be granted pre-judgment and post-judgment interest on the damages caused by TI’s infringing activities and other conduct complained of herein;

e. That this Court declare this an exceptional case and award Liberty Patents its reasonable attorney’s fees and costs in accordance with 35 U.S.C. § 285; and

f. That Liberty Patents be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: January 22, 2021

Respectfully submitted,

/s/ *Zachariah S. Harrington*

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