IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff, v. TEXAS INSTRUMENTS INC, Defendant.	Case No.: 6:21-cv-00140 **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO"), hereby files Complaint for patent infringement against Defendant Texas Instruments Inc. ("TI" or "Defendant"), and alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York 11235.

2. TI is a corporation organized under the laws of the State of Delaware, and may be served with process through its registered agent, CT Corporation System 1999 Bryan Street, Suite 900, Dallas, Texas 75201.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by TI of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. TI is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) TI is a Texas corporation; (ii) TI does business in Texas; (iii) TI sells and offers for sale its products by using distributors and sales representatives located in Texas.

6. Venue is proper in this district under 28 U.S.C. § 1400(b) because (i) TI has committed and continues to commit acts of patent infringement by, inter alia, offering for sale and selling, on their own and as part of a device, infringing TI products; and (ii) has a regular and established place of business in this district, including at 9433 Bee Cave Road, Austin, TX 78746 and 12357 Riata Trace Parkway, Austin, TX 78727.

BACKGROUND

7. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

8. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

9. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

10. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

11. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

12. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

13. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

14. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

15. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

16. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

17. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

18. By email dated September 18, 2019, CCO, via counsel, notified TI of existence of the Patents-in-Suit and of potential infringement of those Patents by TI. CCO's correspondence further identified an exemplary infringing TI product and offered to provide TI with claim charts

for the Patents-in-Suit. CCO's email further invited TI to hold a licensing discussion with CCO.

19. By email dated September 18, 2019, an in-house counsel at TI notified CCO that a different in-house counsel would handle the CCO matter. TI noted that CCO's materials had been forwarded to the appropriate contact at TI.

20. By email dated September 19, 2019, CCO, via counsel, followed up with TI and offered to discuss CCO and its patents.

21. By email dated October 1, 2019, CCO, via counsel, again followed up with TI.

22. By email dated October 17, 2019, CCO, via counsel, again followed up with TI regarding CCO and licensing of CCO's patents.

23. As of the date of this Complaint, CCO has received no further response from TI.

LICENSING

24. As of the time of this Complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, Qualcomm, and Via Technologies, Rockchip, and Socionext.

COUNT I: INFRINGEMENT OF THE '021 PATENT

25. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

26. On information and belief, TI has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States certain processors, microcontrollers, Systems-on-Chips that include DDR3, DDR3L, DDR4, LPDDR2, and/or LPDDR4 memory controller systems ("DDR Controller") (collectively, "Accused TI Products").

27. On information and belief, TI has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk

influence in the transmission line for high-speed transmission of digital data by modifying delays, such as during write training, at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the Accused TI Products, including during regular operation and during development, design, testing, and verification of the DDR Controller, in part because they operate with the guidance of the JEDEC Standard. *See* Ex. 1 at 257-258 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (describing DDR Subsystem and that it comprises the DDR controller, DDR PHY, and wrapper logic to integrate these blocks in the device); Ex. 2 at 6117, 6137 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR subsystem diagram and DDR PHY features description); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing DQS-DQ training); Ex. 17 (External Memory Interfaces Intel Arria 10 FPGA IP User Guide) (describing write DQ ISI/crosstalk).

28. On information and belief, the TI DDR Controller transmits digital data through each transmission line, such as DQ transmission line, provided by at least one driver. Ex. 1 at 258 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (describing DDR PHY features, such as write leveling and read training); Ex. 2 at 6137 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("Up to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16x5) per pin that can be read back via the MPC [Read DQ FIFO] command"); Ex. 9 at 165 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describing write DQ sequence).

29. On information and belief, the TI DDR Controller measures a skew for the

transmitted DQ bit patterns through the transmission line by training write boundaries of a data eye during write leveling. Ex. 1 at 258 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (listing DDR PHY features); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing DQS-DQ training – "After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ Delay) is needed."); Ex. 9 at 165 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describes the write DQ training sequence and states that "[t]he PHY receives the read data from the DRAM and compares it to the expected data. The PHY delays are to be adjusted as needed.").

30. On information and belief, the TI DDR Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("[a]fter writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with 'expect' data to see if further training (DQ delay) is needed"); Ex. 9 at 165 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describes the write DQ training sequence and states that "[t]he PHY receives the read data from the DRAM and compares it to the expected data."); Ex. 17 (External Memory Interfaces Intel Arria 10 FPGA IP User Guide) (describes write DQ ISI/crosstalk).

31. On information and belief, the TI DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate

for the above skew. Ex. 5 at 195, 200 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("[a]fter writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with 'expect' data to see if further training (DQ delay) is needed."); Ex. 9 at 165, 190 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describing write DQ training as an "operation to center the DQS in the write data eye at the DRAM" and further describing write DQ training sequence).

32. On information and belief, TI has induced, and continues to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused TI Products that incorporate the DDR Controller. TI had the knowledge of the '021 Patent, at least from CCO's September 18, 2019, correspondence to TI, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

33. On information and belief, TI has committed the foregoing infringing activities without a license.

34. On information and belief, TI's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

35. On information and belief, TI knew the '021 Patent existed, knew of its claims, and knew of TI's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '021 Patent.

COUNT II: INFRINGEMENT OF THE '234 PATENT

36. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

37. On information and belief, TI has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused TI Products.

38. For example, on information and belief, TI has infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused TI Products that include the DDR Controller, such as DDR3, DDR3L, DDR4, and LPDDR4 Memory Controller Systems, with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the DDR Controller. Ex. 1 at 257 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (DDR Subsystem description); Ex. 2 at 6117 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (memory controllers outline and description); Ex. 12 at 12, 39 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (industry standard compliance statement that the DDR3 controller is compliant with the JESD79-3E DDR3 SDRAM standard).

39. On information and belief, an exemplary DDR Controller reduces timing uncertainty in DDR3, DDR3L, DDR4 and LPDDR4 memory transmission including calibration using the Multi-Purpose Register (MPR), gate training, PHY initialization, read centering, write centering, and write leveling. Ex. 2 at 6133, 6137 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR PHY initialization flow); Ex. 1 at 258 (Texas Instruments, AM654x, AM652x Sitara processors,

Advance Information, Mar. 2019) (outlining DDR PHY features, including write leveling, read DQS gating training, DQ/DQS eye training, read and write data bit deskew, and similar); Ex. 11 at 115 (Texas Instruments, Keystone Architecture DDR3 Memory Controller, User's Guide, REV. Jan. 2015) (describing full leveling (auto leveling); Ex. 7 at 8, 37 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (outlining DDR4 MPR, write leveling, and DQ training); Ex. 16 (DDR4 SDRAM - Initialization, Training and Calibration) (describing MPR, DQ training with MPR); Ex. 16 (DDR4 SDRAM - Initialization, Training and Calibration) (describing read and write centering); Ex. 6 at 17, 48-51 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (outlining DDR3 MRS, MPR, and write leveling); Ex. 5 at 26, 190, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing write leveling, DQ bus training, RD DQ calibration, RD DQ calibration training, and DQS-DQ training for LPDDR4 architecture); Ex. 9 at 120 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describing frequency ratios across the DFI).

40. On information and belief, the DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of inputs and outputs. Ex. 2 at 6117 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR subsystem overview); Ex. 12 at 39 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (DDR3 memory system overview); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface) (outlining "write" training and DRAM interface).

41. On information and belief, the DDR Controller further comprises at least one receiving register for latching received DQ signals, each said receiving register having a plurality of inputs and outputs. Ex. 12 at 39 (Texas Instruments, Keystone II Architecture DDR3 Memory

Controller, User's Guide, REV. Mar. 2015) (DDR3 memory controller); Ex. 14 at 157 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB), Databook, Synopsys, Apr. 2012) (describing DQS gate training – "[r]ead DQS strobes from the DRAM are ordinarily gated by the PHY to suppress noise and correctly capture read data. Precise alignment of the gate to the read data is a prerequisite for proper reads."); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface) (DRAM interface outline); Ex. 15 at 13, 19-20 (Technical Note, High-Speed DRAM Controller Design, Micron) (circular FIFO and strobe delay outline).

42. On information and belief, the DDR Controller includes a main clock for generating a main clock signal, such as a DDR PLL. Ex. 2 at 3193, 3484, 6124 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR PLL and DDR subsystem integration); Ex. 12 at 15, 124 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (describing clock interface and local calibrated delay line register); Ex. 9 at 120 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0); Ex. 8 at 91 (DDR PHY Interface, Version 3.0) ("In a DDR memory subsystem, it may be advantageous to operate the PHY at a higher frequency than the MC. If the PHY operates at a multiple of the MC frequency, the PHY transfers data at a higher data rate relative to the DFI clock and the MC has the option to execute multiple commands in a single DFI clock cycle. The DFI is defined at the MC to PHY boundary and therefore operates in the clock frequency domain of the MC.").

43. On information and belief, the DDR Controller includes a reference clock, such as a DDR PHY clock, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training; said reference clock being associated with the main clock signal. Ex. 2 at 3484, 6124, 6926 (AM65x/DRA80xM Processors, Texas

Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR subsystem integration); Ex. 12 at 15, 124 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (describing DDR3 clock interface and local calibrated delay line register); Ex. 9 at 120 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (describing frequency ratios across the DFI); Ex. 15 at 12 (Technical Note, High-Speed DRAM Controller Design, Micron) (describing capture circuits); Ex. 9 at 16; Ex. 16 (DDR4 SDRAM - Initialization, Training and Calibration) (describing read centering in DDR3, DDR3L, and DDR4 memory controller systems); Ex. 6 at 48-51 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (DDR3 protocol example); Ex. 5 at 190, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing RD DQ calibration in LPDDR4 memory controller systems as well as DQS-DQ training).

44. On information and belief, the DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the CK signal at the destination, such as DATX8 delay lines aligning the timing of the DQS signals following write leveling, or DQ signals following write centering. Ex. 2 at 6137 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (wrute eveling adjustment and write eye centering); Ex. 14 at 34-35, 115, 117 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB) (describing local calibrated delay line register), Databook, Synopsys, Apr. 2012); Ex. 7 at 31-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (DDR4 write leveling); Ex. 11 at 115 (Texas Instruments, Keystone Architecture DDR3 Memory Controller, User's Guide, REV. Jan. 2015) (DDR3 auto leveling); Ex. 6 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (DDR3 write leveling); Ex. 5 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (DDR4 Mode register write-WR leveling

mode and write leveling procedure).

45. On information and belief, TI has induced, and continues to induce, infringement of the ’234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused TI Products that incorporate the DDR Controller. TI had the knowledge of the ’234 Patent, at least from CCO’s September 18, 2019, correspondence to TI, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

46. On information and belief, TI has committed the foregoing infringing activities without a license.

47. On information and belief, TI’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

48. On information and belief, TI knew the ’234 Patent existed, knew of its claims, and knew of TI’s infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’234 Patent.

COUNT III: INFRINGEMENT OF THE ’386 PATENT

49. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

50. On information and belief, TI has infringed the ’386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused TI Products.

51. For example, on information and belief, TI has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused TI Products, which include a DDR Controller, such as DDR3, DDR3L, DDR4, LPDDR2, LPDDR3, and LPDDR4 Memory Controller Systems, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks and compliant with the respective JEDEC standards. *See*, *e.g.*, Ex. 1 at 257 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (describing DDR subsystem and memory controllers); Ex. 2 at 6117-6118 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (key features include bank interleaving and scheduling based on bank openness); Ex. 12 at 15-16, 18, 23, 39 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (DDR3 memory controller interface and features, such as supporting DDR on address bus and having multiple high-priority tiers for sophisticated handling of priority requests); Ex. 19 at 1 (Texas Instruments, AM437x Sitara Processors, SPRS851E, REV. Jan. 2019) (DDR subsystem supports DDR3L, DDR4, and LPDDR4); Ex. 13 at 2 (AM5K2E0x Multicore Arm Keystone II System-on-Chip, Mar. 2015) (DDR3 memory controller device-specific information); Ex. 6 at 15-16 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

52. On information and belief, the DDR Controller comprises a queue comprising a plurality of request stations, wherein each of the plurality of memory transactions is stored in one

of the request stations and is addressed to one of the plurality of memory banks. Ex. 2 at 6128-6129, 6198, 6367-6368 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR subsystem mapping diagram); Ex. 12 at 23 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (DDR3 memory controller FIFO description, block diagram, and key DDR memory controller features, such as out-of-order command execution and read data return, multiple high-priority tiers for sophisticated handling of priority requests, and 512-byte write data buffer and 512-byte read data FIFO); Ex. 13 at 20 (AM5K2E0x Multicore Arm Keystone II System-on-Chip, Mar. 2015) (describing address alias prevention and address mapping); Ex. 6 at 33 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 145 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 80 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

53. On information and belief, the DDR Controller includes an arbiter, such as the memory controller IP block, coupled to each of the plurality of request stations, adapted to select any of the plurality of memory transactions. Ex. 12 at 23-24 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (DDR3 memory controller FIFO block diagram, describing DDR3 arbitration as well as key DDR memory controller features, such as out-of-order command execution and read data return); Ex. 2 at 6118, 6128 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (describing key features and coherency implications).

54. On information and belief, the DDR Controller's arbiter is configured to generate a plurality of bank readiness signals, such as following the submission of an activate command to

the DDR3, DDR4, LPDDR2, and LPDDR4 memory, each bank readiness signal indicating the readiness of one of the plurality of memory banks to accept a memory transaction, and, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. Ex. 12 at 19, 24 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (describing Write WR command, activation, key DDR memory controller features, and arbitration); Ex. 2 at 6118, 6138, 6176 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (TI processor features); Ex. 6 at 18, 55 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)) ("active" command); Ex. 7 at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) ("activate" command); Ex. 3 at 18, 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010) (same); Ex. 5 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (same).

55. On information and belief, TI has induced, and continues to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused TI Products that incorporate the DDR Controller. TI had the knowledge of the '386 Patent, at least from CCO's September 18, 2019, correspondence to TI, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

56. On information and belief, TI has committed the foregoing infringing activities

without a license.

57. On information and belief, TI's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

58. On information and belief, TI knew the '386 Patent existed, knew of its claims, and knew of TI infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT IV: INFRINGEMENT OF THE '069 PATENT

59. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

60. On information and belief, TI has infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused TI Products.

61. For example, on information and belief, TI has infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and verification of the JEDEC-compliant Accused TI Products, which include the DDR Controller, such as a DDR3, DDR3L, DDR4 and LPDDR4 memory controllers that automatically calibrate skew of DDR3, DDR3L, DDR4 and LPDDR4 DDRs. Ex. 1 at 257-258 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (DDR Subsystem); Ex. 2 at 6117, 6133 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR PHY features and DDR subsystem); Ex. 12 at 12, 30, 39, 86 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (DDR3 features and purpose of the peripheral); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface) (DRAM interface). Further, DDR3/3L/4 and

LPDDR4 DDR Subsystems include read/write training functions, such as gate training, read data eye training, and write data eye. Ex.10 at 18-19 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0).

62. On information and belief, TI's DDR Controller calibrates registers of the receiver, such as the DQ and DQS receiver registers, in relation to a reference clock edge. Ex. 2 at 6133, 6441, 6927 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (read DQS gate training); Ex. 12 at 86 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (same); Ex. 14 at 42, 157-158 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB), Databook, Synopsys, Apr. 2012) (PHY initialization flow, DQS gate training, and algorithm); Ex. 15 at 19-20 (Technical Note, High-Speed DRAM Controller Design, Micron); Ex. 9 at 144, 146-147 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (read training, gate training, and training operations in DFI training mode).

63. On information and belief, TI's DDR Controller calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver, such as PHY registers calibrated to receive deskewed DQS and DQ signals during read training. Ex. 2 at 6133, 6441 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (data training flow); Ex. 14 at 42, 163, 183 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB), Databook, Synopsys, Apr. 2012) (PHY initialization flow, data eye training, read training, and write eye centering algorithm); Ex. 9 at 146-147 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0); Ex. 16 (DDR4 SDRAM - Initialization, Training and Calibration) (data eye training and write centering).

64. On information and belief, TI's DDR Controller performs calibration by

measuring time offsets between different signals that form a communication channel, such as the skew between DQS and DQ signals, for a plurality of frequencies or data patterns. Ex. 14 at 163, 183, 312 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB), Databook, Synopsys, Apr. 2012) (DDLs used in the PHY blocks, data eye training, and write eye centering algorithm); Ex. 9 at 147 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (write DQ training, data eye training); Ex. 2 at 3176, 6117, 6475 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (PLL output clocks); Ex. 12 at 12 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (purpose of the peripheral and relevant features); Ex. 16 (DDR4 SDRAM - Initialization, Training and Calibration) (write centering).

65. On information and belief, TI's DDR Controller applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. Ex. 2 at 6556 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019); Ex. 12 at 124 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (Local calibrated delay line register); Ex. 14 at 117, 163 (DesignWare Cores DDR3/2 SDRAM PHY Utility Block (PUB), Databook, Synopsys, Apr. 2012) (local calibrated delay line register and data eye training); Ex. 9 at 164 (DDR PHY Interface, DFI 4.0 Specification, Version 4.0) (write DQ training).

66. On information and belief, TI has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the

Accused TI Products that incorporate the DDR Controller. TI had the knowledge of the '069 Patent, at least from CCO's September 18, 2019, correspondence to TI, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

67. On information and belief, TI has committed the foregoing infringing activities without a license.

68. On information and belief, TI's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

69. On information and belief, TI knew the '069 Patent existed, knew of its claims, and knew of TI infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT V: INFRINGEMENT OF THE '603 PATENT

70. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

71. On information and belief, TI has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused TI Products.

72. For example, on information and belief, TI's JEDEC-compliant DDR Controller infringes at least claim 16 of the '603 Patent by performing a method of using a multiplexer (including multicore shared memory controller (MSMC) and DDR subsystem) to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of JEDEC-compliant

Accused TI Products, which include the DDR Controller, such as a DDR3, DDR3L, DDR4, LPDDR2, and/or LPDDR4. Ex. 2 at 674, 6062, 6117, 7710 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (MSMC and DDR subsystem overview); Ex. 1 at 257 (Texas Instruments, AM654x, AM652x Sitara processors, Advance Information, Mar. 2019) (describing keystone architecture, DDR subsystem, MSMC, and DDR3 memory controller device-specific information); Ex. 6 at 15-16 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

73. On information and belief, the multiplexer used by the TI DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions and a multiplexer output for sending each of the plurality of memory transactions to the memory. Ex. 13 at 2, 117 (AM5K2E0x Multicore Arm Keystone II System-on-Chip, Mar. 2015) (KeyStone II architecture description); Ex. 2 at 6118, 6127 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (DDR subsystem, key features, such as bank interleaving and scheduling based on bank openness, and DDR3 memory controller device-specific information); Ex. 6 at 15-16 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

74. On information and belief, TI DDR Controller receives a plurality of memory transactions at the multiplexer inputs, wherein each memory transaction is addressed to a

corresponding memory bank. Ex. 2 at 6062, 6127, 6129, 7710 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (MSMC overview and DDR subsystem functional description); Ex. 13 at 4, 20 (AM5K2E0x Multicore Arm Keystone II System-on-Chip, Mar. 2015) (address mapping); Ex. 6 at 33 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

75. On information and belief, the TI DDR Controller associates a priority, such as Class of Service (CoS) with each received memory transaction. Ex. 2 at 6118, 6128 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (key features, such as priority based scheduling, scheduling based on bank openness, and CoS, as well as DDR subsystem CoS mapping); Ex. 12 at 24-25, 72 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (CoS and arbitration description).

76. On information and belief, the DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as a read or write request, wherein the plurality of bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. Ex. 2 at 6138 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (PUB commands); Ex. 12 at 18 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (Activation); Ex. 6 at 55 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of

Jesd79-3B, April 2008)) ("active" command); Ex. 3 at 18, 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010) (LPDDR2-SX: "Activate" command); Ex. 5 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("activate" command); Ex. 6 at 18 (JEDEC STANDARD DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)) (DDR3 SDRAM operations); Ex. 7 at 9 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (DDR4 SDRAM operations). For example, associated with the issuance of an Activate command that indicates the readiness of a memory bank to accept a memory transaction, such as a read or write request, TI's Memory Controllers generates a readiness signal, such as setting an internal variable, asserting a flag, changing one or more bits of a status register, or similar indication of bank readiness. The Active command, and the associated bank readiness signal, includes the selection of a bank and a row. The bank readiness signals are based on the bank/row of the requests and the input and output of the multiplexer discussed above. *Id.*

77. The TI DDR Controller sends each of the plurality of memory transactions to its corresponding memory banks via the multiplexer output based on the associated priorities and the bank readiness signals. Ex. 2 at 3779 (AM65x/DRA80xM Processors, Texas Instruments Family of Products, Technical Reference Manual, REV. Dec. 2019) (key features, such as priority based scheduling and scheduling based on bank openness); Ex. 12 at 24-25 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015) (arbitration and CoS).

78. On information and belief, TI DDR Controller prioritizes each memory transaction based on the memory transaction's position in a queue. Ex. 12 at 25 (Texas Instruments, Keystone II Architecture DDR3 Memory Controller, User's Guide, REV. Mar. 2015).

79. On information and belief, TI has induced, and continues to induce, infringement of the ’603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused TI Products that incorporate the DDR Controller. TI had the knowledge of the ’603 Patent, at least from CCO’s September 18, 2019, correspondence to TI, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

80. On information and belief, TI has committed the foregoing infringing activities without a license.

81. On information and belief, TI’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

82. On information and belief, TI knew the ’603 Patent existed, knew of its claims, and knew of TI’s infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against TI, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against TI on all counts;

B. Entry of judgment that TI has infringed the Patents-in-Suit;

C. Entry of judgment that TI’s infringement of the Patents-in-Suit has been willful;

D. An order permanently enjoining TI from infringing the Patents-in-Suit;

E. Award of compensatory damages adequate to compensate CCO for TI's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

F. Award of CCO's costs;

G. Pre-judgment and post-judgment interest on CCO's award; and

H. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Respectfully Submitted,

February 9, 2021

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