IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff, v. BROADCOM INC. AND BROADCOM CORP., Defendants.	Case No.: 6:21-cv-00136 **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO") hereby files Complaint for patent infringement against Defendants Broadcom Inc. and Broadcom Corp. (collectively, "Broadcom" or "Defendants") and alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. Broadcom Inc. is a corporation organized under the laws of the State of Delaware, and may be served with process through its registered agent, Corporation Service Company located at 251 Little Falls Drive, Wilmington, Delaware, 19808.

3. Broadcom Corp. is a corporation organized under the laws of the State of California, and may be served with process through its registered agent, Corporation Service Company d/b/a/ CSC-Lawyers Incorporating Service Company at 211 East 7th Street, Suite 620, Austin, Texas, 78701-3218.

4. On information and belief, Broadcom Corp. is a wholly owned subsidiary of Broadcom Inc. and is a part of the same corporate structure and distribution chain for the making, selling, offering to sell, selling, and using of the infringing devices in the United States, including in the State of Texas and this judicial district.

5. On information and belief, Defendants further share the same ownership, management, advertising platforms, facilities, distribution chains and platforms, infringing product lines, and products involving relevant technologies. Even Broadcom's website states, for example, that the "term 'Broadcom' refers to Broadcom Inc. and/or its subsidiaries." Ex. 24 (Broadcom.com website).

6. On information and belief, Defendants operate as a unitary business and are jointly and severally liable for the acts of patent infringement alleged herein.

JURISDICTION AND VENUE

7. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Broadcom of claims of U.S. Patent Nos. 6,480,021; 7,107,386; 7,278,069; and 7,426,603 ("the Patents-in-Suit").

8. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. Broadcom is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) Broadcom maintains several office locations in the State of Texas; (ii) Broadcom has done and continues to do business in the State of Texas; (iii) Defendants have committed and continue to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, selling, and/or importing infringing products into Texas, including by Internet sales and sales via retail and

wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing a least a portion of any other infringements alleged herein in Texas; and/or (iv) Broadcom places its products in the stream of commerce with intent or knowledge that those products would end up in Texas.

10. Venue is proper in this district under 28 U.S.C. § 1400(b) because (i) Broadcom has committed and continues to commit acts of patent infringement by, inter alia, offering for sale and selling, on their own and as part of a device, infringing Broadcom products; and (ii) has regular and established places of business in this district, including at 2901 Via Fortuna Drive, Austin, Texas 78746 and 810 Hesters Crossing Rd, Round Rock, TX 78681.

BACKGROUND

11. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

12. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

13. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

14. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

15. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew

Calibration."

16. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

17. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

18. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

19. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

20. By letter dated November 30, 2020, CCO notified Broadcom of the existence of the Patents-in-Suit, and of infringement of each of the Patents-in-Suit by Broadcom. CCO's letter identified exemplary infringing Broadcom products and an exemplary infringed claim for each of the Patents-in-Suit. CCO's November 30, 2020 letter invited Broadcom to hold a licensing discussion with CCO. Broadcom received the November 30, 2020 letter on December 10, 2020. As of the date of this Complaint, CCO has not received a response from Broadcom.

LICENSING

21. As of the time of this Complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, Qualcomm, Via Technologies, Rockchip, and Socionext.

COUNT I: INFRINGEMENT OF THE '021 PATENT

22. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

23. On information and belief, Broadcom has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States processors, microcontrollers, and Systems-on-Chip that include DDR3, DDR3L, DDR4, LPDDR2, and/or LPDDR4 memory controller systems ("DDR Controller") (collectively, "Accused Broadcom Products").

24. On information and belief, Broadcom has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the infringing Broadcom products, including during regular operation and during development, design, testing, and verification of the Accused Broadcom Products, in part because they operate with the guidance of the JEDEC Standard, which supports DQS-DQ training. *See* Ex. 1 (Broadcom BCM68650 SoC); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017). JEDEC LPDDR4 supports two modes of training, which include command-based FIFO WR/RD with user patters and an internal DQS clock-tree oscillator to determine the need for and the magnitude of required training. Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

25. On information and belief, Broadcom's SoC's further include a Cadence Denali DDR Memory Controller System, which supports at least LPDDR4 training with write-leveling and data-eye training as well as per-bit deskew on read and write datapath. *See* Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar.

2020); Ex. 15 (openwrt.org website page); Ex. 16 (anandtech.com website page). Cadence Denali DDR memory controller system includes per-bit deskew on read and write datapath as one of its key features. *See* Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020).

26. On information and belief, the Broadcom DDR Controllers continuously transmit data through each transmission line, such as DQ transmission line, provided by at least one driver. *See* Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020) (describing a memory controller interface); Ex. 10 at 35, 37 (Cadence Design IP PHY User's Manual, Nov. 2011) (describing a bidirectional data line to the memory devices); Ex. 13 at 67 (C. Kim et al., High-Bandwidth Memory Interface) (Outlining a DQ/DQS data transmission interface). Per LPDDR4 JEDEC standard that the Broadcom DDR controller complies with, "[u]p to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL x5) per pin that can be read back via the MPC [Read DQ FIFO] command." Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

27. On information and belief, Broadcom DDR Controllers measure a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC] [Read DQ FIFO] command and results compared with 'expect' data to see if further training (DQ delay) is needed."). Further, as stated above, the High-Speed DDR PHY in Broadcom DDR Controllers includes a per-bit deskew process on read and write datapath, which would naturally involve measuring a skew. Ex. 12 at 1 (Denali High-Speed DDR PHY IP for TSMC 22ULP,

Design IP DATASHEET, Cadence, Mar. 2020).

28. On information and belief, the Broadcom DDR Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. The JEDEC LPDDR4 standard, implemented in Broadcom DDR Controllers, encompasses guidance on recording, storing, and reading of information. Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017). Specifically, "[a]fter writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compares with 'expect' data to see if further training (DQ Delay) is needed." *Id*. See also Ex. 23 (Intel.cn website) (discussing Write DQ ISI/crosstalk).

29. On information and belief, the Broadcom DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. Ex. 5 at 195, 200 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017). (Outlining the process of generating and applying a correction to the timing position of a signal). On information and belief, Broadcom has induced, and continues to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, products that incorporate a DDR Controller.

30. Broadcom had the knowledge of the '021 Patent, at least from the time of receiving CCO's November 30, 2020 notice letter, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import

into the United States the infringing instrumentalities described above, including by providing DDR Controllers, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

31. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

32. On information and belief, Broadcom's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

33. On information and belief, Broadcom knew the '021 Patent existed, knew of its claims, and knew of Broadcom's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '021 Patent.

COUNT II: INFRINGEMENT OF THE '386 PATENT

34. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

35. On information and belief, Broadcom has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Broadcom Products.

36. For example, on information and belief, Broadcom has infringed at least claim 1 of the '386 Patent by making, using, selling, or offering for sale in the United States, or importing into the United States apparatus adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks, such as BCM5871X Series Processors. *See*, *e.g.*, Ex. 2 (BCM5871X Series Processors); Ex. 2 at 1-2 (BCM5871X Series Processors, BROADCOM STRATAGX, 2014); Ex. 1 (BCM68650 SoC); Ex. 3 (BCM2837 SoC); Ex. 15 (openwrt.org website page); Ex. 16 (anandtech.com website page); Ex. 11 at 5 (Cadence DDR Controller, Product Datasheet, Dec. 2017) (describing controller structure); Ex.

11 at 9, 10, 12, 14 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing controller structure, transaction processing, and paging policy); Ex. 18 (raspberrypi.org website page); Ex. 11 at 12, 17 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (discussing transaction processing); Ex. 6 at 15-16 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 4 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

37. On information and belief, the DDR Controller comprises a queue comprising a plurality of request stations, wherein each of the plurality of memory transactions is stored in one of the request stations and is addressed to one of the plurality of memory banks. Ex. 11 at 11-14, 20 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing the command queue, command selection logic, transaction processing, and address mapping); Ex. 6 at 33 (JEDEC Standard DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)); Ex. 7 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 4 at 145 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

38. On information and belief, the DDR Controller includes an arbiter, such as the memory controller IP block, coupled to each of the plurality of request stations, adapted to select any of the plurality of memory transactions. Ex. 11 at 12-13 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing command selection logic that determines the method of pulling commands from the queue for running).

39. On information and belief, the arbiter of the DDR Controller is configured to generate a plurality of bank readiness signals, such as following the submission of an activate

command to the DDR memory, each bank readiness signal indicating the readiness of one of the plurality of memory banks to accept a memory transaction, and, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *See* Ex. 11 at 12 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing command selection logic that determines the method of pulling commands from the queue for running and transaction processing logic that is used to process the commands in the command queue); Ex. 6 at 18, 55 (JEDEC Standard, DDR3 SDRAM JESD79-3C (Revision of Jesd79-3B, April 2008)) (describing ACTIVE command); Ex. 7 at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (same); Ex. 4 at 18, 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010) (same); Ex. 5 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (same).

40. On information and belief, Broadcom has induced, and continues to induce, infringement of the ’386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Broadcom Products that incorporate DDR Controllers. Broadcom had the knowledge of the ’386 Patent, at least from the time of receiving CCO’s November 30, 2020 notice letter, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

41. On information and belief, Broadcom has committed the foregoing infringing

activities without a license.

42. On information and belief, Broadcom's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

43. On information and belief, Broadcom knew the '386 Patent existed, knew of its claims, and knew of Broadcom infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT III: INFRINGEMENT OF THE '069 PATENT

44. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

45. On information and belief, Broadcom has infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Broadcom Products.

46. For example, on information and belief, Broadcom has infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, including during development, design, testing, and verification of the Accused Broadcom Products, which include a DDR Controller, such as a DDR3, DDR3L, DDR4 and LPDDR4 memory controller, that automatically calibrates skew, such as in the BCM5871X Series Processors. *See* Ex. 2 at 1-2 (BCM5871X Series Processors, BROADCOM STRATAGX, 2014); Ex. 1 (BCM68650 SoC); Ex. 15 (openwrt.org website page); Ex. 16 (anandtech.com website page); Ex. 11 at 5 (Cadence DDR Controller, Product Datasheet, Dec. 2017); Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020); Ex. 10 at 39, 51, 134 (Cadence Design IP PHY User's Manual, Nov. 2011); Ex. 13 at 67 (C. Kim et al., High-Bandwidth Memory Interface) (Outlining a DQ/DQS data transmission interface).

47. The DDR Controller initiates Write Leveling and Read Optimization via the PHY, which comprises a transmitter and the receiver. Ex. 11 at 31, 33 (Cadence DDR Controller, Product Datasheet, Dec. 2017); Ex. 12 at 1 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020); Ex 10 at 18-19 (DDR PHY Interface, DFI 4.0 Specification).

48. The DDR Controller calibrates registers of the receiver, such as DQ and DQS receiver registers, in relation to a reference clock edge. *See* Ex. 12 at 2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020); Ex. 10 at 37-39, 134 (Cadence Design IP PHY User's Manual, Nov. 2011) (describing the initialization procedure and outlining the timing block); Ex. 9 at 16, 147 (DDR PHY Interface, DFI 4.0 Specification) (describing that the frequency ratio depends on the relationship of the reference clocks for the MC and the PHY as well as gate training and data eye training).

49. The DDR Controller calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver, such as the registers calibrated to receive the samples of CK_t – CK_c during write leveling. Ex. 10 at 33, 39, 40-41, 139-141 (Cadence Design IP PHY User's Manual, Nov. 2011) (describing timing blocks, write leveling, and write path); Ex. 9 at 57, 146-147, 190 (DDR PHY Interface, DFI 4.0 Specification) (describing write leveling operations and read training as well as gate training and data eye training); Ex. 7 at 31 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (describing adjustable delay setting); Ex. 6 at 42 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (same); Ex. 5 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing mode register write-WR leveling mode and write leveling procedure); Ex. 12 at 2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020) (describing DDR PHY IP

architecture as well as data slice and address/control slices).

50. On information and belief, the DDR Controller's calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS_t-DQS-c and CK_t-CK_c signals, for a plurality of data patterns, such as DQS_t – DQS_c patterns with variable delays. Ex. 7 at 30-31, 33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (describing DQS_t – DQS_c delays by the controller to achieve a certain parameter); Ex. 6 at 40, 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (describing DQS – DQS# controller delays to achieve a certain parameter); Ex. 5 at 186, 244 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing mode register write-WR leveling mode and write leveling procedure as well as input clock stop and frequency change); Ex. 10 at 33; Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020) (describing data eye training and per-bit deskew on read and write datapath as key features); Ex. 9 at 190 (DDR PHY Interface, DFI 4.0 Specification) (describing write DQ training).

51. On information and belief, the DDR Controller applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See* Ex. 7 at 32-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012) (describing the controller locking DQS_t – DQS_c setting to achieve write leveling); Ex. 6 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (describing the controller locking DQS – DQS# delay setting to achieve write leveling); Ex. 5 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing mode register write-WR leveling mode and write leveling procedure); Ex. 12 at 1-2 (Denali High-Speed DDR PHY IP for TSMC 22ULP, Design IP DATASHEET, Cadence, Mar. 2020) (outlining deskewing); Ex. 10 at 39, 51 (Cadence

Design IP PHY User's Manual, Nov. 2011) (describing write path timing).

52. On information and belief, Broadcom has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Broadcom Products that incorporate the DDR Controller. Broadcom had the knowledge of the '069 Patent, at least from the time of receiving CCO's November 30, 2020 notice letter, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

53. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

54. On information and belief, Broadcom's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

55. On information and belief, Broadcom knew the '069 Patent existed, knew of its claims, and knew of Broadcom infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT IV: INFRINGEMENT OF THE '603 PATENT

56. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

57. On information and belief, Broadcom has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell,

selling in the United States or importing into the United States the Accused Broadcom Products.

58. For example, on information and belief, Broadcom has infringed at least claim 16 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of the Accused Broadcom Products, which include DDR Controllers, such as a DDR3, DDR3L, DDR4, LPDDR2, and LPDDR4. Ex. 2 at 1-2 (BCM5871X Series Processors, BROADCOM STRATAGX, 2014); Ex. 1 (BCM68650 SoC); Ex. 3 (BCM2837 SoC); Ex. 18 (raspberrypi.org website page); Ex. 15 (openwrt.org website page); Ex. 16 (anandtech.com website page).

59. On information and belief, the multiplexer used by the Broadcom DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions and a multiplexer output for sending each of the plurality of memory transactions to the memory. Ex. 19 at 16 (Cadence, FD-SOI: Ecosystem and IP Design) (outlining plurality of inputs); Ex. 11 at 12; Ex. 6 at 15 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 4 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 9 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

60. On information and belief, the Broadcom DDR Controller receives a plurality of memory transactions at the multiplexer inputs, wherein each memory transaction is addressed to a corresponding memory bank, in accordance with the respective JEDEC standards for each DDR Controller. Ex. 11 at 12, 14 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017); Ex. 6 at 33 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 4 at 145; Ex. 5 at 246 (JEDEC

Standard, LPDDR4, JESD209-4B, Feb. 2017).

61. On information and belief, the Broadcom DDR Controller associates a priority with each received memory transaction. Ex. 11 at 9, 12, 20 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing DDR controller structure including command selection logic and placement logic).

62. On information and belief, the DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, wherein the plurality of bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output, in accordance with the respective JEDEC standards for each DDR Controller. *See* Ex. 11 at 12 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing command selection logic and transaction processing); Ex. 6 at 18, 55 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008) (describing the ACTIVATE command); Ex. 7 at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 4 at 18, 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 5 at 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) (describing the ACTIVATE command).

63. On information and belief, the Broadcom DDR Controller sends each of the plurality of memory transactions to its corresponding memory banks via the multiplexer output based on the associated priorities and the bank readiness signals. Ex. 11 at 12 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (describing command selection logic and transaction processing); Ex. 20 (community.cadence.com website page); Ex. 21 at 2 (Denali Controller IP for DDR); Ex. 22 (chipestimate.com website page).

64. On information and belief, the Broadcom DDR Controller prioritizes each

memory transaction based on the memory transaction's position in a queue. Ex. 11 at 12 (Cadence Denali DDR Controller, Product Datasheet, Dec. 2017) (command selection logic).

65. On information and belief, Broadcom has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, Accused Broadcom Products that incorporate the DDR Controller. Broadcom had the knowledge of the '603 Patent, at least from the time of receiving CCO's November 30, 2020, notice letter, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

66. On information and belief, Broadcom has committed the foregoing infringing activities without a license.

67. On information and belief, Broadcom's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

68. On information and belief, Broadcom knew the '603 Patent existed, knew of its claims, and knew of Broadcom's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Broadcom, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against Broadcom on all counts;

B. Entry of judgment that Broadcom has infringed the Patents-in-Suit;

C. Entry of judgment that Broadcom's infringement of the Patents-in-Suit has been willful;

D. An order permanently enjoining Broadcom from infringing the Patents-in-Suit;

E. Award of compensatory damages adequate to compensate CCO for Broadcom's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

F. Award of CCO's costs;

G. Pre-judgment and post-judgment interest on CCO's award; and

H. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Respectfully Submitted,

February 9, 2021

By: /s/ Raymond W. Mort, III

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