

**IN THE UNITED STATES DISTRICT COURT
FOR THE MIDDLE DISTRICT OF FLORIDA**

BELL SEMICONDUCTOR, LLC,

Plaintiff,

v.

RENESAS ELECTRONICS CORPORATION,
RENESAS ELECTRONICS AMERICA INC.

Defendants.

Civil Action No. 6:19-cv-02196-WWB-GJK

JURY TRIAL DEMANDED

INJUNCTIVE RELIEF REQUESTED

BELL SEMICONDUCTOR, LLC'S
THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Bell Semiconductor, LLC (“Bell Semic”) as and for its complaint against Renesas Electronics Corporation and Renesas Electronics America Inc. (collectively, “Renesas” or “Defendant”) alleges as follows:

INTRODUCTION

1. Bell Semic is a technology and intellectual property licensing company. Bell Semic’s patent portfolio comprises over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world’s leading semiconductor technology innovators, including AT&T Bell Laboratories, Lucent Technologies (Lucent), Agere Systems (Agere), LSI Logic and LSI Corporation (LSI). The portfolio reflects expertise developed at the various R&D laboratories and manufacturing locations of these companies around the world. The technology created, developed, and patented at those companies underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables,

digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors and wireless connectors.

2. Bell Semic was formed in 2017 to manage this portfolio of semiconductor-related intellectual property acquired from Broadcom and assigned to Bell Semic. Several Bell Semic executives previously served as engineers and in leadership roles within the intellectual property departments of Lucent, Agere, LSI, Avago Technologies (Avago), and Broadcom. As a result, Bell Semic executives were personally involved in creating, patenting, and licensing various aspects of the portfolio even before Broadcom assigned it to Bell Semic, including:

- Bell Semic's Chief Executive Officer and Board Member, Mr. John Veschi, served as General Manager of the Intellectual Property business at LSI, had similar responsibilities at Agere, and began his in-house intellectual property experience with the formation of Lucent.
- Bell Semic's President and General Counsel, Mr. Chad Hilyard, served as Managing IP Counsel and in other roles at LSI and Agere, where he was involved in licensing many of the patents in the portfolio now assigned to Bell Semic;
- Bell Semic's Chief Technology Officer, Dr. Sailesh Merchant was a Fellow at Broadcom, Avago, and LSI Corporation; a Distinguished Engineer at LSI Corporation; and a Distinguished Member of the Technical Staff of Agere and Lucent. Dr. Merchant is also a Senior Member of the IEEE and an inventor on more than 250 worldwide patents—including many of the patents in Bell Semic's portfolio—and one of the patents asserted in this Complaint;
- Bell Semic's Senior Director for IP, Mr. Kouros Azimi, served as a Member of the Technical Staff at AT&T Bell Labs, Lucent, and Agere; Director of Intellectual Property at

Avago/Broadcom, and a Patent Engineer and Director of Patent Development at LSI/Avago Technologies.

3. Renesas has infringed and continues to infringe Bell Semic's patents by making, using, selling, offering for sale, and/or importing products (including importing products made by a patented process) throughout the United States, including within this District. Renesas's customers incorporate those products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States and within this District. Such downstream products include, but are not limited to, a robust family of microcontrollers and system-on-chip (SoC) processors, embedded devices for the Internet of Things, power management SoC processors, sensors used in automotive and industrial applications, and a wide array of analog and power devices, among others. Examples of an infringing Renesas devices used in such downstream products include Renesas's Renesas D813301 GPU that was incorporated as the graphics processor in the Nintendo Wii; Renesas's uPD720202 controller used in USB 3.0 applications; and Renesas's TW8836 highly integrated LCD video processor used in automotive applications to display rear camera video.

4. Bell Semic and prior assignees of the Bell Semic portfolio have notified Renesas of its infringement in writing numerous times—but Renesas has not licensed its intellectual property. Instead, Renesas has continued to infringe, and thus its infringement is and has been willful under the Patent Act.

NATURE OF THE CASE

5. This action arises under 35 U.S.C. § 271 for Renesas's infringement of Bell Semic's United States Patent Nos. 6,068,879 ("the Pasch Patent"); 6,153,543 ("the Cheshire

Patent”); 6,727,588 (“the Abdelgadir Patent”); and 6,879,046 (“the Gibson”) (collectively, Bell Semic’s “Asserted Patents”).

PARTIES

6. Bell Semiconductor, LLC is a Delaware limited liability company with a principal place of business of One West Broad Street, Suite 901, Bethlehem, PA 18018.

7. On information and belief, Defendant Renesas Electronics Corporation (“REC”) is a corporation organized under the laws of Japan, having a principal place of business at Toyusa Foresia, 3-2-24 Toyusa, Koto-ku, Tokyo 135-0061, Japan.

8. On information and belief, Defendant Renesas Electronics America Inc. (“REA”) is a corporation organized under the laws of the State of California, having a West Coast Headquarters and Sales Center at 2801 Scott Boulevard, Santa Clara, CA 95050, and an East Coast Headquarters and Sales Center at 1650 Robert J Conlan Blvd NE, Palm Bay, FL 32905. REA is registered to do business in Florida and may be served through its registered agent CT Corporation System, 1200 South Pine Island Road, Plantation, FL 33324.

9. On information and belief, REA is a wholly-owned subsidiary of REC and is responsible for domestic sales, offers for sale, importation, marketing, and support of REC products in the United States.

JURISDICTION AND VENUE

10. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

11. This Court has personal jurisdiction over REC. REC has conducted and does conduct business within the State of Florida. REC has purposefully and voluntarily availed itself

of the privileges of conducting business in the United States, in the State of Florida, and in the Middle District of Florida by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in the Middle District of Florida.

12. This Court has personal jurisdiction over REA. REA has conducted and does conduct business within the State of Florida. REA has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Florida, and in the Middle District of Florida by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in the Middle District of Florida, by registering to do business in Florida and maintaining an agent for service of process in Florida, and by having a physical place of business in this District in Palm Bay, Florida, which it refers to as its East Coast Headquarters and Sales Center.

13. REC and REA have authorized retailers and distributors for the accused products in this judicial district, and Plaintiff's causes of action arise directly from REC's and REA's business contacts and other activities in the State of Florida and the Middle District of Florida.

14. REC and REA have derived substantial revenues from their infringing acts occurring within the State of Florida and within this District.

15. Venue is proper as to REC under 28 U.S.C. § 1391(c)(3) in that it is not a resident of the United States and may, therefore, be sued in any judicial district. *Brunette Mach. Works, Ltd. v. Kockum Indus., Inc.*, 406 U.S. 706, 714 (1972).

16. Venue is proper as to REA under 28 U.S.C. § 1400(b) because REA has committed acts of infringement in this District and has a regular and established physical

property and place of business within this District. *TC Heartland LLC v. Kraft Foods Grp. Brands LLC*, 137 S. Ct. 1514, 1521 (2017). Specifically, REA has represented that its East Coast Headquarters and Sales Center is within this District—namely, in Palm Bay, Florida.

17. Joinder of REA and REC is proper because they are related parties who are either jointly and severally liable for infringement, or who make, use, sell, offer for sale, or import the same or similar accused products that practice the same Patents-in-Suit. Further, upon information and belief, REC and REA use the same underlying hardware and/or software in their infringing products and therefore the factual question of infringement will substantially overlap between REC and REA. Further, Plaintiff anticipates that there will be substantial overlap during the discovery process. Moreover, REC controls and directs the actions of REA, and therefore directs REA to infringe and itself infringes the Asserted Patents.

18. REC exercises control over REA, and acts collectively with REA, both having committed acts of infringement in this District giving rise to this action and do business in this District, including making sales and/or providing service and support for their respective customers in this District. REC and REA purposefully and voluntarily sold one or more of their infringing products with the expectation that they would be purchased by consumers in this District. These infringing products have been and continue to be purchased by consumers in this District. REC and REA have committed acts of patent infringement within the United States, the State of Florida, and the Middle District of Florida.

19. Many of the inventions described in the patents asserted in this action, including the Chesire Patent, Abdelgadir Patent, and Gibson Patent were developed, at least in part, in this District in the late 1990s and early 2000s at the Orlando facility of Lucent Technologies (and subsequently Agere Systems after being spun out of Lucent). On information and belief, one or

more of the named inventors of the asserted patents still live in the Orlando area within this District.

BELL SEMIC'S ASSERTED PATENTS

1) U.S. Patent No. 6,068,879 (Pasch)

20. Bell Semic is the owner by assignment of U.S. Patent No. 6,068,879 (the “Pasch Patent”), owns all right, title, and interest in the Pasch Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Pasch Patent is entitled “Use of Corrosion Inhibiting Compounds to Inhibit Corrosion of Metal Plugs in Chemical-Mechanical Polishing.” A true and correct copy of the ’879 Patent is attached as **Exhibit 1**.

21. The inventor of the Pasch Patent is Nicholas F. Pasch.

22. The application for the Pasch Patent was filed on August 26, 1997, and it issued on May 30, 2000.

23. As of March 2020, the Pasch Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 68 patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Samsung, Texas Instruments, Intel, and Applied Materials, Inc.

2) U.S. Patent No. 6,153,543 (Chesire et al.)

24. Bell Semic is the owner by assignment of U.S. Patent No. 6,153,543 (the “Chesire Patent”), owns all right, title, and interest in the Chesire Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Chesire Patent is entitled “High Density Plasma Passivation Layer and Method of Application.” A true and correct copy of the Chesire Patent is attached as **Exhibit 2**.

25. The inventors of the Chesire Patent are Daniel P. Chesire, Edward P. Martin, Jr., Leonard J. Olmer, Barbara D. Kotzias, and Rafael N. Barba.

26. As of March 2020, the Chesire Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 23 issued patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Cypress Semiconductor Corp., Hynix Semiconductor Inc., and Sandisk 3D LLC.

3) U.S. Patent No. 6,727,588 (Abdelgadir et al.)

27. Bell Semic is the owner by assignment of U.S. Patent No. 6,727,588 (the “Abdelgadir Patent”), owns all right, title, and interest in the Abdelgadir Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Abdelgadir Patent is entitled “Diffusion Preventing Barrier Layer in Integrated Circuit Inter-Metal Layer Dielectrics.” A true and correct copy of the Abdelgadir Patent is attached as **Exhibit 3**.

28. The inventors of the Abdelgadir Patent are Mahjoub Ali Abdelgadir, Nace Layadi, Dr. Merchant, Vivek Saxena, and Pei H. Yih.

29. The application for the Abdelgadir Patent was filed on August 19, 1999, and it issued as a patent on April 27, 2004.

30. As of March 2020, the Abdelgadir Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 6 patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Samsung and IBM.

4) U.S. Patent No. 6,879,046 (Gibson et al.)

31. Bell Semic is the owner by assignment of U.S. Patent No. 6,879,046 (the “Gibson Patent”), owns all right, title, and interest in the Gibson Patent; and holds the right to sue and recover damages for infringement thereof, including past infringement. The Gibson Patent is entitled “Split Barrier Layer Including Nitrogen-Containing Portion and Oxygen Containing Portion.” A true and correct copy of the Gibson Patent is attached as **Exhibit 4**.

32. The inventors of the Gibson patent are Gerald W. Gibson, Jr., Scott Jessen, Steven Alan Lytle, Kurt George Steiner, and Susan Clay Vitkavage.

33. The application for the Gibson Patent was filed on January 2, 2002, and it claims priority to Provisional Application No. 60/301,295, filed on June 28, 2001. The Gibson Patent issued on April 12, 2005.

34. As of March 2020, the Gibson Patent has been cited as pertinent prior art by a USPTO examiner or an applicant during the prosecution of at least 10 patents and published applications—including during the prosecution of patent applications filed by leading technology companies such as Taiwan Semiconductor Manufacturing Co., Micron Technology, and Panasonic Corp.

FACTUAL BACKGROUND

35. Bell Semic incorporates the preceding paragraphs as if fully set forth herein.

36. On June 1, 2002, Lucent, having its roots with Bell Laboratories and AT&T Corporation, spun off its microelectronics business as Agere. Agere later merged with LSI Logic forming LSI Corporation in 2007, which was in turn acquired by Avago in 2014. In 2016, Avago purchased Broadcom and assumed its name to become the current Broadcom Inc. In 2017, Broadcom assigned a patent portfolio containing over 1,900 worldwide patents and applications,

approximately 1,500 of which are active U.S. patents, to Bell Semic that included patents originally assigned or issued to Bell Labs, Lucent, Agere, LSI Logic, and LSI.

37. Portions of the Bell Semic portfolio are presently licensed and/or were previously licensed to leading technology companies by Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*See supra* ¶ 2.) Portions of the Bell Semic portfolio were also invented and co-invented by other Bell Semic senior executives while they were working at Lucent, Agere, LSI, Avago, and/or Broadcom. (*Id.*)

38. Bell Semic's Asserted Patents arise out of the research, conception, creation, and design of innovative technology developed by leading high-technology companies, including LSI Logic, Agere, and LSI Corporation. Prior to their ultimate acquisition by Avago (now Broadcom), those companies were pioneers of innovative semiconductor technology—and made substantial investments into researching, inventing, creating, and manufacturing cutting-edge semiconductor technology. Bell Semic's Asserted Patents are directed to this inventive technology relating to semiconductors, integrated circuits, and related products.

39. Renesas infringes and has infringed by making, selling, offering to sell, using, and/or importing products (including importing products made by a patented process) throughout the United States. Moreover, Renesas works closely with its customers, foundry suppliers, distributors, OEMs, or other third parties to make, use, sell, offer to sell, and/or import semiconductor devices, integrated circuits, and related products. Renesas tailors its manufacturing process for its customers and designs its products to be integrated into downstream products. In addition to its own manufacturing, Renesas's affirmative acts in furtherance of the manufacture, use, sale, offer to sell, and importation of its products in and/or into the United States by itself and others further include, without limitation, any one or a

combination of: (i) designing specifications for manufacture of Renesas's products; (ii) collaborating on, encouraging, and/or funding the development of processes for the manufacture of Renesas's products; (iii) soliciting and/or sourcing the manufacture of Renesas's products; (iv) licensing, developing, and/or transferring technology and know-how to enable the manufacture of their products; (v) enabling and encouraging the use, sale, or importation of their products in the United States; and (vi) advertising its products and/or downstream products incorporating them in the United States.

40. Renesas provides marketing and/or technical support services for its products from its facilities in the United States. For example, Renesas maintains a website that advertises its products, including identifying the applications for which they can be used and providing specifications for their products. (*See, e.g.,* <https://www.renesas.com/us/en/>.) Renesas's publicly-available website also contains user manuals, product documentation, and other materials related to its products. (*Id.*) For example, Renesas's website contains reference designs (<https://www.renesas.com/us/en/products/software-tools/boards-and-kits/reference-designs.html>), spanning analog products, power management products, and microprocessor and microcontrollers; complimentary design review services such as EDA schematic symbols, PCB footprints, and simulation models in industry-standard formats to help shorten development time (<https://www.renesas.com/us/en/support/technical-resources/eda-data.html>); and robust customer support through Renesas's online support platforms including Renesas Rulz forum and Renesas Synergy Platform (<https://www.renesas.com/us/en/support/contact.html>). By way of example only, Renesas maintains a customer support system that "ensur[es] customer's confidence through provision of easy-to-understand documents and technical information, engineering support activities and quality support for customer":

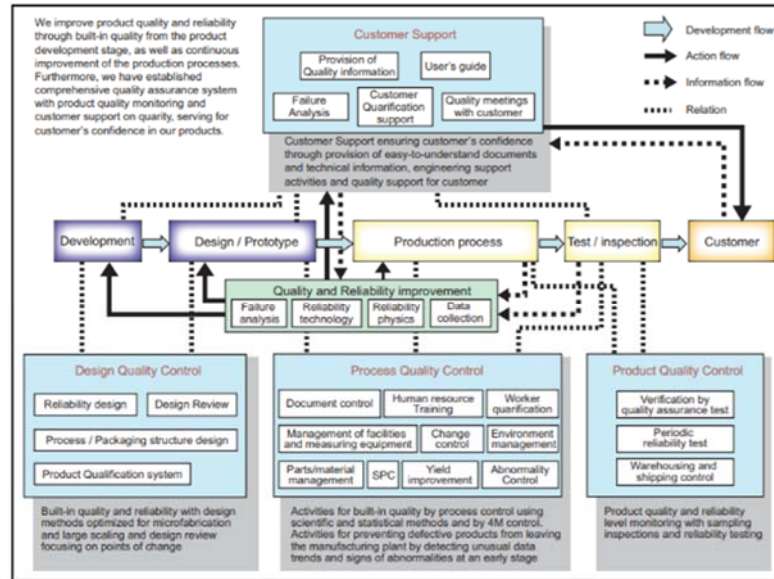


Figure 1.2 Renesas Quality Assurance System for Semiconductor Devices

See <https://www.renesas.com/us/en/doc/products/others/r51zz0001ej0250.pdf> (last accessed March 4, 2020).

41. In addition to these resources, Renesas also provides numerous support resources for the customers of its semiconductor devices in addition to user manuals and datasheets, including through Renesas's "Renesas Academy" (formerly known as Renesas E-Learning) (<https://academy.renesas.com/>); events and webinars for its products (<https://www.renesas.com/us/en/support/training/events.html>); "Engineer School" (<https://www.renesas.com/us/en/support/technical-resources/engineer-school.html>); access to published books covering Renesas technology and products (<https://www.renesas.com/us/en/support/technical-resources/books.html>); and support videos (<https://www.renesas.com/us/en/support/videos.html>). Moreover, Renesas promotes the incorporation of its products through the development of Partner programs, such as the Renesas Alliance Partners program, Renesas R-Car Consortium, and Renesas R-IN Consortium, among others.

RENESAS'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

42. Before filing this lawsuit, Bell Semic and/or the prior assignees of the Bell Semic portfolio contacted Renesas to initiate patent licensing discussions:

- a. On July 10, 2015, Jim Zajko, Senior IP Licensing Manager of Avago Technologies, a prior assignee of the Bell Semic patents, sent a letter to Taylor Davis, Chief Administrative Officer, General Counsel and Secretary, of REA to initiate patent licensing discussions and identified several Asserted Patents as being infringed based on Avago's reverse engineering analysis of Renesas's Cu Technology (copper-based devices where an interconnect is made of copper) and Technology Nodes, and identified exemplary Renesas products infringing the Pasch Patent. Among others, this letter identified the following exemplary Renesas products as infringing this patent:

Patents Infringed	Exemplary Products
Pasch Patent	Renesas uPD720202 USB controller Renesas RA877240D500BGV Renesas R5S72641W144FPU MCU

- b. On July 13, 2015, John Jeter, Senior Corporate Counsel at REA, acknowledged receipt of Avago's July 10, 2015 letter, stating that REA was in the process of reviewing the information and assertions made in the July 10, 2015 letter.
- c. On information and belief, on September 14, 2015, Avago sent a letter to Renesas including claim charts demonstrating how exemplary Renesas products infringed the Pasch, Chesire, Abdelgadir, and Gibson Patents. Among others, this letter identified the following exemplary Renesas products as infringing these patents:

Patents Infringed	Exemplary Infringing Products
Pasch Patent	Renesas D813301 GPU

	Renesas RA877240D500BGV Renesas uPD720202 USB Controller Renesas R5S72641W144FPU MCU
Chesire Patent	Renesas R5F104PJA MCU
Abdelgadir Patent	Renesas UPD9975 PMIC
Gibson Patent	Renesas R8A77240D500BGV

- d. On September 28, 2015, Mr. Zajko and four other Avago representatives, including Dr. Merchant, met in Tokyo, Japan with Renesas, and presented claim charts showing Renesas's infringement of the Pasch, Chesire, Abdelgadir, and Gibson Patents by the above identified Renesas products.
- e. Mr. Zajko and Dr. Merchant met with Renesas again, on behalf of Broadcom after Avago's acquisition of Broadcom, on February 18, 2016; April 21, 2016; and February 15, 2017 in Tokyo, Japan to continue the discussions.
- f. On November 30, 2017, Mr. Hilyard, sent a letter to Renesas's headquarters addressed to Mr. Masaki Yabe (Renesas's Section Manager of the IP Licensing Department) to inform Renesas that Bell Semic "acquired all of the semiconductor-related patent assets previously owned by Agere Systems Inc. and LSI Corporation . . . [t]his portfolio includes patents originally assigned to Bell Labs and Lucent Technologies, as well as those assigned to Agere, LSI and Avago Corporation. We were also assigned some select semiconductor assets that were originally assigned to Broadcom Corporation . . . By way of background, I was previously part of the Lucent/Agere/LSI licensing team. At Bell Semiconductor, I am joined by other former members of the Lucent/Agere/LSI licensing team, including John Veschi and Sailesh Merchant. We are very familiar

with this pioneering patent portfolio, and have licensed this portfolio to many of the world’s leading semiconductor companies. Our goal is [to] build upon the amicable licensing history between Lucent/Agere/LSI and Renesas’s predecessors – NEC, Hitachi and Mitsubishi – as well as the similar relationships we previously established throughout the semiconductor industry.” Bell Semic’s November 30, 2017 letter to Renesas also offered to meet with Renesas in Asia between December 11, 2017 and December 22, 2017, to “discuss the portfolio” and “a path forward to put in place a license agreement” to Bell Semic’s Patent portfolio.

- g. On December 21, 2017, Mr. Hilyard and Dr. Merchant met with Renesas to again discuss patent licensing and put Renesas on notice of their infringing Cu Technology and Technology Nodes and exemplary Renesas products from the Cu Technology and Technology Nodes infringing the Pasch, Chesire, Abdelgadir, and Gibson Asserted Patents:

Reenes Technology	Reenes Technology Node	Reenes Product Code	6,068,879 Pasch	6,153,543 Chesire	6,281,129 Easter	6,403,415 Alers	6,548,854 Kizilyalli	6727588 Abdelgadir	6,794,694 Diodato	6,879,046 Gibson	6,083,271 Morgan	6,292,086 Chu	6,675,139 Jetton	7,253,497 Bhatt	6,222,863 Derkits
High K Metal Gate							X								
MRAM						X									
28nm CMOS									X						
Cu Technology	45nm CMOS	D813301	X		X										
	65nm CMOS	R8A77240D500BGV	X		X					X					
	90nm CMOS	uPD720202	X		X										
	0.13µm CMOS	R5S72641W144FPU	X		X										
Al Technology	0.11µm CMOS	RMLV0408E			X										
	0.15µm CMOS	UPD9975			X			X							
	0.22µm CMOS	R5F104PJA		X	X										
	0.25µm CMOS	UC KTR504KM16			X										
Design Practice	45nm CMOS									X		X			
RF SOC	90nm CMOS									X	X		X		
FP Laser Diode	1310 nm InGaAsP	NX7338BF-AA													X

- h. On March 16, 2018, the parties again met and continued their discussions on patent licensing. Bell Semic again identified Renesas's infringing Cu Technology and Technology Nodes and exemplary Renesas products from the Cu Technology and Technology Nodes infringing the Pasch, Chesire, Abdelgadir, and Gibson Asserted Patents.
- i. On August 9, 2018, Mr. Hilyard sent multiple emails to Renesas requesting another in-person meeting with Renesas in Tokyo, Japan, to discuss "additional research" on its patent portfolio and Renesas products, and "additional [Bell Semic] patents that are infringed by Renesas products." Mr. Hilyard proposed two dates in August 2018, but Renesas did not respond.
- j. On August 14, 2018, Mr. Hilyard sent a follow-up email to Renesas on August 14, 2018 to confirm whether Renesas was available to meet on August 22, 2018, but Renesas did not respond until two days before the proposed meeting date.
- k. In September 2018, Mr. Hilyard again sent multiple emails attempting to schedule another in-person meeting with Renesas in Japan, but Renesas again waited until the last minute, the afternoon before the proposed meeting date, to respond that they were unavailable.
- l. On March 21, 2019, Hilyard again wrote to Renesas inviting Renesas to re-engage in licensing discussions. In that correspondence, Mr. Hilyard disclosed Bell Semic's continued reverse engineering efforts to identify more Renesas products that infringe Bell Semic's patents: "Over the last several months, we have continued to acquire Renesas products and conduct reverse engineering to expand upon the claim charts and infringement positions Broadcom previously presented

to you. Broadcom's previous assertions and our recent analysis of Renesas products evidences that Renesas continues to make, use, sell, and/or offer for sale products that infringe one or more of Bell Semic's patents. The attached document shows (i) patents Broadcom previously asserted against Renesas products, and (ii) additional products Bell Semic has recently reverse engineered, and exemplary patents those products and processing nodes infringe. Indeed, our new reverse engineering analysis has identified an additional 26 claim charts for patents previously presented to Renesas, and 4 entirely new patents not previously identified to Renesas. Of course, as we have mentioned before, the identified patents are exemplary, and Renesas products most likely infringe other patents in the larger Bell Semic portfolio." In the March 21, 2019 correspondence, Mr. Hilyard again invited Renesas to enter into a license agreement and proposed to meet with Renesas in Tokyo, Japan in early April: "We believe it would be beneficial to both parties to continue our patent licensing discussions. Accordingly, we will be in Japan April 3 – 5 and would like to meet with Renesas during that time. Please let me know if you are available to meet while we are there." Attached with Bell Semic's March 21, 2019 correspondence was a summary infringement chart, putting Renesas on notice of Renesas's infringing Cu Technology and Technology Nodes and exemplary Renesas products infringing the Asserted Patents as follows:

Exemplary List of Bell Semic's Patents Infringed by Renesas

Patent Category	Renesas Technology	Renesas Technology Node	Renesas Product Code	6,068,879 Pasch	6,153,543 Cheshire	6,232,658 Catabay	6,281,129 Easter	6,403,415 Ailers	6,548,854 Kozhyallil	6,772,588 Abdeganfir	6,794,694 Diodato	6,879,046 Gibson	6,083,271 Morgan	6,292,086 Chu	6,675,139 Jetton	7,253,497 Bhatt	6,222,863 Deritis	6,960,836 Bachman	6,683,382 Cwynar	6,140,710 Greenberg	6,459,049 Miller	
Semiconductor Processing	High K Metal Gate								X													
	MRAM							X														
	28nm CMOS										X											
	Cu Technology	40 nm CMOS	R75721011VCBG		X	X		X														
		40 nm CMOS	R7F7010233AFP		X	X		X														
		45nm CMOS	D813301		X			X														
		65nm CMOS	R8A77240D500BGV		X			X					X									
		90nm CMOS	uPD720202		X			X														
		90nm CMOS	R5572620W144FPU		X			X				X										
		90nm CMOS	R8A778008NBGV		X			X													X	
		0.13µm CMOS	R5572641W144FPU		X			X														
		0.11µm CMOS	RMLV0408E					X														
		0.11µm CMOS	R5F10AGLKNA			X		X														
	Al Technology	0.11µm CMOS	R5F10CLDJFB			X		X														
		0.11µm CMOS	R5F109ACKSP			X		X														
		0.15µm CMOS	UPD9975					X			X											
		0.15µm CMOS	TW8836-BB2-CR			X	X	X			X										X	
		0.15µm CMOS	UPD70F3353GC					X													X	
		0.15µm CMOS	UPD70F3335GC					X			X										X	
		0.15µm CMOS	UPD70F3371M2GBA1					X			X										X	
0.22µm CMOS		R5F104PJA			X		X															
0.25µm CMOS		JIC-KTR504KM15					X															
Semiconductor Design		Design Practice	45nm CMOS											X		X						
	RF SOC	90nm CMOS											X	X		X						
Optoelectronics	FP Laser Diode	1310 nm InGaAsP															X					
Packaging			R8A77450A01																	X	X	

X December 2017 meeting
 X March 2019

m. After Renesas did not respond to Bell Semic's March 21, 2019 correspondence, Mr. Hilyard sent another email to Renesas on April 26, 2019 with this same detailed chart, requesting another meeting with Renesas. Renesas did not respond.

43. As a result, Bell Semic was thus left with no other choice but to seek relief from this Court by filing its Original Complaint in this matter.

44. Since Bell Semic filed its Original Complaint, Renesas contacted and met with Bell Semic in December 2019 to discuss its infringement of the Asserted Patents. However, meaningful discussions have not progressed, and instead, Renesas continues to knowingly and willfully infringe Bell Semic's Asserted Patents directly, contributorily, and by inducement—to obtain the substantial benefits of those inventions without a license from Bell Semic.

COUNT 1

Willful Infringement of U.S. Patent No. 6,068,879 (Pasch Patent)

45. Plaintiff re-alleges and incorporates by reference the allegations in Paragraphs 1-23 and 35-44 as if fully set forth herein.

46. The Pasch Patent is generally related to a process of inhibiting a corrosion of metal plugs formed in integrated circuits. The corrosion inhibiting process includes providing a partially fabricated integrated circuit surface including the metal plugs on a polishing pad to carry out chemical-mechanical polishing, introducing slurry including a corrosion inhibiting compound on the polishing pad in sufficient concentration to inhibit corrosion of the metal plugs of the partially fabricated integrated circuit surface, and polishing the partially fabricated integrated circuit surface. (*See Pasch Patent, Abstract.*)

47. During the chemical mechanical polishing (CMP) process, a chemical containing slurry interacts with the facing wafer layer, and an abrasive that physically removes that layer is flowed between the wafer and the polishing pad or on the pad near the wafer to planarize various wafer layers such as dielectric and metallization layers. However, during the CMP process, the slurry can chemically attack and open seams in the metal plugs, which are then corroded by other processing chemicals in the post-CMP cleaning steps, making the device susceptible to catastrophic failure. The Pasch Patent solved this problem by inhibiting corrosion during the CMP and post-CMP cleanup processes.

48. The Pasch Patent contains 4 independent claims and 34 total claims, covering various processes. Claim 11 reads:

A process of inhibiting corrosion of metal plugs formed in integrated circuits, comprising:

providing a partially fabricated integrated circuit surface including said metal plugs;

polishing the partially fabricated integrated circuit surface including the metal plugs with a slurry,

introducing a fining solution including a corrosion inhibiting compound on a polishing pad in sufficient concentration to inhibit corrosion of said metal plugs of said partially fabricated integrated circuit; and

fine polishing a surface of said partially fabricated integrated circuit including said metal plugs.

49. Renesas has directly infringed one or more claims of the Pasch Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Pasch Patent, and/or Renesas has directly infringed one or more claims of the Pasch Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Pasch Patent (*e.g.*, claims 11, 13-15, 17, 28, 30-32, and 34).¹

Such products manufactured using these infringing methods include, but are not limited to:

- Renesas’s copper-based products that have a metallization interconnect system and undergo fine polishing/fining and/or wafer scrubbing;
- Renesas’s UPD720202, a USB host controller compatible with the PCIe Gen2 specification and intended for desktop and laptop computers, tablets, and servers; PCI Express Cards; Digital TVs, set-top boxes, and Blu-ray players, and other media applications;

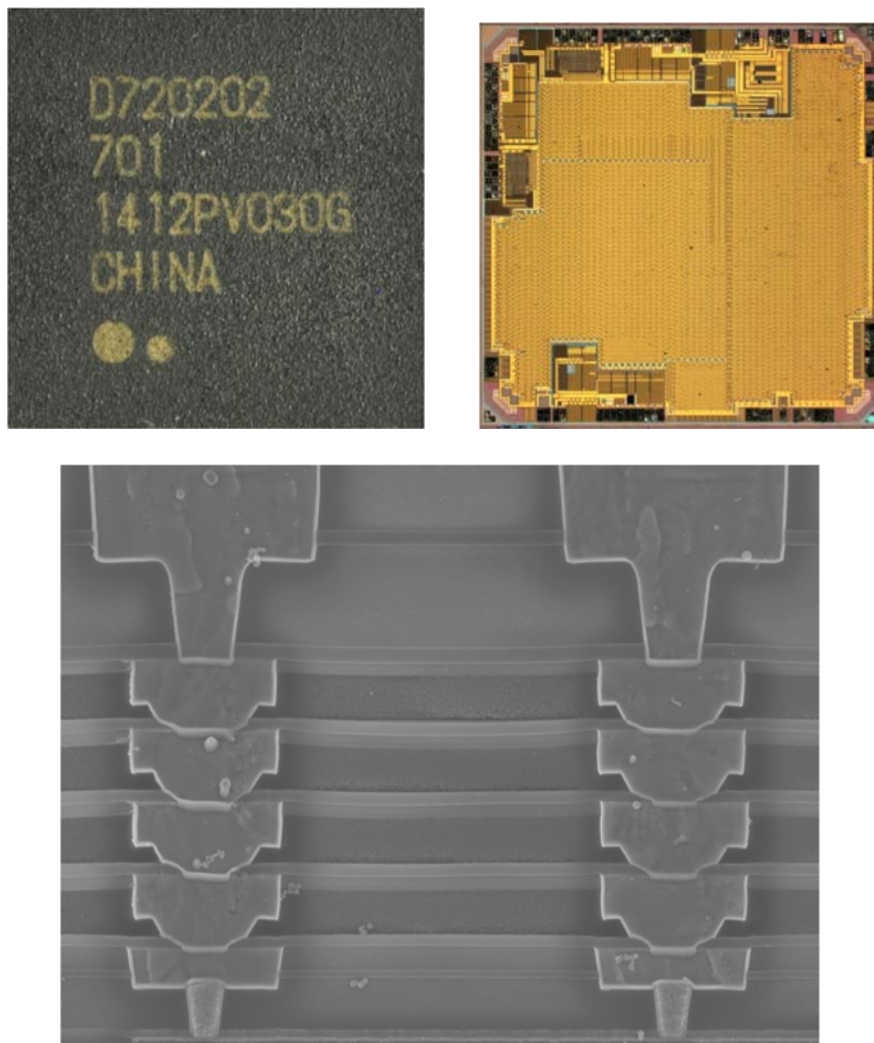
¹ Throughout this Third Amended Complaint, wherever Bell Semic identifies specific claims of the Asserted Patents that Renesas infringes, Bell Semic expressly reserves the right to identify additional asserted claims and products in its infringement contentions in accordance with the local rules and the Court’s Case Management Order. Specifically identified claims throughout this First Amended Complaint are provided for notice pleading only and are not presented as “exemplary” claims of all other claims for any Asserted Patent.

- Renesas's D813301 GPU, incorporated as the graphics processor in the Nintendo Wii;
- Renesas's R8A77240D500BGV, an application processor is intended for use in portable and mobile devices, with support for One-Seg terrestrial digital TV broadcasts, such as in car navigation systems and personal navigation devices;
- Renesas's R5S72641W144FPU MCU from the SuperH RISC Family used in the digital audio field;
- Renesas's R7S721011VCBG MPU from the RZ Family for Intelligent IoT End Point devices;
- Renesas's R7F7010233AFP MCU, an in-vehicle microcomputer for automotive body applications;
- Renesas's R5S72620W144FPU MCU from the SuperH RISC Family used in the digital audio field;
- Renesas's R8A77800BNBGV MCU from the SuperH RISC Family is an embedded, stand-alone Host Processor aimed at the multimedia, infotainment and consumer networking market; and
- Renesas's devices that are processed by Renesas's copper semiconductor manufacturing processes through other technology nodes, including the 45nm, 65nm, 90 nm, and 0.13 μ m nodes (collectively "Pasch Accused Products").

50. By way of non-limiting example only, the Renesas's Cu Technology used to manufacture the Renesas uPD720202 meets all of the steps of claim 11 of the Pasch Patent including a process of inhibiting corrosion of metal plugs by (1) providing a partially fabricated integrated circuit surface with metal plugs; (2) polishing the partially fabricated integrated circuit surface with metal plugs with a slurry; (3) introducing a fining solution with a corrosion

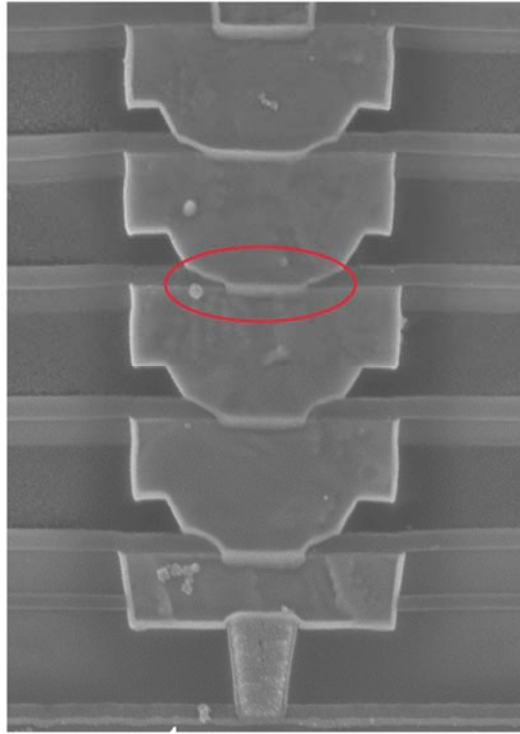
inhibiting compound on a polishing pad in a sufficient concentration to inhibit corrosion of the metal plugs of the partially fabricated integrated circuit; and (4) fine polishing a surface of the partially fabricated integrated circuit with metal plugs.

51. As shown below, the Renesas uPD720202 USB controller is an integrated circuit.



52. On information and belief, during manufacture of the Renesas UPD720202 USB controller, Renesas used a process of inhibiting corrosion of metal plugs formed in integrated circuits, where a partially fabricated integrated circuit surface with metal plugs is polished with a slurry, a fining solution with a corrosion inhibiting compound is introduced (as is now standard industry practice in semiconductor manufacturing) on a polishing pad in sufficient concentration

to inhibit corrosion of the metal plugs of the partially fabricated integrated circuit (as evidenced below), and a surface of the partially fabricated integrated circuit with metal plugs is fine-polished.



53. Claim 11 of the Pasch Patent applies to each Pasch Accused Product at least because those products contain copper interconnects that undergo the same or similar fine polishing/fining and/or wafer scrubbing as the Renesas UPD720202 USB controller.

54. On information and belief, each of the Pasch Accused Products have been available for purchase in the United States, including but not limited to, directly from Renesas, through Renesas's website, and/or through Renesas-authorized Americas distributors

55. By way of example only, the Renesas R7S721011VCBG has been available for purchase in the United States, including but not limited to through Renesas's website, either directly from Renesas or through at least 5 Renesas-authorized Americas distributors:

R7S721011VCBG User's Manual: Hardware

RZ/A1M is a full-featured part in the RZ/A1 family with an Arm® Cortex®-A9 core running at 400MHz and 5MB of on-chip SRAM to support large frame-buffers on-chip.

Overview Design Support Documentation Sample Code Software & Tools Ordering

Orderable Parts

Orderable Part Name	Product Longevity Program (PLP)	Production Status	1000 Piece Budgetary Price For MLO, please inquire.	MOQ	Package Info	Distributors	Request Samples	Buy Direct
R7S721011VCBGAC0	Mar. 2021	Mass Production	call	1	PRBG0324GA-A	21 Distributors	Sample	Buy

Package Information

Pins: 224
 Terminal pitch (mm): 0.8 mm
 Package Type: FBGA
 Dimensions (mm): 19x19 mm²
 Drawing Link: [prbg0324ga_n](#)
 Mount pad: [fig0013e](#)
 Mounting height (mm) [MAX]: 2.1 mm
 Mass (g) [TYP.]: 1.2 g
 Renesas code: PRBG0324GA-A
 JEITA code: P-19GA324-19x19-0.8D
 Terminal material - Base: Sn Ag Cu
 Terminal material - Surface: -
 EU RoHS: Compliant
 RoHS pdf (China RoHS): [English](#)

Order from an Authorized Distributor

Americas EMEA Japan China Asia Pacific

Distributor	Stock	Buy
Arrow Electronics, Inc.	50	Buy
Avnet	1082	Buy
Digi-Key	23	Buy
Mouser	57	Buy
Verical	50	Buy

See <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz/rza/rza1m/device/R7S721011VCBG.html#ordering> (last visited March 3, 2020).

56. Renesas has known of the Pasch Patent and has been on notice of its infringement of Pasch Patent since at least July 10, 2015, when Avago first identified the Renesas UPD720202 USB controller, RA877240D500BGV, and R5S72641W144FPU MCU as exemplary of Renesas's infringement of the Pasch Patent. On September 14, 2015, Avago again identified these Renesas products and another Renesas product, the D813301 GPU, as exemplary of Renesas's infringement of the Pasch Patent, including a claim chart mapping the claims of the Pasch Patent to these same products. After Bell Semic acquired the Broadcom semiconductor portfolio, including the Pasch Patent, Bell Semic met with Renesas on December 21, 2017, and identified these same Renesas products as exemplary of Renesas's infringement of the Pasch Patent. On March 21, 2019, Bell Semic sent a letter to Renesas identifying the same Renesas

products and identified four more Renesas products, the Renesas R7S721011VCBG, R7F7010233AFP, R5S72620W144FPU, and R8A77800BNBGV, as exemplary of Renesas's infringement of the Pasch Patent. Renesas did not respond to that correspondence. Bell Semic wrote again to Renesas on April 26, 2019, again identifying these Renesas products as infringing and exemplary of Renesas's infringement. Renesas has not substantively responded in any way to the infringement allegations in this claim chart or Bell Semic's further identification of infringing products.

57. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Pasch Patent at least because Bell Semic provided Renesas with written notice of its infringement as detailed above.

58. Renesas, knowing that the process of manufacturing its Pasch Accused Products infringed the Pasch Patent and with specific intent for others to infringe the Pasch Patent, has induced infringement of one or more claims of the Pasch Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Pasch Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Pasch Accused Products, as well as products incorporating the same. By way of example only, on information and belief, the Renesas D813301 GPU was incorporated as the graphics processor in the Nintendo Wii:



Despite knowing that this graphics processor would be incorporated in the Nintendo Wii and that at least a sizable number of Nintendo Wiis would be manufactured, imported, sold, and/or used in the United States, Renesas continued to sell the infringing Renesas D813301 GPU to Nintendo for inclusion in the Nintendo Wii.

59. Renesas has known since at least July 10, 2015 that the process of manufacturing the Pasch Accused Products infringed the Pasch Patent. Despite this knowledge, Renesas knowingly and intentionally instructed its OEMs, package assemblers, and foundry suppliers to infringe the Pasch Patent through the unlicensed manufacture and assembly of the Pasch Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. Renesas further knowingly and intentionally aided and abetted infringement of the Pasch Patent by its customers', distributors', and/or other third parties' sale and distribution of the Pasch Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. Renesas further knowing and intentionally aided and abetted infringement of the Pasch Patent through the use, sale, offers for sale, and/or importing in or into the United States of the Pasch Accused Products,

at least through user manuals, product documentation, and other materials, including without limitation those located on Renesas's website.

60. Renesas further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Pasch Accused Products and/or products incorporating the Pasch Accused Products in the United States by marketing the Pasch Accused Products in the United States; providing information such as detailed datasheets supporting use of the Pasch Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the Pasch Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the Pasch Accused Products into end-user products through the development of Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; and by providing online support platforms including Renesas Rulz forum and Renesas Synergy Platform further explaining how to use Renesas products.

61. Bell Semic has sustained and is entitled to recover damages as a result of Renesas's past infringement of the Pasch Patent, in an amount adequate to compensate for Renesas's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

62. Renesas's infringement of the Pasch Patent was knowing, deliberate, and willful. Renesas learned of its infringement of the Pasch Patent no later than July 10, 2015. As detailed above, Bell Semic and Avago sent letters, corresponded, and/or met with Renesas on July 10, 2015, September 14, 2015, December 21, 2017, and March 21, 2019, identifying the Pasch Patent as being infringed by Renesas's exemplary Pasch Accused Products. Despite these efforts, and knowing that it was willfully infringing the Pasch Patent, Renesas continued to commit acts

of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Pasch Patent, despite a risk of infringement that was known or so obvious that it should have been known to Renesas, and/or even though Renesas otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, Renesas's conduct was egregious. Renesas's knowing, deliberate, and willful infringement of the Pasch Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 2

Willful Infringement of U.S. Patent No. 6,153,543 (Chesire Patent)

63. Plaintiff re-alleges and incorporates by reference the allegations in Paragraphs 1-19, 24-26, and 35-44 as if fully set forth herein.

64. The Chesire Patent is generally related to a method of forming a passivation layer over features located on a top layer on a semiconductor device. The method involves depositing a first void-free dielectric layer over the top layer using high density plasma chemical vapor deposition, and depositing a second void-free dielectric layer over the first void-free layer. (*See* Chesire Patent, Abstract.)

65. During the manufacture of semiconductor devices, dielectric and metal layers are added onto a wafer until a final layer of metal is added, *i.e.*, the "top metal layer". Typically, a barrier, or passivation layer, is placed over the top metal layer to maintain the mechanical integrity of the semiconductor device, prevent mobile ion diffusion, and provided some radiation protection for the semiconductor device. Prior art methods of applying passivation layers were capable of filling gaps between adjacent features when the distance between the features was large, however, as the size of features and gaps became smaller, unfilled gaps were left in the

passivation layer, which become voids in the passivation layer. These voids can cause reliability problems due to entrapment of gases or liquids in the voids. These voids can also act as stress raisers, which can result in inferior mechanical strength of the passivation layer and allow metal interconnections to stress relieve into the voids. The inferior mechanical strength caused by these voids can also be a problem when the chip is removed from the wafer and pressed into the die assembly or other chip carrier. This pressing of the chip transmits a significant force to the passivation level of the chip. A common result of such a transmission of force is damage to the runners in the top metal layer. This damage can be even more prevalent when the runners have high aspect ratios such that the height dimension is significantly greater than the width dimension. Features having this type of aspect ratio are more susceptible to a force applied in the vertical or transverse direction, which occurs when the chip is pressed. One method of compensating for the voids has been to provide a very thick passivation level, however, a thick passivation level, besides being more costly, does not solve the problems associated with the voids. The Chesire Patent solved these problems by using high density plasma chemical vapor deposition to deposit a first void-free layer of a first dielectric over the top layer at a first deposition/sputtering-rate ratio, and then depositing a second void-free layer of a second-layer of a second dielectric over the first void-free layer at a deposition/sputtering-rate ratio greater than the first.

66. The Chesire Patent contains 1 independent claim and 9 total claims, covering various methods. Claim 5 depends from independent claim 1 and reads:

[A method of forming a passivation layer over features located on a top layer of a semiconductor device, comprising the steps of:

depositing a first void-free layer of a first dielectric over said top layer using high density plasma chemical vapor deposition at a first D/S ratio, and

depositing a second void-free layer of a second dielectric over said first void-free layer at a second D/S ratio, wherein said second D/S ratio is greater than said first D/S ratio],

wherein said first layer is applied with a thickness of at least 40% of the height of said features.

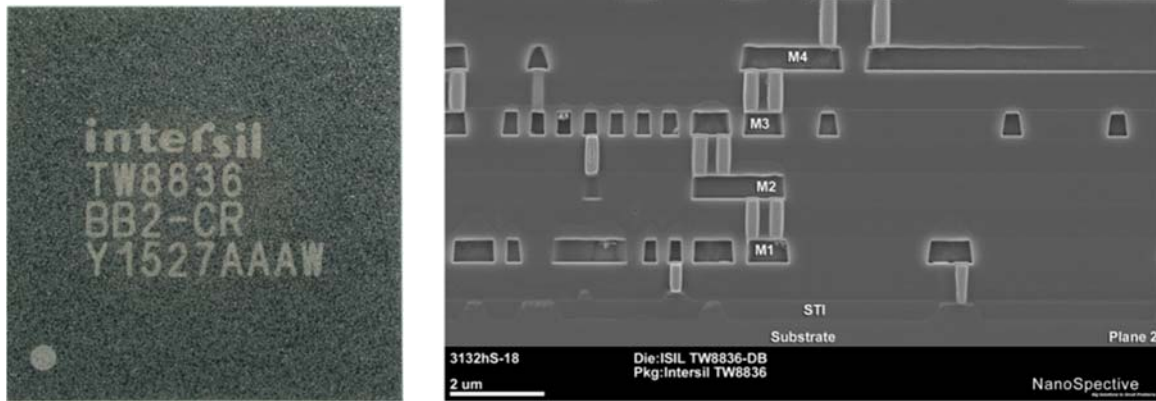
67. Renesas has directly infringed one or more claims of the Chesire Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a) by making products in the United States without authorization using methods covered by one of more claims of the Chesire Patent and/or Renesas has directly infringed one or more claims of the Chesire Patent, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(g) at least by using, selling, offering to sell, and/or importing in or into the United States products that are made by a process using one or more claims of the Chesire Patent (*e.g.*, claims 5-8). Such products manufactured using these infringing methods include, but are not limited to:

- Renesas products with two or more void-free layers of passivation located on the top layer of a semiconductor device with the final metal layer being aluminum;
- Renesas's TW8836, an integrated LCD video processor that incorporates many of the features required to create a multipurpose LCD display system into a single package;
- Renesas's R7S721011VCBG MPU from the RZ Family for designing Intelligent IoT End Point devices;
- Renesas's R7F7010233AFP MCU, an in-vehicle microcomputer from the RH850 Family, for automotive body applications;
- Renesas's R5F10AGEKNA MCU from the RL78 Family, used for general automotive electrical applications (motor control, door control, headlight control, etc.), and motorcycle engine control;

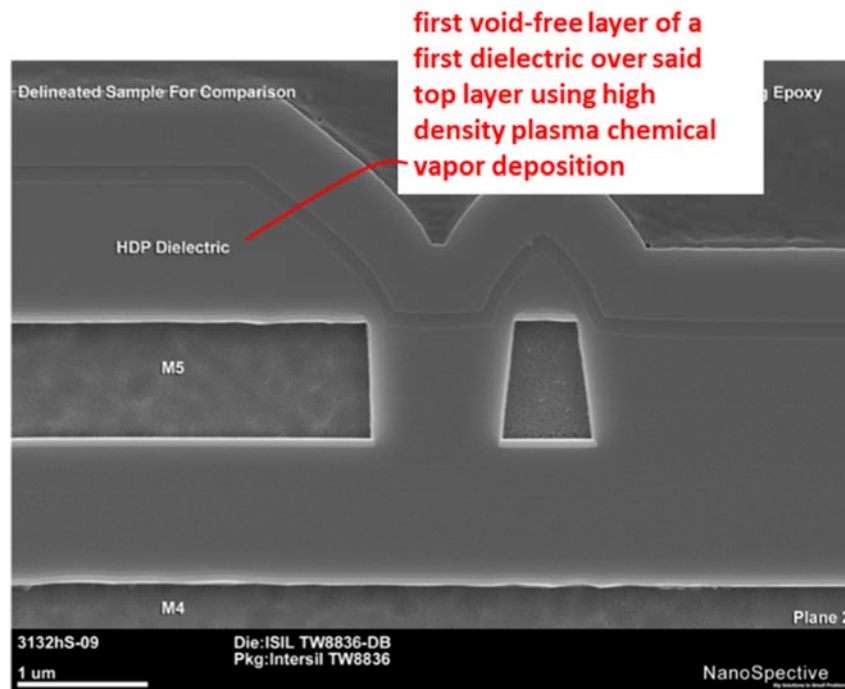
- Renesas’s R5F10CLDJFB MCU from the RL78 Family, used for automotive low-end instrument clusters with built-in features such as sound generator, stepper motor controller/driver, and segmented LCD driver;
- Renesas’s R5F109ACKSP MCU, an automotive general-purpose low-end microcontroller from the RL78 Family, has various built-in functions necessary for automotive application communications and implementing functional safety;
- Renesas’s R5F104PJA MCU from the RL78 Family for motor control as well as industrial and metering applications; and
- Renesas’s devices that are variants of the above-identified products; (collectively “Cheshire Accused Products”).

68. By way of non-limiting example only, the process of manufacturing the Renesas TW8836 meets all the steps of claim 5 of the Cheshire Patent including forming a passivation layer over features located on a top layer of the semiconductor device by (1) depositing a first void-free layer of a first dielectric over the top layer using high density plasma chemical vapor deposition at a first D/S ratio; and (2) depositing a second void-free layer of a second dielectric over the first void-free layer at a second D/S ratio that is greater than the first D/S ratio, and where the first layer is applied with a thickness of at least 40% of the height of the features.

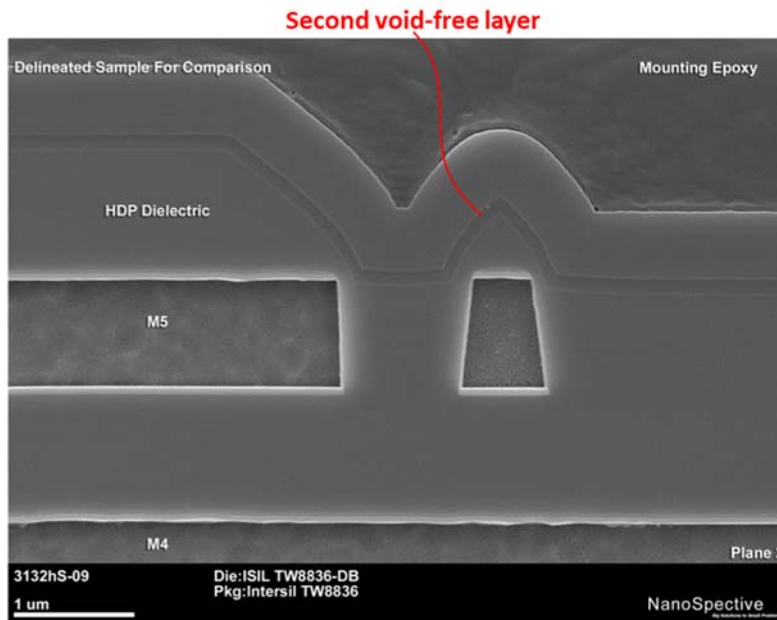
69. As shown below, the Renesas TW8836 is a semiconductor device with a passivation layer formed over features on a top layer of the semiconductor device:



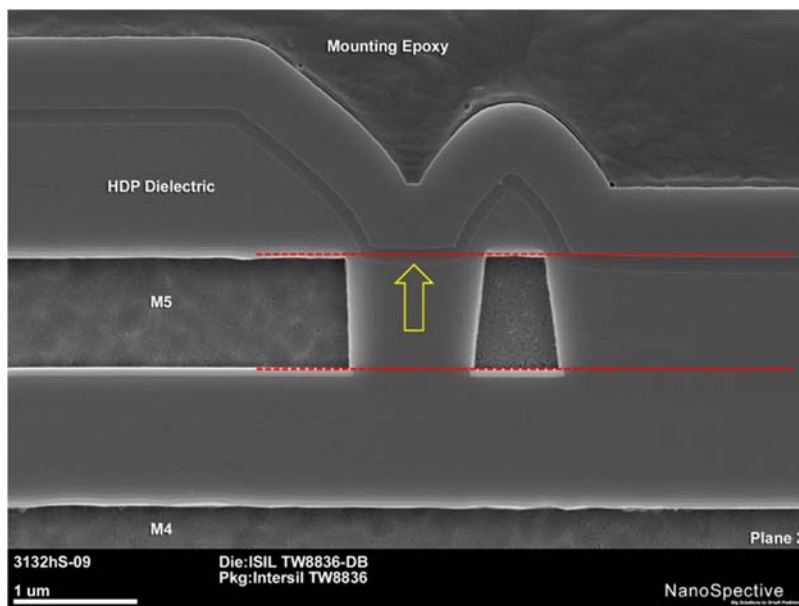
70. During manufacture of the TW8836, a first void-free layer of a first dielectric is deposited over the top layer using high density plasma chemical vapor deposition at a first D/S ratio:



71. During manufacture of the Renesas TW8836, a second void-free layer of a second dielectric is deposited over the first void-free layer at second D/S ratio that is greater than the first D/S ratio:



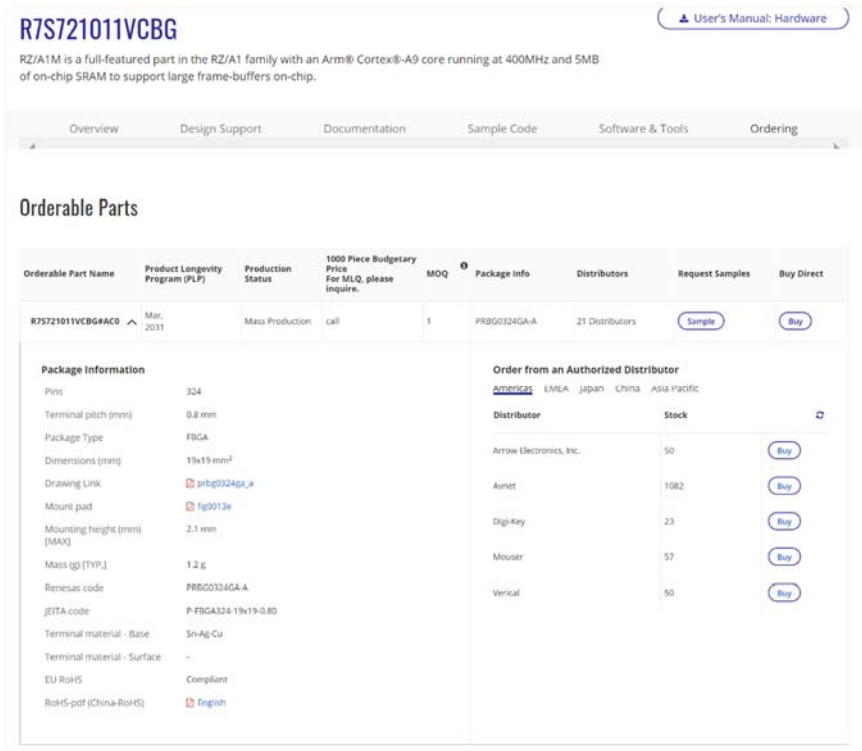
72. The deposited first layer also is applied with a thickness of at least 40% of the height of the features:



73. Claim 5 of the Chesire Patent applies to each Chesire Accused Product at least because each of those products were manufactured with the same or similar two or more void-free layers of passivation located on the top layer of a semiconductor device with the final metal layer being aluminum as the TW8836.

74. On information and belief, each of the Chesire Accused Products have been available for purchase in the United States, including but not limited to, directly from Renesas, through Renesas’s website, and/or through Renesas-authorized Americas distributors

75. By way of example only, on information and belief, the Renesas R7S721011VCBG has been available for purchase in the United States, including but not limited to through Renesas’s website, either directly from Renesas or through at least 5 Americas distributors:



See <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz/rza/rzal1m/device/R7S721011VCBG.html#ordering> (last visited March 4, 2020).

76. Renesas has known of the Chesire Patent and has been on notice of its infringement of Chesire Patent since at least September 14, 2015, when Avago first identified the Renesas R5F104PJA MCU as exemplary of Renesas's infringement of the Chesire Patent, including a claim chart mapping the claims of the Chesire Patent to the Renesas R5F104PJA MCU. After Bell Semic acquired the Broadcom semiconductor portfolio, including the Chesire Patent, Bell Semic met with Renesas on December 21, 2017, and again identified the Renesas R5F104PJA MCU as exemplary of Renesas's infringement of the Chesire Patent. On March 21, 2019, Bell Semic sent a letter to Renesas identifying the Renesas R5F104PJA MCU product and further identified the Renesas R7S721011VCBG MPU, R7F7010233AFP MCU, R5F10AGEKNA MCU, R5F10CLDJFB MCU, R5F109ACKSP MCU, and TW8836 as exemplary of Renesas's infringement of the Chesire Patent. Renesas did not respond to that correspondence. Bell Semic wrote again to Renesas on April 26, 2019, again identifying these Renesas products as exemplary of Renesas's infringement of the Chesire Patent.

77. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Chesire Patent at least because Bell Semic provided Renesas with written notice of its infringement as detailed above.

78. Renesas, knowing that the process of manufacturing the Chesire Accused Products infringes the Chesire Patent and with specific intent for others to infringe the Chesire Patent, has induced infringement of one or more claims of the Chesire Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by (1) actively inducing others to make in the United States without authorization the Chesire Accused Products; and/or (2) actively inducing others to use, sell, offer to sell, and/or import in or into the United States without authorization the Chesire Accused Products, as well as products incorporating the same.

79. Renesas has known since at least September 14, 2015 that the process of manufacturing the Chesire Accused Products infringed the Chesire Patent. Despite this knowledge, Renesas knowingly and intentionally instructed its OEMs and foundry suppliers to infringe the Chesire Patent through the unlicensed manufacture of the Chesire Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. Renesas further knowingly and intentionally aided and abetted infringement of the Chesire Patent by its customers', distributors', and/or other third parties' sale and distribution of the Chesire Accused Products with the expectation that such products, and/or products incorporating the same, would be used, sold, offered for sale, and/or imported in or into the United States. Renesas further knowing and intentionally aided and abetted infringement of the Chesire Patent through the use, sale, offer for sale, and/or importing the Chesire Accused Products, at least through user manuals, product documentation, and other materials, including without limitation those located on Renesas's website.

80. Renesas further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Chesire Accused Products and/or products incorporating the Chesire Accused Products in the United States by marketing the Chesire Accused Products in the United States; providing information such as detailed datasheets supporting use of the Chesire Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the Chesire Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the Chesire Accused Products into end-user products through the development of Partner programs, complimentary design review services, automated utilities, calculators, and reference designs;

and by providing online support platforms including Renesas Rulz forum and Renesas Synergy Platform further explaining how to use Renesas products.

81. Bell Semic has sustained and is entitled to recover damages as a result of Renesas's past infringement of the Chesire Patent, in an amount adequate to compensate for Renesas's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

82. Renesas's infringement of the Chesire Patent was knowing, deliberate, and willful. Renesas learned of its infringement of the Chesire Patent no later than September, 14, 2015. As detailed above, Bell Semic and Avago sent letters, corresponded, and/or met with Renesas on September 14, 2015, December 21, 2017, and March 21, 2019, identifying the Chesire Patent as being infringed by Renesas's exemplary Chesire Accused Products. Despite these efforts, and knowing that it was willfully infringing the Chesire Patent, Renesas continued to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Chesire Patent, despite a risk of infringement that was known or so obvious that it should have been known to Renesas, and/or even though Renesas otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, Renesas's conduct was egregious. Renesas's knowing, deliberate, and willful infringement of the Chesire Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 3

Willful Infringement of U.S. Patent No. 6,727,588 (Abdelgadir Patent)

83. Plaintiff re-alleges and incorporates by reference the allegations in Paragraphs 1-19, 27-30, and 35-44 as if fully set forth herein.

84. The Abdelgadir Patent is generally related to a cap or barrier layer that can prevent the migration of impurities in low dielectric constant material, thereby preventing the impurities from attacking conductive elements in subsequent levels of a multi-level integrated circuit structure. (*See* Abdelgadir Patent, Abstract.)

85. Due to the scaling and miniaturization of integrated circuits, low dielectric constant (low-k) materials are used to reduce parasitic capacitance. Fluorine-based precursors are used to form low-k dielectric layers. However, the presence of unbounded or loosely-bounded fluorine may adversely affect reliability and performance as fluorine can migrate or diffuse in the dielectric layer and attack the metal deposited over the surface of the dielectric layer. The Abdelgadir patent solved this problem by disposing a diffusion preventing barrier layer between a first dielectric layer and a metal layer at an upper level of the integrated circuit. The diffusion preventing barrier layer may be formed in-situ over the impurity containing dielectric material with the subsequent disposition of a metal layer thereover, and further processing of a multi-layer dielectric structure to include polishing. The in-situ deposition of the cap or barrier layer prevents the exposure of the impurity containing layer, thereby avoiding contamination of the layer.

86. The Abdelgadir Patent contains 2 independent claims and 13 total claims, covering various integrated circuits. Claim 6 reads:

An integrated circuit, comprising:

a substrate having at least one first conductive element disposed thereon;

a fluorine doped oxide layer disposed over and contacting said substrate and said first conductive element;

an impurity preventing silicon rich oxide barrier layer disposed over and contacting said fluorine doped oxide layer; and

at least one second conductive element disposed over said impurity preventing silicon rich oxide barrier layer having at least one surface of said second conductive element contacting said impurity preventing silicon rich oxide barrier layer.

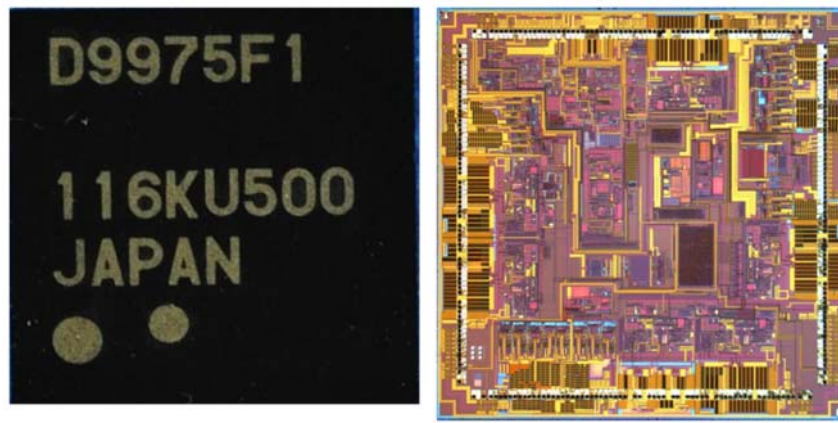
87. Renesas has directly infringed one or more claims of the Abdelgadir Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Abdelgadir Patent (*e.g.*, claims 6-11 and 13), including, but not limited to:

- Renesas products with an inter-level dielectric layer that is doped with fluorine and a silicon oxide layer over the fluorine-doped dielectric layer;
 - Renesas's UPD9975, a PMIC developed for Intel's Atom Processor Z6xx platforms;
 - Renesas's TW8836, an integrated LCD video processor that incorporates many of the features required to create a multipurpose LCD display system into a single package;
 - Renesas's UPD70F3336GC MCU from the V850 Family for applications that require a low power consumption, such as audio and car audio;
 - Renesas's UPD70F3371M2GBA1 from the V850 Family for automotive applications and provides general-purpose peripheral functions like serial communication interfaces, timers/counters, measurement and control functions, with full CAN network support; and
 - Renesas's devices that are variants of the above-identified products;
- (collectively, the "Abdelgadir Accused Products").

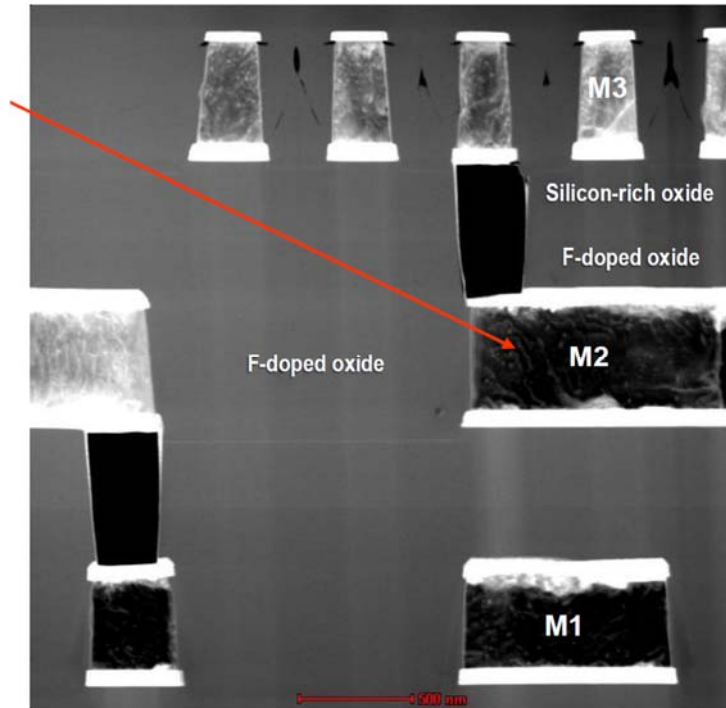
88. By way of non-limiting example only, Renesas's UPD9975 infringes claim 6 of the Abdelgadir Patent because it is a power management integrated circuit that has (1) a substrate with a first conductive element disposed thereon; (2) a fluorine doped oxide layer disposed over

and contacting the substrate and the first conductive element; (3) an impurity preventing silicon rich oxide barrier layer disposed over and contacting the fluorine doped oxide layer; and (4) a second conductive element disposed over the impurity preventing silicon rich oxide barrier layers and a surface of the second conductive element contacting the impurity preventing silicon rich oxide barrier layer.

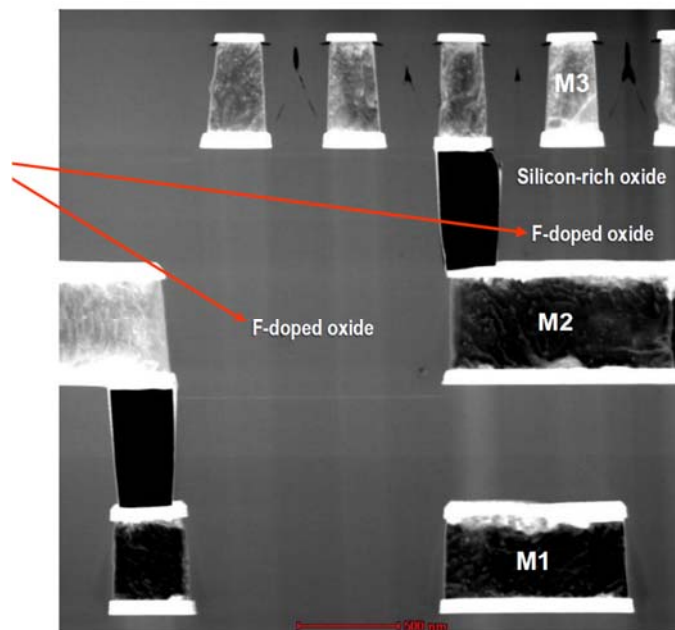
89. As shown below, the Renesas UPD9975 PMIC is an integrated circuit:



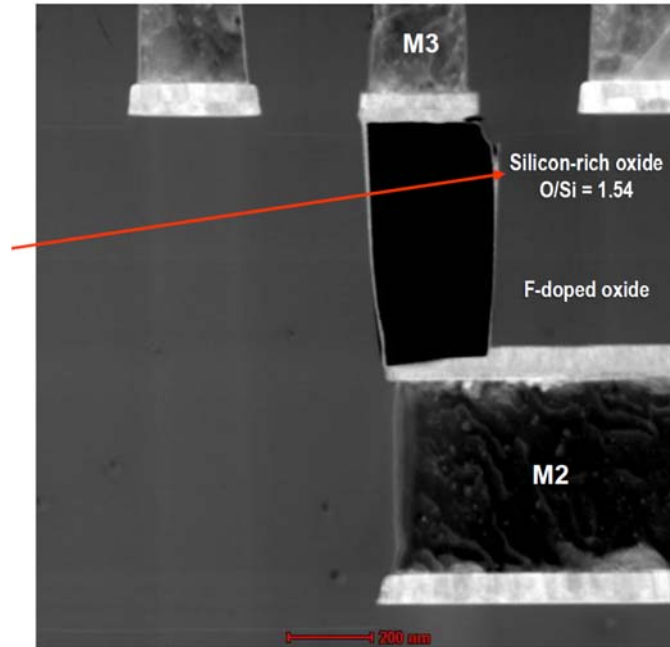
90. The Renesas UPD9975 PMIC has a substrate with a first conductive element disposed thereon:



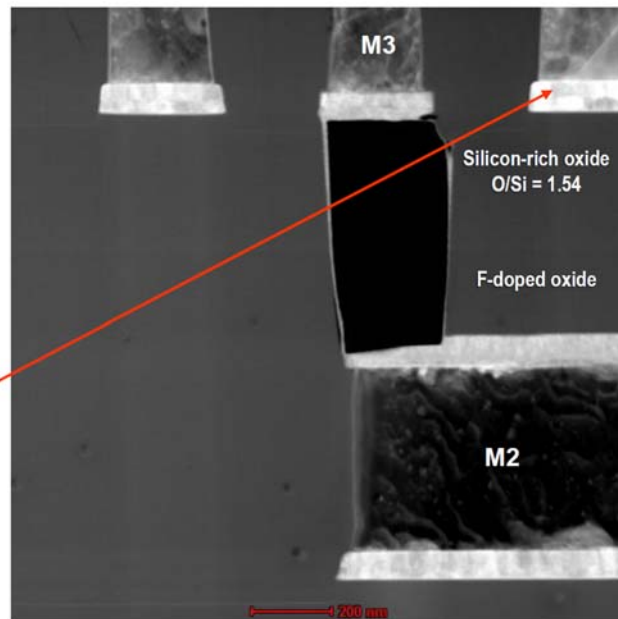
91. The Renesas UPD9975 PMIC further has a fluorine doped oxide layer disposed over and contacting the substrate and the first conductive element:



92. The Renesas UPD9975 PMIC further has an impurity preventing silicon rich oxide barrier layer disposed over and contacting the fluorine doped oxide layer:



93. The Renesas UPD9975 PMIC further has a second conductive element disposed over the impurity preventing silicon rich oxide barrier layer and at least one surface of the second conductive element contacts the impurity preventing silicon rich oxide barrier layer:



94. Claim 6 of the Abdelgadir Patent applies to each Abdelgadir Accused Product at least because each of those products have the same or similar inter-level dielectric layer that is

doped with fluorine and a silicon oxide layer over the fluorine-doped dielectric layer as the Renesas UPD9975 PMIC.

95. On information and belief, each of the Abdelgadir Accused Products have been available for purchase in the United States, including but not limited to, directly from Renesas, through Renesas's website, and/or through Renesas-authorized Americas distributors.

96. By way of example only, the Renesas TW8836 has been available for purchase in the United States, including but not limited to through Renesas's website, either directly from Renesas or through at least one Renesas-authorized Americas distributor:

TW8836
LCD Video Processor with Decoder, Triple ADCs, LVDS and TTL Input, MCU, OSD, TCON and LVDS Interface

Overview Design Support Documentation Ordering

Orderable Parts

Orderable Part Name	Product Longevity Program (PLP)	Production Status	1000 Piece Budgetary Price For MLQ, please inquire.	MOQ	Package Info	Distributors	Request Samples	Buy Direct
TW8836AT-LB2-GET	-	Mass Production	\$7.25	500	Q128.14K14C	0 Distributors	-	Buy
TW8836AT-LB2-GE	-	Mass Production	\$7.15	90	Q128.14K14C	0 Distributors	-	Buy
TW8836-LB2-CE	-	Mass Production	\$6	180	Q128.14K14C	12 Distributors	-	Buy
TW8836-8B2-CR	-	Mass Production	\$6.5	200	V172.8X8	5 Distributors	-	Buy

Package information

Name	TF8GA
Previous code	V9G
Renesas code	V172.8X8
Terminal count	172
Terminal pitch (mm)	0.5 mm
Dimensions (mm)	8.00x8.00
Mass (g) [TYP.]	0.095
Drawing Link	v172.8x8

Order from an Authorized Distributor

Americas EMEA Japan China Asia Pacific

Distributor Stock 235

Digi Key

Orderable Part Information

MSL	3
RoHS Status	RoHS Compliant - See Details

Back to Top

See <https://www.renesas.com/us/en/products/audio-video/display/display-processors/device/TW8836.html#ordering> (last visited March 4, 2020).

97. Renesas has known of the Abdelgadir Patent and has been on notice of its infringement of Abdelgadir Patent since at least September 14, 2015, when Avago first identified the Renesas UPD9975 PMIC as exemplary of Renesas's infringement of the Abdelgadir Patent,

including a claim chart mapping the claims of the Abdelgadir Patent to the Renesas UPD9975 PMIC. After Bell Semic acquired the Broadcom semiconductor portfolio, including the Abdelgadir Patent, Bell Semic met with Renesas on December 21, 2017, and again identified the Renesas UPD9975 PMIC as exemplary of Renesas's infringement of the Abdelgadir Patent. On March 21, 2019, Bell Semic sent a letter to Renesas identifying the Renesas R5F104PJA MCU product and further identified the Renesas TW8836, UPD70F3336GC MCU, and UPD70F3371M2GBA1 as exemplary of Renesas's infringement of the Abdelgadir Patent. Renesas did not respond to that correspondence. Bell Semic wrote again to Renesas on April 26, 2019, again identifying these Renesas products as exemplary of Renesas's infringement of the Abdelgadir.

98. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Abdelgadir Patent because Bell Semic provided Renesas with written notice of its infringement as detailed above.

99. Renesas, knowing its products infringed the Abdelgadir Patent and with specific intent for others to infringe the Abdelgadir Patent, has induced infringement of one or more claims of the Abdelgadir Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, distributors, customers, end-users, and other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Abdelgadir Accused Products, as well as products containing the same. Renesas knowingly and intentionally instructed its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on Renesas's website. Renesas actively and knowingly aided

and abetted infringement through the use, importation, sale, and/or offers for sale by its customers and downstream distributors and through the use by end-users of the products incorporating the Abdelgadir Accused Products in the United States. Renesas has known since at least September 14, 2015, that the Abdelgadir Accused Products infringed the Abdelgadir Patent, and purposefully and knowingly sold and offered to sell the Abdelgadir Accused Products to its customers with the knowledge and expectation that the Abdelgadir Accused Products would enter the United States market, where they would be imported, used, sold, and offered for sale by its customers and downstream distributors.

100. Renesas further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Abdelgadir Accused Products and/or products incorporating the Abdelgadir Accused Products in the United States by marketing the Abdelgadir Accused Products in the United States; providing information such as detailed datasheets supporting use of the Abdelgadir Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the Abdelgadir Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the Abdelgadir Accused Products into end-user products through the development of Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; and by providing online support platforms including Renesas Rulz forum and Renesas Synergy Platform further explaining how to use Renesas products.

101. Renesas has contributed to the infringement of one or more claims of the Abdelgadir Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Abdelgadir Accused Products, which constitute a material part of the invention of the Abdelgadir

Patent, knowing the Abdelgadir Accused Products to be especially made or especially adapted for use in infringement of the Abdelgadir Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

102. Bell Semic has sustained and is entitled to recover damages as a result of Renesas's past infringement, in an amount adequate to compensate for Renesas's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

103. Renesas's infringement of the Abdelgadir Patent was knowing, deliberate, and willful. Renesas learned of its infringement of the Abdelgadir Patent no later than September 14, 2015. As detailed above, Bell Semic and Avago sent letters, corresponded, and/or met with Renesas on September 14, 2015, December 21, 2017, and March 21, 2019, identifying the Abdelgadir Patent as being infringed by Renesas's exemplary Abdelgadir Accused Products. Despite these efforts, and knowing that it was willfully infringing the Abdelgadir Patent, Renesas continued to commit acts of direct and indirect infringement despite knowing its actions constituted infringement of the valid and enforceable Abdelgadir Patent, despite a risk of infringement that was known or so obvious that it should have been known to Renesas, and/or even though Renesas otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, Renesas's conduct was egregious. Renesas's knowing, deliberate, and willful infringement of the Abdelgadir Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

COUNT 4

Willful Infringement of U.S. Patent No. 6,879,046 (Gibson Patent)

104. Plaintiff re-alleges and incorporates by reference the allegations in Paragraphs 1-19, 31-34, and 35-44 as if fully set forth herein.

105. The Gibson Patent is generally related to a split barrier layer that enables copper interconnect wires to be used in conjunction with low-k dielectric films by preventing the diffusion of N—H base groups into photoresists where they can render the photoresist insoluble. The split barrier layer is disposed between the copper and the low-k dielectric, and including a nitrogen-containing, oxygen-free film which contacts the copper, and an oxygen-containing, nitrogen-free film which contacts the low-k dielectric film. The nitrogen-containing film prevents the diffusion of N—H base groups into the low-k dielectric films. (*See* Gibson Patent, Abstract.)

106. During the fabrication of semiconductor devices, the lithography process uses chemically amplified deep ultra-violet (DUV) photoresists to improve the performance of the lithography system and improve device feature resolution. Low dielectric constant (low-k) dielectrics and copper interconnect schemes are favored manufacturing techniques because they increase device speed, provide lower cost processing, and improve level-to-level alignment, which provide for tighter design rules and improve performance. However, during the patterning of the low-k dielectric material to form the damascene or dual-damascene structures, this combination causes base groups such as N—H base groups to diffuse into porous regions of the low-k dielectric materials, rendering any exposed photoresist that interacted with the N—H base group insoluble to developer solution. The N—H base groups are formed during the dual damascene process, where the etch stop layers and barrier films contain nitrogen and N—H base groups are formed. Additionally, ammonia compounds are used to clean or treat copper surfaces

to remove any oxides that may have formed and to remove any organic corrosion inhibitor.

These ammonia containing chemistries also produce the N—H base group. The Gibson Patent solves this problem by providing a method and structure for isolating copper surfaces and nitrogen-containing layers and films, from low-k dielectric materials. The Gibson Patent teaches isolating of these layers by forming a split barrier layer that is disposed between the copper and the low-k dielectric, and including a nitrogen-containing, oxygen-free film which contacts the copper, and an oxygen-containing, nitrogen-free film which contacts the low-k dielectric film. The oxygen-containing film prevents the diffusion of N—H base groups into the low-k dielectric films.

107. The Gibson Patent contains 4 independent claims and 13 total claims, covering various semiconductor products. Claim 1 reads:

A semiconductor product comprising a barrier layer disposed between a copper-containing structure and a low-k dielectric film, said barrier layer comprising a composite film structure including a nitrogen-containing, substantially oxygen-free first film forming a boundary with said copper containing structure and an oxygen-containing, substantially nitrogen-free second film forming a boundary with said low-k dielectric film in which said first film comprises nitrogen-doped silicon carbide and said second film comprises oxygen-doped silicon carbide.

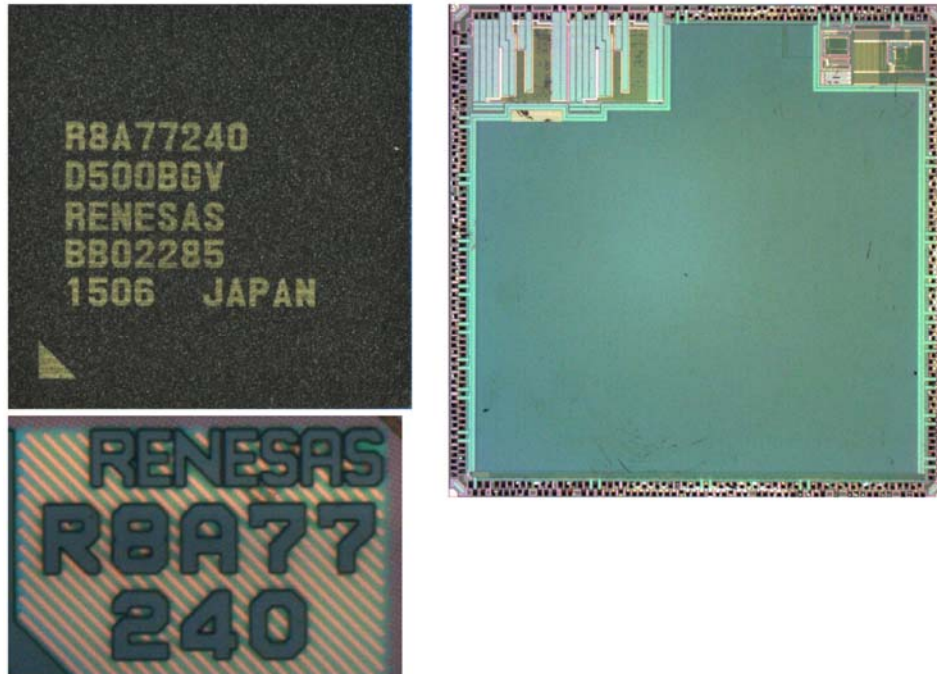
108. Renesas has directly infringed, and continues to directly infringe, one or more claims of the Gibson Patent under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, at least by making, using, selling, offering to sell, and/or importing in or into the United States without authorization products covered by one or more claims of the Gibson Patent (*e.g.*, claims 1-3 and 7), including, but not limited to:

- Renesas products with a split barrier layer that enables copper interconnects to be formed in low-k dielectric films manufactured using chemically amplified photoresists;

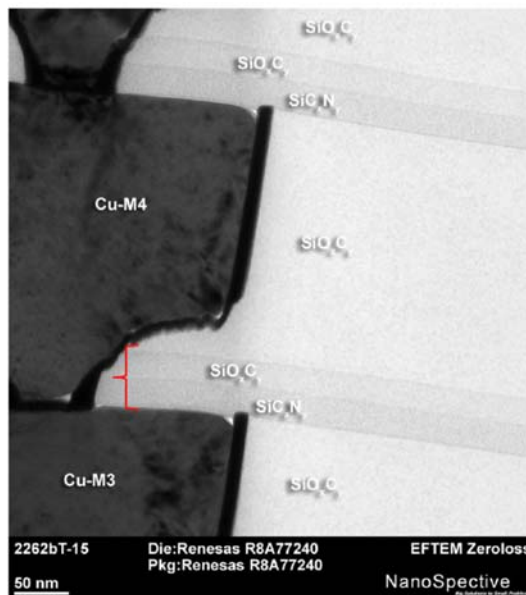
- Renesas’s R8A77240D500BGV, an application processor intended for use in portable and mobile devices with support for One-Seg terrestrial digital TV broadcasts, such as car navigation systems and personal navigation devices;
 - Renesas’s R5S72641W144FPU MCU from SuperH RISC Family for the digital audio field;
 - Renesas’s devices that are variants of the above-identified products; and
 - All other Renesas semiconductor devices, integrated circuits, and products that have copper interconnects and are manufactured using chemically amplified photoresists which use the infringing technology;
- (collectively “Gibson Accused Products”).

109. By way of non-limiting example only, Renesas’s R8A77240D500BGV infringes claim 1 of the Gibson Patent because it is a semiconductor product that has a barrier layer disposed between a copper-containing structure and a low-k dielectric film, where the barrier layer comprises a composite film structure with (1) a nitrogen-containing, substantially oxygen-free first film forming a boundary with the copper-containing structure and (2) an oxygen-containing, substantially nitrogen-free second film forming a boundary with the low-k dielectric film, where the first film comprises nitrogen-doped silicon carbide and the second film comprises oxygen-doped silicon carbide.

110. As shown below, the Renesas R8A77240D500BGV is a semiconductor product:

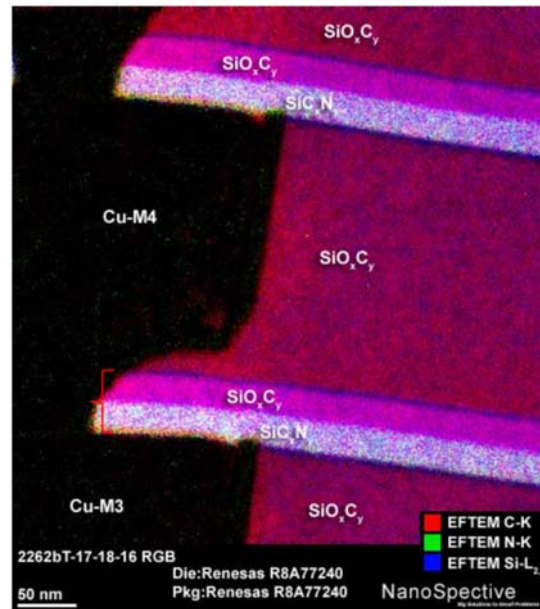


111. The Renesas R8A77240D500BGV has a barrier layer (indicated in red below) between a copper containing structure (designated Cu-M3 below) and a low-k dielectric film disposed above the barrier layer:



112. The barrier layer in the Renesas R8A77240D500BGV comprises a composite film structure with a nitrogen-containing, substantially oxygen-free first film (SiC_xN_y in the barrier

layer) forming a boundary with the copper-containing structure(Cu-M3) and an oxygen-containing, substantially nitrogen-free second film (SiO_xC_y in the barrier layer) forming a boundary with the low-k dielectric film above the barrier layer. The first film comprises nitrogen-doped silicon carbide (SiC_xN_y) and the second film comprises oxygen-doped silicon carbide (SiO_xC_y).



113. Claim 1 of the Gibson Patent applies to each Gibson Accused Product at least because each of those products contain the same or similar split barrier layer that enables copper interconnects to be formed in low-k dielectric films manufactured using chemically amplified photoresists as the Renesas R5S72620W144FPU.

114. On information and belief, each of the Gibson Accused Products have been available for purchase in the United States, including but not limited to, directly from Renesas, through Renesas's website, and/or through Renesas-authorized Americas distributors.

115. By way of example only, on information and belief, the Renesas R5S72620W144FPU has been available for purchase in the United States, including but not

limited to through Renesas’s website, either directly from Renesas or through at least 3 Renesas-authorized Americas distributors:

R5S72620W144FPU User's Manual: Hardware

Renesas Electronics had earlier launched the SH7260 Series of microcontrollers, built around the SH2A-FPU 32-bit CPU core with superb real time processing capability, as a solution for the digital audio field. The SH7262 and SH7264 belong to the SH7260 Series of microcontrollers, and the maximum operating frequency of 144 MHz enables faster operation in applications such as equipment control or digital audio signal processing. This combination of excellent signal processing performance and ROM code efficiency means that compression and decompression of audio data in formats required by digital audio applications, such as MP3, WMA, or AAC (Advanced Audio Coding), is performed more quickly and program sizes are reduced. Thanks to the newly added large-capacity SRAM, not only processing tasks related to equipment control and digital audio, but also video display capabilities can be implemented on a single chip. An ample 1-Mbyte or 640-Kbyte of on-chip SRAM is provided for video display use. It can be configured as a frame buffer to store video data temporarily, which is necessary when implementing graphical display capabilities. The generous SRAM capacity means that it is possible to use a TFTLCD panel display up to WQVGA size (480 x 240 pixels) without the need for external SDRAM as video memory. The SH7262 and SH7264 provide a new video display controller and digital video input pins for use with graphical and video display applications. Digital RGB output pins allow output of images or video in RGB565 format at up to WQVGA size (480 x 240 pixels). This reduces the total number of devices required and helps lower both the cost and the power consumption of the system.

Orderable Parts

Orderable Part Name	Product Longevity Program (PLP)	Production Status	1000 Piece Budgetary Price For MLQ, please inquire.	MOQ	Package Info	Distributors	Request Samples	Buy Direct
R5S72620W144FPU0	Feb, 2029	Mass Production	cell	1	PLQP0176KB-A	16 Distributors	-	Buy

Package Information

Pins	176
Terminal pitch (mm)	0.5 mm
Package Type	LQFP
Dimensions (mm)	24x24 mm ²
Drawing Link	plqp0176kb_a
Mount pad	fg0009e
Mounting height (mm) [MAX]	1.7 mm
Mass (g) [TYP.]	1.8 g
Renesas code	PLQP0176KB-A (old: FP-176EV)
JEITA code	P-LQFP176-24x24-0.50
Terminal material - Base	Cu alloy
Terminal material - Surface	Sn-Bi
EU RoHS	Compliant
RoHS-pdf (China-RoHS)	English

Order from an Authorized Distributor

[Americas](#) [EMEA](#) [Japan](#) [China](#) [Asia Pacific](#)

Distributor	Stock	
Mouser	1	Buy
RS Components	1	Buy
Verical	112	Buy

See <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/superh/sh7260/sh7262/device/R5S72620W144FPU.html#ordering> (last visited March 4, 2020).

116. Renesas has known of the Gibson Patent and has been on notice of its infringement of Gibson Patent since at least September 14, 2015, when Avago first identified the Renesas R8A77240D500BGV as exemplary of Renesas’s infringement of the Gibson Patent,

including a claim chart mapping the claims of the Gibson Patent to Renesas the R8A77240D500BGV. After Bell Semic acquired the Broadcom semiconductor portfolio, including the Gibson Patent, Bell Semic met with Renesas on December 21, 2017, and again identified the Renesas R8A77240D500BGV as exemplary of Renesas's infringement of the Gibson Patent. On March 21, 2019, Bell Semic sent a letter to Renesas identifying the Renesas R8A77240D500BGV product and further identified the Renesas R5S72620W144FPU MCU as exemplary of Renesas's infringement of the Gibson Patent. Renesas did not respond to that correspondence. Bell Semic wrote again to Renesas on April 26, 2019, again identifying these Renesas products as exemplary of Renesas's infringement of the Gibson.

117. To the extent applicable, the requirements of 35 U.S.C. § 287 have been met with respect to the Gibson Patent because Bell Semic provided Renesas with written notice of its infringement as detailed above.

118. Renesas, knowing its products infringe the Gibson Patent and with specific intent for others to infringe the Gibson Patent, has induced infringement of, and continues to induce infringement of, one or more claims of the Gibson Patent under 35 U.S.C. § 271(b), either literally and/or under the doctrine of equivalents, at least by actively inducing others, including its OEMs, foundry suppliers, distributors, customers, end-users, and other third parties, to make, use, sell, offer to sell, and/or import in or into the United States without authorization the Gibson Accused Products, as well as products containing the same. Renesas knowingly and intentionally instructs its customers, OEMs, foundry suppliers, distributors, and/or other third parties to infringe at least through user manuals, product documentation, and other materials, including without limitation those located on Renesas's website. Renesas actively and knowingly aids and abets infringement through the use, importation, sale, and/or offers for sale by its customers and

downstream distributors and through the use by end-users of the products incorporating the Gibson Accused Products in the United States. Renesas knows, and has known since at least September 14, 2015, that the Gibson Accused Products infringe the Gibson Patent, and purposefully and knowingly sells and offers to sell the Gibson Accused Products to its customers with the knowledge and expectation that the Gibson Accused Products will enter the United States market, where they will be imported, used, sold, and offered for sale by its customers and downstream distributors.

119. Renesas further induced infringement by encouraging its customers, downstream distributors, OEMs, and other end-users of the Gibson Accused Products and/or products incorporating the Gibson Accused Products in the United States by marketing the Gibson Accused Products in the United States; providing information such as detailed datasheets supporting use of the Gibson Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the Gibson Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the Gibson Accused Products into end-user products through the development of Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; and by providing online support platforms including Renesas Rulz forum and Renesas Synergy Platform further explaining how to use Renesas products.

120. Renesas has contributed to the infringement of, and continues to contribute to the infringement of, one or more claims of the Gibson Patent under 35 U.S.C. § 271(c), either literally and/or under the doctrine of equivalents, at least by selling, offering to sell, and/or importing in or into the United States the Gibson Accused Products, which constitute a material part of the invention of the Gibson Patent, knowing the Gibson Accused Products to be

especially made or especially adapted for use in infringement of the Gibson Patent, and not a staple article or commodity of commerce suitable for substantial non-infringing use.

121. Bell Semic has sustained and is entitled to recover damages as a result of Renesas's past and continuing infringement, in an amount adequate to compensate for Renesas's infringement, but in no event less than a reasonable royalty for the use made of the invention, together with interest and costs as fixed by the Court.

122. Renesas's infringement of the Gibson Patent is and has been knowing, deliberate, and willful. Renesas learned of its infringement of the Gibson Patent no later than September 14, 2015. As detailed above, Bell Semic and Avago sent letters, corresponded, and/or met with Renesas at least on September 14, 2015, December 21, 2017, and March 21, 2019, identifying the Gibson Patent as being infringed by Renesas's exemplary Gibson Accused Products. Despite these efforts, and knowing that it was willfully infringing the Gibson Patent, Renesas continued, and continues, to commit acts of direct and indirect infringement despite knowing its actions constitute infringement of the valid and enforceable Gibson Patent, despite a risk of infringement that was known or so obvious that it should have been known to Renesas, and/or even though Renesas otherwise knew or should have known that its actions constituted an unjustifiably high risk of infringement of that valid and enforceable patent. Under these circumstances, Renesas's conduct is and has been egregious. Renesas's knowing, deliberate, and willful infringement of the Gibson Patent entitles Bell Semic to increased damages under 35 U.S.C. § 284, and attorney fees and costs from prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

Plaintiff prays for the following relief:

- A. A judgment that Defendants have infringed one or more claims of the Asserted Patents;
- B. A permanent injunction enjoining Defendants and their officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in active concert or participation with Defendants, from infringing the Gibson Patent;
- C. An award of damages resulting from Defendants' acts of infringement in accordance with 35 U.S.C. § 284;
- D. A judgment and order finding that Defendants' acts of infringement were egregious and willful and trebling damages under 35 U.S.C. § 284;
- E. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Plaintiff its reasonable attorneys' fees against Defendants.
- F. A judgment and order requiring Defendants to provide accountings and to pay supplemental damages to Plaintiff, including, without limitation, prejudgment and post-judgment interest; and
- G. Any and all other relief to which Plaintiff may show itself to be entitled.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Dated: March 16, 2021

/s/ Charles C. Koole

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Attorneys for Plaintiff
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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the above and foregoing document was served on March 16, 2021, via the Case Management/Electronic Case Filing (“CM/ECF”) system, which will send a Notice of Electronic Filing to all CM/ECF participants that have appeared in this action.

/s/ Charles C. Koole
Charles C. Koole