IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

FG SRC LLC, Plaintiff, v. XILINX, INC., Defendant.	Case No. 1:20-cv-00601-LPS JURY TRIAL DEMANDED

PLAINTIFF'SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff FG SRC LLC ("SRC") files this Second Amended Complaint for Patent Infringement ("Second Amended Complaint") against Defendant Xilinx, Inc. ("Defendant" or "Xilinx"). Plaintiff alleges as follows:

I. NATURE OF THE ACTION

1. This is an action for infringement of U.S. Patent No. 9,153,311 (the "'311 patent").

2. SRC is a limited liability company incorporated in Delaware and is the successor to SRC Computers, LLC ("SRC Computers").

3. Xilinx, Inc. is a Delaware corporation with its principal place of business located at 2100 Logic Drive, San Jose, California 95154.

II. JURISDICTION

4. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.*, including 35 U.S.C. §§ 271, 281, 283, 284, and 285. This is a patent infringement lawsuit, over which this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has general and specific personal jurisdiction over Defendant because it is present in and transacts and conducts business in and with residents of this District and the

State of Delaware. Defendant is incorporated in the State of Delaware and has conducted and does conduct business therein. Defendant has purposefully and voluntarily availed itself of the privileges of conducting business in the United States and the State of Delaware by continuously and systematically placing goods into the stream of commerce through a distribution channel with the expectation that they will be purchased by consumers in Delaware. Plaintiff's causes of action arise directly from Defendant's business contacts and other activities in the State of Delaware.

6. Upon information and belief, Defendant has committed acts of infringement in this District giving rise to this action and does business in this District, including making sales and/or providing services and support for its customers in this District. Defendant purposefully and voluntarily sold one or more of its infringing products with the expectation that they would be purchased by consumers in this District. These infringing products have been and continue to be purchased by consumers in this District.

III. VENUE

7. Venue is proper as to Defendant under 28 U.S.C. § 1400(b) in that Defendant is incorporated in Delaware and, therefore, resides in this District. *TC Heartland LLC v. Kraft Foods Grp. Brands LLC*, 137 S. Ct. 1514, 1521 (2017).

IV. FG SRC LLC AND DEFENDANT'S PRODUCTS

A. FG SRC LLC

8. SRC Computers was co-founded by Seymour R. Cray, Jim Guzy, and Jon Huppenthal in 1996 to produce unique high-performance computer systems using Intel's Merced microprocessor.

9. SRC is the successor to SRC Computers.

10. Jim Guzy is a co-founder of Intel Corporation and served on Intel's board for 38 years.

11. Mr. Guzy was named to Forbes Midas List, which surveys the top tech deal makers in the world, in 2006 and 2007.

12. Seymour Cray was an American electrical engineer and supercomputer architect who designed a series of computers that were the fastest in the world for decades.

13. Mr. Cray has been credited with creating the supercomputing industry.

14. Unfortunately, Mr. Cray died shortly after founding SRC Computers.

15. But his legacy was carried on by Jon Huppenthal and a talented team of engineers that worked with Mr. Cray and Mr. Huppenthal for decades.

16. SRC Computers' focus was creating easy-to-program, general-purpose reconfigurable computing systems.

17. In early 1997, Mr. Huppenthal and his team realized that the microprocessors of the day had many shortcomings relative to the custom processing engines that they were used to.

18. As a result, they decided to incorporate dedicated processing elements built from Field Programmable Gate Arrays ("FPGAs") and that idea quickly evolved into a novel system combining reconfigurable processors and Central Processing Units ("CPUs").

19. SRC Computers' heterogenous system had 100x performance, 1/50th of the operating expense, 1/100th of the power usage, and required 1/500th of the space of more traditional computer systems.

20. SRC Computers' proven systems are used for some of the most demanding military and intelligence applications, including the simultaneous real-time processing and analysis of radar, flight and mission data collected from a variety of aerial vehicles in over 1,000 successful counter-terrorism and counter-insurgency missions for the U.S. Department of Defense.

21. SRC Computers offered its first commercial product in 2015 called the Saturn 1 server.

22. The Saturn 1 was 100 times faster than a server with standard Intel microprocessors while using one percent of the power.

23. The Saturn 1 was designed to be used in HP's Moonshot server chassis for data centers.

24. SRC Computers has had over 30 U.S. patents issued for its innovative technology.

25. SRC Computers' patent portfolio covers numerous aspects of reconfigurable computing and has more than 2,090 forward citations.

26. In February 2016, SRC Computers restructured into three new entities: a corporate parent FG SRC LLC, an operating company DirectStream, LLC ("DirectStream"), and a licensing entity SRC Labs, LLC ("SRC Labs").

B. Accused Products

27. In this Second Amended Complaint, Plaintiff accuses the following Xilinx products (collectively "Accused Products") of infringing the '311 patent. For clarity, accused product families are listed, as are exemplary device names and/or part numbers or part number prefixes.

Product Family	**Exemplary Device Names**	**Exemplary Part Numbers and/or Part Number Prefixes**
Alveo accelerator cards	U25, U200, U250, U280, SN1022 (aka SN1000)	
Kintex UltraScale+ Evaluation Kit	KCU116	
Virtex UltraScale+ Evaluation Kit	VCU118	
Zynq UltraScale+ Evaluation Kits and Characterization Kits	ZCU102, ZCU104, ZCU106, ZCU111, ZCU208, ZCU216, ZCU1275, ZCU1285	
Kintex UltraScale Evaluation Kit	KCU105	
Virtex UltraScale Evaluation Kit	VCU108	
Virtex-7 Evaluation Kits and Connectivity Kits	VC707, VC709	

Product Family	**Exemplary Device Names**	**Exemplary Part Numbers and/or Part Number Prefixes**
Zynq-7000 Evaluation Kits	ZC702, ZC706	
Kintex UltraScale+ FPGA devices	KU3P, KU5P, KU9P, KU11P, KU13P, KU15P, KU19P	
Virtex UltraScale+ FPGA devices	VU3P, VU5P, VU7P, VU9P, VU11P, VU13P, VU19P, VU23P, VU27P, VU29P, VU31P, VU33P, VU35P, VU37P, VU45P, VU47P, VU57P	
Zynq UltraScale+ MPSoC: CG devices	ZU2CG, ZU3CG, ZU4CG, ZU5CG, ZU6CG, ZU7CG, ZU9CG	
Zynq UltraScale+ MPSoC: EG devices	ZU2EG, ZU3EG, ZU4EG, ZU5EG, ZU6EG, ZU7EG, ZU9EG, ZU11EG, ZU15EG, ZU17EG, ZU19EG	
Zynq UltraScale+ MPSoC: EV devices	ZU4EV, ZU5EV, ZU7EV	
Zynq Ultrascale+ RFSoC devices	ZU21DR, ZU25DR, ZU27DR, ZU28DR, ZU29DR, ZU39DR, ZU42DR, ZU43DR, ZU46DR, ZU47DR, ZU48DR, ZU49DR	
Kintex UltraScale FPGA devices	KU025, KU035, KU040, KU060, KU085, KU095, KU115	
Virtex UltraScale FPGA devices	XCVU065, XCVU080, XCVU095, VCVU125, XCVU160, XCVU190, XCVU440	
Spartan 7-Series FPGA devices		XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
Artix 7-Series FPGA devices		XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T
Kintex 7-Series FPGA devices		XC7K70T, XC7K160T, XC7K325T, XCE7K325T, XC7K355T, XCE7K355T, XC7K410T, XCE7K410T,

Product Family	**Exemplary Device Names**	**Exemplary Part Numbers and/or Part Number Prefixes**
		XC7K420T, XCE7K420T, XC7K480T, XCE7K480T
Virtex 7-Series FPGA devices		XC7V585T, XCE7V585T, XC7V2000T, XC7VX330T, XCE7VX330T, XC7VX415T, XCE7VX415T, XC7VX485T, XCE7VX485T, XC7VX550T, XCE7VX550T, XC7VX690T, XCE7VX690T, XC7VX980T, XCE7VX980T, XCVX1140T, XC7VH580T, XC7VH870T
Zynq-7000 SoC devices	Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, Z-7020, Z-7030, Z-7035, Z-7045, Z-7100	XC7Z007S, XC7Z012S, XC7Z014S, XC7Z010, XC7Z015, XC7Z020, XC7Z030, XC7Z035, XC7Z045, XC7Z100

28. Each of the Accused Products includes an FPGA.

29. In contrast to a purpose-built chip which is designed with a single function in mind and then hardwired to implement it, an FPGA is more flexible.

30. An FPGA can be programmed in the field, after it has been plugged into a socket on a PC board.

31. FPGAs are based around a matrix of configurable logic blocks ("CLBs") connected via programmable interconnects.

32. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks.

33. Today's FPGAs easily push the 500 MHz performance barrier.

34. Programming an FPGA is a matter of connecting CLBs to create the desired logical functions (AND, OR, XOR, and so forth) or storage elements (flip-flops and shift registers).

35. Unlike a CPU which is primarily serial (with a few parallel elements) and has fixed-size instructions and data paths (typically 32 or 64 bit), an FPGA can be programmed to perform many operations in parallel, and the operations themselves can be of almost any width, large or small.

36. The highly parallelized model in FPGAs is ideal for building custom accelerators to process compute-intensive problems.

37. An FPGA has the potential to provide a 30x or greater speedup to many types of genomics, seismic analysis, financial risk analysis, big data search, and encryption algorithms and applications.

38. The Alveo U200 provides up to 90x higher performance than CPUs on key workloads at 1/3 the cost. *See* https://www.xilinx.com/publications/product-briefs/alveo-product-brief.pdf.

39. The Alveo U280 provides up to 3,000 times higher throughput than CPUs on key workloads such as Key-Value-Store. *See* https://www.xilinx.com/publications/product-briefs/alveo-u280-product-brief.pdf.

40. Defendant's customers can use FPGAs to accelerate its applications more than 30x when compared with servers that use CPUs alone.

41. The speed increases referenced in the prior four paragraphs are a result of the FPGAs handling compute-intensive, deeply pipelined, hardware-accelerated operations, which also allows for highly parallelized computing.

V. MARKING AND NOTICE

A. Marking and Constructive Notice to Defendant.

42. SRC Computers complied with 35 U.S.C. § 287 by (i) placing the required notice on all, or substantially all, of its products made, offered for sale, sold, or imported into the United States, or (ii) providing actual notice to Defendant.

43. For example, SRC Computers placed notices such as the following on all, or substantially all, of its products since at least February 19, 2013:[1]

44. The website listed in the notice, WWW.SRCCOMP.COM/ TECHPUBS/PATENTEDTECH.ASP, stated the following:

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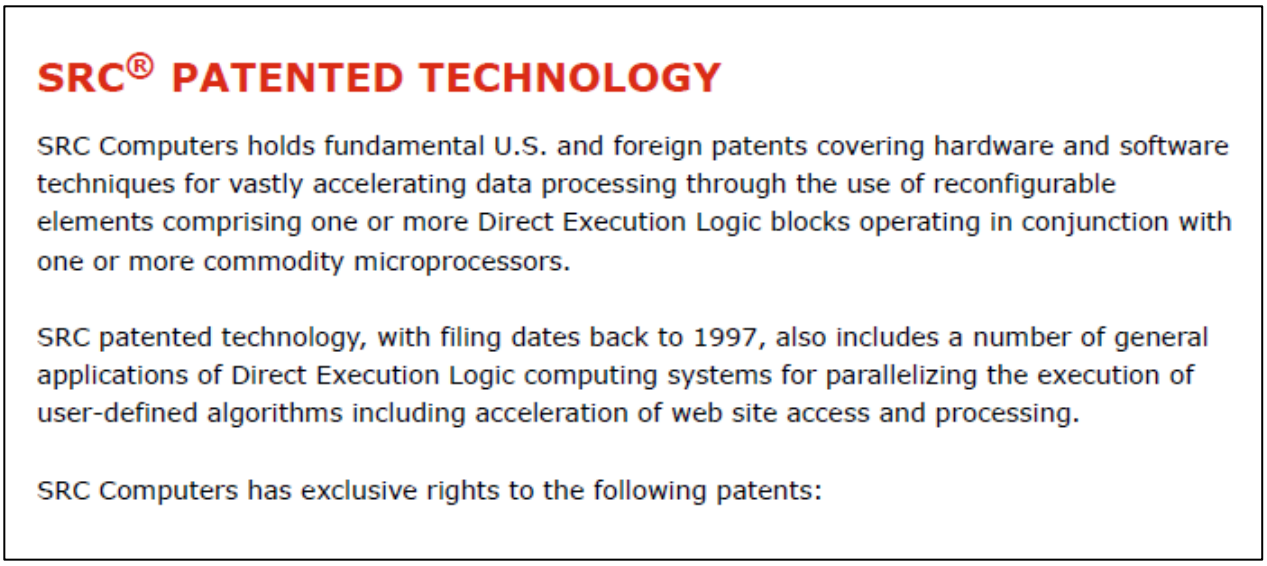
[1] *E.g.,* https://web.archive.org/web/20100930014237/http://www.srccomp.com/techpubs/patentedtech.asp.



SRC® PATENTED TECHNOLOGY

SRC Computers holds fundamental U.S. and foreign patents covering hardware and software techniques for vastly accelerating data processing through the use of reconfigurable elements comprising one or more Direct Execution Logic blocks operating in conjunction with one or more commodity microprocessors.

SRC patented technology, with filing dates back to 1997, also includes a number of general applications of Direct Execution Logic computing systems for parallelizing the execution of user-defined algorithms including acceleration of web site access and processing.

SRC Computers has exclusive rights to the following patents:

B. Actual Notice to Defendant.

45. Xilinx is well-aware of the patent asserted in this action and that instrumentalities accused herein infringe that patent.

46. On or around February 22, 2013, counsel for SRC Computers sent a notice letter to Xilinx advising that "Our client has recently become aware of Xilinx' Zynq-7000 All Programmable SoC devices which are stated to integrate an ARM® dual-core Cortex™-A9 CPU as an application processor unit in conjunction with programmable logic. From the information presently available to us, these devices may possibly involve SRC Computers' patented technology."

47. Between July 2015 and November 2015 SRC Computers and Xilinx communicated regarding a potential acquisition by Xilinx of SRC Computers and/or its intellectual property ("IP"). Persons involved on behalf of Xilinx included Greer Person, Ron Satori, Nate Gazdik, Michael White, and Ivo Bolsens. Persons involved on behalf of SRC Computers included Brandon Freeman and Jon Huppenthal.

48. A third party, 3LP Advisors, LLC ("3LP"), assisted with discussions on behalf of SRC Computers.

49. In order to assist Xilinx with reviewing SRC Computers' patent portfolio, 3LP provided Xilinx with a list of SRC Computers' IP on or around October 1, 2015.

50. On October 18, 2017, SRC Labs sued Amazon Web Services, Inc., Amazon.com, Inc., and VADATA, Inc. (collectively the "Amazon Defendants") alleging infringement of five patents, including the '311 patent. *SRC Labs, LLC v. Amazon Web Services, Inc.*, No. 1-17-cv-01227 (E.D. Va.). The complaint (the "Amazon Complaint") filed in that case (the "Amazon Case") alleged that the Amazon Defendants' products infringed the '311 patent based on usage of Xilinx FPGA products.

51. Moreover, specifically, the Amazon Complaint included—as Exhibit J—a publicly-available claim chart showing how the Amazon Defendants' product EC2 F1 Instance infringed the '311 patent based on its usage of a Xilinx UltraScale+ FPGA. Plaintiff accuses that device of infringing the '311 patent in this Second Amended Complaint and accused said device of infringement in its Original Complaint and First Amended Complaint.

52. On or around January 8, 2018, SRC Labs, LLC served Xilinx with a subpoena in the Amazon Case. That subpoena explicitly referenced the '311 patent, providing Xilinx with further notice of the patent.

53. After learning of the '311 patent, and that its products infringed that patent, on July 13, 2018 Xilinx filed a petition for *inter partes* review, requesting that the Board of Patent Trials and Appeals cancel claims 1 through 5 and 8 through 10 of the '311 patent. IPR2018-01395 (hereinafter "the Xilinx IPR"), Paper No. 1. In its petition, Xilinx noted the complaint against the Amazon Defendants and admitted that "Amazon and Xilinx have a customer/supplier

relationship" and that "Xilinx Ultrascale+ FPGAs and its Vivado Design Suite are referenced in the SRC Labs complaint . . ." That petition was denied on January 23, 2019. IPR201801395, Paper No. 17.

54. The district court case against the Amazon Defendants was transferred to the Western District of Washington on March 1, 2018. *SRC Labs, LLC et al v. Amazon Web Services*, Inc., No. 2-18-cv-00317 (W.D. Wa.).

VI. THE PATENT

A. Asserted Patent is Owned by SRC.

55. On January 22, 2020, DirectStream assigned both the '311 patent to SRC. The assignment was recorded with the USPTO on January 24, 2020 at Reel/Frame 051615/0344.

56. All maintenance fees have been paid to the USPTO to keep the '311 patent enforceable for its full term.

B. Description of the Asserted Patent.

57. The '311 patent is entitled "System and method for retaining DRAM data when reprogramming reconfigurable devices with DRAM memory controllers" and issued on October 6, 2015.

58. A true and correct copy of the '311 patent is attached as **Exhibit A**.

59. The '311 patent is valid and enforceable.

VII. COUNT ONE: DIRECT INFRINGEMENT OF THE '311 PATENT

60. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

61. Defendant has at no time, either expressly or impliedly, been licensed under the '311 patent.

62. Defendant has and continues to directly infringe the '311 patent by making, using, offering for sale, selling, and/or importing in or into the United States in violation of 35 U.S.C.

§ 271(a) the Accused Products. For example, on information and belief Defendant tests, manufactures, and uses each of the Accused Products in an infringing manner at least in order to (1) ensure that functionality such as that appearing in SRC's claim charts attached hereto, including but not limited to those portions of the charts describing partial reconfiguration, works as described and (2) provide support regarding said reconfiguration to its customers, members of its Partner Program, such as its Premier Partners, Certified Partners, Alliance Partners, and Accelerator Partners (*see* https://www.xilinx.com/alliance.html) and members of its University Program (*see* https://www.xilinx.com/support/university.html).

63. Defendant's direct infringement of the '311 patent by the Accused Products has caused, and will continue to cause, substantial and irreparable damage to Plaintiff. Plaintiff is therefore entitled to an award of damages adequate to compensate for Defendant's infringement, but not less than a reasonable royalty, together with pre- and post-judgment interest and costs as fixed by the Court under 35 U.S.C. § 284.

64. Plaintiff adopts, and incorporates by reference, as if fully stated herein, **Exhibits B through E**, which are claim charts that describe and demonstrate how the Accused Products infringe exemplary claims of the '311 patent. These charts collectively show that Xilinx infringes at least claims 1, 3, 9, and 10 of the '311 patent.

VIII. COUNT TWO: INDIRECT INFRINGEMENT OF THE '311 PATENT

65. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

66. Defendant induces infringement under 35 U.S.C. § 271(b) by actively and knowingly aiding and abetting direct infringement by its users.

67. As discussed in § V.B, Defendant received actual and constructive notice of the '311 patent.

68. Defendant learned of its infringement of the '311 patent at least as a result of the filing of the Original Complaint and the First Amended Complaint in this case as well as the filing of this Second Amended Complaint.

69. Defendant also learned that its products infringe the '311 patent as a result of the Amazon Complaint and/or the Amazon Case.

70. Through at least the filing of the Original Complaint, the First Amended Complaint, and this Second Amended Complaint, and the claim charts attached to those complaints, Defendant learned that its actions would result in users of the Accused Products infringing the '311 patent.

71. For example, the claim charts attached to the complaints show how Defendant's UltraScale Architecture-Based FPGA's Memory IP v1.4 LogiCORE IP Product Guide, PG150 provides explicit instructions on using the '311 Accused Products in an infringing manner, such as through partial reconfiguration.

72. Defendant's UltraScale Architecture-Based FPGA's Memory IP v1.4 LogiCORE IP core described in its UltraScale Architecture-Based FPGA's Memory IP v1.4 LogiCORE IP Product Guide, PG150 provides a complete solution for interfacing external DRAM memories to the user FPGA logic. One component of this Memory IP is a memory controller with a maintenance block – both are implemented as part of the reconfigurable processor (FPGA). One of the functions this maintenance block supports is "Self Refresh." The "Self Refresh" feature keeps the DRAM in self-refresh mode; for instance, during partial reconfiguration.

73. Moreover, Defendant provides guides such as that described above, as well as training and support to its customers, members of its Partner Program, such as its Premier Partners, Certified Partners, Alliance Partners, and Accelerator Partners (*see*

https://www.xilinx.com/alliance.html) and members of its University Program (*see* https://www.xilinx.com/support/university.html).

74. Xilinx teaches users to use the Accused Products in an infringing manner, such as that shown by partial reconfiguration in SRC's claim charts.

75. Xilinx actively provides support services for its products. An important part of Xilinx's support services is the Xilinx Community Portal. *See* https://www.xilinx.com/community.html. Xilinx hosts forums where members can ask questions and receive support both from Xilinx engineers and fellow members.

76. Defendant induces infringement of the '311 patent by marketing the Accused Products and providing LogiCORE IP cores, documentation (i.e., the UltraScale Architecture-Based FPGA's Memory IP v1.4 LogiCORE IP Product Guide, PG150), training, and support (i.e. through its Partner Program, and support for non-program members) on how to use said products in ways that infringe the '311 patent.

77. For example, Defendant induces infringement by providing Kits that allow users to develop, simulate, debug, and compile FGPA applications. Defendant actively provides support services for its Kits, and other products, directly and through its Community Forum, in which Xilinx engineers provide support to users.

78. Defendant specifically intends for users of its products to infringe and knows that its acts will result in patent infringement.

IX. COUNT SIX: WILLFUL INFRINGEMENT OF THE '311 PATENT

79. Plaintiff incorporates by reference all paragraphs above as though set forth herein.

80. Defendant has and continues to willfully infringe the '311 patent.

81. As discussed in § V.B herein, Defendant has long had knowledge of the '311 patent and that its products infringe that patent.

82. Even if Defendant had not had such knowledge previously, Defendant would learn of the '311 patent and its infringement as a result of the filing of Plaintiff's Original Complaint, the First Amended Complaint, and this Second Amended Complaint, and this district does not require pre-suit knowledge to establish willfulness. *DermaFocus LLC v. Ulthera, Inc.*, 201 F. Supp. 3d 465, 473 (D. Del. 2016).

83. Despite knowing of the '311 patent, Defendant continued and continues making, using, offering for sale, and selling the Accused Products resulting in infringement as discussed in Counts One and Two herein. At least because of its knowledge of the '311 patent and its claims, Defendant knew or should have known that its conduct resulted in infringement of several claims of the '311 patent. Moreover, Defendant was provided information regarding its infringement in the Original Complaint, the First Amended Complaint, and this Second Amended Complaint.

84. Defendant has continued its infringement of the '311 patent despite its knowing that claims 1 through 5 and 8 through 10 of the '311 patent were held valid on January 23, 2019 in the Xilinx IPR.

85. Therefore, Defendant's infringement was intentional or knowing. Defendant knows or should know that its continued activities result in infringement of the '311 patent.

86. Defendant's actions have not been consistent with the standards of behavior in its industry.

87. Defendant made no effort to avoid infringing the '311 patent.

88. Defendant's infringement of the '311 patent is willful, deliberate, and/or consciously wrongful, and therefore Plaintiff should receive enhanced damages up to three times the amount of actual damages for Defendant's willful infringement under 35 U.S.C. § 284.

X. CONCLUSION

89. Plaintiff is entitled to recover from Defendant the damages sustained by SRC as a result of Xilinx's wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

90. Plaintiff has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action.

91. Plaintiff reserves the right to amend, supplement, or modify its allegations of infringement as facts regarding such allegations arise during the course of this case.

XI. JURY DEMAND

92. Plaintiff hereby demands a trial by jury for all causes of action.

XII. PRAYER FOR RELIEF

Plaintiff requests the following relief:

A. A judgment that Defendant has infringed and continues to infringe the '311 patent;

B. A judgment and order requiring Defendant to pay Plaintiff damages under 35 U.S.C. § 284, including treble damages for willful infringement as provided by 35 U.S.C. § 284, and supplemental damages for any continuing post-verdict infringement up until entry of the final judgment with an accounting as needed;

C. A judgment and order requiring Defendant to pay Plaintiff pre-judgment and post-judgment interest on the damages awarded;

D. A judgment and order awarding a compulsory ongoing royalty; and

E. Such other and further relief as the Court deems just and equitable.

Dated: March 18, 2021

Respectfully submitted,

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EXHIBIT A

US009153311B1

(12) **United States Patent**
Tewalt

(10) **Patent No.: US 9,153,311 B1**
(45) **Date of Patent: Oct. 6, 2015**

(54) **SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS**

(71) Applicant: **SRC Computers, LLC.**, Colorado Springs, CO (US)

(72) Inventor: **Timothy J. Tewalt**, Larkspur, CO (US)

(73) Assignee: **SRC Computers, LLC**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/288,094**

(22) Filed: **May 27, 2014**

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/406 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 11/40615*** (2013.01)

(58) **Field of Classification Search**
USPC 365/222
See application file for complete search history.

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(Continued)

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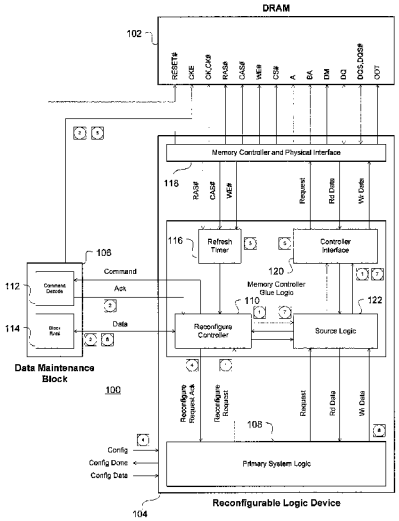
(Continued)

Primary Examiner — Hoai V Ho
(74) *Attorney, Agent, or Firm* — Peter J. Meza; William J. Kubida; Hogan Lovells US LLP

(57) **ABSTRACT**

A system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers such as field programmable gate arrays (FPGAs). The DRAM memory controller is utilized in concert with an internally or externally located data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

19 Claims, 2 Drawing Sheets



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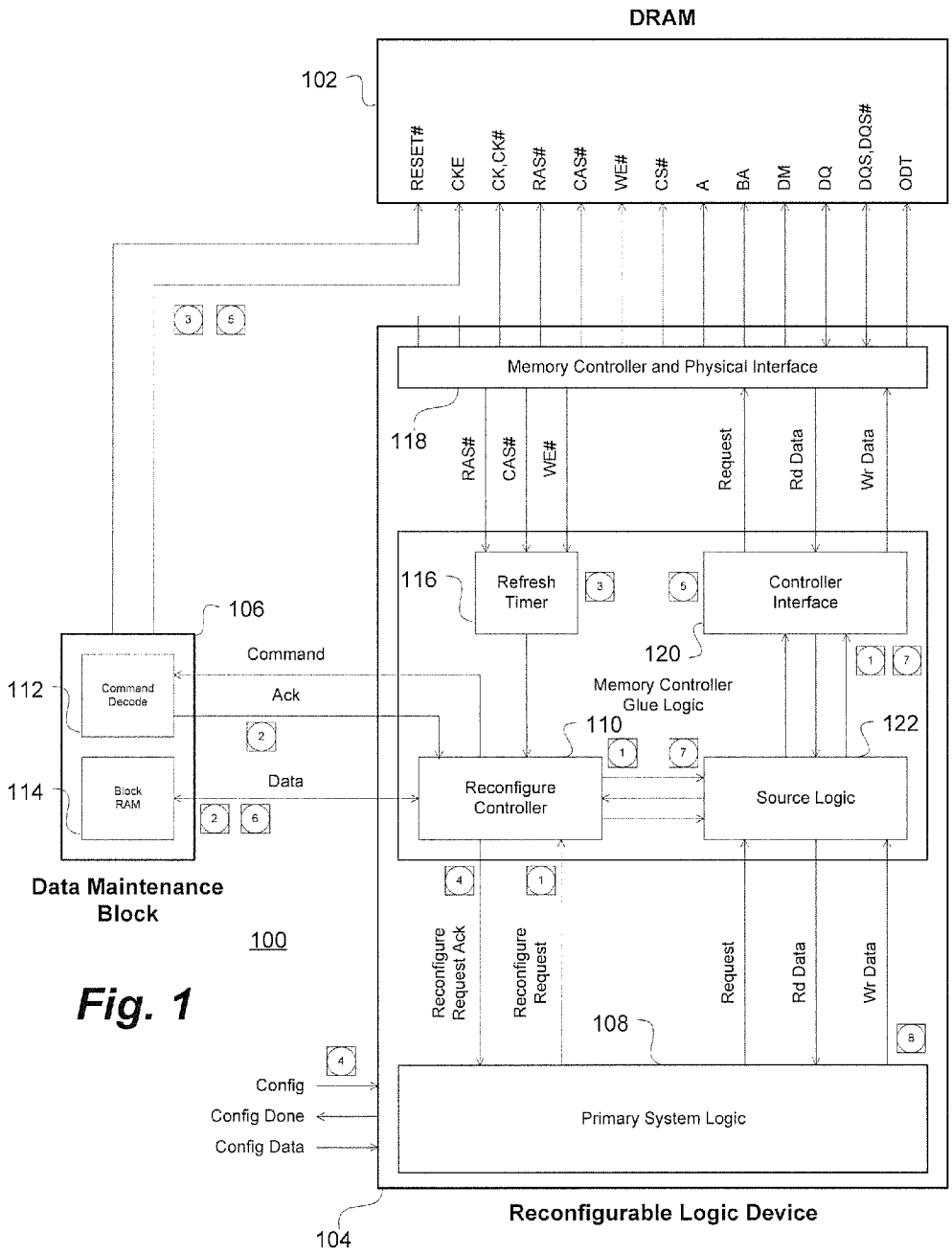

DRAM
102
RESET#
CKE
CK,CK#
RAS#
CAS#
WE#
CS#
A
BA
DM
DQ
DQS,DQS#
ODT
Memory Controller and Physical Interface
118
RAS#
CAS#
WE#
Request
Rd Data
Wr Data
116
Refresh Timer
Controller Interface
120
Memory Controller Glue Logic
110
122
Reconfigure Controller
Source Logic
106
Command
Ack
Data
112
Command Decode
114
Block RAM
Data Maintenance Block
100
Reconfigure Request Ack
Reconfigure Request
Request
Rd Data
Wr Data
108
Primary System Logic
Config
Config Done
Config Data
104
Reconfigurable Logic Device

Fig. 1

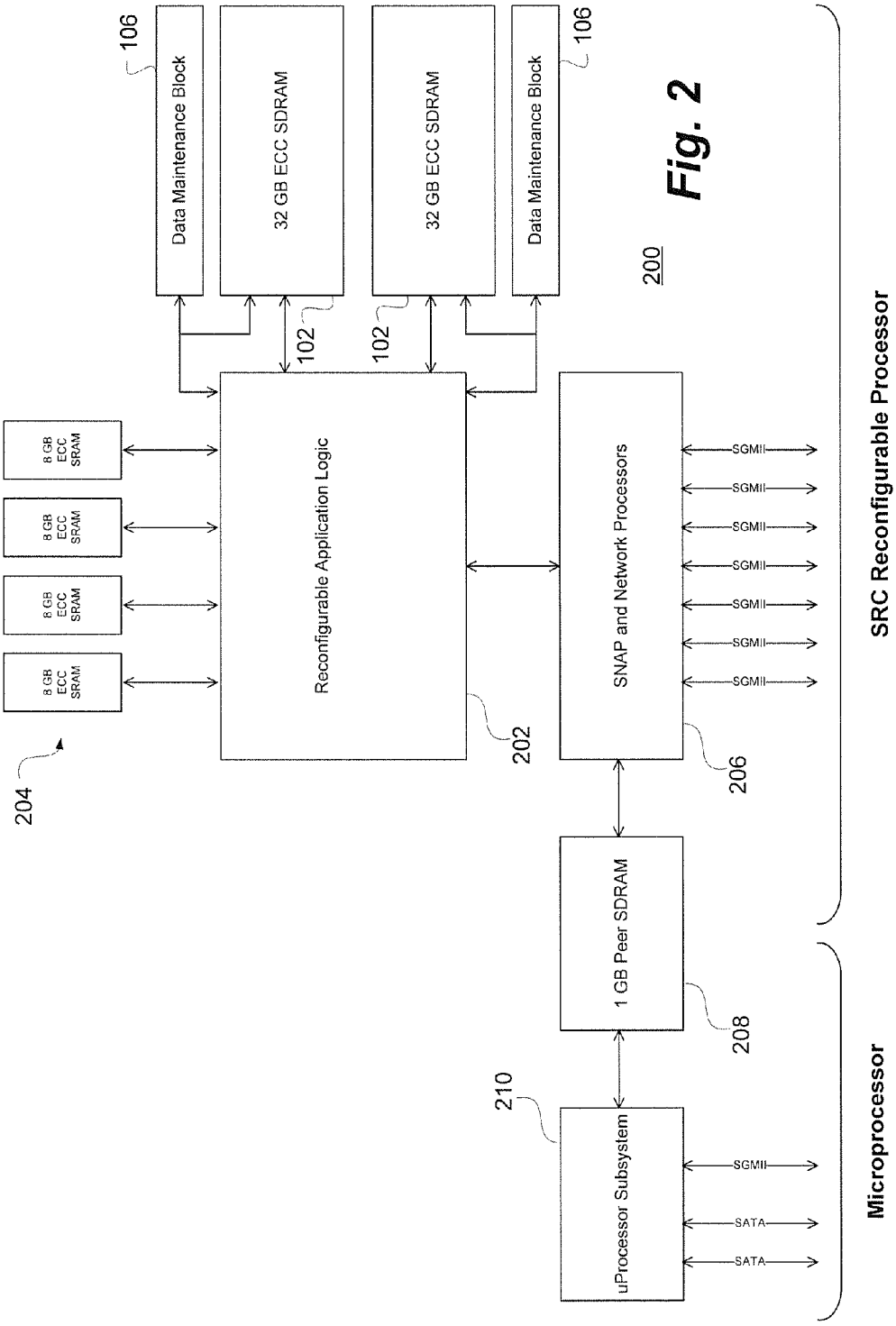

106
Data Maintenance Block
32 GB ECC SDRAM
32 GB ECC SDRAM
Data Maintenance Block
106
200
102
102
8 GB ECC SRAM
8 GB ECC SRAM
8 GB ECC SRAM
8 GB ECC SRAM
Reconfigurable Application Logic
SNAP and Network Processors
SGMII
SGMII
SGMII
SGMII
SGMII
SGMII
204
202
206
SRC Reconfigurable Processor
1 GB Peer SDRAM
208
210
uProcessor Subsystem
SGMII
SATA
SATA
Microprocessor

Fig. 2

SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS

BACKGROUND OF THE INVENTION

The present invention relates, in general, to the field of reconfigurable computing systems. More particularly, the present invention relates to a system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers.

The majority of today's programmable logic designs include a DRAM based memory solution at the heart of their memory subsystem. Today's DRAM devices are significantly faster than previous generation's, albeit at the cost of requiring increasingly complex and resource intensive memory controllers. One example is in double data rate 3 and 4 (DDR3 and DDR4) controllers which require read and write calibration logic. This added logic was not necessary when using previous versions of DRAM (e.g. DDR and DDR2. As a result, companies are forced to absorb substantial design costs and increased project completion times when designing proprietary DRAM controllers utilizing modern DRAM technology.

In order to mitigate design engineering costs and verification time, it is very common for field programmable gate array (FPGA) designers to implement vendor provided memory controller intellectual property (IP) when including DRAM based memory solutions in their designs. See, for example, Allan, Graham; "DDR IP Integration: How to Avoid Landmines in this Quickly Changing Landscape"; Chip Design, June/July 2007; pp 20-22 and Wilson, Ron; "DRAM Controllers for System Designers"; Altera Corporation Articles, 2012.

FPGA designers tend to choose device manufacturer IP designs because they are proven, tested and have the incredible benefit of significantly reduced design costs and project completion times. Many times there is the added benefit of exploiting specialized circuitry within the programmable device to increase controller performance, which is not always readily apparent when designing a controller from scratch.

The downside to using factory supplied IP memory controllers is that there is little flexibility when trying to modify operating characteristics. A significant problem arises in reconfigurable computing when the FPGA is reprogrammed during a live application and the memory controller tri-states all inputs and outputs (I/O) between the FPGA device and the DRAM. The result is corrupted data in the memory subsystem. Therefore, dynamically reconfigurable processors are excluded as viable computing options, especially in regard to database applications or context switch processing. The reason for this is that the time it takes to copy the entire contents of DRAM data and preserve it in another part of the system, reconfigure the processor, then finally retrieve the data and restore it in DRAM is just too excessive.

SUMMARY OF THE INVENTION

Disclosed herein is a system and method for preserving DRAM memory contents when a reconfigurable device, for example an FPGA having a DRAM memory controller, is reconfigured, reprogrammed or otherwise powered down. When an FPGA is reprogrammed, the DRAM inputs are tri-stated including self-refresh command signals. Indeterminate states on the reset or clock enable inputs results in DRAM data corruption.

In accordance with the system and method of the present invention, an FPGA based DRAM controller is utilized in concert with an internally or externally located data maintenance block. In operation, the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

Functionally, the data maintenance block does not contain the memory controller and therefore has no point of reference for when and how to initiate the self-refresh commands, particularly the DRAM self-refresh mode. As also disclosed herein, a communication port is implemented between the FPGA and the data maintenance block that allows the memory controller in the FPGA to direct the self-refresh commands to the DRAM via the data maintenance block. Specifically, this entails when to put the DRAM into self-refresh mode and preserve the data in memory.

At this point, the DRAM data has been preserved throughout the FPGA reconfiguration via the self-refresh mode initiated by the data maintenance block, but the DRAM controller must now re-establish write/read timing windows and will corrupt specific address contents with guaranteed write and read data required during the calibration/leveling process. Consequently, using the self-refresh capability of DRAM alone is not adequate for maintaining data integrity during reconfiguration. (It should be noted that the memory addresses used during calibration/leveling are known and typically detailed in the controller IP specification).

In order to effectuate this, the system transmits a "reconfiguration request" to the DRAM controller. Once received, glue logic surrounding the FPGA vendor provided memory controller IP issues read requests to the controller specifying address locations used during the calibration/leveling process. As data is retrieved from the DRAM, it is transmitted via the communication port from the FPGA device to a block of storage space residing within the data maintenance block itself or another location in the system.

Once the process is complete, the data maintenance block sends a self-refresh command to the DRAM and transmits an acknowledge signal back to the FPGA. The data maintenance block recognizes this as an FPGA reconfiguration condition versus an FPGA initial power up condition and retains this state for later use.

Once the FPGA has been reprogrammed, the DRAM controller has re-established calibration settings and several specific addresses in the DRAM have been corrupted with guaranteed write/read data patterns. At this point, glue logic surrounding the vendor memory controller IP is advised by the data maintenance block (through the communication port) that it has awakened from either an initial power up condition or a reconfiguration condition. If a reconfiguration condition is detected, and before processing incoming DMA requests, the controller retrieves stored DRAM data from the data maintenance block (again through the communication port) and writes it back to the specific address locations corrupted during the calibration/leveling process. Once complete, the DRAM controller in the FPGA is free to begin servicing system memory requests in the traditional fashion.

Among the benefits provided in conjunction with the system and method of the present invention is that since the data maintenance block functions to hold the DRAM in self-refresh mode, the FPGA is free to be reprogrammed to perform

a very application-specific computing job that may not require DRAM. This means all the device resources previously reserved for creating a DRAM controller are now free to be used for different functions.

Further, the overall computer system benefits from the present invention because data previously stored in DRAM has now been preserved and is available for use by the next application that needs it. This leads to the fact that computing solutions requiring a series of specific data manipulation tasks now have the ability to be implemented in a small reconfigurable processor. Each application performs its intended function and data is passed from application to application between reconfiguration periods via the DRAM.

Importantly, it should also be noted that the DRAM data contents are retained even if the reconfigurable device is powered down. This is especially critical, for example, when the system and method of the present invention is implemented in mobile devices.

Particularly disclosed herein is a system and method for preserving DRAM data contents when reconfiguring a device containing one or more DRAM controllers. Also particularly disclosed herein is a system and method for preserving DRAM data contents in a reconfigurable computing environment when the programmable device is reconfigured with a new design that does not include a DRAM controller. Further disclosed herein is a system and method for passing DRAM data between sequential computing tasks in a reconfigurable computing environment as well as system and method for preserving DRAM contents when the reconfigurable device is powered down.

Also particularly disclosed herein is a computer system which comprises a DRAM memory, a reconfigurable logic device having a memory controller coupled to selected inputs and outputs of the DRAM memory and a data maintenance block coupled to the reconfigurable logic device and self-refresh command inputs of the DRAM memory. The data maintenance block is operative to provide stable input levels on the self-refresh command inputs while the reconfigurable logic device is reconfigured.

Still further particularly disclosed herein is a method for preserving the contents of a DRAM memory associated with a reconfigurable device having a memory controller. The method comprises providing a data maintenance block coupled to the reconfigurable device, coupling the data maintenance block to self-refresh command inputs of the DRAM memory, storing data received from the reconfigurable device at the data maintenance block and maintaining stable input levels on the self-refresh command inputs while the reconfigurable logic device is reconfigured.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other features and objects of the present invention and the manner of attaining them will become more apparent and the invention itself will be best understood by reference to the following description of a preferred embodiment taken in conjunction with the accompanying drawings, wherein:

FIG. **1** is a functional block diagram of a computer subsystem comprising a reconfigurable logic device having a reconfigurable DRAM controller with associated DRAM memory and illustrating the data maintenance block of the present invention for retaining DRAM data when the logic device is reconfigured; and

FIG. **2** is a block diagram of a reconfigurable computer system, such as that available from SRC Computers, LLC, assignee of the present invention, incorporating a pair of data maintenance blocks and DRAM memory in accordance with the system and method of the present invention in association with reconfigurable application logic.

DESCRIPTION OF A REPRESENTATIVE EMBODIMENT

With reference now to FIG. **1**, a functional block diagram of a computer subsystem **100** comprising a DRAM memory **102** and reconfigurable logic device **104** is shown. In a representative embodiment of the present invention, the reconfigurable logic device **104** may comprise a field programmable gate array (FPGA). However, it should be noted that the reconfigurable logic device **104** may comprise any and all forms of reconfigurable logic devices including hybrid devices, such as a reconfigurable logic device with partial reconfiguration capabilities or an application specific integrated circuit (ASIC) device with reprogrammable regions contained within the chip.

Also illustrated is a data maintenance block **106** in accordance with the present invention for retaining DRAM memory **102** data when the logic device **104** is reconfigured during operation of the computer subsystem **100**. In a representative embodiment of the present invention, the data maintenance block **106** may be conveniently provided as a complex programmable logic device (CPLD) or other separate integrated circuit device or, in alternative embodiments, may be provided as a portion of an FPGA comprising the reconfigurable logic device **104**.

As illustrated, the reconfigurable logic device **104** comprises a primary system logic block **108** which issues a reconfigure request command to a reconfigure controller **110** and receives a reconfigure request acknowledgement (Ack) signal in return. The reconfigure controller **110**, in turn, issues a command to the command decode block **112** of the data maintenance block **106** and receives an acknowledgement (Ack) signal in return. A block RAM portion **114** of the data maintenance block **106** exchanges data with the reconfigure controller **110**.

The reconfigure controller **110** receives an input from a refresh timer **116** which is coupled to receive row address select (RAS#), column address select (CAS#) and write enable (WE#) signals from a memory controller and physical interface block **118**. The memory controller and physical interface block **118** also provides the RAS#, CAS# and WE# signals to the DRAM memory **102** as well as clock (CR, CK#), chip select (CS#), address (A), bank address (BA), data mask (DM) and on-die termination (ODT) input signals. Bididirectional data (DQ) input/output (I/O) and differential data strobe signals (DQS/DQS#) are exchanged between the DRAM memory **102** and the memory controller and physical interface block **118** as shown. The data maintenance block **106** is coupled to the DRAM memory **102** to supply reset (RESET#) and clock enable (CKE#) signals thereto.

The memory controller and physical interface block **118** responds to a request from the controller interface **120** to provide data read from the DRAM memory **102** (Rd Data) and to receive data to be written to the DRAM memory **102** (Wr Data) as shown. A source logic block **122** is coupled to the controller interface **120** as well as the reconfigure controller **110** as also illustrated. The source logic block **122** receives a data request from the primary system logic block **108** and supplies data read from the DRAM memory **102** while receiving data to be written thereto.

As indicated by the operation at numeral **1**, a reconfiguration request is received at the reconfigure controller **110** from the primary system logic block **108** of the reconfigurable

logic device **104**. The reconfigure controller **110** initiates direct memory access (DMA) read requests to memory addresses used in a calibration/leveling sequence after the reconfigurable logic device **104** is reconfigured. Returned data is stored in a small section of block RAM (not shown) in the reconfigure controller **110**.

As indicated by the operation at numeral **2**, the reconfigure Controller **110** stores its block RAM contents in another small section of block RAM **114** located in the data maintenance block **106**. When complete, the data maintenance block **106** asserts an acknowledge signal from its command decode block **112**. At the operation indicated by numeral **3**, the reconfigure controller **110** detects a refresh command from the refresh timer **116**, waits a refresh cycle time (t_{RFC}) and instructs the data maintenance block **106** to de-assert CKE to the DRAM memory **102**.

The reconfigure controller **110** asserts the Reconfigure Request Ack signal at the operation indicated by numeral **4** and the reconfigurable logic device **104** is reconfigured. As indicated by the operation at numeral **5**, the reconfigure controller **110** recognizes a post-reconfigure condition (Ack=High), holds the memory controller and physical interface **118** in reset and instructs the data maintenance block **106** to assert CKE to the DRAM memory **102**. The memory controller and physical interface **118** is then released from reset and initializes the DRAM memory **102**.

At the operation indicated by numeral **6**, the reconfigure controller **110** retrieves the data maintenance block **106** block RAM **114** contents and stores it in a small section of block RAM (not shown) in the reconfigure controller **110**. The reconfigure controller **110** detects that the memory controller and physical interface **118** and DRAM memory **102** initialization is complete at the operation indicated by numeral **7** and initiates DMA write requests to restore the memory contents corrupted during the calibration/leveling sequence with the data values read prior to reconfiguration. At the operation indicated by numeral **8**, the memory controller and physical interface **118** glue logic (comprising reconfigure controller **110**, refresh timer **116**, controller interface **120** and source logic block **122**) resumes DMA activity with the primary system logic **108** in a conventional fashion.

It should be noted certain of the aforementioned operational steps may, in fact, operate substantially concurrently. Further, while functionally accurate, some of the operational steps enumerated have been listed out of order to provide logical continuity to the overall operation and to facilitate comprehensibility of the process. In a particular implementation of the system and method of the present invention, one or more of the operational steps disclosed may be conveniently re-ordered to increase overall hardware efficiency. Moreover, steps which can serve to facilitate relatively seamless integration in an active application can be provided in addition to those described as may be desired.

With reference additionally now to FIG. **2**, a block diagram of a reconfigurable computer system **200** is illustrated incorporating a pair of data maintenance blocks **106** and DRAM memory **102** in accordance with the system and method of the present invention in association with reconfigurable application logic **202**. In this representative embodiment of a reconfigurable computer system **200**, the DRAM memory **102** is illustrated in the form of 32 GB error correction code (ECC) synchronous dynamic random access memory (SDRAM).

The reconfigurable application logic **202** is coupled to the data maintenance blocks **106** and DRAM memory **102** as depicted and described previously with respect to the preceding figure and is also illustrated as being coupled to a number of 8 GB ECC static random access memory (SRAM) memory modules **204**. The reconfigurable application logic **202** is also coupled to an SRC Computers, LLC SNAP™ and network processors block **206** having a number of serial gigabit media independent interface (SGMII) links as shown. It should be noted that the DRAM memory **102** controller in the reconfigurable application block **202** may be omitted upon subsequent reconfigurations as the DRAM memory **102** data contents will be maintained in the data maintenance blocks **106**.

The SNAP and network processors block **206** shares equal read/write access to a 1 GB peer SDRAM system memory **208** along with a microprocessor subsystem **210**. The microprocessor subsystem **210**, as illustrated, also comprises an SGMII link as well as a pair of serial advanced technology attachment (SATA) interfaces.

For continuity and clarity of the description herein, the term "FPGA" has been used in conjunction with the representative embodiment of the system and method of the present invention and refers to just one type of reconfigurable logic device. However, it should be noted that the concept disclosed herein is applicable to any and all forms of reconfigurable logic devices including hybrid devices, inclusive of reconfigurable logic devices with partial reconfiguration capabilities or an ASIC device with reprogrammable regions contained within the chip.

Representative embodiments of dynamically reconfigurable computing systems incorporating the DRAM memory **102**, reconfigurable logic device **104**, associated microprocessors and programming techniques are disclosed in one or more of the following United States Patents and United States Patent Publications to SRC Computers LLC, assignee of the present invention, the disclosures of which are herein specifically incorporated by this reference in their entirety: U.S. Pat. No. 6,026,459; U.S. Pat. No. 6,076,152; U.S. Pat. No. 6,247,110; U.S. Pat. No. 6,295,598; U.S. Pat. No. 6,339,819; U.S. Pat. No. 6,356,983; U.S. Pat. No. 6,434,687; U.S. Pat. No. 6,594,736; U.S. Pat. No. 6,836,823; U.S. Pat. No. 6,941,539; U.S. Pat. No. 6,961,841; U.S. Pat. No. 6,964,029; U.S. Pat. No. 6,983,456; U.S. Pat. No. 6,996,656; U.S. Pat. No. 7,003,593; U.S. Pat. No. 7,124,211; U.S. Pat. No. 7,134,120; U.S. Pat. No. 7,149,867; U.S. Pat. No. 7,155,602; U.S. Pat. No. 7,155,708; U.S. Pat. No. 7,167,976; U.S. Pat. No. 7,197,575; U.S. Pat. No. 7,225,324; U.S. Pat. No. 7,237,091; U.S. Pat. No. 7,299,458; U.S. Pat. No. 7,373,440; U.S. Pat. No. 7,406,573; U.S. Pat. No. 7,421,524; U.S. Pat. No. 7,424,552; U.S. Pat. No. 7,565,461; U.S. Pat. No. 7,620,800; U.S. Pat. No. 7,680,968; U.S. Pat. No. 7,703,085; U.S. Pat. No. 7,890,686; U.S. Pat. No. 8,589,666; U.S. Pat. Pub. No. 2012/0117318; U.S. Pat. Pub. No. 2012/0117535; and U.S. Pat. Pub. No. 2013/0157639.

While there have been described above the principles of the present invention in conjunction with specific apparatus and methods, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it miti-

gates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

As used herein, the terms "comprises", "comprising", or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a recitation of certain elements does not necessarily include only those elements but may include other elements not expressly recited or inherent to such process, method, article or apparatus. None of the description in the present application should be read as implying that any particular element, step, or function is an essential element which must be included in the claim scope and THE SCOPE OF THE PATENTED SUBJECT MATTER IS DEFINED ONLY BY THE CLAIMS AS ALLOWED. Moreover, none of the appended claims are intended to invoke paragraph six of 35 U.S.C. Sect. 112 unless the exact phrase "means for" is employed and is followed by a participle.

What is claimed is:

1. A computer system comprising:

a DRAM memory;

a reconfigurable logic device having a memory controller coupled to selected inputs and outputs of said DRAM memory; and

a data maintenance block coupled to said reconfigurable logic device and self-refresh command inputs of said DRAM memory, said data maintenance block operative to provide stable input levels on said self-refresh command inputs while said reconfigurable logic device is reconfigured.

2. The computer system of claim **1** wherein said DRAM memory comprises DDR3 compliant memory devices.

3. The computer system of claim **1** wherein said reconfigurable logic device comprises an FPGA.

4. The computer system of claim **1** wherein said data maintenance block comprises a command decode portion coupled to a reconfigure controller of said reconfigurable logic device.

5. The computer system of claim **4** wherein said command decode portion of said data maintenance block is operative in response to a command from said reconfigure controller and provides an acknowledgement signal in response.

6. The computer system of claim **1** wherein said data maintenance block comprises a memory block coupled to a reconfigure controller of said reconfigurable logic device.

7. The computer system of claim **6** wherein said memory block is operative to retain data received from said reconfigure controller of said reconfigurable logic device.

8. The computer system of claim **1** wherein said data maintenance block comprises a CPLD.

9. The computer system of claim **1** wherein said reconfigurable logic device comprises said data maintenance block.

10. The computer system of claim **1** wherein said data maintenance block is operable to hold said DRAM memory in self-refresh mode while said reconfigurable logic device is reconfigured.

11. A method for preserving contents of a DRAM memory associated with a reconfigurable device having a memory controller comprising:

providing a data maintenance block coupled to said reconfigurable device;

coupling said data maintenance block to self-refresh command inputs of said DRAM memory;

storing data received from said reconfigurable device at said data maintenance block; and

maintaining stable input levels on said self-refresh command inputs while said reconfigurable logic device is reconfigured.

12. The method of claim **11** wherein said step of providing comprises:

providing a command decode portion of said data maintenance block coupled to receive commands from said reconfigurable device and return acknowledgment signals in response thereto.

13. The method of claim **11** wherein said step of storing comprises:

providing a memory block in said data maintenance block for storing said data received from said reconfigurable device and returning said data to said reconfigurable device upon completion of a reconfiguration function.

14. The method of claim **11** wherein said step of storing comprises:

providing a memory block in said data maintenance block for storing said data received directly from said DRAM memory and returning said data directly to said DRAM memory upon completion of a reconfiguration function.

15. The method of claim **11** wherein said step of providing said data maintenance block comprises:

providing a portion of said reconfigurable device as said data maintenance block.

16. The method of claim **11** wherein said step of providing said data maintenance block comprises:

providing a CPLD as said data maintenance block.

17. The method of claim **11** wherein said step of providing said data maintenance block comprises:

providing a block RAM for storing said data received from said reconfigurable device; and

providing a command decode portion responsive to said reconfigurable device and coupled to said reset and lock enable inputs of said DRAM memory.

18. The method of claim **11** further comprising:

passing said data between sequential computing tasks in a reconfigurable computing environment.

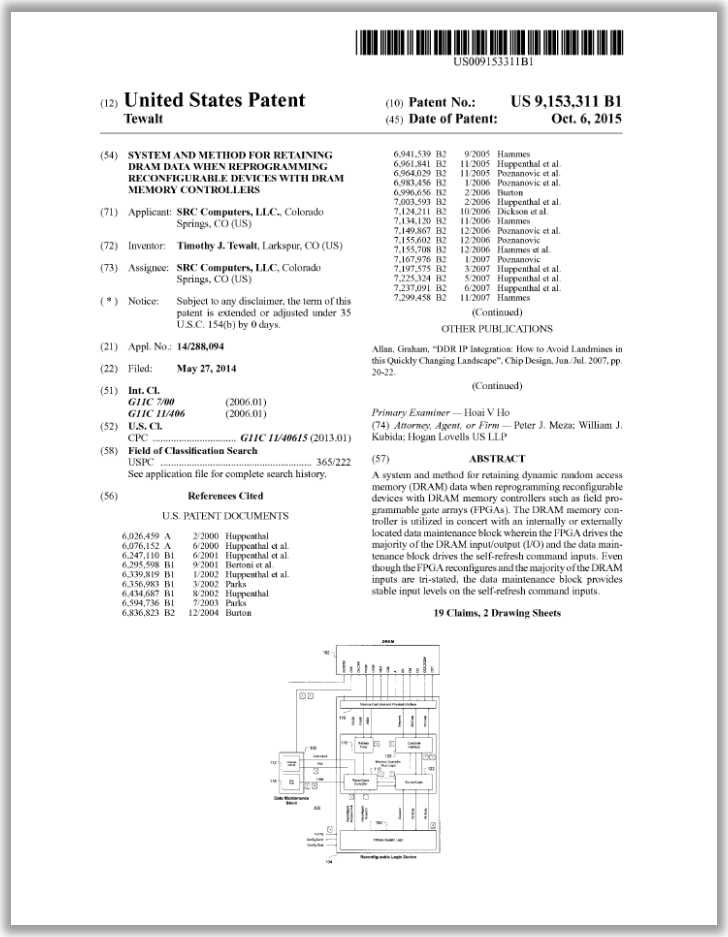
19. The method of claim **11** further comprising:

preserving said data at said data maintenance block while said reconfigurable logic device is powered down.

* * * * *

EXHIBIT B

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)



US009153311B1

(12) **United States Patent**
Tewalt

(10) **Patent No.: US 9,153,311 B1**
(45) **Date of Patent: Oct. 6, 2015**

(54) **SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS**

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(72) Inventor: **Timothy J. Tewalt**, Larkspur, CO (US)

(73) Assignee: **SRC Computers, LLC**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/288,094**

(22) Filed: **May 27, 2014**

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/406 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 11/40615*** (2013.01)

(58) **Field of Classification Search**
USPC 365/222
See application file for complete search history.

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Primary Examiner — Hoai V Ho
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(57) **ABSTRACT**

A system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers such as field programmable gate arrays (FPGAs). The DRAM memory controller is utilized in concert with an internally or externally located data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

19 Claims, 2 Drawing Sheets

Title: SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS

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Issued Date: Oct. 06, 2015

Expiration Date: May 27, 2034

Inventor: Timothy J. Tewalt

Exemplary Claims: 1, 3, 9, 10

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A **(CS) computer system** comprising:

a **(D) DRAM memory**;

a **(RL) reconfigurable logic device** having a (MC) **memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is operable to hold said **(D) DRAM memory** in **(SR) self-refresh mode** while said **reconfigurable logic device** is **(R) reconfigured**.

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

CS

	Feature	Alveo U25
Dimensions	Width	Single Slot
	Form Factor	Half Height, ½ Length
Logic Resources[1]	Look-Up Tables	523K
	Registers	1,045K
DRAM Memory	DDR Format	- 1x 2GB x 40 DDR4-2400 - 1x 4GB x 72 DDR4-2400
Interfaces	PCI Express®	Gen3 x16, 2xGen3 x8
	Link Speeds	10/25GbE
	Network Interface	2x SFP28
Networking	Thermal Cooling	Passive
	Typical Power	55W
	Maximum Power	75W
	Stateless Offloads	Yes
	Tunneling Offloads	VXLAN, Geneve, Custom
	SR-IOV	Yes
	Advanced Packet Filtering	Yes
	Acceleration	DPDK, Onload®
Time Stamp	Hardware Timestamping	Yes
Manageability	PMCI Protocols	NC-SI, PLDM Monitoring and Control, PLDM
	PMCI Transports	MCTP SMBus, MCTP PCIe VDM
	Boot Support	PXE and UEFI
Tool Support	Vitis™ Developer Environment	Yes

RL

D

Alveo™ SmartNIC Da

Notes:
1. Logic resources shown without platform usage; refer to card user guides for platform resource usage.

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Adapter Hardware

- 2x PCIe Gen 3 x8 (x16 connector in bifurcated mode)
- 2x10/25G SFP28 DA copper or optical transceiver;
- XtremeScale™ Ethernet Controller
- Zynq® UltraScale+™ XCU25 FPGA — **RL**
- 1x 2GB x 40 DDR4-2666
- 2x 4GB x 72 DDR4-2666 — **D**

Source: Xilinx Alveo Product Selection Guide – Data Center Accelerator Cards, XMP451 (v1.6), 2019-2020
Xilinx Alveo U25 2x10/25Gb Ethernet PCIe SmartNIC: Product Brief, WW02272020, 2020

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

The Alveo™ SN1000 family of composable SmartNICs meets these challenges with software-defined hardware acceleration. Revolutionary Xilinx composability empowers providers and enterprises to effortlessly support new protocols, build custom offloads, and deploy efficient and fluid application-specific data paths using P4 or HLS.

SN1000 SmartNICs deliver protocol-level programmability at line-rate performance, and are powered by a Xilinx 16nm UltraScale+™ architecture FPGA and a 16-core NXP Arm® processor. **RL**

Starting with the SN1022 100Gb/s composable SmartNIC, the Alveo™ SN1000 family provides a comprehensive suite of solutions for network, storage, and compute acceleration functions on a single platform. **CS**

Xilinx uses both SN1000 and SN1022 to identify their newest accelerator card.

CS

Hardware
- PCIe Gen 4 x8 or Gen 3 x16 **RL**
- 2x100G QSFP28 DA copper or optical transceiver
- XCU26 FPGA based on Xilinx 16nm UltraScale+ architecture
- On-board CPU: 16 64-bit Arm Cortex®-A72 cores at 2.0 GHz with 8 MB cache
- 1x 4GB x 72 DDR4-2400 (Processor)
- 2x 4GB x 72 DDR4-2400 (FPGA) **D**

Feature	Alveo U25	Alveo SN1022
Dimensions: Width	Single Slot	Single Slot
Dimensions: Form Factor	Half Height, ½ Length	Full Height, ½ Length
Logic Resources: Look-Up Tables	523K	1,030K
Logic Resources: Registers	1,045K	2,059K
DDR Format	- 1x 2GB x 40 DDR4-2400 - 1x 4GB x 72 DDR4-2400	- 1x 4GB x 72 DDR4-2400 (Arm® Processor) - 2x 4GB x 72 DDR4-2400 (FPGA)
PCI Express®	Gen3 x16, 2xGen3 x8	Gen 3 x16, Gen 4 x8
Link Speeds	10/25GbE	100GbE
Network Interface	2x SFP28	2x QSFP28
Arm Processor	Integrated Quad-core Cortex®-A53 Arm Processor	Discrete 16-core Cortex-A72 Processor
Thermal Cooling	Passive	Passive
Thermal Design Power	40W	70W
Total Power	75W	75W
Stateless Offloads	Yes	Yes
Tunneling Offloads	VXLAN, NVGRE, Geneve, Custom	VXLAN, NVGRE, Custom
SR-IOV	Yes	Yes

RL

D

Alveo™ SmartNIC Data Center

Source: Xilinx Alveo Product Selection Guide – Data Center Accelerator Cards, XMP451 (v1.7), 2019-2021
Xilinx Alveo SN1000 Smart NICs; Product Brief, JD022221, 2021

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

CS

	Feature	Alveo U30[1]
Dimensions	Width	Single Slot
	Form Factor, Passive Form Factor, Active	Half Height, ½ Length
Logic Resources[2]	Look-Up Tables	460K
	Registers	920K
	DSP Slices	3,456
Video support	Video Codec Unit (VCU)	Hardened
	Codec	H.264 and H.265
	Video Transcodes per Card	2 x 4kp60, 8 x 1080p60,16 x 1080p30, 32 x 720p30
DRAM Memory	DDR Format	2 x 4GB 72b DDR4
	DDR Total Capacity	8GB
	DDR Max Data Rate	2400MT/s
	DDR Total Bandwidth	38GB/s
Internal SRAM	Total Capacity	11MB
	Total Bandwidth	10TB/s
Interfaces	PCI Express®	Gen3 x8, 2 x Gen3 x4[3]
	Network Interface	–
Power and Thermal	Thermal Cooling	Passive
	Typical Power	40W
	Maximum Power	75W
Tool Support	Vivado® Design Suite	No
	FFmpeg with Xilinx Video Plugins	Yes
	Vitis™ Developer Environment	No
Solutions	Solutions & Libraries	Video Transcoding Solutions

RL

D

Alveo™ Media Data Center Accelerator Cards

Notes
1. The Alveo U30 Media Accelerator Card is designed for use in Xilinx real-time evaluation servers or turn-key high-density video transcoding appliances offered by Xilinx VARs..
2. Logic resources shown are without platform usage. User does not have access to these resources on the Alveo U30 card.
3. Servers need to support bifurcation for users to take advantage of both Zynq® UltraScale+™ devices on the Alveo U30 card.

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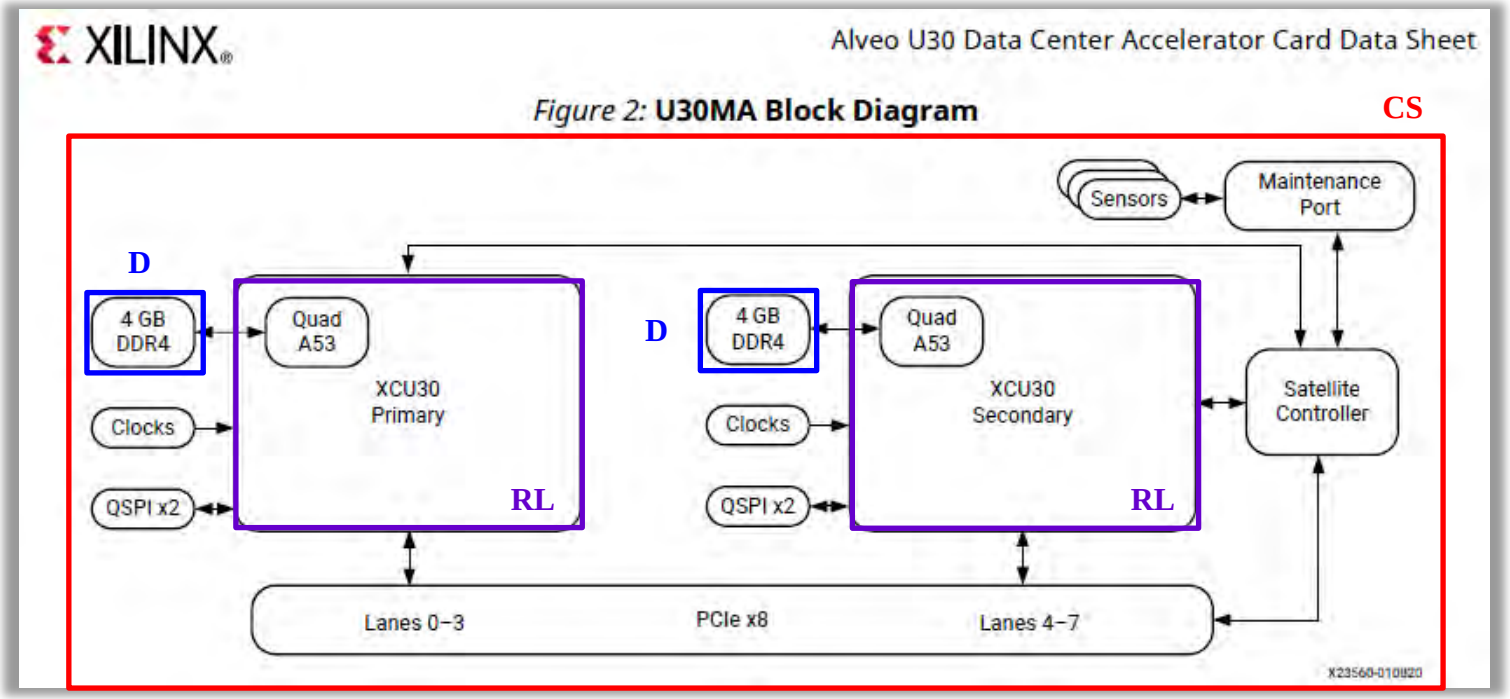
Source: Xilinx Alveo Product Selection Guide – Data Center Accelerator Cards, XMP451 (v1.6), 2019-2020
Xilinx Alveo U30 Data Center Accelerator Card Data Sheet, DS970 (v1.1) June16, 2020

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: Xilinx Alveo U30 Data Center Accelerator Card Data Sheet, DS970 (v1.1) June16, 2020

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

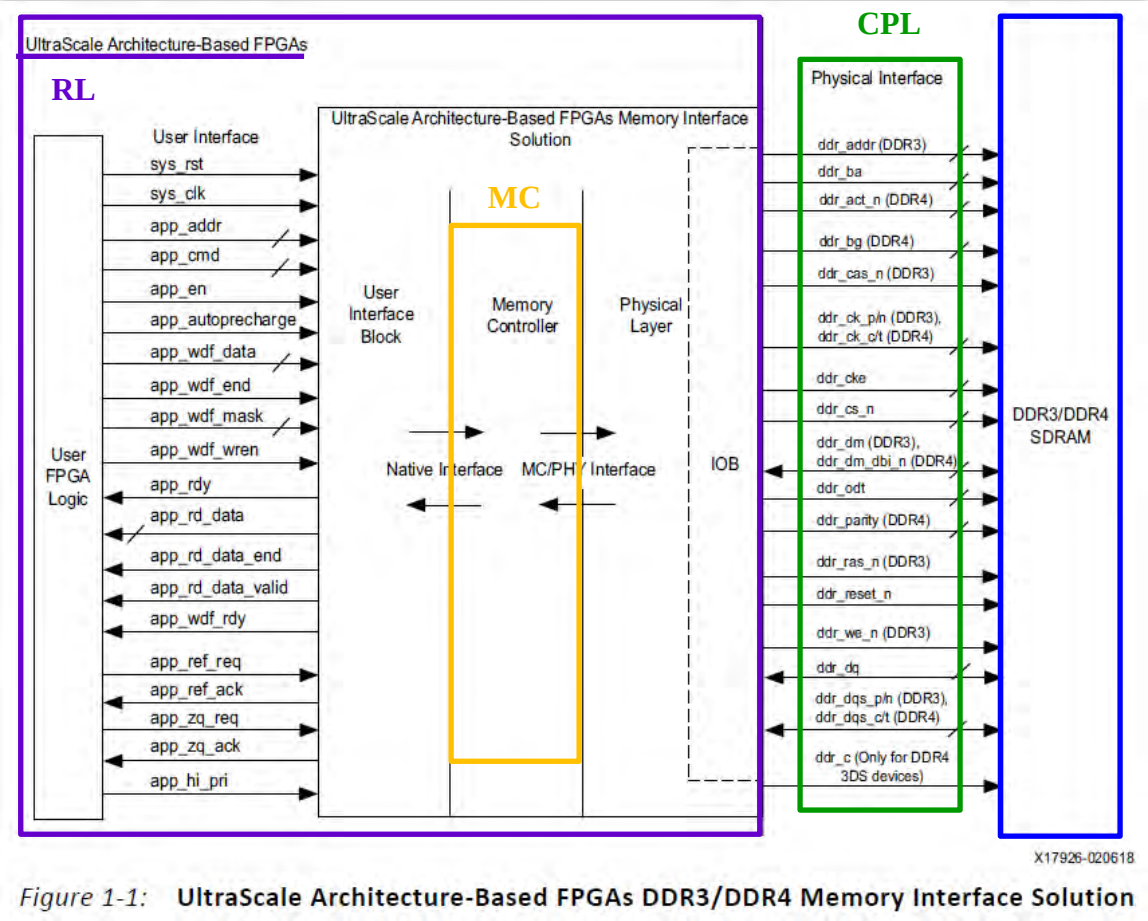


Figure 1-1: **UltraScale Architecture-Based FPGAs DDR3/DDR4 Memory Interface Solution**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit B - U.S. Patent No. 9,153,311 – Xilinx Alveo U25, U30, SN1022 (aka SN1000)

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

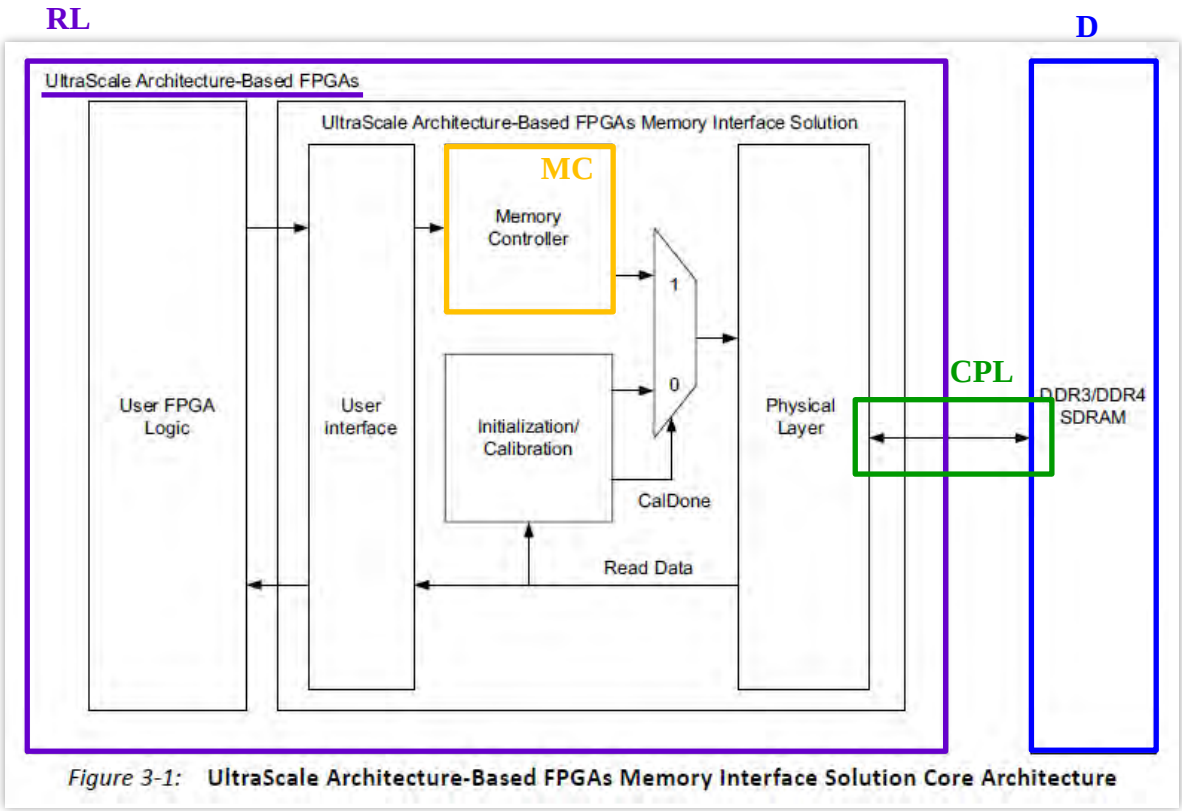
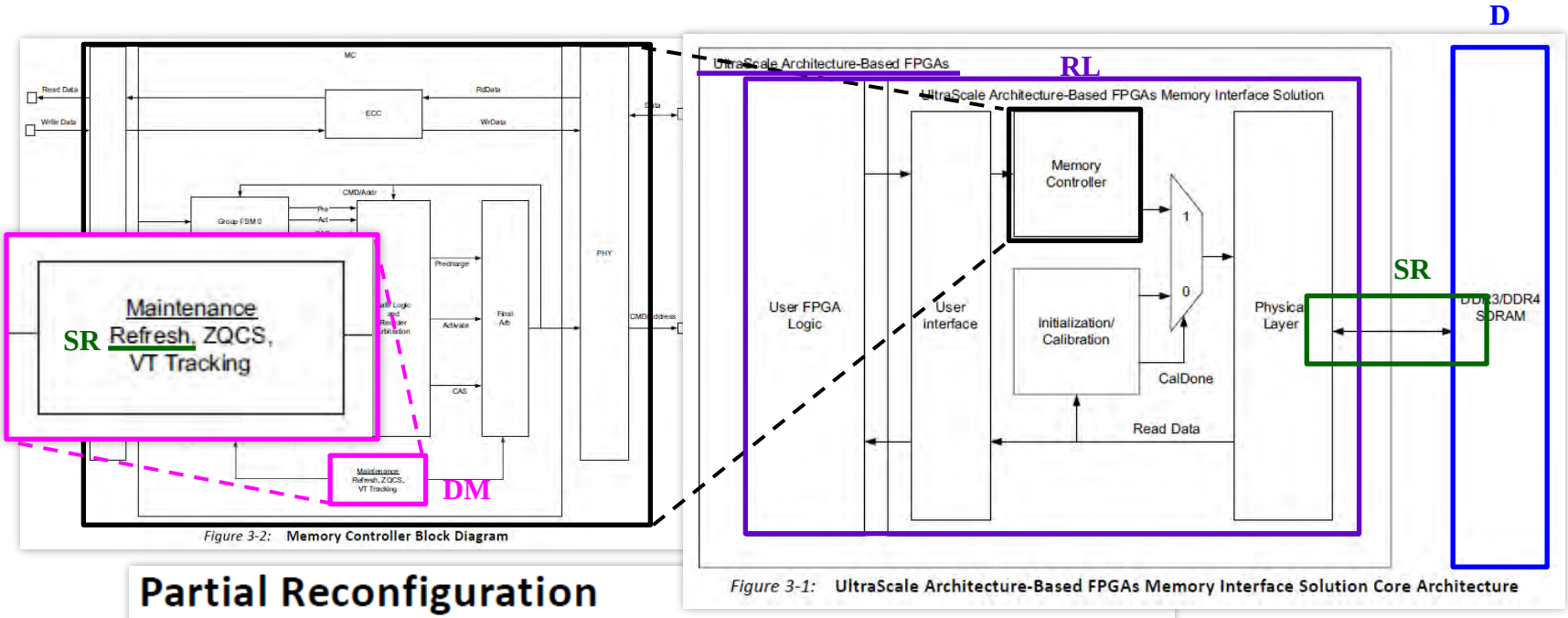


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,



Partial Reconfiguration

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

SR

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh **SIL**

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

SIL

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R **RL**

Partial Reconfiguration

SR

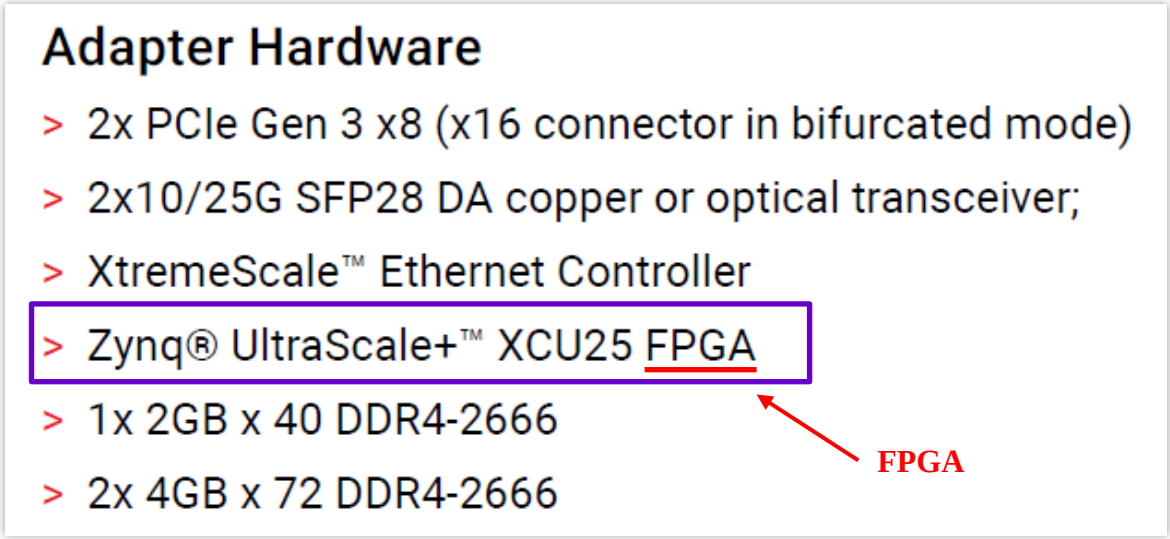
The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.



Source: Xilinx Alveo U25 2x10/25Gb Ethernet PCIe SmartNIC: Product Brief, WW02272020, 2020

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

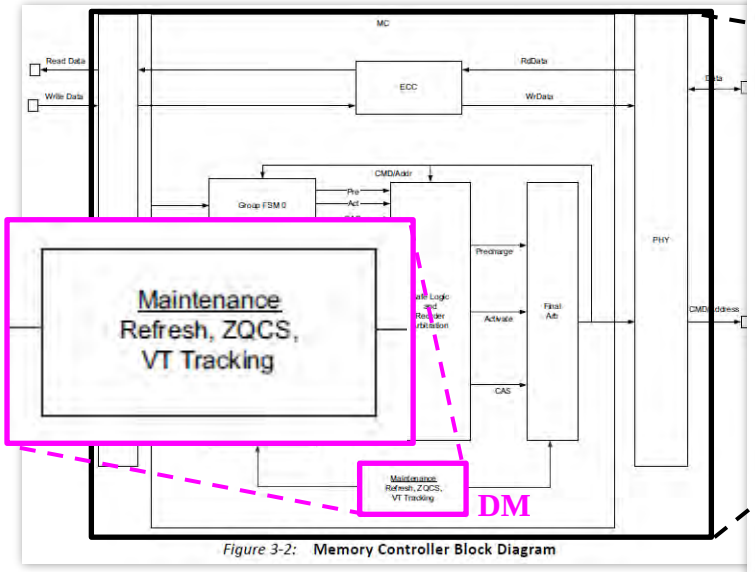


Figure 3-2: **Memory Controller Block Diagram**

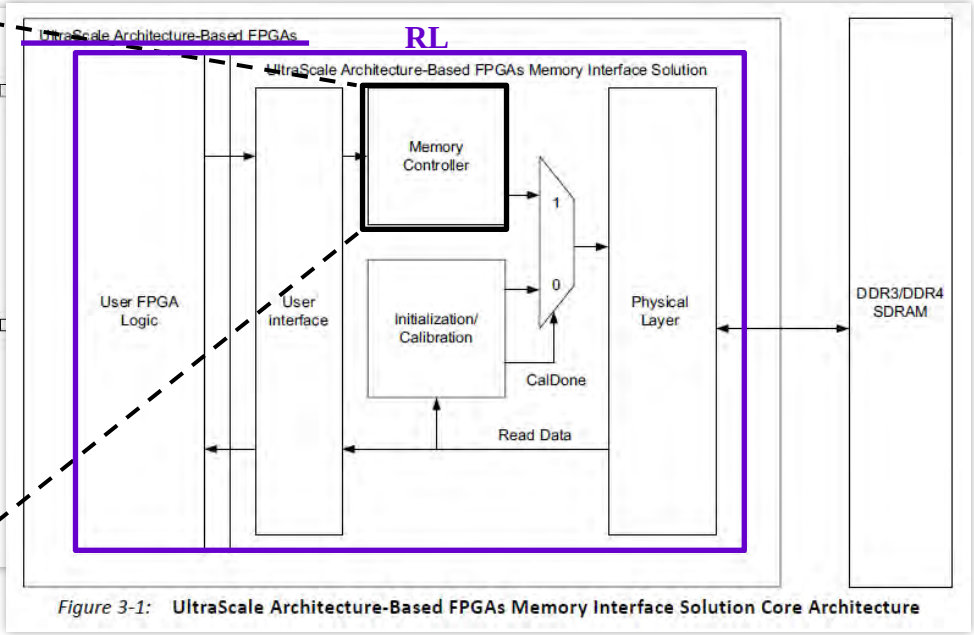


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is **(HSR) operable to hold said DRAM memory in self-refresh mode** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh HSR

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

HSR

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R RL

Partial Reconfiguration

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration; it is used to hold/keep the DRAM memory in self-refresh mode.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is **(HSR) operable to hold said DRAM memory in self-refresh mode** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

The maintenance blocks (DM) of the controller command path include:

1. Blocks that generate refresh and ZQCS commands
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh (HSR)

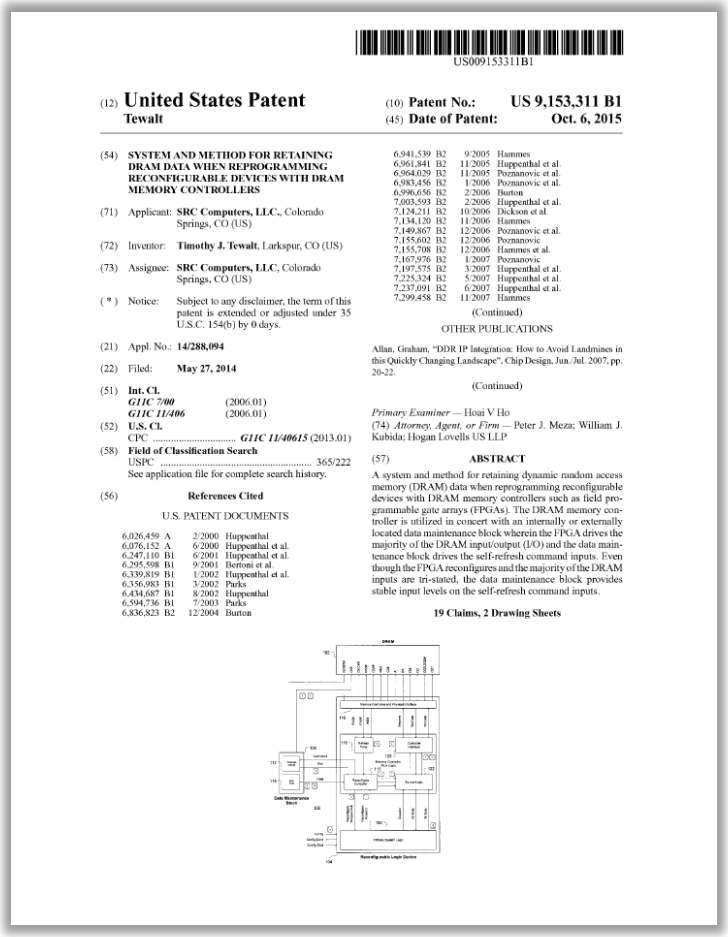
Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

Self-refresh feature keeps the DRAM in self-refresh mode (HSR). It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram (R) the FPGA (RL) or turn it off. It is referred as self-refresh entry cycle.

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

EXHIBIT C

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280



US009153311B1

(12) **United States Patent**
Tewalt

(10) **Patent No.: US 9,153,311 B1**
(45) **Date of Patent: Oct. 6, 2015**

(54) **SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS**

(71) Applicant: **SRC Computers, LLC**, Colorado Springs, CO (US)

(72) Inventor: **Timothy J. Tewalt**, Larkspur, CO (US)

(73) Assignee: **SRC Computers, LLC**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/288,094**

(22) Filed: **May 27, 2014**

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/406 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 11/40615*** (2013.01)

(58) **Field of Classification Search**
USPC 365/222
See application file for complete search history.

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Primary Examiner — Hoai V Ho
(74) *Attorney, Agent, or Firm* — Peter J. Meza; William J. Kubida; Hogan Lovells US LLP

(57) **ABSTRACT**

A system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers such as field programmable gate arrays (FPGAs). The DRAM memory controller is utilized in concert with an internally or externally located data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

19 Claims, 2 Drawing Sheets

Title: SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS

Priority Date: May 27, 2014

Filed Date: May 27, 2014

Issued Date: Oct. 06, 2015

Expiration Date: May 27, 2034

Inventor: Timothy J. Tewalt

Exemplary Claims: 1, 3, 9, 10

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280

Claim 1

A **(CS) computer system** comprising:

a **(D) DRAM memory**;

a **(RL) reconfigurable logic device** having a (MC) **memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is operable to hold said **(D) DRAM memory** in **(SR) self-refresh mode** while said **reconfigurable logic device** is **(R) reconfigured**.

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

CS

	Product Name	Alveo U200	Alveo U250	Alveo U280	Alveo U50
Dimensions	Width	Dual Slot	Dual Slot	Dual Slot	Single Slot
	Form Factor, Passive Form Factor, Active	Full Height, ¾ Length Full Height, Full Length	Full Height, ¾ Length Full Height, Full Length	Full Height, ¾ Length Full Height, Full Length	Half Height, ½ Length
Logic Resources[1]	Look-Up Tables	1,182K	1,728K	1,304K	872K
	Registers	2,364K	3,456K	2,607K	1,743K
	DSP Slices	6,840	12,288	9,024	5,952
DRAM Memory	DDR Format	4x 16GB 72b DIMM DDR4	4x 16GB 72b DIMM DDR4	2x 16GB 72b DIMM DDR4	–
	DDR Total Capacity	64GB	64GB	32GB	–
	DDR Max Data Rate	2400MT/s	2400MT/s	2400MT/s	–
	DDR Total Bandwidth	77GB/s	77GB/s	38GB/s	–
	HBM2 Total Capacity	–	–	8GB	8GB
	HBM2 Total Bandwidth	–	–	460GB/s	316GB/s[4]
Internal SRAM	Total Capacity	43MB	57MB	43MB	28MB
	Total Bandwidth	37TB/s	47TB/s	35TB/s	24TB/s
Interfaces	PCI Express®	Gen3 x16	Gen3 x16	Gen3 x16, 2xGen4 x8, CCIX	Gen3 x16, 2xGen4 x8, CCIX
	Network Interface	2x QSFP28	2x QSFP28	2x QSFP28	U50[2] - 1x QSFP28 U50DD[3] - 2x SFP-DD
Power and Thermal	Thermal Cooling	Passive, Active	Passive, Active	Passive, Active	Passive
	Typical Power	100W	110W	100W	50W
	Maximum Power	225W	225W	225W	75W
Time Stamp	Clock Precision	–	–	–	IEEE Std 1588
Compute Performance	INT8 TOPs	18.6	33.3	24.5	16.2
	Machine Learning	Machine Learning Solution Brief			
	Acceleration Applications	Acceleration Application Solutions			

RL

D

Alveo™ Data Center Accelerator Cards

Notes
1. Logic resources shown without shell usage; refer to card user guides for shell resource usage
2. U50 is a production qualified card for volume deployment
3. U50DD is an engineering sample card not for volume production
4. For A-U50DD-P00G-ES3-G and A-U50-P00G-PQ-G measured 316 GB/s peak HBM2 bandwidth, 201 GB/s nominal

Page 2

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Source: Xilinx Alveo Product Selection Guide – Data Center Accelerator Cards, XMP451 (v1.3), 2019

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

FPGA Resource Information

The Xilinx Alveo U200 and U250 accelerator cards (CS) are custom-built UltraScale+ FPGAs (RL) that run optimally (and exclusively) on the Alveo architecture. The Alveo U200 card features the XCU200 FPGA and the Alveo U250 card uses the XCU250 FPGA, which uses Xilinx stacked silicon interconnect (SSI) technology to deliver breakthrough FPGA capacity, bandwidth, and power efficiency. This technology allows for increased density by combining multiple super logic regions (SLRs). The XCU200 comprises three SLRs and the XCU250 comprises four SLRs. Both devices connect to 16 lanes of PCI Express® that can operate up to 8 GT/s (Gen3). Both devices connect to four DDR4 16 GB, 2400 MT/s, 64-bit with error correcting code (ECC) DIMMs for a total of 64 GB of DDR4. Both devices connect to two QSFP28 connectors with associated clocks generated on board. The following figures show the SLR regions along with the connections for PCIe, DDR4 and QSFP28. **D**

FPGA Resource Information

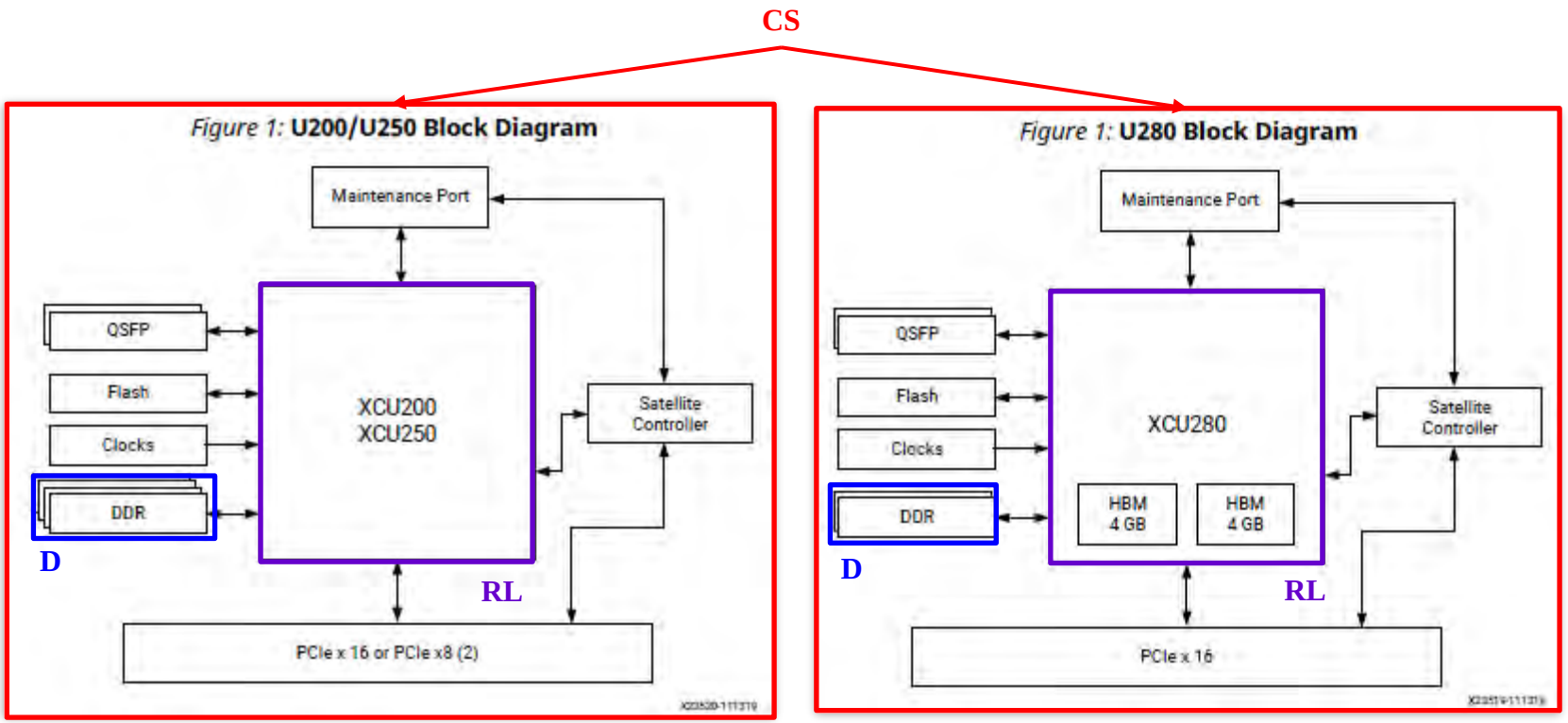
The Xilinx Alveo U280 accelerator card (CS) is a custom-built UltraScale+ FPGA (RL) that runs optimally (and exclusively) on the Alveo architecture. The Alveo U280 card features the XCU280 FPGA, which uses Xilinx stacked silicon interconnect (SSI) technology to deliver breakthrough FPGA capacity, bandwidth, and power efficiency. This technology allows for increased density by combining multiple super logic regions (SLRs). The XCU280 comprises three SLRs with the bottom SLR (SLR0) integrating an HBM controller to interface with the adjacent 8 GB HBM2 memory. The bottom SLR also connects to 16 lanes of PCI Express® that can operate up to 16 GT/s (Gen4). SLR0 and SLR1 both connect to a DDR4 16 GB, 2400 MT/s, 64-bit with error correcting code (ECC) DIMM for a total of 32 GB of DDR4. SLR2 connects two QSFP28 connectors with associated clocks generated on the U280 board. The following figure shows the three SLR regions along with the connections for PCIe, DDR4, and QSFP28. The HBM is co-located on the XCU280 device and connects directly to SLR0. **D**

Source: Xilinx Alveo U200 and U250 Data Center Accelerator Cards Data Sheet, DS962 (v1.2.1) December 9, 2019
Xilinx Alveo U280 Data Center Accelerator Card Data Sheet, DS963 (v1.2) November 20, 2019

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: Xilinx Alveo U200 and U250 Data Center Accelerator Cards Data Sheet, DS962 (v1.2.1) December 9, 2019
Xilinx Alveo U280 Data Center Accelerator Card Data Sheet, DS963 (v1.2) November 20, 2019

Exhibit C - U.S. Patent No. 9,153,311 – Xilinx Alveo U200, U250, U280

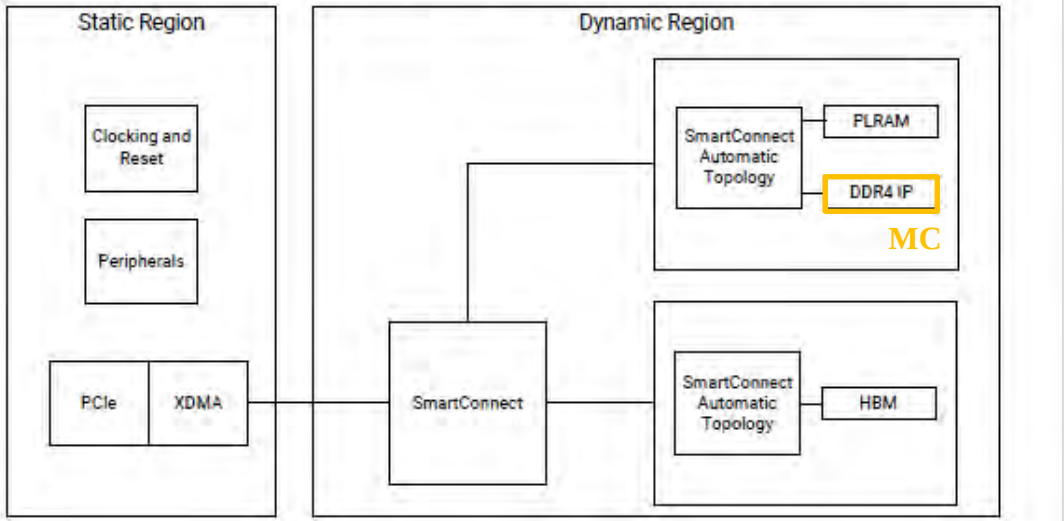
Claim 1

A computer system comprising:
a DRAM memory;
a reconfigurable logic device having a **(MC) memory controller** coupled to selected inputs and outputs of said DRAM memory; and

MC

The dynamically programmable region has several DDR/HBM/PLRAM memory interfaces coupled with interconnect logic. The term PLRAM refers to internal UltraRAM/block RAM that can be accessed by host and user kernels. The dynamically programmable region uses the Memory Subsystem (MSS) IP (for DDR/PLRAM) and the HBM Memory Subsystem (HMSS) IP (for HBM). These subsystems are unique to the Vitis platforms. They contain multiple memory interfaces, coupled with the appropriate interconnect IP. When the dynamic region is being built

Figure 5: **Static Region (Target Platform) and Dynamic Region of U280 Card**



The Alveo cards use Memory Subsystem IP for its interface to DDR4; this MSS IP (DDR4 IP in the figure) contains the **(MC) memory controller**.

Source: Xilinx Alveo U280 Data Center Accelerator Card User Guide, UG1314 (v1.2.1) November 20, 2019

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

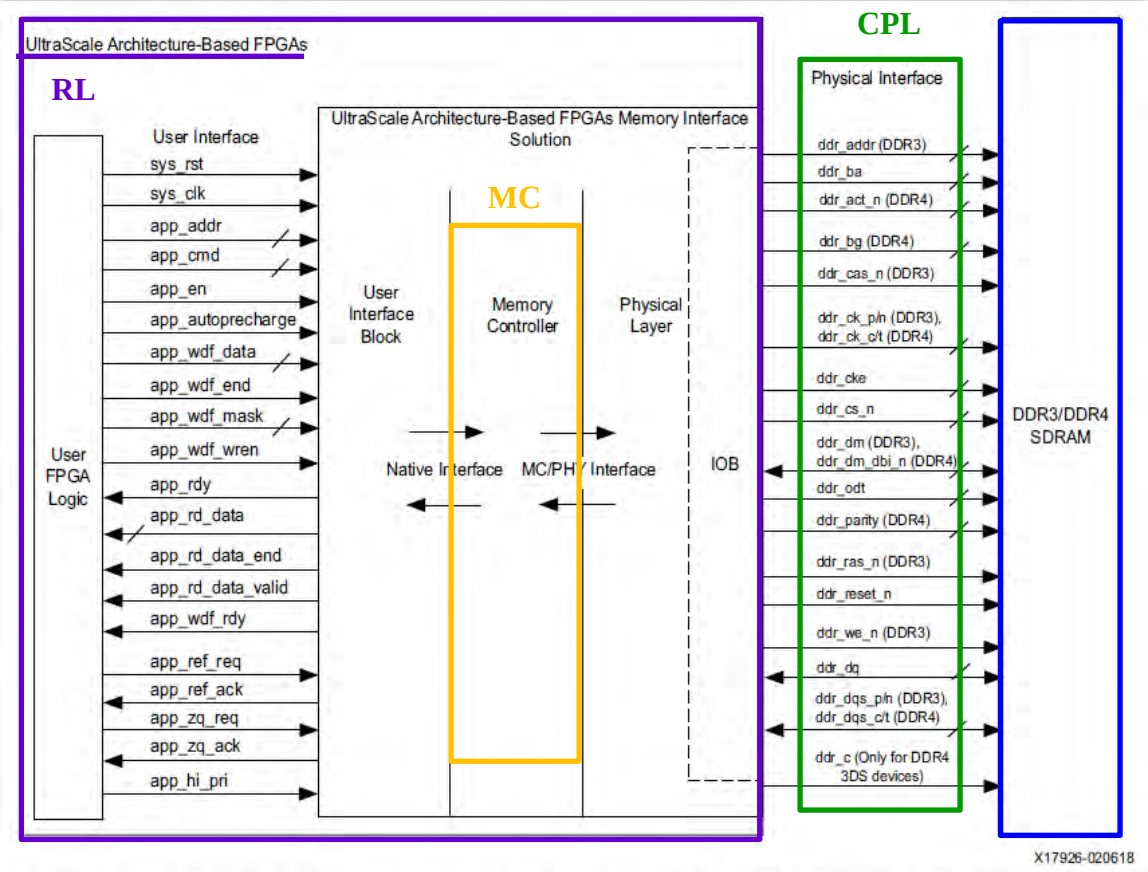


Figure 1-1: **UltraScale Architecture-Based FPGAs DDR3/DDR4 Memory Interface Solution**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

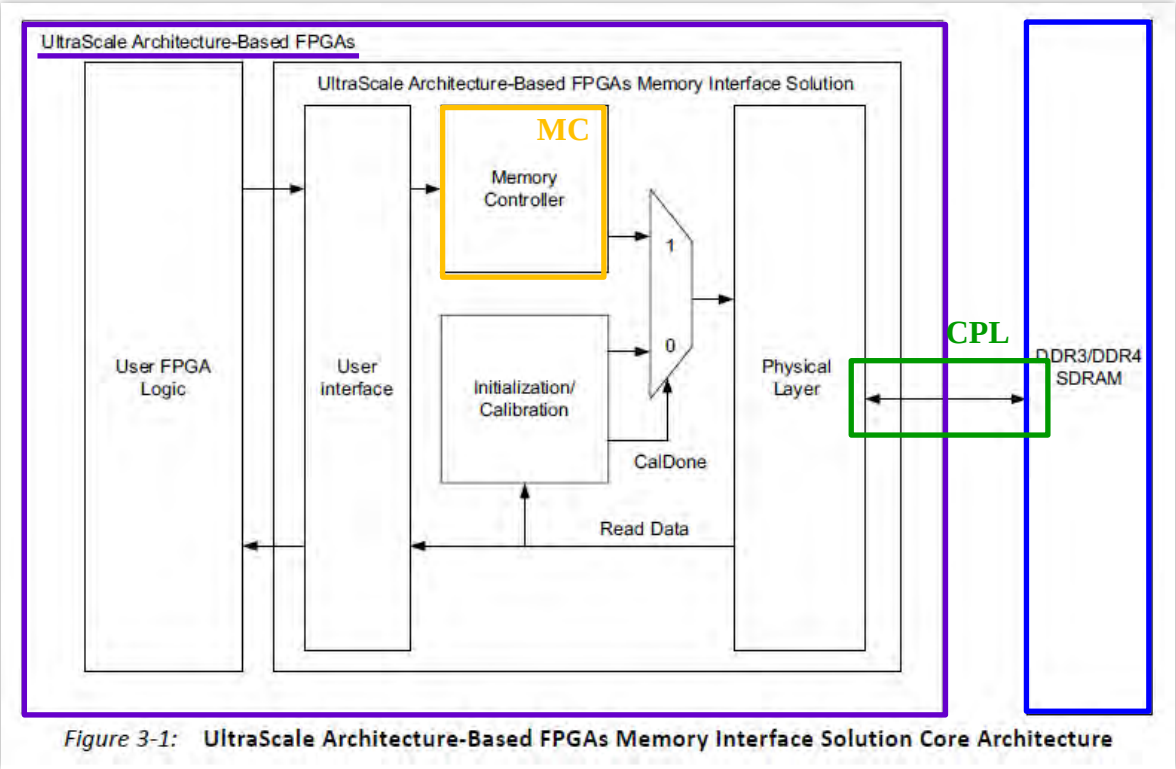


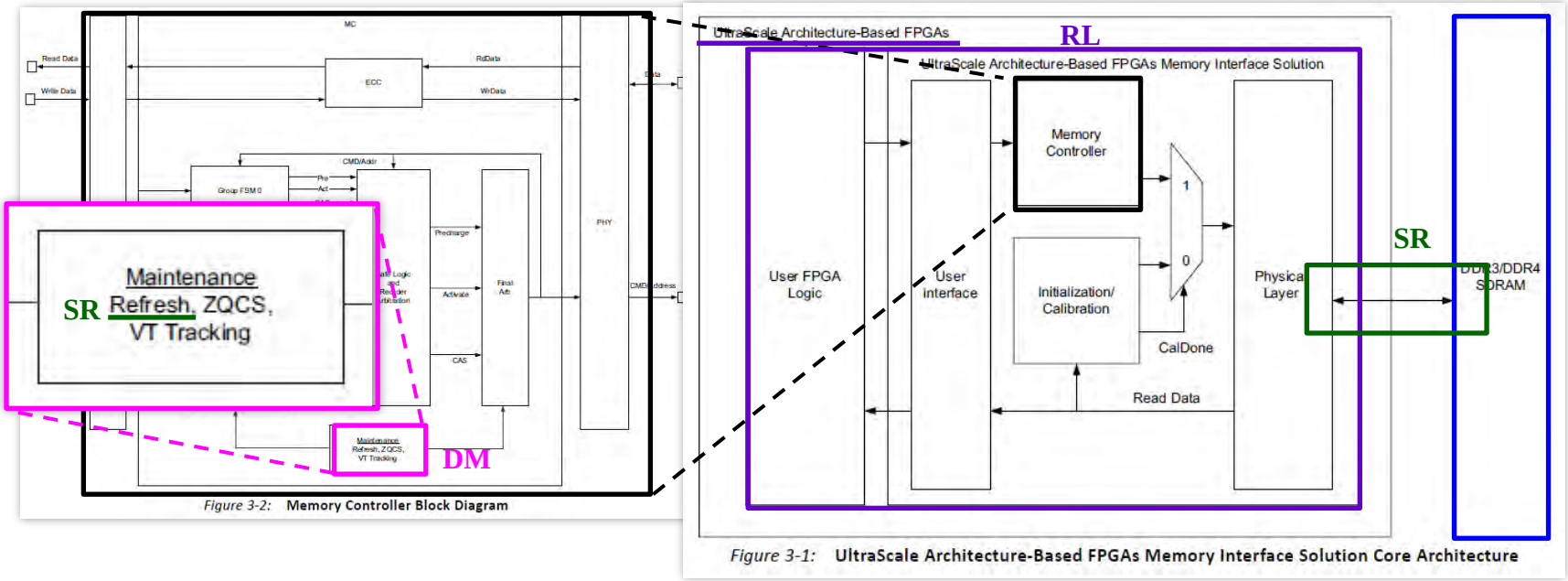
Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

D



DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh **SIL**

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

SIL

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R **RL**

Partial Reconfiguration **SR**

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

FPGA Resource Information

RL

The Xilinx Alveo U200 and U250 accelerator cards are custom-built UltraScale+ FPGAs that run optimally (and exclusively) on the Alveo architecture. The Alveo U200 card features the XCU200 FPGA and the Alveo U250 card uses the XCU250 FPGA, which uses Xilinx stacked silicon interconnect (SSI) technology to deliver breakthrough FPGA capacity, bandwidth, and power efficiency. This technology allows for increased density by combining multiple super logic regions (SLRs). The XCU200 comprises three SLRs and the XCU250 comprises four SLRs. Both devices connect to 16 lanes of PCI Express® that can operate up to 8 GT/s (Gen3). Both devices connect to four DDR4 16 GB, 2400 MT/s, 64-bit with error correcting code (ECC) DIMMs for a total of 64 GB of DDR4. Both devices connect to two QSFP28 connectors with associated clocks generated on board. The following figures show the SLR regions along with the connections for PCIe, DDR4 and QSFP28.

FPGA

FPGA Resource Information

RL

The Xilinx Alveo U280 accelerator card is a custom-built UltraScale+ FPGA that runs optimally (and exclusively) on the Alveo architecture. The Alveo U280 card features the XCU280 FPGA, which uses Xilinx stacked silicon interconnect (SSI) technology to deliver breakthrough FPGA capacity, bandwidth, and power efficiency. This technology allows for increased density by combining multiple super logic regions (SLRs). The XCU280 comprises three SLRs with the bottom SLR (SLR0) integrating an HBM controller to interface with the adjacent 8 GB HBM2 memory. The bottom SLR also connects to 16 lanes of PCI Express® that can operate up to 16 GT/s (Gen4). SLR0 and SLR1 both connect to a DDR4 16 GB, 2400 MT/s, 64-bit with error correcting code (ECC) DIMM for a total of 32 GB of DDR4. SLR2 connects two QSFP28 connectors with associated clocks generated on the U280 board. The following figure shows the three SLR regions along with the connections for PCIe, DDR4, and QSFP28. The HBM is co-located on the XCU280 device and connects directly to SLR0.

FPGA

Source: Xilinx Alveo U200 and U250 Data Center Accelerator Cards Data Sheet, DS962 (v1.2.1) December 9, 2019
Xilinx Alveo U280 Data Center Accelerator Card Data Sheet, DS963 (v1.2) November 20, 2019

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

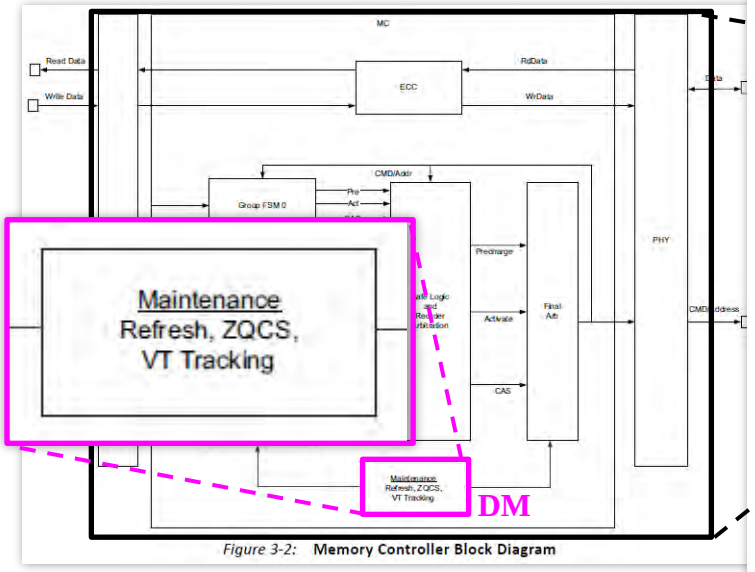


Figure 3-2: **Memory Controller Block Diagram**

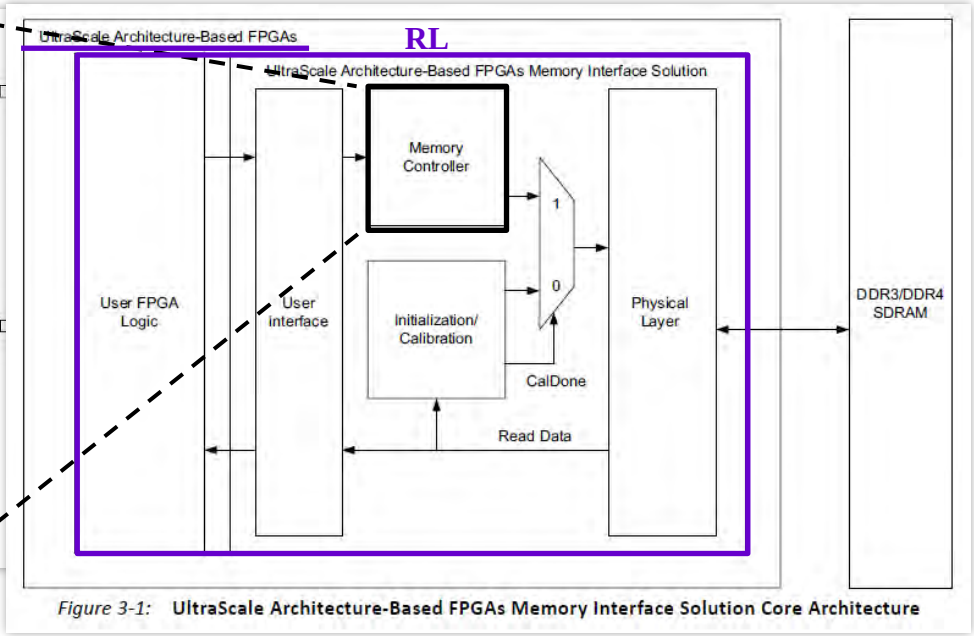


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is **(HSR) operable to hold said DRAM memory in self-refresh mode** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh HSR

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

HSR

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R RL

Partial Reconfiguration

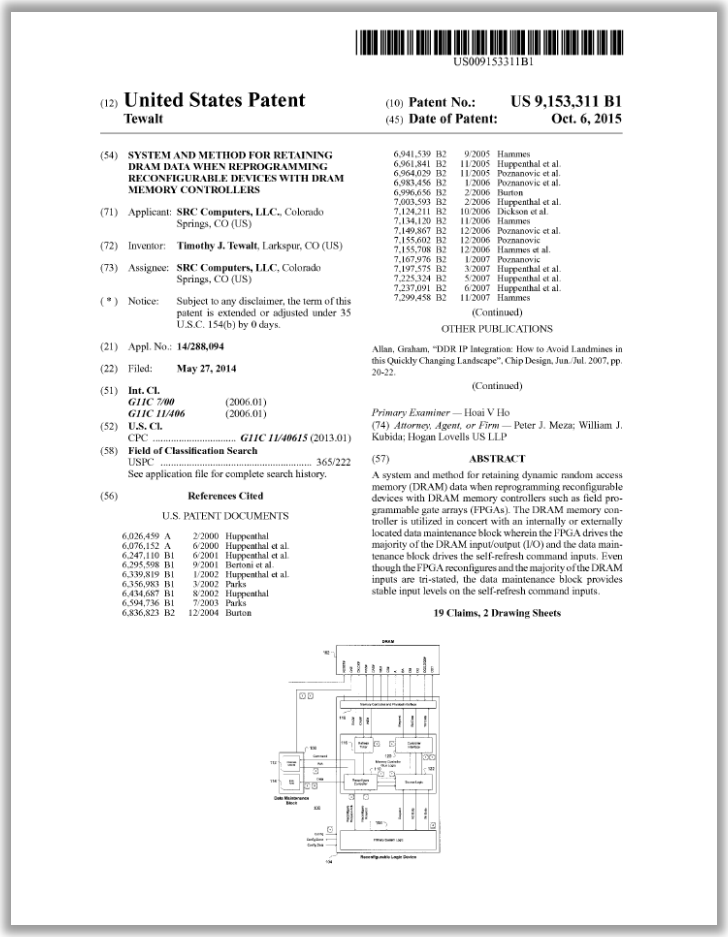
The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration; it is used to hold/keep the DRAM memory in self-refresh mode.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

EXHIBIT D

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's



US009153311B1

(12) **United States Patent**
Tewalt

(10) **Patent No.: US 9,153,311 B1**
(45) **Date of Patent: Oct. 6, 2015**

(54) **SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS**

(71) Applicant: **SRC Computers, LLC**, Colorado Springs, CO (US)

(72) Inventor: **Timothy J. Tewalt**, Larkspur, CO (US)

(73) Assignee: **SRC Computers, LLC**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/288,094**

(22) Filed: **May 27, 2014**

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/406 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 11/40615*** (2013.01)

(58) **Field of Classification Search**
USPC 365/222
See application file for complete search history.

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Primary Examiner — Hoai V Ho
(74) *Attorney, Agent, or Firm* — Peter J. Meza; William J. Kubida; Hogan Lovells US LLP

(57) **ABSTRACT**

A system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers such as field programmable gate arrays (FPGAs). The DRAM memory controller is utilized in concert with an internally or externally located data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

19 Claims, 2 Drawing Sheets

Title: SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS

Priority Date: May 27, 2014

Filed Date: May 27, 2014

Issued Date: Oct. 06, 2015

Expiration Date: May 27, 2034

Inventor: Timothy J. Tewalt

Exemplary Claims: 1, 3, 9, 10

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:

a **(D) DRAM memory**;

a **(RL) reconfigurable logic device** having a (MC) **memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is operable to hold said **(D) DRAM memory** in **(SR) self-refresh mode** while said **reconfigurable logic device** is **(R) reconfigured**.

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

RL

	Device Name	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P	KU19P
Logic	System Logic Cells (K)	356	475	600	653	747	1,143	1,843
	CLB Flip-Flops (K)	325	434	548	597	683	1,045	1,685
	CLB LUTs (K)	163	217	274	299	341	523	842
Memory	Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8	11.6
	Total Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6	60.8
	UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0	81.0
Clocking	Clock Mgmt Tiles (CMTs)	4	4	4	8	4	11	9
	DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968	1,080
Integrated IP	PCIE4 (PCIe® Gen3 x16)	1	1	0	4	0	5	0
	PCIE4C (PCIe® Gen3 x16 / Gen4 x8 /CCIX)	0	0	0	0	0	0	3
	150G Interlaken	0	0	0	1	0	4	0
	100G Ethernet w/ KR4 RS-FEC	0	1	0	2	0	4	1
I/O	Max. Single-Ended HD I/Os	96	96	96	96	96	96	72
	Max. Single-Ended HP I/Os	208	208	208	416	208	572	468
	GTH 16.3Gb/s Transceivers	0	0	28	32	28	44	0
	GTY 32.75Gb/s Transceivers	16	16	0	20	0	32	32
Speed Grades	Extended[1]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2
Footprint[2, 3]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s						
B784[4]	23x23[5]	96, 208, 0, 16	96, 208, 0, 16					
A676[4]	27x27	48, 208, 0, 16	48, 208, 0, 16					
B676	27x27	72, 208, 0, 16	72, 208, 0, 16					
D900[4]	31x31	96, 208, 0, 16	96, 208, 0, 16		96, 312, 16, 0			
E900	31x31			96, 208, 28, 0		96, 208, 28, 0		
A1156[4]	35x35				48, 416, 20, 8		48, 468, 20, 8	

Kintex® UltraScale+™ FPGAs

For clarity, accused products from the above-referenced table appear below:

- Kintex UltraScale+ FPGA Devices - KU3P, KU5P, KU9P, KU11P, KU13P, KU15P, KU19P

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Kintex devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx UltraScale+ FPGA Product Tables and Product Selection Guide, XMP103 (v1.21)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

RL

	Foundation							58G PAM4		
Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU23P	VU27P	VU29P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	8,938	2,252	2,835	3,780
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	8,172	2,059	2,592	3,456
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	4,086	1,030	1,296	1,728
Max. Dist. RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	58.4	14.2	36.2	48.3
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	75.9	74.3	70.9	94.5
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	99.0	270.0	360.0
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840	1,320	9,216	12,288
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	10.4	4.1	28.7	38.3
PCIe® Gen3 x16	2	4	4	6	3	4	0	0	1	1
PCIe Gen3 x16/Gen4 x8 / CCIX[1]	–	–	–	–	–	–	8	4	–	–
150G Interlaken	3	4	6	9	6	8	0	0	8	8
100G Ethernet w/ KR4 RS-FEC	3	4	6	9	9	12	0	2	15	15
Max. Single-Ended HP I/Os	520	832	832	832	624	832	1,976	572	676	676
Max. Single-Ended HD I/Os	0	0	0	0	0	0	96	72	0	0
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80	34	32	32
GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	–	4	48	48
100G / 50G KP4 FEC	–	–	–	–	–	–	–	2 / 4	24 / 48	24 / 48
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	-1, -2	-1 -2	-1 -2

Footprint[3,4,5]	Dim. (mm)	HP I/O, GTY						HP I/O, HD I/O, GTY	HP I/O, HD I/O, GTY, GTM		
A1365[4]	35x35								364, 0, 34[8], 4		
C1517	40x40	520, 40									
J1760	42.5x42.5								572, 72, 34, 4		
F1924[6]	45x45					624, 64					
A2104	47.5x47.5		832, 52	832, 52	832, 52						
	52.5x52.5[7]						832, 52				
B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
	52.5x52.5[7]						702, 76				
C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
	52.5x52.5[7]						416, 104				
D2104	47.5x47.5				676, 76	572, 76					
	52.5x52.5[7]						676, 76			676, 16, 30	676, 16, 30
H2104	47.5x47.5										
A2577	52.5x52.5				448, 120	448, 96	448, 128			448, 32, 48	448, 32, 48

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Virtex® UltraScale+™ FPGAs

For clarity, accused products from the above-referenced table appear below:

- Virtex UltraScale+ FPGA Devices - VU3P, VU5P, VU7P, VU9P, VU11P, VU13P, VU19P, VU23P, VU27P, VU29

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Virtex devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx UltraScale+ FPGA Product Tables and Product Selection Guide, XMP103 (v1.21)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

	HBM (4GB)	HBM (8GB)			HBM (16GB)		
Device Name	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P	VU57P
System Logic Cells (K)	962	962	1,907	2,852	1,907	2,852	2,852
CLB Flip-Flops (K)	879	879	1,743	2,607	1,743	2,607	2,607
CLB LUTs (K)	440	440	872	1,304	872	1,304	1,304
Max. Dist. RAM (Mb)	12.5	12.5	24.6	36.7	24.6	36.7	36.7
Total Block RAM (Mb)	23.6	23.6	47.3	70.9	47.3	70.9	70.9
UltraRAM (Mb)	90.0	90.0	180.0	270.0	180.0	270.0	270.0
HBM DRAM (GB)	4	8	8	8	16	16	16
HBM AXI Interfaces	32	32	32	32	32	32	32
Clock Mgmt Tiles (CMTs)	4	4	8	12	8	12	12
DSP Slices	2,880	2,880	5,952	9,024	5,952	9,024	9,024
Peak INT8 DSP (TOP/s)	8.9	8.9	18.6	28.1	18.6	28.1	28.1
PCIe® Gen3 x16	0	0	1	2	1	2	0
PCIe Gen3 x16/Gen4 x8 / CCIX[1]	4	4	4	4	4	4	4
150G Interlaken	0	0	2	4	2	4	4
100G Ethernet w/ KR4 RS-FEC	2	2	5	8	5	8	10
Max. Single-Ended HP I/Os	208	208	416	624	416	624	624
GTY 32.75Gb/s Transceivers	32	32	64	96	64	96	32
GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	32
100G / 50G KP4 FEC	–	–	–	–	–	–	16/32
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	–	–	–	–	–	–	–
Footprint[3, 4, 5, 6] Dim. (mm)	HP I/O, GTY						HP I/O, GTY, GTM
H1924 45x45	208, 32						
H2104 47.5x47.5		208, 32	416, 64		416, 64		
H2892 55x55			416, 64	624, 96	416, 64	624, 96	
K2892 55x55							624, 32, 32

Virtex® UltraScale+™ FPGAs

RL

For clarity, accused products from the above-referenced table appear below:

- Virtex UltraScale+ FPGA Devices - VU31P, VU33P, VU35P, VU37P, VU45P, VU47P, VU57P

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Virtex devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx UltraScale+ FPGA Product Tables and Product Selection Guide, XMP103 (v1.21)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq® UltraScale+™ MPSoCs: CG Devices

		Device Name[1]	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core** ARM® Cortex™-A53 MPCore™ up to 1.3GHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor						
PS to PL Interface			12 x 32/64/128b AXI Ports						
le Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600
		CLB Flip-Flops (K)	94	141	176	234	429	461	548
		CLB LUTs (K)	47	71	88	117	215	230	274
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4
		DSP Slices	240	360	728	1,248	1,973	1,728	2,520

RL

For clarity, accused products from the above-referenced table appear below:

- Zynq UltraScale+ MPSoC: CG Devices - ZU2CG, ZU3CG, ZU4CG, ZU5CG, ZU6CG, ZU7CG, ZU9CG

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Zynq devices (DDR4, DDR3, DDR3L, LPDDR4, LPDDR3,External Quad-SPI, NAND, eMMC). Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx Zynq UltraScale+ MPSoC Product Tables and Product Selection Guide, XMP104 (v2.4)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq® UltraScale+™ MPSoCs: EG Devices

		Device Name[1]	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB										
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core										
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz										
		Memory	L2 Cache 64KB										
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC										
		Static Memory Interfaces	NAND, 2x Quad-SPI										
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet										
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO										
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains										
		Security	RSA, AES, and SHA										
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor										
PS to PL Interface			12 x 32/64/128b AXI Ports										
PL	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6

RL

For clarity, accused products from the above-referenced table appear below:

- Zynq UltraScale+ MPSoC: EG Devices - ZU2EG, ZU3EG, ZU4EG, ZU5EG, ZU6EG, ZU7EG, ZU9EG, ZU11EG, ZU15EG, ZU17EG, ZU19EG

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Zynq devices (DDR4, DDR3, DDR3L, LPDDR4, LPDDR3,External Quad-SPI, NAND, eMMC). Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx Zynq UltraScale+ MPSoC Product Tables and Product Selection Guide, XMP104 (v2.4)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq® UltraScale+™ MPSoCs: EV Devices

		Device Name[1]	ZU4EV	ZU5EV	ZU7EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB		
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz		
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core		
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz		
		Memory	L2 Cache 64KB		
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC		
		Static Memory Interfaces	NAND, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains		
		Security	RSA, AES, and SHA		
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor		
PS to PL Interface			12 x 32/64/128b AXI Ports		
Logic (PL)	Programmable Functionality	System Logic Cells (K)	192	256	504
		CLB Flip-Flops (K)	176	234	461
		CLB LUTs (K)	88	117	230
	Memory	Max. Distributed RAM (Mb)	2.6	3.5	6.2
		Total Block RAM (Mb)	4.5	5.1	11.0
		UltraRAM (Mb)	13.5	18.0	27.0
	Clocking	Clock Management Tiles (CMTs)	4	4	8

RP

For clarity, accused products from the above-referenced table appear below:

- Zynq UltraScale+ MPSoC: EV Devices - ZU4EV, ZU5EV, ZU7EV

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Zynq devices (DDR4, DDR3, DDR3L, LPDDR4, LPDDR3,External Quad-SPI, NAND, eMMC). Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx Zynq UltraScale+ MPSoC Product Tables and Product Selection Guide, XMP104 (v2.4)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
		Gen 1					Gen 2	Gen 3					
PS		Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5F MPCore up to 533MHz											
RF Data Converter	12-bit RF-ADC # of ADCs	0	8	8	8	16	16	–	–	–	–	–	–
	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–
	14-bit RF-ADC # of ADCs	–	–	–	–	–	–	8 2	4	8 4	8	8	16
	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	5.0	2.5
	14-bit RF-DAC # of DACs	0	8	8	8	16	16	8	4	12	8	8	16
	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0	10.0
	SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0
	Number of DDCs per RF-ADC[1]	0	1	1	1	1	1	1	2	1	1	1	1
	RF input Freq max. GHz			4			5			6			
	Decimation / Interpolation			1x, 2x, 4x, 8x			1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930
	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425
	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0
	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0
	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5
	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272
	GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–
	PCIeGen3 x16/Gen4 x8 / CCIX[2]	–	–	–	–	–	–	0	2	2	2	2	2
	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1
	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2
	System Monitor	1	1	1	1	1	1	1	1	1	1	1	1

Zynq® UltraScale+™ R

RL

For clarity, accused products from the above-referenced table appear below:

- Zynq UltraScale+ RFSoC Devices - ZU21DR, ZU25DR, ZU27DR, ZU28DR, ZU29DR, ZU39DR, ZU42DR, ZU43DR, ZU46DR, ZU47DR, ZU48DR, ZU49DR

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Zynq devices (DDR4, DDR3, DDR3L, LPDDR4, LPDDR3,External Quad-SPI, NAND, eMMC). Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx Zynq UltraScale+ RFSoC Product Tables and Product Selection Guide, XMP105 (v1.9)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Kintex® UltraScale™ FPGAs

	Device Name	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
Logic Resources	System Logic Cells (K)	318	444	530	726	1,088	1,176	1,451
	CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
	CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	4,230	5,908	7,050	9,180	13,770	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	360	540	600	1,080	1,620	1,680	2,160
	Block RAM/FIFO (18Kb each)	720	1,080	1,200	2,160	3,240	3,360	4,320
	Total Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
	I/O DLL	24	40	40	48	56	64	64
I/O Resources	Maximum Single-Ended HP I/Os	208	416	416	520	572	650	676
	Maximum Differential HP I/O Pairs	96	192	192	240	264	288	312
	Maximum Single-Ended HR I/Os	104	104	104	104	104	52	156
	Maximum Differential HR I/O Pairs	48	48	48	48	56	24	72
Integrated IP Resources	DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
	System Monitor	1	1	1	1	2	1	2
	PCIe® Gen1/2/3	1	2	3	3	4	4	6
	Interlaken	0	0	0	0	0	2	0
	100G Ethernet	0	0	0	0	0	2	0

RL

For clarity, accused products from the above-referenced table appear below:

- Kintex UltraScale FPGA Devices - KU025, KU035, KU040, KU060, KU085, KU095, KU115

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Virtex devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx UltraScale FPGA Product Tables and Product Selection Guide, XMP102 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Virtex® UltraScale™ FPGAs

	Device Name	XCVU065	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU440
Logic Resources	System Logic Cells (K)	783	975	1,176	1,567	2,027	2,350	5,541
	CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
	CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Memory Resources	Maximum Distributed RAM (Kb)	4,830	3,980	4,800	9,660	12,690	14,490	28,710
	Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
	Block RAM/FIFO (18Kb each)	2,520	2,842	3,456	5,040	6,552	7,560	5,040
	Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	16	16	20	28	30	30
	I/O DLL	40	64	64	80	120	120	120
	Transceiver Fractional PLL	5	8	8	10	13	15	0
I/O Resources	Maximum Single-Ended HP I/Os	468	780	780	780	650	650	1,404
	Maximum Differential HP I/O Pairs	216	360	360	360	300	300	648
	Maximum Single-Ended HR I/Os	52	52	52	52	52	52	52
	Maximum Differential HR I/O Pairs	24	24	24	24	24	24	24
Integrated IP Resources	DSP Slices	600	672	768	1,200	1,560	1,800	2,880
	System Monitor	1	1	1	2	3	3	3
	PCIe® Gen1/2/3	2	4	4	4	4	6	6
	Interlaken	3	6	6	6	8	9	0
	100G Ethernet	3	4	4	6	9	9	3
	GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48

RL

For clarity, accused products from the above-referenced table appear below:

- Virtex UltraScale FPGA Devices - XCVU065, XCVU080, XCVU095, VCVU125, XCVU160, XCVU190, XCVU440

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Virtex devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx UltraScale FPGA Product Tables and Product Selection Guide, XMP102 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Spartan-7 FPGAs

		I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V)					
	Part Number	XC7S6	XC7S15	XC7S25	XC7S50	XC7S75	XC7S100
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L

RL

For clarity, accused products from the above-referenced table appear below:

- Spartan 7-Series FPGA Devices - XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Spartan-7 devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx All Programmable 7 Series Product Selection Guide, XMP101 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Artix-7 FPGAs

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)							
	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max	2	4	4	4	4	8	8	16

RL

For clarity, accused products from the above-referenced table appear below:

- Artix 7-Series FPGA Devices - XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Artix-7 devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx All Programmable 7 Series Product Selection Guide, XMP101 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Kintex-7 FPGAs

		Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)						
	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]	—	—	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
	Total Block RAM (Kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2[2]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1

RL

For clarity, accused products from the above-referenced table appear below:

- Kintex 7-Series FPGA Devices - XC7K70T, XC7K160T, XC7K325T, XCE7K325T, XC7K355T, XCE7K355T, XC7K410T, XCE7K410T, XC7K420T, XCE7K420T, XC7K480T, XCE7K480T

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Kintex-7 devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx All Programmable 7 Series Product Selection Guide, XMP101 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Virtex-7 FPGAs

		Optimized for Highest System Performance and Capacity (1.0V)										
	Part Number	XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
	EasyPath™ Cost Reduction Solutions[1]	XCE7V585T	–	XCE7VX330T	XCE7VX415T	XCE7VX485T	XCE7VX550T	XCE7VX690T	XCE7VX980T	–	–	–
Logic Resources	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1,100	600	300
	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528	288	144
Integrated IP Resources	DSP Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCIe® Gen2[2]	3	4	–	–	4	–	–	–	–	–	–
	PCIe Gen3	–	–	2	2	–	2	3	3	4	2	3
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]	36	36	–	–	56	–	–	–	–	–	–

RL

For clarity, accused products from the above-referenced table appear below:

- Virtex 7-Series FPGA Devices - XC7V585T, XCE7V585T, XC7V2000T, XC7VX330T, XCE7VX330T, XC7VX415T, XCE7VX415T, XC7VX485T, XCE7VX485T, XC7VX550T, XCE7VX550T, XC7VX690T, XCE7VX690T, XC7VX980T, XCE7VX980T, XCVX1140T, XC7VH580T, XC7VH870T

FPGA's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Virtex-7 devices. Board level integration of FPGA's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx All Programmable 7 Series Product Selection Guide, XMP101 (v1.7)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq®-7000 SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
m (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz(1)			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	AXI 64b ACP 16 Interrupts									
mmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.2Mb	26.5Mb
	(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)	(265)	(500)	(545)	(755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8

RL

For clarity, accused products from the above-referenced table appear below:

- Zynq-7000 SoC Devices - XC7Z007S, XC7Z012S, XC7Z014S, XC7Z010, XC7Z015, XC7Z020, XC7Z030, XC7Z035, XC7Z045, XC7Z100

SoC's are typically used in designs including external memory, like the **(D) DRAM memory** → external memory devices supported by Zynq-7000 devices. Board level integration of SoC's connected or coupled to **(D) DRAM memory** → external memory creates a **(CS) computer system**.

Source: Xilinx Zynq-7000 SoC Product Selection Guide, XMP097 (v1.3.2)

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a reconfigurable logic device having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC). **D**

Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input look-up table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s. **D**
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to max. rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.
- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.
- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering.

Source: Xilinx 7 Series FPGAs Data Sheet: Overview, DS180 (v2.6), February 27, 2018
Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

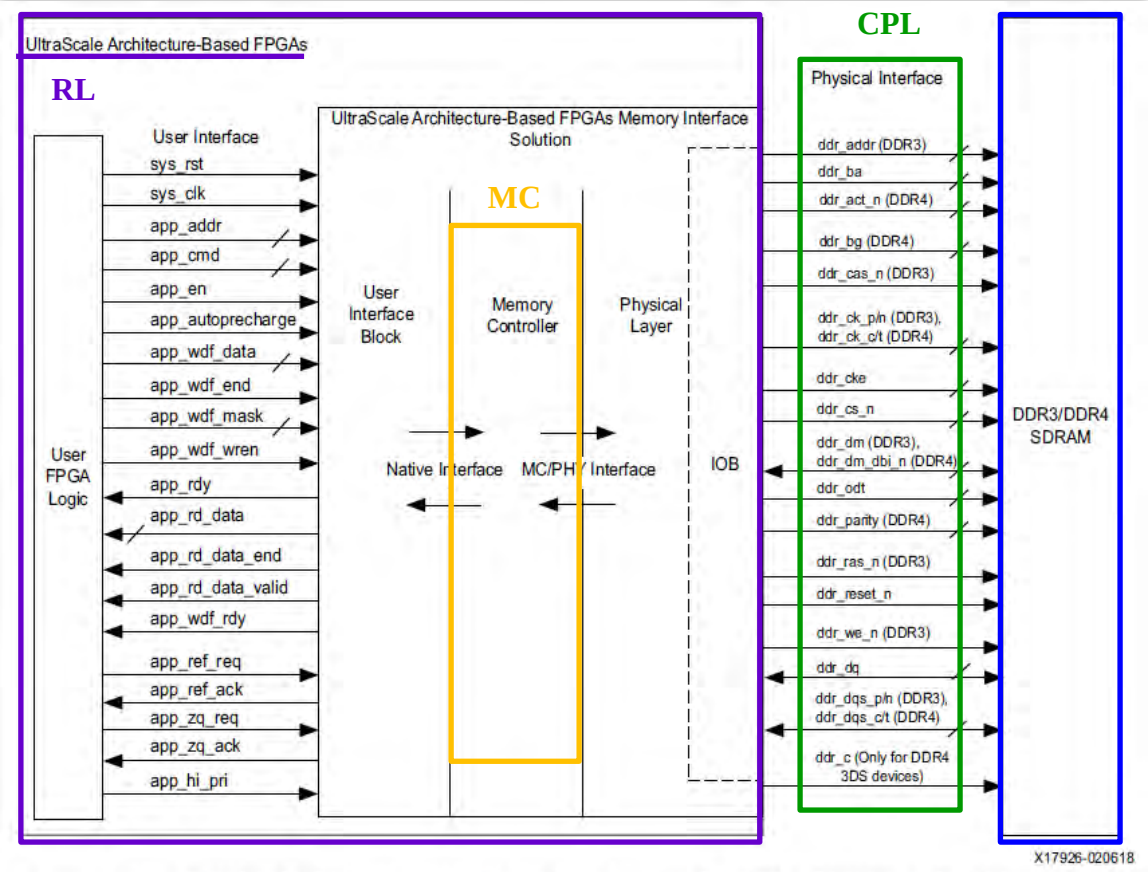


Figure 1-1: **UltraScale Architecture-Based FPGAs DDR3/DDR4 Memory Interface Solution**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

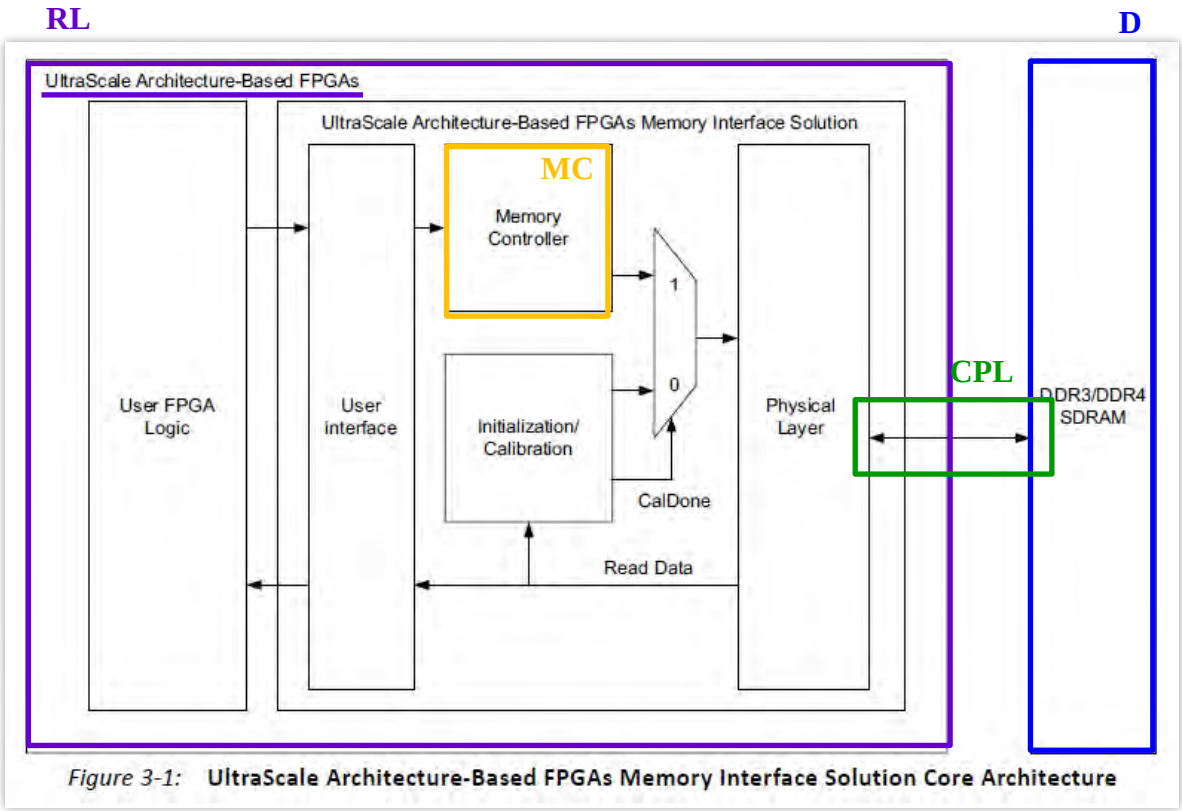


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

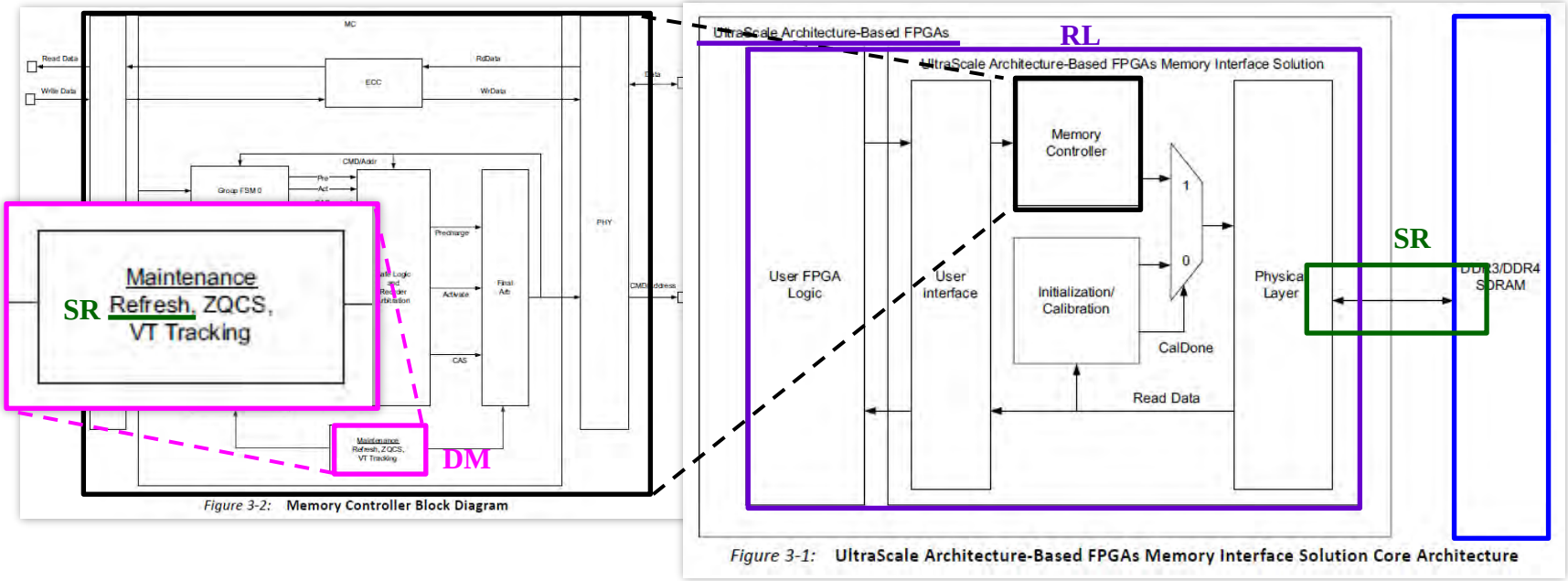
Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

D



DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 1

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh **SIL**

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

SIL

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R **RL**

Partial Reconfiguration **SR**

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

Exhibit D – U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Family Comparisons

Table 1: **Device Resources**

RL

FPGA

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,143	783–5,541	862–8,938	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–16		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–2,072	82–668	280–408

Source: Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Application Overview

RL

Zynq UltraScale+ MPSoC is the Xilinx second-generation Zynq platform, combining a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system features the Arm® flagship Cortex®-A53 64-bit quad-core or dual-core processor and Cortex-R5 dual-core real-time processor. In addition to the cost and integration benefits previously provided by the Zynq-7000 devices, the Zynq UltraScale+ MPSoC and RFSoC devices also provide these new features and benefits.

Power Management Framework

Introduction

The Zynq® UltraScale+™ MPSoC is the industry's first heterogeneous multiprocessor SoC (MPSoC) that combines multiple user programmable processors, FPGA, and advanced power management capabilities.

FPGA

Source: Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019
Xilinx Zynq UltraScale+ MPSoC Software Developer Guide, UG1137 (v11.0) December 5, 2019

Exhibit D – U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

RL

General Description **FPGA**

Xilinx® 7 series FPGAs comprise four FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series FPGAs include:

- Spartan®-7 Family: Optimized for low cost, lowest power, and high I/O performance. Available in low-cost, very small form-factor packaging for smallest PCB footprint.
- Artix®-7 Family: Optimized for low power applications requiring serial transceivers and high DSP and logic throughput. Provides the lowest total bill of materials cost for high-throughput, cost-sensitive applications.
- Kintex®-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex®-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Source: Xilinx 7 Series FPGAs Data Sheet: Overview, DS180 (v2.6), February 27, 2018

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

RL

Table 1: **Zynq-7000 and Zynq-7000S SoCs *(Cont'd)***

	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent **FPGA**	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Block RAM (# 36 Kb Blocks)	1.8 Mb (50)	2.5 Mb (72)	3.8 Mb (107)	2.1 Mb (60)	3.3 Mb (95)	4.9 Mb (140)	9.3 Mb (265)	17.6 Mb (500)	19.2 Mb (545)	26.5 Mb (755)
	DSP Slices (18x25 MACCs)	66	120	170	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	73 GMACs	131 GMACs	187 GMACs	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express (Root Complex or Endpoint)(3)		Gen2 x4			Gen2 x4		Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication									

Source: Xilinx Zinq-7000 SoC Data Sheet: Overview, DS 190 (v1.11.1) July 2 , 2018

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

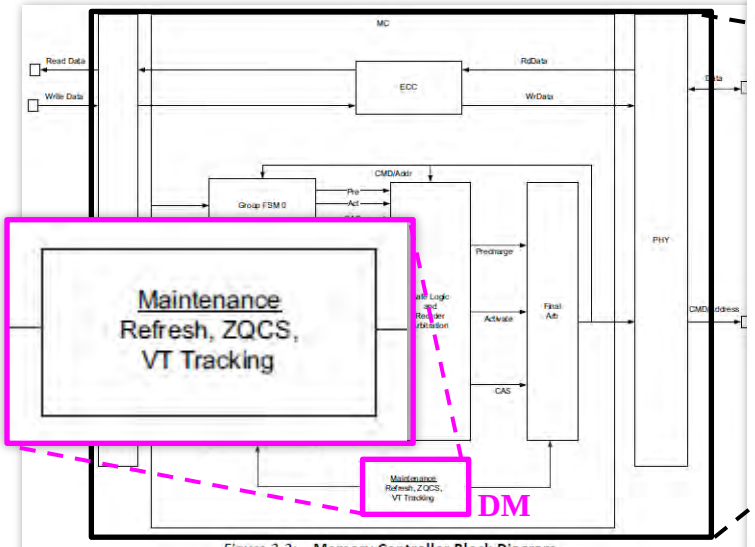


Figure 3-2: **Memory Controller Block Diagram**

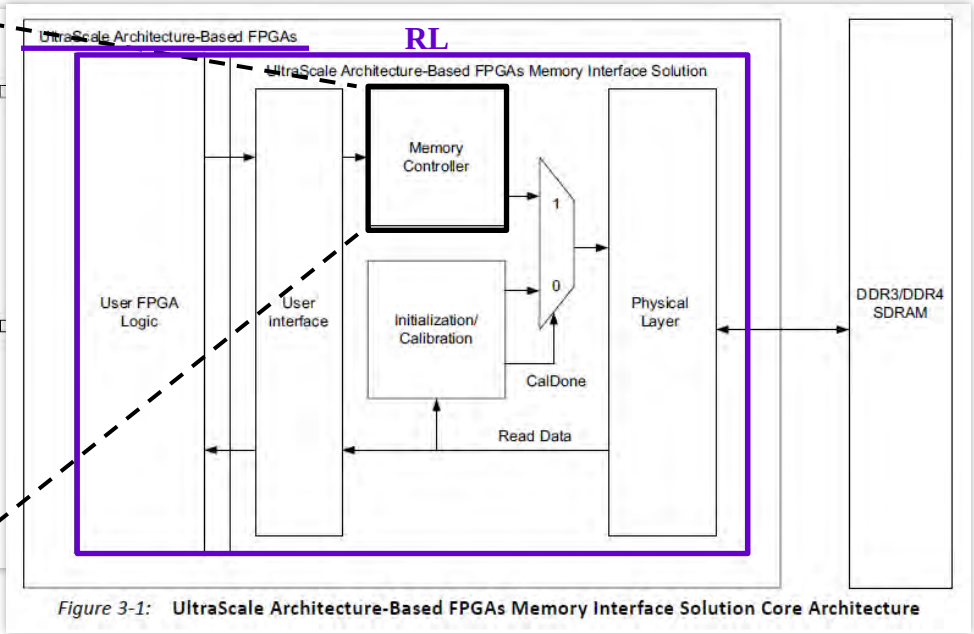


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit D - U.S. Patent No. 9,153,311 – Xilinx UltraScale+, UltraScale, Zynq-7000 All Programmable SoC, 7 series FPGA's

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is **(HSR) operable to hold said DRAM memory in self-refresh mode** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh HSR

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

HSR

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R **RL**

Partial Reconfiguration

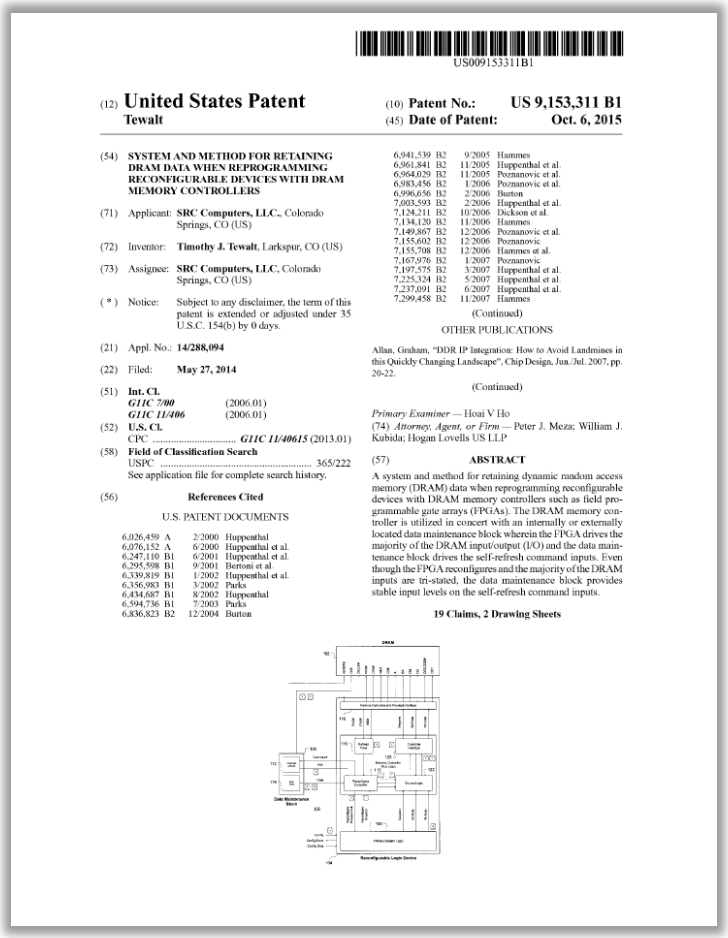
The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration; it is used to hold/keep the DRAM memory in self-refresh mode.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

EXHIBIT E

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits



US009153311B1

(12) **United States Patent**
Tewalt

(10) **Patent No.: US 9,153,311 B1**
(45) **Date of Patent: Oct. 6, 2015**

(54) **SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS**

(71) Applicant: **SRC Computers, LLC**, Colorado Springs, CO (US)

(72) Inventor: **Timothy J. Tewalt**, Larkspur, CO (US)

(73) Assignee: **SRC Computers, LLC**, Colorado Springs, CO (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/288,094**

(22) Filed: **May 27, 2014**

(51) **Int. Cl.**
G11C 7/00 (2006.01)
G11C 11/406 (2006.01)

(52) **U.S. Cl.**
CPC ***G11C 11/40615*** (2013.01)

(58) **Field of Classification Search**
USPC 365/222
See application file for complete search history.

(56) **References Cited**

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(Continued)

Primary Examiner — Hoai V Ho
(74) *Attorney, Agent, or Firm* — Peter J. Meza; William J. Kubida; Hogan Lovells US LLP

(57) **ABSTRACT**

A system and method for retaining dynamic random access memory (DRAM) data when reprogramming reconfigurable devices with DRAM memory controllers such as field programmable gate arrays (FPGAs). The DRAM memory controller is utilized in concert with an internally or externally located data maintenance block wherein the FPGA drives the majority of the DRAM input/output (I/O) and the data maintenance block drives the self-refresh command inputs. Even though the FPGA reconfigures and the majority of the DRAM inputs are tri-stated, the data maintenance block provides stable input levels on the self-refresh command inputs.

19 Claims, 2 Drawing Sheets

Title: SYSTEM AND METHOD FOR RETAINING DRAM DATA WHEN REPROGRAMMING RECONFIGURABLE DEVICES WITH DRAM MEMORY CONTROLLERS

Priority Date: May 27, 2014

Filed Date: May 27, 2014

Issued Date: Oct. 06, 2015

Expiration Date: May 27, 2034

Inventor: Timothy J. Tewalt

Exemplary Claims: 1, 3, 9, 10

Claim 1

A **(CS) computer system** comprising:

a **(D) DRAM memory**;

a **(RL) reconfigurable logic device** having a (MC) **memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is operable to hold said **(D) DRAM memory** in **(SR) self-refresh mode** while said **reconfigurable logic device** is **(R) reconfigured**.

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

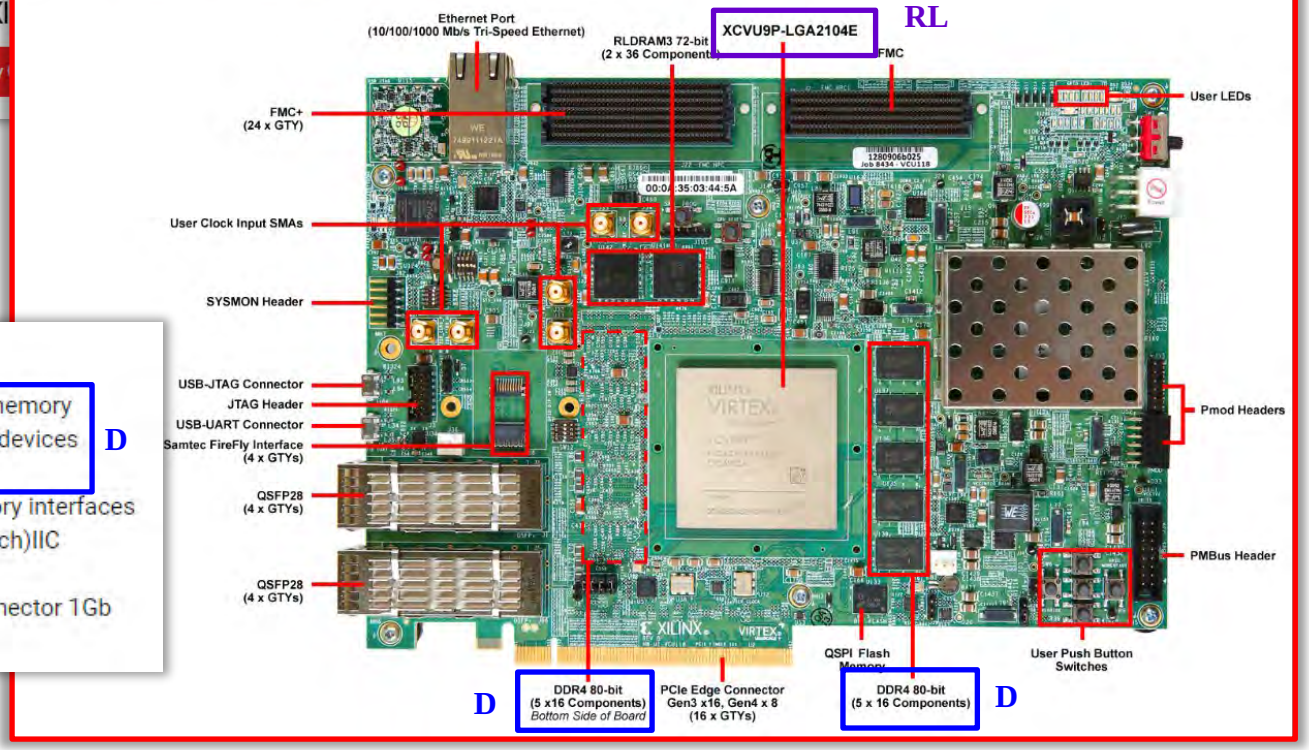
A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit

Price: $6,995
Part Number: EK-U1-VCU118-G
Lead Time: 4 Weeks
Device

CS

Featuring the **Virtex® UltraScale+™ XCVU9P-L2FLGA2104E FPGA**



Memory

- Two 4 GB DDR4 component memory interfaces (five [256 Mb x 16] devices each) **D**
- 4 MB RLD3 component memory interfaces (five [256 Mb x 16] devices each)IIC EEPROM: 8Kb
- Micro Secure Digital (SD) connector 1Gb Quad SPI Flash

Source: https://www.xilinx.com/products/boards-and-kits/vcu118.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

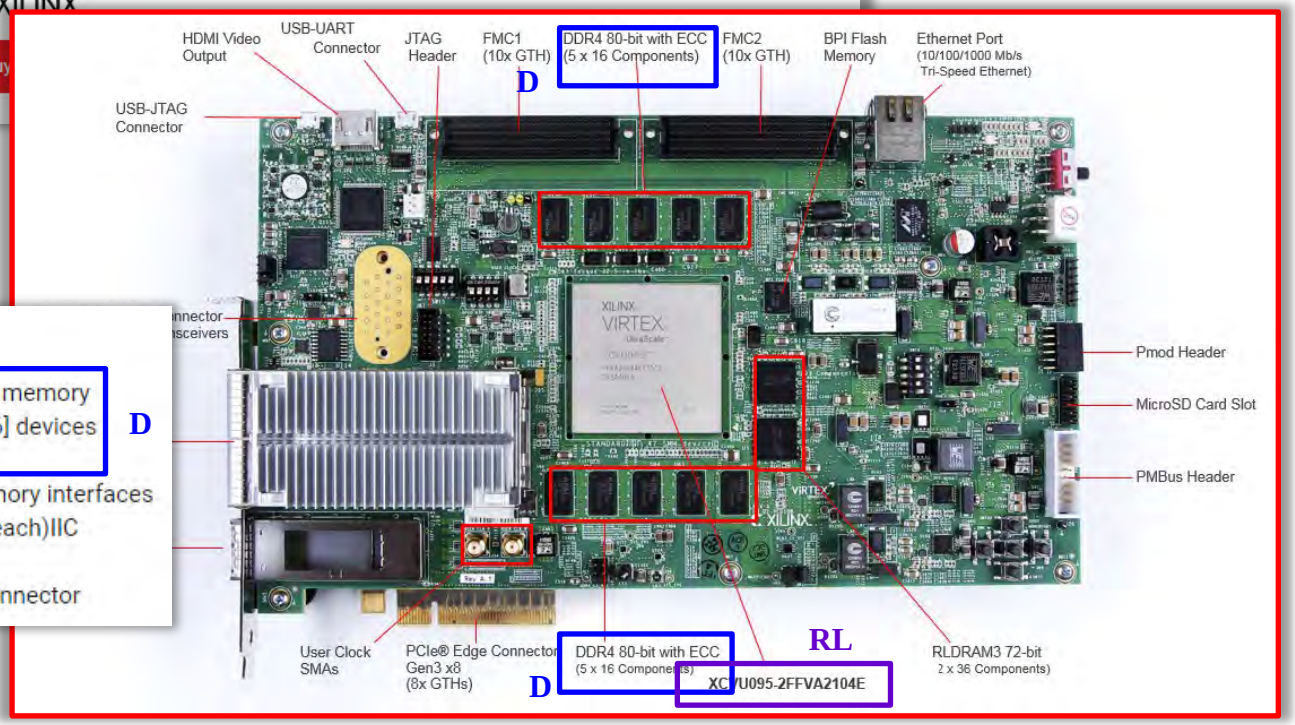
Xilinx Virtex UltraScale FPGA VCU108 Evaluation Kit

Price: $5,995
Part Number: EK-U1-VCU108-G
Lead Time: 2 Weeks
Device Support: Virtex UltraScale

XILINX

Buy

CS



Memory

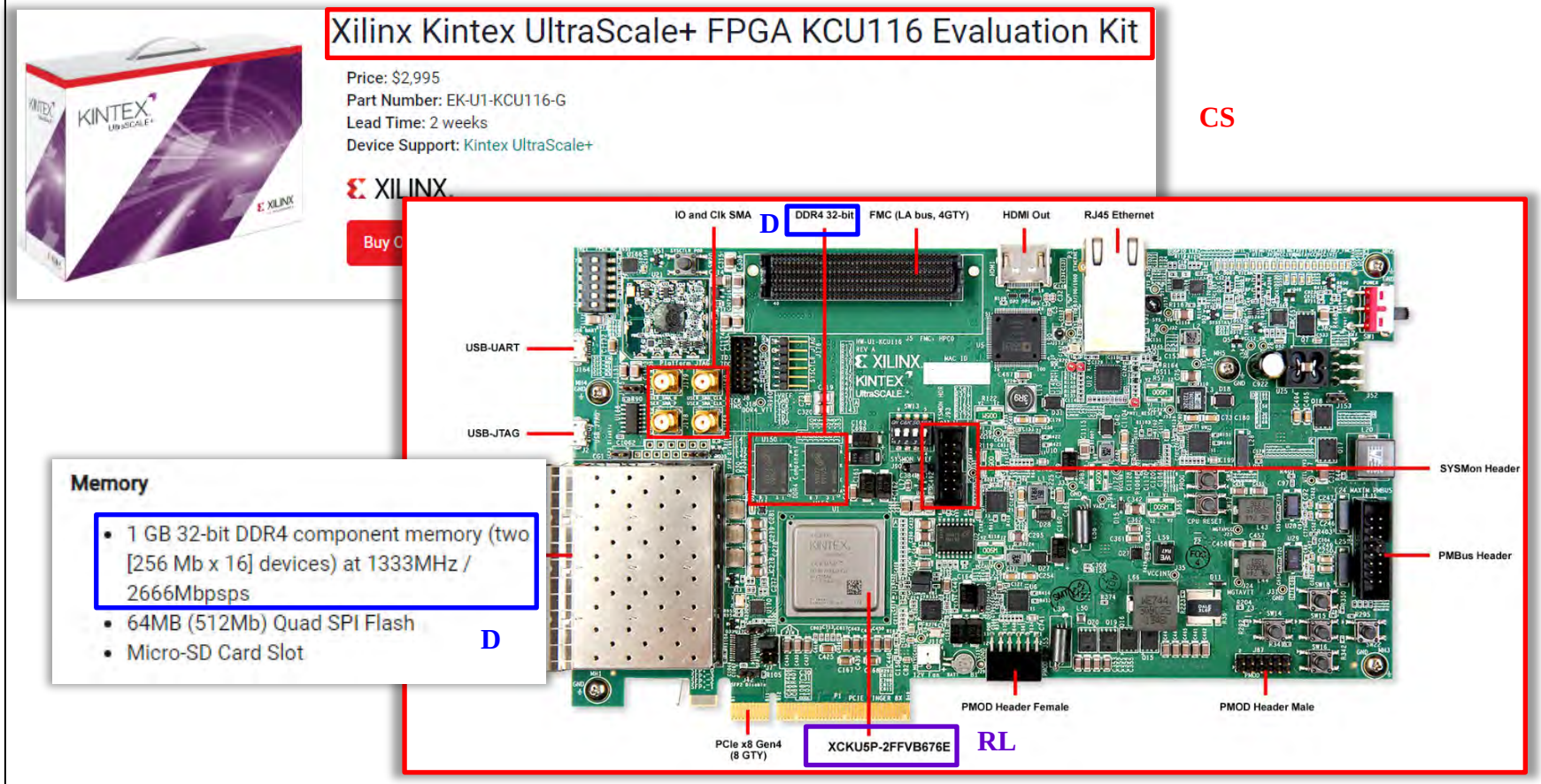
- Two 4 GB DDR4 component memory interfaces (five [256 Mb x 16] devices each) **D**
- 4 MB RLD3 component memory interfaces (five [256 Mb x 16] devices each)IIC EEPROM: 8Kb
- Micro Secure Digital (SD) connector

Source: https://www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: https://www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit

Price: $2,995
Part Number: EK-U1-KCU105-G
Lead Time: 2 Weeks
Device Support: Kintex UltraScale

XILINX

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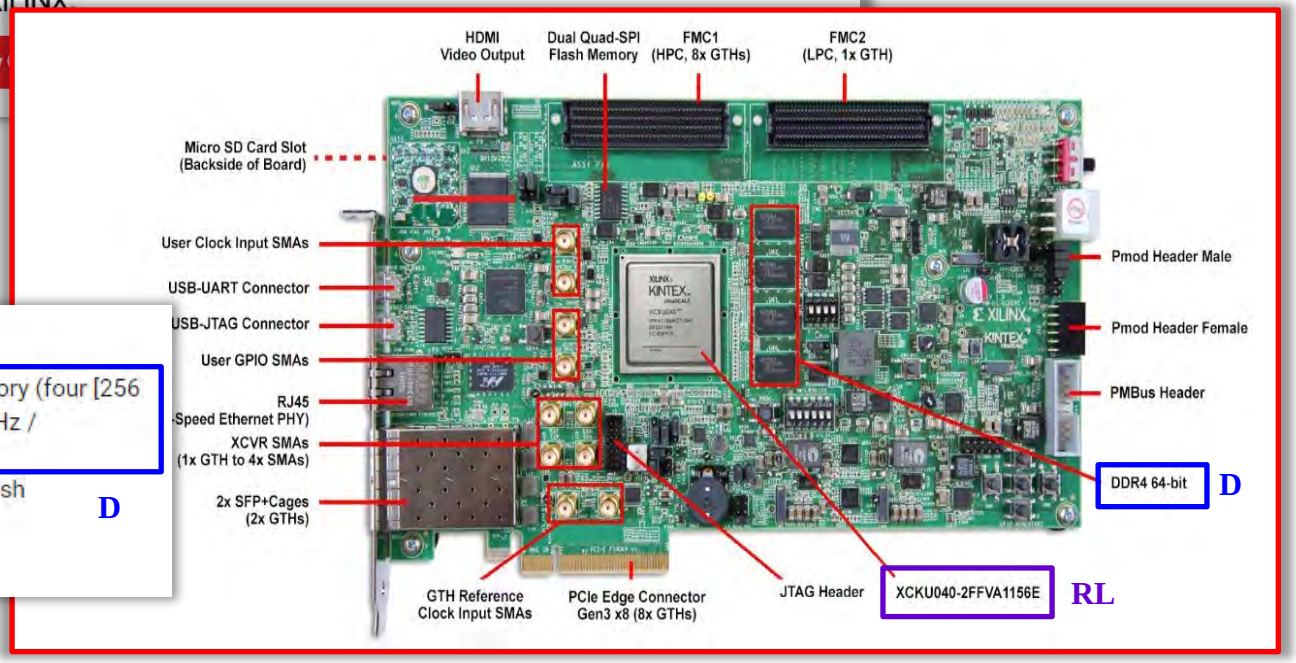
CS

Memory

- 2GB DDR4 component memory (four [256 Mb x 16] devices) at 1200MHz / 2400Mbpsps
- 64MB (512Mb) Quad SPI Flash
- 8Kb IIC EEPROM
- Micro SD Card Slot

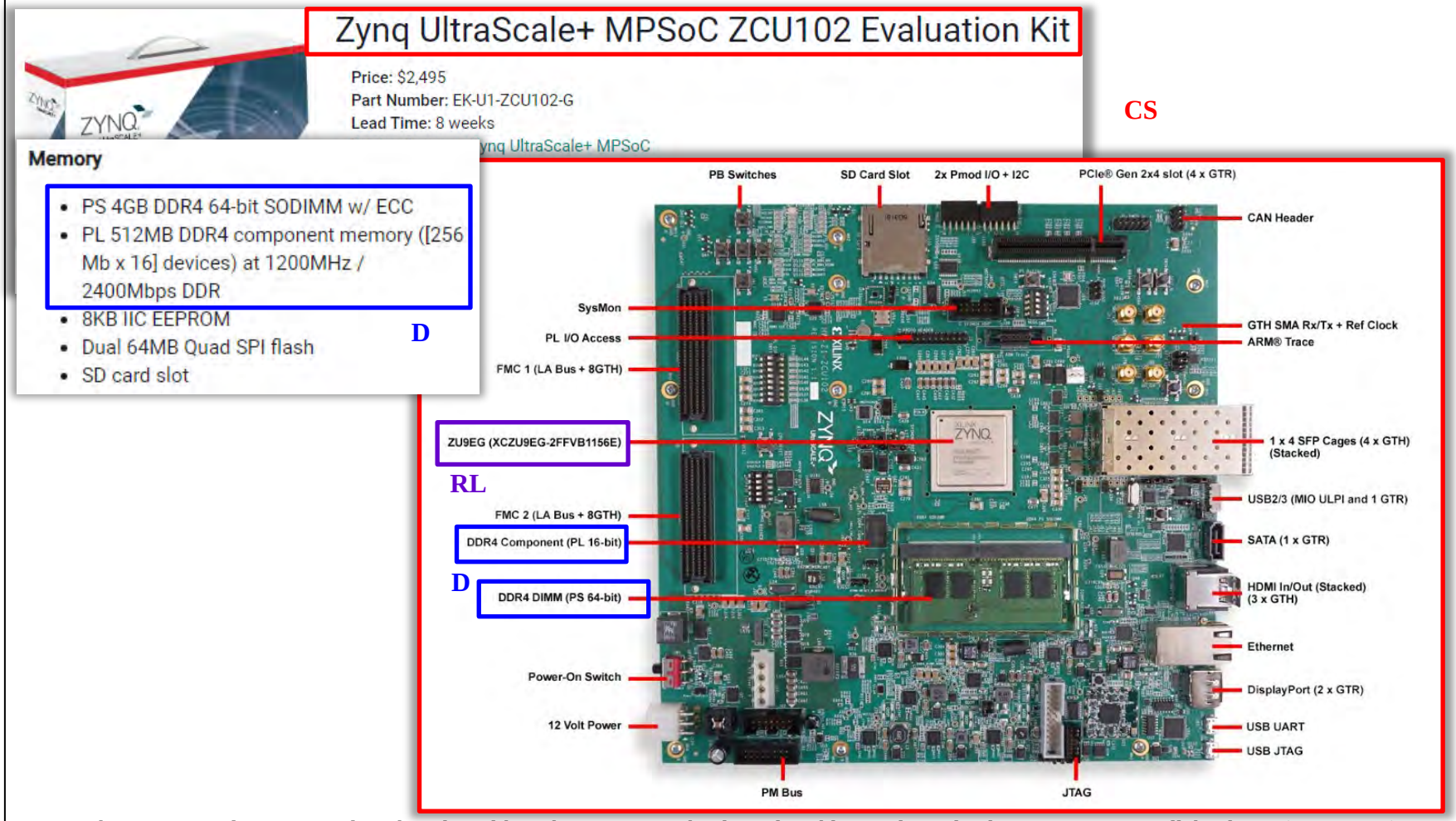
D



Source: https://www.xilinx.com/products/boards-and-kits/kcu105.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

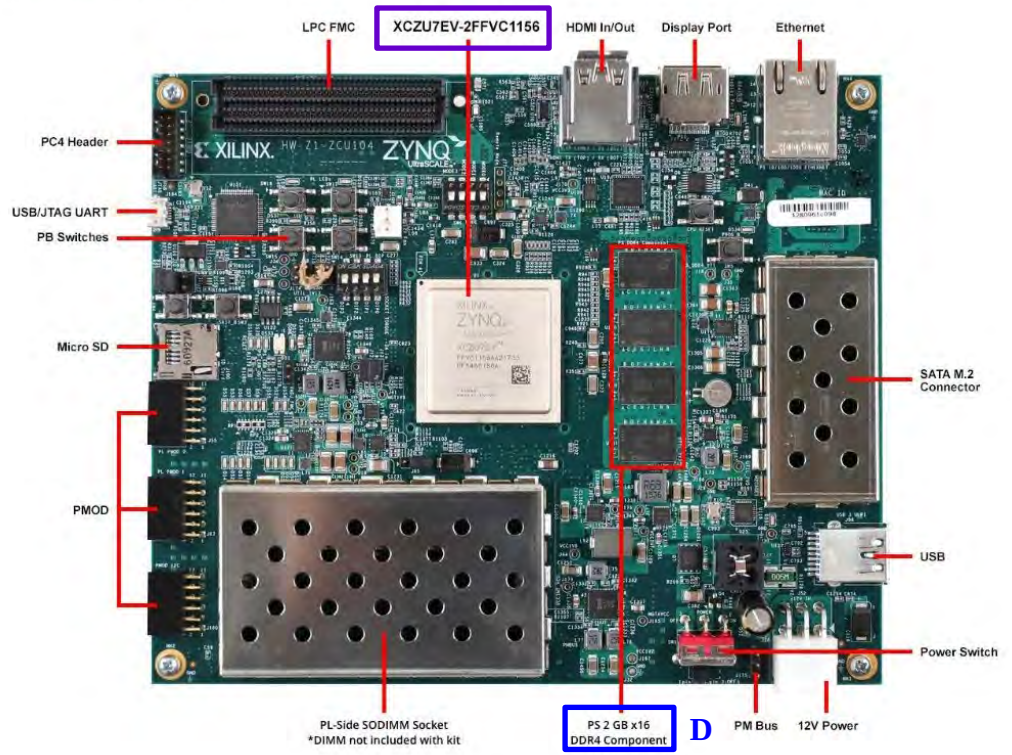
Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit

Price: $1,295
Part Number: EK-U1-ZCU104-G

CS

Featuring the Zynq UltraScale+ **XCZU7EV-2FFVC1156 MPSoC**

RL



D

Memory

- PS DDR4 64-bit Component
- Quad-SPI flash
- Micro SD card slot

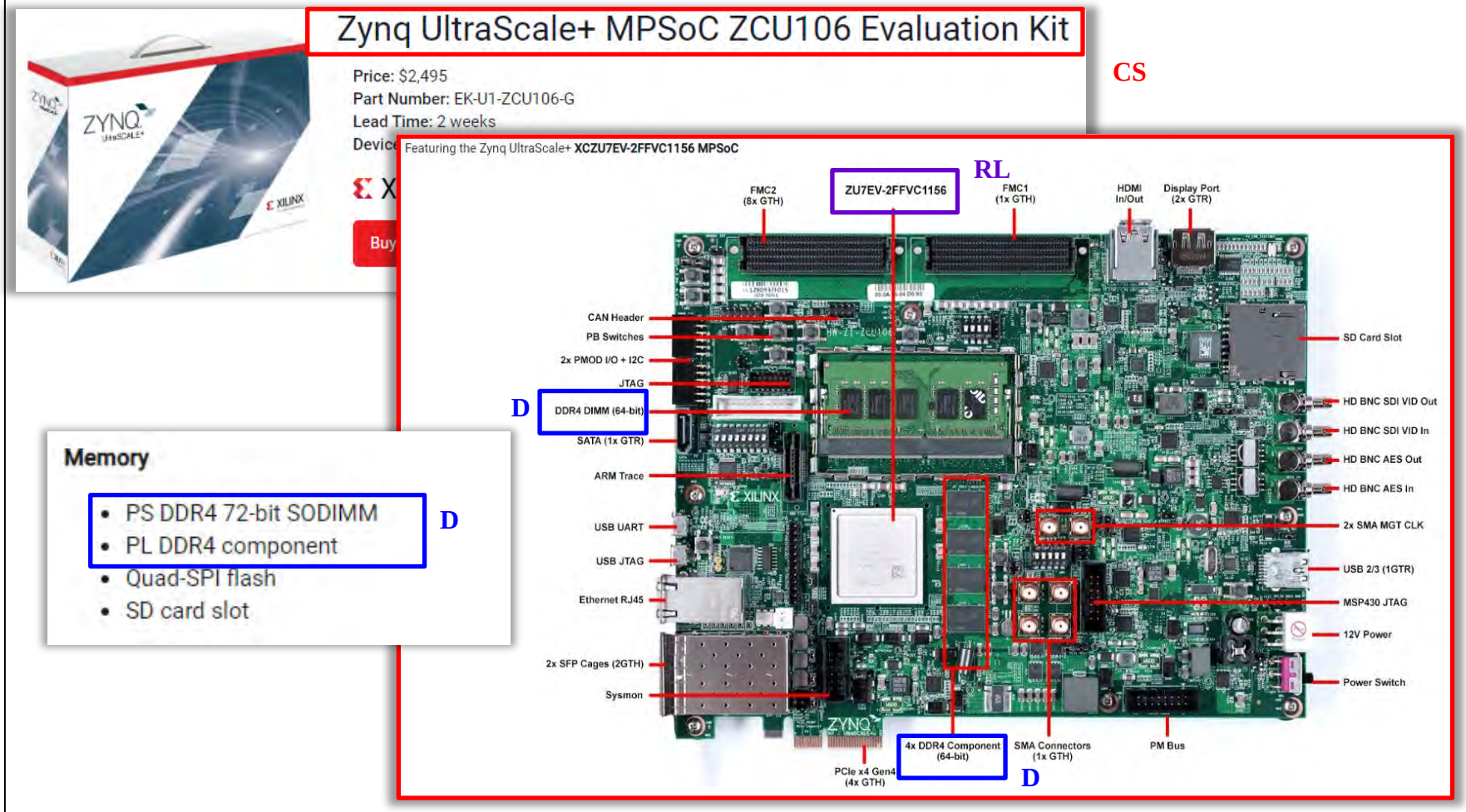
D

Source: https://www.xilinx.com/products/boards-and-kits/zcu104.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: https://www.xilinx.com/products/boards-and-kits/zcu106.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

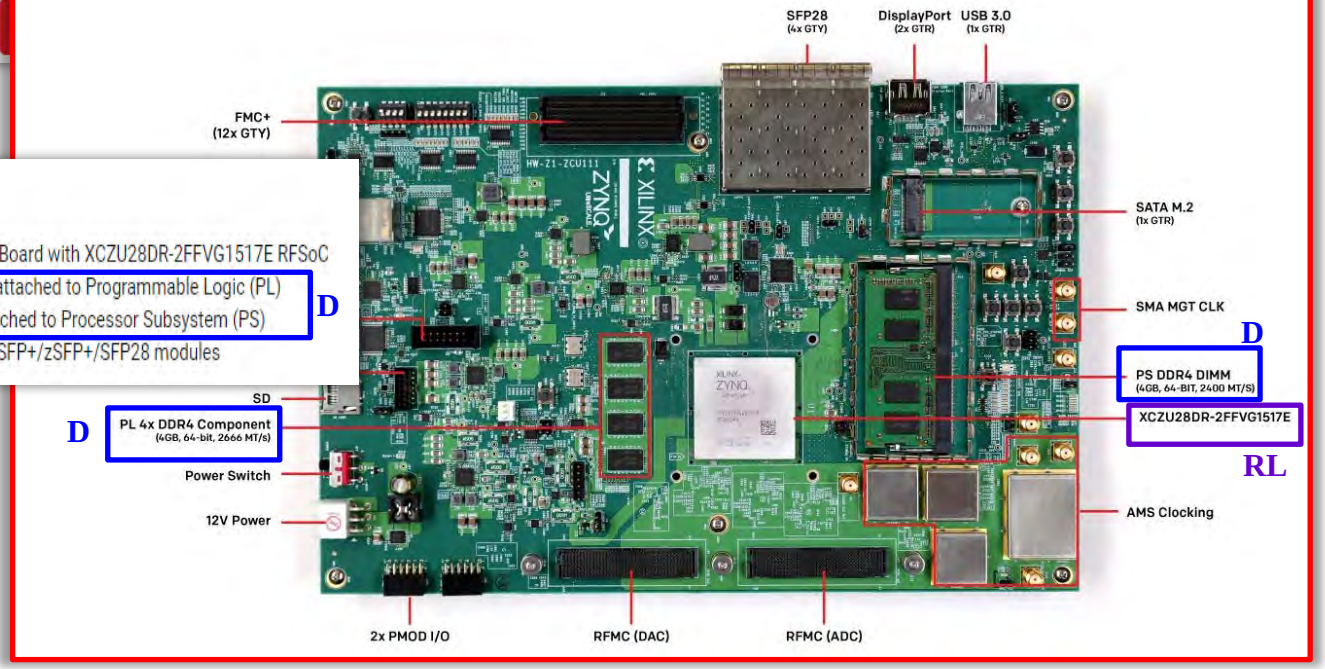
A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit

Price: $8,995
Part Number: EK-U1-ZCU111-G
Lead Time: 5 weeks
Device Support: Zynq UltraScale+ RFSoC

CS

Featuring the Zynq® UltraScale+™ XCZU28DR-2FFVG1517E RFSoC



Key Features & Benefits

- Zynq UltraScale+ RFSoC ZCU111 Evaluation Board with XCZU28DR-2FFVG1517E RFSoC
- DDR4 Component – 4GB, 64-bit, 2666MT/s, attached to Programmable Logic (PL)
- DDR4 SODIMM – 4GB 64-bit, 2400MT/s, attached to Processor Subsystem (PS)
- Ganged SFP28 cage to support up to 4 SFP/SFP+/zSFP+/SFP28 modules

D

Source: https://www.xilinx.com/products/boards-and-kits/zcu111.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#overview (07/17/2020)
https://www.xilinx.com/products/boards-and-kits/zcu111.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#specifications (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit

Price: $19,995
Part Number: CK-U1-ZCU1275-G
Lead Time: 5 weeks
Device Support: Zynq UltraScale+ RFSoC

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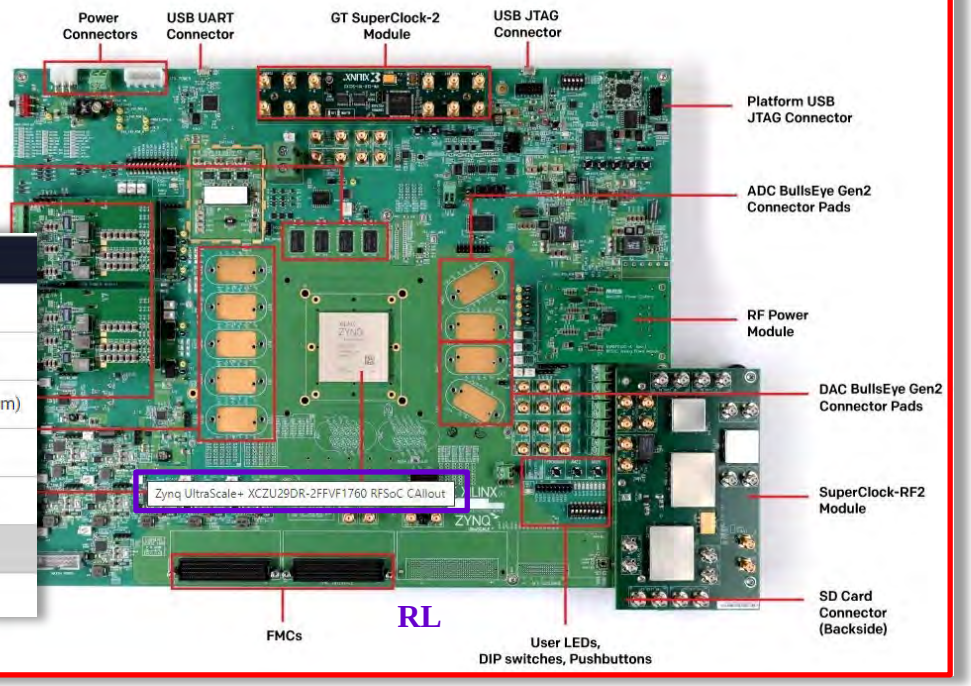
Buy

CS

Featuring the Zynq® UltraScale+™ **XCZU29DR-2FFVF1760** RFSoC



Board Specifications	Value
Length	16 inch (40.6 cm)
Height	12.6 inch (30.0 cm)
Thickness (+/-5%)	0.13456 inch (0.3418 cm)
Operating Environmental Temperature	0°C to +45°C
Storage Environmental Temperature	-25°C to +60°C
Memory	
PS DDR3 Component	4x2GB

D

Source: https://www.xilinx.com/products/boards-and-kits/zcu1275.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#specifications (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq UltraScale+ RFSoC ZCU1285 Characterization Kit

Price: $24,995
Part Number: CK-U1-ZCU1285-G
Lead Time: 5 weeks
Device Support: Zynq UltraScale+ RFSoC

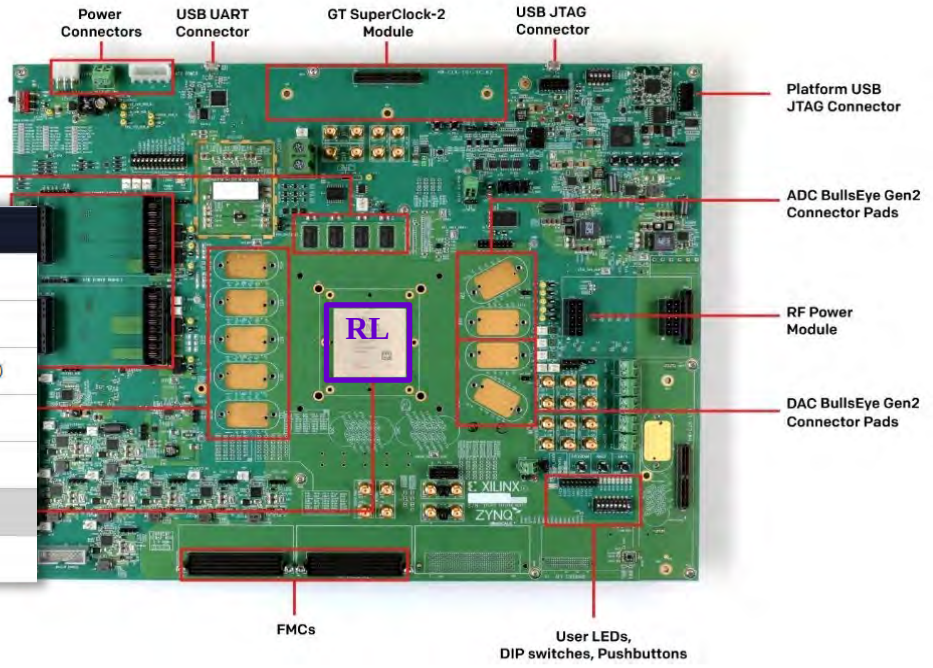
XILINX

Buy

CS

Featuring the Zynq® UltraScale+™ **XCZU39DR-2FFVF1760I** RFSoC

RL



D

PS 4x DDR3 Component (2GB, 16-bit, 2133MT/s)

Board Specifications	Value
Length	16 inch (40.6 cm)
Height	12.6 inch (30.0 cm)
Thickness (+/-5%)	0.13456 inch (0.3418 cm)
Operating Environmental Temperature	0°C to +45°C
Storage Environmental Temperature	-25°C to +60°C
Memory	
PS DDR3 Component	4x2GB

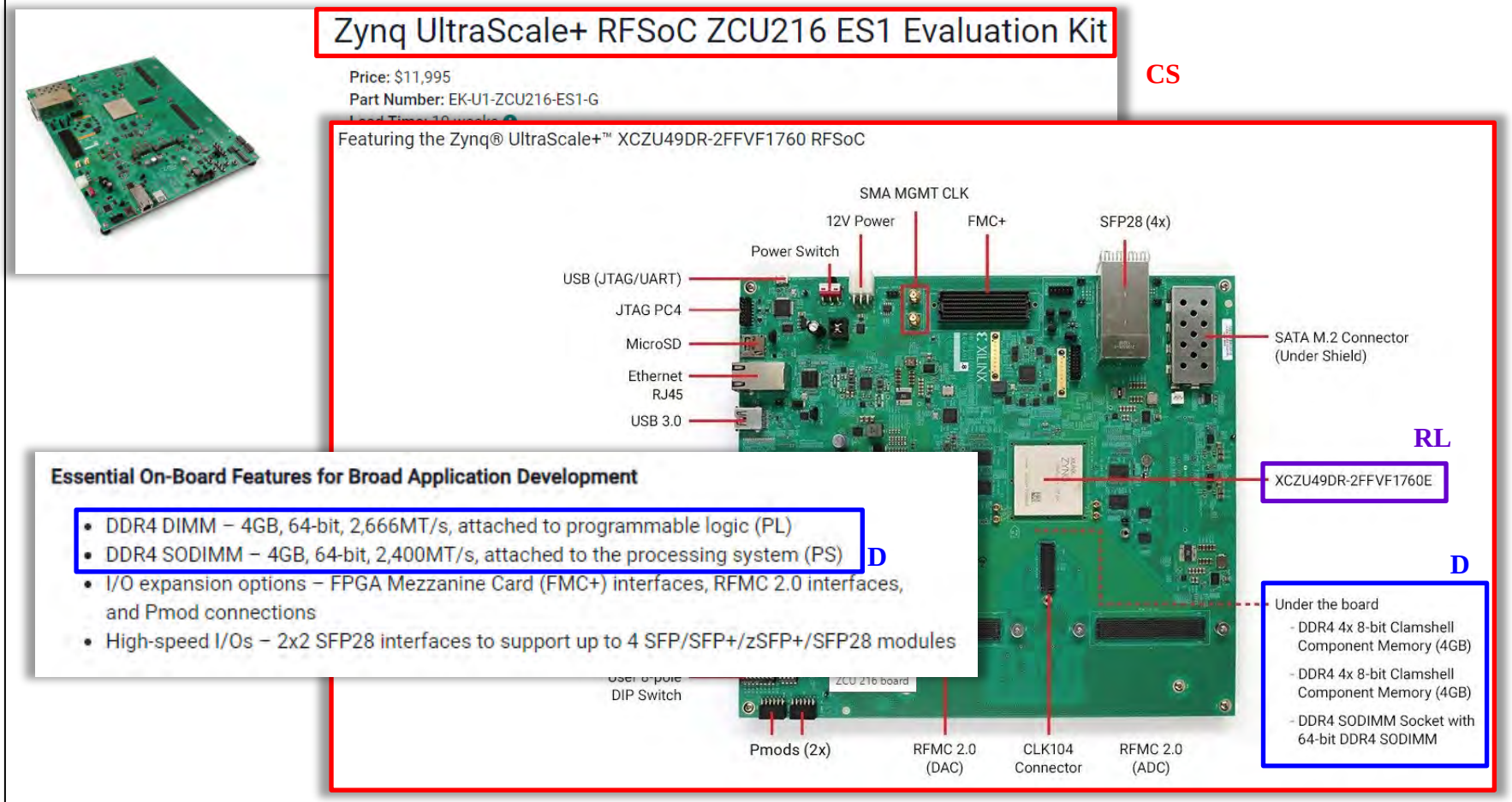
D

Source: https://www.xilinx.com/products/boards-and-kits/zcu1285.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#specifications (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and



Source: https://www.xilinx.com/products/boards-and-kits/zcu216.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#overview (07/17/2020)
https://www.xilinx.com/products/boards-and-kits/zcu216.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#specifications (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Zynq UltraScale+ RFSoC ZCU208 ES1 Evaluation Kit

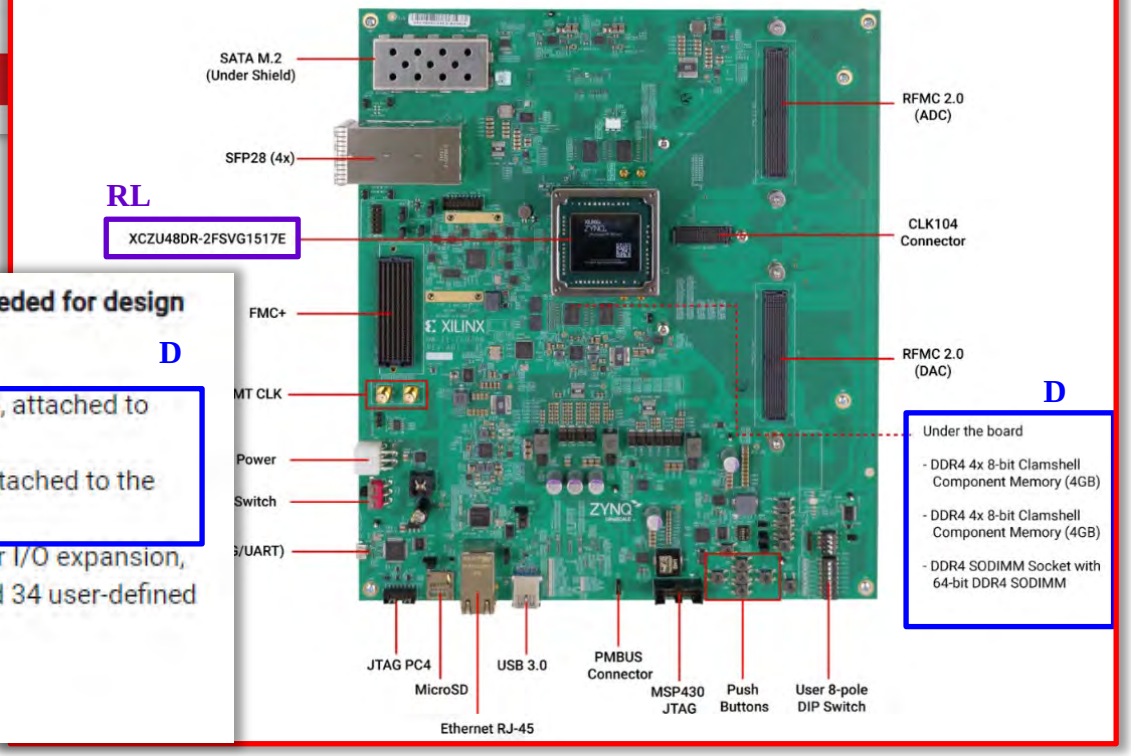
Price: $10,995
Part Number: EK-U1-ZCU208-ES1-G
Lead Time: 6 weeks
Device Support: Zynq U

XILINX.

Buy Online

CS

Featuring the Zynq® UltraScale+™ XCZU48DR-2FSVG1517E RFSoC



Comes equipped with all board-level features needed for design development

D

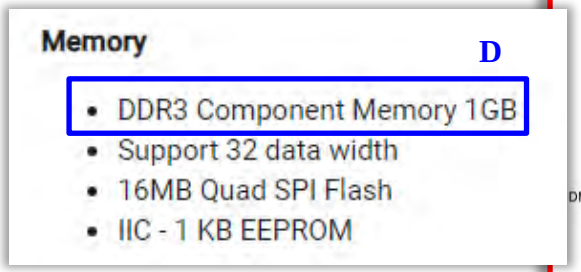
- DDR4 Component – 4GB, 64-bit, 2666MT/s, attached to programmable logic (PL)
- DDR4 SODIMM – 4GB 64-bit, 2400MT/s, attached to the processing subsystem (PS)
- FPGA Mezzanine Card (FMC+) interface for I/O expansion, including 12x 33Gb/s GTY transceivers and 34 user-defined differential I/O signals
- Quad zSFP/zSFP+ cage assembly
- 8 user-I/O, single-color LEDs

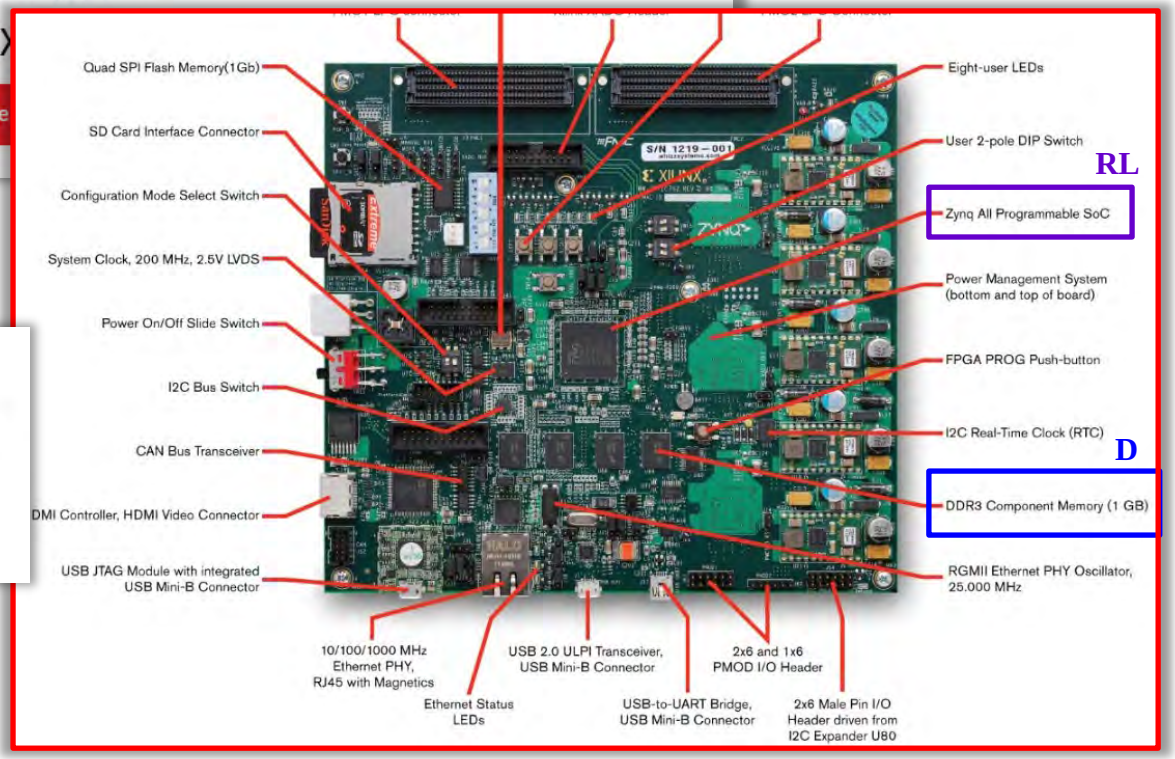
Source: https://www.xilinx.com/products/boards-and-kits/zcu208.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#overview (07/17/2020)
https://www.xilinx.com/products/boards-and-kits/zcu208.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#specifications (07/17/2020)

Exhibit E - U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and





Source: https://www.xilinx.com/products/boards-and-kits/ek-z7-zc702-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

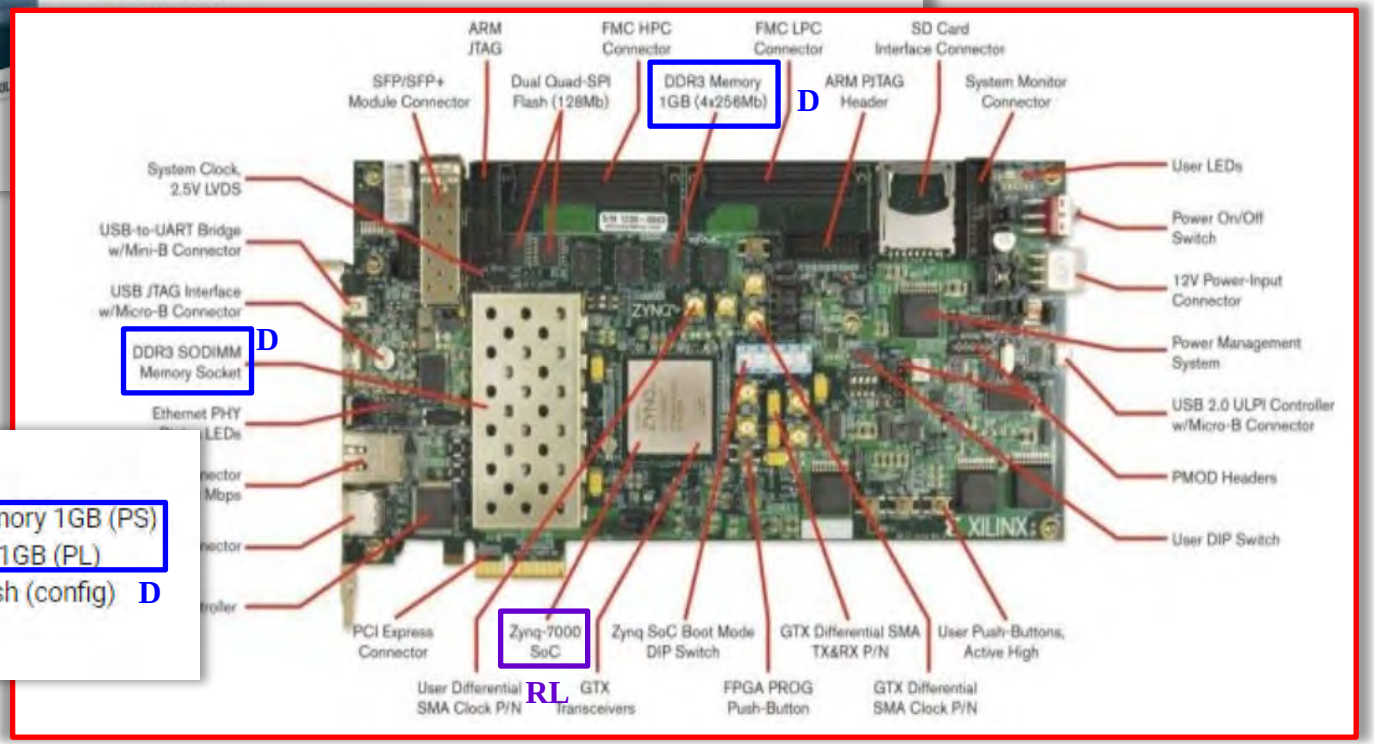
Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Xilinx Zynq-7000 SoC ZC706 Evaluation Kit

Price: $2,495
Part Number: EK-Z7-ZC706-G
Lead Time: 2 Weeks
Device Support: Zynq-7000

CS



Memory

- DDR3 Component Memory 1GB (PS)
- DDR3 SODIM Memory 1GB (PL)
- 2X16MB Quad SPI Flash (config) **D**
- IIC - 1 KB EEPROM

Source: https://www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

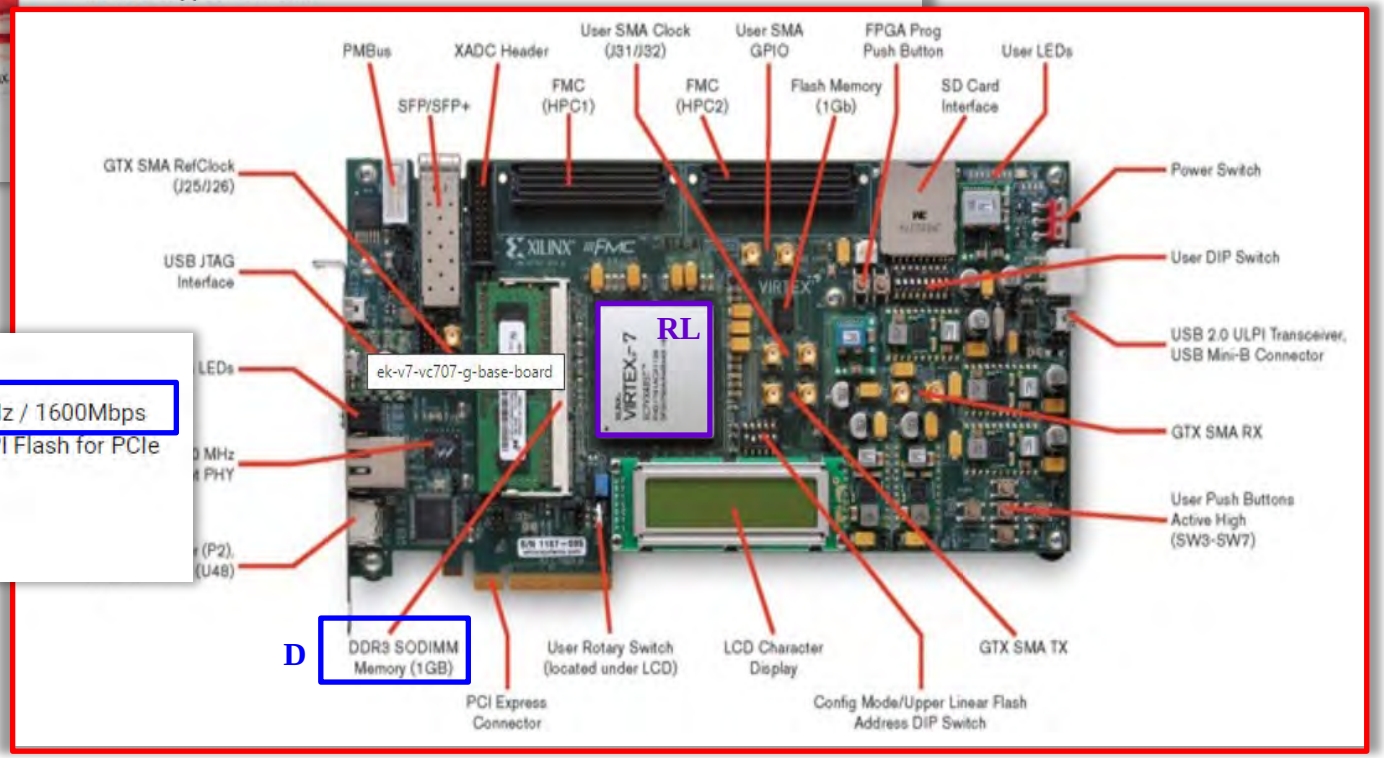
Xilinx Virtex-7 FPGA VC707 Evaluation Kit

Price: $3,495
Part Number: EK-V7-VC707-G
Lead Time: 2 Weeks
Device Support: Virtex-7

CS

Memory D

- 1GB DDR3 SODIMM 800MHz / 1600Mbps
- 128MB (1024Mb) Linear BPI Flash for PCIe Configuration
- SD Card Slot
- 8Kb IIC EEPROM



Source: https://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

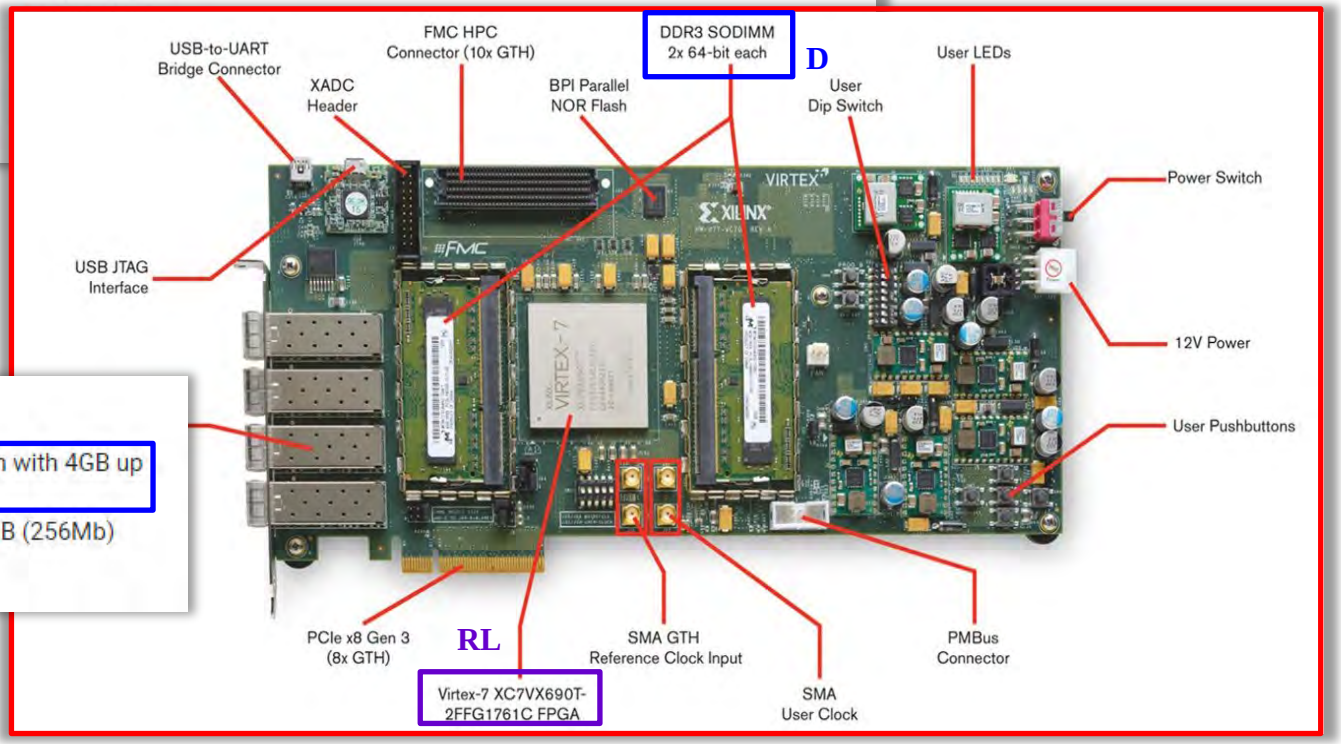
Claim 1

A **(CS) computer system** comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Xilinx Virtex-7 FPGA VC709 Connectivity Kit

Price: $4,995
Part Number: DK-V7-VC709-G
Lead Time: 2 Weeks
Device Support: Virtex-7

CS



Memory **D**

- DDR3 SODIMM (qty 2) - each with 4GB up to 933MHz / 1866Mbps
- BPI Parallel NOR Flash: 32MB (256Mb)
- IIC EEPROM: 1KB (8Kb)

Source: https://www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html?resultsTablePreSelect=xlnxdocumenttypes:SeeAll#hardware (07/17/2020)

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a reconfigurable logic device having a memory controller coupled to selected inputs and outputs of said **(D) DRAM memory**; and

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as hybrid memory cube (HMC). **D**

Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input look-up table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s. **D**
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to max. rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.
- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.
- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering.

Source: Xilinx 7 Series FPGAs Data Sheet: Overview, DS180 (v2.6), February 27, 2018
Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

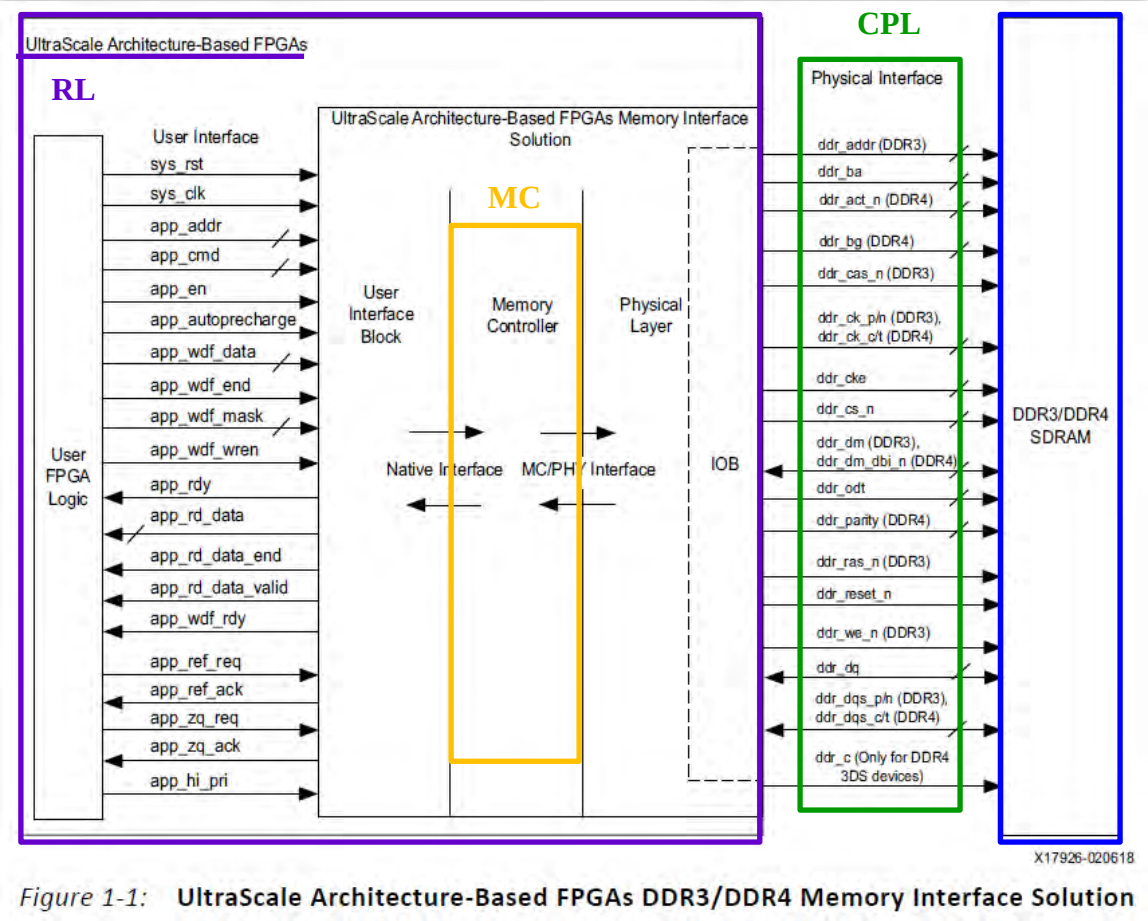


Figure 1-1: **UltraScale Architecture-Based FPGAs DDR3/DDR4 Memory Interface Solution**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Exhibit E – U.S. Patent No. 9,153,311 – Xilinx Evaluation, Characterization, and Connectivity Kits

Claim 1

A computer system comprising:
a **(D) DRAM memory**;
a **(RL) reconfigurable logic device** having a **(MC) memory controller** **(CPL) coupled to selected inputs and outputs** of said **(D) DRAM memory**; and

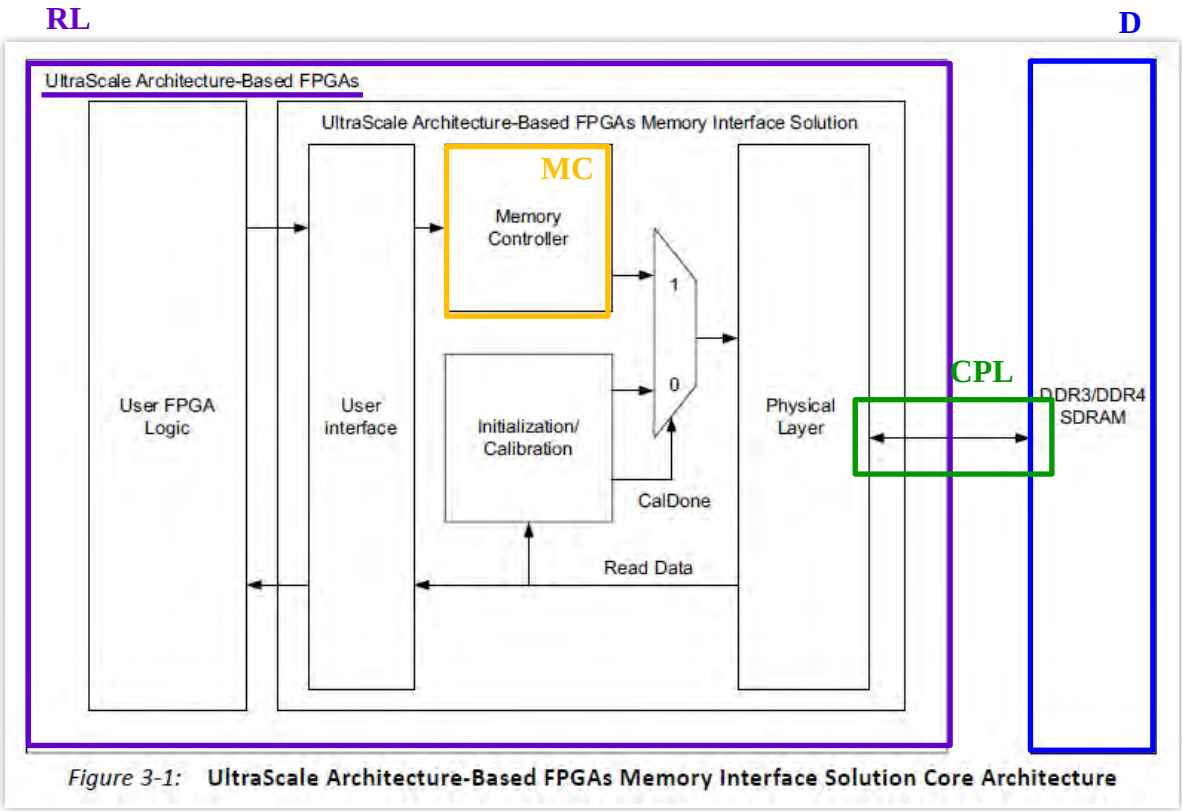
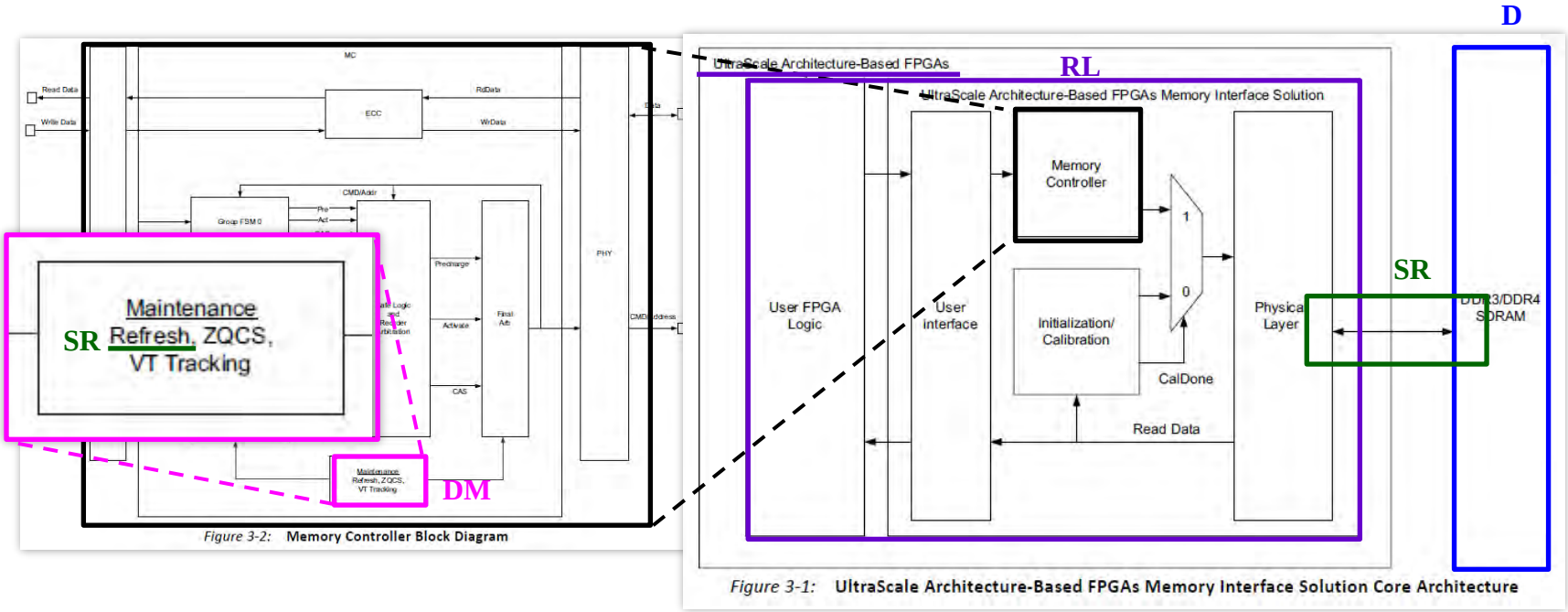


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

a **(DM) data maintenance block** coupled to said **(RL) reconfigurable logic device** and **(SR) self-refresh command inputs** of said **(D) DRAM memory**,



DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 1

said **(DM) data maintenance block** **(SIL) operative to provide stable input levels** on said **(SR) self-refresh command inputs** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands **SR**
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh **SIL**

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

SIL

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R **RL**

Partial Reconfiguration **SR**

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

Family Comparisons

Table 1: **Device Resources**

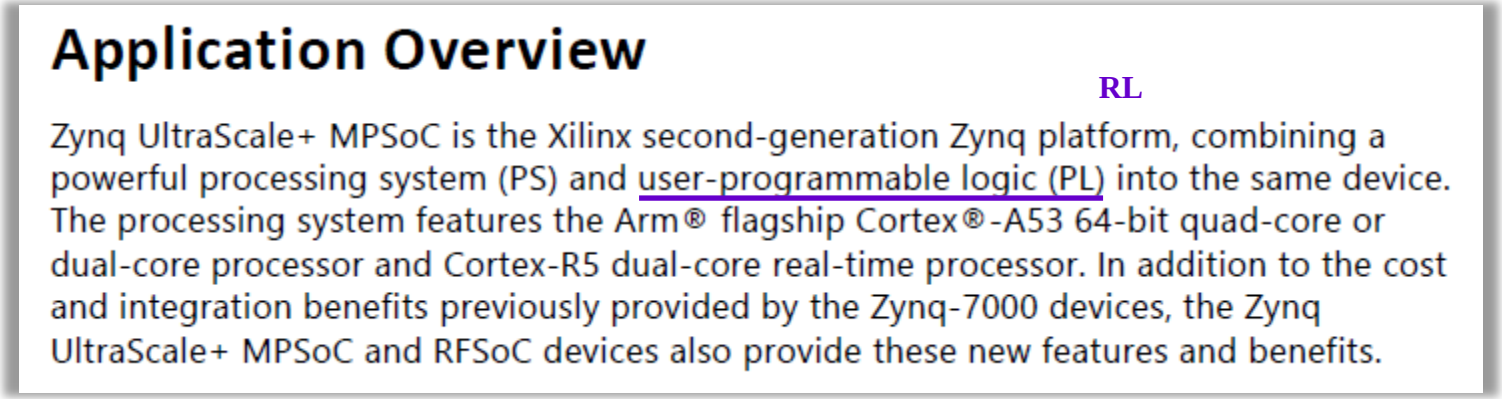
RL

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K) **FPGA**	318–1,451	356–1,143	783–5,541	862–8,938	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–16		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–2,072	82–668	280–408

Source: Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019

Claim 3

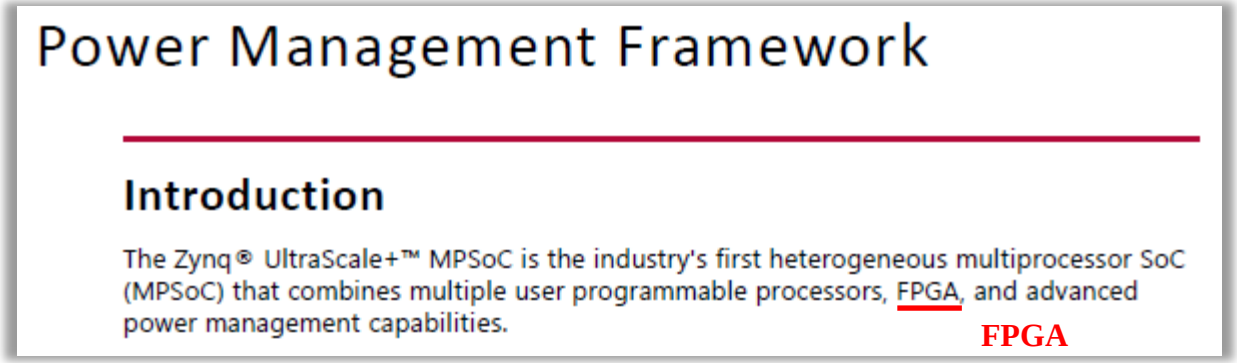
The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.



Application Overview

RL

Zynq UltraScale+ MPSoC is the Xilinx second-generation Zynq platform, combining a powerful processing system (PS) and user-programmable logic (PL) into the same device. The processing system features the Arm® flagship Cortex®-A53 64-bit quad-core or dual-core processor and Cortex-R5 dual-core real-time processor. In addition to the cost and integration benefits previously provided by the Zynq-7000 devices, the Zynq UltraScale+ MPSoC and RFSoC devices also provide these new features and benefits.



Power Management Framework

Introduction

The Zynq® UltraScale+™ MPSoC is the industry's first heterogeneous multiprocessor SoC (MPSoC) that combines multiple user programmable processors, FPGA, and advanced power management capabilities.

FPGA

Source: Xilinx UltraScale Architecture and Product Data Sheet; Overview, DS890 (v3.10), August 21, 2019
Xilinx Zynq UltraScale+ MPSoC Software Developer Guide, UG1137 (v11.0) December 5, 2019

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

RL

General Description **FPGA**

Xilinx® 7 series FPGAs comprise four FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series FPGAs include:

- Spartan®-7 Family: Optimized for low cost, lowest power, and high I/O performance. Available in low-cost, very small form-factor packaging for smallest PCB footprint.
- Artix®-7 Family: Optimized for low power applications requiring serial transceivers and high DSP and logic throughput. Provides the lowest total bill of materials cost for high-throughput, cost-sensitive applications.
- Kintex®-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex®-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Source: Xilinx 7 Series FPGAs Data Sheet: Overview, DS180 (v2.6), February 27, 2018

Claim 3

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises an **(FPGA) FPGA**.

RL

Table 1: **Zynq-7000 and Zynq-7000S SoCs *(Cont'd)***

	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent **FPGA**	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Block RAM (# 36 Kb Blocks)	1.8 Mb (50)	2.5 Mb (72)	3.8 Mb (107)	2.1 Mb (60)	3.3 Mb (95)	4.9 Mb (140)	9.3 Mb (265)	17.6 Mb (500)	19.2 Mb (545)	26.5 Mb (755)
	DSP Slices (18x25 MACCs)	66	120	170	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	73 GMACs	131 GMACs	187 GMACs	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express (Root Complex or Endpoint)[3]		Gen2 x4			Gen2 x4		Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[2]	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication									

Source: Xilinx Zinq-7000 SoC Data Sheet: Overview, DS 190 (v1.11.1) July 2 , 2018

Claim 9

The computer system of claim 1 wherein said **(RL) reconfigurable logic device** comprises said **(DM) data maintenance block**.

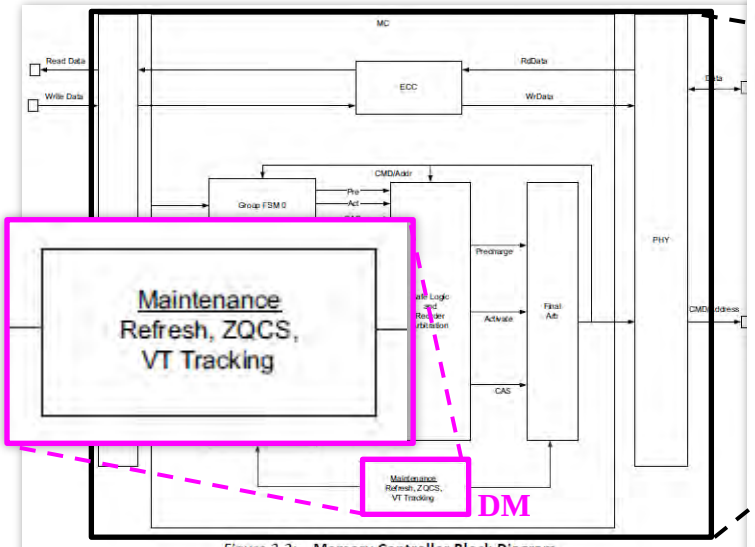


Figure 3-2: **Memory Controller Block Diagram**

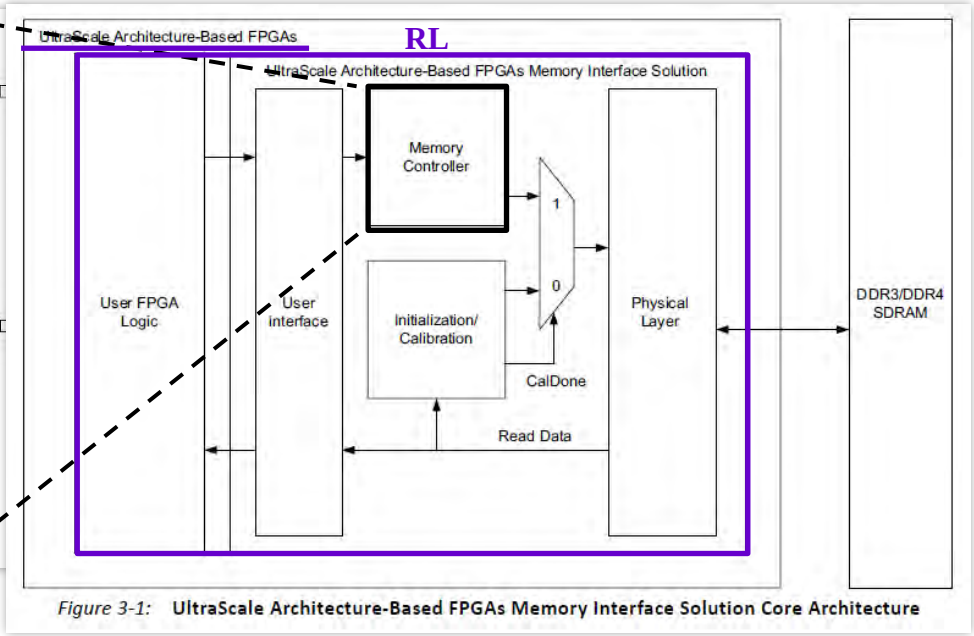


Figure 3-1: **UltraScale Architecture-Based FPGAs Memory Interface Solution Core Architecture**

Source: Xilinx UltraScale Architecture-Based FPGA's Memory IP v1.4, PG150, October 30, 2019

Claim 10

The computer system of claim 1 wherein said **(DM) data maintenance block** is **(HSR) operable to hold said DRAM memory in self-refresh mode** while said **(RL) reconfigurable logic device** is **(R) reconfigured**.

DM

The maintenance blocks of the controller command path include:

1. Blocks that generate refresh and ZQCS commands
2. Commands needed for VT tracking
3. Optional block that implements a SECDED ECC for 72-bit wide data buses

Self-Refresh HSR

Self-refresh feature is supported for Controller/PHY mode of the Controller and Physical Layer. This feature is not valid for any PHY_ONLY (Physical Layer Only and Physical Layer Ping Pong) designs.

HSR

Self-refresh feature keeps the DRAM in self-refresh mode. It also provides a set of XSDB ports at the user interface through which, you can save and restore the memory controller calibration data. This way you can drive the DRAM into self-refresh mode, save the calibration data into an external memory, and reprogram the FPGA or turn it off. It is referred as self-refresh entry cycle.

R RL

Partial Reconfiguration

The Partial Reconfiguration option can be selected from the **Disable OBUF on reset# (DDR3) or reset_n (DDR4)**option in **Advance Memory Options** section in the **Advanced Options** tab (see Figure 5-5 and Figure 5-6) when **Self Refresh** or **Save-Restore** option is enabled. When Partial Reconfiguration is enabled, the `ddr3_reset#/ddr4_reset_n` port is not included in the pin planning list and is a part of the user interface. It is your responsibility to use this port in driving the actual memory interface pin outside the DDR3/DDR4 IP design. The DDR3/DDR4 IP design is a part of the reconfigurable block, while the driver of the `ddr3_reset#/ddr4_reset_n` pin stays in the static location.

With UltraScale architecture included DDR cores feature a memory controller having a maintenance block implemented as part of the reconfigurable processor. One of the functions this maintenance block supports is “Self Refresh”. The “Self Refresh” feature keeps the DRAM in self-refresh mode; for instance during partial reconfiguration.
The driver of the *ddr3_reset#/ddr4_reset* port providing stable inputs to DRAM is part of the static region of the FPGA and not affected by the FPGA reconfiguration; it is used to hold/keep the DRAM memory in self-refresh mode.

Source: Xilinx UltraScale Architecture-Based FPGA’s Memory IP v1.4, PG150, October 30, 2019