IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	C.A. No. 6:19-cv-254 **JURY TRIAL DEMANDED**

VLSI TECHNOLOGY LLC'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff VLSI Technology LLC ("VLSI"), by and through its undersigned counsel, pleads the following against Intel Corporation ("Intel") and alleges as follows:

THE PARTIES

1. Plaintiff VLSI is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of VLSI is Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801. The name of VLSI's registered agent at that address is The Corporation Trust Company.

2. VLSI is the assignee and owns all right, title, and interest to U.S. Patent Nos. 8,156,357 ("the '357 Patent"), 7,523,373 ("the '373 Patent"), and 7,725,759 ("the '759 Patent") (collectively, the "Asserted Patents").

3. On information and belief, Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business in the Western District of Texas, including at 1300 S. Mopac Expressway, Austin, Texas 78746.[1]

JURISDICTION AND VENUE

4. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over Intel because Intel manufactures products that are and have been used, offered for sale, sold, and purchased in the Western District of Texas, and Intel has committed, and continues to commit, acts of infringement in the Western District of Texas, has conducted business in the Western District of Texas, and/or has engaged in continuous and systematic activities in the Western District of Texas.

6. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this judicial district because Intel maintains a regular and established place of business in this district and has committed acts of infringement within this judicial district giving rise to this action.

[1] https://www.intel.com/content/www/us/en/location/usa.html; https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html.

FIRST CLAIM

(Infringement of U.S. Patent No. 8,156,357)

7. VLSI re-alleges and incorporates herein by reference Paragraphs 1-6 of its Complaint.

8. The '357 Patent, entitled "Voltage-based memory size scaling in a data processing system," was duly and lawfully issued on April 10, 2012. A true and correct copy of the '357 Patent is attached hereto as Exhibit 1.

9. The '357 Patent names Shayan Zhang, James D. Burnett, Prashant U. Kenkare, Hema Ramamurthy, Andrew C. Russell, and Michael D. Snyder as co-inventors.

10. The '357 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '357 Patent, including the right to seek damages for past, current, and future infringement thereof.

11. The '357 Patent "relates generally to data processing systems, and more specifically, to voltage-based memory size scaling in a data processing system." Ex. 1 at 1:7-9.

12. The '357 Patent explains that "when a fixed Vmin [minimum supply voltage] is selected which is higher than a supply voltage level at which most memories can operate, loss of functionality and/or efficiency of a data processing system in its memory usage may occur when operating at supply voltages lower than the fixed Vmin value." *Id*. at 1:48-53.

13. The '357 Patent states that "[i]n one embodiment, the supply voltage (Vmem) for a memory is changed to different Vmin, levels where as the Vmin levels decreases, increasingly larger sections of the memory become non-functional…. Therefore, at lower voltage levels for Vmem [supply voltage for a memory], the size of the memory may be scaled down such that the memory can still operate, but with a smaller number of functional bits." *Id*. at 1:53-56, 64-66.

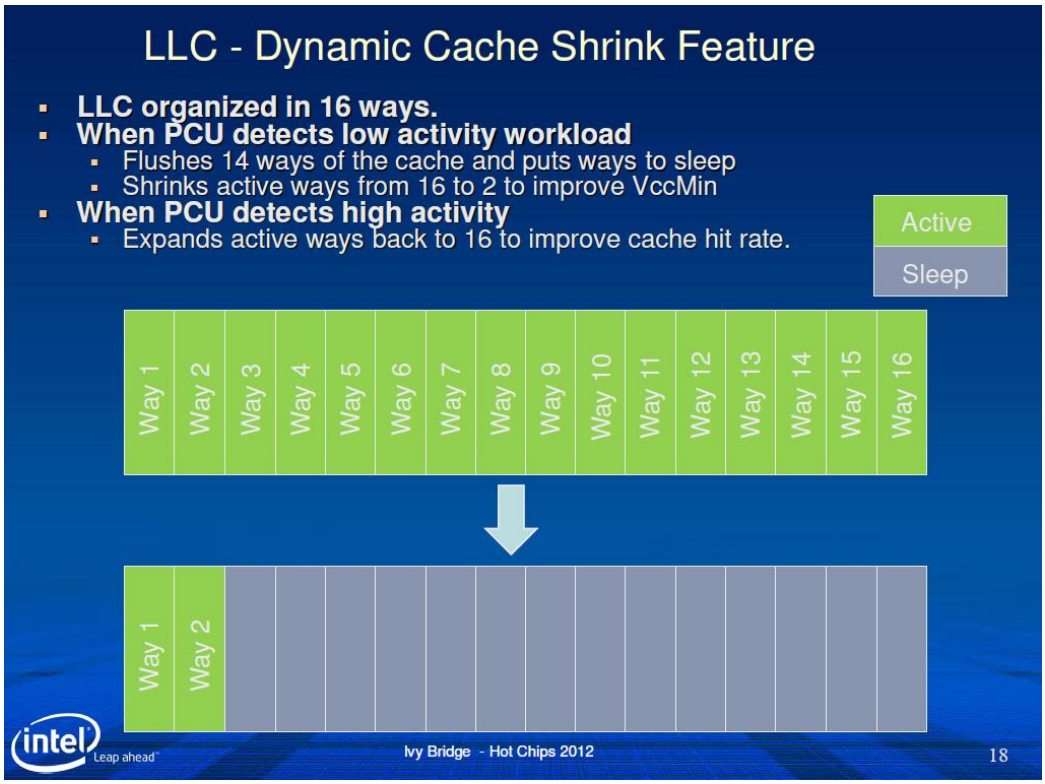
14. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the ’357 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that use dynamic cache shrink technology in an infringing manner.

15. For example, the ’357 accused products embody every limitation of at least claim 1 of the ’357 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

[“1. A method of using a cache having a plurality of ways, comprising:”]

16. Intel Ivy Bridge processors operate using a method of using cache having a plurality of ways.

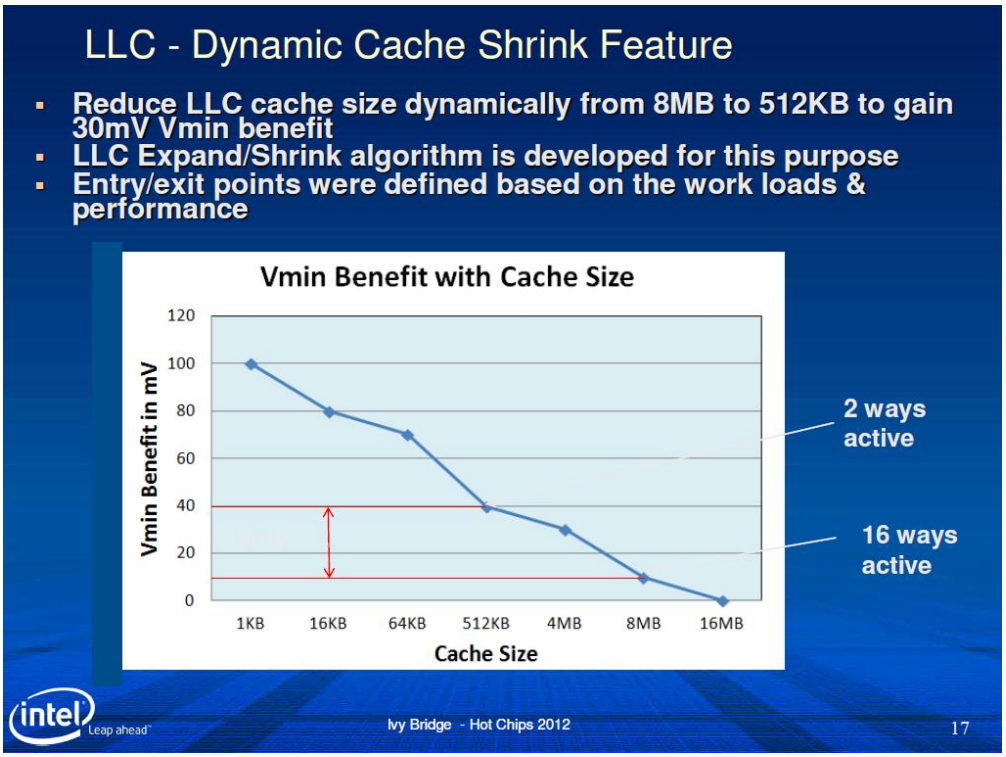
17. For example, Intel Ivy Bridge processors include a cache organized in 16 ways. *See*, *e.g.*, Power Management of the Third Generation Core Micro Architecture formerly codenamed Ivy Bridge [hereinafter "PM"] at 18:



["accessing the cache with a power supply voltage applied to the cache at a first value; reducing the power supply voltage to a second value;"]

18. Intel Ivy Bridge processors operate using a method comprising accessing the cache with a power supply voltage applied to the cache at a first value and reducing the power supply voltage to a second value.

19. For example, the Intel Ivy Bridge processor cache has a nominal operating voltage. Using the Dynamic Cache Shrink Feature, it is capable of reducing the power supply to the cache by 30 mV to a second, reduced voltage. *See, e.g.*, PM at 16:

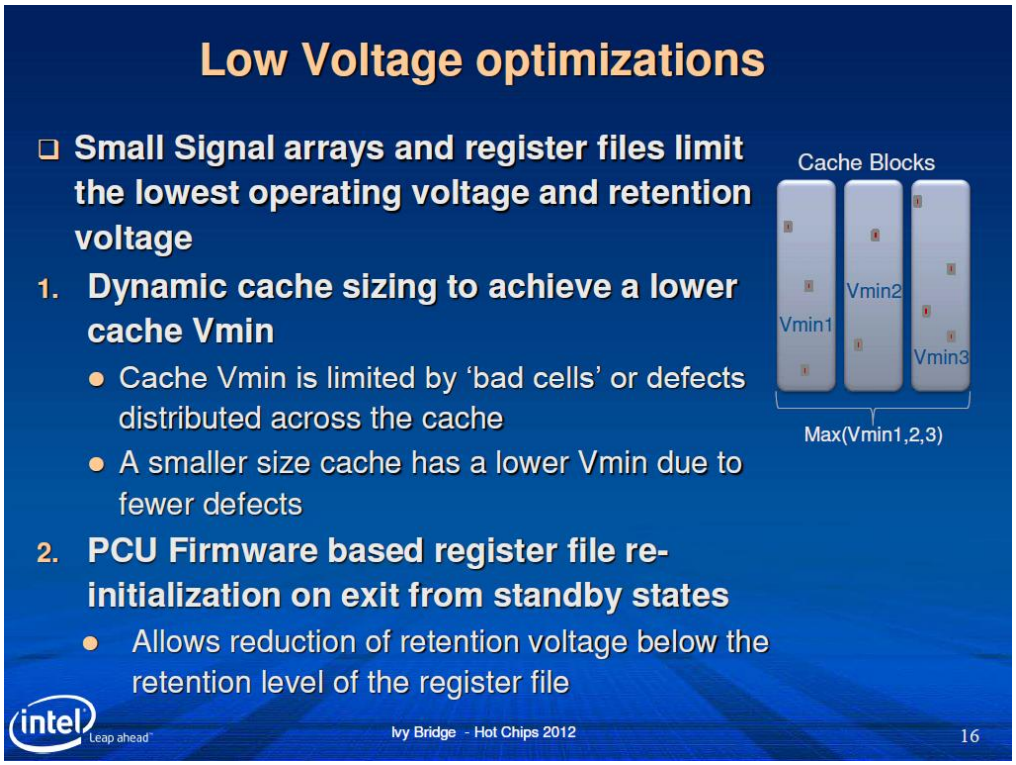


["identifying a first set of ways of the plurality of ways as being non-functional, wherein the being non-functional is caused by the power supply voltage being at the second value, wherein the first set of ways is less than all ways of the cache, and the step of identifying the first set of ways comprises: retrieving information that correlates non-functional ways of the cache with values of the power supply voltage;"]

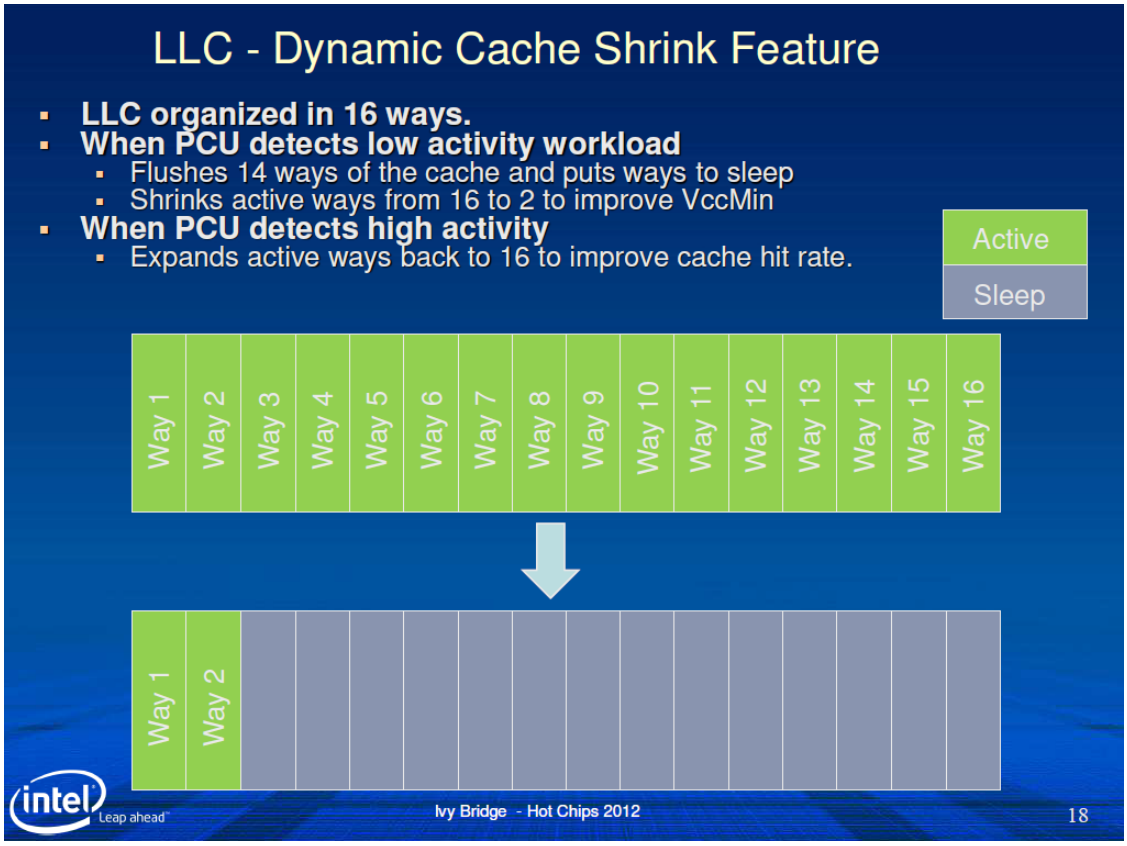
20. The Intel Ivy Bridge processors operate using a method comprising identifying a first set of ways of the plurality of ways as being non-functional, wherein the being non-functional is caused by the power supply voltage being at the second value, wherein the first set of ways is less than all ways of the cache and the step of identifying the first set of ways comprises retrieving

information that correlates non-functional ways of the cache with values of the power supply voltage.

21. For example, the Intel Ivy Bridge processor identifies a set of ways that include "defects" that are randomly distributed throughout the cache. These ways are identified as being non-functional at the reduced voltage. *See, e.g.*, PM at 16:



22. The PCU flushes and puts to sleep a subset of the ways, shown here as ways 3-16, that would be non-functional at the lower voltage. *See, e.g.*, PM at 16:

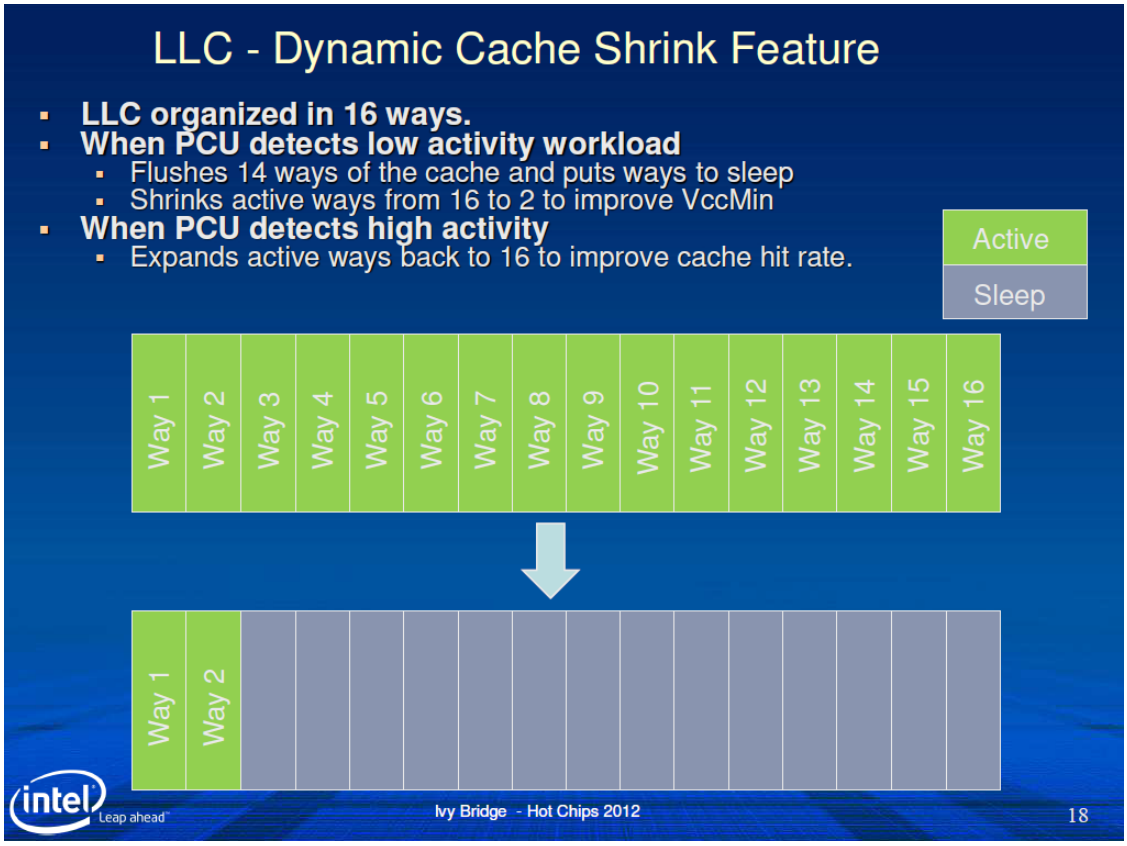


["accessing the cache exclusive of the first set of ways, wherein the step of accessing the cache exclusive of the first set of ways is performed with the power supply voltage at the second value;"]

23. Intel Ivy Bridge processors operate using a method of using cache having a plurality of ways.

24. Intel Ivy Bridge processors are operated using a method comprising accessing the cache exclusive of the first set of ways, wherein the step of accessing the cache exclusive of the first set of ways is performed with the power supply voltage at the second value.

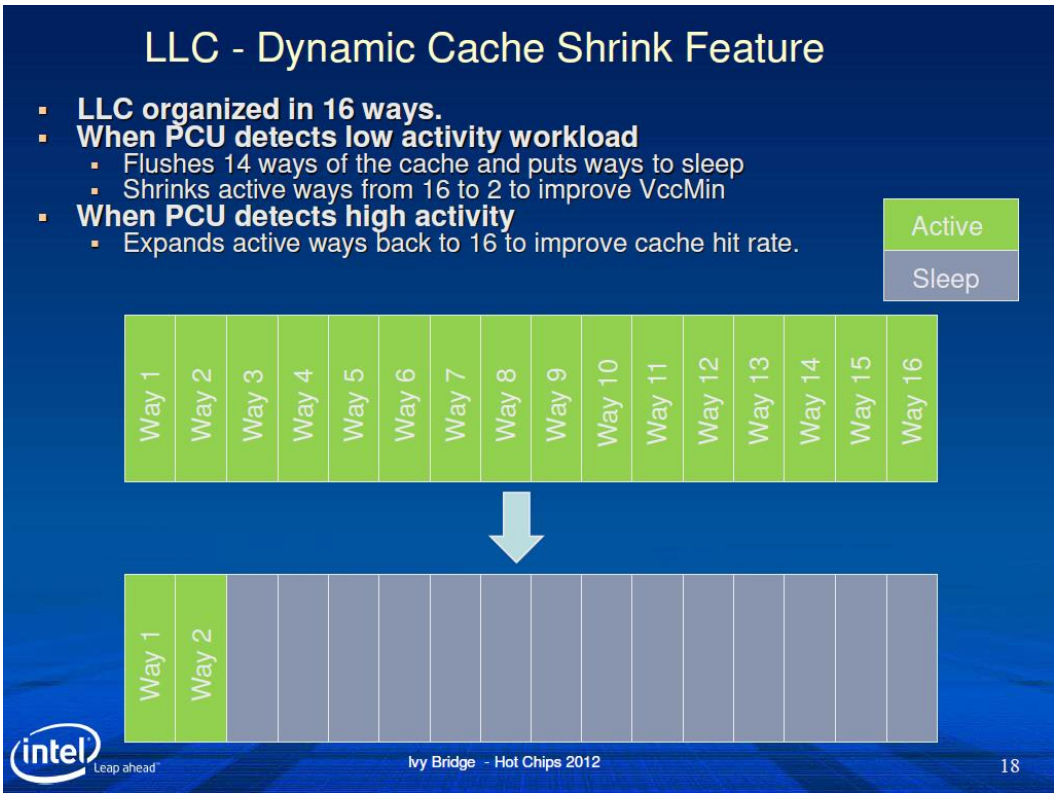
25. For example, the ways of the cache that were put to sleep are not accessed during this mode. *See, e.g.*, PM at 16:



["increasing the power supply voltage to a third value; identifying a second set of ways of the first set of ways that is functional with the power supply being applied at the third value; and accessing the cache including the second set of ways."]

26. Intel Ivy Bridge processors operate using a method comprising increasing the power supply voltage to a third value, identifying a second set of ways of the first set of ways that is functional with the power supply being applied at the third value, and accessing the cache including the second set of ways.

27. For example, when the PCU detects high activity, it returns to normal operation by expanding back to the full set of 16 ways, all of which are functional at the nominal (non-reduced) operating voltage of the cache. *See, e.g.*, PM at 18:



28. Intel has had knowledge of the '357 Patent and its infringement of the '357 Patent at least since the filing of this Complaint, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the '357 Patent and its infringement of the '357 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals. For example, in *Intel Corp. v. Future Link Sys*., LLC, 268 F. Supp. 3d 605, 623 (D. Del. 2017) the court noted the patent owner's observation that "Intel's own engineers concede that they avoid reviewing other, non-Intel patents so as to avoid willfully infringing them." As a further example, former Intel employees, including Intel's long-time Chief Architect Robert Colwell, have admitted that this policy's purpose is to "avoid possible

triple damages for 'willful infringement.'" As still another example, Intel has been sued for infringing patents previously assigned to NXP, while this policy was in place, including for infringing a patent naming all four of David Burnett,[2] Prashant Kenkare, Andrew Russell, and Michael Snyder (each of whom is also an inventor on the '357 Patent) as an inventor. Yet despite this notice, Intel proceeded to infringe other patents on inventions developed in the same area by these four named inventors.[3] Under the circumstances present here, including explicit notice having been provided of Intel's infringement of other NXP patents and NXP's competitive position with Intel in the marketplace, Intel knew or should have known of the high probability that NXP had patented other technologies, such as those to which the '357 Patent is directed, that Intel had included within its microprocessor products. Intel should have known that its conduct was infringing both prior to and following the filing of this Complaint.

29. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '357 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '357 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly

[2] The inventor's full name is James David Burnett. He is listed as James D. Burnett on the '357 patent.

[3] Intel was also sued for infringing an additional patent naming James D. Burnett as an inventor.

infringe the ’357 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

30. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the ’357 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the ’357 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the ’357 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the ’357 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel’s customers directly infringe the ’357 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

31. As a result of Intel’s infringement of the ’357 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel’s wrongful acts in an amount subject to proof at trial.

32. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the ’357 Patent.

33. In addition, Intel’s infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

34. VLSI is informed and believes, and thereon alleges, that Intel's infringement of the '357 Patent has been and continues to be willful. As noted above, Intel has had knowledge of the '357 Patent and its infringement of the '357 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

35. Based on the information alleged in this claim, as well as the information alleged in the Second and Third Claims *infra*, VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

SECOND CLAIM

(Infringement of U.S. Patent No. 7,523,373)

36. VLSI re-alleges and incorporates herein by reference Paragraphs 1-35 of its Complaint.

37. The '373 Patent, entitled "Minimum memory operating voltage technique," was duly and lawfully issued on April 21, 2009. A true and correct copy of the '373 Patent is attached hereto as Exhibit 2.

38. The '373 Patent names Andrew C. Russell, David R. Bearden, Bradford L. Hunter, and Shayan Zhang as co-inventors.

39. The '373 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '373 Patent, including the right to seek damages for past, current, and future infringement thereof.

40. The '373 Patent relates "generally to memories, and more specifically, to a minimum memory operating voltage technique." Ex. 2 at 1:6-8.

41. The ’373 Patent states that “the memory in a data processing system may fail at a higher voltage than the processor.” *Id*. at 2:4-5. “Furthermore, this minimum operating voltage for a memory varies across parts, such that one integrated circuit (IC) may tolerate one minimum operating voltage while another IC may be able to tolerate even a lower operating voltage[.]” *Id*. at 2:17-21.

42. The ’373 Patent explains that “[t]he value of the minimum operating voltage is stored in a non-volatile memory location that may be a non-volatile register. This minimum operating voltage information can then be used in determining when an alternative power supply voltage may be switched to the memory or ensuring that the minimum voltage is otherwise met.” *Id*. at Abstract.

43. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the ’373 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the United States, without authority or license, Intel products that use fuses or other non-volatile memory to store information about SRAM minimum voltages in an infringing manner.

44. For example, the ’373 accused products embody every limitation of at least claim 16 of the ’373 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

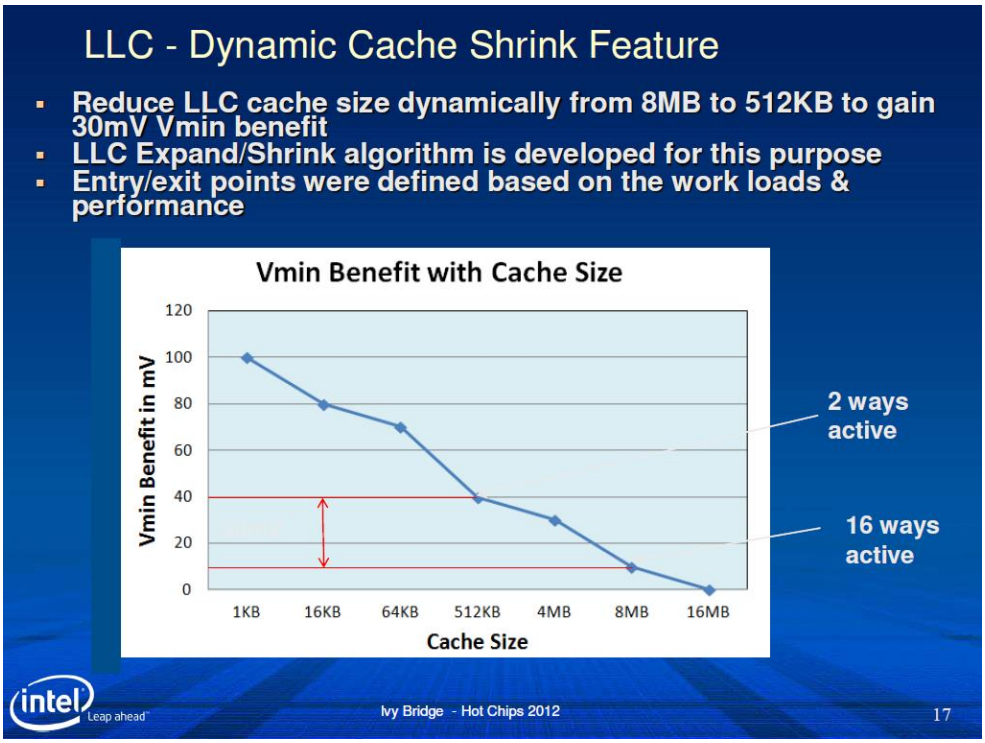
[“16. A method comprising:”]

45. Intel Ivy Bridge processors operate using a method comprising the elements described below.

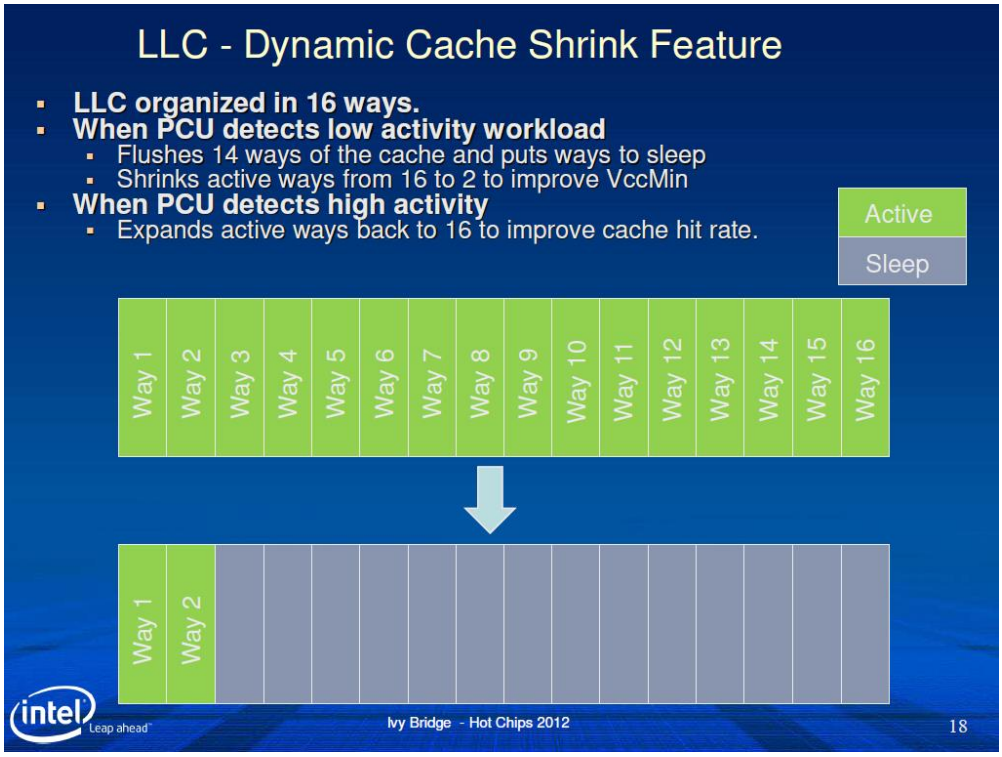
["providing an integrated circuit with a memory that uses an operating voltage; testing the memory to determine the operating voltage of the memory that is a minimum operating voltage; storing, in a non-volatile manner, the value of the minimum operating voltage;"]

46. Intel Ivy Bridge processors operate using a method comprising providing an integrated circuit with a memory that uses an operating voltage, testing the memory to determine the operating voltage of the memory that is a minimum operating voltage, storing, in a non-volatile manner, the value of the minimum operating voltage.

47. For example, Intel Ivy Bridge processors store the minimum operating voltage for different size configurations of the last level cache memory array in a non-volatile manner, accessible after reboots. *See, e.g.*, Power Management of the Third Generation Core Micro Architecture formerly codenamed Ivy Bridge [hereinafter "PM"] at 17:



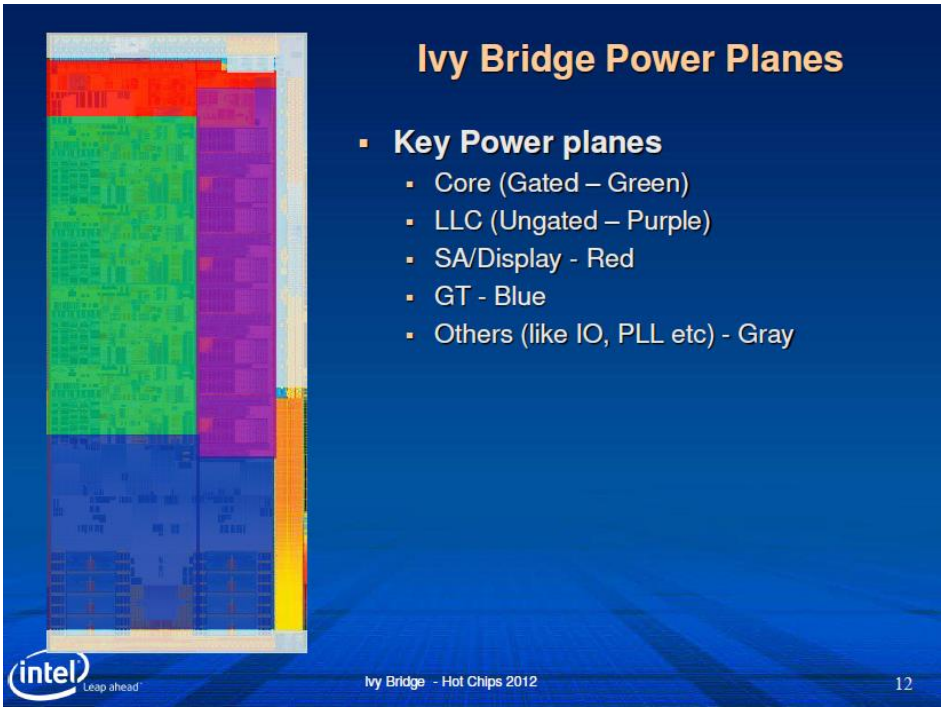
48. *See* also, *e.g.*, *id.* at 18:



[“providing a functional circuit on the integrated circuit exclusive of the memory;”]

49. The Intel Ivy Bridge processors operate using a method comprising providing a functional circuit on the integrated circuit exclusive of the memory.

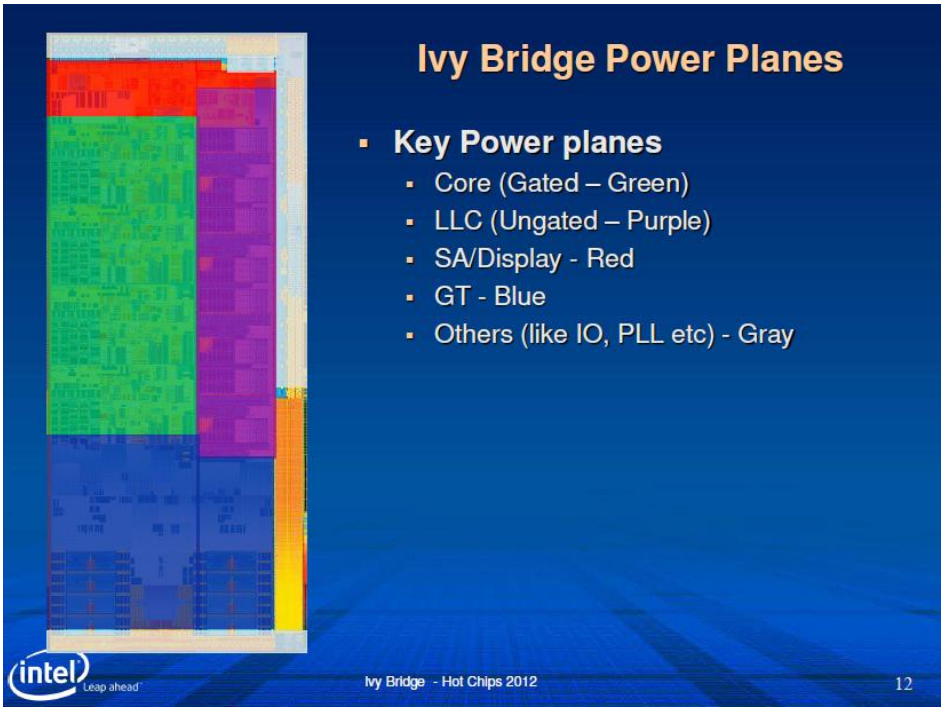
50. For example, the Intel Ivy Bridge processor includes cores (shown below in green), exclusive of the last level cache (LLC) memory (shown below in purple). *See, e.g.*, PM at 12:



[“providing a first regulated voltage to the functional circuit;”]

51. The Intel Ivy Bridge processors operate using a method comprising providing a first regulated voltage to the functional circuit.

52. For example, the core is powered via a power gate, which regulates the voltage (first voltage) at the cores. *See, e.g.*, PM at 12:

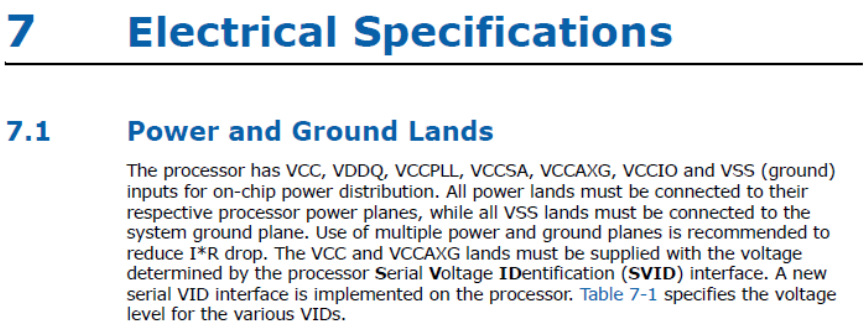


[“providing a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage;”]

53. Intel Ivy Bridge processors operate using a method comprising providing a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage.

54. For example, the processor itself is powered via a “core power rail,” VCC, a second voltage, regulated by the off-chip voltage regulator as specified by the processor “Serial Voltage

Identification" (SVID) interface. *See, e.g.*, Desktop 3rd Generation Intel Core Processor Family Datasheet [hereinafter "Datasheet"] at 75:



7 Electrical Specifications

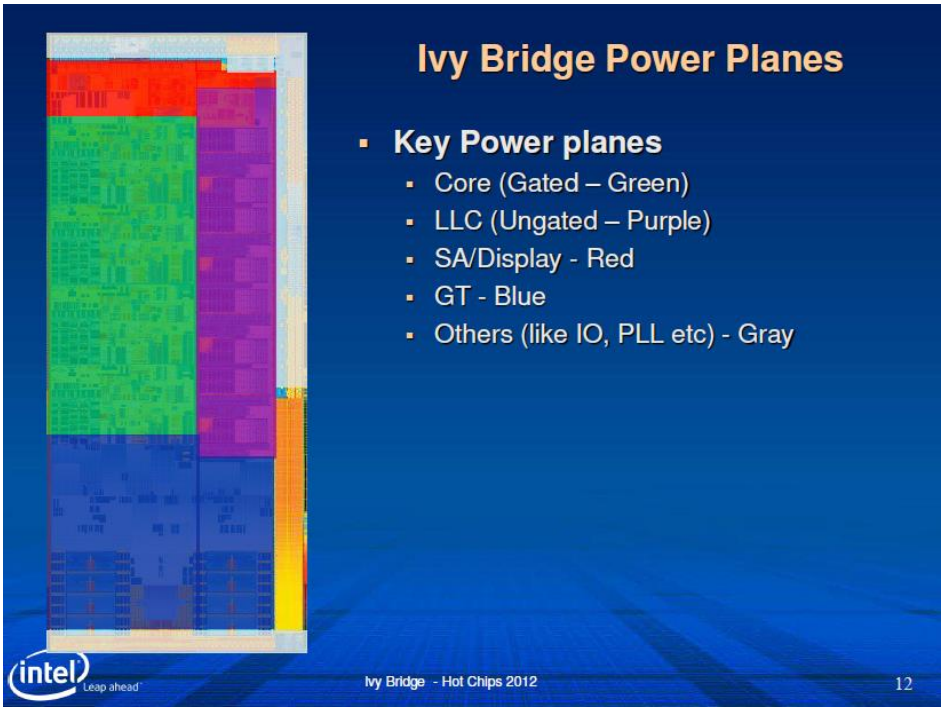
7.1 Power and Ground Lands

The processor has VCC, VDDQ, VCCPLL, VCCSA, VCCAXG, VCCIO and VSS (ground) inputs for on-chip power distribution. All power lands must be connected to their respective processor power planes, while all VSS lands must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The VCC and VCCAXG lands must be supplied with the voltage determined by the processor **S**erial **V**oltage **ID**entification (**SVID**) interface. A new serial VID interface is implemented on the processor. Table 7-1 specifies the voltage level for the various VIDs.

["providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and"]

55. Intel Ivy Bridge processors operate using a method comprising providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage.

56. For example, the voltage provided to the LLC memory is "ungated," meaning that the memory array is always provided with VCC, the second voltage. *See, e.g.*, PM at 12:



57. The on-chip power gates can only reduce the core (first) voltage from the supplied VCC power rail. When the core voltage (the first voltage) is above the operating voltage of the memory, the power gate will be fully opened, and the first voltage (core voltage) and the second voltage (VCC) will be the same. Thus, when the first voltage is above the minimum operating voltage of the memory, the first voltage will be provided to the memory array.

["providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit."]

58. Intel Ivy Bridge processors operate using a method comprising providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.

59. For example, when the core voltage (the first voltage) is below the operating voltage of the memory, the power gate will be partially or fully closed, and the first voltage will be below the second voltage (VCC). Thus, when the first voltage is below the minimum operating voltage of the memory, the second voltage will be provided to the memory array.

60. Intel has had knowledge of the ’373 Patent and its infringement of the ’373 Patent at least since the filing of this Complaint, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the ’373 Patent and its infringement of the ’373 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals, as already described above. As still another example, Intel has been sued for infringing patents previously assigned to NXP, while this policy was in place, including for infringing a patent naming all three of Bradford Hunter, Andrew Russell, and Shayan Zhang (each of whom is also an inventor on the ’373 Patent) as an inventor. Yet despite this notice, Intel proceeded to infringe other patents on inventions developed in the same area by these named inventors.[4] Under the circumstances present here, including explicit notice having been provided of Intel’s infringement of other NXP patents and NXP’s competitive position with Intel in the marketplace, Intel knew or should have known of the high probability

[4] Intel was also sued for infringing an additional patent naming David R. Bearden (also an inventor on the ’373 Patent) as an inventor.

that NXP had patented other technologies, such as those to which the '373 Patent is directed, that Intel had included within its microprocessor products. Intel should have known that its conduct was infringing both prior to and following the filing of this Complaint.

61. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '373 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '373 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly infringe the '373 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

62. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the '373 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the '373 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the '373 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the '373 Patent and are not staple articles or commodities of commerce suitable for

substantial noninfringing use. On information and belief, Intel's customers directly infringe the '373 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

63. As a result of Intel's infringement of the '373 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

64. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the '373 Patent.

65. In addition, Intel's infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

66. VLSI is informed and believes, and thereon alleges, that Intel's infringement of the '373 Patent has been and continues to be willful. As noted above, Intel has had knowledge of the '373 Patent and its infringement of the '373 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

67. Based on the information alleged in this claim, as well as the information alleged in the First Claim *supra* and the Third Claim *infra*, VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

THIRD CLAIM

(Infringement of U.S. Patent No. 7,725,759)

68. VLSI re-alleges and incorporates herein by reference Paragraphs 1-67 of its Complaint.

69. The '759 Patent, entitled "System and method of managing clock speed in an electronic device," was duly and lawfully issued on May 25, 2010. A true and correct copy of the '759 Patent is attached hereto as Exhibit 3.

70. The '759 Patent names Matthew Henson as inventor.

71. The '759 Patent has been in full force and effect since its issuance. VLSI owns by assignment the entire right, title, and interest in and to the '759 Patent, including the right to seek damages for past, current, and future infringement thereof.

72. The '759 Patent states that it "relates to electronic devices and to managing clock speeds within electronic devices." Ex. 3 at 1:6-7.

73. The '759 Patent explains, for instance, "there is a need for an improved system and method of controlling a clock frequency in an electronic device in order to selectively deliver faster clock speeds." *Id*. at 1:22-24.

74. The '759 Patent discloses, among other things, "[a] method of controlling a clock frequency . . . [that] includes monitoring a plurality of master devices that are coupled to a bus within a system." *Id*. at 1:46-48.

75. VLSI is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the '759 Patent, in violation of 35 U.S.C. § 271, by, among other things, making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and importing into the

United States, without authority or license, Intel products that use infringing Hardware-Controlled Performance States ("HWP" or "Speed Shift") technology.

76. For example, the '759 accused products embody every limitation of at least claim 1 of the '759 Patent, literally or under the doctrine of equivalents, as set forth below. The further descriptions below, which are based on publicly available information, are preliminary examples and are non-limiting.

["1. A method comprising:"]

77. Intel Skylake processors, which include Hardware-Controlled Performance States (HWP or "Speed Shift"), are operated using a method comprising the elements listed below. *See, e.g.*, https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/6th-gen-core-family-mobile-brief.pdf at 8:

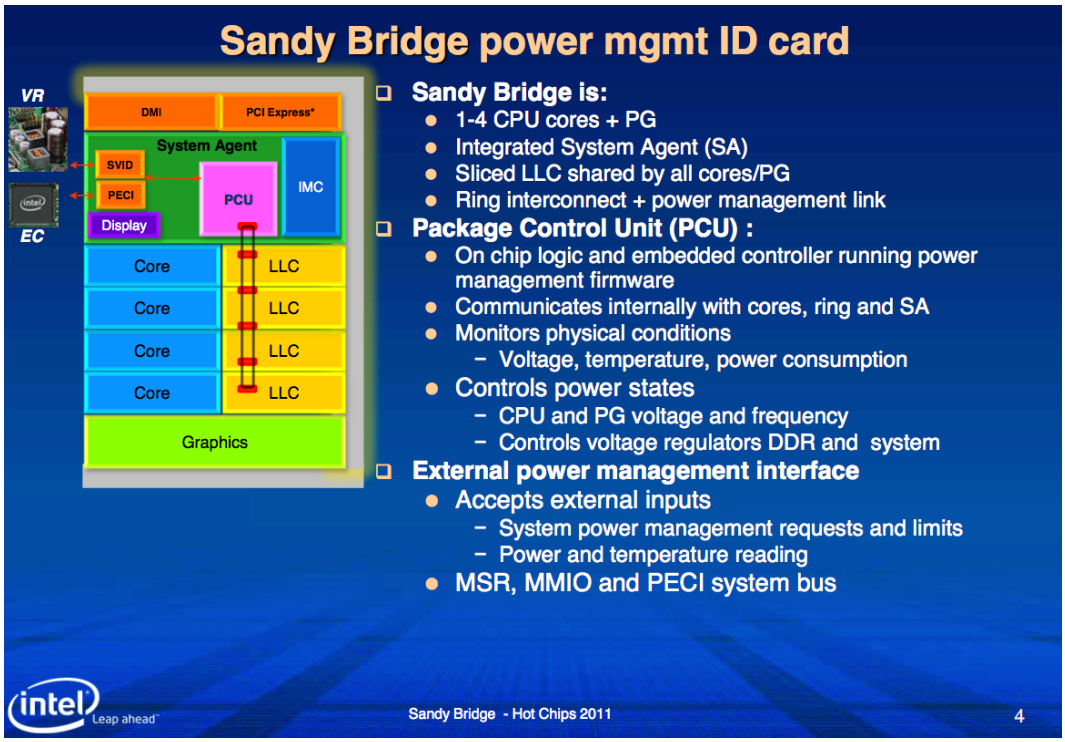
6TH GEN INTEL® CORE PROCESSOR™ FEATURES AT A GLANCE

FEATURES[1]	BENEFITS
Intel® Active Management Technology (Intel® AMT)[15]	Using built-in platform capabilities and popular third-party management and security applications, Intel AMT allows IT to discover, heal, and protect computing assets on wired and wireless networks. Intel AMT is supported on platforms that have Intel® vPro™.
Intel® Rapid Storage Technology (Intel® RST)[17]	Offers excellent levels of performance, responsiveness, and expandability. Take advantage of the enhanced performance and lower power consumption available with Intel® RST with one or more SATA or PCIe storage drives. With additional SATA drives, Intel® RST provides quicker access to digital photo, video, and data files with RAID 0, 5, and 10, and greater data protection against a storage disk drive failure with RAID 1, 5, and 10. Dynamic Storage Accelerator unleashes the maximum performance of Solid State Drives (SSD) when multitasking.[17]
Intel® Speed Shift Technology	Delivers dramatically quicker responsiveness with single-threaded, transient (short duration) workloads, such as web browsing, by allowing the processor to more quickly select its best operating frequency and voltage for optimal performance and power efficiency.

["monitoring a plurality of master devices coupled to a bus;"]

78. Intel Skylake processors are operated using a method that comprises monitoring a plurality of master devices coupled to a bus.

79. For example, Intel Skylake processors include a "Package Control Unit" that monitors the operations of a plurality of cores. These cores are connected by a "ring interconnect" bus. *See, e.g.*, "Power management architecture of the 2nd generation Intel Core microarchitecture, formally codenamed Sandy Bridge" [hereinafter "PCU"] at 4:



80. On information and belief, these and the other pertinent portions of the Sandy Bridge family of processors were carried over to Skylake processors in a manner that is materially the same with respect to the infringement analysis presented in this example.

["receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device,"]

81. Intel Skylake processors are operated using a method that comprises receiving a request, from a first master device of the plurality of master devices, to change a clock frequency

of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device.

82. For example, each core monitors its own "applied workload" for a change in performance in that device. If a first core detects a predefined change in performance, it will request that the system change P-state, which corresponds to the high-speed frequency of operation of the cores on the device. This detection is signaled as a request to the PCU, which is responsible for setting frequencies on the microprocessor. *See*, *e.g.*, Intel Software Developer's Manual [hereinafter "SDM"] at 3158-3159:

14.4 HARDWARE-CONTROLLED PERFORMANCE STATES (HWP)

Intel processors may contain support for Hardware-Controlled Performance States (HWP), which autonomously selects performance states while utilizing OS supplied performance guidance hints. The Enhanced Intel Speed-Step® Technology provides a means for the OS to control and monitor discrete frequency-based operating points via the IA32_PERF_CTL and IA32_PERF_STATUS MSRs.

In contrast, HWP is an implementation of the ACPI-defined Collaborative Processor Performance Control (CPPC), which specifies that the platform enumerates a continuous, abstract unit-less, performance value scale that is not tied to a specific performance state / frequency by definition. While the enumerated scale is roughly linear in terms of a delivered integer workload performance result, the OS is required to characterize the performance value range to comprehend the delivered performance for an applied workload.

When HWP is enabled, the processor autonomously selects performance states as deemed appropriate for the applied workload and with consideration of constraining hints that are programmed by the OS. These OS-provided hints include minimum and maximum performance limits, preference towards energy efficiency or performance, and the specification of a relevant workload history observation time window. The means for the OS to override HWP's autonomous selection of performance state with a specific desired performance target is also provided, however, the effective frequency delivered is subject to the result of energy efficiency and performance optimizations.

["wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and"]

83. Intel Skylake processors are operated using a method wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval.

84. For example, the change in performance measured is due to the loading of the processor in a predefined time interval, the "moving workload history observation window." This

window can either be specified by an operating system or determined by the processor. *See, e.g.*, SDM at 3161-3162:

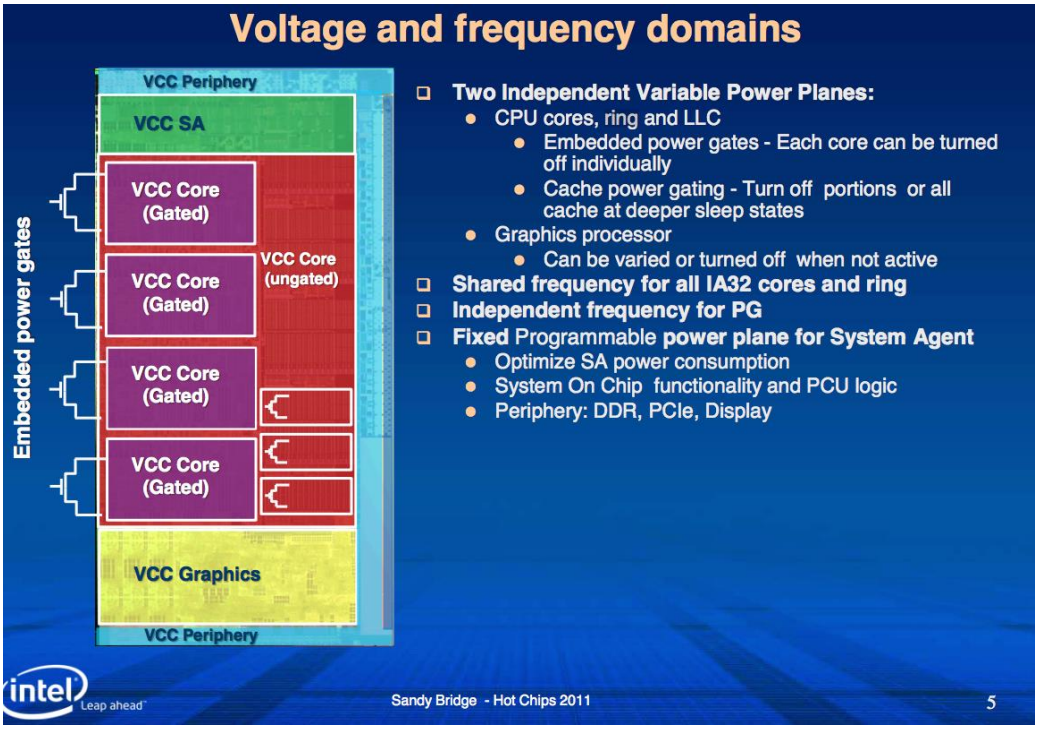
> **Activity_Window (bits 41:32, RW)** — Conveys a hint to the HWP hardware specifying a moving workload history observation window for performance/frequency optimizations. If 0, the hardware will determine the appropriate window size. When writing a non-zero value to this field, this field is encoded in the format of bits 38:32 as a 7-bit mantissa and bits 41:39 as a 3-bit exponent value in powers of 10. The resultant value is in microseconds. Thus, the minimal/maximum activity window size is 1 microsecond/1270 seconds. Combined with the Energy_Performance_Preference input, Activity_Window influences the rate of performance increase
>
> / decrease. This non-zero hint only has meaning when Desired_Performance = 0. The default value of this field is 0.

["in response to receiving the request from the first master device: providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and"]

85. Intel Skylake processors are operated using a method that comprises, in response to receiving the request from the first master device, providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus.

86. For example, when the PCU receives the request from the first core to change the clock frequency, the same frequency is also supplied to each other core in the platform, at least

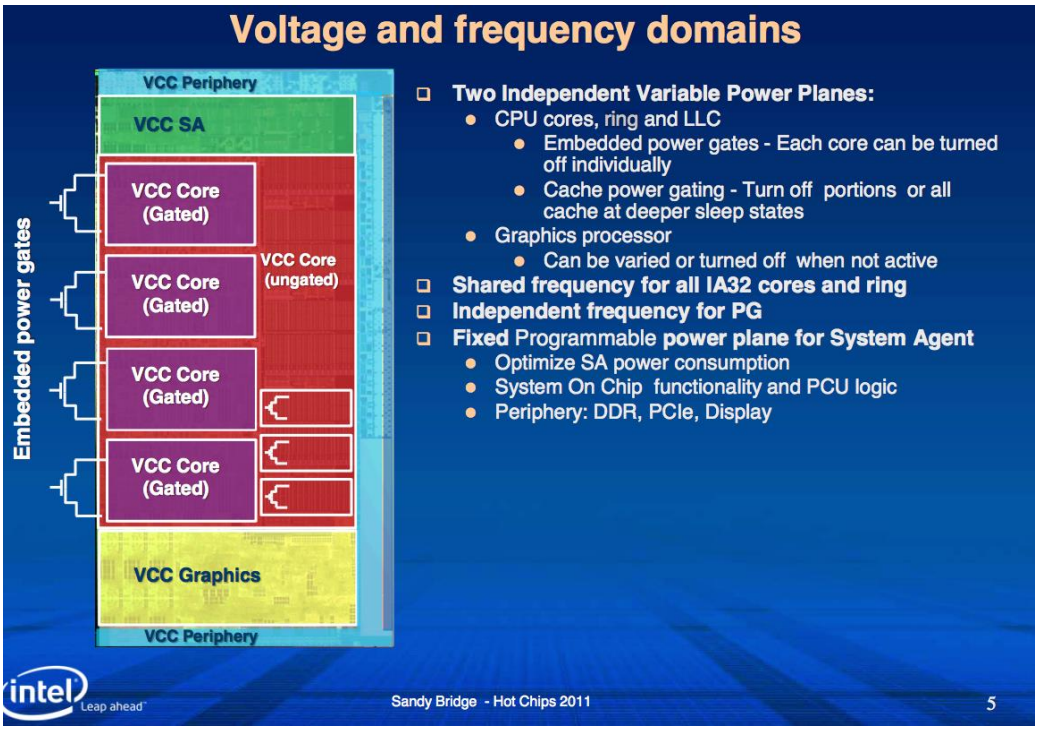
one of which is a second master device coupled to the ring interconnect bus. Each core shares a common frequency. *See, e.g.*, PCU at 5:



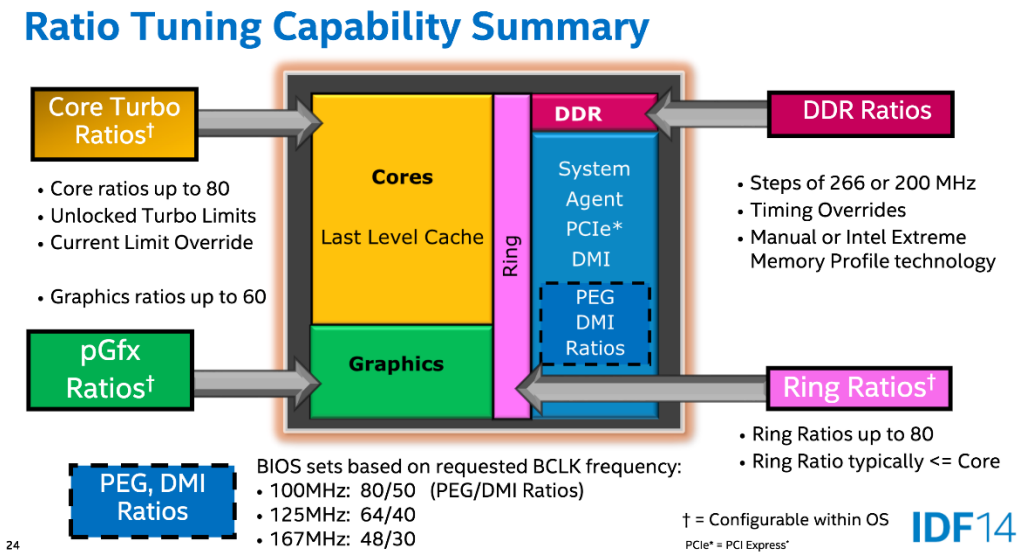
["providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus."]

87. Intel Skylake processors are operated using a method that comprises providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

88. For example, when the PCU receives the request from the first core to change the clock frequency, the same frequency is also supplied to the ring interconnect itself, which shares a clock frequency with the cores. *See, e.g.*, PCU at 5:



89. *See also, e.g.*, http://docplayer.net/38640265-Overclocking-intel-core-processors-taking-overclocking-to-the-next-level.html at 24:



90. Intel has had knowledge of the '759 Patent and its infringement of the '759 Patent at least since the filing of the complaint in *VLSI Technology LLC v. Intel Corp.*, Civil Action No. 19-00426 (D. Del.) (filed Mar. 1, 2019) (the "Delaware Complaint") which asserted infringement by Intel of the '759 Patent, and if it did not have actual knowledge prior to that time, it was willfully blind to the existence of the '759 Patent and its infringement of the '759 Patent based on, for example, its publicly-known corporate policy forbidding its employees from reading patents held by outside companies or individuals, as already described above. As still another example, on information and belief, Intel has been sued for infringing patents previously assigned to NXP while this policy was in place. Under the circumstances present here, including explicit notice having been provided of Intel's infringement of other NXP patents and NXP's competitive position with Intel in the marketplace, Intel knew or should have known of the high probability that NXP had patented other technologies, such as those to which the '759 Patent is directed, that Intel had included within its microprocessor products. Intel should have known that its conduct was infringing both prior to and following the filing of the Delaware Complaint.

91. VLSI is informed and believes, and thereon alleges, that Intel actively, knowingly, and intentionally has induced infringement of the '759 Patent by, for example, controlling the design and manufacture of, offering for sale, selling, supplying, and otherwise providing instruction and guidance regarding the above-described products with the knowledge and specific intent to encourage and facilitate infringing uses of such products by its customers both inside and outside the United States. For example, Intel publicly provides documentation, including datasheets available through Intel's publicly accessible ARK service and software developer's manuals, instructing customers on uses of Intel's products that infringe the methods of the '759 Patent. *See, e.g.*, http://ark.intel.com. On information and belief, Intel's customers directly

infringe the ’759 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

92. VLSI is informed and believes, and thereon alleges, that Intel has contributed to the infringement by its customers of the ’759 Patent by, without authority, importing, selling and offering to sell within the United States materials and apparatuses for practicing the claimed invention of the ’759 Patent both inside and outside the United States. For example, the above-described products constitute a material part of the inventions of the ’759 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel knows that the above-described products constitute a material part of the inventions of the ’759 Patent and are not staple articles or commodities of commerce suitable for substantial noninfringing use. On information and belief, Intel’s customers directly infringe the ’759 Patent by, for example, making, using, offering to sell, and selling within the United States, and importing into the United States, without authority or license, products containing the above-described Intel products.

93. As a result of Intel’s infringement of the ’759 Patent, VLSI has been damaged. VLSI is entitled to recover for damages sustained as a result of Intel’s wrongful acts in an amount subject to proof at trial.

94. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the ’759 Patent.

95. In addition, Intel’s infringing acts and practices have caused and are causing immediate and irreparable harm to VLSI.

96. VLSI is informed and believes, and thereon alleges, that Intel's infringement of the '759 Patent has been and continues to be willful. As noted above, Intel has had knowledge of the '759 Patent and its infringement of the '759 Patent. Intel has deliberately continued to infringe in a wanton, malicious, and egregious manner, with reckless disregard for VLSI's patent rights. Thus, Intel's infringing actions have been and continue to be consciously wrongful.

97. Based on the information alleged in this claim, as well as the information alleged in the First and Second Claims, *supra*, VLSI is informed and believes, and thereon alleges, that this is an exceptional case, which warrants an award of attorney's fees to VLSI pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, VLSI prays for judgment against Intel as follows:

A. That Intel has infringed, and unless enjoined will continue to infringe, each of the Asserted Patents;

B. That Intel has willfully infringed each of the Asserted Patents;

C. That Intel pay VLSI damages adequate to compensate VLSI for Intel's infringement of each of the Asserted Patents, together with interest and costs under 35 U.S.C. § 284;

D. That Intel be ordered to pay prejudgment and post-judgment interest on the damages assessed;

E. That Intel pay VLSI enhanced damages pursuant to 35 U.S.C. § 284;

F. That Intel be ordered to pay supplemental damages to VLSI, including interest, with an accounting, as needed;

G. That Intel be enjoined from infringing the Asserted Patents, or if its infringement is not enjoined, that Intel be ordered to pay ongoing royalties to VLSI for any post-judgment infringement of the Asserted Patents;

H. That this is an exceptional case under 35 U.S.C. § 285, and that Intel pay VLSI's attorneys' fees and costs in this action; and

I. That VLSI be awarded such other and further relief, including equitable relief, as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), VLSI hereby demands a trial by jury on all issues triable to a jury.

Dated: April 11, 2019

Respectfully submitted,

By: */s/J. Mark Mann*

J. Mark Mann
State Bar No. 12926150
mark@themannfirm.com
G. Blake Thompson
State Bar No. 24042033
blake@themannfirm.com
MANN | TINDEL | THOMPSON
300 W. Main Street
Henderson, TX 75652
Telephone: 903.657.8540
Fax: 903.657.6003

Andy Tindel (Texas Bar No. 20054500)
atindel@andytindel.com
MANN | TINDEL | THOMPSON
112 E. Line Street, Suite 304
Tyler, Texas 75702
Telephone: (903) 596-0900
Facsimile: (903) 596-0909

Craig D. Cherry (Texas Bar No. 24012419)
ccherry@haleyolson.com
HALEY & OLSON, P.C.
100 N. Ritchie Road, Suite 200
Waco, Texas 76701
Telephone: (254) 776-3336
Facsimile: (254) 776-6823

Attorneys for Plaintiff VLSI Technology LLC