

**UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION**

VIDEOLABS, INC.,

Plaintiff,

v.

DELL TECHNOLOGIES INC. and
DELL INC.

Defendants.

Civil Action No. 6:21-cv-456

JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff VideoLabs, Inc. (“VideoLabs” or “Plaintiff”), by and through its undersigned counsel, complains and alleges against Dell Technologies Inc. and Dell Inc. (collectively “Dell” or “Defendants”) as follows:

NATURE OF THE ACTION

1. This is a civil action for infringement of U.S. Patent Nos. 7,769,238 and 8,139,878, (collectively, “the Asserted Patents”) arising under the patent laws of the United States, 35 U.S.C. §§ 1 et seq.

THE PARTIES

2. VideoLabs is a corporation organized under the laws of the State of Delaware, with its principal place of business in Palo Alto, California. Founded in October 2019, VideoLabs is a professional intellectual property services company and licensing platform with a primary focus on acquiring and licensing high-quality patents relevant to the video ecosystem. Video is a megatrend – it is an extremely important way in which people create, communicate and consume information and entertainment. Thousands of companies and their employees around the world use video and video technologies in their businesses. VideoLabs’ principals recognized that a

large number of companies would substantially benefit from an efficient avenue through which to take licenses to collections of highly valuable video-related patents. Based on this, at its founding and through to today, VideoLabs has acquired patents originating from some of the world's most recognizable and inventive companies, including Nokia Corporation, Alcatel-Lucent S.A., Siemens AG, Swisscom AG, 3Com, Panasonic, Ericsson, Samsung, LG, and Hewlett Packard Enterprise. VideoLabs has invested heavily and continues to identify and acquire important patents thereby continually increasing the value of its licensing platform and promoting greater efficiency for the industry.

3. On information and belief, defendant Dell Technologies Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682.

4. On information and belief, defendant Dell Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682. Dell Inc. has additional offices at 1404 Park Center Dr., Austin, Texas, 701 E. Parmer Lane, Bldg. PS2, Austin, Texas, 12500 Tech Ridge Road, Austin, Texas, 9715 Burnet Road, Austin, Texas, and 4309 Emma Browning Avenue, Austin, Texas.

JURISDICTION AND VENUE

5. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Dell pursuant to due process and/or the Texas Long Arm Statute because Dell has committed and continues to commit acts of patent infringement, including acts giving rise to this action, within the State of Texas and this District, and because Dell recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state. The Court's exercise of jurisdiction over Dell would not offend traditional notions of fair play and substantial justice because Dell has established minimum contacts with the forum.

7. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400 because a substantial part of the events or omissions giving rise to the claims occurred in this District, and Dell has committed acts of infringement and has a regular and established place of business in this District.

8. Dell has committed acts of infringement in this District, directly and/or through intermediaries, by, among other things, making, using, offering to sell, selling, and/or importing products and/or services that infringe the Asserted Patents, as alleged herein.

9. Dell has regular and established places of business in this District including a shared corporate office at One Dell Way, Round Rock, Texas 78682. Dell is also registered to do business in Texas.

VIDEOLABS' ASSERTED PATENTS

10. On August 3, 2010, the United States Patent Office issued U.S. Patent No. 7,769,238, titled "Picture Coding Method And Picture Decoding Method" (the "'238 patent"). A true and correct copy of the '238 patent is attached hereto as Exhibit A.

11. On March 20, 2012, the United States Patent Office issued U.S. Patent No. 8,139,878, titled "Picture Coding Method and Picture Decoding Method" (the "'878 patent"). A true and correct copy of the '878 patent is attached hereto as Exhibit B.

12. VideoLabs is the owner of all right, title, and interest in and to each of the Asserted Patents with full and exclusive right to bring suit to enforce the Asserted Patents, including the right to recover for past damages and/or royalties prior to the expiration of the Asserted Patents.

13. The Asserted Patents are valid and enforceable.

BACKGROUND

Dell

14. Dell manufactures, uses, imports, offers for sale, and/or sells products that incorporate context adaptive variable length coding (CAVLC) defined in the H.264 standard

(“Accused Products”). The Accused Products include, but are not limited to, laptops (*e.g.*, Latitude, Vostro, Inspiron, XPS, G-Series, Rugged, Chromebook Enterprise, Education, and Alienware), tablets and 2-in-1s (*e.g.*, XPS, Latitude, Inspiron, Rugged, Chromebook Enterprise, and Education) and desktops (*e.g.*, OptiPlex and OptiPlex Ultra).

COUNT I

Infringement of the '238 Patent

15. VideoLabs re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

16. In violation of 35 U.S.C. § 271(a), Dell has infringed the '238 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the Accused Products which contain each and every limitation of claim 1 of the '238 patent. Dell has infringed literally and/or under the doctrine of equivalents.

17. The Accused Products support the H.264 standard and CAVLC entropy encoding defined in the standard. In addition, the Accused Products are implemented in a manner that not only complies with the H.264 standard, but also infringes the '238 patent.

18. Each Accused Product is a receiving apparatus which receives multiplexed data which is obtained by multiplexing coded audio data and coded picture data.

19. H.264 carries audio and video multiplexed in a single stream. H.264 is directed to the picture portion of video, so devices containing H.264 encoders and decoders must demultiplex audio and picture data in order to obtain the H.264 picture data. Encoders multiplex the audio and pictures into a single stream, so that decoders receive the complete video presentation including sound. Decoders decode the stream to recreate the video. In the ISO Media File Format, which each Accused Product is capable of processing, a coded stream such as an H.264 video sequence or an audio stream is stored as a track, representing a sequence of coded data items or samples. Figure 8.32 below, illustrates an example of such multiplexed data, in which coded audio

data and coded picture data are multiplexed together.

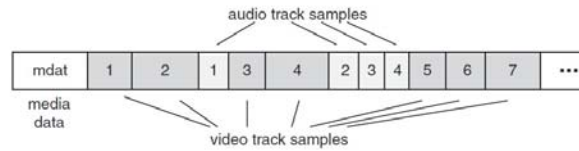


Figure 8.32 ISO Media File

See *The H.264 Advanced Video Compression Standard, 2nd Edition, Iain E. Richardson, ISBN: 978-0-470-51692-8, p. 247, Figure 8.32*. Each Accused Product complies with the H.264 standard and is configured to perform decoding of coded audio and picture data multiplexed in a single stream.

20. Each Accused Product has a demultiplexing unit configured to separate the multiplexed data into the coded audio data and the coded picture data. H.264 is directed to only the picture portion of video. Each Accused Product must therefore incorporate demultiplex circuitry to separate the coded audio and coded picture data in order to obtain the H.264 picture data. *Id.*

21. Each Accused Product has an audio processing unit configured to decode the separated coded audio data. By way of one representative example, the Dell XPS 13 2-in-1 laptop incorporates the Realtek ALC3281-CG audio controller that is configured to decode separated coded audio data.

Audio

The following table lists the audio specifications of your XPS 13 2-in-1 (9310 2n1).

Table 9. Audio specifications

Description		Values
Audio controller		Realtek ALC3281-CG
Stereo conversion		Supported
Internal audio interface		High definition audio interface
External audio interface		Universal Audio Jack
Number of speakers		2
Internal-speaker amplifier		Supported (Audio codec integrated)
External volume controls		Keyboard shortcut controls
Speaker output:		
	Average speaker output	2 W
	Peak speaker output	2.5 W
Subwoofer output		Not supported
Microphone		Digital-array microphones

See XPS 13 2-in-1 Setup and Specifications, Chapter 3, p. 14 (2020).

22. Each Accused Product has a picture decoding unit configured to decode the separated coded picture data. By way of one representative example, the Dell XPS 13 2-in-1 laptop incorporates an integrated Intel graphics processor (either UHD or Iris XE) that supports H.264 hardware decoding. The integrated graphics processor is configured to decode the separated coded picture data in accordance with H.264 standard requirements.

Processor

The following table lists the details of the processors supported by your XPS 13 2-in-1 (9310 2n1).

Table 3. Processor

Description	Option one	Option two	Option three	Option Four	Option Five
Processor type	11 th Generation Intel Core i3-1115G4	11 th Generation Intel Core i5-1135G7	11 th Generation Intel Core i5-1145G7	11 th Generation Intel Core i7-1165G7	11 th Generation Intel Core i7-1185G7
Processor wattage	13 W	13 W	15 W	13 W	15 W
Processor core count	2	4	4	4	4
Processor thread count	4	8	8	8	8
Processor speed	Up to 4.1 GHz	Up to 4.2 GHz	Up to 4.4 GHz	Up to 4.7 GHz	Up to 4.8 GHz
Processor cache	6 MB	8 MB	8 MB	12 MB	12 MB
Integrated graphics	Intel UHD Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics

See XPS 13 2-in-1 Setup and Specifications, Chapter 3, p. 11 (2020)

Features

DirectX* Support 	12.1
Vulkan* Support	Yes
OpenGL* Support 	4.6
H.264 Hardware Encode/Decode	Yes
H.265 (HEVC) Hardware Encode/Decode	Yes, 12-bit

See <https://ark.intel.com/content/www/us/en/ark/products/211014/intel-iris-xe-dedicated-graphics-card-80-eu.html>

23. The picture decoding unit in each Accused Product includes a block decoding unit configured to decode coded block data included in the coded picture data, the coded block data being obtained by dividing a picture signal into plural blocks, generating a residual block image from a block image of the respective blocks and a predictive block image obtained by intra-picture prediction or inter-picture prediction and coding, on a block basis, coefficients obtained by performing orthogonal transformation and quantization on the residual block image. In accordance with the H.264 standard, compliant H.264 decoders, such as that in the integrated Intel graphics processor, operate on a macroblock, consisting of a 16 x 16 block of luma samples and two corresponding blocks of chroma samples. A macroblock can be further portioned for inter prediction forming segmentations for motion representation as small as 4 x 4 luma samples in size. See generally, *ITU-T H.264, Series H: Audio Visual and Multimedia Systems, Infrastructure of Audiovisual Services – Coding of Moving Video, Advanced Video Coding for Generic Audio Visual Services (“H.264 Standard”), Section 0.6.3, p. 5 (09/2019)*. Two main coding types are specified in H.264, intra coding and inter coding. Intra coding is done without reference to other pictures while inter coding uses inter prediction of each block of sample values from some previously decoded picture. See generally, *H.264 Standard, Section 0.6.1, p. 4 (09/2019)*. H.264 decoding is based on the use of a block-based transform method for spatial redundancy removal. The resulting residual block is split into 4 x 4 blocks. These residual blocks are converted into the

transform domain where they are quantized. *See generally, H.264 Standard, Section 0.6.4, p. 5 (09/2019).* H.264 specifies an *entropy_coding_mode* flag that dictates the entropy encoding algorithm used to encode the picture data. When this flag is set to “0” the residual block data is coded using a CAVLC scheme. *See generally, H.264 Standard, Section 7.4.2.2, pp. 81-82 (09/2019).* In H.264 CAVLC encoding generally, the total number of non-zero coefficients included in a current block to be coded is derived. Since CAVLC is a context-adaptive variable length coding technique, the number of non-zero coefficients in neighboring blocks is correlated as part of the entropy coding process. A predictive value is used to select one of four encoding tables to use for encoding the number of non-zero coefficients for the current block to be coded and the total number of non-zero coefficients included in the current block is coded by the selected variable length code table. *See generally, H.264 Standard, Sections 7.4.5.3.2, 9.2.1, and Table 9-5, pp. 110, 214-218, (09/2019).* A H.264 compliant decoder reverses this process to decode the coded picture data.

24. The block decoding unit in each Accused Product includes a coefficient number decoding unit configured to decode the coded block data to obtain the number of non-zero coefficients which are coefficients included in a current block to be decoded and having a value other than “0.” In H.264, the total number of non-zero coefficients in the current block is encoded by the variable *coeff_token*. The coefficient number decoding unit in each Accused Product is configured to decode the coded block data by executing the function $\text{TotalCoeff}(\text{coeff_token})$ to return the number of non-zero transform coefficient levels derived from *coeff_token*. *See generally, H.264 Standard, Section 7.4.5.3.2, p. 110 (09/2019).* A “level” in this context is the value of a transform coefficient prior to scaling. *See generally, H.264 Standard, Section 3.175 (transform coefficient level definition), p. 15 (09/2019).*

25. The block decoding unit in each Accused Product includes a unit configured to obtain coefficients corresponding to a residual block image of the current block by decoding the

coded block data. H.264-compliant decoders, such as those in the Accused Products, read the encoded residual macroblock data and extract the coefficients that are encoded in that data. In accordance with H.264 requirements, the decoder parses the coded block data to obtain a list of coefficients corresponding to the residual block image. This involves extracting the residual luma and chroma coefficient blocks, calculating the quantization parameter, and carrying out inverse quantization and inverse transformation to (re)produce the residual sample blocks. The H.264 decoding process in this instance employs a CAVLC parsing process to obtain a list of transform coefficient levels (coeffLevel) of the luma block or the chroma block. *See generally, H.264 Standard, Section 9.2-9.2.4, pp. 214-223 (09/2019).*

26. The block decoding unit in each Accused Product is configured to obtain the residual block image of the current block by performing inverse quantization and inverse orthogonal transformation on the coefficients corresponding to the residual block image of the current block. As noted above, once the residual luma and chroma coefficient blocks are extracted, the H.264-compliant decoder in the Accused Products calculates a quantization parameter, and carries out inverse quantization and inverse transformation to (re)produce the residual sample blocks. *See generally, The H.264 Advanced Video Compression Standard, 2nd Edition, Iain E. Richardson, ISBN: 978-0-470-51692-8 (“Richardson”), p. 96.*

27. The block decoding unit in each Accused Product includes a reproducing unit configured to reproduce a block image of the current block, from the obtained residual block image and a predictive block image obtained by intra-picture prediction or inter-picture prediction. H.264-compliant decoders, such as those in the Accused Products, store previously-decoded macroblocks in the decoded picture buffer to use for predicting the current macroblock based on previous macroblocks, using the same predictions the encoder used.

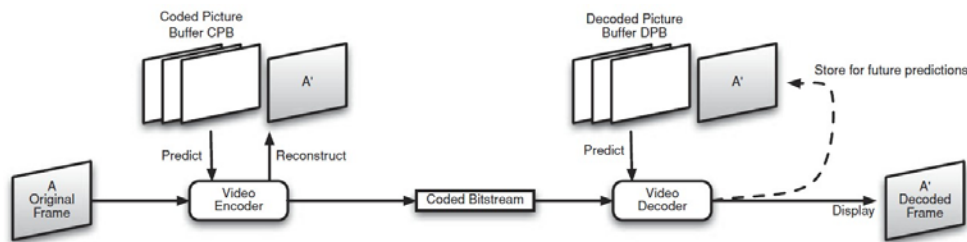


Figure 4.3 Video codec: high level view

See generally, Richardson, Figure 4.3. The H.264 decoder presents the reconstructed original video by adding the prediction to the decoded residual.

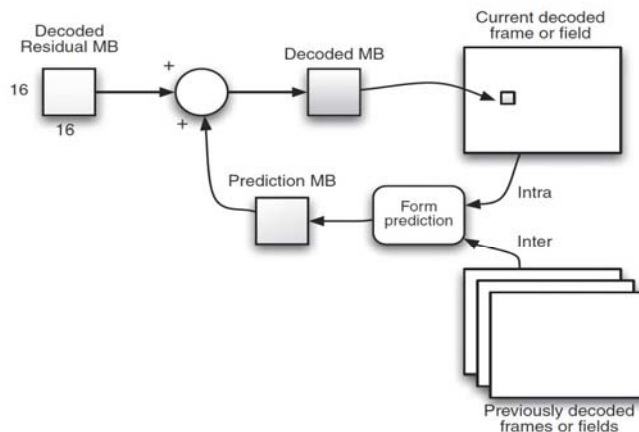


Figure 4.17 Reconstruction flow diagram

See generally, Richardson, Figure 4.17.

28. The coefficient number decoding unit in each Accused Product includes a determining unit configured to determine a predictive value for the number of non-zero coefficients included in the current block based on the number of non-zero coefficients included in a decoded block located on a periphery of the current block. The H.264-compliant decoder in the Accused Products obtains the number of non-zero coefficients in the left and above blocks to set the variable nC , the prediction of the current macroblock's number of non-zero coefficients based on the neighboring macroblocks' number of non-zero coefficients. See generally, *H.264 Standard, Section 9.2.1, pp. 214-216 (09/2019)*.

29. The coefficient number decoding unit in each Accused Product includes a selecting unit configured to select a variable length code table based on the determined predictive value. The H.264-compliant decoder in each of the Accused Products uses the predictive value nC to

select one of the variable length coding tables specified in Table 9-5 of the H.264 standard. *See generally, H.264 Standard, Section 9.2.1 and Table 9-5, pp. 214-218 (09/2019).*

30. The coefficient number decoding unit in each Accused Product includes a variable length decoding unit configured to perform variable length decoding on a coded stream which is generated by coding the number of the non-zero coefficients included in the current block, by using the selected variable length code table. Finally, the H.264-compliant decoder in the Accused Products uses the selected variable length code table to perform variable length decoding on the syntax element *coeff_token* in the coded stream. *See generally, H.264 Standard, Section 9.2.1 and Table 9-5, pp. 214-218 (09/2019).*

31. Dell is not licensed or otherwise authorized to practice the claims of the '238 patent.

32. By reason of Dell's infringement, VideoLabs has suffered and continues to suffer damages.

33. VideoLabs is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

COUNT II

Infringement of the '878 Patent

34. VideoLabs re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

35. In violation of 35 U.S.C. § 271(a), Dell has infringed the '878 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the Accused Products which practice each and every limitation of at least claim 1 of the '878 patent. Dell has infringed literally and/or under the doctrine of equivalents.

36. The Accused Products support the H.264 standard and CAVLC entropy encoding defined in the standard. In addition, the Accused Products are implemented in a manner that not only complies with the H.264 standard, but also infringes the '878 patent.

37. H.264 carries audio and video multiplexed in a single stream. H.264 is directed to the picture portion of video, so devices containing H.264 encoders and decoders must multiplex and demultiplex audio and picture data. Encoders multiplex the audio and pictures into a single stream, so that decoders receive the complete video presentation including sound. Decoders decode the stream to recreate the video. In the ISO Media File Format, which each Accused Product is capable of processing, a coded stream such as an H.264 video sequence or an audio stream is stored as a track, representing a sequence of coded data items or samples. Figure 8.32, below, illustrates an example of such multiplexed data, in which coded audio data and coded picture data are multiplexed together.

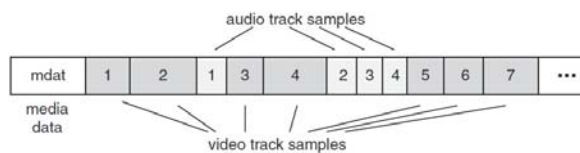


Figure 8.32 ISO Media File

See *The H.264 Advanced Video Compression Standard, 2nd Edition, Iain E. Richardson, ISBN: 978-0-470-51692-8, p. 247, Figure 8.32*. Each Accused Product complies with the H.264 standard and is configured to perform encoding of coded audio and picture data multiplexed in a single stream.

38. Each Accused Product is a transmitting apparatus which transmits multiplexed data which is obtained by multiplexing coded audio data and coded picture data. Each Accused Product has a multiplexing unit configured to separate the multiplexed data into the coded audio data and the coded picture data. Each Accused Product must therefore incorporate multiplexing circuitry to combine the coded audio and coded picture data in order to obtain the H.264 picture data. *Id.*

39. Each Accused Product includes an audio processing unit configured to code audio data to obtain coded audio data. By way of one representative example, the Dell XPS 13 2-in-1 laptop incorporates the Realtek ALC3281-CG audio controller that is configured to code audio

data.

Audio

The following table lists the audio specifications of your XPS 13 2-in-1 (9310 2n1).

Table 9. Audio specifications

Description		Values
Audio controller		Realtek ALC3281-CG
Stereo conversion		Supported
Internal audio interface		High definition audio interface
External audio interface		Universal Audio Jack
Number of speakers		2
Internal-speaker amplifier		Supported (Audio codec integrated)
External volume controls		Keyboard shortcut controls
Speaker output:		
	Average speaker output	2 W
	Peak speaker output	2.5 W
Subwoofer output		Not supported
Microphone		Digital-array microphones

See XPS 13 2-in-1 Setup and Specifications, Chapter 3, p. 14 (2020).

40. Each Accused Product includes a picture coding unit configured to code picture data to obtain coded picture data. By way of one representative example, the Dell XPS 13 2-in-1 laptop incorporates an integrated Intel graphics processor (either UHD or Iris XE) that supports H.264 hardware coding. The integrated graphics processor is configured to encode the picture data in accordance with H.264 standard requirements.

Processor

The following table lists the details of the processors supported by your XPS 13 2-in-1 (9310 2n1).

Table 3. Processor

Description	Option one	Option two	Option three	Option Four	Option Five
Processor type	11 th Generation Intel Core i3-1115G4	11 th Generation Intel Core i5-1135G7	11 th Generation Intel Core i5-1145G7	11 th Generation Intel Core i7-1165G7	11 th Generation Intel Core i7-1185G7
Processor wattage	13 W	13 W	15 W	13 W	15 W
Processor core count	2	4	4	4	4
Processor thread count	4	8	8	8	8
Processor speed	Up to 4.1 GHz	Up to 4.2 GHz	Up to 4.4 GHz	Up to 4.7 GHz	Up to 4.8 GHz
Processor cache	6 MB	8 MB	8 MB	12 MB	12 MB
Integrated graphics	Intel UHD Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics	Intel Iris Xe Graphics

See XPS 13 2-in-1 Setup and Specifications, Chapter 3, p. 11 (2020)

Features

DirectX* Support 	12.1
Vulkan* Support	Yes
OpenGL* Support 	4.6
H.264 Hardware Encode/Decode	Yes
H.265 (HEVC) Hardware Encode/Decode	Yes, 12-bit

See <https://ark.intel.com/content/www/us/en/ark/products/211014/intel-iris-xe-dedicated-graphics-card-80-eu.html>

41. Each Accused Product includes a multiplexing unit configured to multiplex the coded audio data and the coded picture data to obtain multiplexed data. Because the Accused Products can transmit H.264 coded audio and video information, the Accused Products include a multiplexing unit to multiplex the coded audio and picture data. Encoders multiplex the audio and pictures into a single stream, so that decoders receive the complete video presentation including sound. In the ISO Media File Format, which each Accused Product is capable of processing, a coded stream such as an H.264 video sequence or an audio stream is stored and transmitted as a track, representing a sequence of coded data items or samples. Figure 8.32, below, illustrates an example of such multiplexed data, in which coded audio data and coded picture data are multiplexed together.

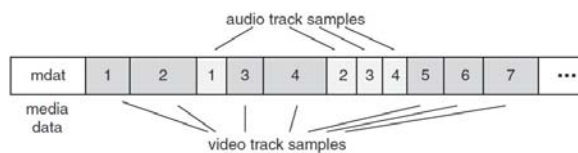


Figure 8.32 ISO Media File

See *The H.264 Advanced Video Compression Standard, 2nd Edition, Iain E. Richardson, ISBN: 978-0-470-51692-8, p. 247, Figure 8.32*. Each Accused Product complies with the H.264 standard and is configured to perform coding of coded audio and picture data multiplexed in a single stream.

Id.

42. The picture coding unit in each Accused Product includes a block coding unit configured to code a block image to obtain coded block data, the block image being obtained by dividing a picture signal into plural blocks, generating a residual block image from the block image of the respective blocks and a predictive block image obtained by intra-picture prediction or inter-picture prediction, and coding, on a block basis, coefficients obtained by performing orthogonal transformation and quantization on the residual block image. In accordance with the H.264 standard, compliant H.264 encoders, such as that in the integrated Intel graphics processor, operate on a macroblock, consisting of a 16 x 16 block of luma samples and two corresponding blocks of chroma samples. A macroblock can be further portioned for inter prediction forming segmentations for motion representation as small as a block 4 x 4 luma samples in size. *See generally, ITU-T H.264, Series H: Audio Visual and Multimedia Systems, Infrastructure of Audiovisual Services – Coding of Moving Video, Advanced Video Coding for Generic Audio Visual Services (“H.264 Standard”), Section 0.6.3, p. 5 (09/2019).* Two main coding types are specified in H.264, intra coding and inter-coding. Intra-coding is done without reference to other pictures while inter-coding uses inter-prediction of each block of sample values from some previously coded picture. *See generally, H.264 Standard, Section 0.6.1, p. 4 (09/2019).* H.264 encoding is based on the use of a block-based transform method for spatial redundancy removal. The resulting residual block is split into 4 x 4 blocks. These residual blocks are converted into the transform domain where they are quantized. *See generally, H.264 Standard, Section 0.6.4, p. 5 (09/2019).* H.264 specifies an *entropy_coding_mode* flag that dictates the entropy encoding algorithm used to encode the picture data. When this flag is set to “0” the residual block data is coded using a CAVLC scheme. *See generally, H.264 Standard, Section 7.4.2.2, pp. 81-82 (09/2019).*

43. The block coding unit includes a coefficient number coding unit configured to code a total number of non-zero coefficients included in a current block to be coded, each of the non-zero coefficients being a coefficient having a value other than “0.” In H.264 CAVLC encoding

generally, the total number of non-zero coefficients included in a current block to be coded is derived. Since CAVLC is a context-adaptive variable length coding technique, the number of non-zero coefficients in neighboring blocks is correlated as part of the entropy coding process. A predictive value is used to select one of four encoding tables to use for encoding the number of non-zero coefficients for the current block to be coded and the total number of non-zero coefficients included in the current block is coded by the selected variable length code table. *See generally, H.264 Standard, Sections 7.4.5.3.2, 9.2.1, and Table 9-5, pp. 110, 214-218, (09/2019)*

44. The coefficient number coding unit includes a determining unit configured to determine a predictive value for the total number of non-zero coefficients included in the current block based on a total number of non-zero coefficients included in a coded block located on a periphery of the current block. The H.264-compliant encoder in the Accused Products obtains the number of non-zero coefficients in the left and above blocks to set the variable nC , the prediction of the current macroblock's number of non-zero coefficients based on the neighboring macroblocks' number of non-zero coefficients. *See generally, H.264 Standard, Section 9.2.1, pp. 214-216 (09/2019).*

45. Each Accused Product has a selecting unit configured to select a variable length code table based on the determined predictive value. The H.264-compliant encoder in each of the Accused Products uses the predictive value nC to select one of the variable length coding tables specified in Table 9-5 of the H.264 standard. *See generally, H.264 Standard, Section 9.2.1 and Table 9-5, pp. 214-218 (09/2019).*

46. Each Accused Product has a variable length coding unit configured to perform variable length coding on the total number of the non-zero coefficients included in the current block, by using the selected variable length code table. The H.264-compliant decoder in the Accused Products uses the selected variable length code table to perform variable length coding on the syntax element *coeff_token* in the coded stream. *See generally, H.264 Standard, Section*

9.2.1 and Table 9-5, pp. 214-218 (09/2019).

47. Dell is not licensed or otherwise authorized to practice the claims of the '878 patent.

48. By reason of Dell's infringement, VideoLabs has suffered and continues to suffer damages.

49. VideoLabs is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff hereby demands a trial by jury as to all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully prays for the following relief:

- (a) A judgment that Defendants have infringed each of the Asserted Patents;
- (b) Damages adequate to compensate VideoLabs for Defendants' infringement of the Asserted Patents pursuant to 35 U.S.C. § 284;
- (c) Pre-judgment interest;
- (d) Post-judgment interest; and
- (e) Such other relief as the Court deems just and equitable.

Dated: May 3, 2021

/s/ M. Elizabeth Day w/permission Wesley Hill
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