UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

OPTICAL LICENSING, LLC, Plaintiff v. **ARROW ELECTRONICS, INC.,** Defendant	**Case No. 6:21-cv-00186** **JURY TRIAL DEMANDED**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Optical Licensing, LLC ("Optical" or "Plaintiff") files this Complaint for patent infringement against Arrow Electronics, Inc. ("Defendant"), and alleges as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under 35 U.S.C. § 1 *et seq*.

PARTIES

2. Optical is a limited liability company organized and existing under the laws of the State of Texas with its principal place of business in Plano, Texas.

3. Upon information and belief, Defendant is a corporation organized and existing under the laws of New York with a principal place of business at 1908 Kramer Lane, Suite 200, Austin, Texas 78758.

JURISDICTION AND VENUE

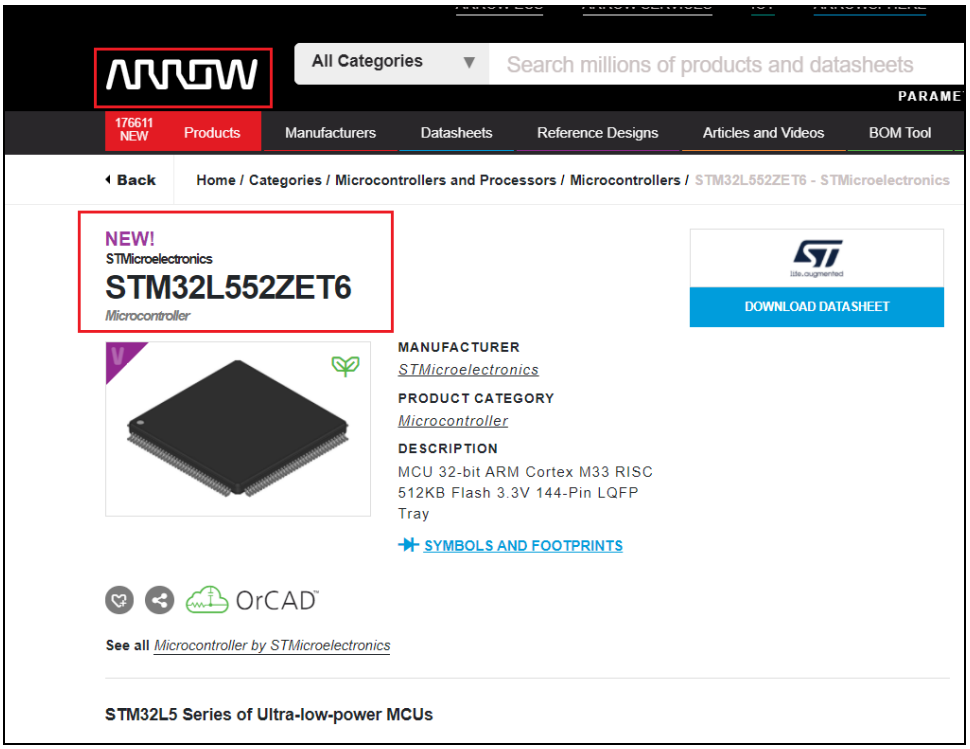
4. This Court has original jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. Upon information and belief, Defendant is subject to personal jurisdiction of this Court based upon it having regularly conducted business, including the acts complained of herein, within the State of Texas and/or deriving substantial revenue from goods and services provided to individuals in Texas and in this District.

6. Venue is proper in this District under 28 U.S.C. § 1400 because Defendant has committed acts of infringement and has regular and established places of business in this judicial district.

IDENTIFICATION OF THE ACCUSED PRODUCT

7. Upon information and belief, Defendant sells and offers for sale the STMicroelectronics STM32L552ZET6 microcontroller (hereafter, "Accused Product"), which includes RAM and a RAM controller for providing asynchronous and synchronous memory access.



Arrow Electronics Website, *available at*: https://www.arrow.com/en/products/stm32l552zet6/stmicroelectronics (last accessed May 10, 2021). The Accused Product is exemplified by the following references:

- "STMicroelectronics RM0438 Reference Manual" ("**STM1**"), *available at*: https://www.st.com/resource/en/reference_manual/dm00346336-stm32l552xx-and-stm32l562xx-advanced-arm-based-32-bit-mcus-stmicroelectronics.pdf (last accessed May 10, 2021).
- "STMicroelectronics STM32L552xx Datasheet" ("**STM2**"), *available at*: https://www.st.com/resource/en/datasheet/stm32l552ze.pdf (last accessed May 10, 2021).

- "STMicroelectronics STM32L552xx Data Brief" ("**STM3**"), *available at*: https://static6.arrow.com/aropdfconversion/1da1e143d60c11973e8e5c61d77611c471a34c5c/en.dm00504265.pdf (last access May 10, 2021)

8. The information contained in References **STM1**, **STM2**, and **STM3** is incorporated by reference as if set forth fully herein.

9. The information contained in Reference **STM1** accurately describes the operation and functionality of the Accused Product.

10. The information contained in Reference **STM2** accurately describes the operation and functionality of the Accused Product.

11. The information contained in Reference **STM3** accurately describes the operation and functionality of the Accused Product.

COUNT I
(Infringement of U.S. Patent No. 6,791,898)

12. Optical incorporates the above paragraphs as though fully set forth herein.

13. Plaintiff is the owner, by assignment, of U.S. Patent No. 6,791,898 (the "'898 Patent"), entitled MEMORY DEVICE PROVIDING ASYNCHRONOUS AND SYNCHRONOUS DATA TRANSFER, which issued on September 14, 2004. A copy of the '898 Patent is attached as Exhibit PX-898.

14. The '898 Patent is valid, enforceable, and was duly issued in full compliance with Title 35 of the United States Code.

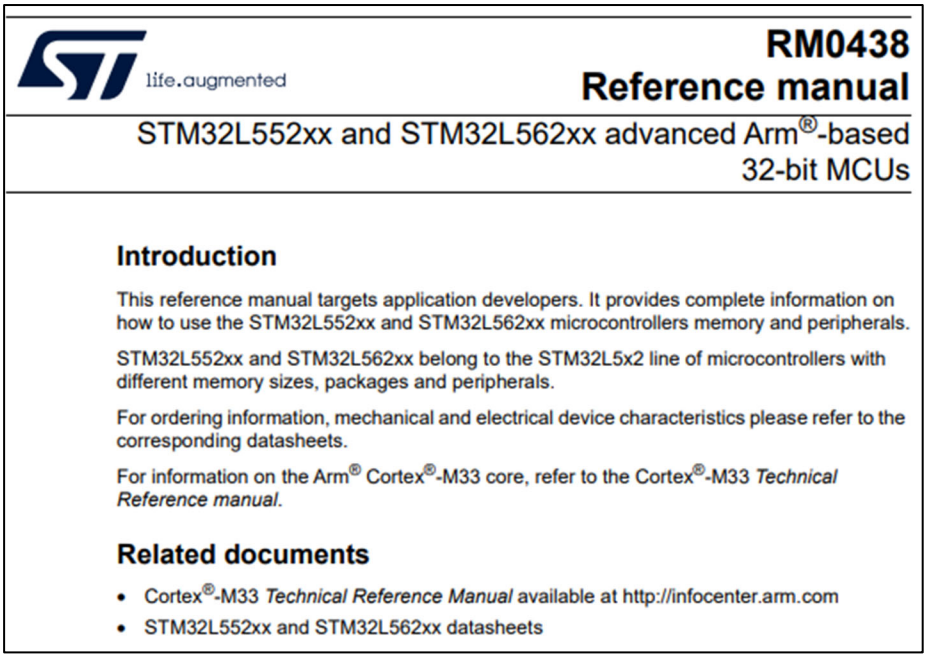
15. Upon information and belief, Defendant has been and is now infringing one or more claims of the '898 Patent under 35 U.S.C. § 271 by making, using, selling, and offering to sell the Accused Product in the United States without authority.

16. Claim 7 of the '898 recites:

> 7. A memory device comprising:
>
> an array of memory cells for storing data;
>
> an asynchronous/synchronous logic coupled to a plurality of control signals and said array of memory cells, wherein asynchronous transfer of data stored in said array of memory cells is provided based upon a first state of said control signals and wherein synchronous transfer of data stored in said array of memory cells is provided based upon a second state of said control signals; and
>
> a configuration register coupled to said asynchronous/synchronous logic, wherein said first state of said control signals or said second state of said control signals is latched for access by said asynchronous/synchronous logic.

17. Defendant infringes at least claim 7 of the '898 Patent by selling, using, and offering to sell the Accused Product.

18. The Accused Product is a memory device.



life.augmented

RM0438
Reference manual

STM32L552xx and STM32L562xx advanced Arm®-based 32-bit MCUs

Introduction

This reference manual targets application developers. It provides complete information on how to use the STM32L552xx and STM32L562xx microcontrollers memory and peripherals.

STM32L552xx and STM32L562xx belong to the STM32L5x2 line of microcontrollers with different memory sizes, packages and peripherals.

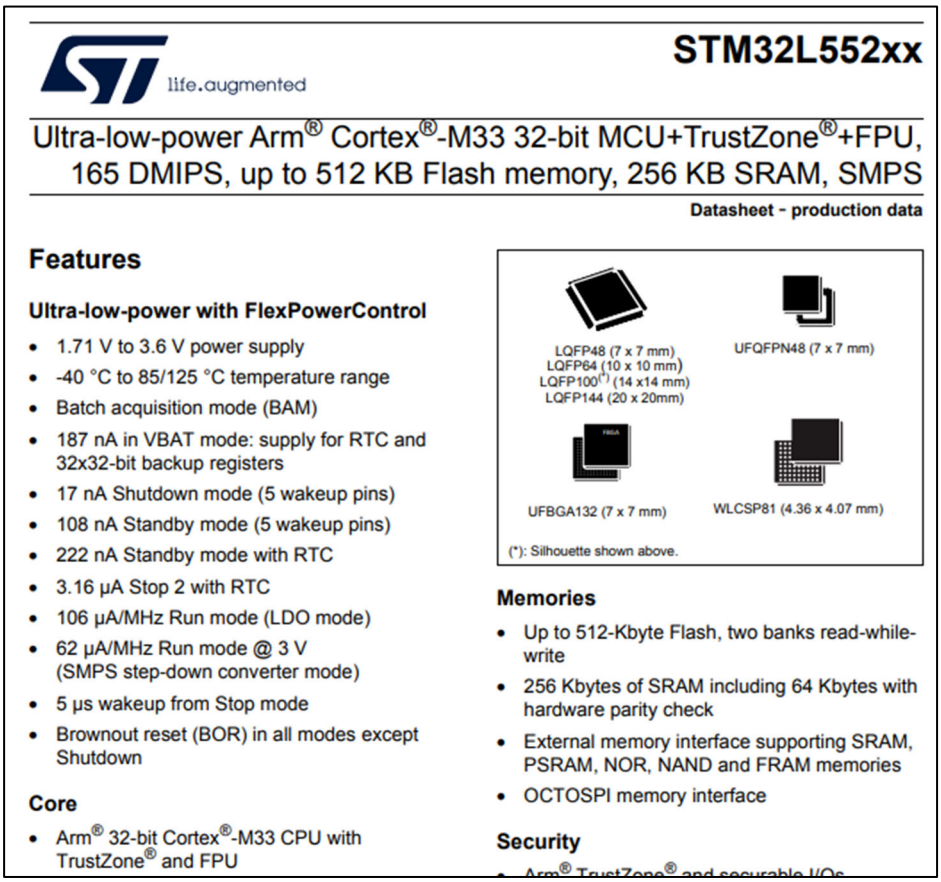
For ordering information, mechanical and electrical device characteristics please refer to the corresponding datasheets.

For information on the Arm® Cortex®-M33 core, refer to the Cortex®-M33 *Technical Reference manual*.

Related documents

- Cortex®-M33 *Technical Reference Manual* available at http://infocenter.arm.com
- STM32L552xx and STM32L562xx datasheets

Source: **STM1**.



life.augmented

STM32L552xx

Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS

Datasheet - production data

Features

Ultra-low-power with FlexPowerControl

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- Batch acquisition mode (BAM)
- 187 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
- 17 nA Shutdown mode (5 wakeup pins)
- 108 nA Standby mode (5 wakeup pins)
- 222 nA Standby mode with RTC
- 3.16 µA Stop 2 with RTC
- 106 µA/MHz Run mode (LDO mode)
- 62 µA/MHz Run mode @ 3 V (SMPS step-down converter mode)
- 5 µs wakeup from Stop mode
- Brownout reset (BOR) in all modes except Shutdown

Core

- Arm® 32-bit Cortex®-M33 CPU with TrustZone® and FPU

LQFP48 (7 x 7 mm)
LQFP64 (10 x 10 mm)
LQFP100(*) (14 x14 mm)
LQFP144 (20 x 20mm)

UFQFPN48 (7 x 7 mm)

UFBGA132 (7 x 7 mm)

WLCSP81 (4.36 x 4.07 mm)

(*): Silhouette shown above.

Memories

- Up to 512-Kbyte Flash, two banks read-while-write
- 256 Kbytes of SRAM including 64 Kbytes with hardware parity check
- External memory interface supporting SRAM, PSRAM, NOR, NAND and FRAM memories
- OCTOSPI memory interface

Security

- Arm® TrustZone® and securable I/Os

Source: **STM2**.

life.augmented

STM32L552xx

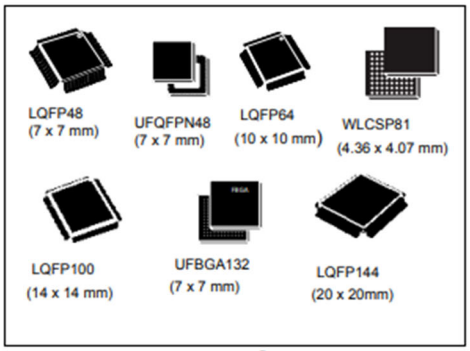
Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS

Data brief

Features

Ultra-low-power with FlexPowerControl

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- Batch acquisition mode (BAM)
- 225 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
- 33 nA Shutdown mode (5 wakeup pins)
- 110 nA Standby mode (5 wakeup pins)
- 385 nA Standby mode with RTC
- 3.6 µA Stop 2 with RTC

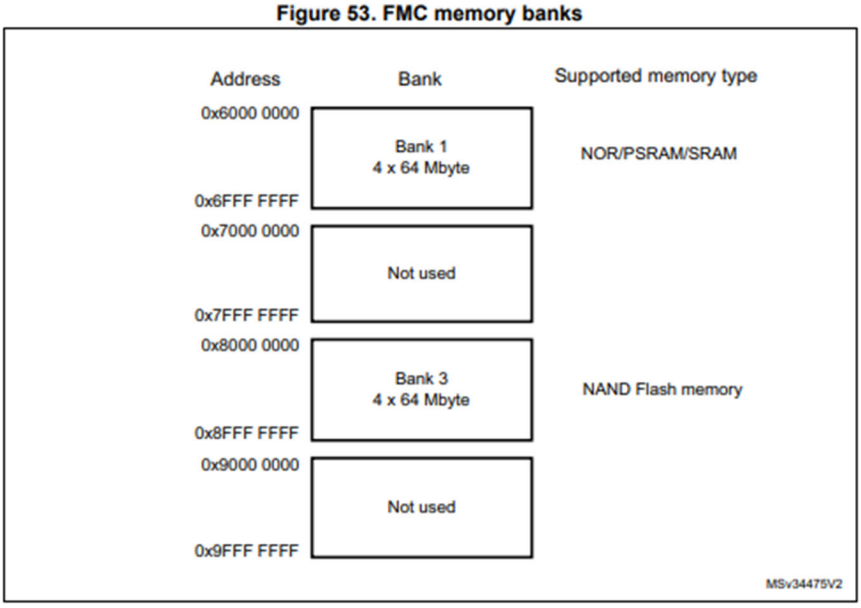


- 27400 SecureMark-TLS® score

Source: **STM3**.

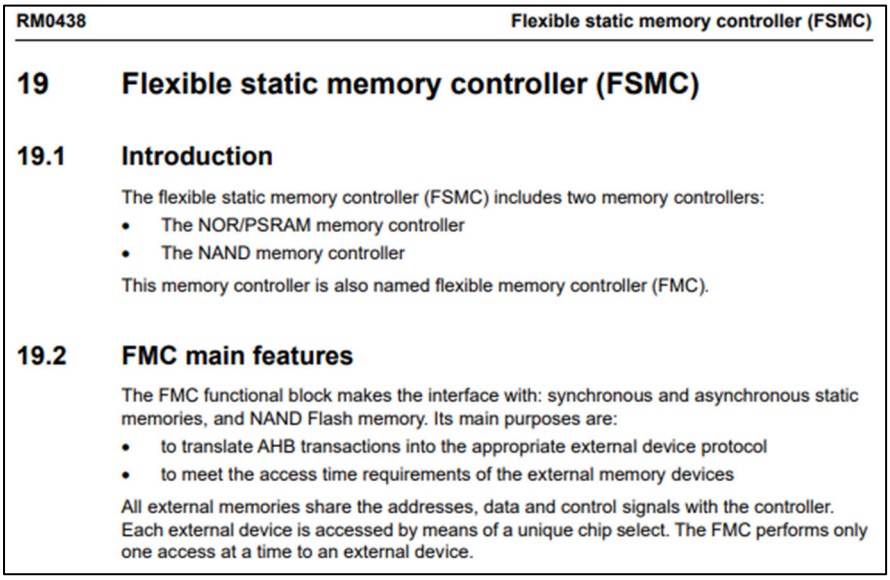
19. The Accused Product comprises an array of memory cells for storing data.

Figure 53. FMC memory banks



Source: **STM1**.

20. The Accused Product comprises an asynchronous/synchronous logic coupled to a plurality of control signals and the array of memory cells, wherein asynchronous transfer of data stored in the array of memory cells is provided based upon a first state of the control signals and wherein synchronous transfer of data stored in the array of memory cells is provided based upon a second state of the control signals.



RM0438 Flexible static memory controller (FSMC)

19 Flexible static memory controller (FSMC)

19.1 Introduction

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND memory controller

This memory controller is also named flexible memory controller (FMC).

19.2 FMC main features

The FMC functional block makes the interface with: synchronous and asynchronous static memories, and NAND Flash memory. Its main purposes are:

- to translate AHB transactions into the appropriate external device protocol
- to meet the access time requirements of the external memory devices

All external memories share the addresses, data and control signals with the controller. Each external device is accessed by means of a unique chip select. The FMC performs only one access at a time to an external device.

Source: **STM1**.

19.6 NOR Flash/PSRAM controller

The FMC generates the appropriate signal timings to drive the following types of memories:

- Asynchronous SRAM, FRAM and ROM
  - 8 bits
  - 16 bits
- PSRAM (CellularRAM™)
  - Asynchronous mode
  - Burst mode for synchronous accesses
  - Multiplexed or non-multiplexed
- NOR Flash memory
  - Asynchronous mode
  - Burst mode for synchronous accesses
  - Multiplexed or non-multiplexed

The FMC outputs a unique chip select signal, NE[4:1], per bank. All the other signals (addresses, data and control) are shared.

The FMC supports a wide range of devices through a programmable timings among which:

- Programmable wait states (up to 15)
- Programmable bus turnaround cycles (up to 15)
- Programmable output enable and write enable delays (up to 15)
- Independent read and write timings and protocol to support the widest variety of memories and timings
- Programmable continuous clock (FMC_CLK) output.

The FMC Clock (FMC_CLK) is a submultiple of the HCLK clock. It can be delivered to the selected external device either during synchronous accesses only or during asynchronous and synchronous accesses depending on the CCKEN bit configuration in the FMC_BCR1 register:

- If the CCLKEN bit is reset, the FMC generates the clock (CLK) only during synchronous accesses (Read/write transactions).
- If the CCLKEN bit is set, the FMC generates a continuous clock during asynchronous and synchronous accesses. To generate the FMC_CLK continuous clock, Bank 1 must be configured in Synchronous mode (see *Section 19.6.6: NOR/PSRAM controller registers*). Since the same clock is used for all synchronous memories, when a continuous output clock is generated and synchronous accesses are performed, the AHB data size has to be the same as the memory data width (MWID) otherwise the FMC_CLK frequency is changed depending on AHB data transaction (refer to *Section 19.6.5: Synchronous transactions* for FMC_CLK divider ratio formula).

The size of each bank is fixed and equal to 64 Mbytes. Each bank is configured through dedicated registers (see *Section 19.6.6: NOR/PSRAM controller registers*).

The programmable memory parameters include access times (see *Table 119*) and support for wait management (for PSRAM and NOR Flash accessed in Burst mode).

Source: **STM1**.

Bit 20 **CCLKEN:** Continuous clock enable

This bit enables the FMC_CLK clock output to external memory devices.
0: The FMC_CLK is only generated during the synchronous memory access (read/write transaction). The FMC_CLK clock ratio is specified by the programmed CLKDIV value in the FMC_BCRx register (default after reset).
1: The FMC_CLK is generated continuously during asynchronous and synchronous access. The FMC_CLK clock is activated when the CCLKEN is set.

Note: The CCLKEN bit of the FMC_BCR2..4 registers is don't care. It is only enabled through the FMC_BCR1 register. Bank 1 must be configured in Synchronous mode to generate the FMC_CLK continuous clock.

Note: If CCLKEN bit is set, the FMC_CLK clock ratio is specified by CLKDIV value in the FMC_BTR1 register. CLKDIV in FMC_BWTR1 is don't care.

Note: If the Synchronous mode is used and CCLKEN bit is set, the synchronous memories connected to other banks than Bank 1 are clocked by the same clock (the CLKDIV value in the FMC_BTR2..4 and FMC_BWTR2..4 registers for other banks has no effect.)

Bit 19 **CBURSTRW:** Write burst enable

For PSRAM (CRAM) operating in Burst mode, the bit enables synchronous accesses during write operations. The enable bit for synchronous read accesses is the BURSTEN bit in the FMC_BCRx register.
0: Write operations are always performed in Asynchronous mode.
1: Write operations are performed in Synchronous mode.

Bits 18:16 **CPSIZE[2:0]**: CRAM page size

These are used for CellularRAM™ 1.5 which does not allow burst access to cross the address boundaries between pages. When these bits are configured, the FMC controller splits automatically the burst access when the memory page size is reached (refer to memory datasheet for page size).
000: No burst split when crossing page boundary (default after reset)
001: 128 bytes
010: 256 bytes
011: 512 bytes
100: 1024 bytes
Others: reserved

Bit 15 **ASYNCWAIT**: Wait signal during asynchronous transfers

This bit enables/disables the FMC to use the wait signal even during an asynchronous protocol.
0: NWAIT signal is not taken in to account when running an asynchronous protocol (default after reset).
1: NWAIT signal is taken in to account when running an asynchronous protocol.

Bit 14 **EXTMOD:** Extended mode enable

This bit enables the FMC to program the write timings for non multiplexed asynchronous accesses inside the FMC_BWTR register, thus resulting in different timings for read and write operations.
0: values inside FMC_BWTR register are not taken into account (default after reset)
1: values inside FMC_BWTR register are taken into account

Note: When the Extended mode is disabled, the FMC can operate in mode 1 or mode 2 as follows:

- *Mode 1 is the default mode when the SRAM/PSRAM memory type is selected (MTYP = 0x0 or 0x01)*
- *Mode 2 is the default mode when the NOR memory type is selected (MTYP = 0x10).*

Source: **STM1**.

Bit 13 **WAITEN:** Wait enable bit
This bit enables/disables wait-state insertion via the NWAIT signal when accessing the memory in Synchronous mode.
0: NWAIT signal is disabled (its level not taken into account, no wait state inserted after the programmed Flash latency period).
1: NWAIT signal is enabled (its level is taken into account after the programmed latency period to insert wait states if asserted) (default after reset).

Bit 12 **WREN:** Write enable bit
This bit indicates whether write operations are enabled/disabled in the bank by the FMC.
0: Write operations are disabled in the bank by the FMC, an AHB error is reported.
1: Write operations are enabled for the bank by the FMC (default after reset).

Bit 11 **WAITCFG:** Wait timing configuration
The NWAIT signal indicates whether the data from the memory are valid or if a wait state must be inserted when accessing the memory in Synchronous mode. This configuration bit determines if NWAIT is asserted by the memory one clock cycle before the wait state or during the wait state:
0: NWAIT signal is active one data cycle before wait state (default after reset).
1: NWAIT signal is active during wait state (not used for PSRAM).

Bit 10 Reserved, must be kept at reset value.

Bit 9 **WAITPOL:** Wait signal polarity bit
Defines the polarity of the wait signal from memory used for either in Synchronous or Asynchronous mode.
0: NWAIT active low (default after reset)
1: NWAIT active high

Bit 8 **BURSTEN:** Burst enable bit
This bit enables/disables synchronous accesses during read operations. It is valid only for synchronous memories operating in Burst mode.
0: Burst mode disabled (default after reset). Read accesses are performed in Asynchronous mode.
1: Burst mode enable. Read accesses are performed in Synchronous mode.

Bit 7 Reserved, must be kept at reset value.

Bit 6 **FACCEN:** Flash access enable
Enables NOR Flash memory access operations.
0: Corresponding NOR Flash memory access is disabled.
1: Corresponding NOR Flash memory access is enabled (default after reset).

Bits 5:4 **MWID[1:0]:** Memory data bus width
Defines the external memory device width, valid for all type of memories.
00: 8 bits
01: 16 bits (default after reset)
10: reserved
11: reserved

Source: **STM1**.

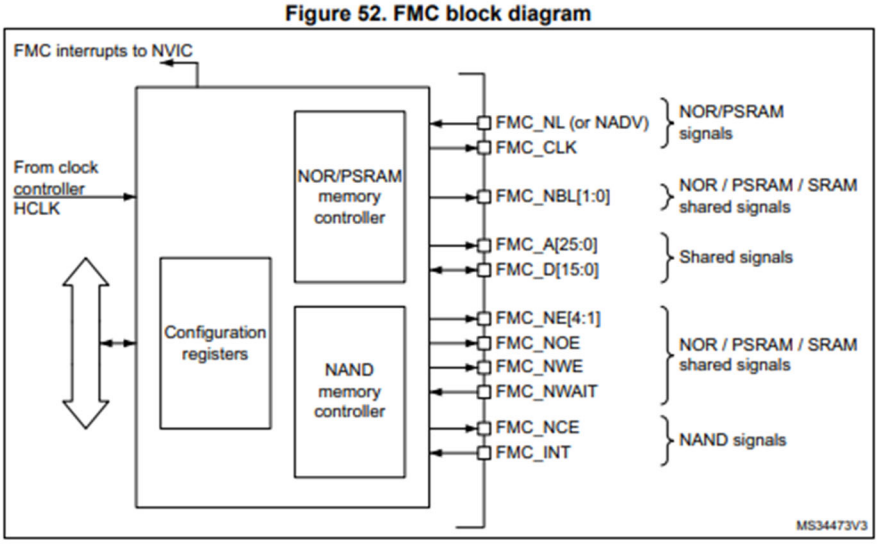
19.3 FMC block diagram

The FMC consists of the following main blocks:

- The AHB interface (including the FMC configuration registers)
- The NOR Flash/PSRAM/SRAM controller

The block diagram is shown in the figure below.

Figure 52. FMC block diagram



Source: **STM1**.

21. The Accused Product comprises a configuration register coupled to the asynchronous/synchronous logic, wherein the first state of the control signals or the second state of the control signals is latched for access by the asynchronous/synchronous logic.

19.5 External device address mapping

From the FMC point of view, the external memory is divided into fixed-size banks of 256 Mbytes each (see *Figure 53*):

- Bank 1 used to address up to 4 NOR Flash memory or PSRAM devices. This bank is split into 4 NOR/PSRAM subbanks with 4 dedicated chip selects, as follows:
  - Bank 1 - NOR/PSRAM 1
  - Bank 1 - NOR/PSRAM 2
  - Bank 1 - NOR/PSRAM 3
  - Bank 1 - NOR/PSRAM 4
- Bank 3 used to address NAND Flash memory devices.The MPU memory attribute for this space must be reconfigured by software to Device.

For each bank the type of memory to be used can be configured by the user application through the Configuration register.

Source: **STM1**.

This situation occurs when a byte access is requested to a 16-bit wide Flash memory. Since the device cannot be accessed in Byte mode (only 16-bit words can be read/written from/to the Flash memory), Write transactions and Read transactions are allowed (the controller reads the entire 16-bit memory word and uses only the required byte).

Wrap support for NOR Flash/PSRAM

Wrap burst mode for synchronous memories is not supported. The memories must be configured in Linear burst mode of undefined length.

Configuration registers

The FMC can be configured through a set of registers. Refer to *Section 19.6.6*, for a detailed description of the NOR Flash/PSRAM controller registers. Refer to *Section 19.7.7*, for a detailed description of the NAND Flash registers.

Source: **STM1**.

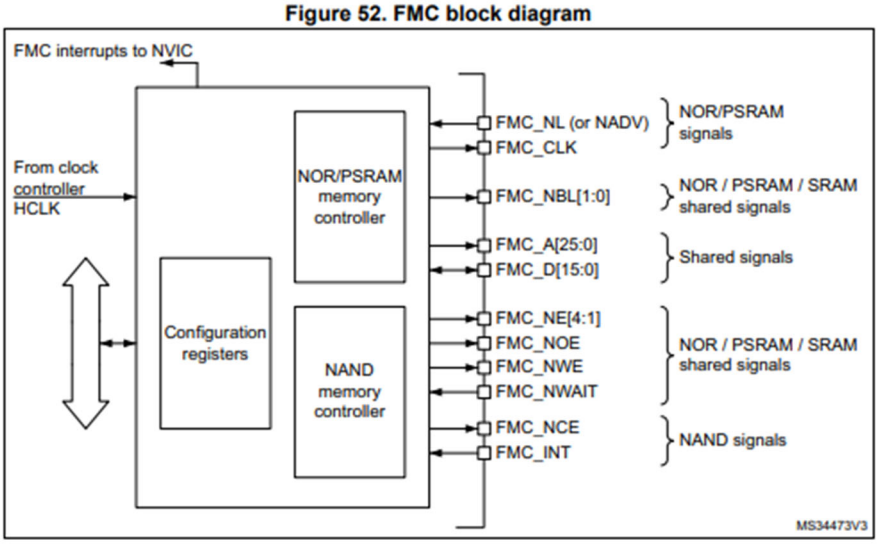
19.3 FMC block diagram

The FMC consists of the following main blocks:

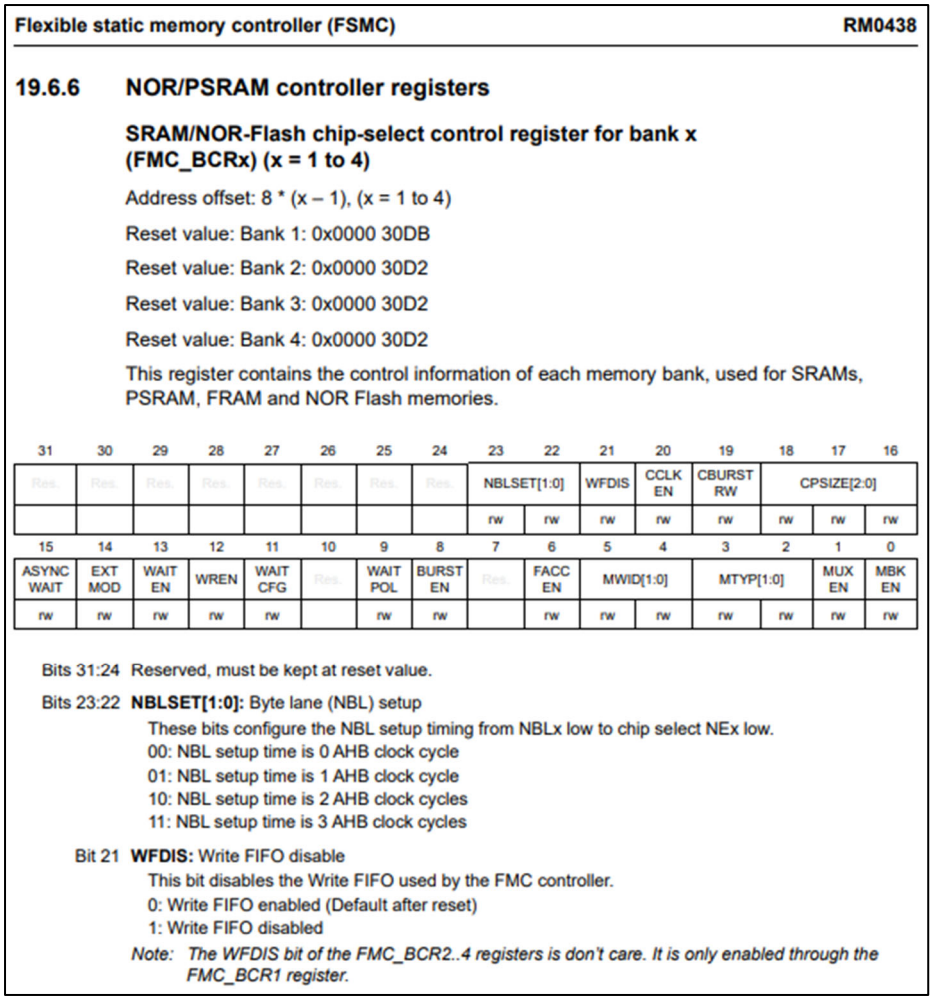
- The AHB interface (including the FMC configuration registers)
- The NOR Flash/PSRAM/SRAM controller

The block diagram is shown in the figure below.

Figure 52. FMC block diagram



Source: **STM1**.



Flexible static memory controller (FSMC) RM0438

19.6.6 NOR/PSRAM controller registers

SRAM/NOR-Flash chip-select control register for bank x (FMC_BCRx) (x = 1 to 4)

Address offset: 8 * (x – 1), (x = 1 to 4)

Reset value: Bank 1: 0x0000 30DB

Reset value: Bank 2: 0x0000 30D2

Reset value: Bank 3: 0x0000 30D2

Reset value: Bank 4: 0x0000 30D2

This register contains the control information of each memory bank, used for SRAMs, PSRAM, FRAM and NOR Flash memories.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	NBLSET[1:0]		WFDIS	CCLK EN	CBURST RW	CPSIZE[2:0]		
								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASYNC WAIT	EXT MOD	WAIT EN	WREN	WAIT CFG	Res.	WAIT POL	BURST EN	Res.	FACC EN	MWID[1:0]		MTYP[1:0]		MUX EN	MBK EN
rw	rw	rw	rw	rw		rw	rw		rw	rw	rw	rw	rw	rw	rw

Bits 31:24 Reserved, must be kept at reset value.

Bits 23:22 **NBLSET[1:0]:** Byte lane (NBL) setup

These bits configure the NBL setup timing from NBLx low to chip select NEx low.
00: NBL setup time is 0 AHB clock cycle
01: NBL setup time is 1 AHB clock cycle
10: NBL setup time is 2 AHB clock cycles
11: NBL setup time is 3 AHB clock cycles

Bit 21 **WFDIS:** Write FIFO disable

This bit disables the Write FIFO used by the FMC controller.
0: Write FIFO enabled (Default after reset)
1: Write FIFO disabled

Note: The WFDIS bit of the FMC_BCR2..4 registers is don't care. It is only enabled through the FMC_BCR1 register.

Source: **STM1**.

22. Plaintiff has been damaged by Defendant's infringing activities.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests the Court enter judgment against Defendant:

1. declaring that the Defendant has infringed the '898 Patent;

2. awarding Plaintiff its damages suffered as a result of Defendant's infringement of the '898 Patent;

3. awarding Plaintiff its costs, attorneys' fees, expenses, and interest; and

4. granting Plaintiff such further relief as the Court finds appropriate.

JURY DEMAND

Plaintiff demands trial by jury, Under Fed. R. Civ. P. 38.

Dated: May 11, 2021

Respectfully submitted,

/s/ Raymond W. Mort, III

Raymond W. Mort, III
Texas State Bar No. 00791308
raymort@austinlaw.com

THE MORT LAW FIRM, PLLC
100 Congress Ave, Suite 2000
Austin, Texas 78701
Tel/Fax: (512) 865-7950

ATTORNEY FOR PLAINTIFF