UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
DALLAS DIVISION

RANGING OPTICS LLC, Plaintiff v. **CALLAWAY GOLF COMPANY** Defendant	**Case No. 3:21-cv-1108** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Ranging Optics LLC ("Ranging Optics" or "Plaintiff") hereby asserts the following claims for patent infringement against Defendant Callaway Golf Company ("Defendant" or "Callaway"), and alleges as follows:

SUMMARY

1. Ranging Optics owns United States Patent Nos. 6,512,574 ("the '574 patent"), and 7,443,927 ("the '927 patent") (collectively, the "Asserted Patents").

2. Defendant has infringed and continues to infringe at least one or more claims of each of Ranging Optic's Asserted Patents at least by making, using, selling, and/or offering to sell a number of its laser range finder products including, *inter alia*, the Callaway 300 Pro Laser Rangefinder (collectively, the "Accused Product").

3. By this action, Ranging Optics seeks to obtain compensation for the harm Ranging Optics has suffered as a result of Defendant's infringement of the Asserted Patents.

NATURE OF THE ACTION

4. This is a civil action for patent infringement arising under the patent laws of the

United States, 35 U.S.C. § 1 *et seq*.

5. Defendant has infringed and continues to infringe at least one or more claims of each of Ranging Optic's Asserted Patents at least by making, using, selling, and/or offering to sell its products and services in the United States, including in this District.

6. Ranging Optics is the legal owner by assignment of the Asserted Patents, which were duly and legally issued by the United States Patent and Trademark Office ("USPTO"). Ranging Optics seeks monetary damages for Defendant's infringement of the Asserted Patents.

THE PARTIES

7. Plaintiff Ranging Optics LLC is a Texas limited liability company with its principal place of business at 17330 Preston Road Ste 200, Dallas, TX 75252. Ranging Optics is the owner of intellectual property rights at issue in this action.

8. Upon information and belief, Defendant is a corporation organized and existing under the laws of Delaware, with a principal place of business at 2180 Rutherford Rd. Carlsbad, CA 92008-7328.

9. On information and belief, Defendant directly and/or indirectly develops, designs, manufactures, distributes, markets, offers to sell and/or sells infringing products and services in the United States, including in the Northern District of Texas, and otherwise directs infringing activities to this District in connection with its products and services.

JURISDICTION AND VENUE

10. As this is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*., this Court has subject matter jurisdiction over the matters asserted herein under 28 U.S.C. §§ 1331 and 1338(a).

11. In particular, Defendant has committed and continues to commit acts of

infringement in violation of 35 U.S.C. § 271, and has made, used, marketed, distributed, offered for sale, sold, and/or imported infringing products in the State of Texas, including in this District, and engaged in infringing conduct within and directed at or from this District. For example, Defendant has purposefully and voluntarily placed the Accused Products into the stream of commerce with the expectation that the Accused Products will be used in this District. The Accused Products have been and continue to be distributed to and used in this District. Defendant's acts cause and have caused injury to Ranging Optics, including within this District.

12. Venue is proper in this District under the provisions of 28 U.S.C. §§ 1391 and 1400(b) at least because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendant has committed acts of infringement in this District. Furthermore, Defendant has a regular and established place of business in the District located at 15221 N Beach St, Fort Worth, TX 76177, as well as 8787 Park Lane, Dallas, TX 75231.

The '574 Patent

13. U.S. Patent No. 6,512,574 ("the '574 Patent") is titled "Light Receiving Circuit of Laser Range Finder," and was issued on January 28, 2003. A true and correct copy of the '574 Patent is attached as Exhibit PX-574.

14. The '574 Patent was filed on February 12, 2001 as U.S. Patent Application No. 09/780,364.

15. Ranging Optics is the owner of all rights, title, and interest in and to the '574 Patent, with the full and exclusive right to bring suit to enforce the '574 Patent, including the right to recover for past infringement.

16. The '574 Patent is valid and enforceable under United States Patent Laws.

17. The '574 Patent disclosed, among other things, "a light receiving circuit of a laser

range finder comprising a photo-sensitive element, a conversion resistance amplifying loop, and main amplification loop, and a one short circuit." PX-574 at Abstract.

18. The '574 Patent recognized various shortcomings of existing range finder device. As one example, traditional laser range funders employed a pulse type of the laser transmitter to transmit short laser pulses of about 20 nanoseconds onto a target. *Id.* at 1:12-15. "The reflected laser signal from the target is received by employing a low noise high sensitivity laser received to evaluate the distance" using a mathematical formula which includes calculating the time delay. *Id.* at 1:15-20. However, noise may interfere with the calculation of the time delay and noise increases as the distance measured increases. To overcome the problems in the prior art, the '574 Patent discloses "a light receiving receiver with a bias stabilized main amplifier followed by a one-shot circuit to get a digital output signal with fixed pulse width." *Id.* at 1:42-45. This novel apparatus provides a function of maximum sensitivity for the laser receiving circuit, therefore increasing the ranging distance of the laser range finger.

The '927 Patent

19. U.S. Patent No. 7,443,927 ("the '927 Patent") is titled "Signal Detector," and was issued on October 28, 2008. A true and correct copy of the '927 Patent is attached as Exhibit PX-927.

20. The '927 Patent was filed on June 12, 2007 as U.S. Patent Application No. 11/761,439.

21. Ranging Optics is the owner of all rights, title, and interest in and to the '927 Patent, with the full and exclusive right to bring suit to enforce the '927 Patent, including the right to recover for past infringement.

22. The '927 Patent is valid and enforceable under United States Patent Laws.

23. The '927 Patent discloses, among other things, "a signal detector compris[ing] a signal translator, a data signal detector, a clock signal detector and an inputting control circuit for detecting abnormal clock and data signals." PX-927 at Abstract.

24. The '927 Patent recognized various shortcomings of existing types of "[signal] detectors in the market for various uses, such as fire warning, anti-theft, quantity surveying and so on…" *Id.* at 1:16-18. These signal detection devices detect conditions such as temperature, pressure or light and send out a warning signal. *Id.* at 1:18-20. However, once a clock signal is interrupted during a transmission, the whole course of transmission is interrupted as well without any warning. *Id.* at 1:21-25. These interruptions cause delays in time and transmission, thereby wasting valuable resources. *Id.* at 1:26-27. Furthermore, if a short circuit or some other factor cause the system, to continuously output a series of data signals, the abnormal data transmission may cause the transmission facility as well as the laser to become overly exhausted or break down. *Id.* at :28-32.

25. The '927 provided a solution to this problem by among other things, providing a novel signal detector comprising a signal translator, a data signal detector and an inputting control circuit. *Id.* at 1:38-40. The signal translator converts differential data signals into a single data signal and the data signal detector outputs a data detecting signal according to the signal data signal. *Id.* at 1:4-43. The '927 Patent further utilized an interrupting control circuit which receives the data detecting signal and outputs a shutdown signal when the single data signal is at a high voltage level over a predefined ratio. *Id.* at 1:43-46.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 6,512,574

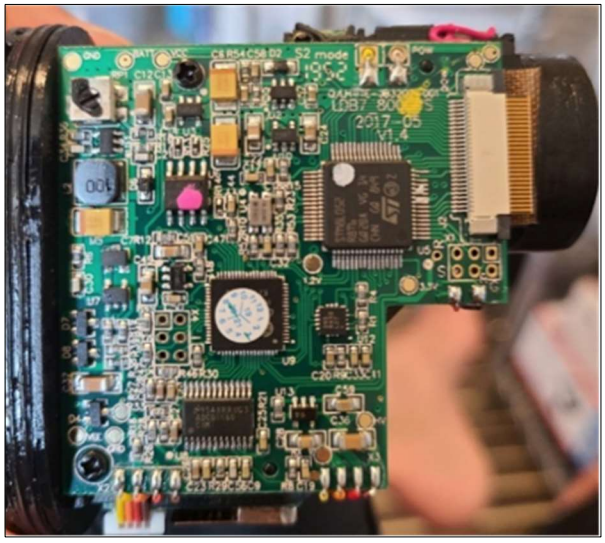
26. Ranging Optics incorporates by reference and re-alleges paragraphs 13-18 of this Complaint as if fully set forth herein.

27. Defendant has infringed, either literally or under the doctrine of equivalents, the '574 Patent in violation of 35 U.S.C. § 271 *et seq*., directly and/or indirectly, by having made, used, offered for sale, or sold in the United States, and/or imported into the United States without authority or license the Accused Products.

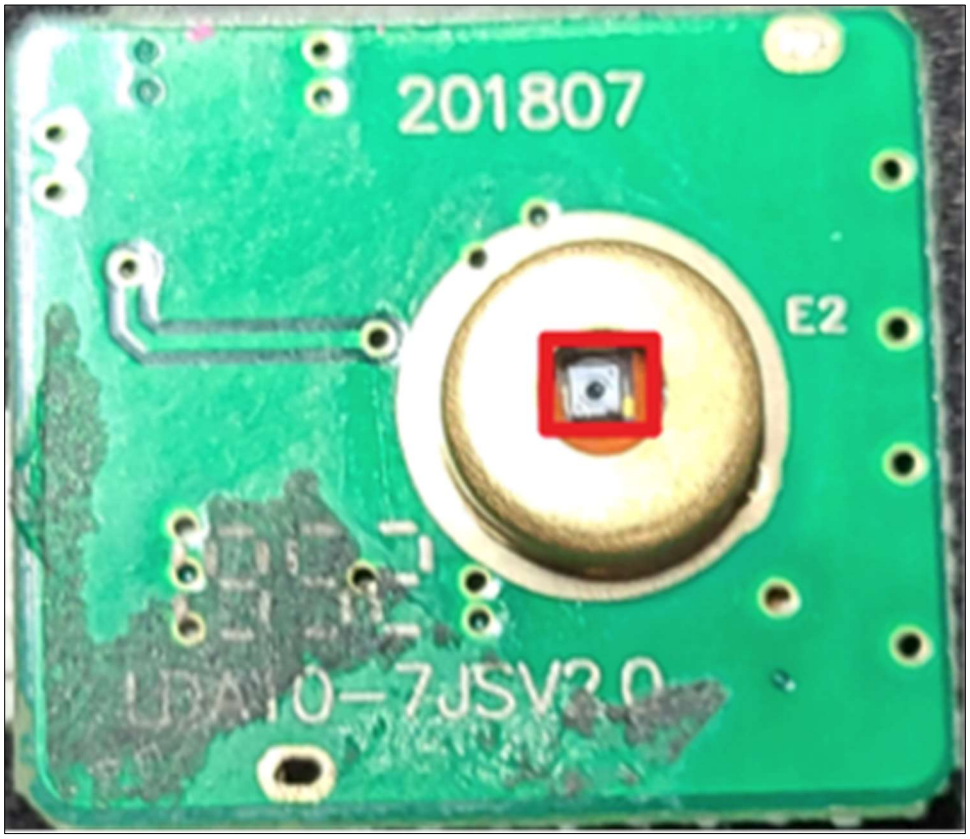
28. As just one non-limiting example, set forth below (with claim language in bold and italics) is exemplary evidence of infringement of Claim 7 of the '574 Patent in connection with the Accused Products. This description is based on publicly available information. Ranging Optics reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

29. ***7(a). A light receiving circuit of a laser range finder, said light receiving circuit comprising:***—Defendant made, used, sold, and/or offered to sell a device or system that is covered by the apparatus in accordance with Claim 7.

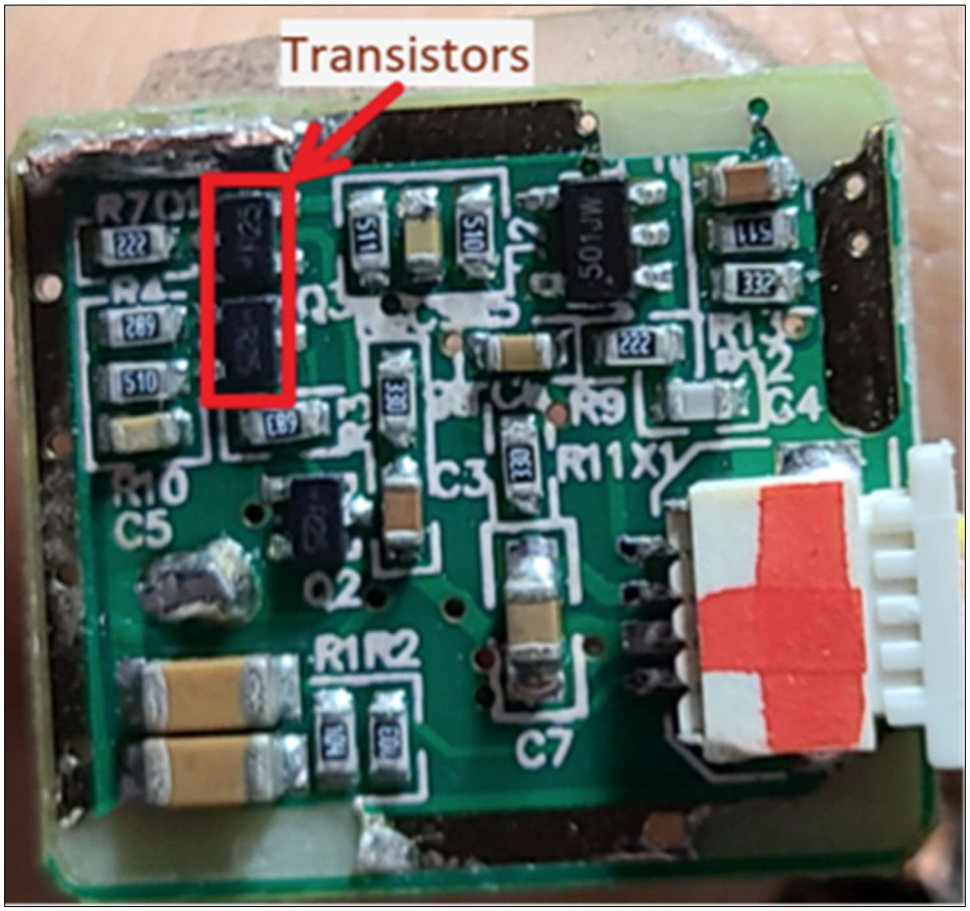
For instance, the Callaway 300 Pro Laser Rangefinder houses a light receiving circuit.



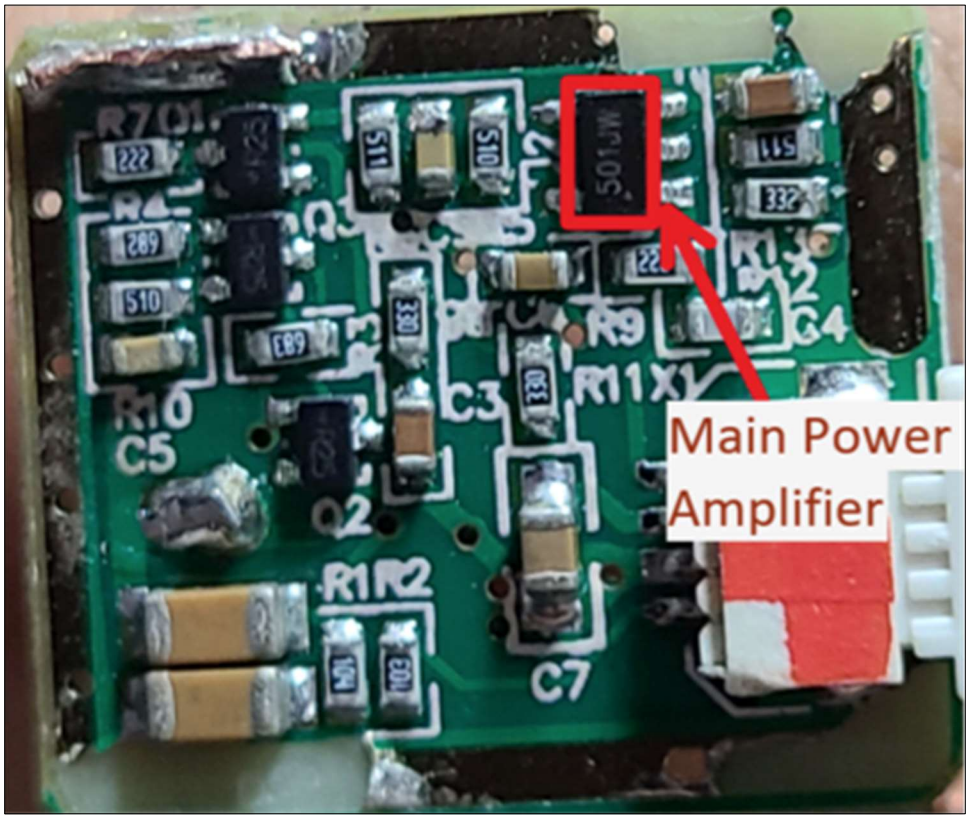
7(b): a photosensitive element for converting a light signal into a current signal;— Defendant makes, uses, sells, and/or offers to sell a device or system that includes a photosensitive element (APD – Avalance Photodiode).



7(c): a conversion amplifier connected with said photosensitive element for converting the current signal outputted from the photosensitive element into a voltage signal;— Defendant makes, uses, sells, and/or offers to sell a device or system that includes transistors that convert the current signal into a voltage signal.

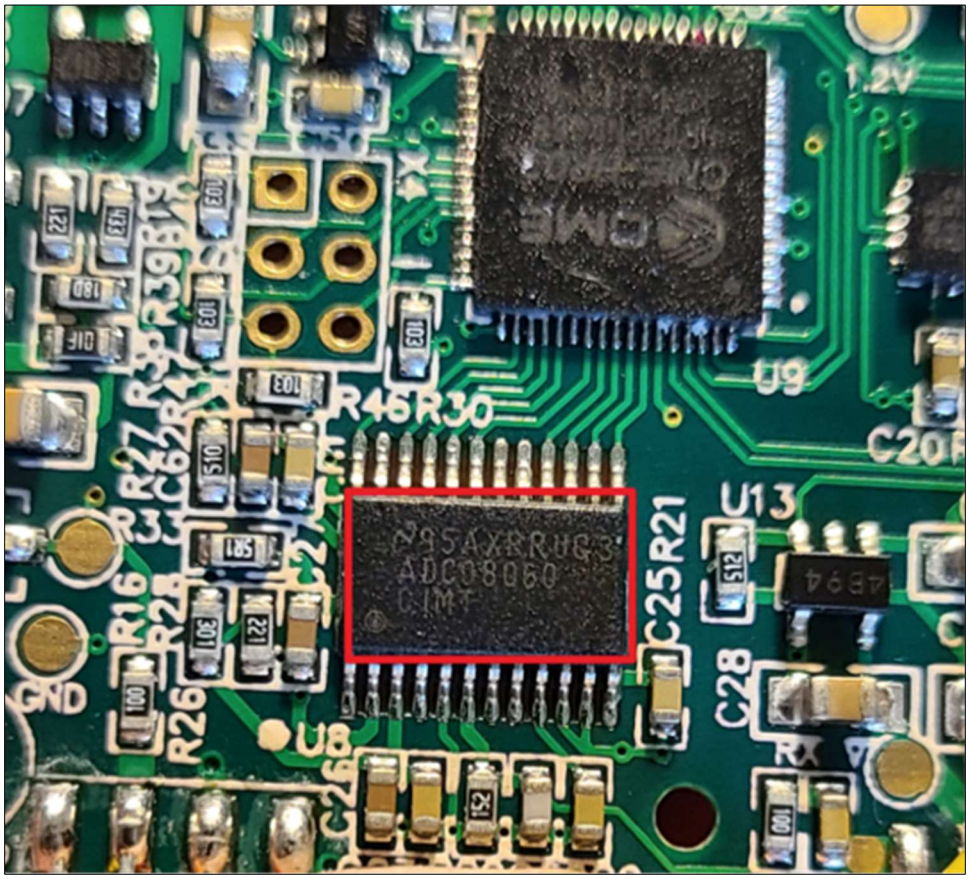


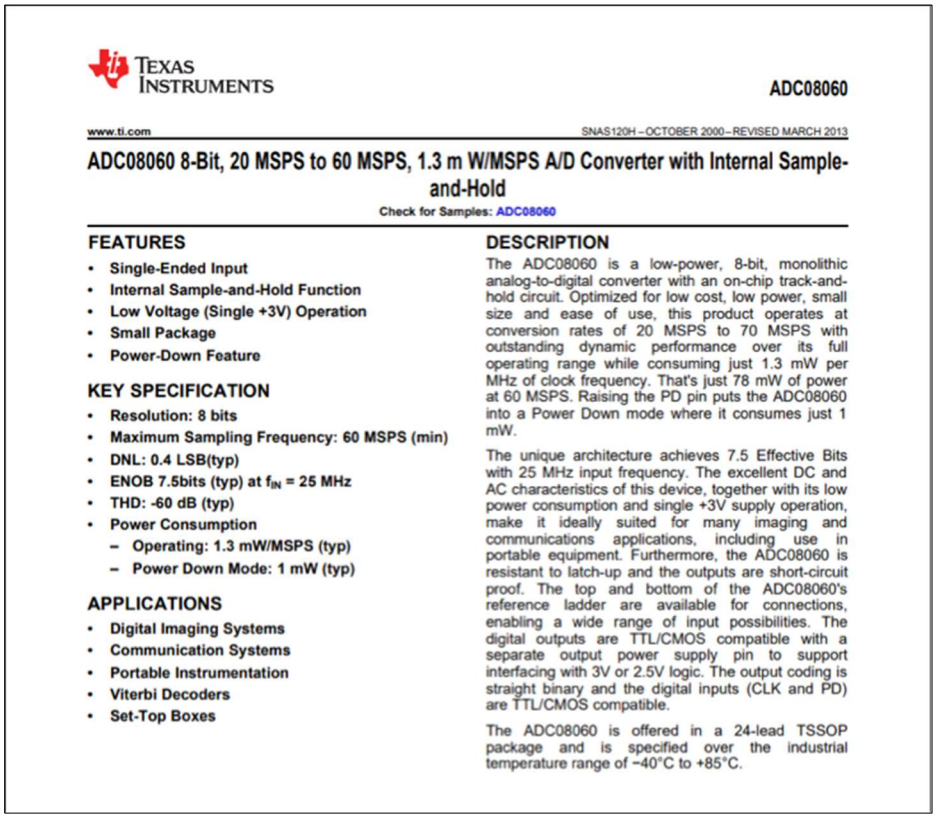
7(d): a main amplifier connected with the conversion amplifier for amplifying the output voltage signal from the conversion amplifier;— Defendant makes, uses, sells, and/or offers to sell a device or system that includes a main amplifier connected to the conversion amplifier.



The Main Amplifier amplifies the input voltage of an incoming signal.

7(e): a one-shot circuit connected with the main amplifier for shaping the output voltage signal from the main amplifier into a digital signal by which the range-finding computation is attained by the laser range finder;— Defendant makes, uses, sells, and/or offers to sell a device or system that includes a one-shot circuit which includes a comparator. The comparator utilizes the voltage signal from the main amplifier to generate a digital signal (e.g. compares the incoming voltage signal with a stable input signal to generate a digital output).


1.2V
U9
R46R30
C20
U13
C25R21
C28
R16
R26
U8
GND



TEXAS INSTRUMENTS

ADC08060

www.ti.com

SNAS120H – OCTOBER 2000 – REVISED MARCH 2013

ADC08060 8-Bit, 20 MSPS to 60 MSPS, 1.3 m W/MSPS A/D Converter with Internal Sample-and-Hold

Check for Samples: ADC08060

FEATURES

- Single-Ended Input
- Internal Sample-and-Hold Function
- Low Voltage (Single +3V) Operation
- Small Package
- Power-Down Feature

KEY SPECIFICATION

- Resolution: 8 bits
- Maximum Sampling Frequency: 60 MSPS (min)
- DNL: 0.4 LSB(typ)
- ENOB 7.5bits (typ) at f_{IN} = 25 MHz
- THD: -60 dB (typ)
- Power Consumption
  - Operating: 1.3 mW/MSPS (typ)
  - Power Down Mode: 1 mW (typ)

APPLICATIONS

- Digital Imaging Systems
- Communication Systems
- Portable Instrumentation
- Viterbi Decoders
- Set-Top Boxes

DESCRIPTION

The ADC08060 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 MSPS to 70 MSPS with outstanding dynamic performance over its full operating range while consuming just 1.3 mW per MHz of clock frequency. That's just 78 mW of power at 60 MSPS. Raising the PD pin puts the ADC08060 into a Power Down mode where it consumes just 1 mW.

The unique architecture achieves 7.5 Effective Bits with 25 MHz input frequency. The excellent DC and AC characteristics of this device, together with its low power consumption and single +3V supply operation, make it ideally suited for many imaging and communications applications, including use in portable equipment. Furthermore, the ADC08060 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08060's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The output coding is straight binary and the digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08060 is offered in a 24-lead TSSOP package and is specified over the industrial temperature range of −40°C to +85°C.

https://www.ti.com/lit/ds/symlink/adc08060.pdf

FUNCTIONAL DESCRIPTION

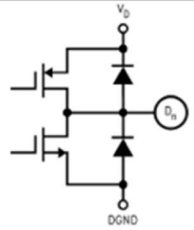
The ADC08060 uses a new, unique architecture that achieves over 7.4 effective bits at input frequencies up to 30 MHz.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Output format is straight binary. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RB} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08060 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

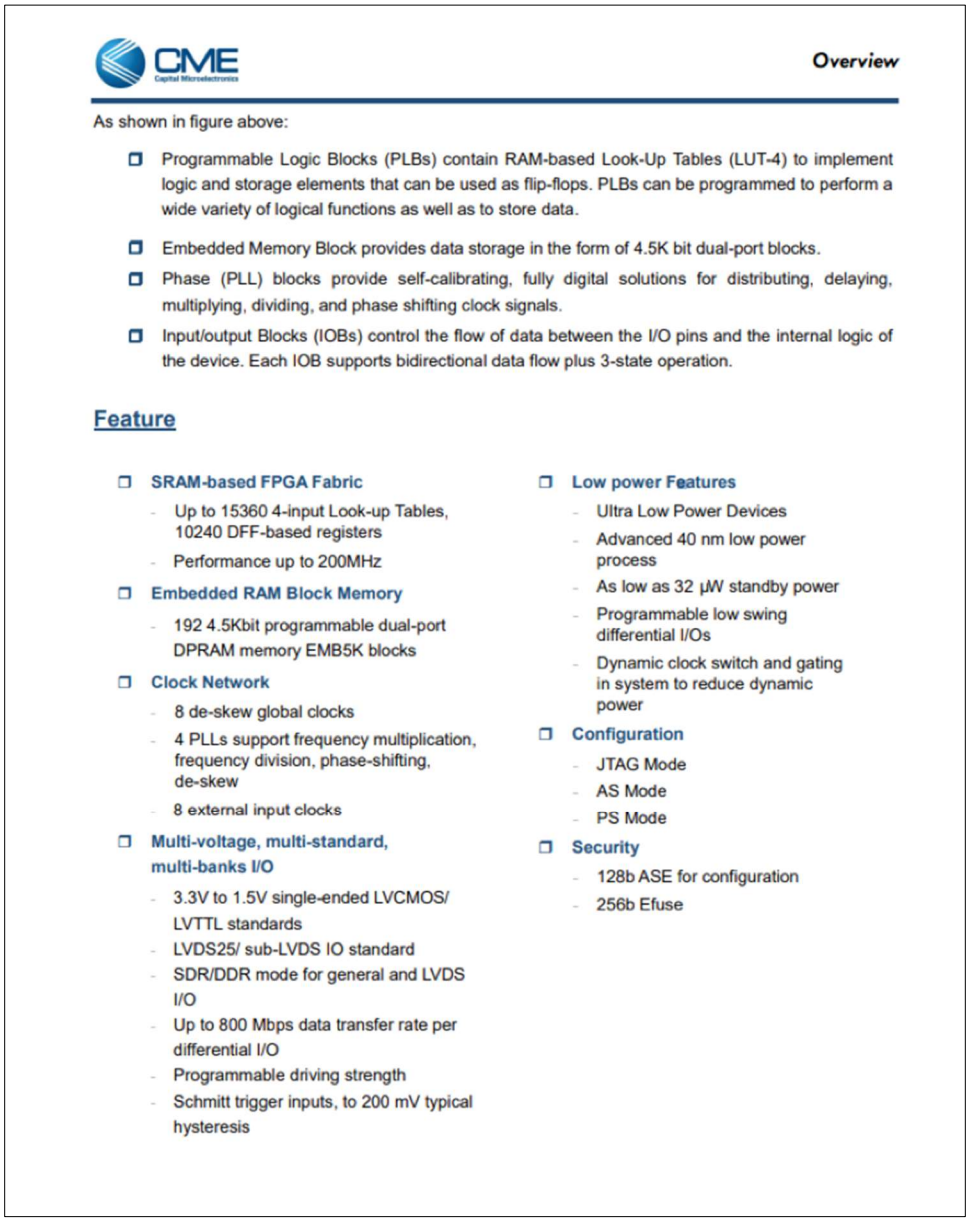
Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus t_{OD} later. The ADC08060 will convert as long as the clock signal is present. The output coding is straight binary.

The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes just 1 mW.

13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.

https://www.ti.com/lit/ds/symlink/adc08060.pdf

The digital signal is then sent to the logic chip (e.g. Capital Microelectronics HR03PN0Q68), which performs the range finding computation.



CME Capital Microelectronics

Overview

As shown in figure above:

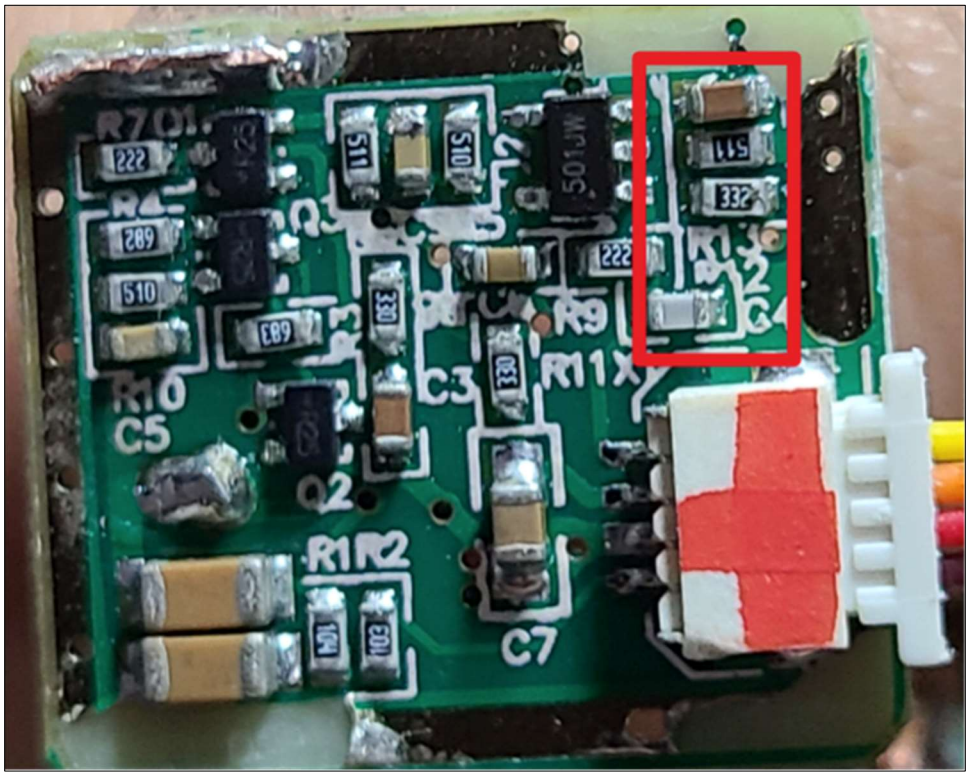
- Programmable Logic Blocks (PLBs) contain RAM-based Look-Up Tables (LUT-4) to implement logic and storage elements that can be used as flip-flops. PLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Embedded Memory Block provides data storage in the form of 4.5K bit dual-port blocks.
- Phase (PLL) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.
- Input/output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation.

Feature

- **SRAM-based FPGA Fabric**
  - Up to 15360 4-input Look-up Tables, 10240 DFF-based registers
  - Performance up to 200MHz
- **Embedded RAM Block Memory**
  - 192 4.5Kbit programmable dual-port DPRAM memory EMB5K blocks
- **Clock Network**
  - 8 de-skew global clocks
  - 4 PLLs support frequency multiplication, frequency division, phase-shifting, de-skew
  - 8 external input clocks
- **Multi-voltage, multi-standard, multi-banks I/O**
  - 3.3V to 1.5V single-ended LVCMOS/ LVTTL standards
  - LVDS25/ sub-LVDS IO standard
  - SDR/DDR mode for general and LVDS I/O
  - Up to 800 Mbps data transfer rate per differential I/O
  - Programmable driving strength
  - Schmitt trigger inputs, to 200 mV typical hysteresis
- **Low power Features**
  - Ultra Low Power Devices
  - Advanced 40 nm low power process
  - As low as 32 μW standby power
  - Programmable low swing differential I/Os
  - Dynamic clock switch and gating in system to reduce dynamic power
- **Configuration**
  - JTAG Mode
  - AS Mode
  - PS Mode
- **Security**
  - 128b ASE for configuration
  - 256b Efuse

7(f): wherein said main amplifier is a bias stabilized amplifier.. — Defendant makes, uses, sells, and/or offers to sell a device or system that includes the main amplifier as a bias stabilized

amplifier (e.g. The main amplifier is connected to a plurality of capacitors and resistors, which bias-stabilize the input current.)



30. Ranging Optics is in compliance with any applicable marking and/or notice provisions of 35 U.S.C. § 287 with respect to the '574 Patent.

31. Defendant has had notice of its infringement of the '574 Patent no later than October 26, 2020.

32. Ranging Optics is entitled to recover from Defendant all damages that Ranging Optics has sustained as a result of Defendant's infringement of the '574 Patent, including, without limitation, a reasonable royalty.

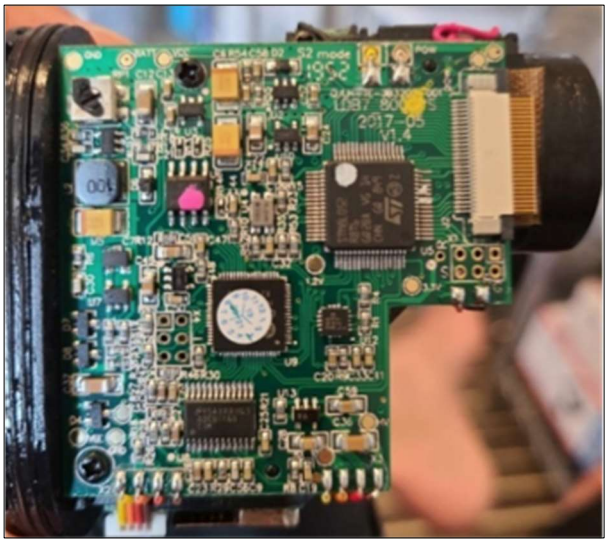
COUNT II: INFRINGEMENT OF U.S. PATENT NO. 7,443,927

33. Ranging Optics incorporates by reference and re-alleges paragraphs 19-25 of this Complaint as if fully set forth herein.

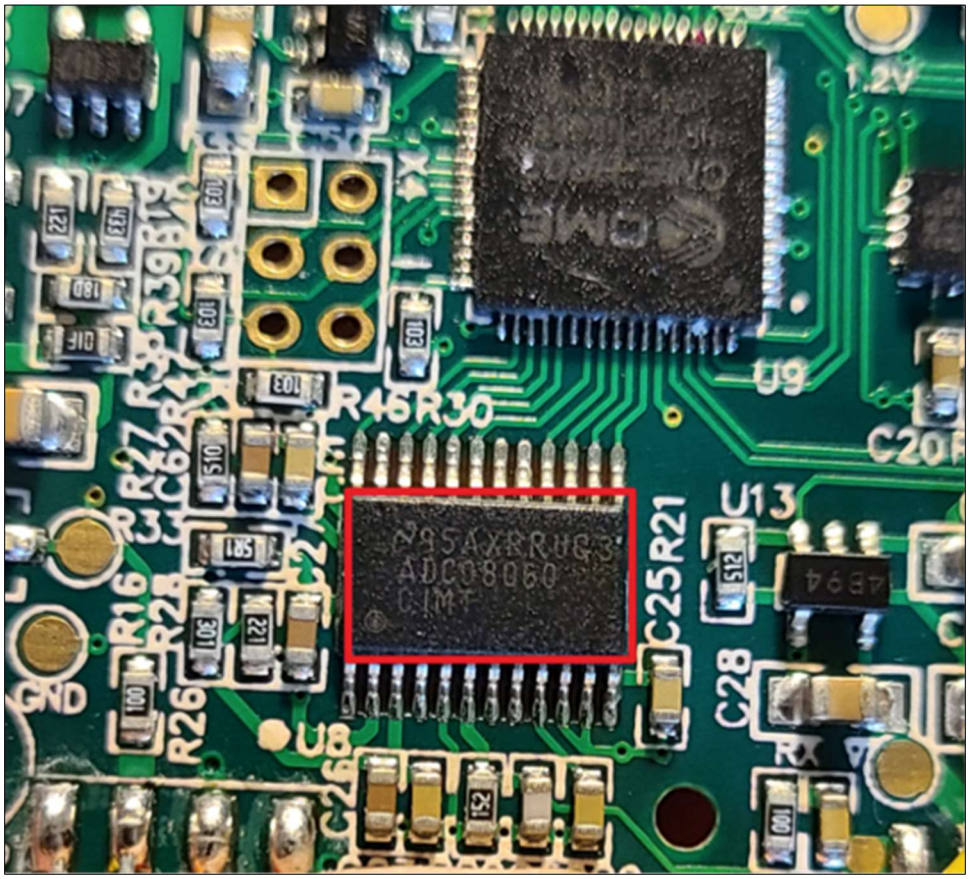
34. Defendant has infringed and is infringing, either literally or under the doctrine of equivalents, the '927 Patent in violation of 35 U.S.C. § 271 et seq., directly and/or indirectly, by making, using, offering for sale, or selling in the United States, and/or importing into the United States without authority or license the Accused Products.

35. As just one non-limiting example, set forth below (with claim language in bold and italics) is exemplary evidence of infringement of Claim 1 of the '927 Patent in connection with the Accused Products. This description is based on publicly available information. Ranging Optics reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

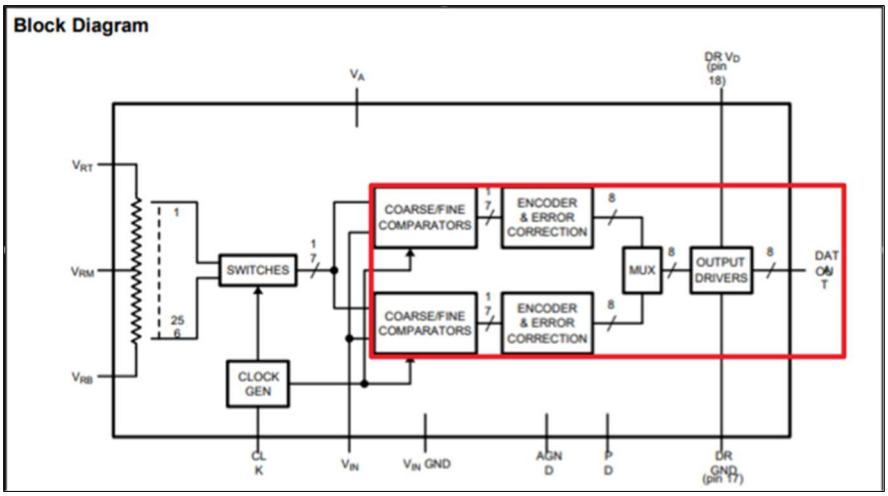
36. ***1(a): A signal detector, comprising:***—Defendant makes, uses, sells, and/or offers to sell a signal detector (e.g. the Accused Products detects an incoming light signal)



1(b): a signal translator converting differential data signals into a single data signal:— Defendant makes, uses, sells, and/or offers to sell a device or system that includes a signal translator (e.g. ADC08060 A/D Converter) operable to convert differential data signals into a signal data signal.



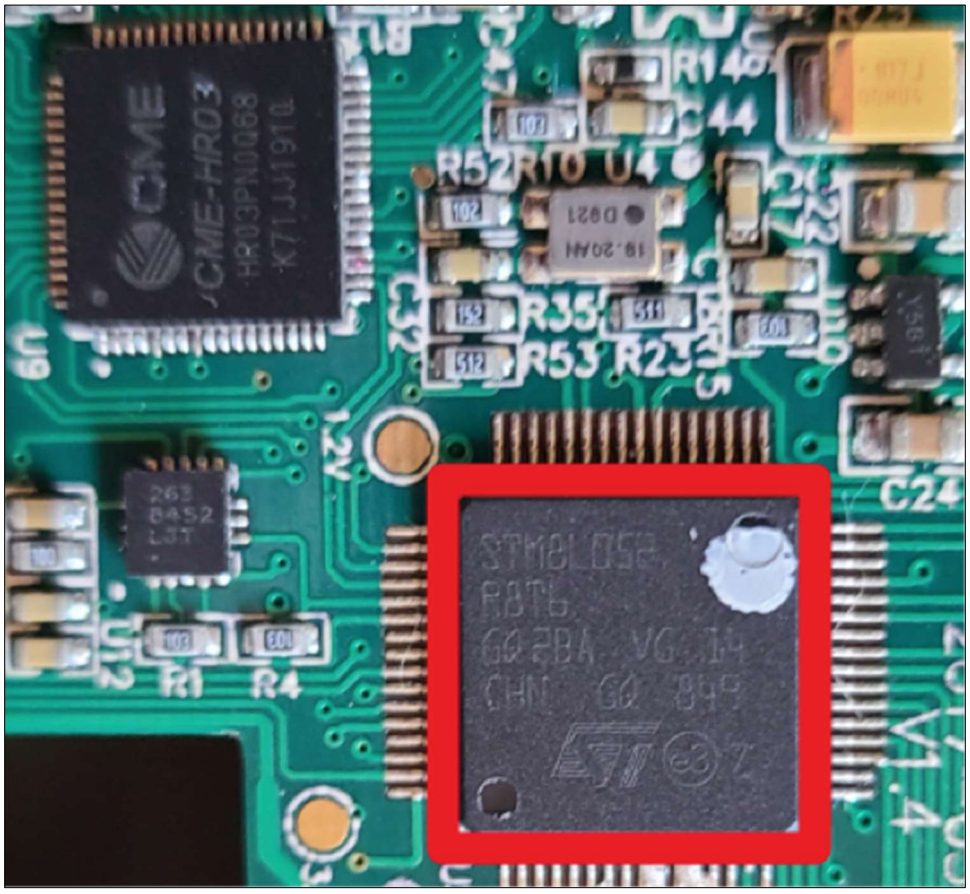
https://www.ti.com/lit/ds/symlink/adc08060.pdf



1(c): a data signal detector outputting a data detecting signal according to the single data signal; and:— Defendant makes, uses, sells, and/or offers to sell a device or system that includes

a data signal detector operable to output a data detecting signal (e.g. The Capital Microelectronics HR03PN0Q68, which outputs a high voltage signal) according to the single data signal (e.g. The A/D Converter output).

1(d): an interrupting control circuit receiving the data detecting signal and outputting a shutdown signal when the single data signal is at high voltage level over a predefined ratio:— Defendant makes, uses, sells, and/or offers to sell a device or system that includes an interrupting control circuit (e.g. STM32F103C8T6) for receiving the data detecting signal and outputting a shutdown signal according to the voltage of the data detecting signal.



The STM8L052R8T6 contains a reset routine, which outputs a shutdown signal when the input voltage the single data signal is at a high voltage over a predefined ratio.

life.augmented

STM8L052R8

Value Line, 8-bit ultralow power MCU, 64-KB Flash, 256-byte data EEPROM, RTC, LCD, timers, USART, I2C, SPI, ADC

Datasheet - production data

Features

- Operating conditions
  - Operating power supply: 1.8 V to 3.6 V
  - Temperature range: -40 °C to 85 °C
- Low power features
  - 5 low power modes: Wait, Low power run (5.9 µA), Low power wait (3 µA), Active-halt with full RTC (1.4 µA), Halt (400 nA)
  - Dynamic power consumption: 200 µA/MHz + 330 µA
  - Ultra-low leakage per I/O: 50 nA
  - Fast wakeup from Halt: 4.7 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq. 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low power, ultra-safe BOR reset with 5 programmable thresholds
  - Ultra low power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1 to 16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC
  - 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5ppm accuracy
  - Advanced anti-tamper detection
- LCD: 8x24 or 4x28 w/ step-up converter
- Memories
  - 64 KB Flash program memory and 256 bytes data EEPROM with ECC, RWW
  - Flexible write and read protection modes
  - 4 KB of RAM

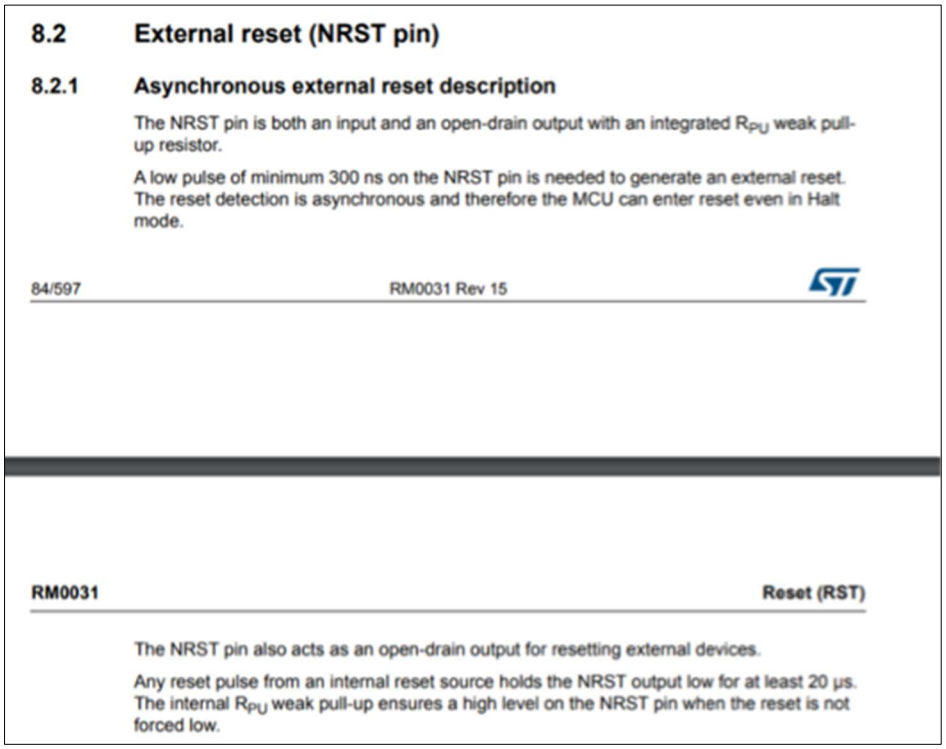
LQFP64

- DMA
  - 4 channels supporting ADC, SPIs, I2C, USARTs, timers
  - 1 channel for memory-to-memory
- 12-bit ADC up to 1 Msps/27 channels
  - Internal reference voltage
- Timers
  - Three 16-bit timers with 2 channels (used as IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with 3 channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - 2 watchdogs: 1 Window, 1 Independent
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Two synchronous serial interfaces (SPI)
  - Fast I2C 400 kHz SMBus and PMBus
  - Three USARTs (ISO 7816 interface + IrDA)
- Up to 54 I/Os, all mappable on interrupt vectors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART

3.2.2 Interrupt controller

The high density value line STM8L05xxx devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts



8.2 External reset (NRST pin)

8.2.1 Asynchronous external reset description

The NRST pin is both an input and an open-drain output with an integrated R_{PU} weak pull-up resistor.

A low pulse of minimum 300 ns on the NRST pin is needed to generate an external reset. The reset detection is asynchronous and therefore the MCU can enter reset even in Halt mode.

84/597 RM0031 Rev 15

RM0031 Reset (RST)

The NRST pin also acts as an open-drain output for resetting external devices.

Any reset pulse from an internal reset source holds the NRST output low for at least 20 µs. The internal R_{PU} weak pull-up ensures a high level on the NRST pin when the reset is not forced low.

https://www.st.com/resource/en/datasheet/stm8l052r8.pdf

37. Ranging Optics is in compliance with any applicable marking and/or notice provisions of 35 U.S.C. § 287 with respect to the ‘927 Patent.

38. Defendant has had notice of its infringement of the ’927 Patent no later than October 26, 2020.

39. Ranging Optics is entitled to recover from Defendant all damages that Ranging Optics has sustained as a result of Defendant’s infringement of the ‘927 Patent, including, without limitation, a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Ranging Optics respectfully requests:

A. That Judgment be entered that Defendant has infringed at least one or more claims of the Asserted Patents, directly and/or indirectly, literally and/or under the doctrine of equivalents;

B. An award of damages sufficient to compensate Ranging Optics for Defendant's infringement under 35 U.S.C. § 284;

C. That the case be found exceptional under 35 U.S.C. § 285 and that Ranging Optics be awarded its reasonable attorneys' fees;

D. Costs and expenses in this action;

E. An award of prejudgment and post-judgment interest; and

F. Such other and further relief as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Ranging Optics respectfully demands a trial by jury on all issues triable by jury.

Dated: May 17, 2021

Respectfully submitted,

/s/ Hao Ni
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hni@nilawfirm.com
Neal G. Massand
Texas Bar No. 24039038
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