UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC., Plaintiff, v. **HISENSE CO., LTD. and HISENSE VISUAL TECHNOLOGY CO., LTD. (F/K/A QINGDAO HISENSE ELECTRONICS CO., LTD. and HISENSE ELECTRIC CO., LTD.),** Defendants.	**Case No. 6:21-cv-00562** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff ParkerVision, Inc. ("ParkerVision"), by and through its undersigned counsel, files this Complaint against Defendants Hisense Co., Ltd. and Hisense Visual Technology Co., Ltd. (f/k/a Qingdao Hisense Electronics Co., Ltd. and Hisense Electric Co., Ltd.) (collectively, "Hisense" or "Defendants") for patent infringement of United States Patent Nos. 6,879,817 and 9,288,100 (collectively, the "patents-in-suit") and alleges as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*.

PARTIES

2. Plaintiff ParkerVision is a Florida corporation with its principal place of business at 4446-1A Hendricks Avenue, Suite 354, Jacksonville, Florida 32207.

3. Defendant Hisense Co., Ltd. is a foreign corporation duly organized and existing under the laws of the People's Republic of China, with a principal place of business at Hisense Tower, No. 17 Donghaixi Road, Qingdao, Shandong Province, 266071, P.R. China. Hisense Co., Ltd. is a parent corporation of Defendant Hisense Visual Technology Co., Ltd.

4. Defendant Hisense Visual Technology Co., Ltd. is a foreign corporation duly organized and existing under the laws of the People's Republic of China, with a principal place of business at No. 218, Qianwangang Road, Economic and Technological Development Zone, Qingdao, Shandong Province, 266555, P.R. China. Hisense Visual Technology Co., Ltd. formerly did business under the names Qingdao Hisense Electronics Co., Ltd. and Hisense Electric Co., Ltd.

5. On information and belief, Defendants act in concert to design, manufacture, sell, offer for sale, import, distribute, advertise, and/or otherwise promote the accused infringing products in the United States, the State of Texas, and this judicial district.

JURISDICTION AND VENUE

6. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*.

7. Hisense is subject to this Court's personal jurisdiction in accordance with due process and/or the Texas Long-Arm Statute. *See* Tex. Civ. Prac. & Rem. Code §§ 17.041 et seq.

8. This Court has personal jurisdiction over Hisense because Hisense has sufficient minimum contacts with this forum as a result of business conducted within the State of Texas and this judicial district. In particular, this Court has personal jurisdiction over Hisense because, inter alia, Hisense, on information and belief, has substantial, continuous, and systematic business contacts in this judicial district, and derives substantial revenue from goods provided to individuals in this judicial district.

9. Hisense has purposefully availed itself of the privileges of conducting business within this judicial district, has established sufficient minimum contacts with this judicial district such that it should reasonably and fairly anticipate being hauled into court in this judicial district, has purposefully directed activities at residents of this judicial district, and at least a portion of the patent infringement claims alleged in this Complaint arise out of or are related to one or more of the foregoing activities.

10. This Court has personal jurisdiction over Hisense because Hisense (directly and/or through its subsidiaries, affiliates, or intermediaries) has committed and continues to commit acts of infringement in this judicial district in violation of at least 35 U.S.C. § 271(a). In particular, on information and belief, Hisense uses, sells, offers for sale, imports, advertises, and/or otherwise promotes infringing products in the United States, the State of Texas, and this judicial district.

11. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b) – (d) and/or 1400(b). Hisense is registered to do business in the State of Texas, maintains a regular and established place of business within this judicial district, and has committed acts of infringement in this judicial district.

BACKGROUND

12. In 1989, Jeff Parker and David Sorrells started ParkerVision in Jacksonville, Florida. Through the mid-1990s, ParkerVision focused on developing commercial video cameras, e.g., for television broadcasts. The cameras used radio frequency (RF) technology to automatically track the camera's subject.

13. When developing consumer video cameras, however, ParkerVision, encountered a problem – the power and battery requirements for RF communications made a cost effective, consumer-sized product impractical. So, Mr. Sorrels and ParkerVision's engineering team began researching ways to solve this problem.

14. At the time, a decade's-old RF technology called super-heterodyne dominated the consumer products industry. But this technology was not without its own problems – the circuity was large and required significant power.

15. From 1995 through 1998, ParkerVision engineers developed an innovative method of RF direct conversion by a process of sampling a RF carrier signal and transferring energy to create a down-converted baseband signal.

16. After creating prototype chips and conducting tests, ParkerVision soon realized that its technology led to improved RF receiver performance, lower power

consumption, reduced size and integration benefits. In other words, RF receivers could be built smaller, cheaper and with greater improved performance.

17. ParkerVision's innovations did not stop there. ParkerVision went on to develop additional RF down-conversion technologies, RF up-conversion technologies and other related direct-conversion technologies. ParkerVision also developed complementary wireless communications technologies that involved interactions, processes, and controls between the baseband processor and the transceiver, which improved and enhanced the operation of transceivers that incorporate ParkerVision's down-converter and up-converter technologies. To date, ParkerVision has been granted over 200 patents related to its innovations, including the patents-in-suit.

18. ParkerVision's technology helped make today's wireless devices, such as televisions, a reality by enabling RF chips used in these devices to be smaller, cheaper, and more efficient, and with higher performance.

HISENSE

19. Hisense Co., Ltd. is a Chinese multinational electronics company headquartered in Qingdao, China. On information and belief, Hisense Visual Technology Co., Ltd. is a subsidiary of Hisense Co., Ltd.

20. On information and belief, since at least 2010, Hisense (or those acting on its behalf) has made, used, sold, offered for sale and/or imported televisions ("Hisense TVs") in/into the United States. https://www.warc.com/newsandopinion/news/hisense-targets-international-growth/26179.

21. On information and belief, from 2015 to 2019, Hisense entered into a brand licensing agreement with Sharp Electronics Corporation and/or Sharp Corporation through which Hisense sold Sharp-branded televisions ("Sharp TVs") in the United States. https://www.lifewire.com/hisense-now-has-sharp-assets-1847076. Hereinafter, Hisense TVs and Sharp TVs are collectively referred to as "Hisense Products."

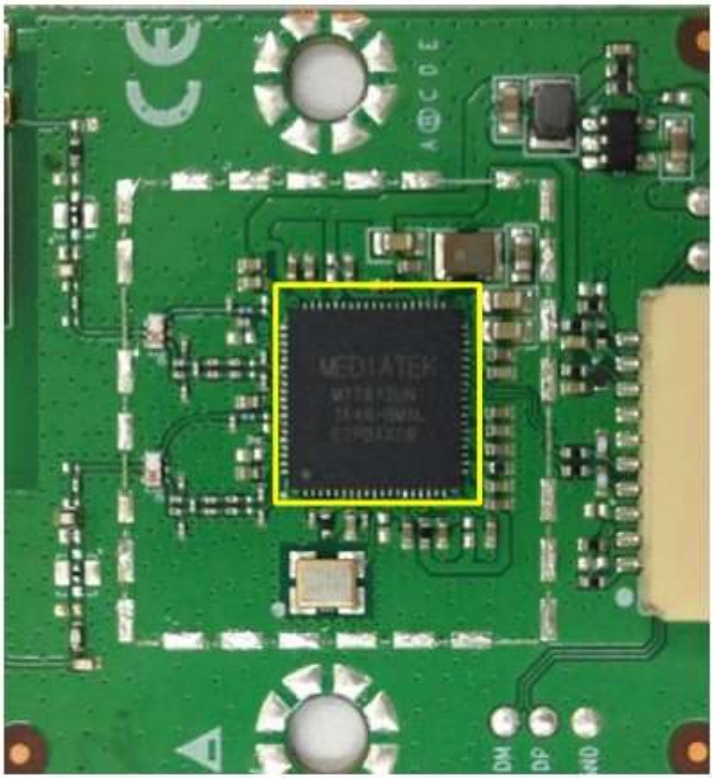
22. Hisense Products can be purchased through retailers throughout the United States including, without limitation, Best Buy, Target, Walmart, Costco, BJ Wholesale, B&H and PC Richards & Sons.

23. In 2019, Hisense was the fastest growing Top 6 TV brand in the United States by units and dollars. https://www.prnewswire.com/news-releases/hisense-unveils-a-full-lineup-of-uled-android-tvs-300847241.html.

24. Hisense Products include modules containing Wi-Fi chips including, without limitation, MediaTek MT7612UN and Realtek RTL8812BU (each a "Hisense Chip"; collectively, the "Hisense Chips"). Hisense Chips provide wireless connectivity for Hisense Products.

25. The image below shows the back panel of a Sharp-branded Hisense television (Model No. LC-55P6000U).

26. The back panel of the television includes an identification of the wireless module used in the television – FCC ID: 2AJVQZDGFMT7612U (shown in the red box above). On information and belief, the wireless product assigned FCC ID: 2AJVQ-ZDGFMT7612U is a Wi-Fi signal module containing MediaTek's MT7612UN chip (shown in the yellow box below).



https://fccid.io/2AJVQ-ZDGFMT7612U/Internal-Photos/Internal-Photos-3377285

27. On information and belief, Hisense Products also include modules (e.g., PPQ-WN4519L) containing Realtek Wi-Fi chips. On information and belief, the PPQWN4519L module includes a Realtek RTL8812BU chip.

https://fccid.io/PPQ-WN4519L/Internal-Photos/Internal-Photos-3283972

THE ASSERTED PATENTS

United States Patent No. 6,879,817

28. On April 12, 2005, the United States Patent and Trademark Office duly and legally issued United States Patent No. 6,879,817 ("the '817 patent") entitled "DC Offset, Re-Radiation, And I/Q Solutions Using Universal Frequency Translation Technology" to David F. Sorrells et al.

29. The '817 patent is presumed valid under 35 U.S.C. § 282.

30. ParkerVision owns all rights, title, and interest in the '817 patent.

United States Patent No. 9,288,100

31. On March 15, 2016, the United States Patent and Trademark Office duly and legally issued United States Patent No. 9,288,100 ("the '100 patent") entitled "Method and System for Down-Converting and Electromagnetic Signal" to David F. Sorrells et al.

32. The '100 patent is presumed valid under 35 U.S.C. § 282.

33. ParkerVision owns all rights, title, and interest in the '100 patent.

CLAIMS FOR RELIEF

COUNT I - Infringement of United States Patent No. 6,879,817

34. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

35. Hisense directly infringes (literally and/or under the doctrine of equivalents) the '817 patent by making, using, selling, offering for sale, and/or importing in/into the United States products covered by at least claims 1, 3, 5, 6, 7, 8, 9, 10, 11, 14, 17, 19, 20, 25, and 30 of the '817 patent.

36. Hisense products that infringe one or more claims of the '817 patent include, but are not limited to, the Hisense Products and any other Hisense device that is capable of down-converting an electromagnetic signal, as claimed in the '817 patent.

37. With respect to claim 1, each Hisense Chip is/includes an apparatus for down-converting an electromagnetic signal (e.g., high frequency radio frequency (RF) signal). Each Hisense Chip includes a first frequency down-conversion module that receives an input signal (e.g., high frequency RF signal), wherein the first frequency

down-conversion module down-converts the input signal according to a first control signal (e.g., local oscillator (LO) signal) and outputs a first down-converted signal.

38. Each Hisense Chip has a second frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the second frequency down-conversion module down-converts the input signal according to a second control signal (e.g., LO signal) and outputs a second down-converted signal.

39. Each Hisense Chip has a first subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the second down-converted signal from the first down-converted signal and outputs a first channel down-converted signal.

40. Each Hisense Chip has a third frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the third frequency down-conversion module down-converts the input signal according to a third control signal (e.g., LO signal) and outputs a third down-converted signal.

41. Each Hisense Chip has a fourth frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the fourth frequency down-conversion module down-converts the input signal according to a fourth control signal (e.g., LO signal) and outputs a fourth down-converted signal.

42. Each Hisense Chip has a second subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the fourth down-converted signal from the third down-converted signal and outputs a second channel down-converted signal.

43. Each Hisense Chip is/includes an apparatus wherein the input signal comprises an I/Q modulated signal, wherein the first channel down-converted signal comprises an I-phase information signal portion of the I/Q modulated signal, and wherein the second channel down-converted signal comprises a Q-phase information signal portion of the I/Q modulated signal.

44. Each Hisense Chip is/includes an apparatus wherein the first frequency down-conversion module under-samples the input signal according to the first control signal, and the second frequency down-conversion module under-samples the input signal according to the second control signal.

45. With respect to claim 3, each Hisense Chip is/includes an apparatus wherein the first and second channel down-converted signals are baseband signals.

46. With respect to claim 5, each Hisense Chip is/includes an apparatus wherein the first control signal (e.g., LO signal) comprises a first control pulse and the second control signal (e.g., LO signal) comprises a second control pulse, wherein the second control signal pulse is delayed relative to the first control signal pulse by 0.5+n cycles of the input signal (e.g., high frequency RF signal), wherein n is an integer.

47. With respect to claim 6, each Hisense Chip is/includes an apparatus wherein the first subtractor comprises a differential amplifier.

48. With respect to claim 7, each Hisense Chip is/includes an apparatus wherein the first subtractor and the second subtractor each comprises a differential amplifier.

49. With respect to claim 8, each Hisense Chip is/includes an apparatus further comprising: a first filter that filters the first down-converted signal; a second filter that filters the second down-converted signal; a third filter that filters the third down-converted signal; and a fourth filter that filters the fourth down-converted signal.

50. With respect to claim 9, each Hisense Chip is/includes an apparatus wherein the first, second, third, and fourth filters each comprise a low-pass filter.

51. With respect to claim 10, each Hisense Chip is/includes an apparatus wherein the low-pass filter comprises a resistor and a capacitor.

52. With respect to claim 11, each Hisense Chip is/includes an apparatus further comprising a low-noise amplifier (LNA) that amplifies the input signal (e.g., high frequency RF signal).

53. With respect to claim 14, each Hisense Chip is/includes an apparatus, further comprising at least one control signal generator (e.g., LO and/or LO circuitry) that outputs the first, the second, the third, and the fourth control signal (e.g., LO signals)

54. With respect to claim 17, each Hisense Chip is/includes an apparatus for down-converting an electromagnetic signal, comprising: a first frequency down-conversion module that receives an input signal (e.g., high frequency RF signal), wherein the first frequency down-conversion module down-converts the input signal according to a first control signal (e.g., LO signal) and outputs a first down-converted signal.

55. Each Hisense Chip has a second frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the second frequency down-conversion module down-converts the input signal according to a second control signal (e.g., LO signal) and outputs a second down-converted signal.

56. Each Hisense Chip has a subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the second down-converted signal from the first down-converted signal and outputs a first channel down-converted signal.

57. Each Hisense Chip has a third frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the third frequency down-conversion module down-converts the input signal according to a third control signal (e.g., LO signal) and outputs a third down-converted signal.

58. Each Hisense Chip has a fourth frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the fourth frequency down-conversion module down-converts the input signal according to a fourth control signal (e.g., LO signal) and outputs a fourth down-converted signal.

59. Each Hisense Chip has a second subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the fourth down-converted signal from the third down-converted signal and outputs a second channel down-converted signal.

60. Each Hisense Chip is/includes an apparatus wherein the input signal (e.g., high frequency RF signal) comprises an I/Q modulated signal, wherein the first

channel down-converted signal comprises an I-phase information signal portion of the I/Q modulated signal, and wherein the second channel down-converted signal comprises a Q-phase information signal portion of the I/Q modulated signal.

61. Each Hisense Chip is/includes an apparatus wherein a second control signal pulse of the second control signal (e.g., LO signal) occurs 1.5 cycles of a frequency of the input signal (e.g., high frequency RF signal) after the occurrence of a first control signal pulse of the first control signal (e.g., LO signal), wherein a fourth control signal pulse of the fourth control signal (e.g., LO signal) occurs 1.5 cycles of the frequency of the input signal (e.g., high frequency RF signal) after the occurrence of a third control signal pulse of the fourth control signal (e.g., LO signal); and wherein the third control signal pulse occurs 0.75 cycles of the frequency of the input signal (e.g., high frequency RF signal) after the occurrence of the first control signal pulse.

62. With respect to claim 19, each Hisense Chip is/includes an apparatus down-converting an electromagnetic signal (e.g., high frequency RF signal). Each Hisense Chip includes a first frequency down-conversion module that receives an input signal (e.g., high frequency RF signal), wherein the first frequency down-conversion module down-converts the input signal according to a first control signal (e.g., LO signal) and outputs a first down-converted signal.

63. Each Hisense Chip has a second frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the second frequency down-conversion module down-converts the input signal according to a second control signal (e.g., LO signal) and outputs a second down-converted signal.

64. Each Hisense Chip has a first subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the second down-converted signal from the first down-converted signal and outputs a first channel down-converted signal.

65. Each Hisense Chip has a third frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the third frequency down-conversion module down-converts the input signal according to a third control signal (e.g., LO signal) and outputs a third down-converted signal.

66. Each Hisense Chip has a fourth frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the fourth frequency down-conversion module down-converts the input signal according to a fourth control signal (e.g., LO signal) and outputs a fourth down-converted signal.

67. Each Hisense Chip has a second subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the fourth down-converted signal from the third down-converted signal and outputs a second channel down-converted signal.

68. Each Hisense Chip is/includes an apparatus wherein the first frequency down-conversion module samples the input signal (e.g., high frequency RF signal) according to the first control signal (e.g., LO signal), the second frequency down-conversion module samples the input signal according to the second control signal (e.g., LO signal), the third frequency down-conversion module samples the input signal according to the third control signal (e.g., LO signal), and the fourth frequency down-

conversion module samples the input signal according to the fourth control signal (e.g., LO signal).

69. With respect to claim 20, each Hisense Chip is/includes an apparatus wherein the input signal (e.g., high frequency RF signal) comprises an I/Q modulated signal.

70. With respect to claim 25, each Hisense Chip is/includes an apparatus wherein the first, the second, the third, and the fourth frequency down-conversion modules each comprise a switch and a storage element, wherein a first node of the storage element is coupled to a node of the switch, and a second node of the storage element is coupled to a reference potential (e.g., ground).

71. With respect to claim 30, each Hisense Chip is/includes an apparatus for down-converting an electromagnetic signal (e.g., high frequency RF signal). Each Hisense Chip includes a first frequency down-conversion module that receives an input signal (e.g., high frequency RF signal), wherein the first frequency down-conversion module down-converts the input signal according to a first control signal (e.g., LO signal) and outputs a first down-converted signal.

72. Each Hisense Chip has a second frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the second frequency down-conversion module down-converts the input signal according to a second control signal (e.g., LO signal) and outputs a second down-converted signal.

73. Each Hisense Chip has a first subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the second down-

converted signal from the first down-converted signal and outputs a first channel down-converted signal.

74. Each Hisense Chip has a third frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the third frequency down-conversion module down-converts the input signal according to a third control signal (e.g., LO signal) and outputs a third down-converted signal.

75. Each Hisense Chip has a fourth frequency down-conversion module that receives the input signal (e.g., high frequency RF signal), wherein the fourth frequency down-conversion module down-converts the input signal according to a fourth control signal (e.g., LO signal) and outputs a fourth down-converted signal.

76. Each Hisense Chip has a second subtractor module (e.g., differential amplifier with parallel resistor-capacitor feedback) that subtracts the fourth down-converted signal from the third down-converted signal and outputs a second channel down-converted signal.

77. Each Hisense Chip has a control signal generator, wherein the control signal generator comprises: a local oscillator; a 180 degree phase shifter coupled to an output of the local oscillator; a first divide-by-two module coupled to the output of the local oscillator; a second divide-by-two module coupled to an output of the 180 degree phase shifter; a first pulse generator coupled to an output of the first divide-by-two module, wherein the first pulse generator outputs the first control signal (e.g., LO signal); a second pulse generator coupled to an inverting output of the first divide-by-two module, wherein the second pulse generator outputs the second control signal (e.g.,

LO signal); a third pulse generator coupled to an output of the second divide-by-two module, wherein the third pulse generator outputs the third control signal (e.g., LO signal); and a fourth pulse generator coupled to an inverting output of the second divide-by-two module, wherein the fourth pulse generator outputs the fourth control signal (e.g., LO signal).

78. ParkerVision has been damaged by the direct infringement of Hisense and is suffering and will continue to suffer irreparable harm and damages as a result of this infringement.

COUNT II - Infringement of United States Patent No. 9,288,100

79. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

80. Hisense directly infringes (literally and/or under the doctrine of equivalents) the '100 patent by making, using, selling, offering for sale, and/or importing in/into the United States products covered by at least claims 1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 19, 20, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, and 32 of the '100 patent.

81. Hisense products that infringe one or more claims of the '100 patent include, but are not limited to, the Hisense Products and any other Hisense device that is capable of down-converting an electromagnetic signal, as claimed in the '100 patent.

82. With respect to claim 1, each Hisense Chip is/includes a system for frequency down-converting a modulated carrier signal (e.g., high frequency RF signal) to a demodulated baseband signal, comprising: a first switch (e.g., transistor(s)) that

receives a first portion of energy from the modulated carrier signal during a sampling aperture with a specified frequency of a first control signal (e.g., LO signal) that controls when the first switch is on and when the first switch is off.

83. Each Hisense Chip has a first storage device (e.g., capacitor(s)) which stores the first portion of energy from the modulated carrier signal (e.g., high frequency RF signal) output by the first switch (e.g., transistor(s)) when the switch is on the first storage device having previously accumulated energy from the modulated carrier signal as a first accumulation of energy, the first portion of energy being added to the first accumulation of energy to result in a second accumulation of energy, discharges at least some of the second accumulation of energy when the first switch is off so as to leave a third accumulation of energy stored at the first storage device, and outputs a down-converted in-phase baseband signal portion of the modulated carrier signal derived from the energy stored at the first storage device both while the first switch is on and while the first switch is off.

84. Each Hisense Chip has a second switch (e.g., transistor(s)) that receives a second portion of energy from the modulated carrier signal (e.g., high frequency RF signal) during a sampling aperture with a specified frequency of a second control signal (e.g., LO signal) that controls when the second switch is on and when the second switch is off.

85. Each Hisense Chip has a second storage device (e.g., capacitor(s)) which stores the second portion of energy from the modulated carrier signal (e.g., high frequency RF signal) output by the second switch (e.g., transistor(s)) when the second

switch is on, the second storage device having previously accumulated energy from the modulated carrier signal as a fourth accumulation of energy, the second portion of energy being added to the fourth accumulation of energy to result in a fifth accumulation of energy, discharges at least some of the fifth accumulation of energy when the second switch is off so as to leave a sixth accumulation of energy stored at the second storage device, and outputs a down-converted inverted in-phase baseband signal portion of the modulated carrier signal derived from the energy stored at the second storage device both while the second switch is on and while the second switch is off.

86. Each Hisense Chip is/includes a system wherein the down-converted in-phase baseband signal portion is generated from both the second accumulation of energy and the third accumulation of energy, and wherein the down-converted inverted in-phase baseband signal portion is generated from both the fifth accumulation of energy and the sixth accumulation of energy.

87. Each Hisense Chip has a first differential amplifier circuit (e.g., differential amplifier with parallel resistor-capacitor feedback) that combines the down-converted in-phase baseband signal portion with the down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.

88. With respect to claim 2, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes an amplitude variation.

89. With respect to claim 3, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes a phase variation.

90. With respect to claim 4, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes a combination of amplitude variation and phase variation.

91. With respect to claim 5, each Hisense Chip is/includes a system wherein the sampling aperture of the first control signal (e.g., LO signal) transfers energy for at least one-tenth of a cycle of the modulated carrier signal (e.g., high frequency RF signal) and no more than a half cycle of the modulated carrier signal.

92. With respect to claim 7, each Hisense Chip is/includes a system wherein the sampling apertures of the first and second control signals (e.g., LO signals) are defined by a windowing function u(t)−u(t−TA), where a length of a windowing function aperture is TA, which is at least one-tenth of a cycle of the modulated carrier signal (e.g., high frequency RF signal) and no more than a half cycle of the modulated carrier signal.

93. With respect to claim 8, each Hisense Chip is/includes a system wherein for each respective storage device (e.g., capacitor(s)), the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for a next charging cycle that begins immediately following the given discharge cycle.

94. With respect to claim 10, each Hisense Chip is/includes a system further comprising: a first filter that filters the down-converted in-phase baseband signal

portion; and a second filter that filters the down-converted inverted in-phase baseband signal portion.

95. With respect to claim 11, each Hisense Chip is/includes a system wherein the first and second filters each comprise a low-pass filter.

96. With respect to claim 12, each Hisense Chip is/includes a system wherein the first and second storage devices (e.g., capacitor(s)) are capacitive storage circuits.

97. With respect to claim 13, each Hisense Chip is/includes a system further comprising: a third switch (e.g., transistor(s)) that receives a third portion of energy from the modulated carrier signal (e.g., high frequency RF signal) during a sampling aperture with a specified frequency of a third control signal (e.g., LO signal) that controls when the third switch is on and when the third switch is off.

98. Each Hisense Chip has a third storage device (e.g., capacitor(s)) which stores the third portion of energy from the modulated carrier signal (e.g., high frequency RF signal) output by the third switch (e.g., transistor(s)) when the third switch is on, the third storage device having previously accumulated energy from the carrier signal as a seventh accumulation of energy, the third portion of energy being added to the seventh accumulation of energy to result in an eighth accumulation of energy, discharges at least some of the eighth accumulation of energy when the third switch is off so as to leave a ninth accumulation of energy stored at the third storage device, and outputs a down-converted quadrature-phase baseband signal portion of the modulated carrier signal derived from the energy stored at the third storage device both while the third switch is on and while the third switch is off.

99. Each Hisense Chip has a fourth switch (e.g., transistor(s)) that receives a fourth portion of energy from the modulated carrier signal (e.g., high frequency RF signal) during a sampling aperture with a specified frequency of a fourth control signal (e.g., LO signal) that controls when the fourth switch is on and when the fourth switch is off.

100. Each Hisense Chip has a fourth storage device (e.g., capacitor(s)) that stores the fourth portion of energy from the modulated carrier signal (e.g., high frequency RF signal) output by the fourth switch (e.g., transistor(s)) when the fourth switch is on, the fourth storage device having previously accumulated energy from the carrier signal as a tenth accumulation of energy, the fourth portion of energy being added to the tenth accumulation of energy to result in an eleventh accumulation of energy, discharges at least some of the eleventh accumulation of energy when the fourth switch is off so as to leave a twelfth accumulation of energy stored at the fourth storage device, and outputs a down-converted inverted quadrature-phase baseband signal portion of the modulated carrier signal derived from the energy stored at the fourth storage device both while the fourth switch is on and while the fourth switch is off.

101. Each Hisense Chip is/includes a system wherein the down-converted quadrature-phase baseband signal portion is generated from both the eighth accumulation of energy and the ninth accumulation of energy, and wherein the down-converted inverted quadrature-phase baseband signal portion is generated from both the eleventh accumulation of energy and the twelfth accumulation of energy.

102. Each Hisense Chip has a second differential amplifier circuit (e.g., differential amplifier with parallel resistor-capacitor feedback) that combines the down-converted quadrature-phase baseband signal portion with the down-converted inverted quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.

103. With respect to claim 14, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes an amplitude variation.

104. With respect to claim 15, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes a phase variation.

105. With respect to claim 16, each Hisense Chip is/includes a system wherein the modulated carrier signal (e.g., high frequency RF signal) includes a combination of amplitude variation and phase variation.

106. With respect to claim 17, each Hisense Chip is/includes a system wherein the sampling aperture of the third control signal (e.g., LO signal) transfers energy for at least one-tenth of a cycle of the modulated carrier signal (e.g., high frequency RF signal) and no more than a half cycle of the modulated carrier signal.

107. With respect to claim 19, each Hisense Chip is/includes a system wherein the sampling apertures of the third and fourth control signals (e.g., LO signals) are defined by a windowing function u(t)−u(t−TA), where a length of a windowing function aperture is TA, which is at least one-tenth of a cycle of the modulated carrier

signal (e.g., high frequency RF signal) and no more than a half cycle of the modulated carrier signal.

108. With respect to claim 20, each Hisense Chip is/includes a system wherein for each respective third and fourth storage device (e.g., capacitor(s)), the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for a next charging cycle that begins immediately following the given discharge cycle.

109. With respect to claim 22, each Hisense Chip is/includes a system further comprising: a first filter that filters the down-converted in-phase baseband signal portion; a second filter that filters the down-converted inverted in-phase baseband signal portion; a third filter that filters the down-converted quadrature-phase baseband signal portion; and a fourth filter that filters the down-converted inverted quadrature-phase baseband signal portion.

110. With respect to claim 23, each Hisense Chip is/includes a system wherein the first, second, third, and fourth filters each comprise a low-pass filter.

111. With respect to claim 24, each Hisense Chip is/includes a system wherein the first, second, third and fourth storage devices (e.g., capacitor(s)) are capacitive storage circuits.

112. With respect to claim 25, each Hisense Chip is/includes a system wherein the first, second, third, and fourth switch (e.g., transistor(s)); the first, second, third, and fourth storage device (e.g., capacitor(s)); and the first and second differential amplifier

circuit (e.g., differential amplifiers with parallel resistor-capacitor feedback) are implemented in an integrated circuit.

113. With respect to claim 26, each Hisense Chip is/includes a system wherein the first control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the first switch (e.g., transistor(s)) is on or off, wherein the second control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the second switch (e.g., transistor(s)) is on or off, wherein the third control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the third switch (e.g., transistor(s)) is on or off, and wherein the fourth control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the fourth switch (e.g., transistor(s)) is on or off.

114. With respect to claim 27, each Hisense Chip is/includes a system wherein the pulses operate at a rate that is substantially equal to the frequency of the modulated carrier signal (e.g., high frequency RF signal) or to a subharmonic thereof.

115. With respect to claim 28, each Hisense Chip is/includes a system wherein the first storage device (e.g., capacitor(s)) is coupled to a first load (e.g., low impedance load), wherein the second storage device (e.g., capacitor(s)) is coupled to a second load (e.g., low impedance load), wherein the third storage device (e.g., capacitor(s)) is coupled to a third load (e.g., low impedance load), wherein the fourth storage device (e.g., capacitor(s)) is coupled to a fourth load (e.g., low impedance load), wherein the at least some of the second accumulation of energy discharged when the first switch (e.g., transistors(s)) is off is discharged into the first load, wherein the at least some of the

fifth accumulation of energy discharged when the second switch (e.g., transistors(s)) is off is discharged into the second load, wherein the at least some of the eighth accumulation of energy discharged when the third switch (e.g., transistors(s)) is off is discharged into the third load, and wherein the at least some of the eleventh accumulation of energy discharged when the fourth switch (e.g., transistors(s)) is off is discharged into the fourth load.

116. With respect to claim 29, each Hisense Chip is/includes a system wherein the first and second switch (e.g., transistor(s)), the first and second storage device (e.g., capacitor(s)), and the first differential amplifier circuit (e.g., differential amplifier with parallel resistor-capacitor feedback) are implemented in an integrated circuit.

117. With respect to claim 30, each Hisense Chip is/includes a system wherein the first control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the first switch (e.g., transistor(s)) is on or off and wherein the second control signal (e.g., LO signal) comprises a train of substantially non-sinusoidal pulses to control when the second switch (e.g., transistor(s)) is on or off.

118. With respect to claim 31, each Hisense Chip is/includes a system wherein the pulses operate at a rate that is substantially equal to the frequency of the modulated carrier signal (e.g., high frequency RF signal) or to a subharmonic thereof.

119. With respect to claim 32, each Hisense Chip is/includes a system wherein the first storage device (e.g., capacitor(s)) is coupled to a first load (e.g., low impedance load), wherein the second storage device (e.g., capacitor(s)) is coupled to a second load (e.g., low impedance load), wherein said at least some of the second accumulation of

energy discharged when the first switch (e.g., transistor(s)) is off is discharged into the first load, and wherein the at least some of the fifth accumulation of energy discharged when the second switch (e.g., transistor(s)) is off is discharged into the second load.

120. ParkerVision has been damaged by the direct infringement of Hisense, and is suffering and will continue to suffer irreparable harm and damages as a result of this infringement.

JURY DEMANDED

121. Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, ParkerVision hereby requests a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, ParkerVision respectfully requests that the Court enter judgment in its favor and against Hisense as follows:

a. finding that Hisense directly infringes one or more claims of each of the patents-in-suit;

b. awarding ParkerVision damages under 35 U.S.C. § 284, or otherwise permitted by law, including supplemental damages for any continued post-verdict infringement;

c. awarding ParkerVision pre-judgment and post-judgment interest on the damages award and costs;

d. awarding cost of this action (including all disbursements) and attorney fees pursuant to 35 U.S.C. § 285, or as otherwise permitted by the law; and

e. awarding such other costs and further relief that the Court determines to be just and equitable.

Dated: June 2, 2021

Respectfully submitted,

/s/Raymond W. Mort, III

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**Pro hac vice to be filed*
 # Not admitted to practice in Virginia