IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

FORUTOME IP LLC, Plaintiff, v. **LATTICE SEMICONDUCTOR CORPORATION**, Defendant.	C.A. No. 1:21-cv-426-RGA **JURY TRIAL DEMANDED** **PATENT CASE**

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Forutome IP LLC files this First Amended Complaint for Patent Infringement against Lattice Semiconductor Corporation pursuant to Rule 15(a)(1)(B), Fed.R.Civ.P., and would respectfully show the Court as follows:

I. THE PARTIES

1. Plaintiff Forutome IP LLC ("Forutome" or "Plaintiff") is a Texas limited liability company having an address at 6009 W Parker Rd, Ste 149 – 1092, Plano, TX 75093-8121.

2. On information and belief, Defendant Lattice Semiconductor Corporation ("Defendant") is a corporation organized and existing under the laws of Delaware. Defendant has a registered agent at Corporation Service Company, 251 Little Falls Dr., Wilmington, DE 19808.

II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the Delaware Long-Arm Statute, due at least to its business in this forum, including at least a portion of the infringements alleged herein.

Furthermore, Defendant is subject to this Court's specific and general personal jurisdiction because Defendant is a Delaware corporation.

5. Without limitation, on information and belief, within this state, Defendant has used the patented inventions thereby committing, and continuing to commit, acts of patent infringement alleged herein. In addition, on information and belief, Defendant has derived revenues from its infringing acts occurring within Delaware. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in Delaware. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within Delaware. Defendant has committed such purposeful acts and/or transactions in Delaware such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, Defendant is incorporated in Delaware. Under the patent venue analysis, Defendant resides only in this District. On information and belief, from and within this District Defendant has committed at least a portion of the infringements at issue in this case.

7. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

III. COUNT I
(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,191,607)

8. Plaintiff incorporates the above paragraphs herein by reference.

9. On February 20, 2001, United States Patent No. 6,191,607 ("the '607 Patent") was duly and legally issued by the United States Patent and Trademark Office. The '607 Patent is titled

"Programmable Bus Hold Circuit and Method of Using the Same." A true and correct copy of the '607 Patent is attached hereto as Exhibit A and incorporated herein by reference.

10. Forutome is the assignee of all right, title and interest in the '607 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the '607 Patent. Accordingly, Forutome possesses the exclusive right and standing to prosecute the present action for infringement of the '607 Patent by Defendant.

11. The invention in the '607 Patent relates to the field of computer input/output devices and circuits that reduce input/output bus contention in such devices. (*Id.* at col. 1:5-8).

12. The '607 patent explains the problems with conventional ways of preventing bus contention in input/output buses in conventional input/output ("I/O") devices in computer systems. The conventional I/O devices are often required to quickly drive I/O buses that are connected to I/O pins in order to meet various timing requirements. (*Id.* at col. 1:11-14). The I/O devices are typically equipped with output drivers that have high signal switching strengths in order to meet the various timing requirements. (*Id.* at col. 1:14-16). When an output driver is turned offer, there is a potential problem with the bus. (*Id.* at col. 1:16-17). A user may pull the bus either high or low with external circuitry that may cause excessive noise due to may outputs switching simultaneously. (*Id.* at col. 1:17-20). A conventional solution to this problem of preventing bus contention is to add a bus hold circuit, for example configured as a weak latch. (*Id.* at col. 1:20-22).

13. Bus hold circuits reduce the bus noise level; however, bus hold circuits are not always needed or desirable. (*Id.* at col. 1:23-24). For example, if an application requires that multiple I/O pins be tied together, a number of individual bus hold circuits associated with these pins may consume a large amount of operating current. (*Id.* at col. 1:25-28). As a result, a voltage

level held by multiple bus hold circuits may tend to be more difficult to override. (*Id.* at col. 1:28-30). Some users may also wish to purchase I/O devices that are not constructed with bus hold circuits because of the expected cost savings which may result. (*Id.* at col. 1:30-32). In such a situation it would be cost prohibitive for a manufacturer to produce two identical devices with one version having bus hold circuits and another without such circuits. (*Id.* at col. 1:35-36). The inventors therefore invented an improved bus hold circuit and methods for using the improved bus hold circuit such as a programmable bus hold circuit including a tri-state buffer, for example, one that is under control of a memory cell or other programmable bit capable of enabling or disabling the programmable bus hold circuit. (*Id.* at col. 1:45-49).

14. Figure 1 of the '607 patent is a non-limiting example of a programmable bus hold circuit (600) including a tri-state buffer (604):

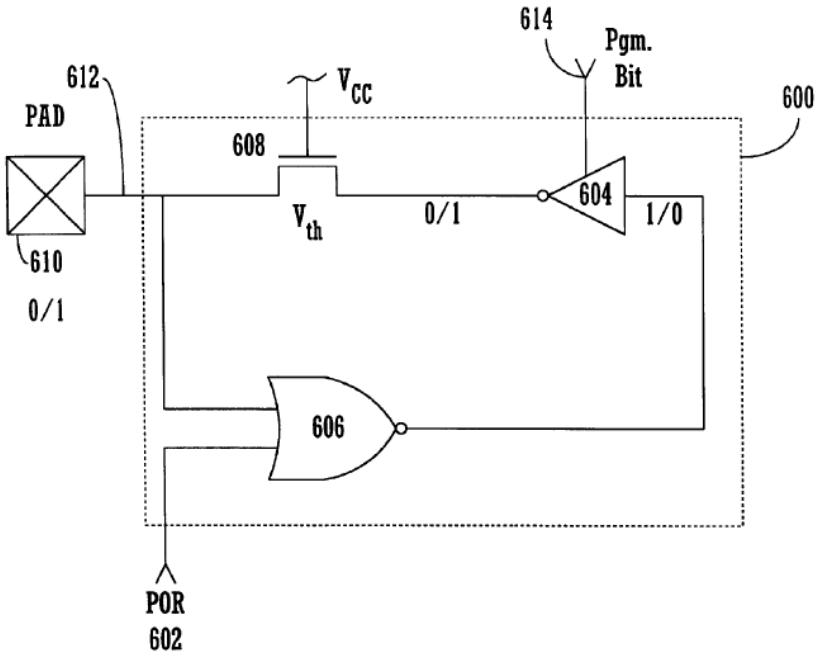


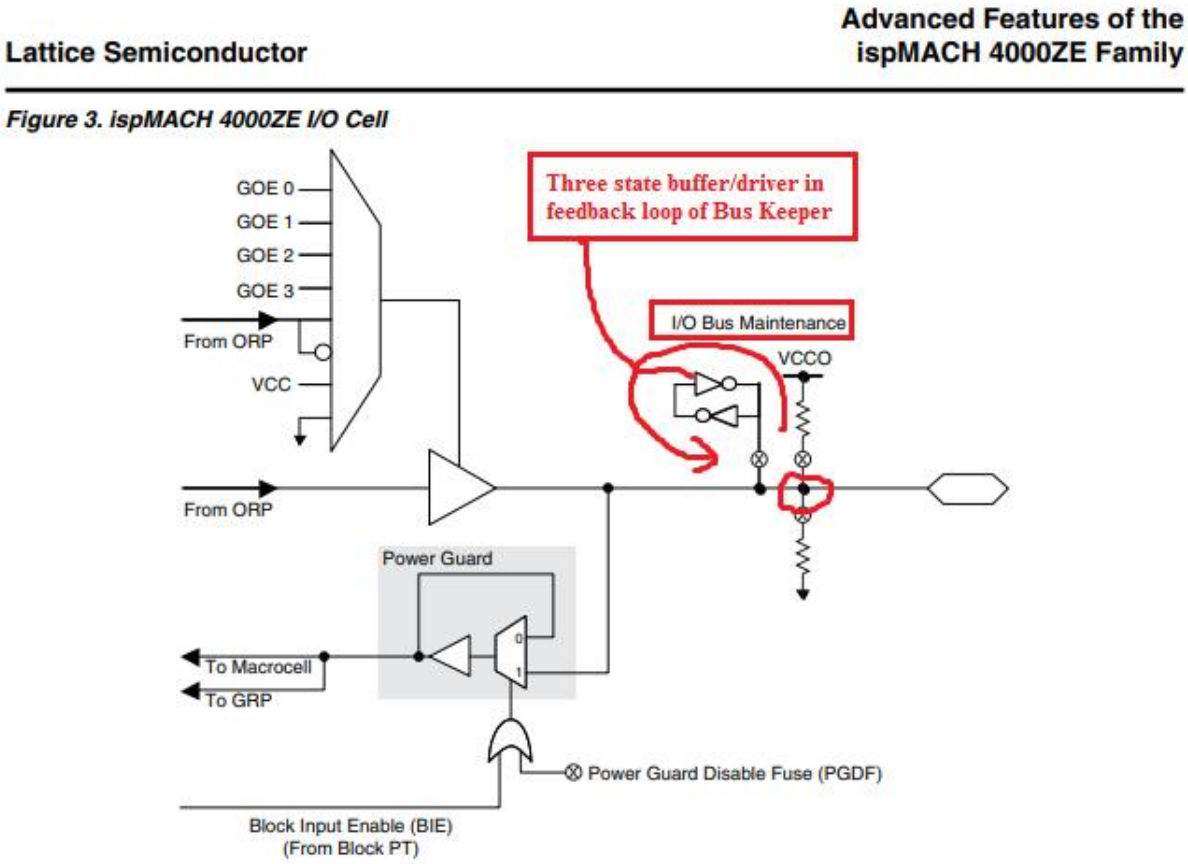
FIGURE 1

(*Id.* at col. 2:36-37; Fig. 1). The tri-state buffer (604) is under the control of a programmable bit (614), which is coupled to the control input of the buffer. (*Id.* at col. 2:44-46). The programmable bit may be used to activate or deactivate the buffer. (*Id.* at col. 2:46-47). In Figure 1, the programmable bus circuit is arranged as a programmable feedback path associated with an output of the circuit. (*Id.* at col. 2:55-57). Figure 2 of the '607 patent is a non-limiting example of a tri-state buffer controlled by a programmable bit and suitable for use in a bus hold circuit. (*Id.* at col. 2:58-64; Fig. 2).

15. **Direct Infringement.** Upon information and belief, Defendant has been directly infringing at least claim 12 of the '607 patent in Delaware, and elsewhere in the United States, by performing actions (including through testing and demonstrations) comprising at least performing the method comprising programming a tri-state buffer included as part of a feedback path of a bus hold circuit to hold or tri-state a voltage at an input/output pad through using at least the ispMACH 4000ZE ("Accused Instrumentality") (e.g., https://web.archive.org/web/20160208234352/http://latticesemi.com/en/Products/FPGAandCPLD/ispMACH4000ZE.aspx#_215D66708B2C4BFFAFE0846737AB0490; http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

16. The Accused Instrumentality practices the claimed method by using a bus keeper circuit in a processor that includes a programmable tri-state buffer that is included as part of the feedback path of the bus keeper circuit to hold or tri-state a voltage (e.g., a high impedance state and values previously held by an I/O) at an input/output pad. (e.g.,

https://web.archive.org/web/20160208234352/http://latticesemi.com/en/Products/FPGAandCPLD/ispMACH4000ZE.aspx#_215D66708B2C4BFFAFE0846737AB0490; http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135). For example, in the Accused Instrumentality has a tristate buffer included as part of a feedback path of a bus hold circuit:



(*E.g.*, https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/

Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

> In situations where the host's bus parking mechanism is not available, it's time to make use of the pull-up/down and Bus Hold functions available in most modern CPLDs. As with most devices in its class, the I/O pins of the Lattice ispMACH 4000ZE CPLD are equipped with selectable pull-up and pull-down resistors that can be used to provide the appropriate logic level during a standby state (Figure 3). The 4000ZE series is also equipped with a power-saving Bus Keeper function (also know as Bus Hold), a weak active driver circuit that can be set at either an active one or zero while drawing much less power than a simple resistor. *A note of caution: While the Bus Keeper function offers significant power savings, care must be taken to make sure it's the only active device on the line or you run the risk of turning it into a large current sink.*
>
> 5 Practical Low Power CPLD Design
> A Lattice Semiconductor White Paper

(E.g., http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; *also* https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135). The tristate buffer included in the feedback path of the bus hold circuit is programmed to hold or tri-state a voltage at an input/output pad:

> **Individual I/O Bus Maintenance**
>
> The ispMACH4000ZE I/Os have individual programmable I/O bus maintenance options. The four options for the I/O are programmable pull-up, pull-down, bus keeper and off. The I/O bus maintenance can be set using the ispLEVER Constraints Editor or using the HDL attribute PULL set to either "UP", "DOWN", "HOLD", or "OFF".
>
> 6
>
> The circuit can be programmed to act as Bus hold/bus keeper circuit

(https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

17. Upon information and belief, Defendant has been directly infringing at least 14 of the '607 patent in Delaware, and elsewhere in the United States, by performing actions comprising making, using, selling, and/or offering for sale a product including bus hold circuit, comprising a feedback path including a programmable tri-state buffer coupled to an output of the circuit in at least the ispMACH 4000ZE ("Accused Instrumentality") (*e.g.*, https://web.archive.org/web/20160208234352/http://latticesemi.com/en/Products/FPGAandCPLD/ispMACH4000ZE.aspx#_215D66708B2C4BFFAFE0846737AB0490; http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

18. The Accused Instrumentality comprises a bus hold circuit (e.g., Bus keeper circuit), comprising a feedback path including a programmable tri-state buffer (e.g., programmable buffer of the bus keeper circuit in the accused product) coupled to an output of the circuit (e.g., output pad). (*e.g.*, http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; https://web.archive.org/web/20160208234352/http://latticesemi.com/en/Products/FPGAandCPLD/ispMACH4000ZE.aspx#_215D66708B2C4BFFAFE0846737AB0490; https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?docum

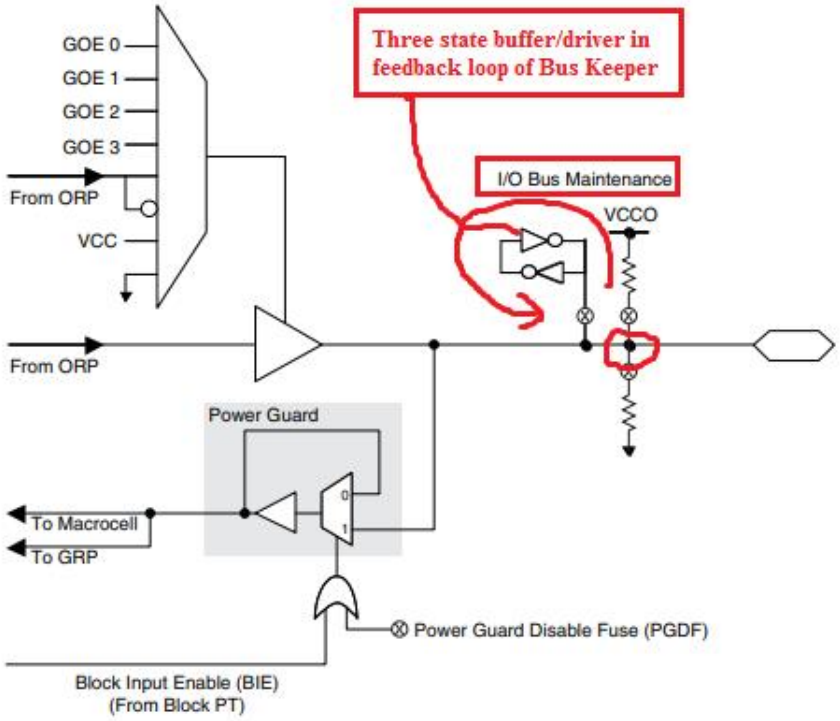
ent_id=29135). For example, in the Accused Instrumentality the bus keeper circuitry contains a tristate buffer which is programmed to allow the circuitry to act as Bus Keeper:

> In situations where the host's bus parking mechanism is not available, it's time to make use of the pull-up/down and Bus Hold functions available in most modern CPLDs. As with most devices in its class, the I/O pins of the Lattice ispMACH 4000ZE CPLD are equipped with selectable pull-up and pull-down resistors that can be used to provide the appropriate logic level during a standby state (Figure 3). The 4000ZE series is also equipped with a power-saving Bus Keeper function (also know as Bus Hold), a weak active driver circuit that can be set at either an active one or zero while drawing much less power than a simple resistor. *A note of caution: While the Bus Keeper function offers significant power savings, care must be taken to make sure it's the only active device on the line or you run the risk of turning it into a large current sink*.
>
> 5 Practical Low Power CPLD Design
> A Lattice Semiconductor White Paper

(*E.g.*, http://file.elecfans.com/web1/M00/20/B4/ooYBAFmk0aSABwUSAAIlM1QcYro087.pdf; *also* https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

19. As shown below, the bus keeper circuit contains a feedback path that includes a programmable tristate buffer coupled to an output of the circuit:

Figure 3. ispMACH 4000ZE I/O Cell



(https://web.archive.org/web/20170314154409/http://www.latticesemi.com/~/media/LatticeSemi/Documents/ApplicationNotes/AD/AdvancedFeaturesoftheispMACH4000ZEFamily.PDF?document_id=29135).

Individual I/O Bus Maintenance

The ispMACH4000ZE I/Os have individual programmable I/O bus maintenance options. The four options for the I/O are programmable pull-up, pull-down, bus keeper and off. The I/O bus maintenance can be set using the ispLEVER Constraints Editor or using the HDL attribute PULL set to either "UP", "DOWN", "HOLD", or "OFF".

The circuit can be programmed to act as Bus hold/bus keeper circuit

(*Id.*).

20. Plaintiff has been damaged as a result of Defendant's infringing conduct. Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '607 patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

21. On information and belief, Defendant has had at least constructive notice of the '607 patent by operation of law and marking requirements have been complied with.

IV. JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of United States Patent No. 6,191,607 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;

d. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein;

e. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein;

h. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

June 28, 2021

CHONG LAW FIRM, P.A.

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CERTIFICATE OF SERVICE

I hereby certify that on June 28, 2021, I electronically filed the above documents with the Clerk of Court using CM/ECF which will send electronic notification of such filings to all registered counsel.

/s/ Jimmy Chong
Jimmy Chong (#4839)